

KVision

Variant: [No Variations]

13/01/2018
V1I2

DRAFT

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

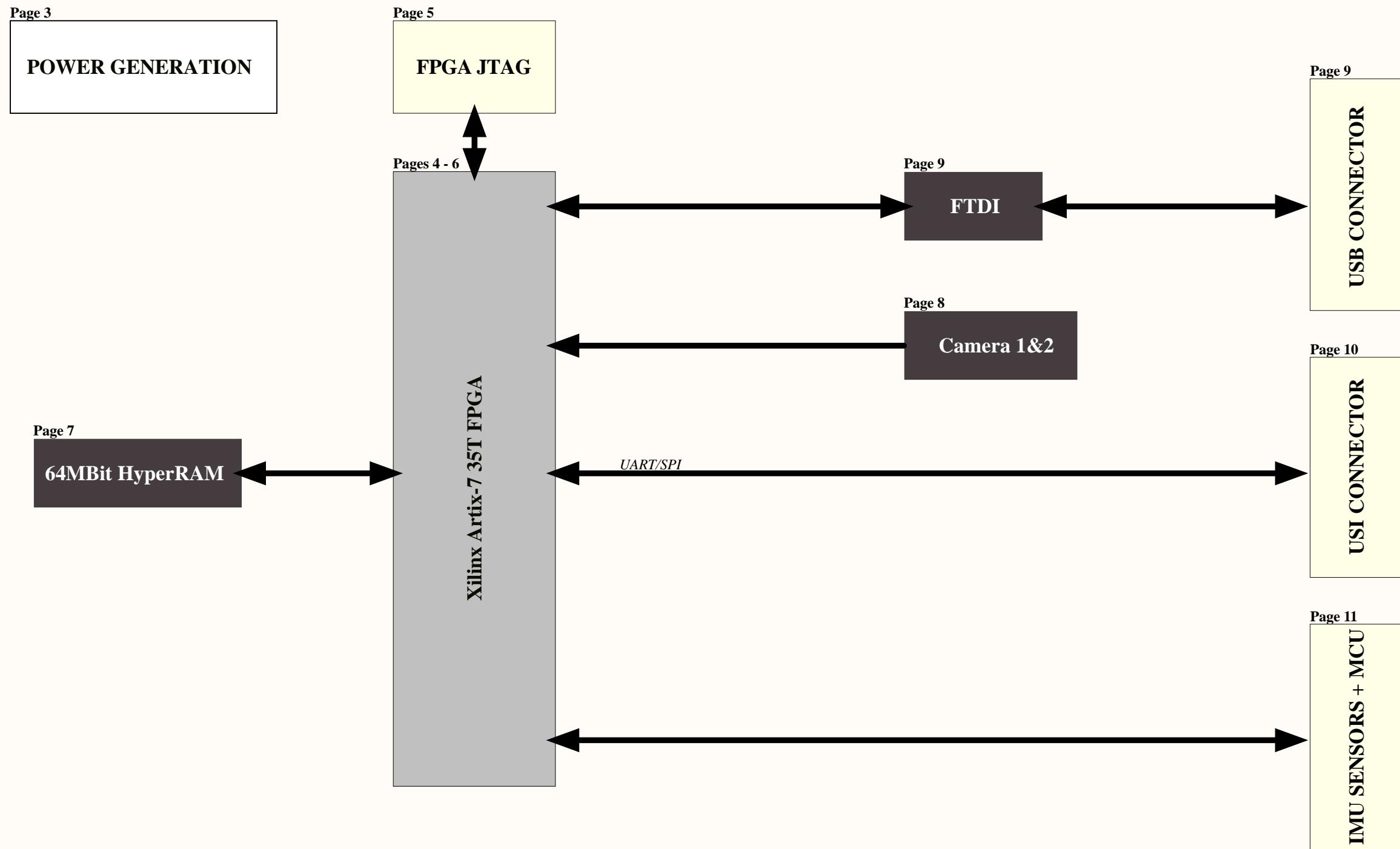
DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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(Block Diagram)

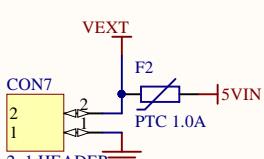
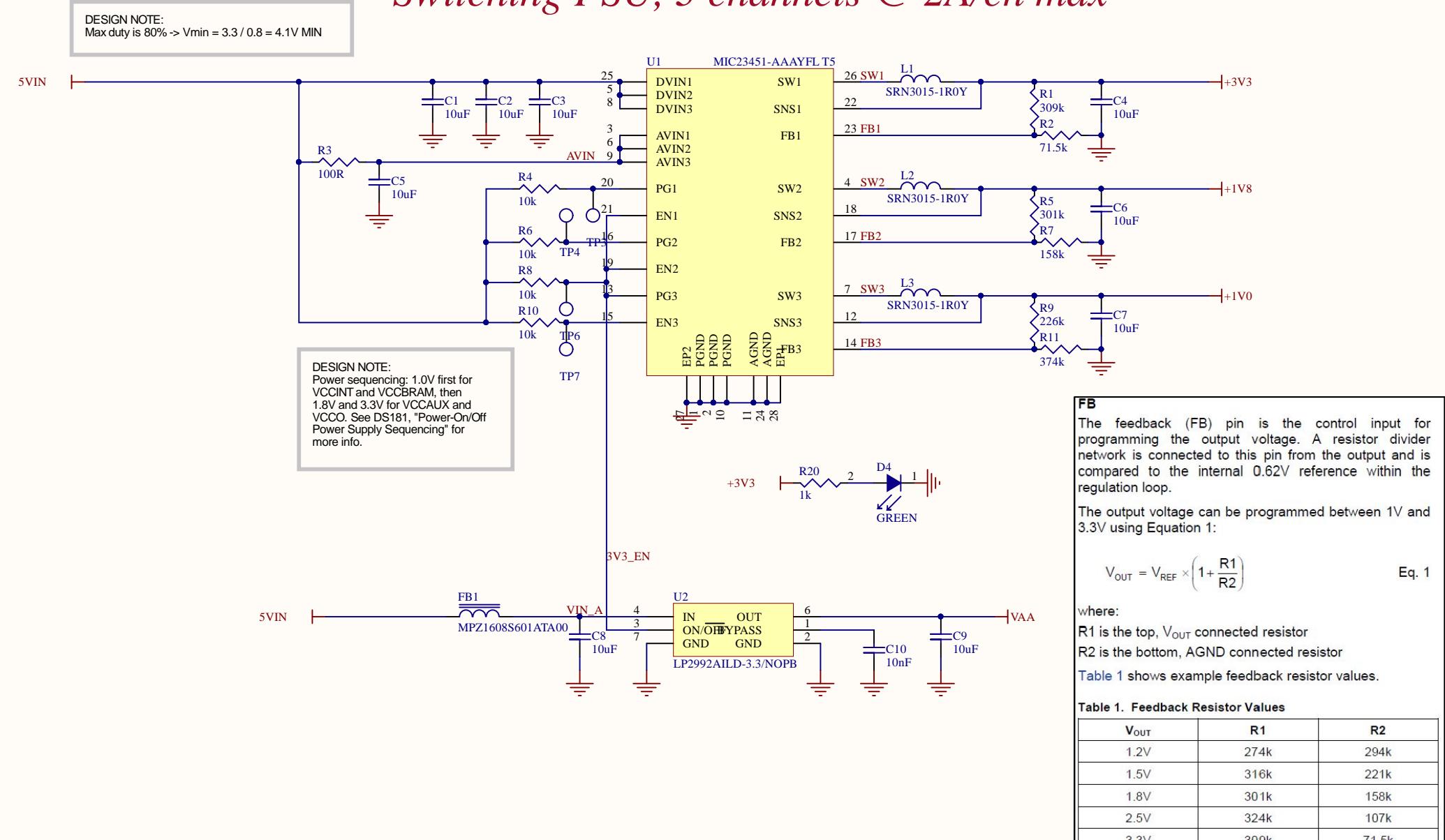


CLOCKS/PLL & PCI

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Power

Switching PSU, 3 channels @ 2A/ch max

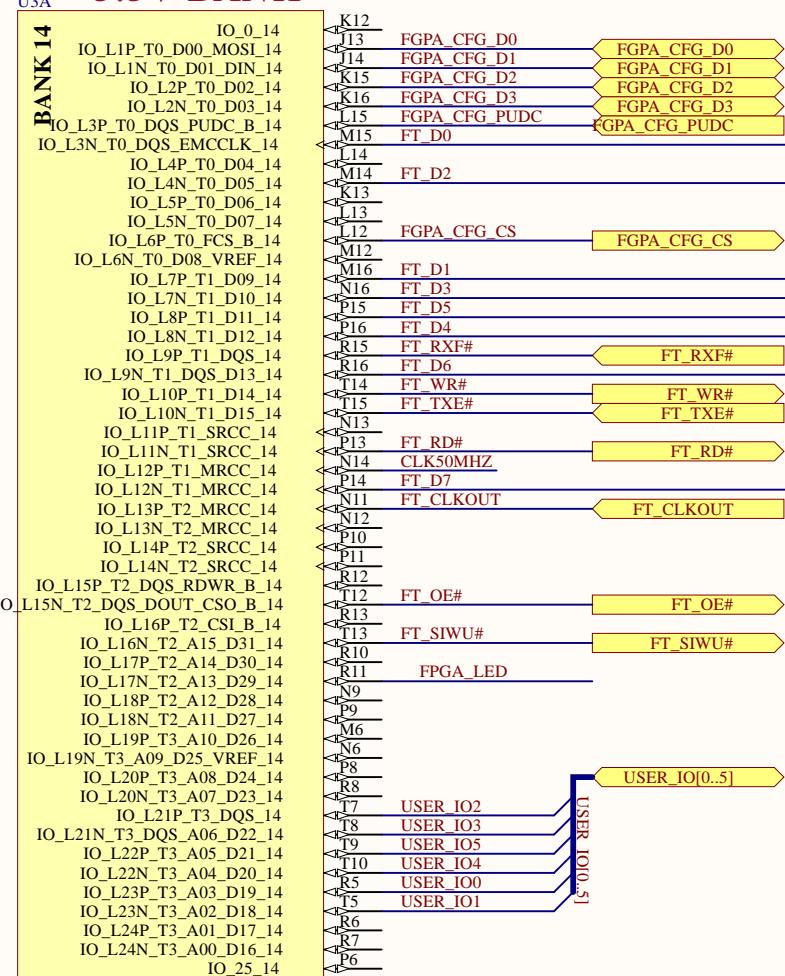


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FPGA

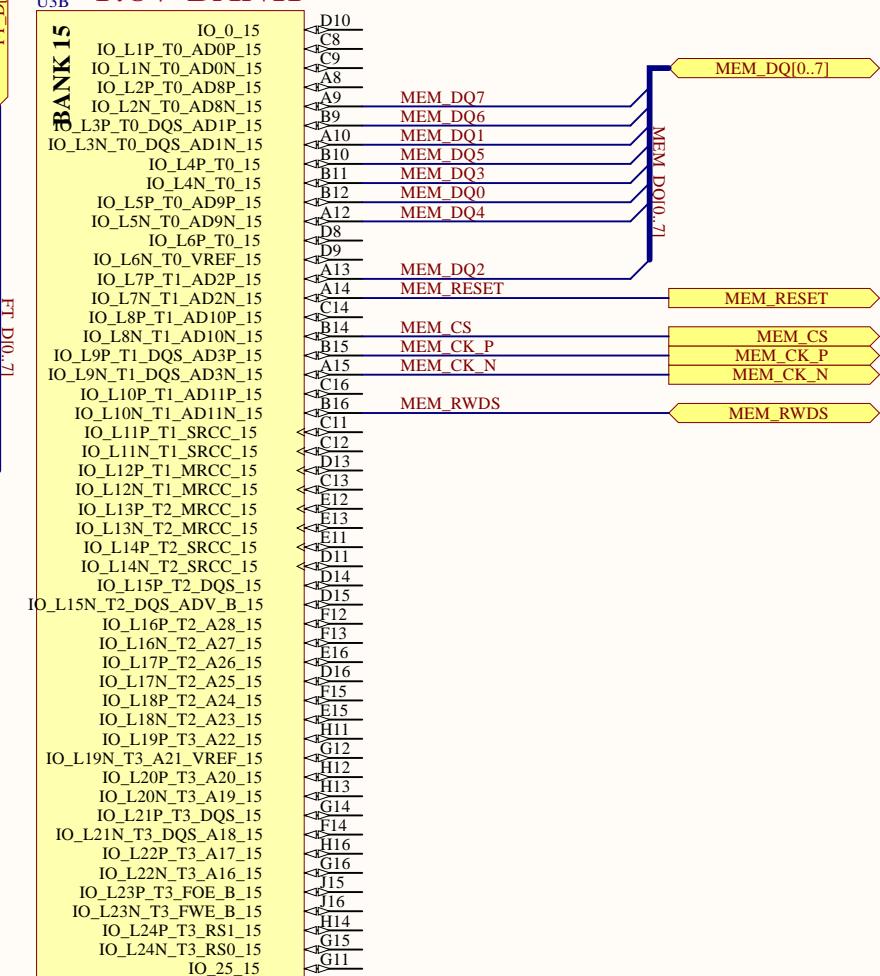
FPGA Communication

3.3V BANK



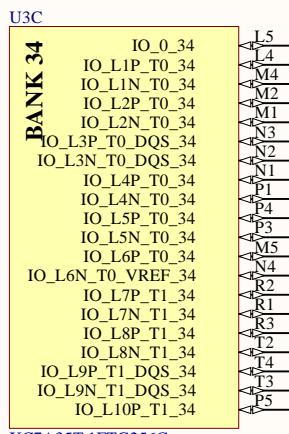
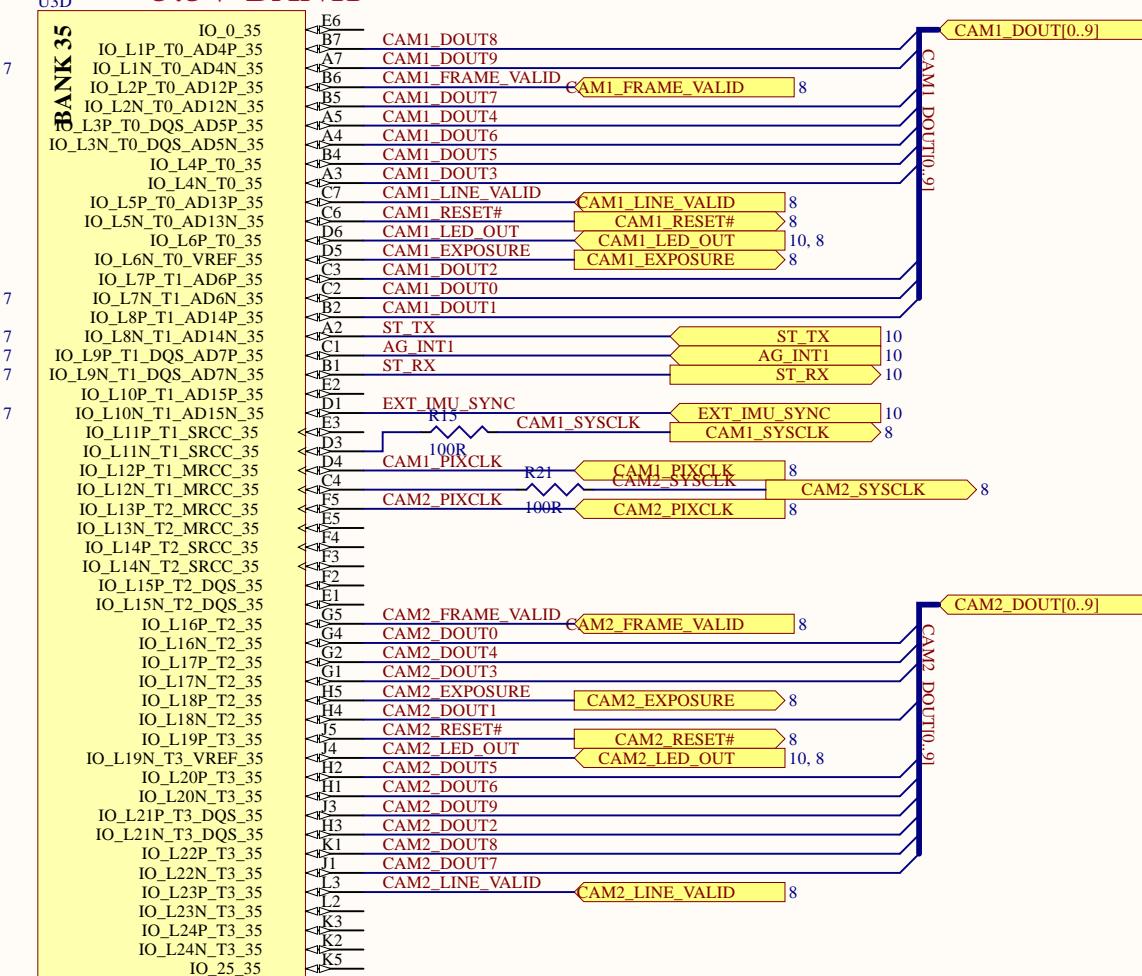
Memory Interface

1.8V BANK

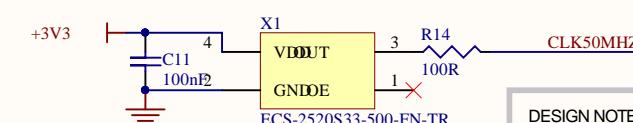


Camera Interface

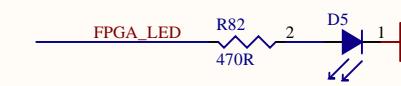
3.3V BANK



Clock Generation: 50 MHz



DESIGN NOTE:
Optional series termination in case
there is ringing on the clock line.

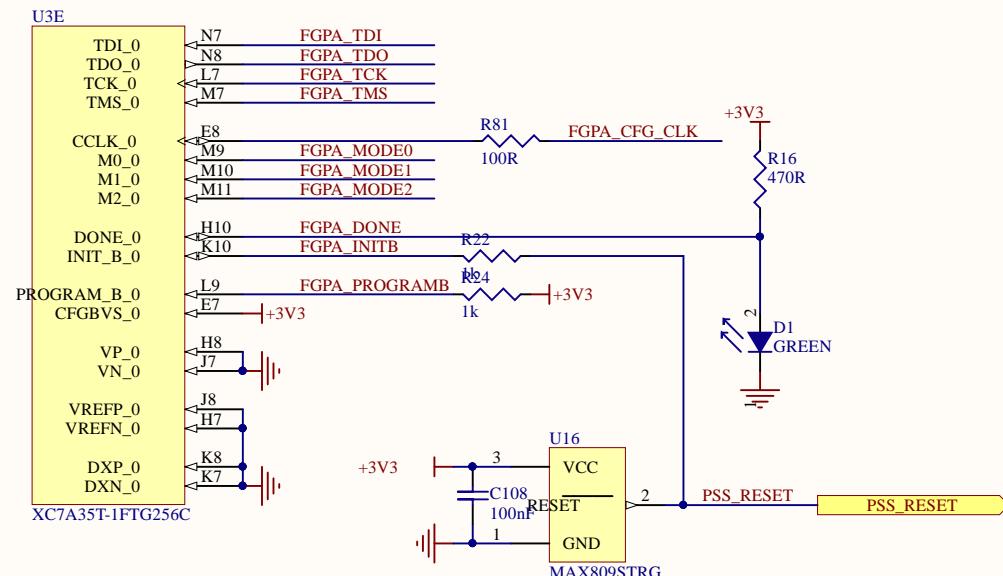


LAYOUT NOTE:
The termination resistors should
be placed close to the source.

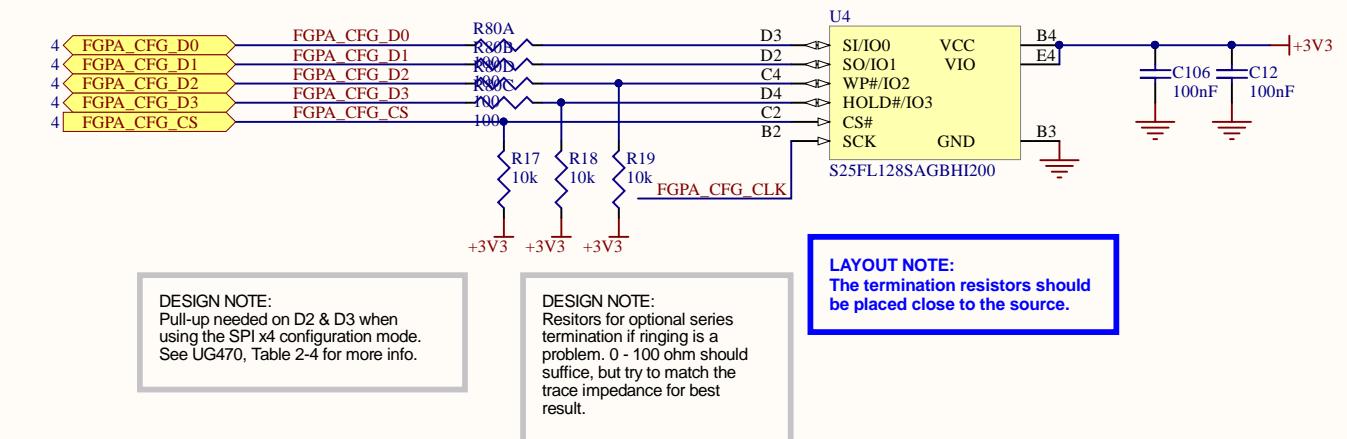
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FPGA Configuration

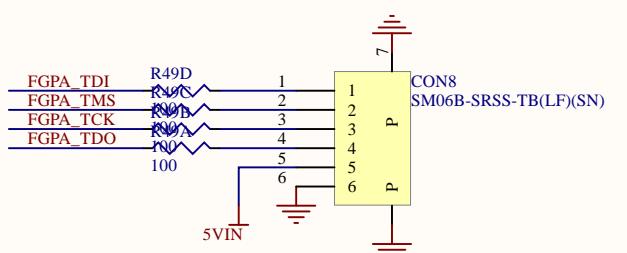
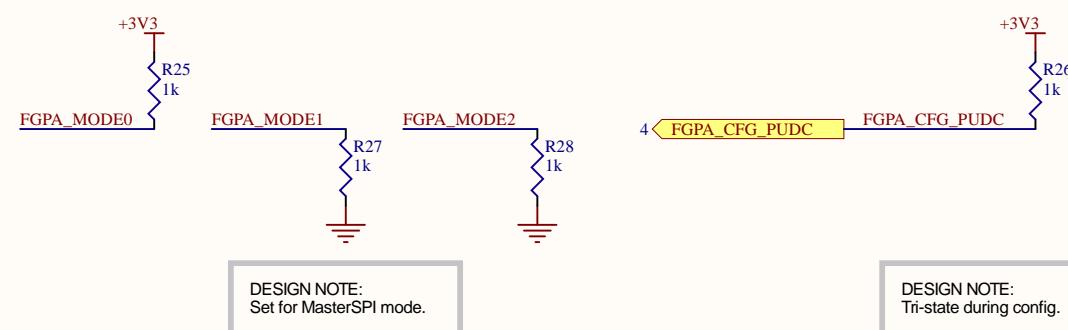
JTAG / Modes



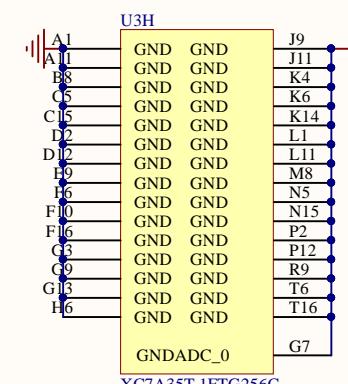
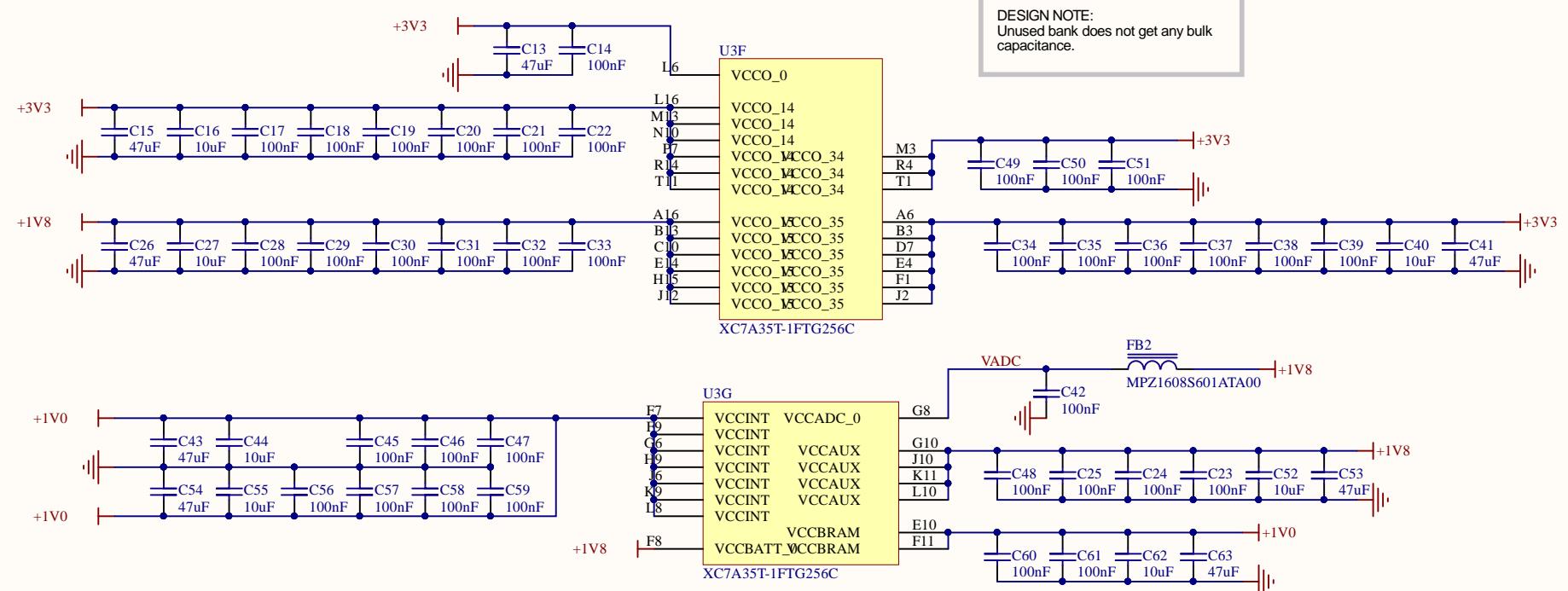
128MBit Configuration Flash



JTAG



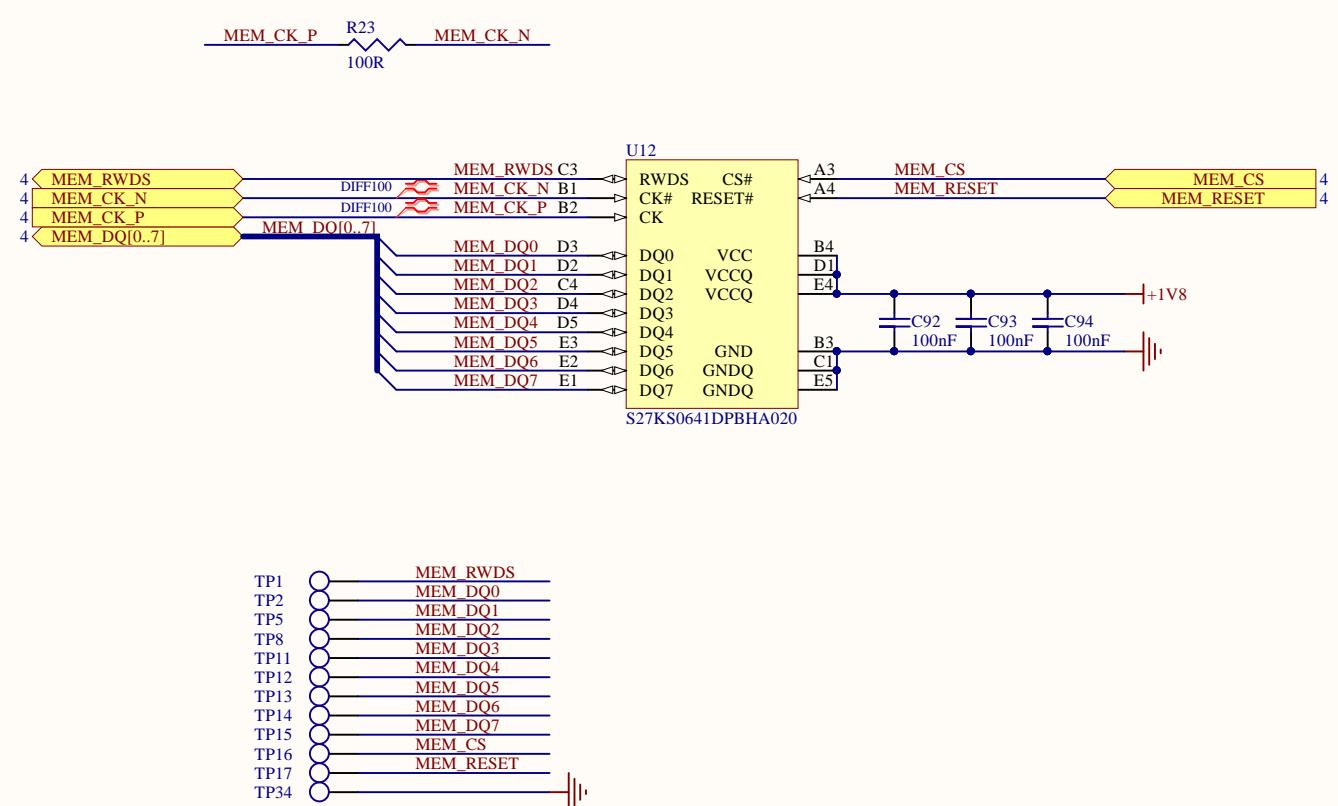
FPGA Power



CLOCKS/PLL/PDIO

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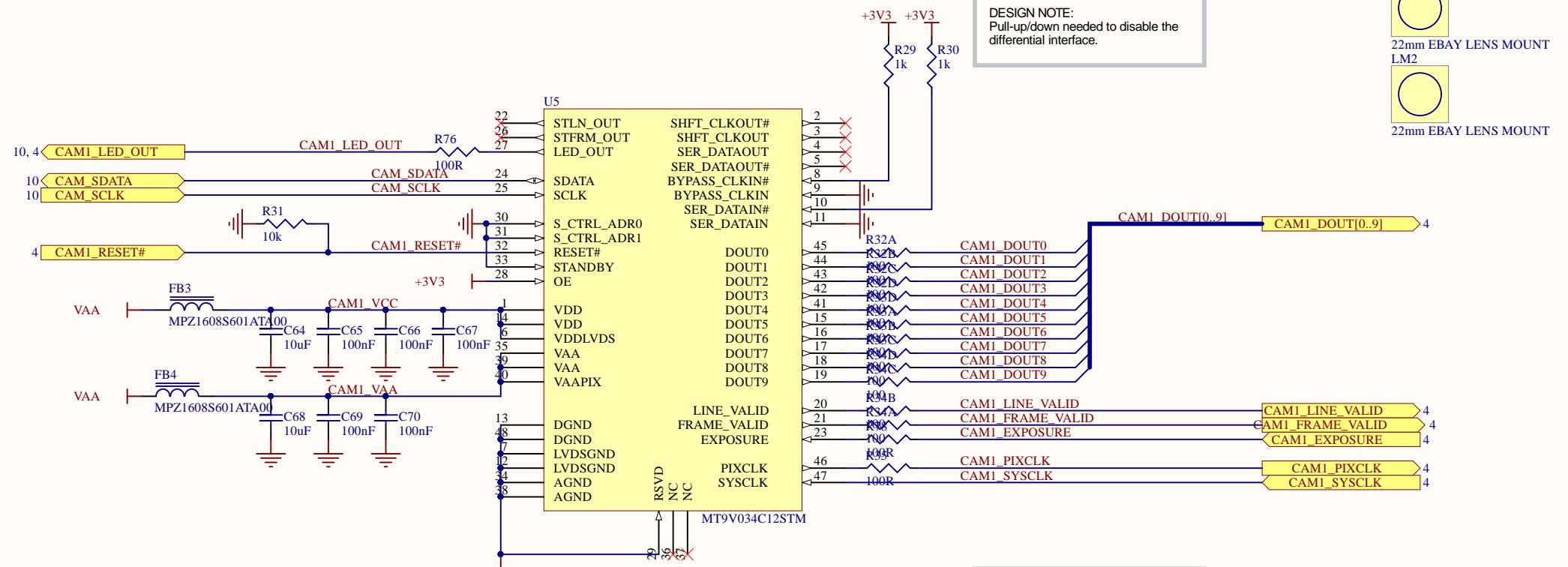
Memory



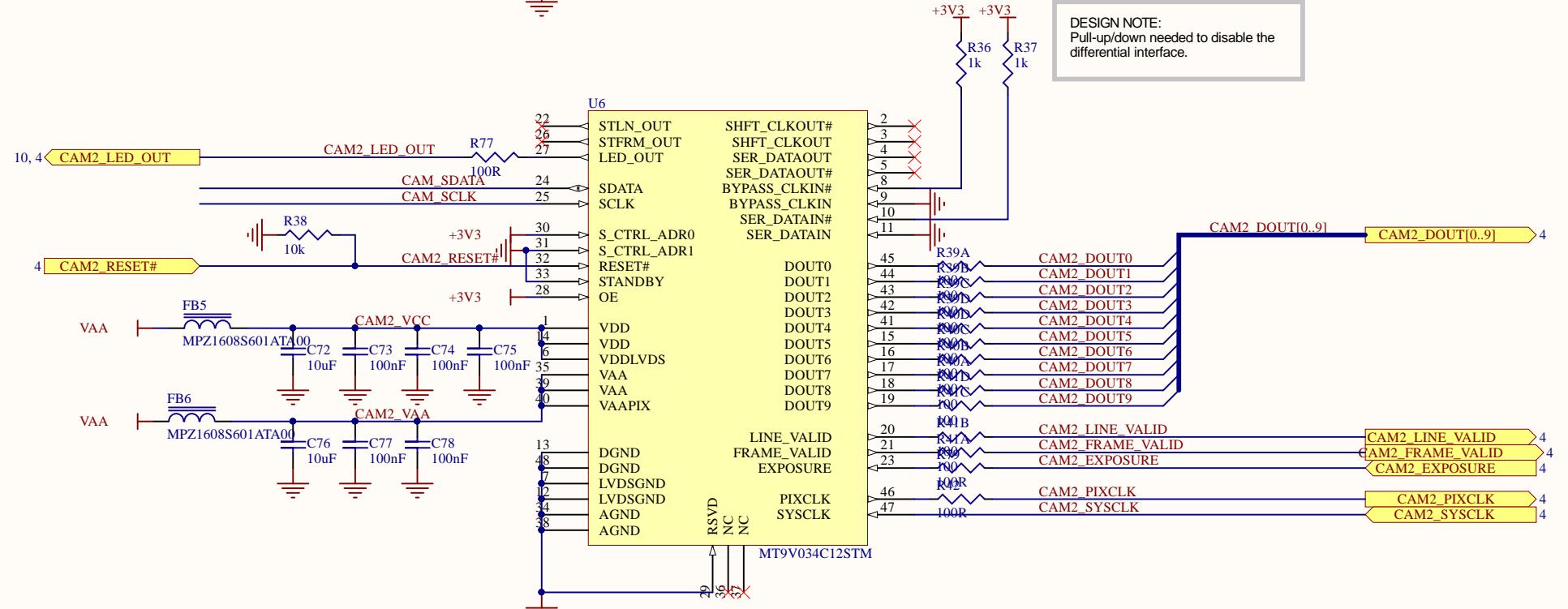
CLOCKS/PINS/PIN

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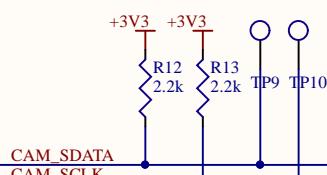
Image Sensor



DESIGN NOTE:
Pull-up/down needed to disable the differential interface.

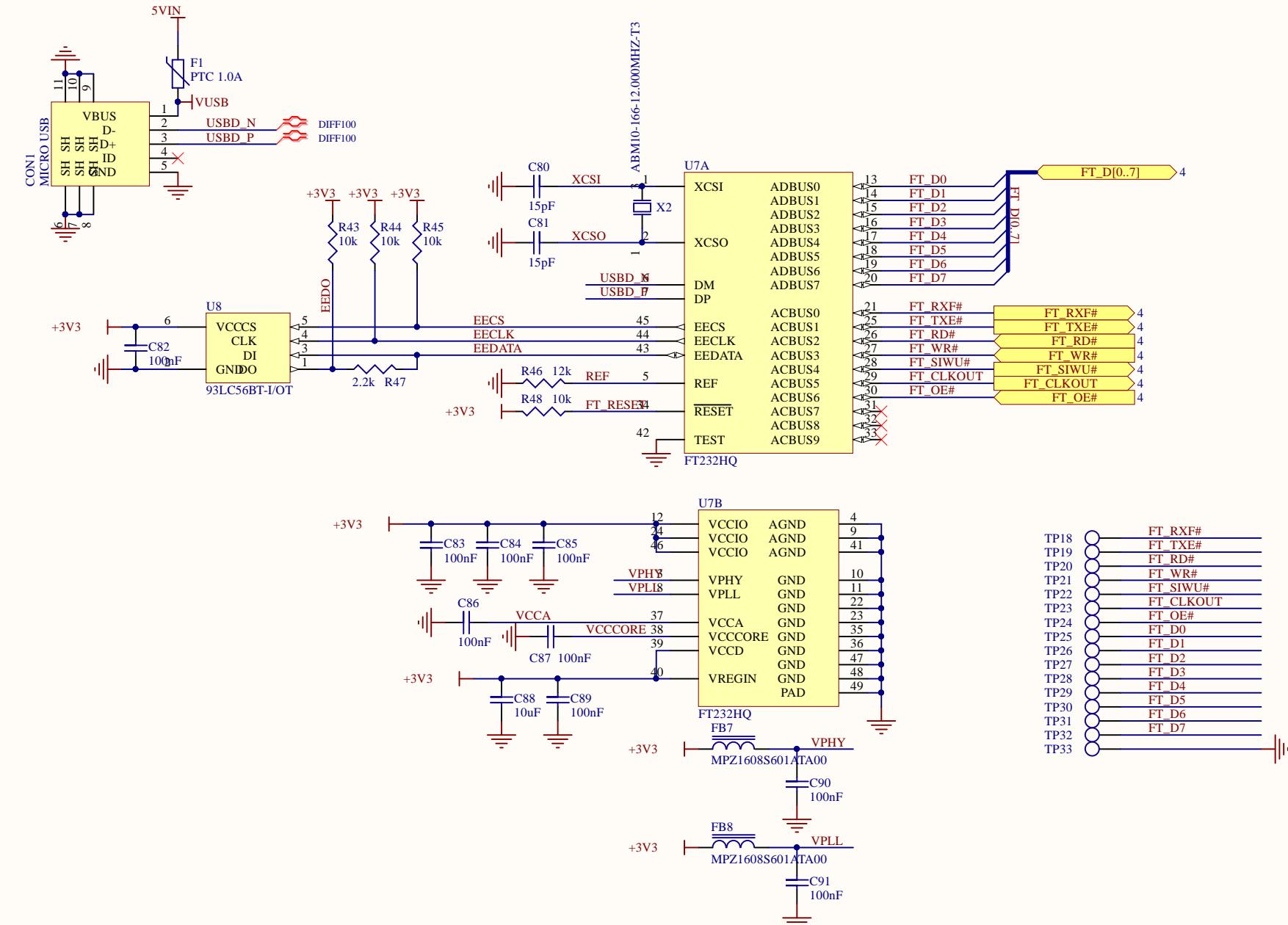


DESIGN NOTE:
Pull-up/down needed to disable the differential interface.



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FTDI Interface

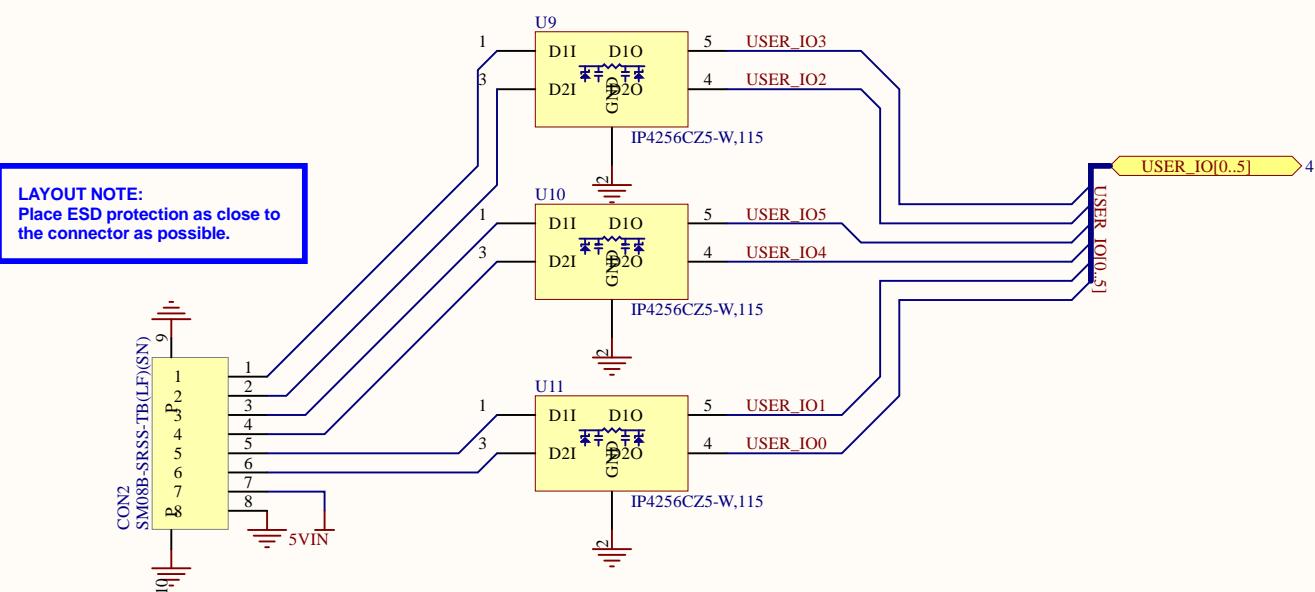


CLOCKS/PLL/PDN

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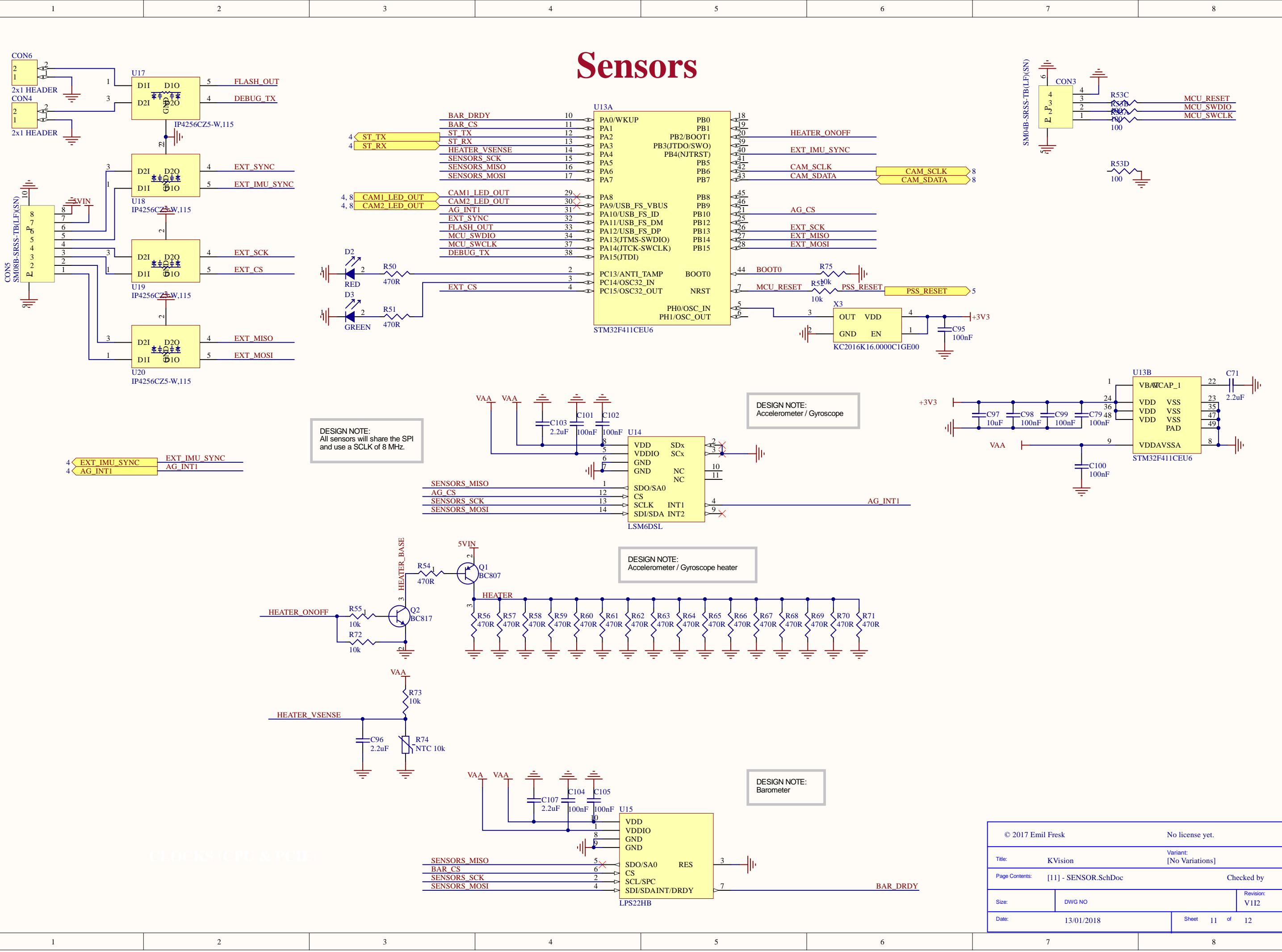
Connectors

I/O Connector



CLOCKS/PURPOSE

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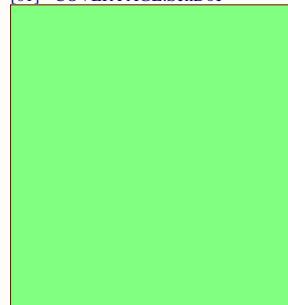
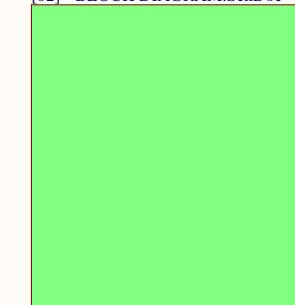
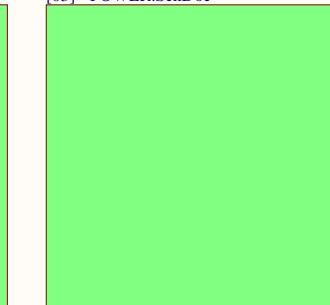
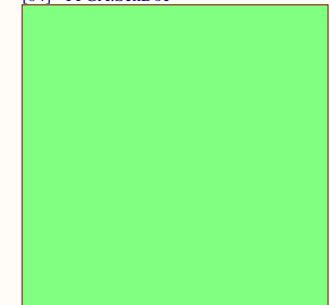
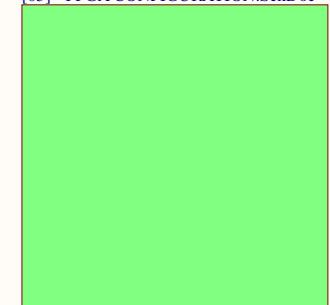
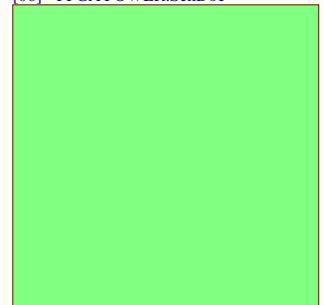
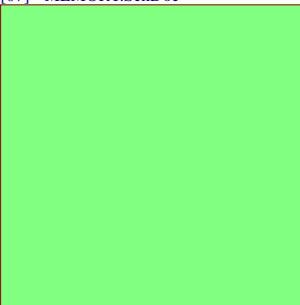
DOC: Revision History

Rev. B

- Fixed error in MEMORY clock P/N being swapped
- Fixed IMU interrupt signals direction on FPGA schematic
- Moved all clock inputs to _P pins
- Added termination on memory clock
- Added testpoints for memory & FT232
- Updated lensholder holes to slots to fit 22 and 21mm hole spacing
- Moved camera power supply

CLOCKS(PINS & PINS)

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Designator
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[04] - FPGA.SchDocDesignator
[05] - FPGA CONFIGURATION.SchDocDesignator
[06] - FPGA POWER.SchDocDesignator
[07] - MEMORY.SchDoc

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as

NF

Net Class Example



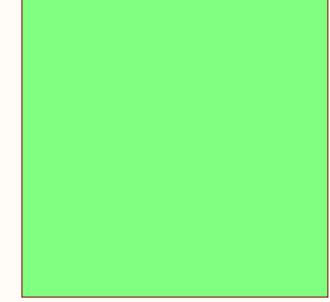
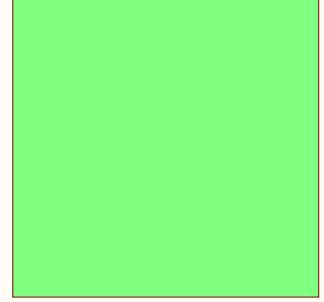
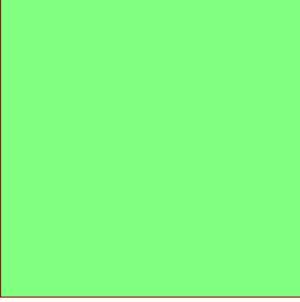
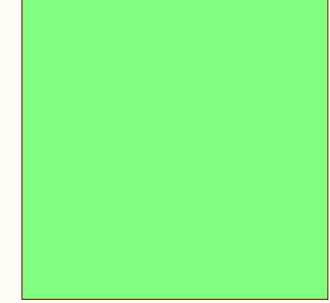
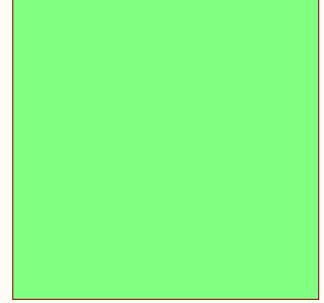
Differential signal example



TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE*Peripheral / Group of component title**Smaller Title*

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.**PRELIMINARY** - Close to final schematic.**CHECKED** - There should not be any mistakes. Tell the engineer if you find one.**RELEASED** - A board with this schematic has been sent to production.Designator
[08] - IMAGE SENSOR.SchDocDesignator
[09] - FTDI.SchDocDesignator
[10] - CONNECTORS.SchDocDesignator
[11] - SENSOR.SchDocDesignator
[XX] - DOC REVISION HISTORY.SchDoc

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