Prasanna Korlapati

Graduate Student · Portland State University
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Education

Portland State University **Jun 24**
Master of Science, Electrical and Computer Engineering **GPA: 3.7**
SRKR Engineering College **Jun '18**
Bachelor of Engineering, Electrical and Communication Engineering **GPA: 3.5**

Coursework and Certifications

System Verilog	Microprocessor System Design	ASIC
Computer Architecture	Front End Management of new product Development	Project Management

Skills

Languages	: Verilog, System Verilog, OOP concepts, C++ , Python
Protocols	: MESI, MSI, MOESI
Tools	: ModelSim, Vstudio, Eclipse, Mentor Graphics - Questa Sim, Xilinx - Vivado
Operating System	: Windows, Linux, Ubuntu
Verification Methodology	: System Verilog Assertions- SVA, Constraint Randomization
Other Tools etc...	: Product Quality Analysis, Debugging product flow,Confluence, Jira,Grafana,SLA and KPI

Work Experience

TCS (Telia) **Sep '18 - Dec '21**

System Engineer

- Worked on developing and testing multiple functional test scenarios in different phases of product implementation.
- Experienced in utilizing Python scripting to automate repetitive activities and enhance workflow efficiency, saving time and money.
- Worked in different roles as a Product Quality Analyst, Wiki JIRA administrator, and Team lead.
- Expertise in various testing methodologies, including functional, regression, integration, and performance verification and validation.
- Maintained close to 6 dev,pre-prod environments up to date with production and received appreciation from clients on many occasions.
- Worked on data visualization tools such as Grafana and Icinga to check the order flow, user login count, Availability of product, and load(CPU, Memory, Disc, etc..) on machines.

Academic Projects

Design and Verification of a I2C(communication protocol) based memory subsystem using SystemVerilog

- Designed and implemented I2C protocol between functional unit and memory subsystem. Implemented Assertions and OOPS concepts as a part of verification process.

Design and Simulation of Split L1 Cache using MESI protocol using System Verilog

- Implement a split L1 cache with N way set associativity for a 32-bit processor and Reporting the statistics on cache misses, hits, reads, writes, and hit ratio.

Automating compilation of scripts using Python

- Identifying directories with similar naming patterns and organizing them by grouping them into a separate directory and Compiling and executing the code using the scripting.

Strategic Planning of a product Business development| Market analysis, Competitor identification etc...

- Worked with a Helmet manufacturing company(NOMO) and analyzed and provided Strategic planning that would help the company to become a major player in the industry.