Printed Circuit Board(PCB) Design Checklist

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Details

Catalog	No.	Details	Record
Rounting	1	All traces have been routed.	
	2	No exposed traces or vias under metal cased or similar poorly insulated parts. Better to make these area clear (as keep-out area).	
	3	Use large diameter vias for these traces connect to power/ground plane.	
	4	Check 3W rule for these differential, high speed data or other sensitive signals.	
	5	The minimum width of the traces connected to IC power/ground pins are 6mil (recommend width is 8mil). Keep these trace as short as possible. i.e., connect IC power/ground pins to the power/ground plane through via where nearest possible.	
	6	Use mitered 45 degree bend instead of 90 degree bend where trace changes direction.	
	7	No traces under crystal/oscillator, transformer, opticalcoupler, and power supply model.	
Silk screen	8	All parts should have reference designator values. Designator text should be visible when components are installed.	
	9	Mark pin1 on connectors, pin headers, ICs, crystals, and any other components where pin1 is not readily identifiable.	
	10	No silkscreen text over vias (if vias not soldermasked), pads or holes.	
	11	The polarity of these polarized component (e.g., cap, diode, LED) should be indicated. This should be visible when component is installed.	

	12	Switches, jumpers or LEDs are labeled with their functions.	
	13	All designator texts read in one or two directions (left to right, or top to bottom).	
	14	PCB information shown on silkscreen layer (name, version, data, logo,etc.)	
Part placement /foot print	15	All components should be placed with an appropriate functional group.	
	16	Print 1:1 scale PCB file, check the footprint by placing the component on it.	
	17	These components which need to be at the fixed position (could be connector, display, switch, button,ect.) have been placed properly.	
	18	Component spacing restriction has been checked (Details are here).	
	19	No parts in keep-out area.	
	20	Heavy components (e.g., coils, transformers) placed near PCB holder or the edge.	
	21	I/O drivers should near where their signals leave the board.	
	22	Board to board connectors (or pin headers) placed near to the edge of PCB.	
High speed trace /signal integrity	23	Series-matching/damping resistors should be close to source side. Termination resistors should be close to target pins.	
	24	One single trace should not change characteristic impedance value over its length.	
	25	These traces, which end to end length are longer than 1/6 of the rising time, is recommended to do signal integration simulation (with simulation tool).	
	26	Bypass capacitors placed close to IC power pins. Each pin have one local bypass cap.	
	27	Digital and analog parts are placed separately. Digital parts on digital ground (DGND) and analog parts on analog ground (AGND). Put a ferrite bead between analog and digital ground to reduce interference.	
	28	Keep clock traces as straight and short as possible. Minimize the number of vias in clock transmission lines.	
	29	High speed singles design rule check (termination, impedance, reference plane, EMI, multi-points connection topology,etc.).	
	30	Run the differential traces as closely as possible after they leave the source parts.	
	31	Minimize the number of vias over these high speed differential traces.	
	32	The lengths between the differential traces should be the same.	
	33	PCB layer stackup (multilayer PCB) has been properly setup in achieving the best possible electrical performance.	
Design for manufacture	34	Perform DRC check to ensure the design meets manufacturing capabilities (Details are here).	
	35	On power/ground plane, distribute the via density about the available space as evenly as possible.	

	36	On one single trace, in the case the trace width need to be changed (this normally happens on the traces from small chips, BGAs or fine pitch component pins), the increased/decreased width at one place should not larger than the thinnest trace width. For example, if the trace need change from 8mil to 24mil, use a piece of 16mil trace as transition wire.	
	37	No Trace/via/pad within 20mil around non-plating holes at inner layers. This value changes to 12mil for outer layers.	
	38	For these chip components (0805 and smaller package), ensure the trace width is the same on both side of .	
	39	Keep at least 8mil between adjecent copper pours.	
Design for assembly	40	Three global fiducial marks should be located on PCB that contain components to be mounted with automated machine.	
	41	All Fine Pitch or BGA package footprints need two local fiducial marks if automated machine used for fitting them.	
	42	The global fiducial marks should be located at the corner area (3.0mm to 5.5mm distance to the edge) or the frame of the panel (see a sample here).	
	43	The recommended size for fiducial mark is 1.0mm.	
	44	Keep clear within 3.0mm around the fiducial marks.	
	45	Finished hole sizes are at least 10mils larger than the fitting leads (Thru-hole parts).	
	46	For SMT pads, the length are at least 8mil longer than pins' length (4mil each side). The width should be at least equal to pads' width.	
	47	Aligning/mechanical holes are recommended to be non-plated. In the case plating aligning/mechanical holes are used ensure don't expose the pads on soldering side. Otherwise peelable ink should be used in wave soldering process (cost increased).	
	48	No trace/via/pad within 1.5mm around the mechanical holes. This value increases to 3.0mm if the screw/washer are conductive (metal material) one.	
	49	Better to have reference designator value for each mechanical hole. This information is helpful in assembly process.	
	50	All via/hole under BGAs should be filled and covered by solder mask. PCB manufacturers normal do this by default.	
	51	No via/hole on the pads of these components populated with reflow machine. Keep solder-masked via/hole at least 15mil away from the pads. This value increase to 20mil, if the via/hole are exposed one.	

	52	On component side, no parts within 3.0mm area to plug sockets (or pin headers). No components and pads under these sockets (or pin headers) on the soldering side.	
	53	Thermal relief pad used for these pads which could have cold solder joint issue (e.g., power/ground pins of through-hole parts).	
Design for test	54	Test pads/vias have added on these important signals. These pads/vias should not be placed within 5mm of the edge.	
	55	Test vias are exposed.	
	56	JTAG header included on board (connected to JTAG pins of devices) where possible.	
Thermal analysis	57	Thermal considerations require that the component density be distributed about the available board space as evenly as possible.	
	58	For these high power dissipation parts (e.g., FET,LDO,DC/DC module), make enough copper coverage on all the layers. Also thermal vias (plated thru-holes) are needed under the package.	
	59	Locate these temperature-sensitive components (e.g., electrolytic cap, oscillator) away from hot part (e.g., transformer, heat sink).	
	60	Thermal land (exposed copper area directly underneath the body of the hot component.e.g., LDO) should not covered by solder mask.	
EMC and ESD	61	Crystal case should be flush to the PCB and grounded.	
	62	These circuit protection parts (e.g., PTC thermistor, TVS diode) close to the parts/sockets being protected.	
	63	For multilayer PCBs, check 20H rule for power and ground plane.	
	64	No isolated shapes on power/ground plane.	
	65	Hatched copper pour (12mil trace and 20mil pitch) rather than solid copper pour where possible.	
	66	Avoid small copper area and sharp shape area as this may act as antennae and emit noise.	
Power Integrity	67	Minimizing the current loop in power supply design. If the board power is supplied by switch mode, the switching parts (e.g., FET, inductor, diode,capactor) should be as close as possible.	
	68	Check the current capability. A practical rule: 1oz copper weight: 1A/mm width. Use this link to perform temperature rise vs trace width analysis.	