17 data transfer between cpu and main memory.

> Processore 110 - Data transfer between OPU and I/o modale,

some avithmetic ore logical on data. > Data processing -> Contral.

-> Alteration of or sequence of operations. - Carrier data - there is no dittetenopestatione > Comb mation of above. of the precession must acceps Instruction Cycle: - to writer down grand sount > Instruction featch (if) Address Bus --> Instruction operation decoding (iod) > operand address calculation (oac) -> operand fetch (of) > Data operation (do) -) Operand storce (05). System Bus: - A bus that connects major computer components is called a system bus. - Data bus. -> control bus, so of a base of the -7 Address bus.

Data bus : practically shope

> It is a bidirectional Bus.

> Data can flow in both direction.
> Usually a multiple of 8. 8, 16, 32, 64.

-> Carries data: - there is no difference between data

-> The processor must access the memory module tuice dwing each instruction eycle.

Address Bus: - carones memory address of the instructions which one to be executed.

> unidirectional.

> The number of locations that the cour address

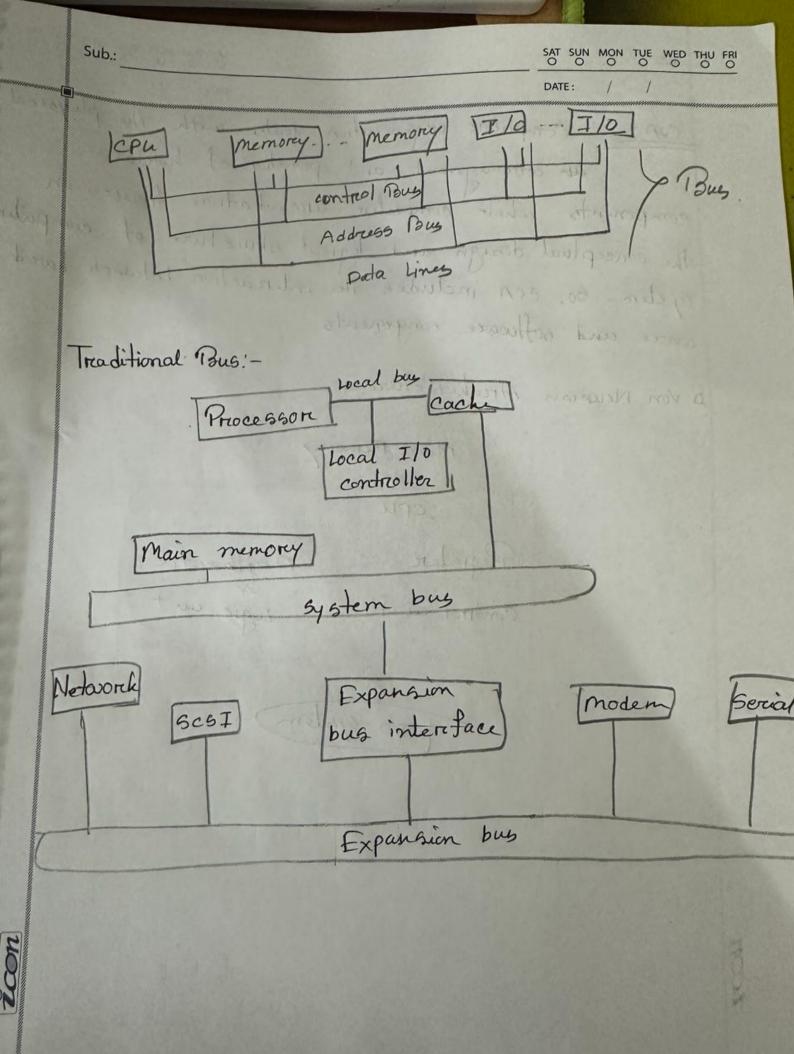
is determine by the number of address lines.

Control Bus:

It carries timing and control signals generated by the cou that we used to synchronize operation of the individual microconquier elements.

) It can carry many different signals. -> I/o Read, I/o write, but of

-) Memory Read, memory write,



COA:- Computer organization deals with the physical an aveaugment and operation of hardware components, while computer anchitecture focuses on the conceptual design and logical structure of computer System. So, coa includes the interaction between hard ware and software components. Traditional Bus D Von Neuman Arichitecture: Processon I main memory Control unit Logie unit (Register) T/o system 1000 Exparision bus

Sub.: