Selçuk Köse
Department of Electrical Engineering, 813.974.6636 (phone)
University of South Florida, kose@usf.edu
4202 E. Fowler Ave., ENB118, Tampa, Florida 33620 http://www.eng.usf.edu/∼kose

Research Interests

- **Research interests:** On-chip voltage regulation; Power management; Hardware security; 3-D integration; Green computing

Education

- **University of Rochester** Rochester, NY
  Doctor of Philosophy in Electrical and Computer Engineering *March 2008 - June 2012*
  Dissertation: High Performance Power Delivery in Nanoscale Integrated Circuits
- **University of Rochester** Rochester, NY
  Master of Science in Electrical and Computer Engineering *September 2006 - March 2008*
- **Bilkent University** Ankara, Turkey
  Bachelor of Science in Electrical and Electronics Engineering *September 2001 - May 2006*

Work Experience

- **University of South Florida** Tampa, FL
  Assistant Professor, Electrical Engineering Department *August 2012 - Current*
- **University of Rochester** Rochester, NY
  Research Assistant, High Performance Integrated Circuit Design Laboratory *September 2007 - June 2012*
- **Freescale Semiconductor** Tempe, AZ
  Graduate Intern, Microwave and Mixed-Signal Laboratory *May 2010 - August 2010*
- **Eastman Kodak Company** Rochester, NY
  Graduate Intern, CMOS Image Sensors R&D Laboratory *May 2009 - June 2009*
- **Intel Corporation** Santa Clara, CA
  Graduate Intern, Central Technology and Special Circuits Team *May 2008 - August 2008*
- **Intel Corporation** Santa Clara, CA
  Graduate Intern, Central Technology and Special Circuits Team *May 2007 - August 2007*
- **The Scientific and Technological Research Council of Turkey** Ankara, Turkey
  Part-Time Engineer, VLSI Design Center *March 2006 - June 2006*
- **NanoMagnetics Instruments** Ankara, Turkey
  Technical Intern *June 2005 - August 2005*

Awards

- USF Faculty Outstanding Research Achievement Award, 2017
  – The most prestigious award for research achievements at USF. Only 17 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2017

- USF Outstanding Faculty Award, 2016

  – Only 10 researchers (out of over 1700 faculty members) received this prestigious university-wide award in 2016

- Cisco Research Award, 2015, 2016 & 2017
- National Science Foundation CAREER Award, 2014

  – National Science Foundation's most prestigious award in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education and the integration of education and research within the context of the mission of their organizations

- USF College of Engineering Outstanding Junior Research Achievement Award, 2014

  – Only one assistant professor received this prestigious award in 2014

- Turkiye Is Bankasi *Golden Youth Award* for outstanding success in University Entrance Exam

  – **12**th over 1.5 million candidates, Turkey, 2001

- Full scholarship and stipend awarded by Bilkent University, Ankara, Turkey, 2001-2006
- Awarded with Abroad Undergraduate Education Fellowship by Turkish Government, Turkey, 2001

Sponsored Research

Total funds: ***$1,160,000*** Personal share: ***$1,055,000***

- **NSF/SRC joint SaTC/STARSS award (sole PI)** $370,000
  SaTC: STARSS: Small: Combined Side-channel Attacks and Mathematical Foundations of Combined Countermeasures *2017 - 2020*

- **Cisco Research Award (PI: Kose & Co-PI: Chen)** $80,000*
  Reconfigurable Voltage Regulation for Security and Efficiency *2017 - 2018*
  *Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.

- **I4 Corridor Matching Grant (sole PI)** $50,000
  On-Chip Voltage Regulation in an Advanced Technology *2016 - 2017*

- **Cisco Research Award (PI: Kose & Co-PI: Chen)** $80,000**
  On-Chip Voltage Regulation in an Advanced Technology *2016 - 2017*
  **Cisco also covers the fabrication cost of a test chip at 28 nm FDSOI technology.

- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI: Kose & Co-PI: DeMara)** $50,000
  Trusted IoT using Cross-layer Leveraging of Reconfigurable Device Signatures *2016 - 2017*

- **Cisco Research Award (sole PI)** $30,000
  On-Chip Voltage Regulation in an Advanced FDSOI Process *2015 - 2016*

- **Florida Center for Cybersecurity (FC^2) Seed Grant (PI: Kose & Co-PI: DeMara)** $50,000
  Aging-Aware Hardware-Trojan Detection at Runtime *2015 - 2016*

- **National Science Foundation CAREER award (sole PI)** $450,000
  CAREER: Regulator-Gating (ReGa): A New On-Chip Power Delivery Architecture *2014 - 2019*

Publications

Books

B1. I. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *On-Chip Power Delivery and Management, Fourth Edition*, Springer, 2016, ISBN # 978-3319293936.

B2. R. Jakushokas, M. Popovich, A. V. Mezhiba, **S. Köse**, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors, Second Edition*, Springer, 2011, ISBN # 978-1-4419-7870-7.

– Chinese translation by China Machine Press, 2014, Chinese ISBN # 978-7-111-44929-4

Journals

J1. M. H. Yilmaz, **S. Köse**, N. Chamok, M. Ali, and H. Arslan , "Partially Overlapping Filtered Multitone with Reconfigurable Antennas in Uncoordinated Networks," *Physical Communication*, (accepted on August 8^{th}, 2017).

J2. W. Yu and **S. Köse**, "False Key-Controlled Aggressive Voltage Scaling: A Countermeasure Against LPA Attacks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, (accepted on March 9^{th}, 2017).

J3. W. Yu and **S. Köse**, "Exploiting Voltage Regulators to Enhance Various Power Attack Countermeasures," *IEEE Transactions on Emerging Topics in Computing*, (accepted on October 15^{th}, 2016).

J4. L. Wang, S. K. Khatamifard, O. A. Uzun, U. R. Karpuzcu, and **S. Köse** , "Efficiency, Stability, and Reliability Implications of Unbalanced Current Sharing among Distributed On-Chip Voltage Regulators," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 11, pp. 3019 – 3032, November 2017 .

J5. W. Yu and **S. Köse**, "A Lightweight Masked AES Implementation for Securing IoT Against CPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 64, No. 11, pp. 2934 – 2944, November 2017.

J6. W. Yu and **S. Köse**, "Security-Adaptive Voltage Conversion as a Lightweight Countermeasure Against LPA Attacks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 7, pp. 2183 - 2187, July 2017.

J7. W. Yu and **S. Köse**, "A Voltage Regulator-Assisted Lightweight AES Implementation Against DPA Attacks," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 63, No. 8, pp. 1152 - 1163, August 2016.

J8. W. Yu and **S. Köse**, "Charge-Withheld Converter-Reshuffling (CoRe): A Countermeasure Against Power Analysis Attacks," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 63, No. 5, pp. 438 - 442, May 2016.

J9. W. Yu and **S. Köse**, "Security Implications of Simultaneous Dynamic and Leakage Power Analysis Attacks on Nanoscale Cryptographic Circuits," *IET Electronics Letters*, Vol. 52, Issue 6, pp. 466 - 468, March 2016.

– Featured as the *Interview* article of the March issue of the IET Electronics Letters.

J10. W. Yu and **S. Köse**, "Time-Delayed Converter-Reshuffling: An Efficient and Secure Power Delivery Architecture," *IEEE Embedded Systems Letters*, Vol. 7, No. 3, pp. 73 - 76, September 2015.

J11. I. Vaisband,B. Price, **S. Köse**, Y. Kolla, E. G. Friedman, and J. Fischer, "Distributed Power Delivery with 28 nm Ultra-Small LDO Regulator," *Analog Integrated Circuits and Signal Processing*, Vol. 83, Issue 3, pp. 295 - 309, March 2015.

J12. I. Vaisband, M. Azhar, E. G. Friedman and **S. Köse**, "Digitally Controlled Pulse Width Modulator for On-Chip Power Management," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 22, No. 12, pp. 2527 - 2534, December 2014.

J13. O. Uzun and **S. Köse**, "Converter-Gating: A Power Efficient and Secure On-Chip Power Delivery System," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 2, pp. 169 - 179, June 2014.

J14. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "Active Filter Based Hybrid On-Chip DC-DC Converters for Point-of-Load Voltage Regulation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 21, No. 4, pp. 680 - 691, April 2013.

J15. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Noise in TSV-Based 3-D Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 48, No. 2, pp. 587 - 597, February 2013.

J16. **S. Köse** and E. G. Friedman, "Distributed On-Chip Power Delivery," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, Vol. 4, No. 4, pp. 704 - 713, December 2012.

J17. **S. Köse** and E. G. Friedman, "Efficient Algorithms for Fast IR Drop Analysis Exploiting Locality," *Integration, the VLSI Journal*, Vol. 45, No. 2, pp. 149 - 161, March 2012.

J18. **S. Köse** and E. G. Friedman, "Effective Resistance of a Two Layer Mesh," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 58, No. 11, pp. 739 - 743, November 2011.

J19. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 19, No. 8, pp. 1458 - 1468, August 2011.

Conferences

C1. A. W. Khan, T. Wanchoo, G. Mumcu, and **S. Köse**, "Implications of Distributed On-Chip Power Delivery on EM Side-Channel Attacks," *Proceedings of the IEEE International Conference on Computer Design (ICCD)*, November 2017.

C2. B. Pekoz, **S. Köse**, and H. Arslan, "Adaptive Windowing of Insufficient CP for Joint Minimization of ISI and ACI Beyond 5G," *Proceedings of the IEEE Annual International Symposium on Personal, Indoor, and Mobile Radio Communications (PIMRC)*, October 2017.

C3. A. Roohi, R. Demara, L. Wang, and **S. Köse**, "Secure Intermittent-Robust Computation for Energy Harvesting Device Security and Outage Resilience," *Proceedings of the IEEE Conference on Advanced and Trusted Computing (ATC)*, August 2017.

C4. S. K. Khatamifard, L. Wang, W. Yu, **S. Köse**, and U. R. Karpuzcu, "ThermoGater: Thermally-Aware On-Chip Voltage Regulation," *Proceedings of the IEEE International Symposium on Computer Architecture (ISCA)*, pp. 120 - 132, June 2017.

C5. W. Yu and **S. Köse**, "A Lightweight AES Implementation Against Bivariate First-Order DPA Attacks," *Proceedings of the ACM Hardware and Architectural Support for Security and Privacy (HASP)*, pp. 1 - 7, June 2017.

C6. **S. Köse**, "Efficient and Secure On-Chip Reconfigurable Voltage Regulation for IoT Devices," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 369 - 374, May 2017.

C7. V. T. Alaparthy and **S. Köse**, "An Adaptive Senior Design Course with an Emphasis on Undergraduate Course Curriculum," *Proceedings of the IEEE International Conference on Microelectronics System Education*, pp. 59 - 62, May 2017.

C8. W. Yu and **S. Köse**, "Implications of Noise Insertion Mechanisms of Different Countermeasures Against Side-Channel Attacks," *Proceedings of the IEEE International Symposium on Circuits and Systems*, May 2017.

C9. **S. Köse**, L. Wang, and R. F. DeMara, "On-Chip Sensor Circle Distribution Technique for Real-Time Hardware Trojan Detection," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, March 2017.

C10. W. Yu, O. A. Uzun, and **S. Köse**, "Leveraging On-Chip Voltage Regulators as a Countermeasure Against Side-Channel Attacks," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2015.

C11. M. E. Belviranli, W. Yu, and **S. Köse**, "Ultra-Fine Grain Power Management at Datapath-Level: Fact or Fiction," *International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) WACI Session*, March 2015.

C12. O. Uzun and **S. Köse**, "Regulator-Gating Methodology With Distributed Switched Capacitor Voltage Converters," *Proceedings of the IEEE Computer Society Annual Symposium on VLSI*, pp. 13 - 18, July 2014.

C13. **S. Köse**, "Thermal Implications of On-Chip Voltage Regulation: Upcoming Challenges and Possible Solutions," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 1 - 6, June 2014.

C14. M. Azhar and **S. Köse**, "An Enhanced Pulse Width Modulator with Adaptive Duty Cycle and Frequency Control," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 958 - 961, June 2014.

C15. **S. Köse**, "Regulator-Gating: Adaptive Management of On-Chip Voltage Regulators," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 105 - 110, May 2014.

C16. **S. Köse**, I. Vaisband, and E. G. Friedman, "Digitally Controlled Wide Range Pulse Width Modulator for on-Chip Power Supplies," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2251 - 2254, May 2013.

C17. **S. Köse**, R. M. Secareanu, O. Hartin, and E. G. Friedman, "Current Profile of a Microcontroller to Determine Electromagnetic Emissions" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2650 - 2653, May 2013.

C18. **S. Köse** and E. G. Friedman, "Distributed Power Delivery for Energy Efficient and Low Power Systems," *Asilomar Conference on Signals, Systems, and Computers*, November 2012, **(invited paper)**.

C19. **S. Köse** and E. G. Friedman, "Design Methodology to Distribute On-Chip Power in Next Generation Integrated Circuits," *IEEE 27-th Convention of Electrical and Electronics Engineers in Israel*, November 2012, **(invited paper)**.

C20. **S. Köse** and E. G. Friedman, "Power Delivery in Heterogeneous Integrated Circuits," *IEEE CAS-FEST Workshop (in conjunction with ISCAS2012)*, May 2012, **(invited talk)**.

C21. **S. Köse**, S. Tam, S. Pinzon, B. McDermott, and E. G. Friedman, "An Area Efficient On-Chip Hybrid Voltage Regulator," *Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 398 - 403, March 2012.

C22. **S. Köse** and E. G. Friedman, "Fast Algorithms for IR Voltage Drop Analysis Exploiting Locality," *Proceedings of the IEEE/ACM Design Automation Conference (DAC)*, pp. 996 - 1001, June 2011.

C23. **S. Köse** and E. G. Friedman, "Distributed Power Network Co-Design with On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, June 2011.

C24. I. Savidis, **S. Köse**, and E. G. Friedman, "Power Grid Noise in TSV-Based 3-D Integrated Systems," *Government Microcircuit Applications and Critical Technology Conference (GOMACHTech)*, pp. 129 - 132, March 2011.

C25. **S. Köse** and E. G. Friedman, "Simultaneous Co-Design of Distributed On-Chip Power Supplies and Decoupling Capacitors," *Proceedings of the IEEE International SoC Conference*, pp. 15 - 18, September 2010.

C26. **S. Köse** and E. G. Friedman, "An Area Efficient Fully Monolithic Hybrid Voltage Regulator" *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2718 - 2721, May/June 2010.

C27. **S. Köse** and E. G. Friedman, "Fast Algorithms for Power Grid Analysis Based on Effective Resistance," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 3661 - 3664, May/June 2010.

C28. **S. Köse** and E. G. Friedman, "On-Chip Point-of-Load Voltage Regulator for Distributed Power Supplies," *Proceedings of the ACM/IEEE Great Lakes Symposium on VLSI*, pp. 377 - 380, May 2010.

C29. **S. Köse**, E. Salman, and E. G. Friedman, "Shielding Methodologies in the Presence of Power/Ground Noise," *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2277 - 2280, May 2009.

C30. **S. Köse**, E. Salman, Z. Ignjatovic, and E. G. Friedman, "Pseudo-Random Clocking to Enhance Signal Integrity," *Proceedings of the IEEE International SoC Conference*, pp. 47 - 50, September 2008.

Workshop Presentations

W1. I. Vaisband, **S. Köse**, I. Savidis, and E. G. Friedman, "On-Chip Power Delivery," University Technology Showcase, Rochester, New York, April 6, 2011.

Patents

P1. **S. Köse** and O. A. Uzun, "Secure Converter-Gating, Reconfiguration, and Regulation," US Patent 9,812,954, November 7, 2017.

P2. **S. Köse**, O. A. Uzun, and W. Yu, "Time Delayed Converter Reshuffling," US Patent 9,748,837, August 29, 2017.

P3. **S. Köse** and O. A. Uzun, "System and Method for Distributed Voltage Regulator-Gating," US Patent 9,372,490, June 21, 2016.

P4. **S. Köse** and E. G. Friedman, "A Digitally Controlled Wide Range Pulse Width Modulator," US Patent 9,007,140, April 14, 2015.

P5. **S. Köse** and O. A. Uzun, "System and Method for Voltage Regulator-Gating," US Patent 8,922,272, December 30, 2014.

Invited Talks

- Security Implications of Reconfigurable Voltage Regulators, Cybersecurity Research Symposium, Tampa, Florida, April 2017.
- Efficient and Secure On-Chip Power Delivery, Cisco Systems, San Jose, California, December 2016.

  – Invited speaker at the Cisco PI Summit
- Efficient and Secure On-Chip Power Delivery, Cukurova University, Adana, Turkey, July 2016.
- Efficient and Secure On-Chip Power Delivery, Istanbul Technical University, Istanbul, Turkey, June 2016.
- Ultra-Fine Grain Power Management at Datapath-Level: Fact or Fiction, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) WACI Session, Istanbul, Turkey, March 2015.
- Efficient and Secure On-Chip Power Delivery, IEEE Student Branch, University of South Florida, Tampa, Florida, March 2015.
- Design of Efficient and Trustworthy On-Chip Power Delivery Systems, Workshop on Energy-Secure System Architectures (ESSA) (In Conjunction with ISCA'14), Minneapolis, Minnesota, June 2014.
- Converter-Gating: An Efficient On-Chip Power Delivery Architecture, Intel Corporation, Santa Clara, California, June 2014.
- Converter-Gating: An Efficient On-Chip Power Delivery Architecture, Synaptics Austin Design Center, Austin, Texas, May 2014.
- Distributed On-Chip Power Delivery – On-going Research and New Directions, IBM T. J. Watson Research Center, Yorktown Heights, New York, April 2013.
- Distributed Power Delivery for Energy Efficieny and Low Power Systems, Asilomar Conference on Signals, Systems, and Computers, Monterey, California, November 2012.
- High Performance Power Delivery for Nanoscale Integrated Circuits, University of South Florida, Tampa, Florida, February 2012.
- EMMA: A Methodology to Model Current Activity of a Digital Block to Determine Emission Level for a Broad Frequency Range, *RF, Analog, and Sensor Group*, Freescale Semiconductor, Tempe, Arizona, August 2010.
- Simultaneous Co-Design of Clock and Power Distribution Networks, *Central Technology and Special Circuits Team*, Intel Corporation, Santa Clara, California, March 2009.
- Un-Core Clock Distribution of Nehalem-Ex Processor and the De-Skew Machine Operation Principles, *Central Technology and Special Circuits Team*, Intel Corporation, Santa Clara, California, August 2007.

Teaching

- **Instructor** University of South Florida
  Emerging Topics in Performance and Security of Modern Integrated Systems — Spring 2017, 6 students
  Design II (Senior Design Project) — Fall 2016, 40 students
  Design II (Senior Design Project) — Spring 2016, 45 students
  Design II (Senior Design Project) — Fall 2015, 40 students
  Design II (Senior Design Project) — Spring 2015, 45 students
  Design II (Senior Design Project) — Fall 2014, 40 students
  Design II (Senior Design Project) — Spring 2014, 54 students
  High Performance Integrated Circuit Design — Fall 2013, 8 students
  Introduction to Electrical Systems I (EGN 3373) — Fall 2012, > 120 students

- **Co-Lecturer** University of Rochester
  Performance Issues in IC/VLSI Design and Analysis — Fall 2011, > 10 students

- **Teaching Assistant** University of Rochester
  VLSI Design Methodologies — Fall 2009, > 10 students
  Circuits and Signals — Fall 2006, > 30 students
  Introduction to Signals and Circuits — Spring 2007, > 35 students

- **Teaching Assistant** Bilkent University, Ankara
  Analog Electronics — Fall 2004, Fall 2005, > 100 students
  Microprocessors — Spring 2005, Spring 2006 > 100 students

Student Awards

- **Longfei Wang** Stipend+Tuition
  University of South Florida Graduate Fellowship *2015 - 2016*

- **Weize Yu** Stipend+Tuition+Travel
  University of South Florida Presidential Doctoral Fellowship *2014 - 2019*

Professional Activities

- Associate editor
  Journal of Circuits, Systems, and Computers (JCSC), 2012 – present
  Microelectronics Journal, 2014 – present

- Committee member
  IEEE VLSI System Application Technical Committee, 2017 – present

- Technical program committee member
  IEEE International Symposium on Quality Electronic Design (ISQED), 2015-2017
  ACM Great Lakes Symposium on VLSI, 2013-2017
  IEEE Computer Society Annual Symposium on VLSI, 2014, 2015
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2015-2017
  IEEE International Symposium on Circuits and Systems (ISCAS), 2017

- Special session organizer
  Efficient IoT Systems: The Power of Heterogeneous Integration at GLSVLSI'17

- Local arrangement chair
  IEEE Computer Society Annual Symposium on VLSI, 2014

- Publications chair
  ACM/IEEE System Level Interconnect Prediction (SLIP) Workshop, 2017

- External reviewer
  Journals: *IEEE Journal of Solid-State Circuits (JSSC)*, *IEEE Transactions on Power Electronics (TPEL)*, *ACM Computing Surveys*, *IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS)*, *IEEE Transactions on Very Large Scale Integration (VLSI) Circuits (TVLSI)*, *IEEE Transactions Circuits and Systems-I (TCAS-I)*, *IEEE Transactions Circuits and Systems-II (TCAS-II)*, *IEEE Transactions Computer-Aided Design (TCAD)*, *IEEE Electron Device Letters (EDL)*, *ASP Journal of Low Power Electronics (JOLPE)*, *Analog Integrated Circuits and Signal Processing*, *Integration, the VLSI Journal*, *IET Circuits, Devices & Systems*, *Microelectronics Journal*
  Conferences: International Conference on Computer-Aided Design (ICCAD), International Symposium on Quality Electronic Design (ISQED), Design, Automation and Test in Europa (DATE), International Conference on Circuits and Systems (ISCAS), International Conference on Computer Design (ICCD), System-on-Chip Conference (SOCC), Asia Pacific Conference on Circuits and Systems (APCCAS), International Workshop on Power And Timing Modeling, Optimization and Simulation (PATMOS), Asia Symposium on Quality Electronic Design (ASQED), International Symposium on Networks-on-Chip (NOCS), Great Lakes Symposium on VLSI (GLSVLSI), International Conference on Very Large Scale Integration (VLSI-SOC)

- Professional Societies
  Member, IEEE
  Member, ACM
  Member, NAI

Service

International

- External reviewer for Israel Ministry of Science, Technology and Space, 2016

- External reviewer for Israel Science Foundation, 2017

National

- Participant at the "CCC/SIGDA Workshop on Extreme Scale Design Automation" visioning workshop (invitation only), organized by ACM special interest group on design automation (ACM/SIGDA), 02/21-22/2014

- NSF Panelist, 2014, 2015, 2016

University of South Florida

- Member of the USF System Research Council , Fall'15 – present
  – *Represent College of Engineering on matters pertaining to policies and procedures intended to promote growth, excellence, and integrity in research and creative activity throughout the university community.*

- Member of the College-wide Faculty Search Committee, 2015 – 2016

- Member of the Departmental Faculty Search Committee, 2014 – 2015

- Internal NSF CAREER reviewer, 2014, 2015

- Member of the Electrical Engineering Design Committee, Spring'14 – present

- Member of the Electrical Engineering Student Success Committee, Fall'12 – present