*University of Cincinnati*

Department of Electrical Engineering and Computing Systems

EECE 2060C – Digital Design ELTN 1040C – Digital Systems

# **Lab 4: Unsigned 2-Bit Adder Design**

Fall 2022

**Introduction**

The purposes of this experiment are to: (a) design the first computing device, adder, for arithmetic and logic unit (ALU) of a computer; and (b) successfully wire a computing device with reasonable size by divide and conquer.

Before the pandemic, students could use **74181 ALU** chip and several gates to design a 5**-bit signed 2’s complement adder/subtractor.** Due the breaking of the chip supply chain caused by the pandemic, we do NOT have 74181 to use, so let us build a **2-bit unsigned (positive) adder** instead.

**Design Specification**

The two-bit adder uses **unsigned number system** that can deal with positive numbers only. The first (second) number has two bits X1 (Y1) and X0 (Y0) where X1 (Y1) is the most significant bit. The unsigned 2-bit full adder has 5 inputs, (X1, X0, Y1, Y0, C0) and 3 outputs (C2, S1, S0) where each Si is a sum bit and C2 is the carry out of the last stage (i.e., overflow). The unsigned 2-bit adder adds X and Y. For example, if X1X0=11 and Y1Y0=10, then S1S0=01 and C2=1 (overflow). Inputs come directly from Vdd and GND or from the switches, and outputs are displayed to logic value indicator (LEDs).

**Task 1 – Single-Bit Full Adder Design**

As discussed in the lectures, there are several different full adder designs and you are suggested to use the 5-gate design (2 EXORs, 2 ANDs, 1 OR) due to the smaller number of gates used and smaller wiring efforts. This design can be found on Page 162 of the textbook. Each single-bit full adder design has 3 inputs, Xi, Yi, Ci, and has 2 outputs Si and Ci+1.

**Task 2 – Two-Bit Full Adder Design**

A 2-bit full adder can be easily designed by **cascading** two single-bit adders together. There is no need to use circuit simulation for circuit design verification because your design comes from the textbook. Again, the unsigned 2-bit full adder has 5 inputs, (X1, X0, Y1, Y0, C0) and 3 outputs (C2, S1, S0).

**Circuit Wiring**

It is suggested that **you test your circuit after you wire one or two gates**. This divide and conquer method (or correctness by construction method) will greatly reduce the trouble-shooting time. It will be a nightmare if you wire all things and find errors.

**Circuit Testing**

The number of inputs for this circuit is 5 and it is time-consuming to verify all input combinations. You must give a good **test plan**. For example, try to add two small numbers and see whether it works; try to add two large numbers; try to add one small number and one large; test overflow circuit; test 0+0; ……. You MUST use at least 10 test patterns. Complete the following table (Table 1), and have the TA check for you once you are sure the circuit passes test patterns below.

**Table 1**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Pattern no.** | **1st number**  **C0, X1, X0** | **2nd number**  **Y1, Y0** | **Expected Results**  **C2, S1, S0** | **Actual Results**  **C2, S1, S0** | **Purpose** |
| 1 | 1,0,0 | 0,0 | 0,0,1 | 0,0,1 |  |
| 2 | 1,0,0 | 1,1 | 1,0,0 | 1,0,0 |  |
| 3 | 0,0,0 | 1,1 | 0,1,1 | 0,1,1 |  |
| 4 | 1,1,1 | 1,1 | 1,1,1 | 1,1,1 |  |
| 5 | 0,0,1 | 0,1 | 0,0,1 | 0,0,1 |  |
| 6 | 1,1,1 | 1,0 | 1,1,0 | 1,1,0 |  |
| 7 | 0,1,0 | 1,0 | 1,0,0 | 1,0,0 |  |
| 8 | 0,1,1 | 1,0 | 1,0,1 | 1,0,1 |  |
| 9 | 1,0,1 | 0,0 | 0,1,0 | 0,1,0 |  |
| *10* | 0,0,0 | 0,0 | 0,0,0 | 0,0,0 |  |

**Project Pre-lab Design Report:**

Not required because the design is from the textbook

**Project Pre-lab Design Report (PDR) Format:**

**Not required.**