*University of Cincinnati  
Department of Electrical Engineering and Computing Systems***EECE 2060C – Digital Design, Lab room 806/808 Rodes, Section# 005**

**Andrew Koski, M14561095, 10/25/2022**

**Laboratory Project 7  
A Sequence Detector Implementation using Breadboard  
Fall 2022**

Description:

In this lab, a synchronous sequential circuit is designed to recognize a sequence of 11\*00\* where 1\*   
represents any number of logic 1’s, e.g., 0 logic 1, 1 logic 1, 2 logic 1’s, ... , and 0\* represents any   
number of logic 0’s, e.g., 0 logic 0, 1 logic 0, 2 logic 0’s, ..... The sequential circuit has one input I and one output Z, and Z outputs logic 1 when the machine identifies a sequence of 11\*00\*. A sample input sequence and output response is given below.  
I = 0 1 1 0 0 1 0 1 0 0 1   
Z= 0 0 0 1 1 0 1 0 1 1 0

Module designs:

A piece of paper with writing

Description automatically generated with low confidence

**module D\_FF**(Q, D, CLK, Clr);

output Q;

input D, CLK, Clr;

reg Q;

always @(posedge CLK, negedge Clr)

if (~Clr) Q <= 1'b0; else Q <= D;

endmodule

**module Moore\_sequential**(output y\_out, A, B, input x\_in, clock, reset);

wire Da, Db;

assign Da = ~x\_in & (A | B);

assign Db = x\_in;

assign y\_out = Da;

D\_FF m1 (A, Da, clock, reset);

D\_FF m2 (B, Db, clock, reset);

Endmodule

**module testtb;**

reg x\_in;

reg clock;

reg reset;

wire y\_out;

Moore\_sequential uut (.y\_out(y\_out), .A(A), .B(B), .x\_in(x\_in), .clock(clock), .reset(reset));

initial begin

x\_in = 0;

clock = 0;

reset = 1;

#1 reset = 0;

#1 reset = 1;

repeat (13)

#5 clock = ~clock;

end

initial begin

#7 x\_in = 0;

#10 x\_in = 1;

#10 x\_in = 1;

#10 x\_in = 0;

#10 x\_in = 0;

#10 x\_in = 1;

#10 x\_in = 0;

#10 x\_in = 1;

#10 x\_in = 0;

#10 x\_in = 0;

#10 x\_in = 1;

end

endmodule

Graphical user interface

Description automatically generated

Design Time: 3 hours in total