*University of Cincinnati  
Department of Electrical Engineering and Computing Systems***EECE 2060C – Digital Design, Lab room 806/808 Rodes, Section# 005**

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**Laboratory Project 8  
An Updown Counter Design and Implementation using Verilog Vivado and FPGA  
Fall 2022**

**Design Specification**

In this lab, a 4-bit synchronous updown counter will be designed. It has inputs: up\_down,   
clear\_b, and clock, and outputs: MSG and a\_to\_g [6:0] as shown in Figure 1 of file: 03-Lab8-  
figures. Inputs:

When up\_down = 1 (0), the counter counts up (down). This signal will be input by a switch on

the FPGA board.

When clear\_b = 0, the counter is reset to 0. When clear\_b = 1, the counter is counting up or down depending on the value of up\_down. This signal will be input by a switch on the FPGA board.  
Signal clock is the clock signal of the counter, and is a built-in clock with 100 MHz on the Basys   
3 FPGA board. The clock frequency is too high to be used. We will use a device to greatly   
reduce the clock frequency.

Outputs:

MSG is an LED on the FPGA board to display the counter value (second digit).  
Signals a\_to\_g [6:0] give seven output signals to a seven-segment display on the FPGA board.   
 Details about seven-segment display will be given later.

**Design correlation**

Diagram, schematic

Description automatically generated

**UpDownCounter module And Waveform testbenches**

Text, letter

Description automatically generated

Graphical user interface, text, application

Description automatically generated

Chart, treemap chart

Description automatically generated

**Bin2bcd module And Waveform testbenches**

Text

Description automatically generated

Table

Description automatically generated

Graphical user interface

Description automatically generated

**Final waveforms Combining all modules**Graphical user interface, chart

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Total Work Time 5 hours 25 minutes .