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## VCU108 MIG Design Creation

December 2017

# Revision History

Date	Version	Description
12/20/17	12.0	Updated for 2017.4.
10/26/17	11.0	Updated for 2017.3.1.
06/20/17	10.0	Updated for 2017.2.
04/19/17	9.0	Updated for 2017.1.
12/19/16	8.0	Updated for 2016.4.
11/22/16	7.1	RLD3 Designs added. AR66800 fixed.
10/13/16	7.0	Updated for 2016.3.
08/16/16	6.1	Updated RLD3 build instructions and RDF file.
06/08/16	6.0	Updated for 2016.2.
04/13/15	5.0	Updated for 2016.1. Added AR66800.
11/24/15	4.0	Updated for 2015.4.
10/06/15	3.0	Updated for 2015.3.
07/15/15	2.0	Updated for 2015.2.
06/30/15	1.0	Initial version for 2015.1.

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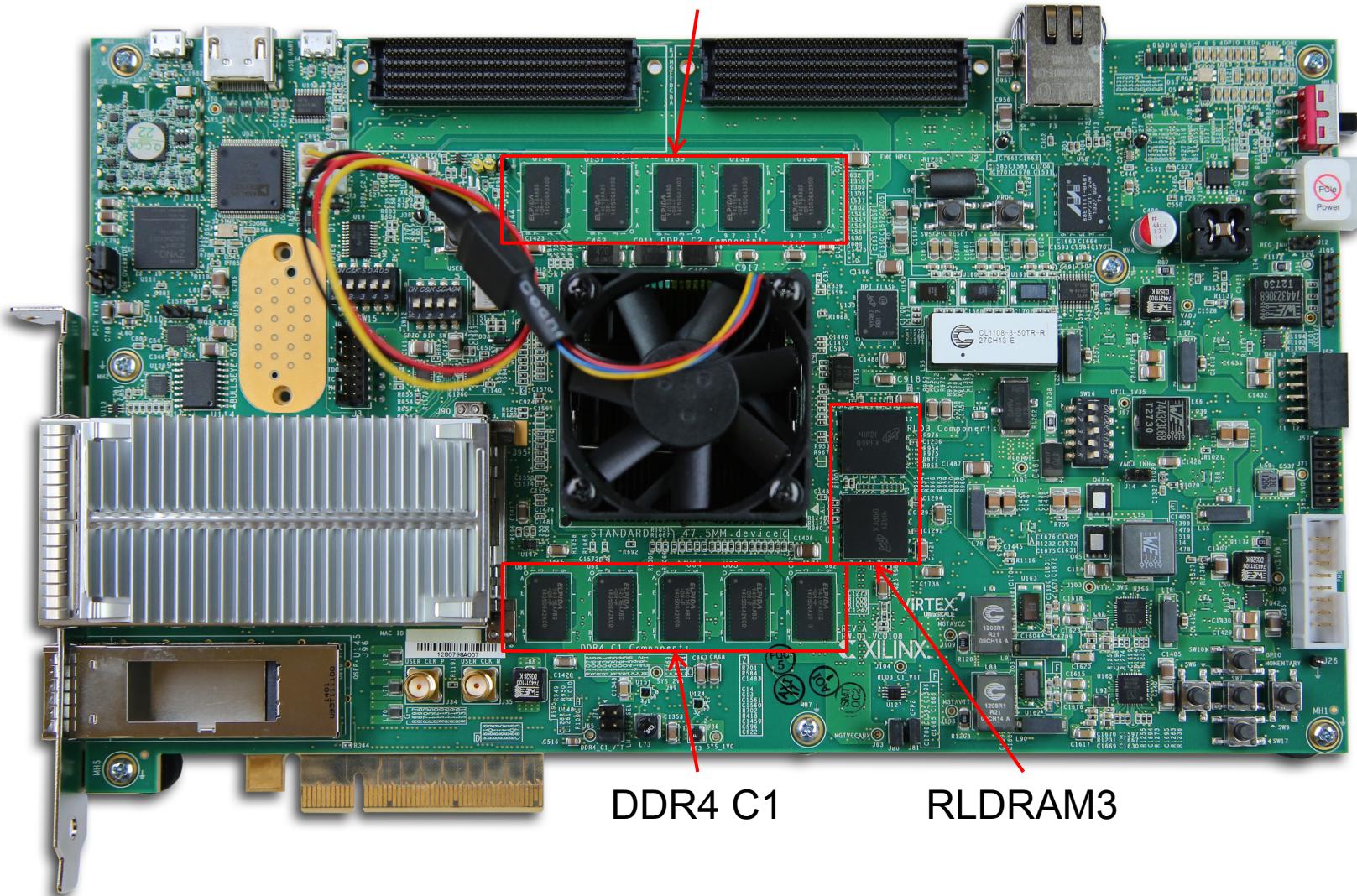
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# Xilinx VCU108 Board

DDR4 C2



# VCU108 Software Install and Board Setup

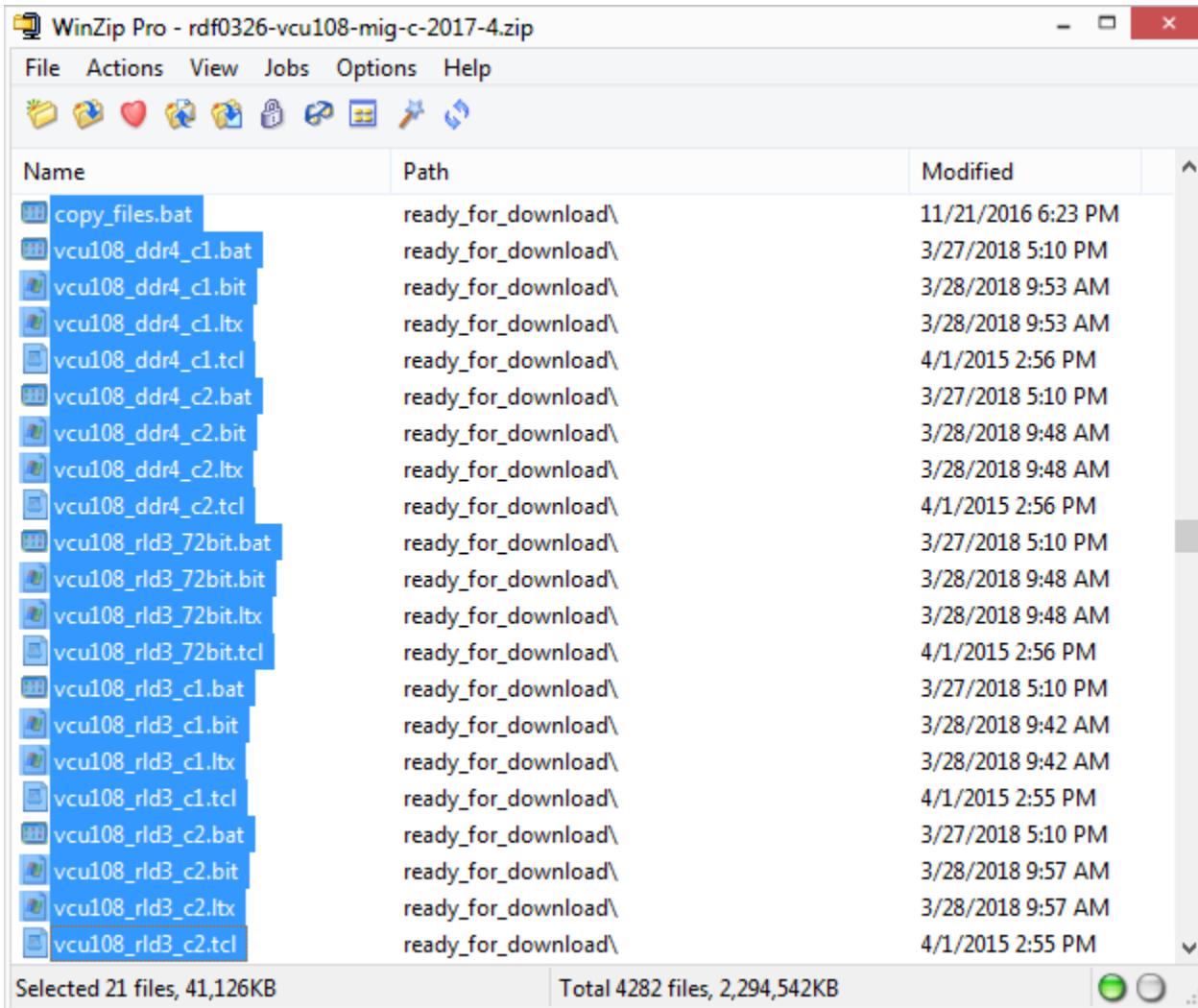
► Complete setup steps in XTP368 – VCU108 Software Install and Board Setup:

- Software Requirements
- VCU108 Board Setup



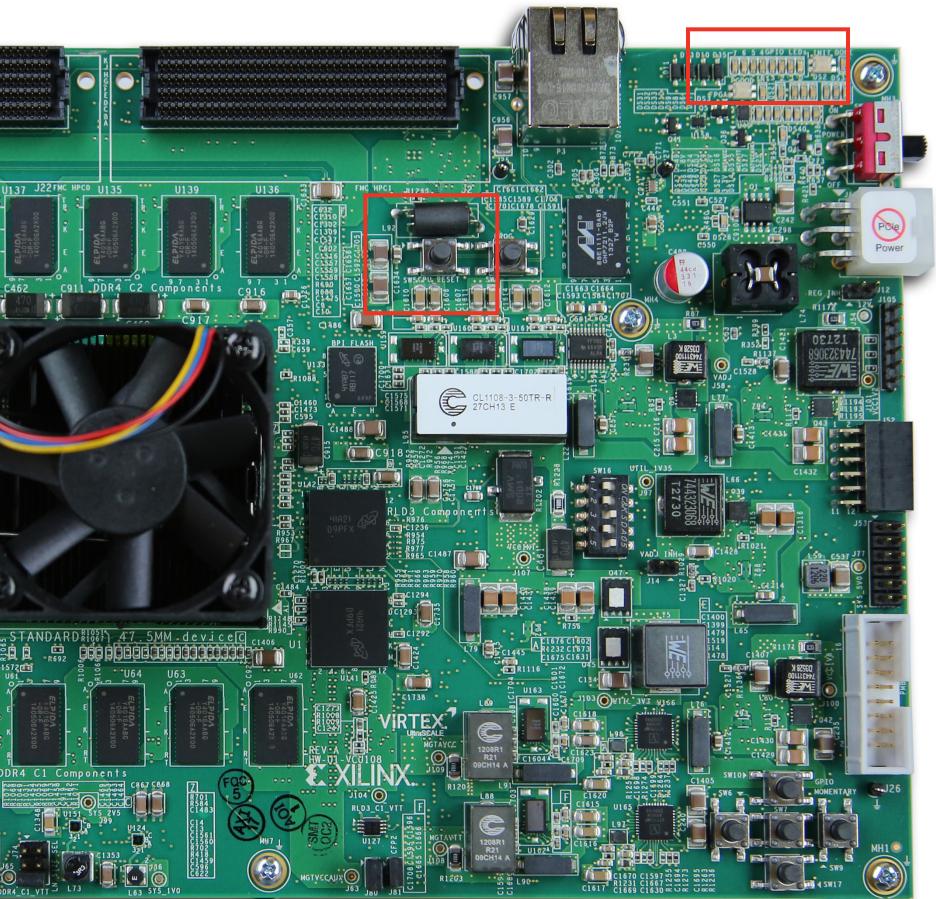
# VCU108 Setup

- Open the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file, and extract the “ready\_for\_download” files to your C:\ drive:



# Run MIG Example Designs

# Run MIG Example Design



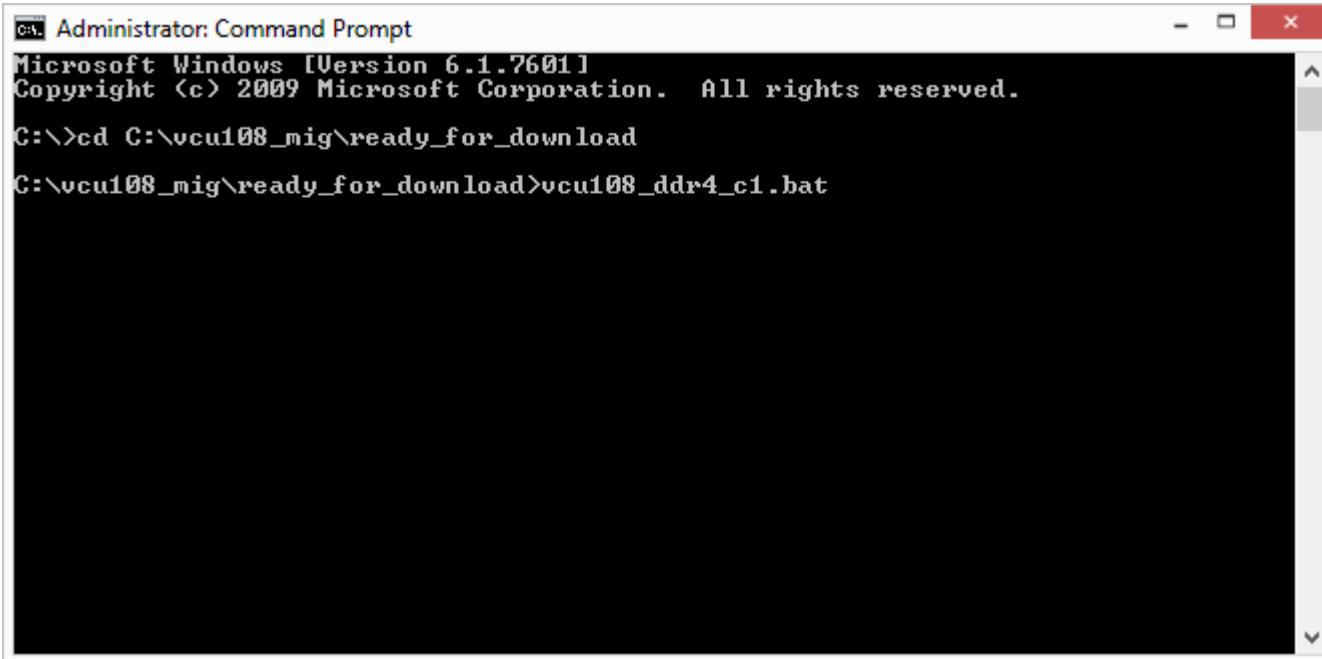
- For the following five tests:
- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset
- On the DDR4 bitstreams, LEDs 4-7 are pulled up and will be lit

# Run MIG Example Design

- From a Command Prompt, type:

```
cd C:\vcu108_mig\ready_for_download  
vcu108_ddr4_c1.bat
```

- View results on LEDs



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright © 2009 Microsoft Corporation. All rights reserved.

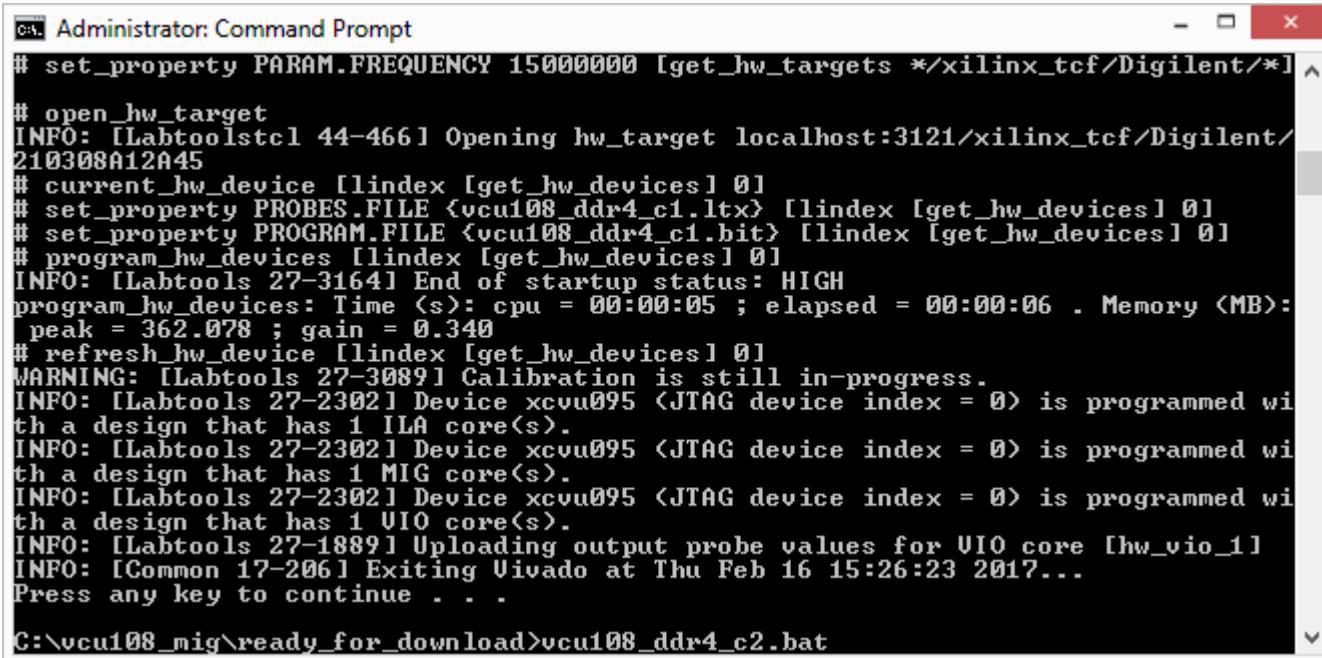
C:\>cd C:\vcu108_mig\ready_for_download
C:\vcu108_mig\ready_for_download>vcu108_ddr4_c1.bat
```

# Run MIG Example Design

► Type:

**vcu108\_ddr4\_c2.bat**

► View results on LEDs



The screenshot shows an Administrator Command Prompt window with the title 'Administrator: Command Prompt'. The window contains the following text output from the batch file:

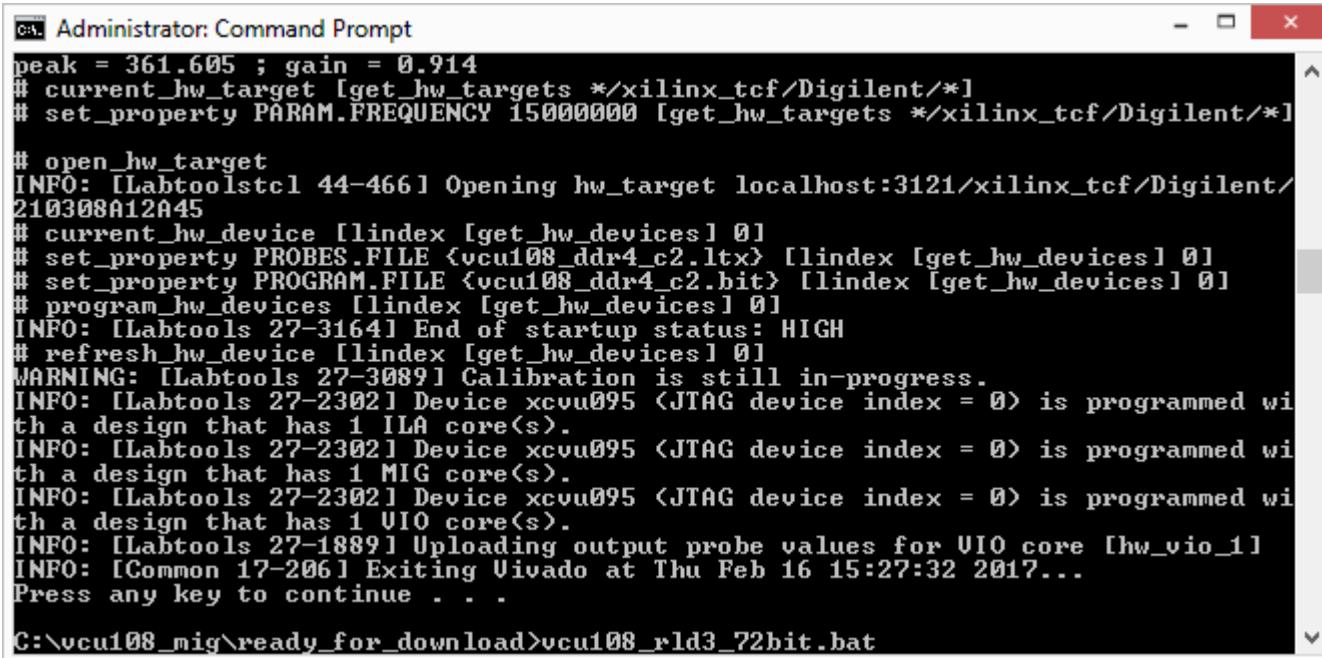
```
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
# open_hw_target
INFO: [Labtools 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210308A12A45
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu108_ddr4_c1.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu108_ddr4_c1.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:05 ; elapsed = 00:00:06 . Memory <MB>:
peak = 362.078 ; gain = 0.340
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Common 17-206] Exiting Vivado at Thu Feb 16 15:26:23 2017...
Press any key to continue . . .
C:\vcu108_mig\ready_for_download>vcu108_ddr4_c2.bat
```

# Run MIG Example Design

► Type:

**vcu108\_rld3\_72bit.bat**

► View results on LEDs



```
Administrator: Command Prompt
peak = 361.605 ; gain = 0.914
# current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]

# open_hw_target
INFO: [Labtools 44-4661] Opening hw_target localhost:3121/xilinx_tcf/Digilent/
210308A12A45
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu108_ddr4_c2.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu108_ddr4_c2.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed wi
th a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed wi
th a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed wi
th a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Common 17-206] Exiting Vivado at Thu Feb 16 15:27:32 2017...
Press any key to continue . . .

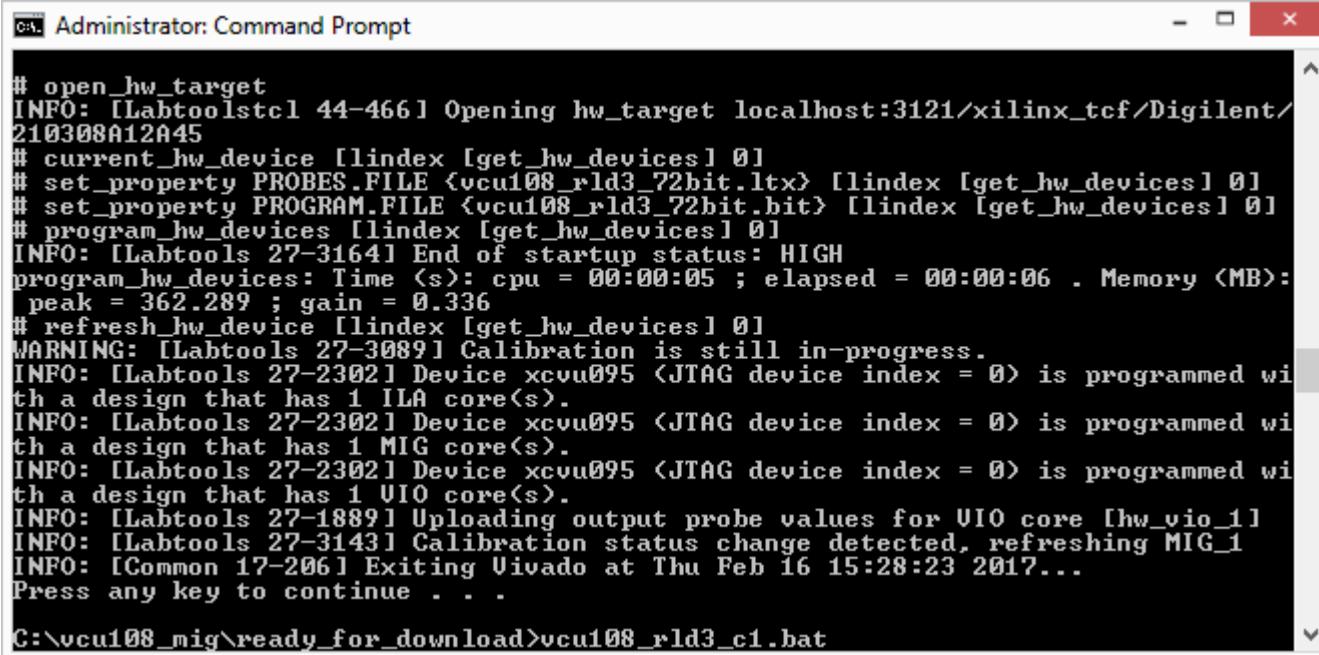
C:\vcu108_mig\ready_for_download>vcu108_rld3_72bit.bat
```

# Run MIG Example Design

► Type:

**vcu108\_rld3\_c1.bat**

► View results on LEDs



The screenshot shows an 'Administrator: Command Prompt' window with a black background and white text. The window title is 'Administrator: Command Prompt'. The command entered was 'vcu108\_rld3\_c1.bat'. The output of the script is displayed below:

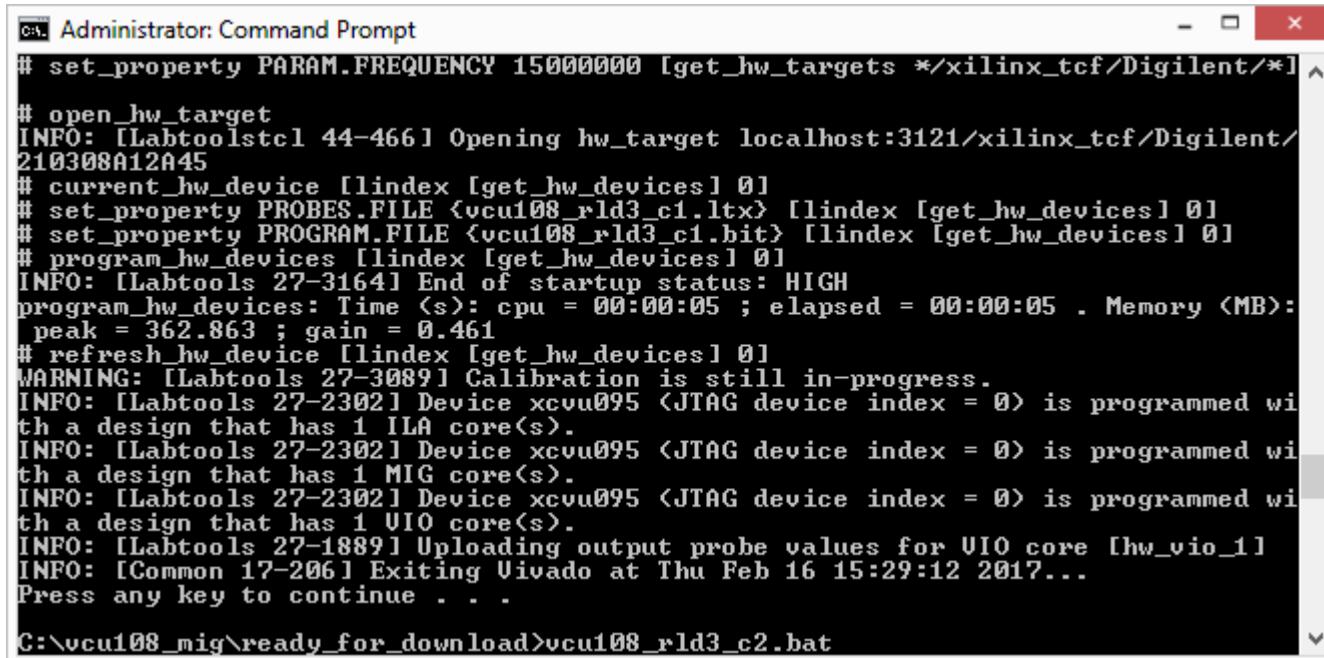
```
# open_hw_target
INFO: [Labtoolstcl 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210308A12A45
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu108_rld3_72bit.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu108_rld3_72bit.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:05 ; elapsed = 00:00:06 . Memory (MB):
peak = 362.289 ; gain = 0.336
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Labtools 27-3143] Calibration status change detected, refreshing MIG_1
INFO: [Common 17-206] Exiting Vivado at Thu Feb 16 15:28:23 2017...
Press any key to continue . . .
C:\vcu108_mig\ready_for_download>vcu108_rld3_c1.bat
```

# Run MIG Example Design

► Type:

**vcu108\_rld3\_c2.bat**

► View results on LEDs



The screenshot shows an Administrator Command Prompt window with the title 'Administrator: Command Prompt'. The window contains the output of a command-line script named 'vcu108\_rld3\_c2.bat'. The script performs several tasks: it sets the frequency to 15MHz, opens a hardware target, and programs an XCVU095 device with an MIG core. It also uploads output probe values for a VIO core and exits Vivado. The output ends with a prompt to press any key to continue.

```
# set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
# open_hw_target
INFO: [Labtools 44-466] Opening hw_target localhost:3121/xilinx_tcf/Digilent/210308A12A45
# current_hw_device [lindex [get_hw_devices] 0]
# set_property PROBES.FILE {vcu108_rld3_c1.ltx} [lindex [get_hw_devices] 0]
# set_property PROGRAM.FILE {vcu108_rld3_c1.bit} [lindex [get_hw_devices] 0]
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:05 ; elapsed = 00:00:05 . Memory <MB>: peak = 362.863 ; gain = 0.461
# refresh_hw_device [lindex [get_hw_devices] 0]
WARNING: [Labtools 27-3089] Calibration is still in-progress.
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 ILA core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 MIG core(s).
INFO: [Labtools 27-2302] Device xcvu095 (JTAG device index = 0) is programmed with a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
INFO: [Common 17-206] Exiting Vivado at Thu Feb 16 15:29:12 2017...
Press any key to continue . . .
C:\vcu108_mig\ready_for_download>vcu108_rld3_c2.bat
```

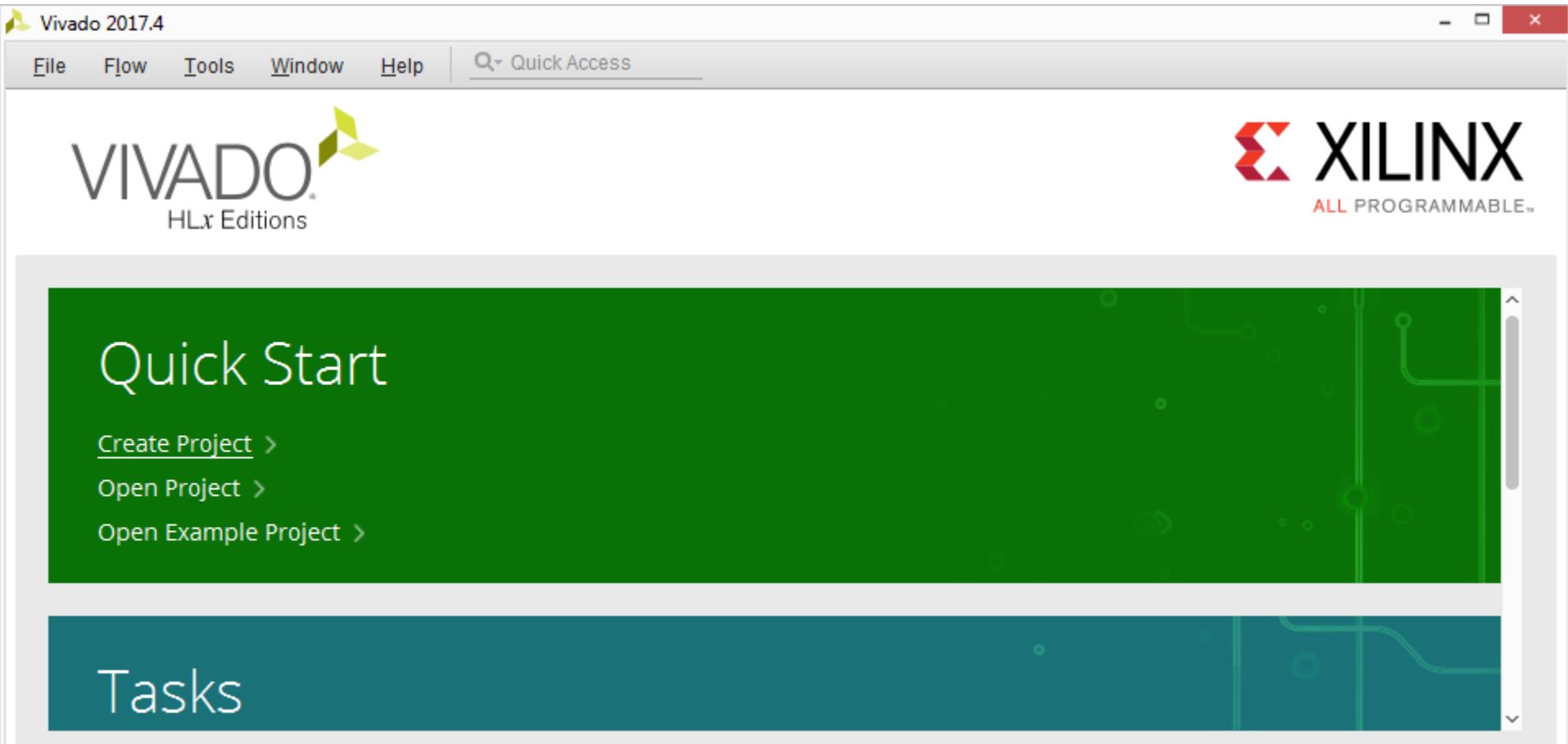
# Generate MIG DDR4 C1 Example Design

# Generate MIG DDR4 C1 Example Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.4 → Vivado

► Select Create Project



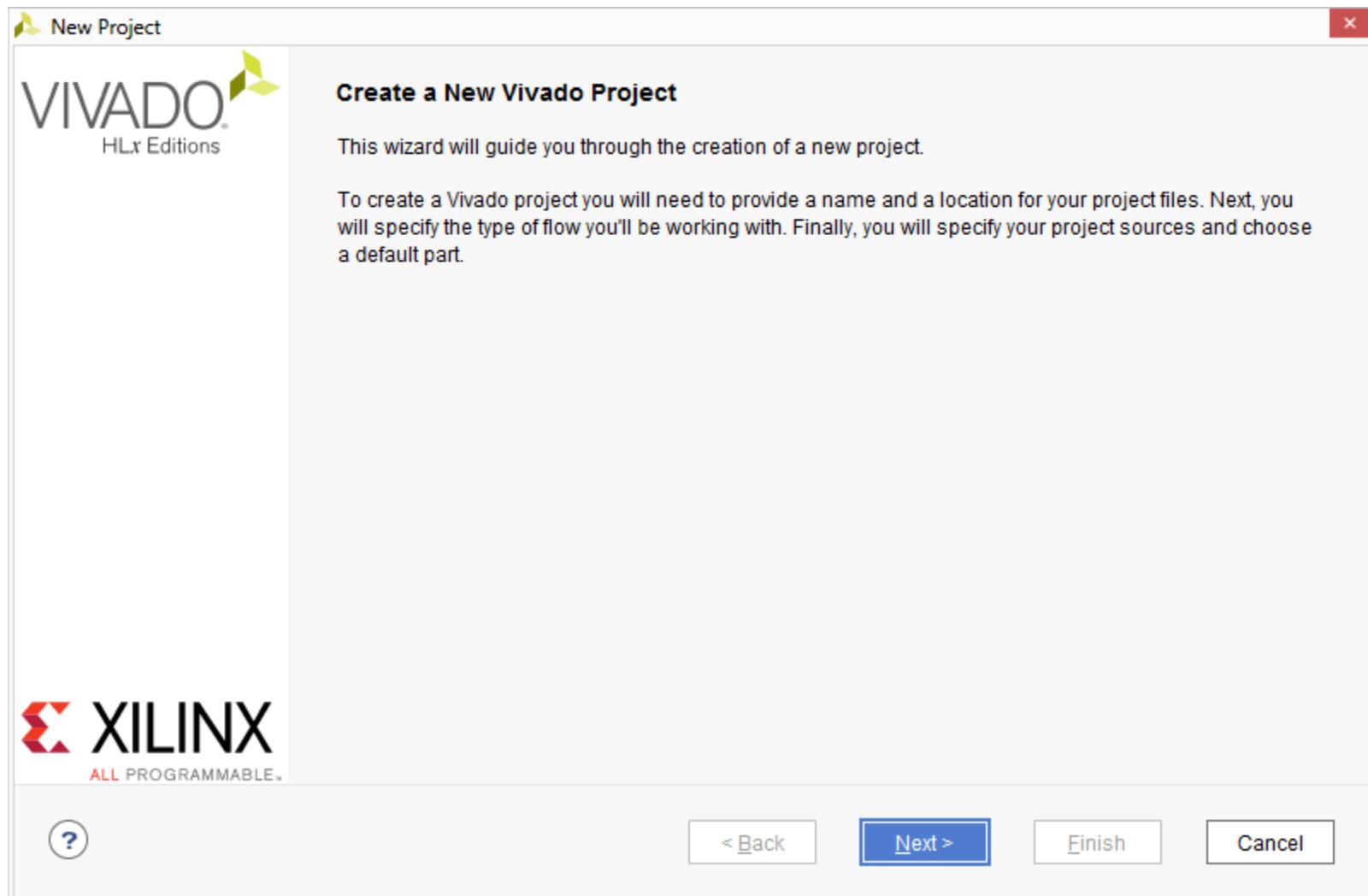
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU108

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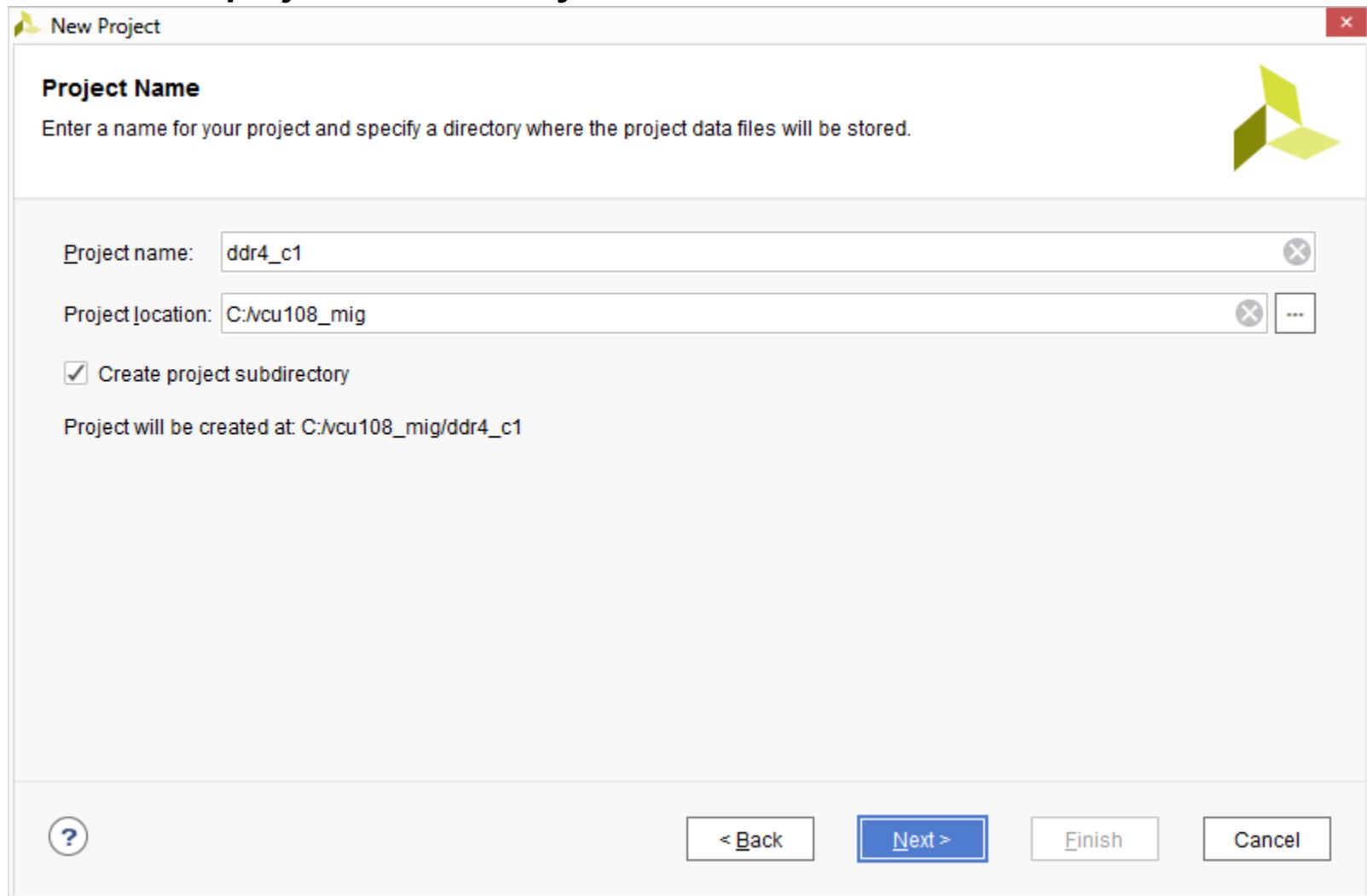
# Generate MIG DDR4 C1 Example Design

► Click Next



# Generate MIG DDR4 C1 Example Design

- Set the Project name to **ddr4\_c1** and location to **C:/vcu108\_mig**
  - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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# Generate MIG DDR4 C1 Example Design

## ► Select RTL Project

- Select **Do not specify sources at this time**

New Project

**Project Type**  
Specify the type of project to create.



RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Generate MIG DDR4 C1 Example Design

► Under Boards, select the VCU108 Evaluation Platform

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

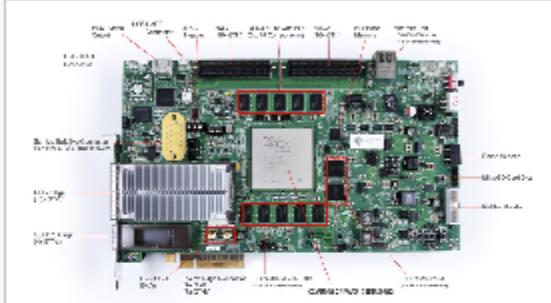
Select: Parts Boards

Filter/ Preview

Vendor: All  
Display Name: All  
Board Rev: Latest

Reset All Filters

Search:



Display Name	Vendor	Board Rev	Part
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2
<b>Virtex-UltraScale VCU108 Evaluation Platform</b>	xilinx.com	1.0	<b>xcvu095-fvfa2104-2-e</b>
Virtex-UltraScale VCU110 Evaluation Platform	xilinx.com	1.0	xcvu190-flac2104-2-e

No Board Connectors

?

< Back

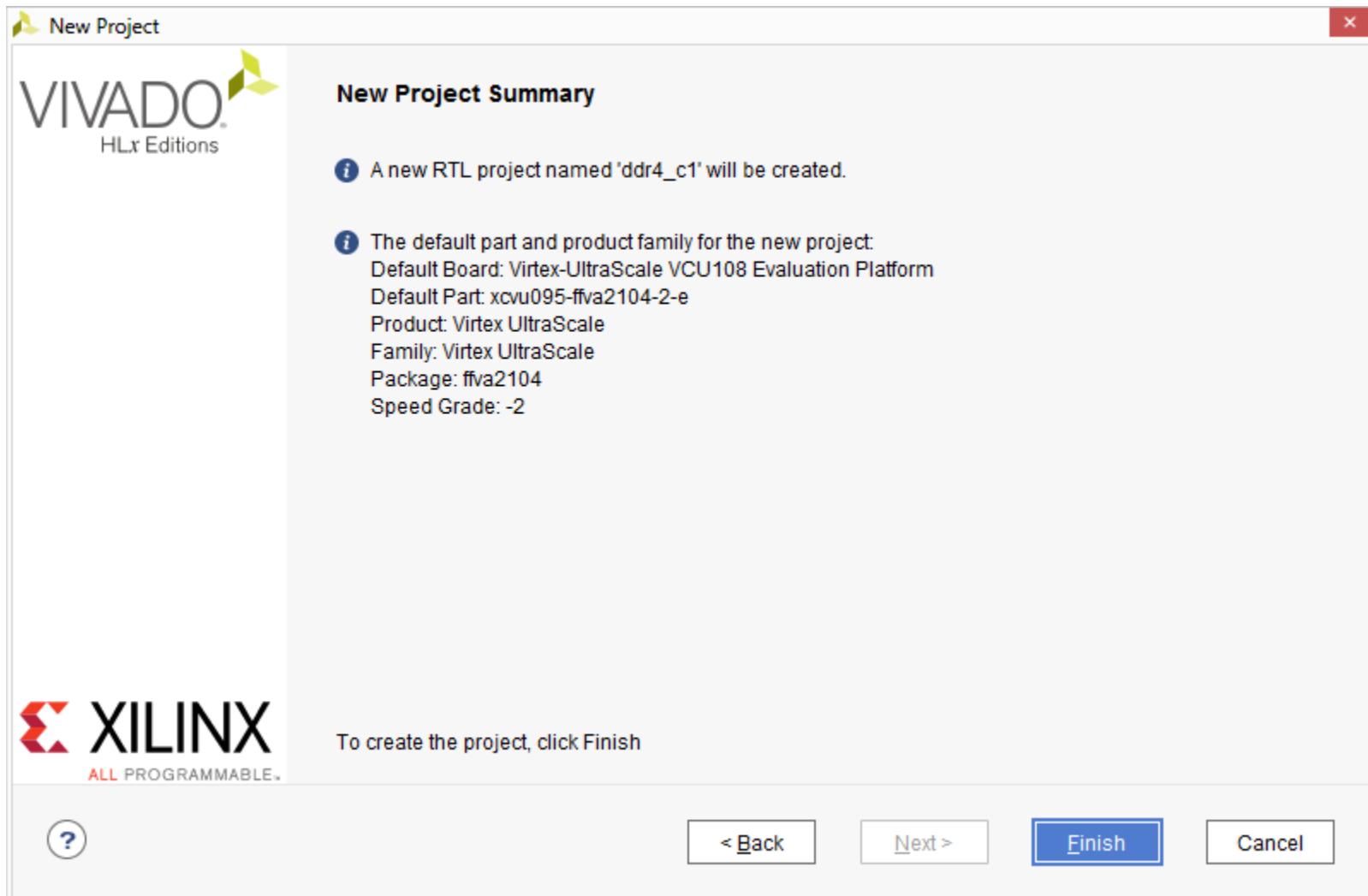
Next >

Finish

Cancel

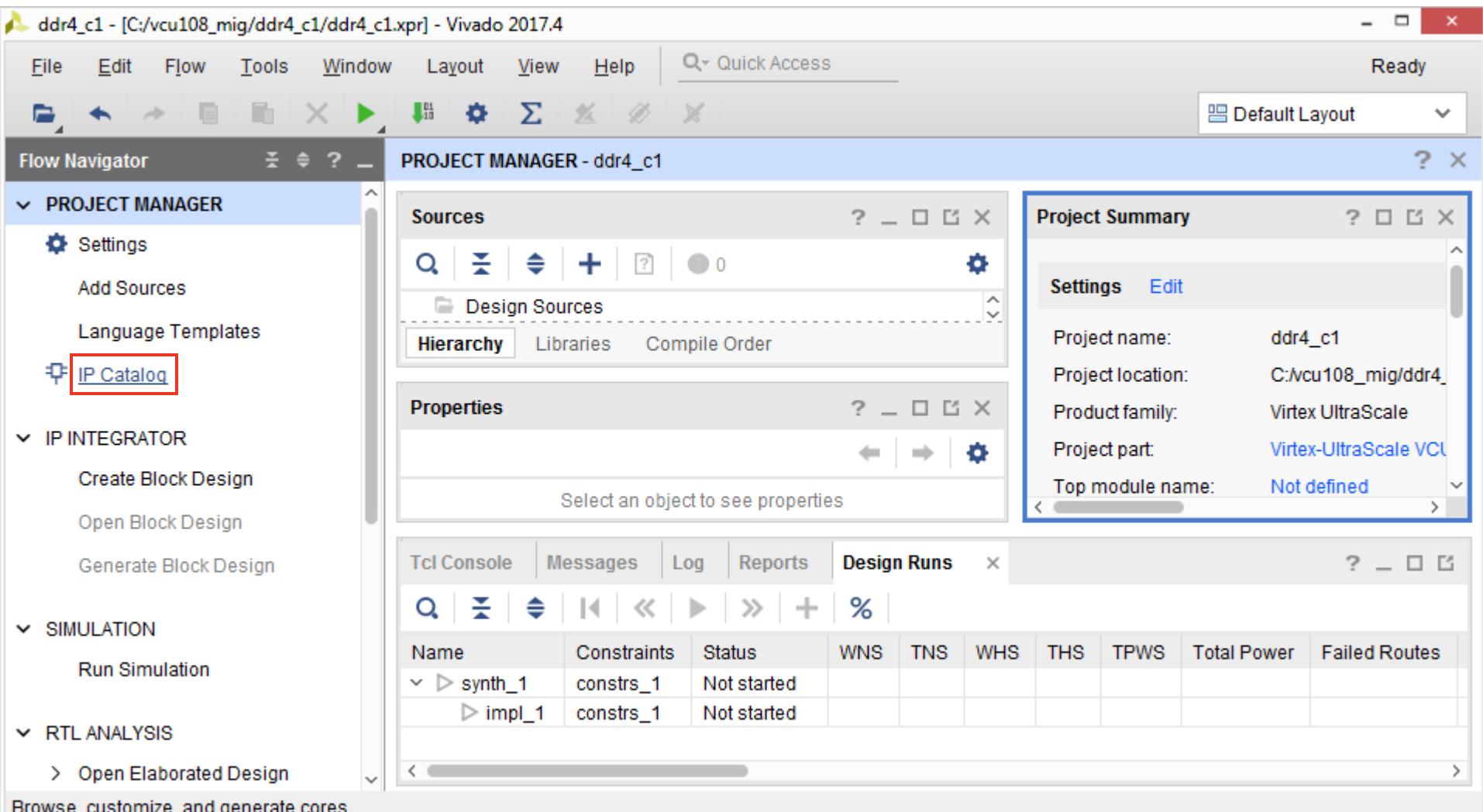
# Generate MIG DDR4 C1 Example Design

► Click Finish



# Generate MIG DDR4 C1 Example Design

► Click on IP Catalog



# Generate MIG DDR4 C1 Example Design

## ► Select DDR4 SDRAM (MIG), v2.2

The screenshot shows the Vivado 2017.4 interface with the project "ddr4\_c1" open. The left sidebar contains sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The IP INTEGRATOR section is expanded, showing options like Create Block Design, Open Block Design, and Generate Block Design. The central area is the PROJECT MANAGER - ddr4\_c1 window, which has tabs for Project Summary and IP Catalog. The IP Catalog tab is active, displaying the IP Catalog interface. Under the Cores tab, there is a list of components. The DDR4 SDRAM (MIG) component is selected, highlighted with a blue background. The table below shows the details for the selected component:

Name	Status	License	VLI
ECC	Production	Included	xilinx
External Memory Interface			
DDR3 SDRAM (MIG)	Production	Included	xilinx
<b>DDR4 SDRAM (MIG)</b>	<b>Production</b>	<b>Included</b>	<b>xilinx</b>
LPDDR3 SDRAM (MIG)	Pre-Production	Included	xilinx

Below the table, the Details section provides specific information about the selected component:

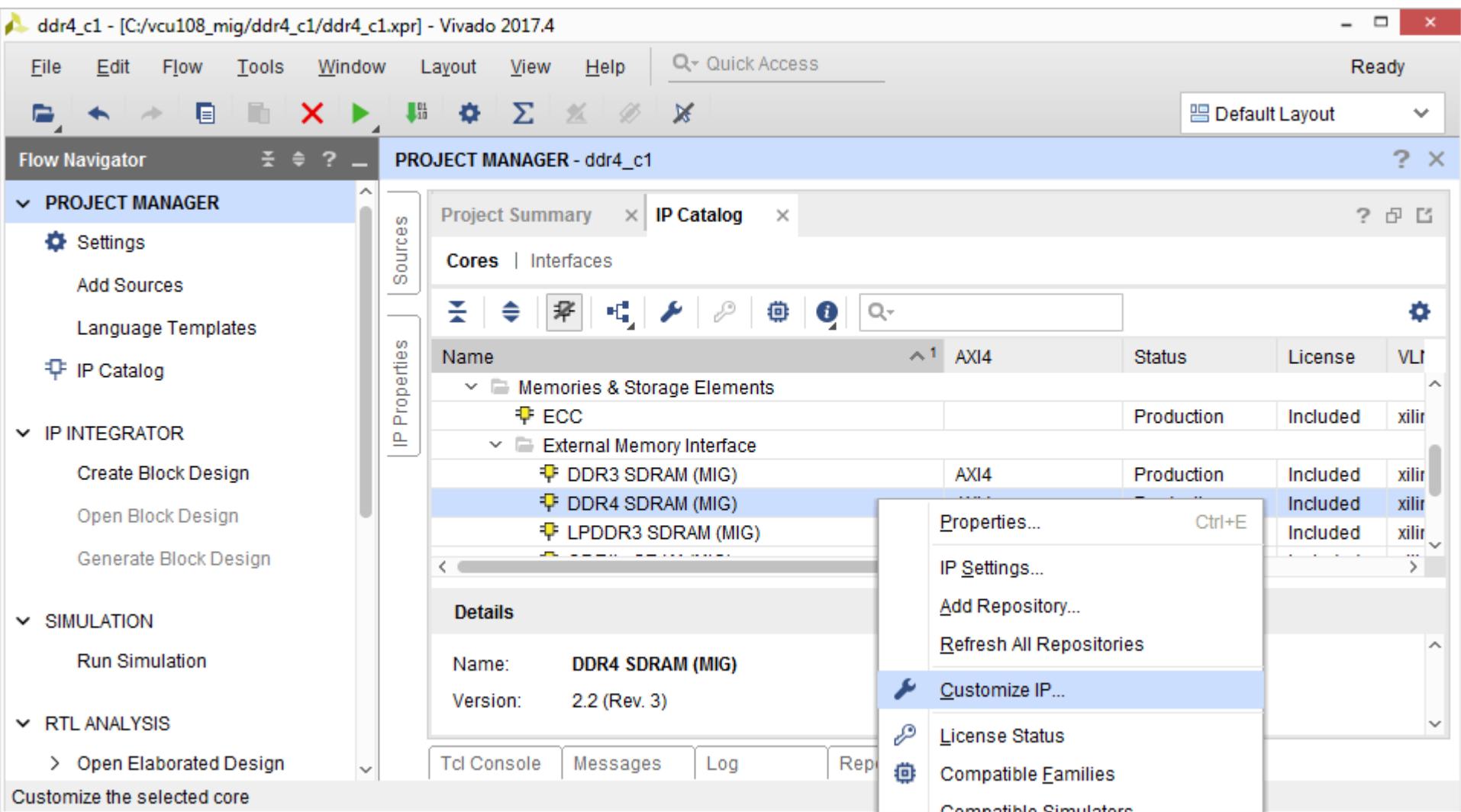
Name: DDR4 SDRAM (MIG)  
Version: 2.2 (Rev. 3)

The bottom navigation bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs. A status bar at the bottom left indicates "IP: DDR4 SDRAM (MIG)".

# Generate MIG DDR4 C1 Example Design

► Right click on **DDR4 SDRAM (MIG)**

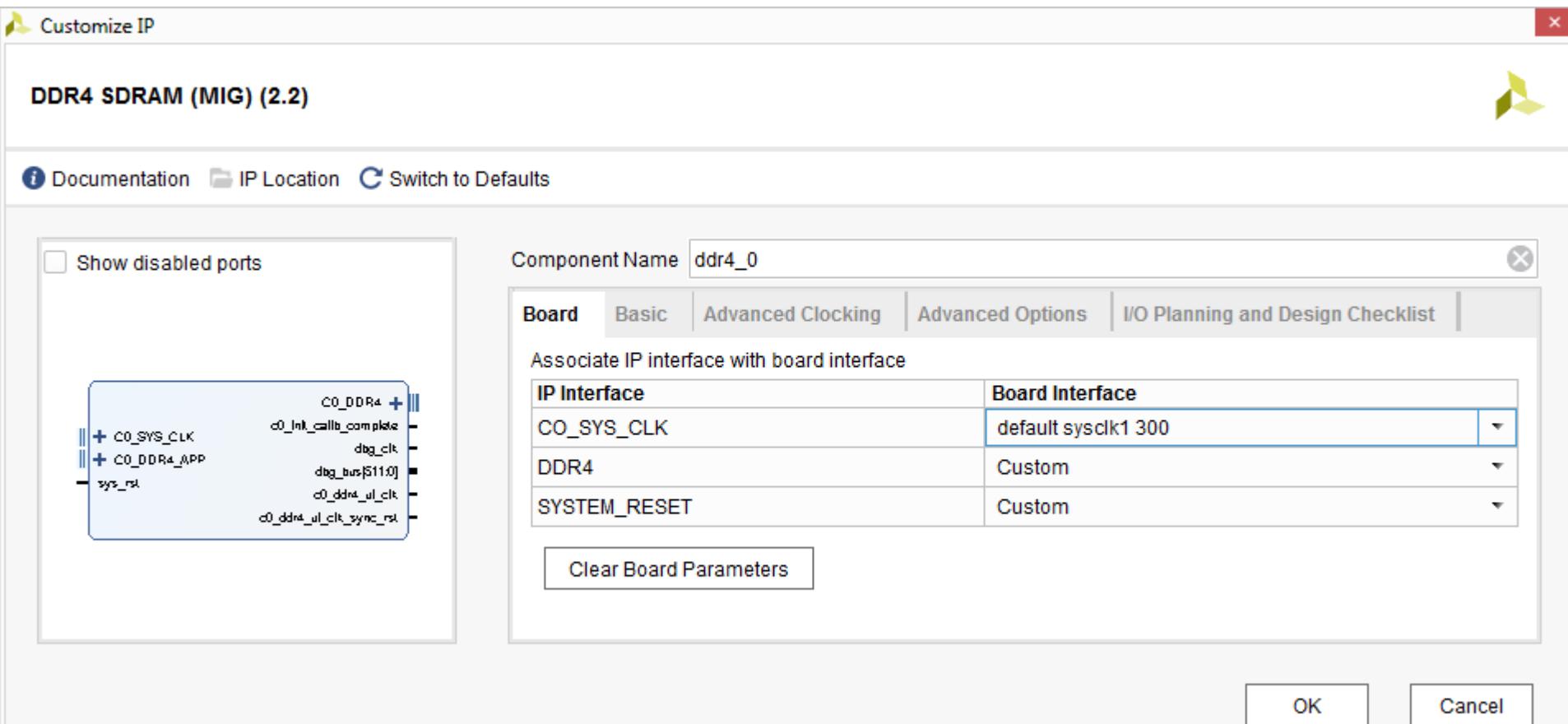
- Select **Customize IP**



# Generate MIG DDR4 C1 Example Design

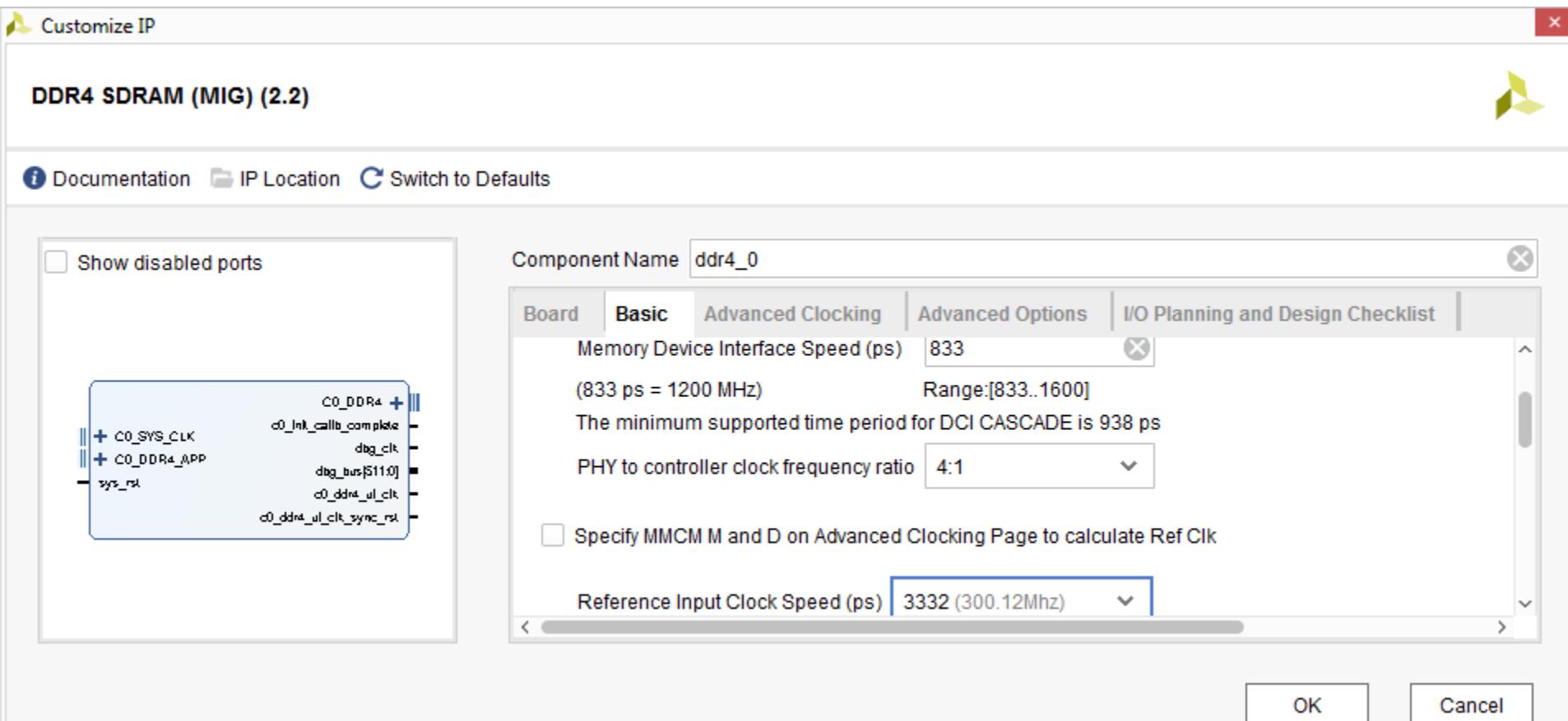
► Under the **Board** tab, set the DDR4 interfaces

- Set C0\_SYS\_CLK to **default sysclk1 300**
- Set C0\_DDR4 to **Custom**
- Set SYSTEM\_RESET to **Custom**



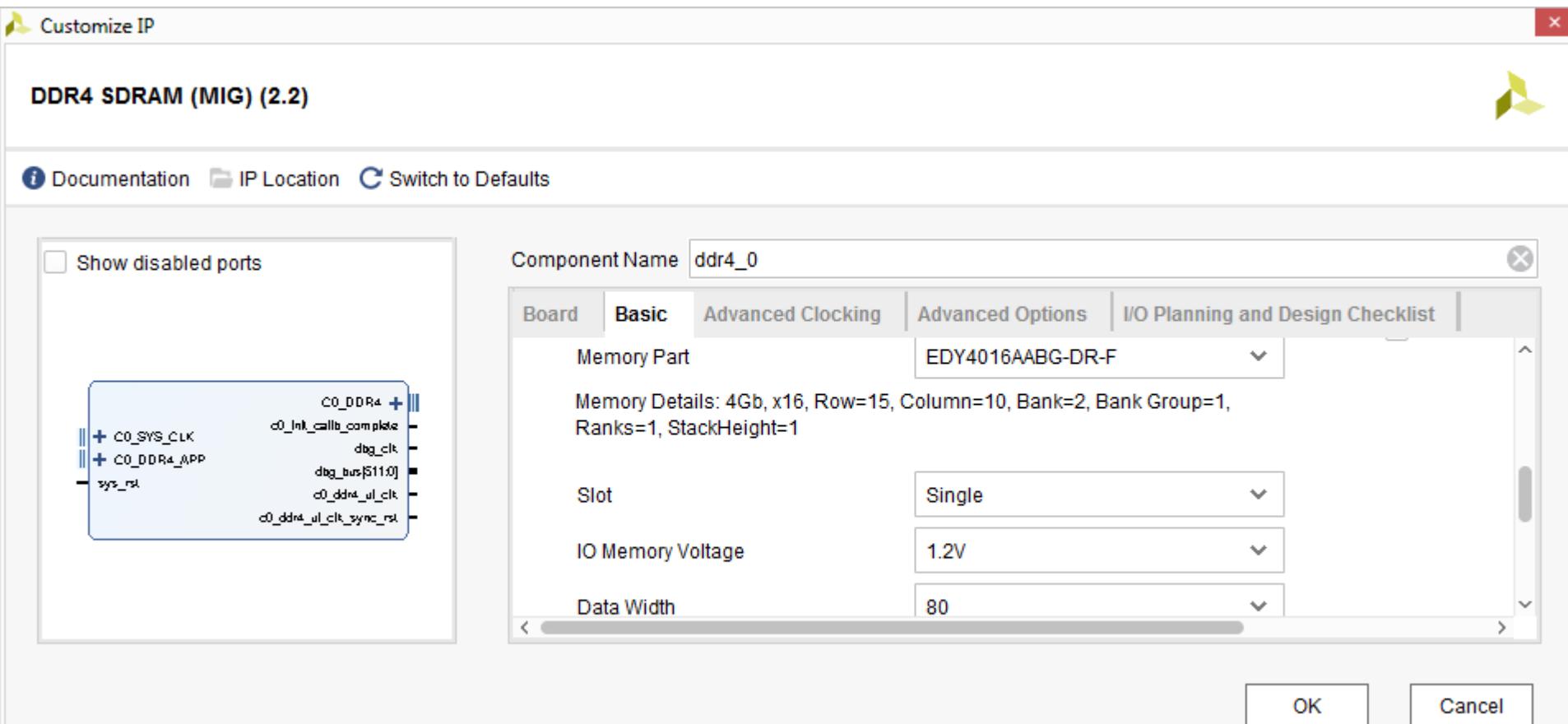
# Generate MIG DDR4 C1 Example Design

- Set the Clock period to **833** for 2400 Mb/s operation.
- Set the Input Clock to **3332** ps for 300 MHz
- Scroll down



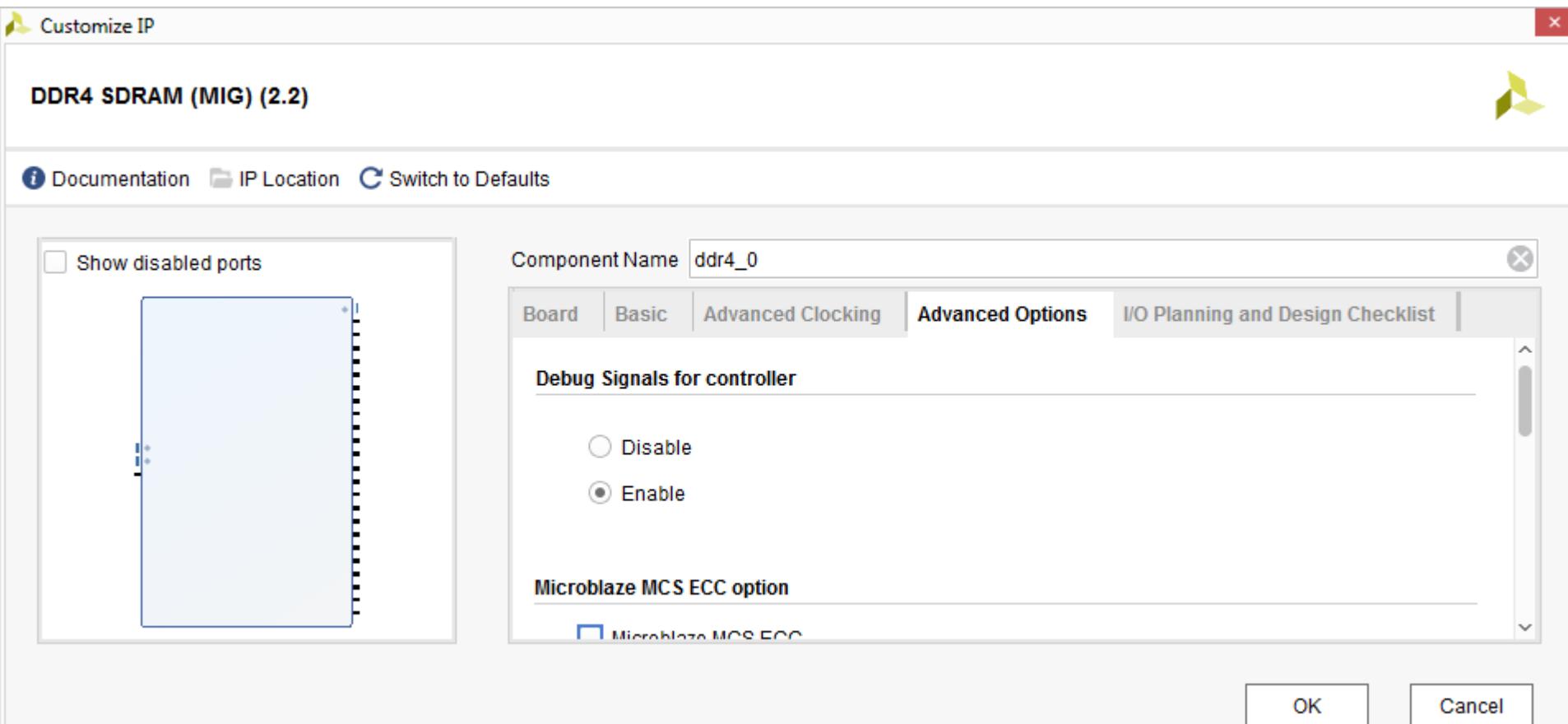
# Generate MIG DDR4 C1 Example Design

- Set the part to **EDY4016AABG-DR-F**
- Set the Data Width to **80** and click the **Advanced Options** tab



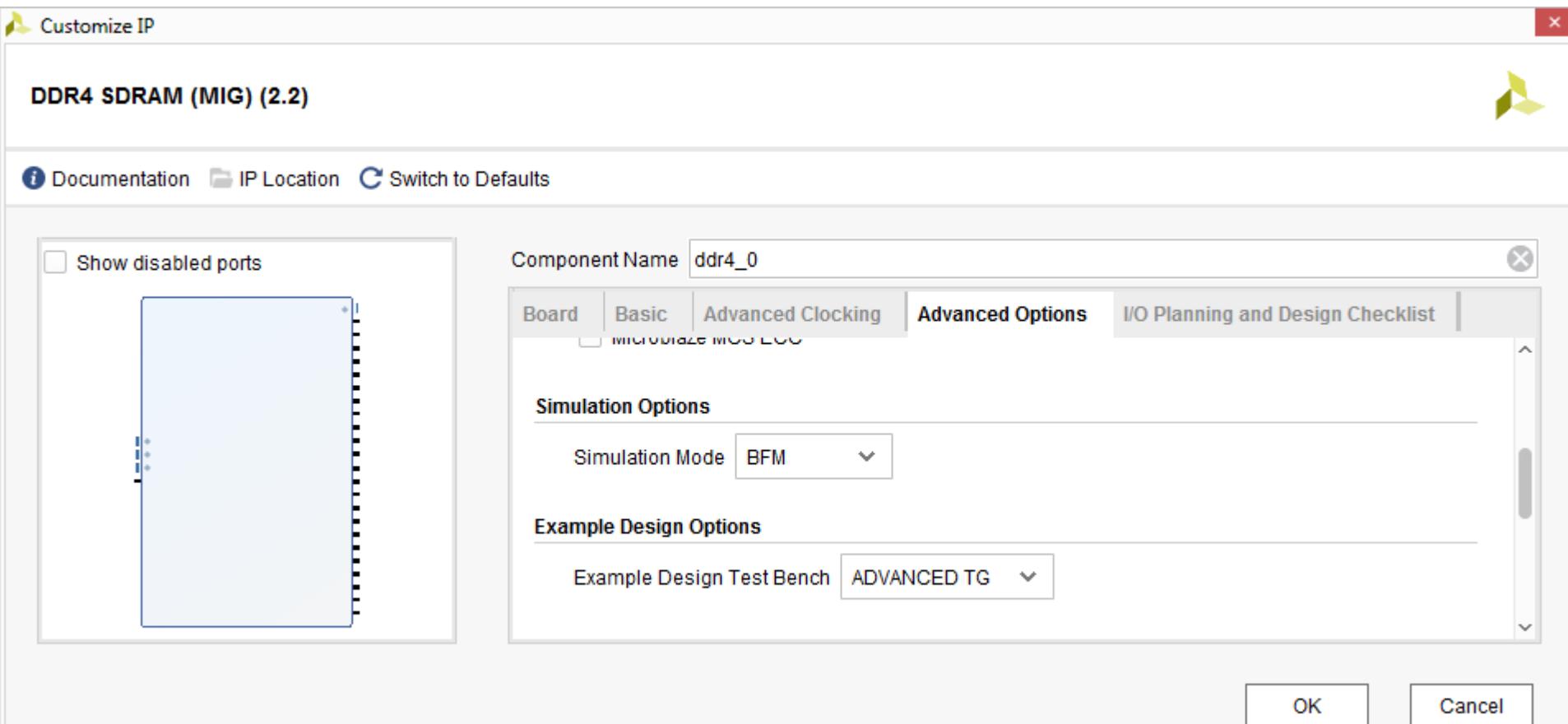
# Generate MIG DDR4 C1 Example Design

- Set the Debug Signals to **Enable**
- Scroll down



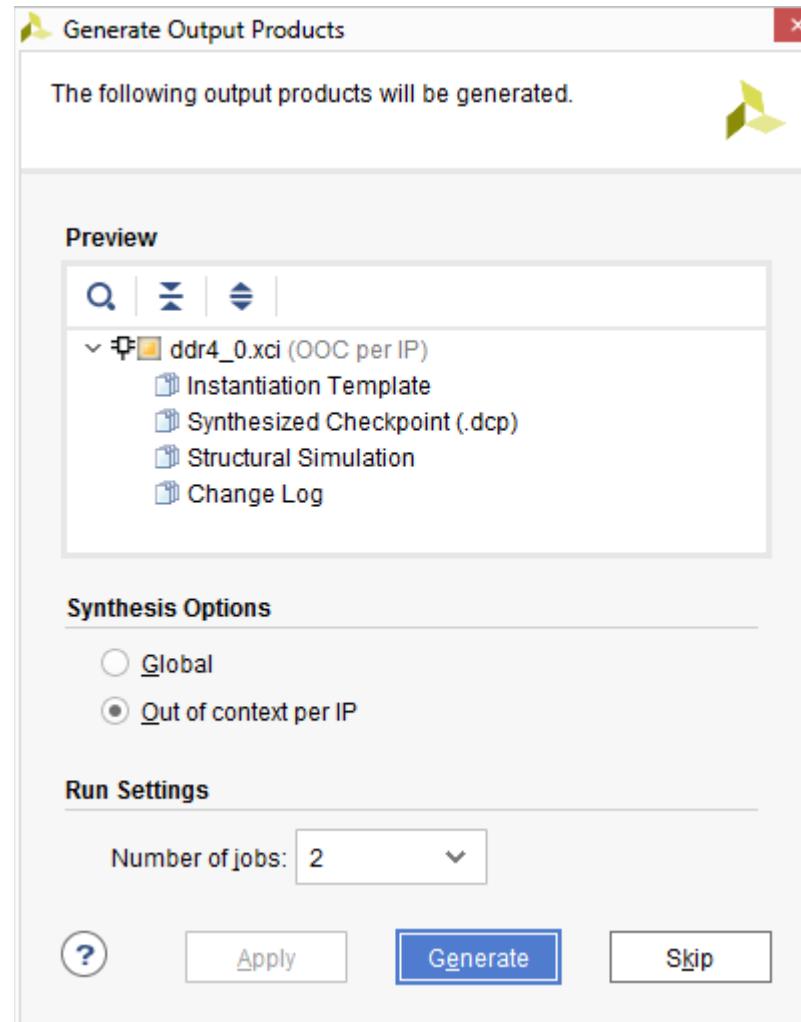
# Generate MIG DDR4 C1 Example Design

- Set the Example Design Test Bench to **ADVANCED TG**
- Click **OK**



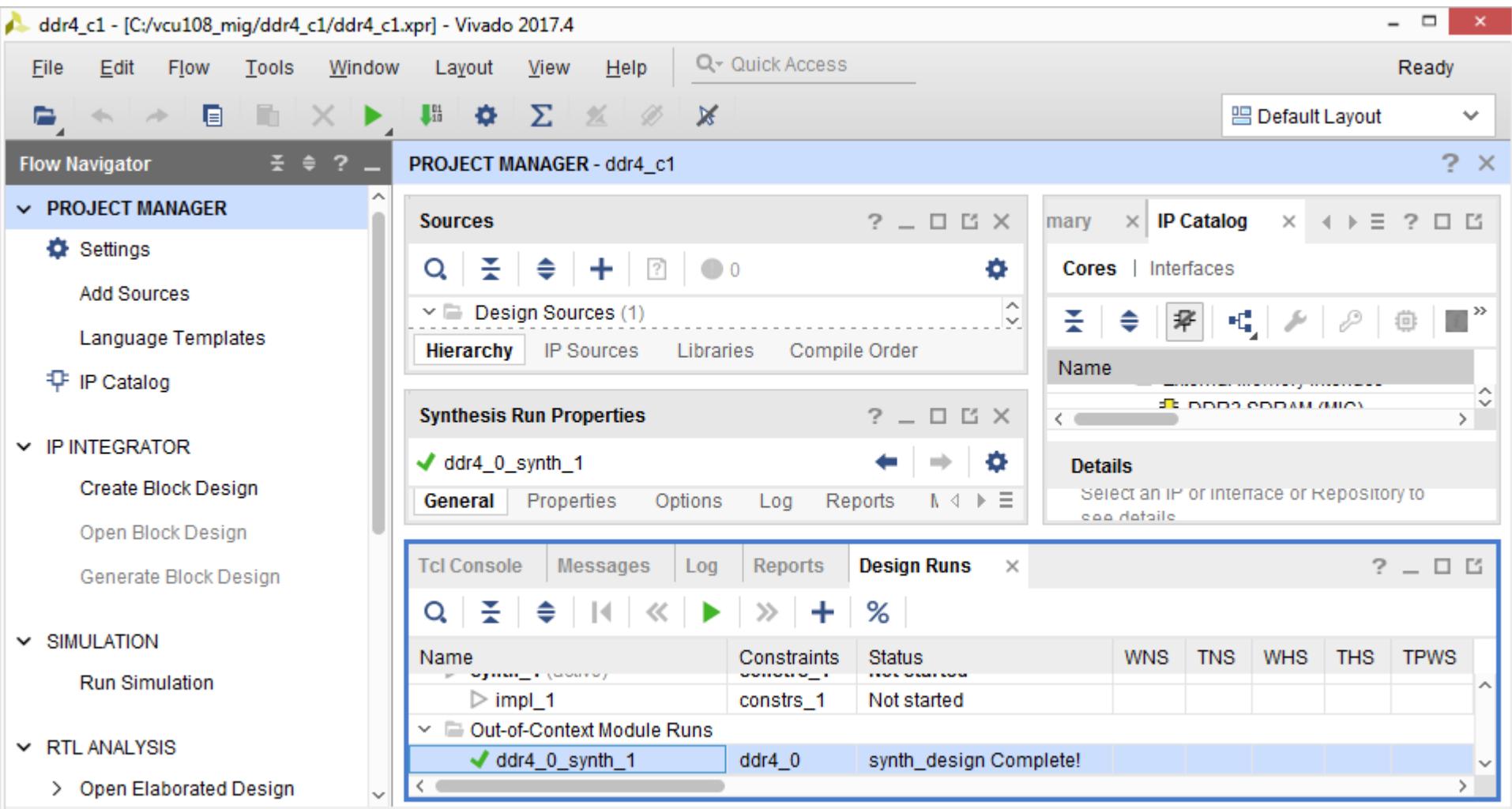
# Generate MIG DDR4 C1 Example Design

► Click Generate



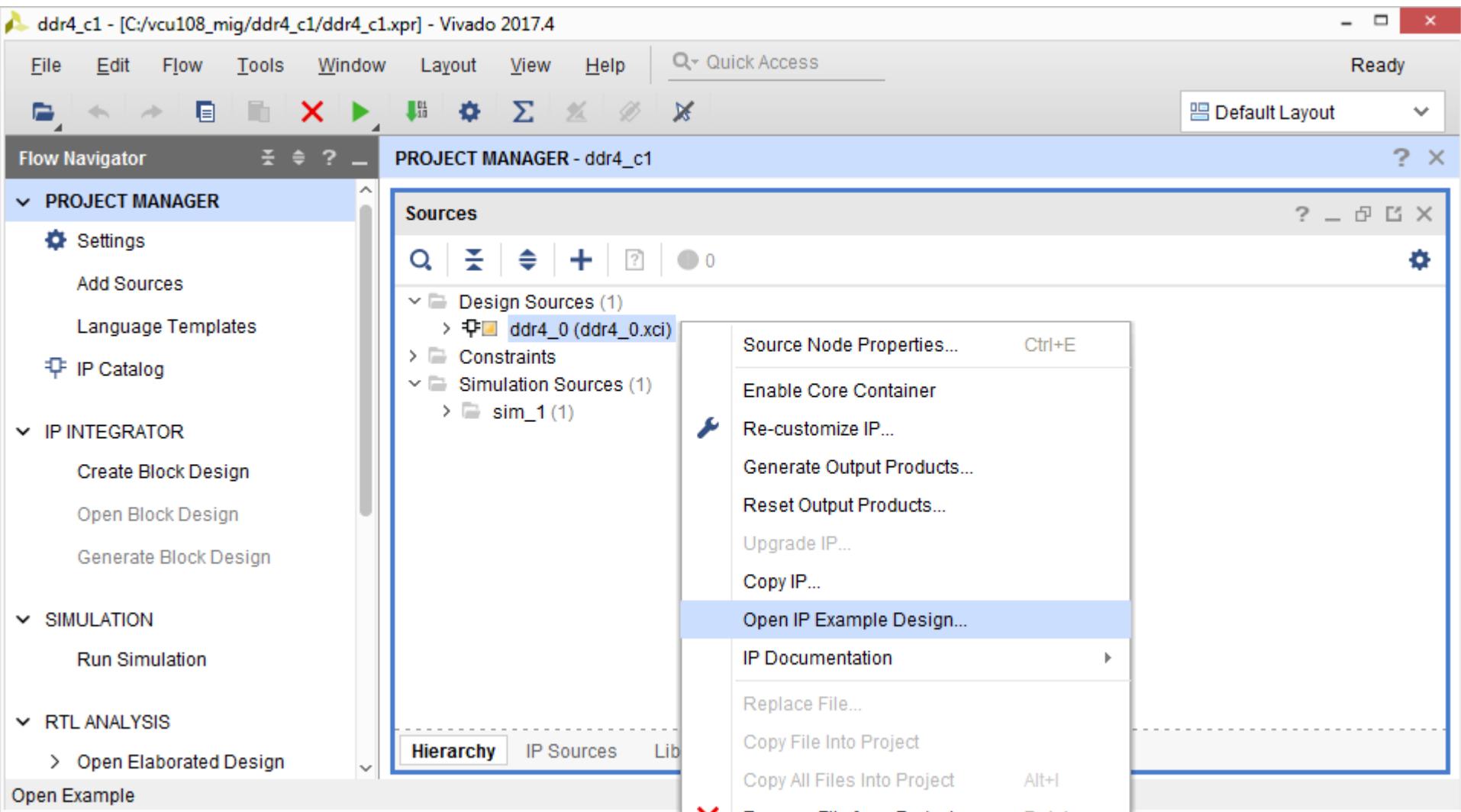
# Generate MIG DDR4 C1 Example Design

► Wait until checkmark appears on **ddr4\_0\_synth\_1**



# Compile Example Design

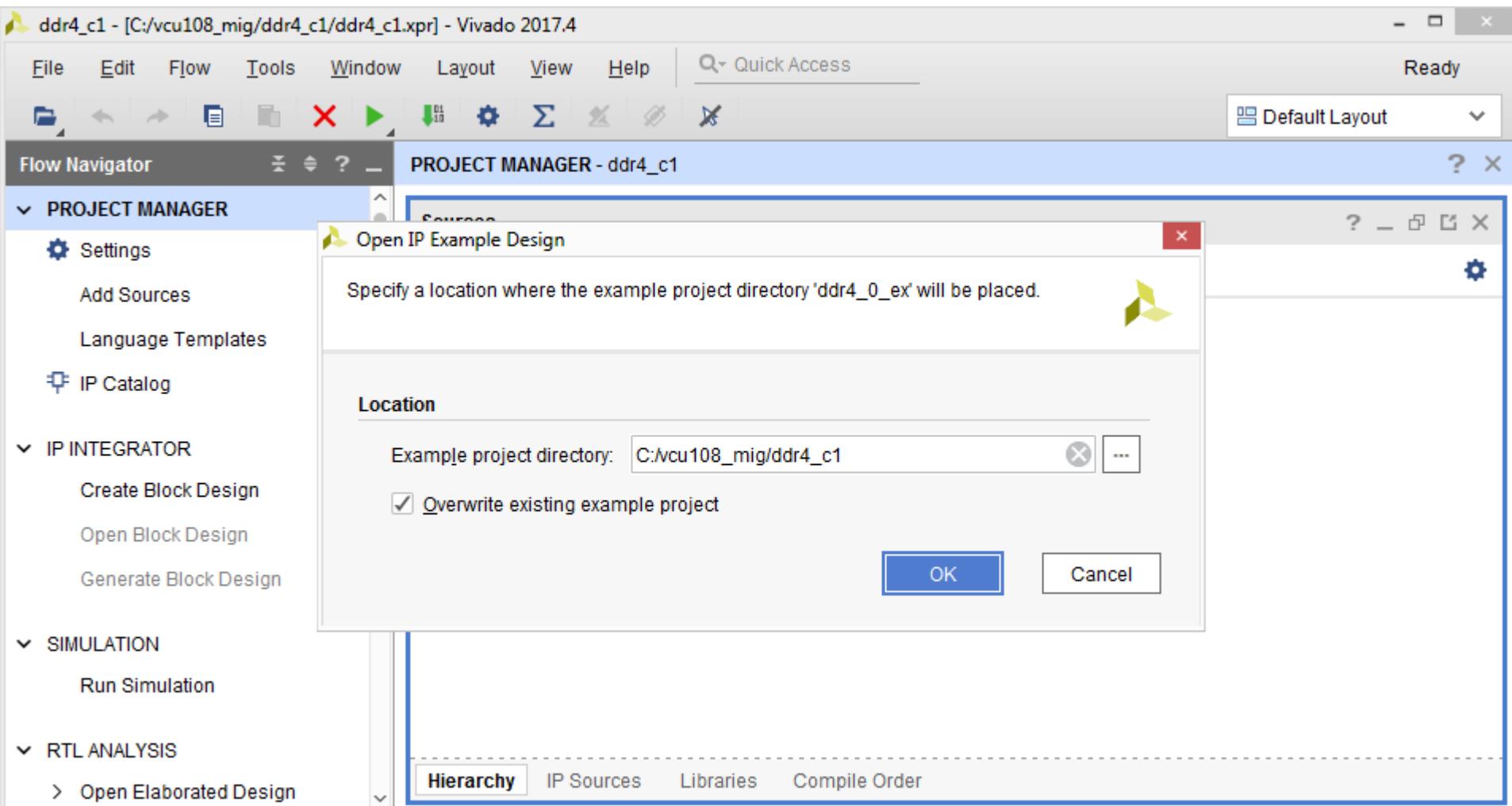
► Right click on **ddr4\_0** and select **Open IP Example Design...**



Note: Presentation applies to the VCU108

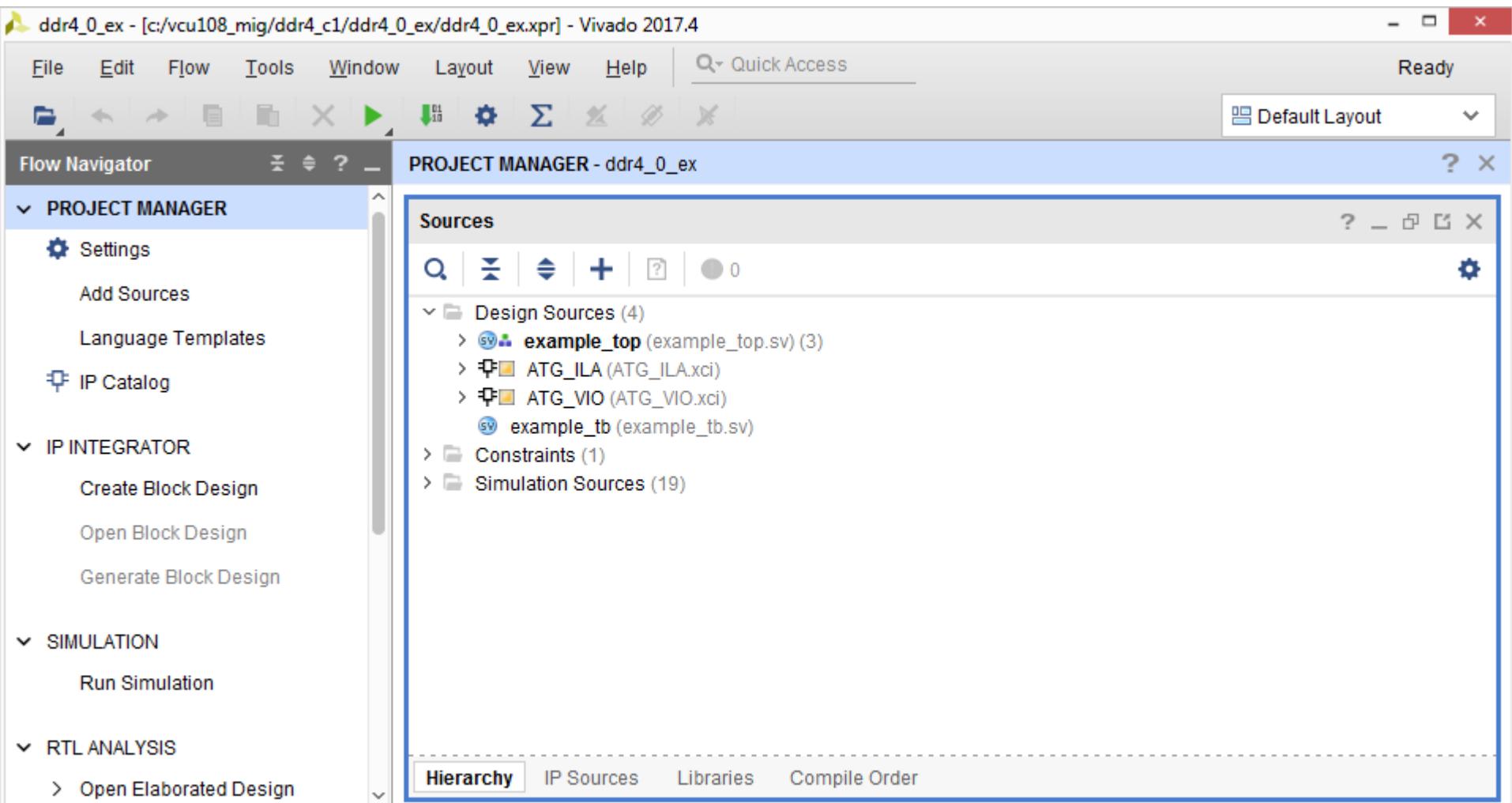
# Compile Example Design

► Set the location to C:/vcu108\_mig/ddr4\_c1 and click **OK**



# Compile Example Design

- A new project is created under <design path>/



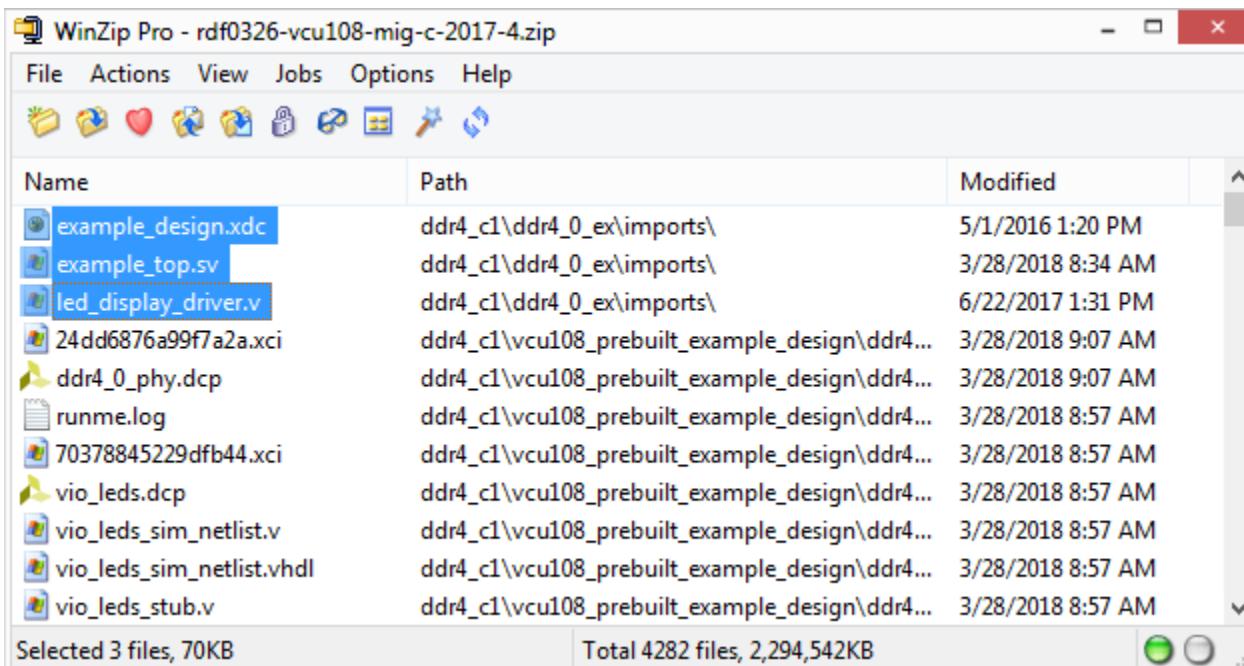
Note: The original project window can be closed

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# Modifications to Example Design

## ► From the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file

- Extract the **ddr4\_c1** files, **example\_design.xdc**, **example\_top.sv**, and **led\_display\_driver.v**
- Overwrite these three existing files in your **ddr4\_c1** MIG design
- Do this **after** creating the Example Design; changes only affect the Example Design



# Modifications to Example Design

## ► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs
- The following commands will add the led\_display\_driver.v and create the required VIO IP
- From the Tcl Console, run these commands:

```
add_files -norecurse
```

```
C:/vcu108_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
```

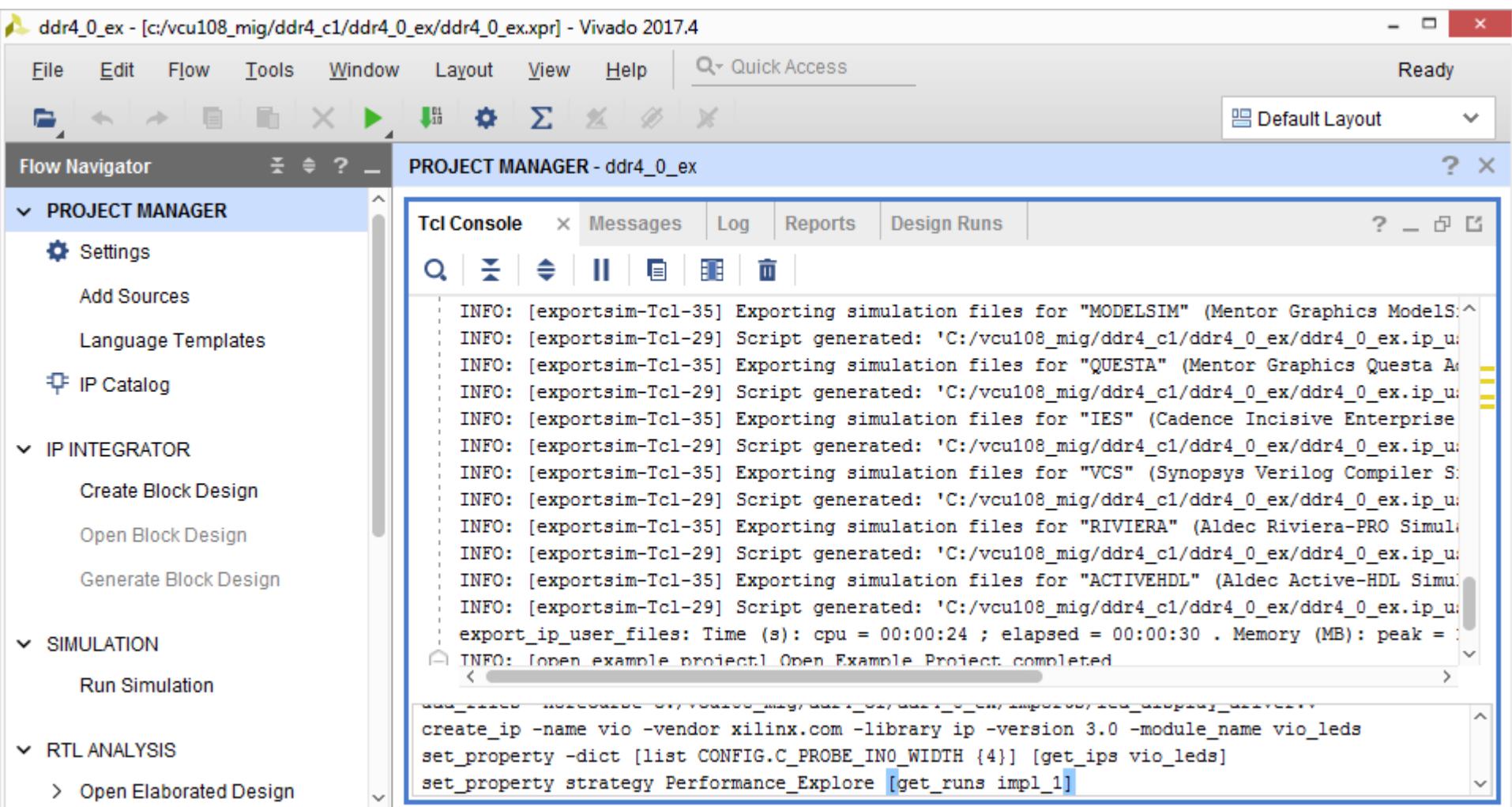
```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

```
set_property strategy Performance_Explore [get_runs impl_1]
```

# Modifications to Example Design

► Press enter after entering Tcl commands



# Modifications to Example Design

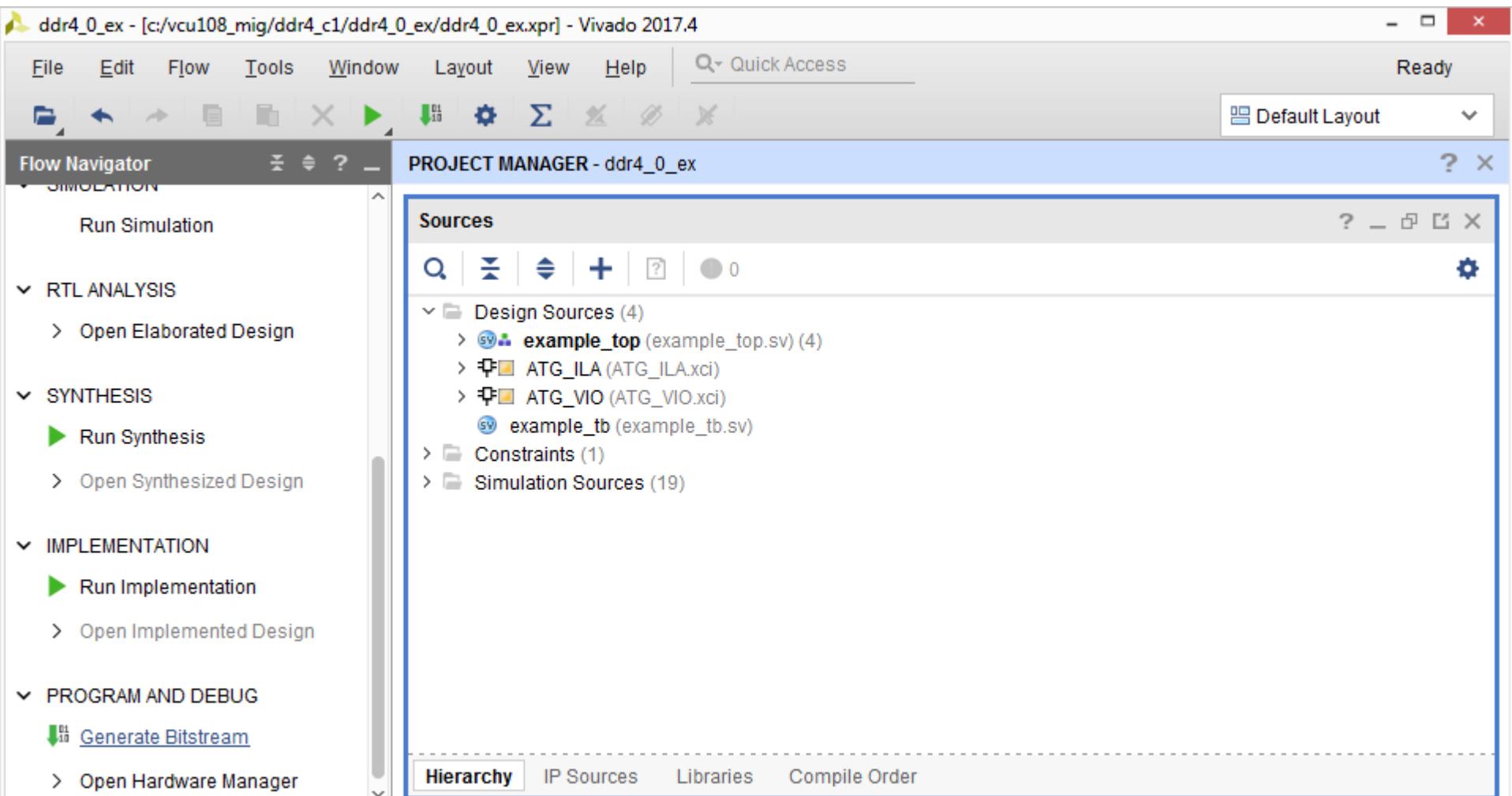
► Tcl commands completed successfully

The screenshot shows the Vivado 2017.4 interface with the project "ddr4\_0\_ex" open. The left sidebar contains sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The PROJECT MANAGER section is expanded, showing options like Settings, Add Sources, Language Templates, and IP Catalog. The central area is the PROJECT MANAGER - ddr4\_0\_ex window, which has tabs for Tcl Console, Messages, Log, Reports, and Design Runs. The Tcl Console tab is selected, displaying a series of blue-highlighted Tcl commands and their corresponding INFO log messages. The commands include exporting simulation files for Riviera-PRO and Active-HDL, generating scripts for Aldec tools, and performing various file operations and IP catalog updates. The log messages indicate the completion of these tasks.

```
INFO: [exportsim-Tcl-35] Exporting simulation files for "RIVIERA" (Aldec Riviera-PRO Simulator)
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu108_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.ip_u...
INFO: [exportsim-Tcl-35] Exporting simulation files for "ACTIVEHDL" (Aldec Active-HDL Simulator)
INFO: [exportsim-Tcl-29] Script generated: 'C:/vcu108_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.ip_u...
export_ip_user_files: Time (s): cpu = 00:00:24 ; elapsed = 00:00:30 . Memory (MB): peak = ...
INFO: [open_example_project] Open Example Project completed
update_compile_order -fileset sources_1
add_files -norecurse C:/vcu108_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
C:/vcu108_mig/ddr4_c1/ddr4_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name vio_leds
c:/vcu108_mig/ddr4_c1/ddr4_0_ex/ddr4_0_ex.srcs/sources_1/ip/vio_leds/vio_leds.xci
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
0
set_property strategy Performance_Explore [get_runs impl_1]
update_compile_order -fileset sources_1
```

# Compile Example Design

► Click on **Generate Bitstream**



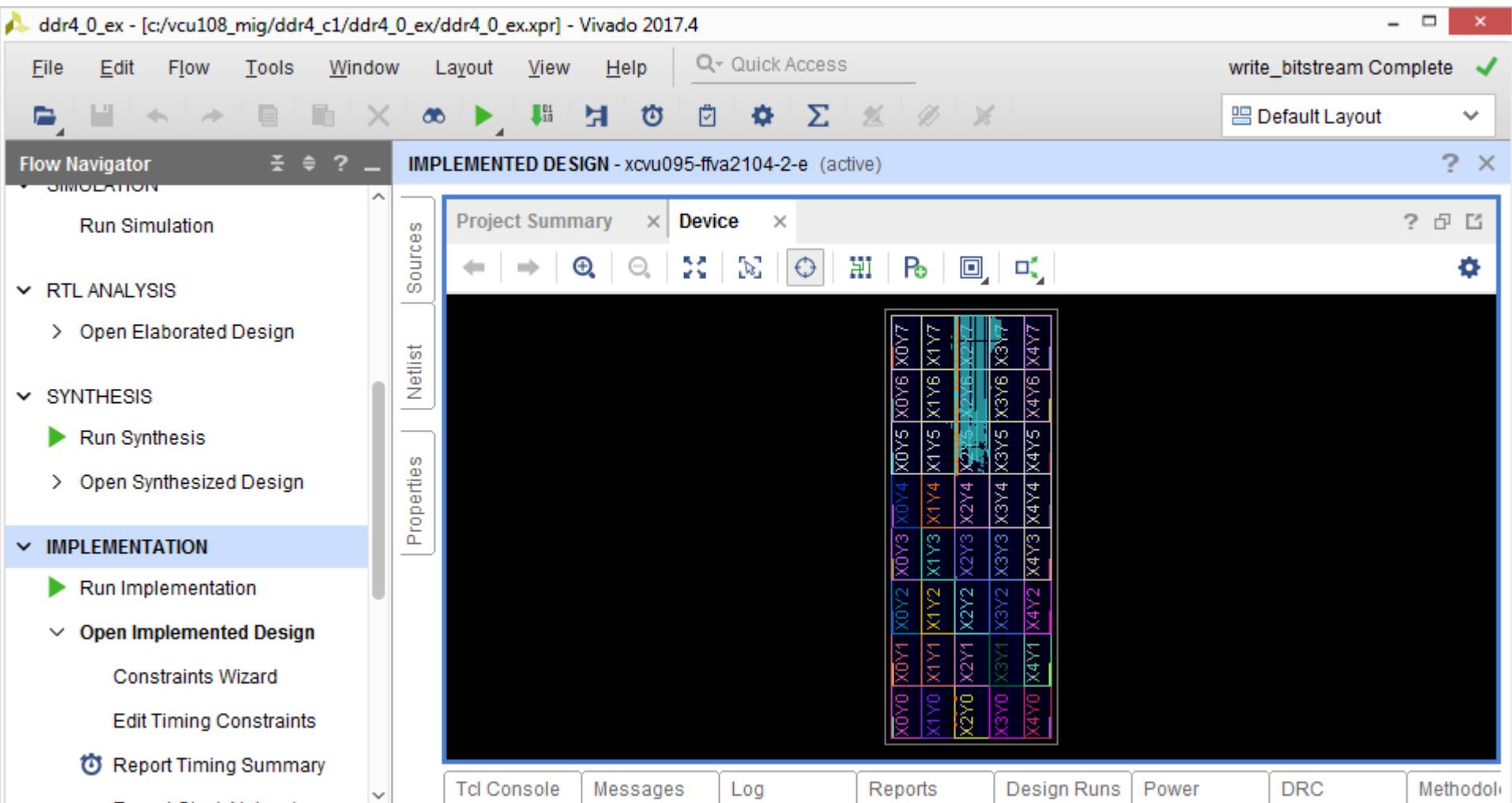
Generate a programming file after implementation

Note: Presentation applies to the VCU108

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# Compile Example Design

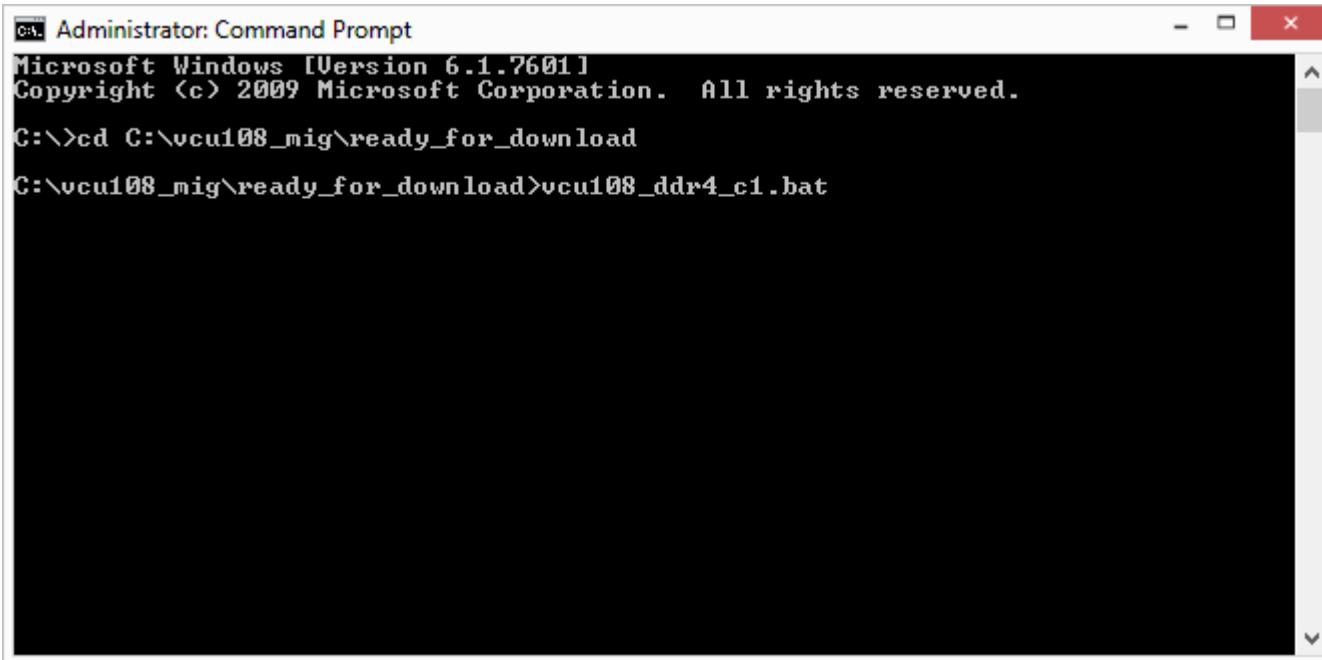
► Open and view the Implemented Design



# Run MIG Example Design

- ▶ From a Command Prompt, type:

```
cd C:\vcu108_mig\ready_for_download  
vcu108_ddr4_c1.bat
```

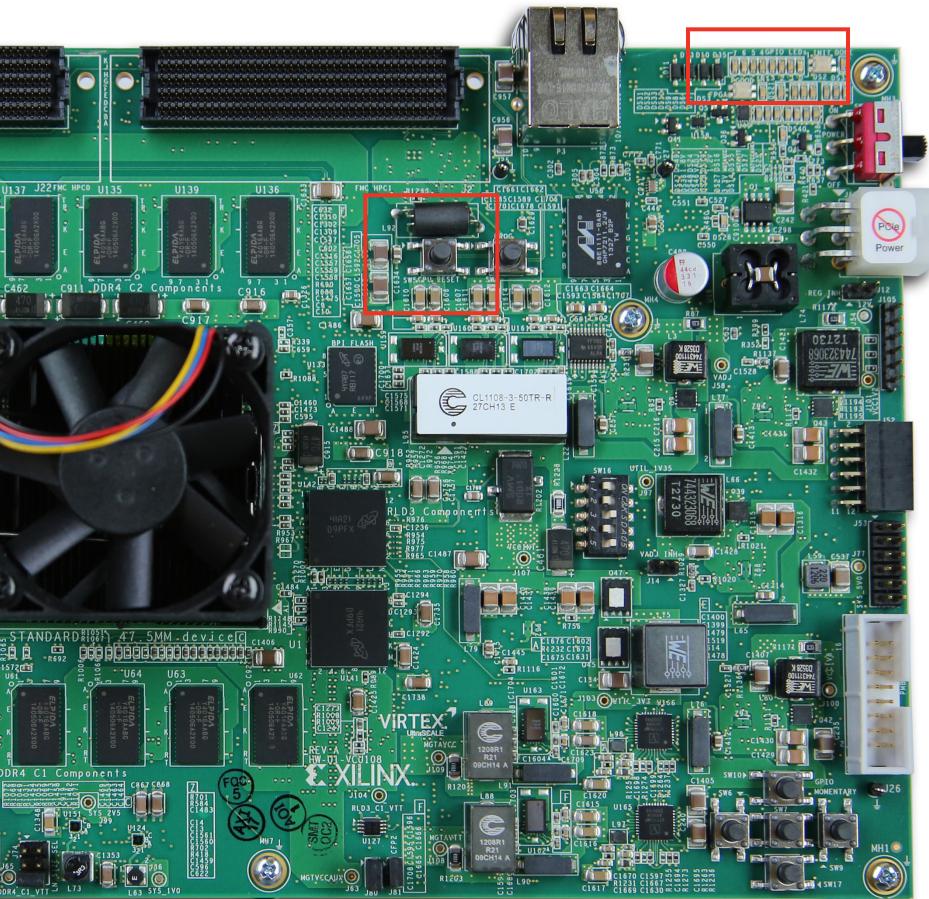


The screenshot shows a Windows Command Prompt window with the title "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu108_mig\ready_for_download
C:\vcu108_mig\ready_for_download>vcu108_ddr4_c1.bat
```

# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset

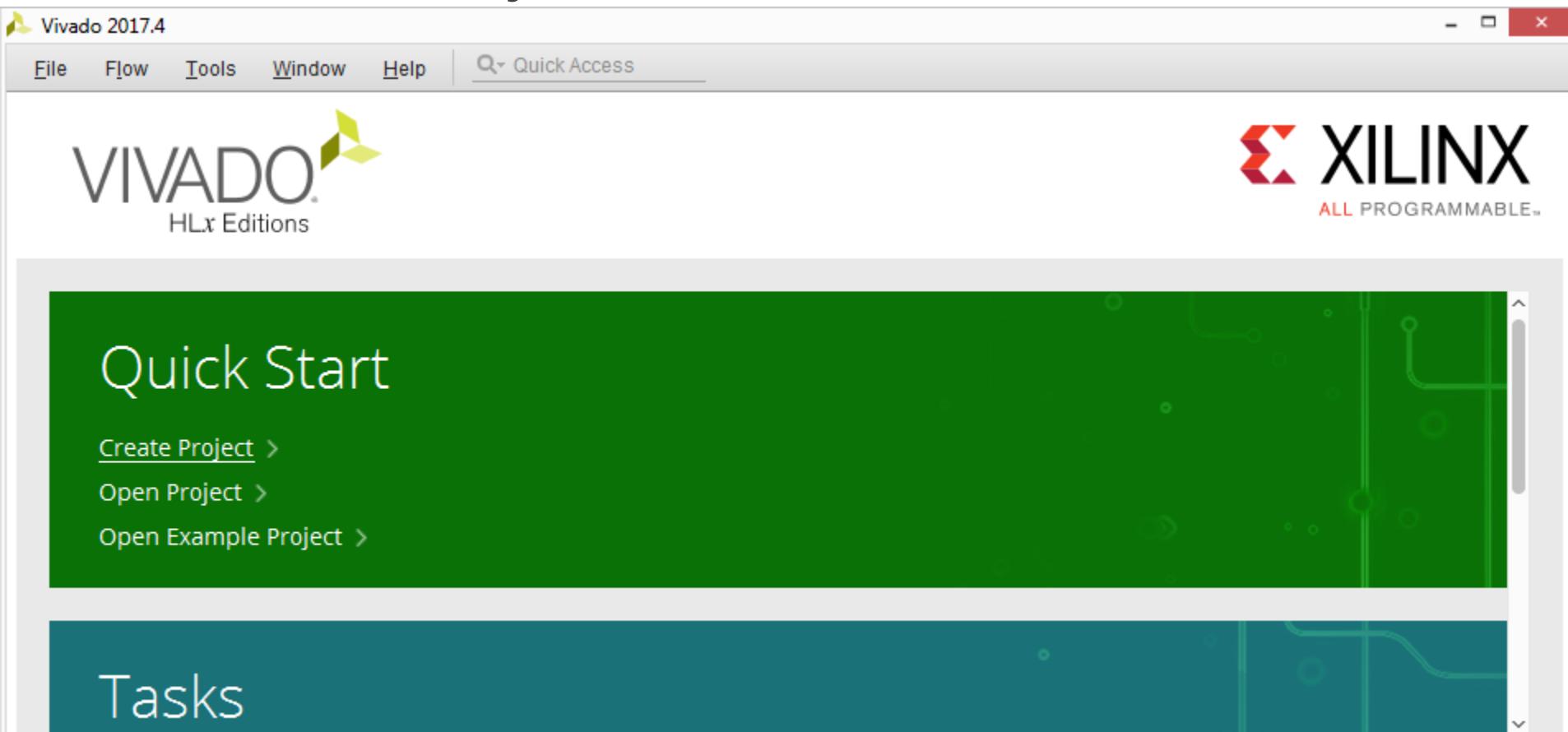
# Generate MIG DDR4 C2 Example Design

# Generate MIG DDR4 C2 Example Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.4 → Vivado

► Select Create Project



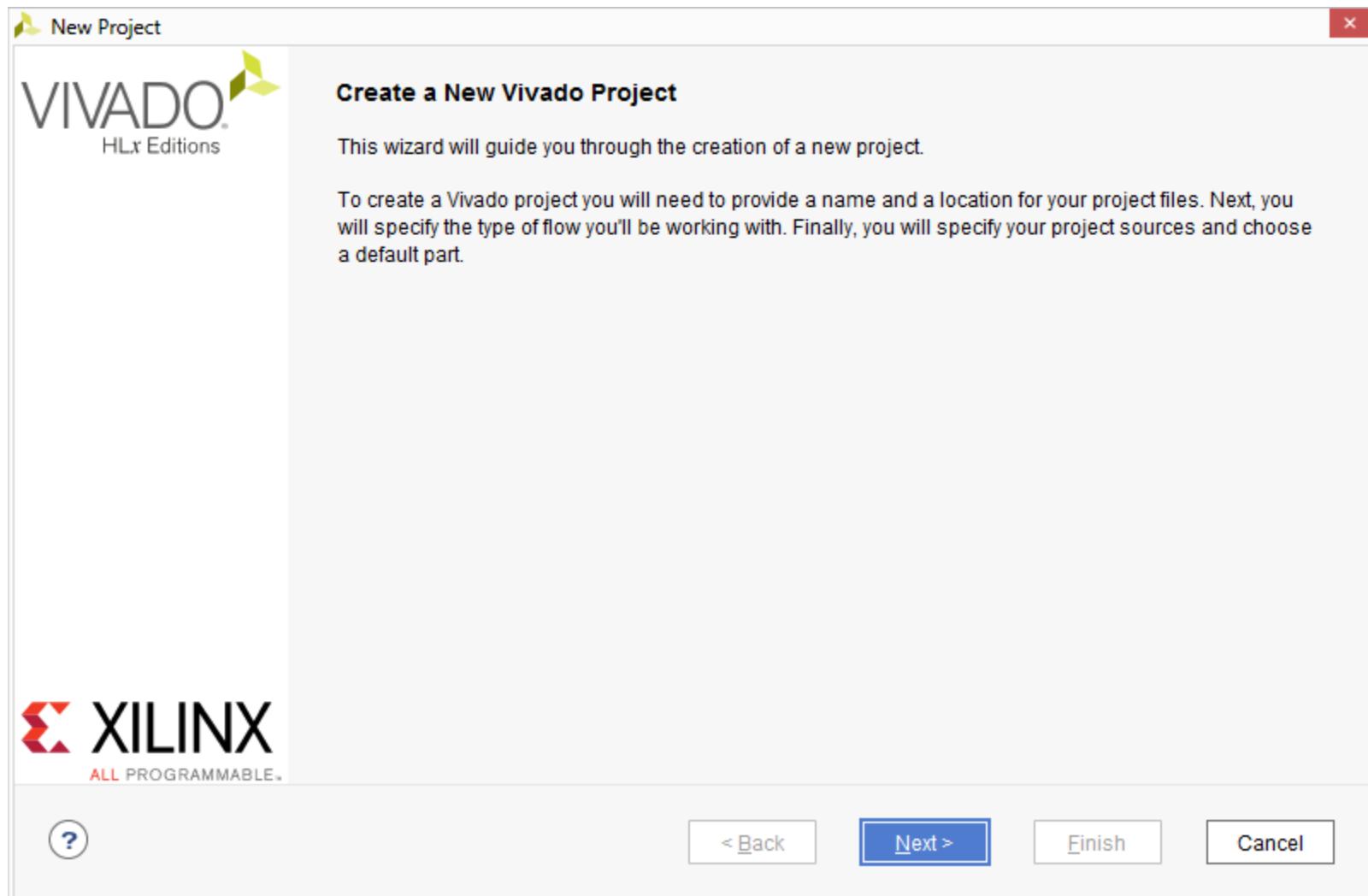
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU108

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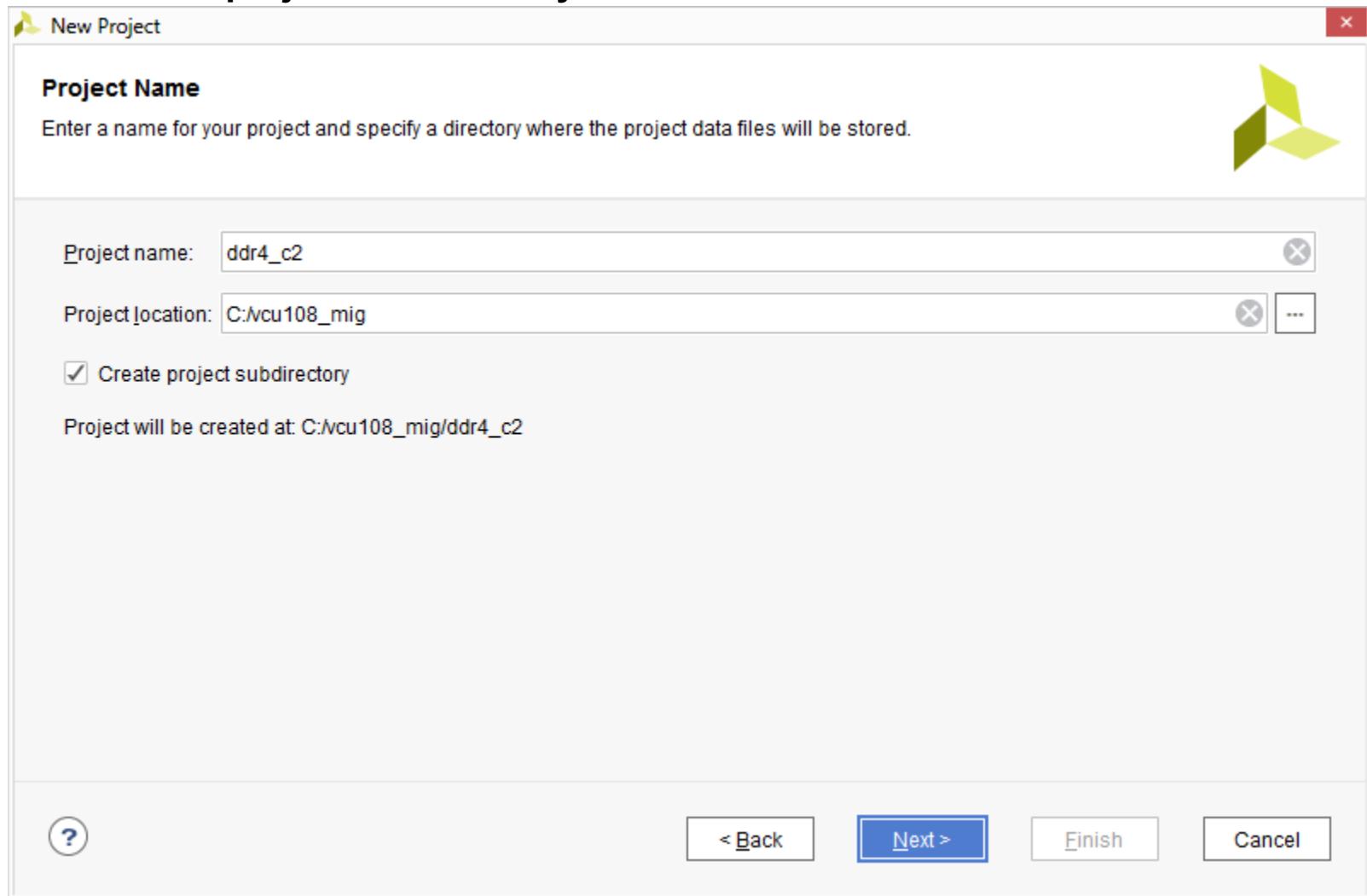
# Generate MIG DDR4 C2 Example Design

► Click Next



# Generate MIG DDR4 C2 Example Design

- Set the Project name to **ddr4\_c2** and location to **C:/vcu108\_mig**
  - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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# Generate MIG DDR4 C2 Example Design

## ► Select RTL Project

- Select **Do not specify sources at this time**

New Project

**Project Type**  
Specify the type of project to create.



RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Generate MIG DDR4 C2 Example Design

► Under Boards, select the VCU108 Evaluation Platform

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

Filter/ Preview

Vendor: All  
Display Name: All  
Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2
<b>Virtex-UltraScale VCU108 Evaluation Platform</b>	xilinx.com	1.0	<b>xcvu095-ffva2104-2-e</b>
Virtex-UltraScale VCU110 Evaluation Platform	xilinx.com	1.0	xcvu190-flac2104-2-e

No Board Connectors

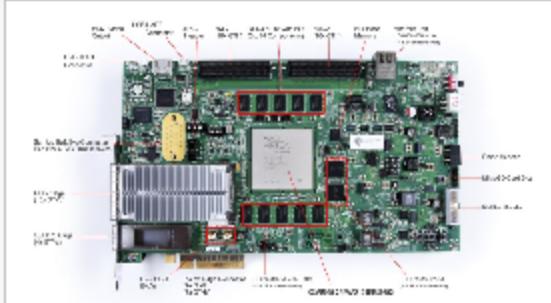
?

< Back

Next >

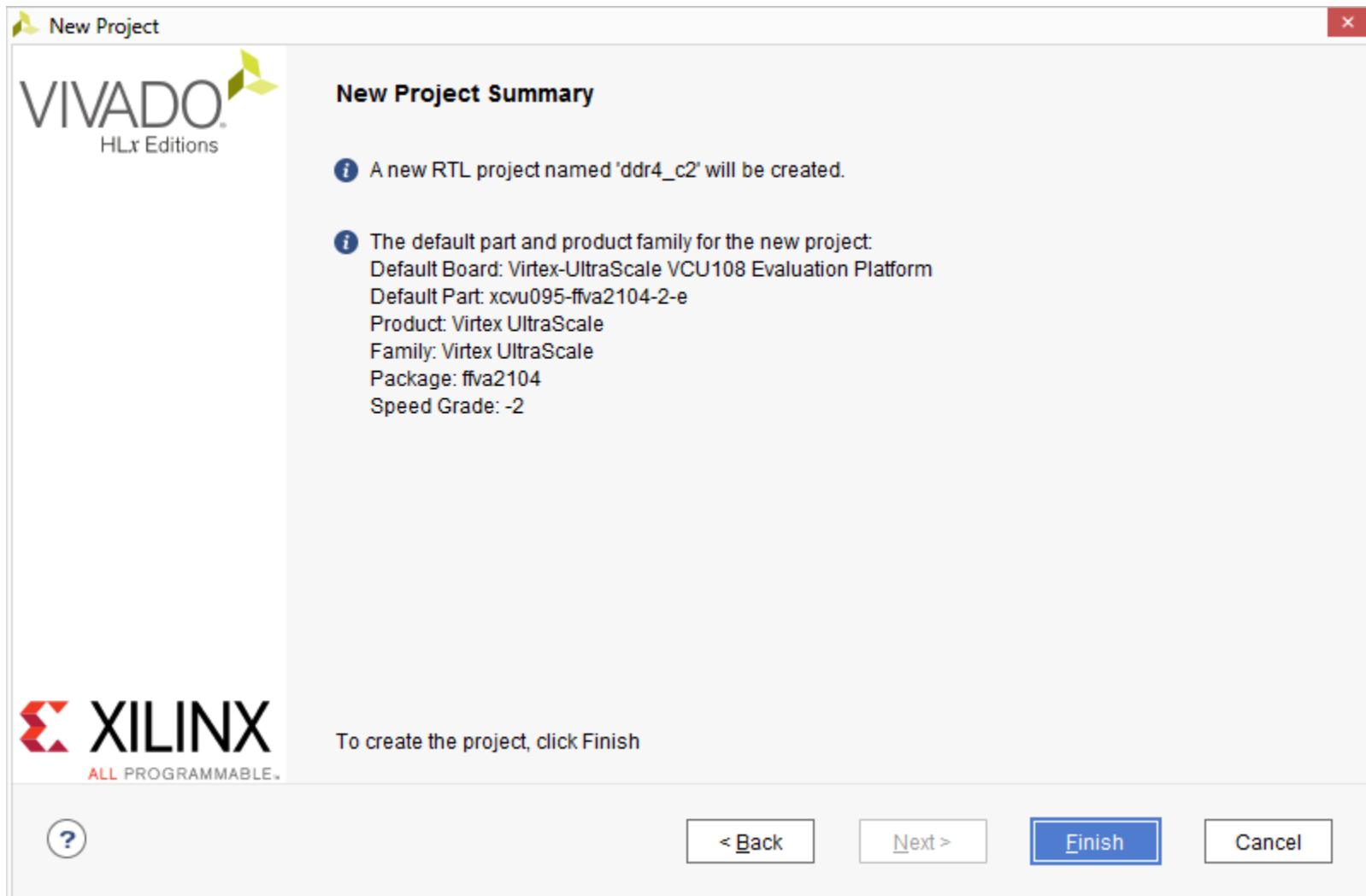
Finish

Cancel



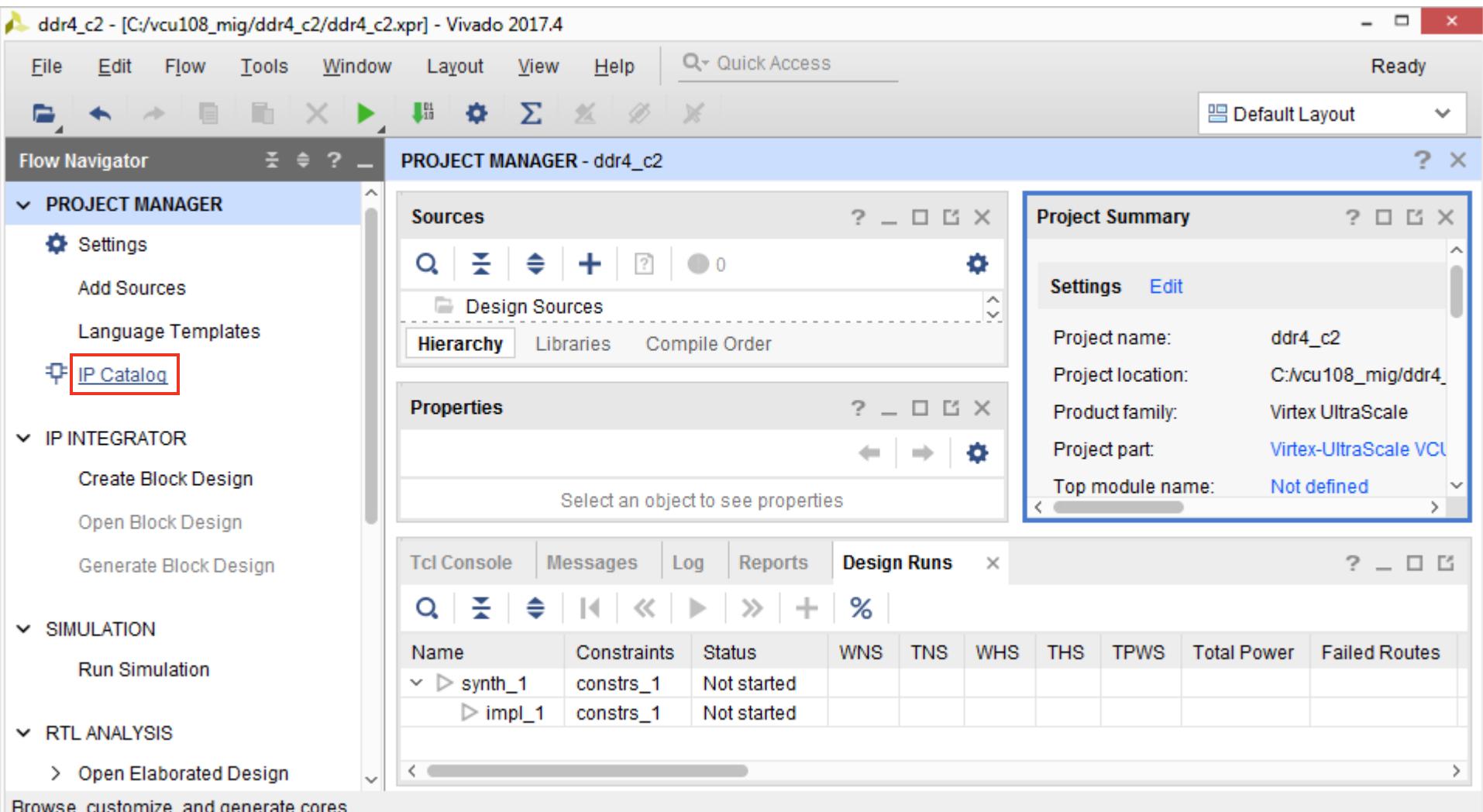
# Generate MIG DDR4 C2 Example Design

► Click Finish



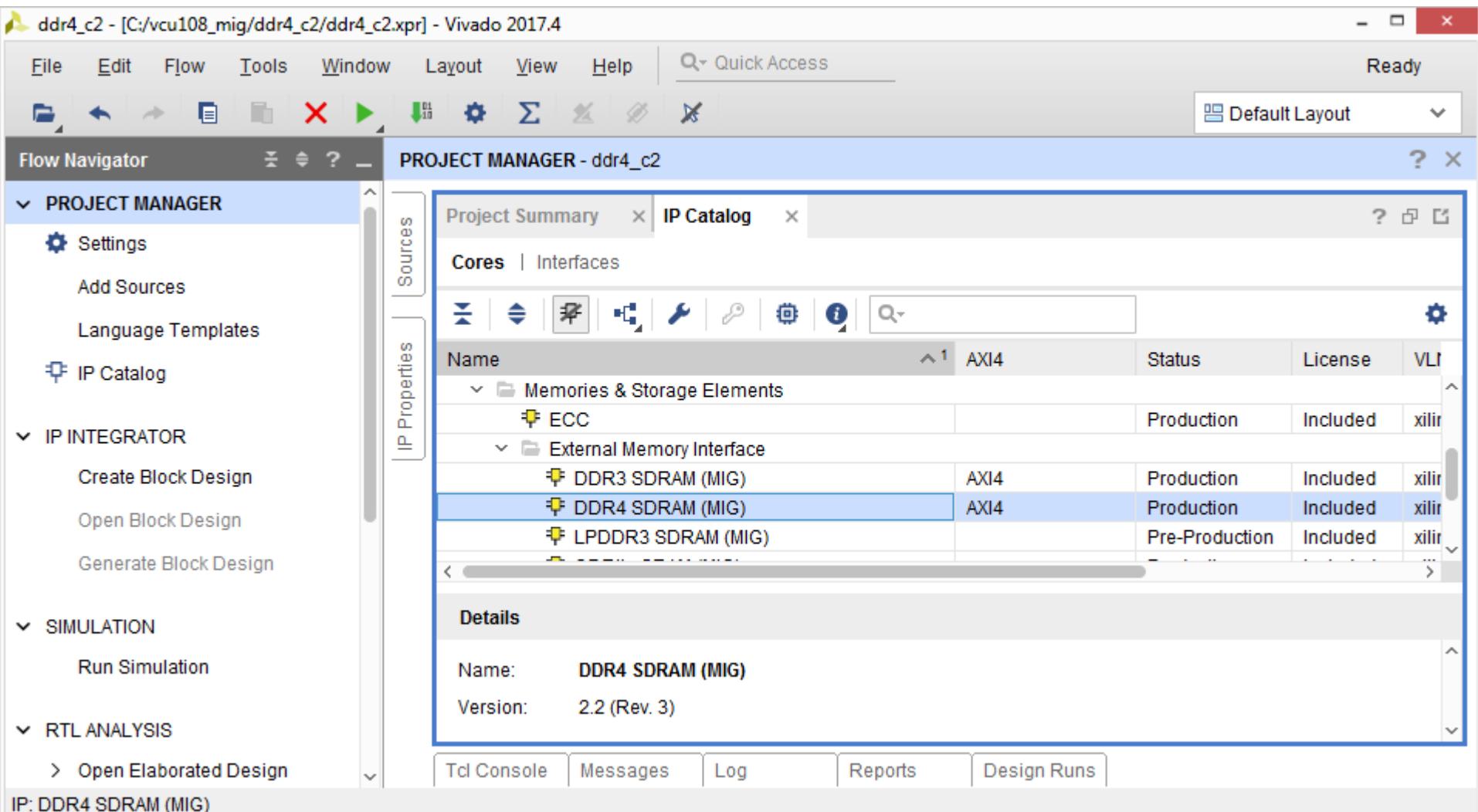
# Generate MIG DDR4 C2 Example Design

► Click on IP Catalog



# Generate MIG DDR4 C2 Example Design

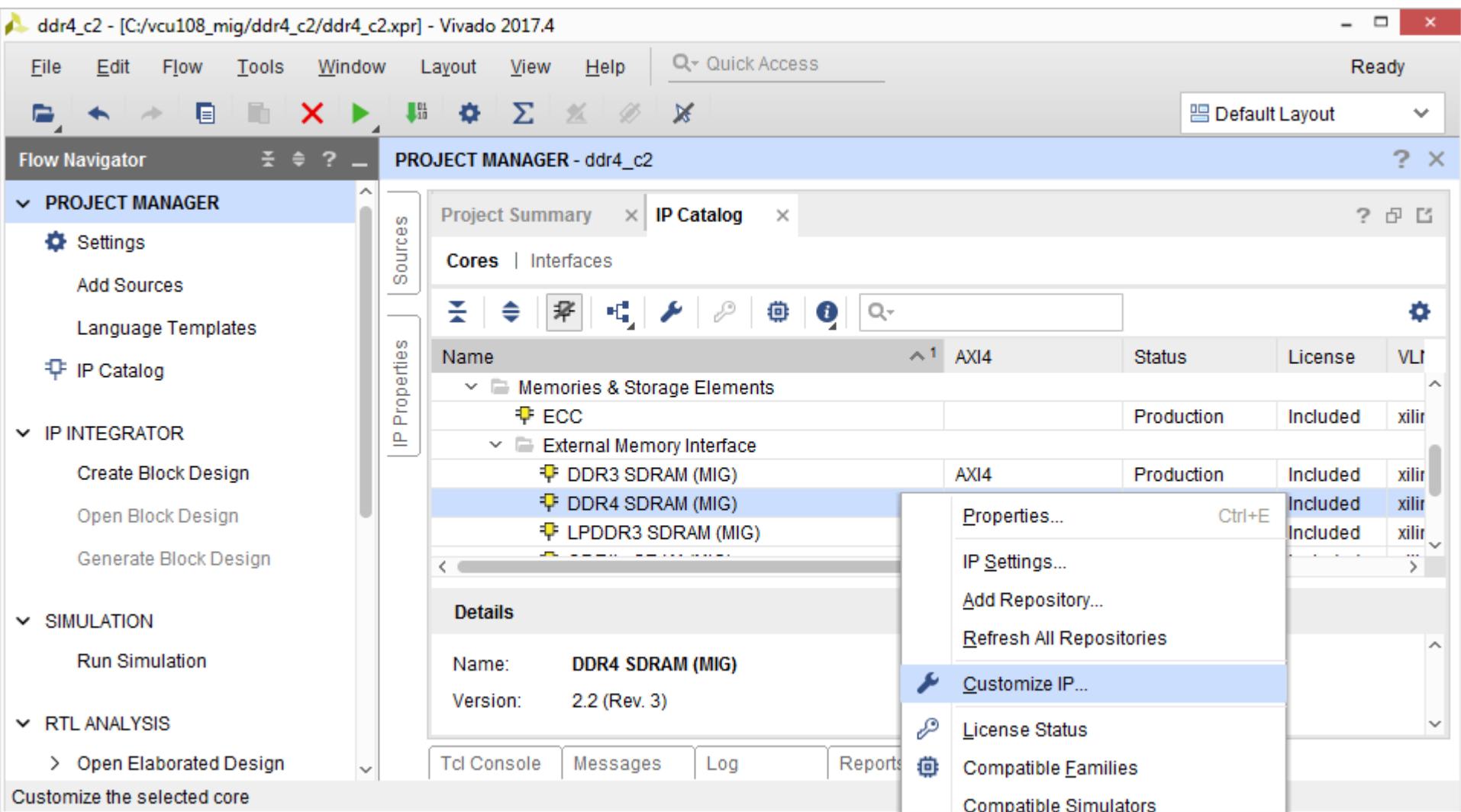
## ► Select DDR4 SDRAM (MIG), v2.2



# Generate MIG DDR4 C2 Example Design

► Right click on **DDR4 SDRAM (MIG)**

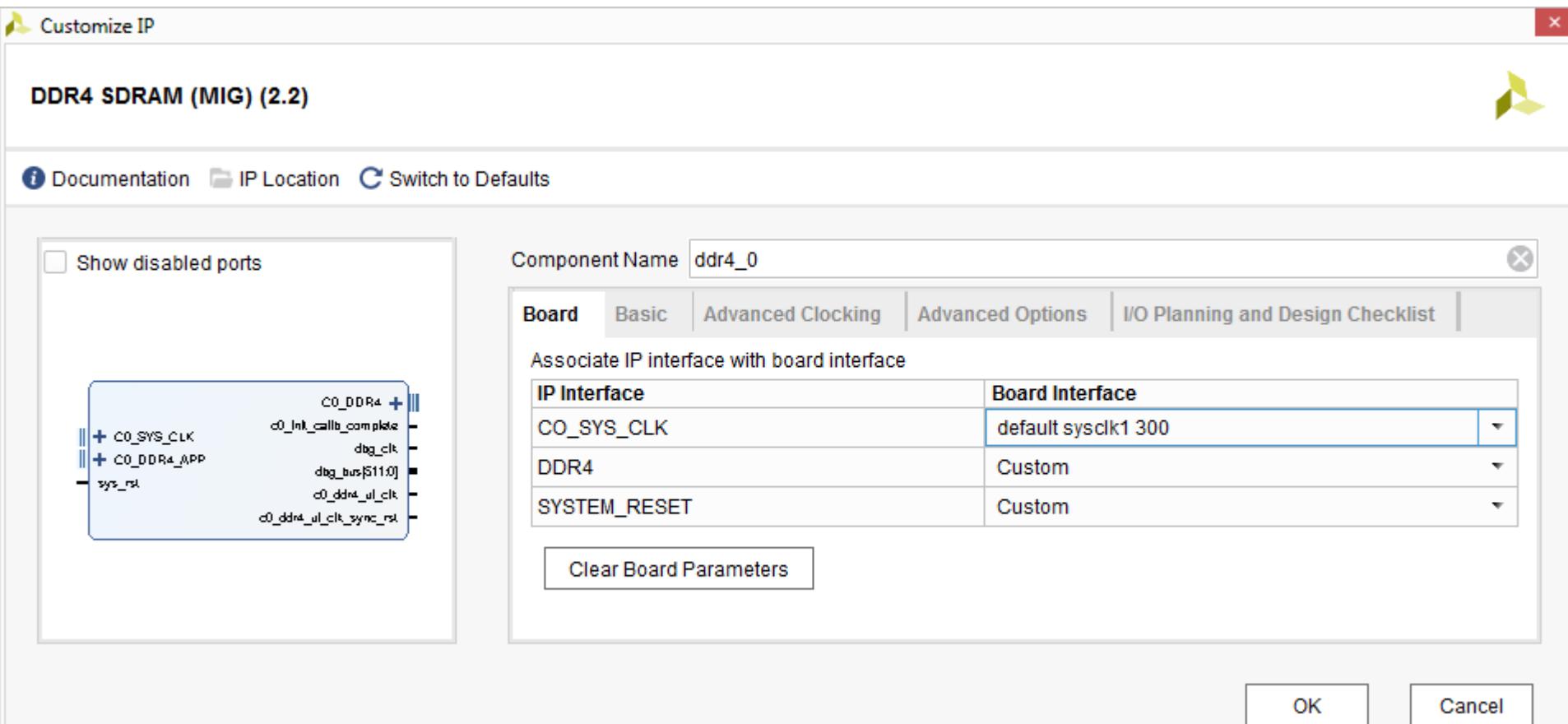
- Select **Customize IP**



# Generate MIG DDR4 C2 Example Design

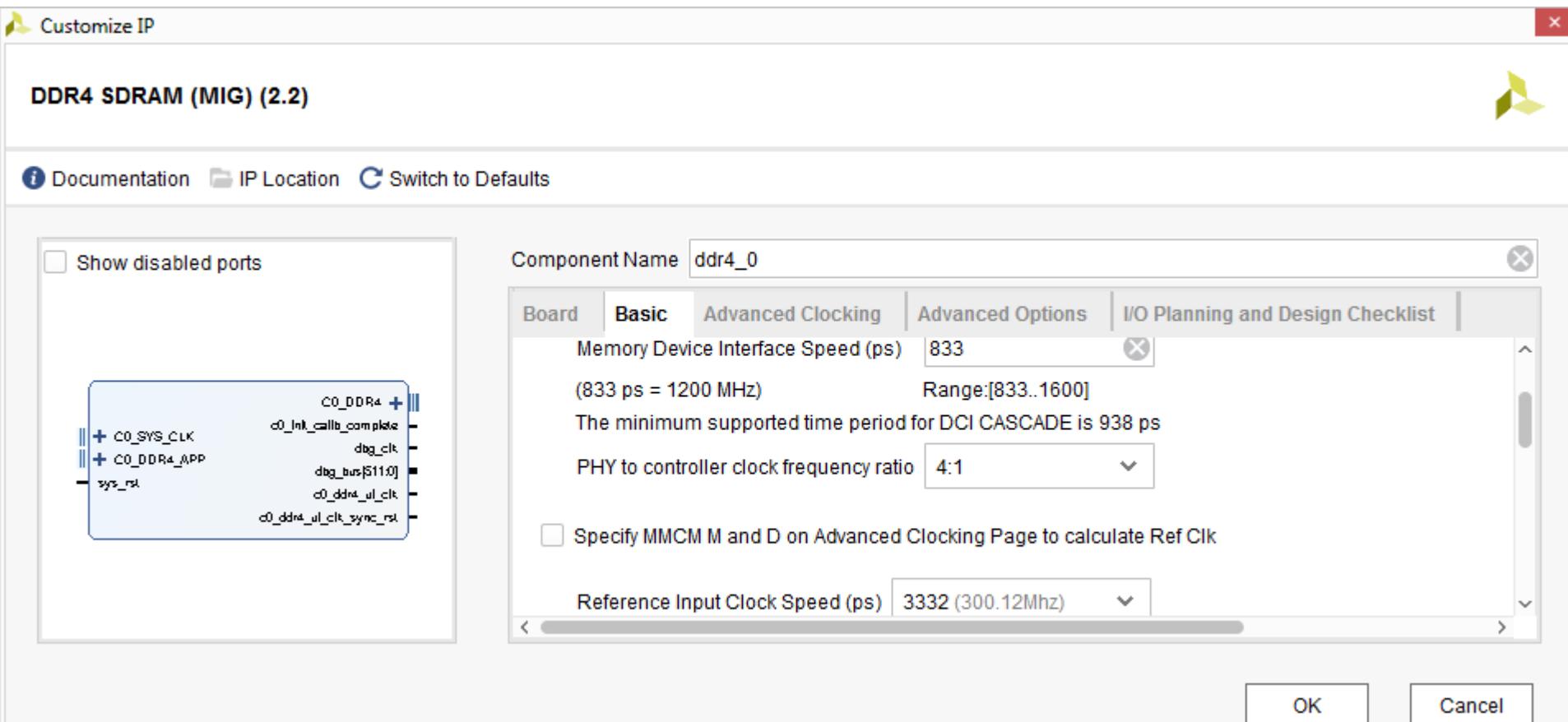
► Under the **Board** tab, set the DDR4 interfaces

- Set C0\_SYS\_CLK to **default sysclk1 300**
- Set C0\_DDR4 to **Custom**
- Set SYSTEM\_RESET to **Custom**



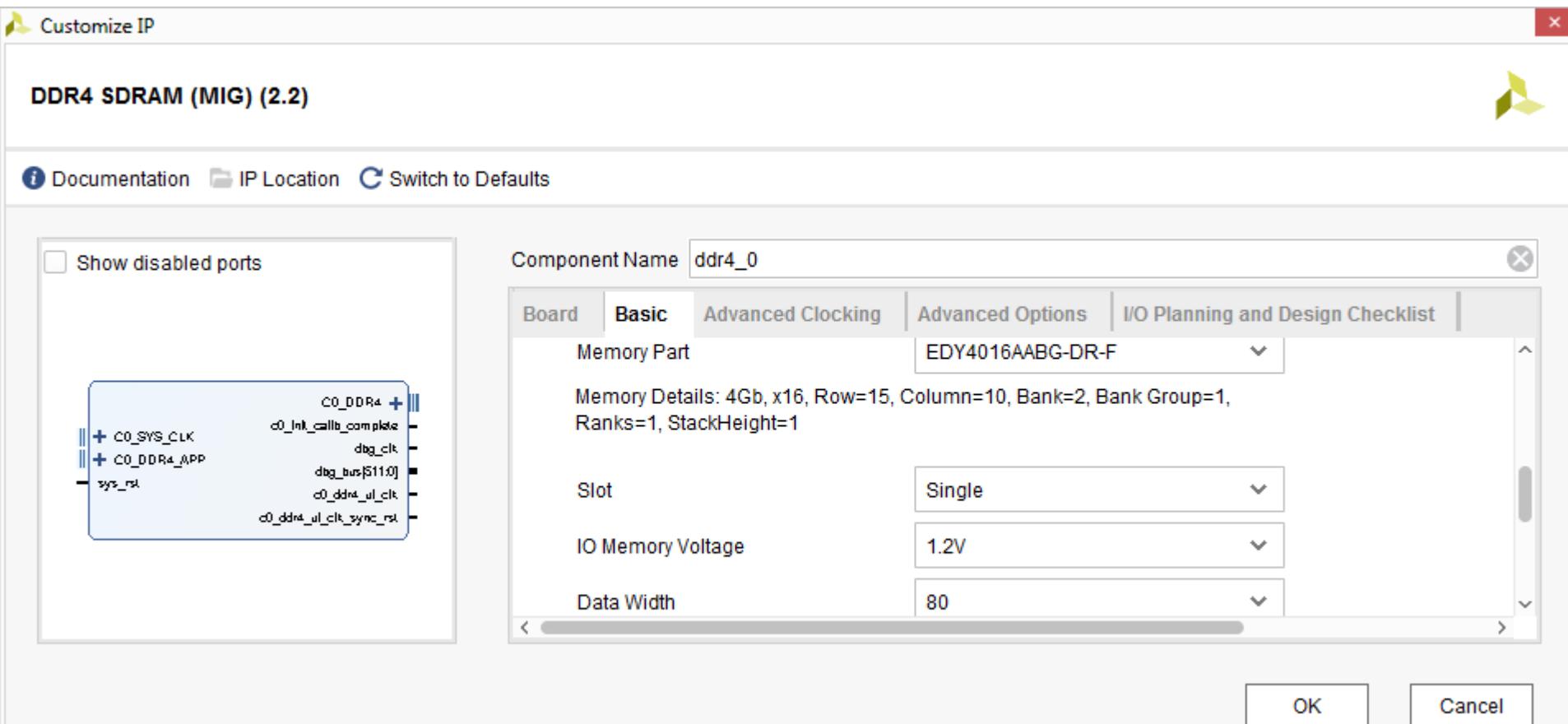
# Generate MIG DDR4 C2 Example Design

- Set Clock period to **833** for 2400 Mb/s operation.
- Set the Input Clock to **3332** ps for 300 MHz
- Scroll down



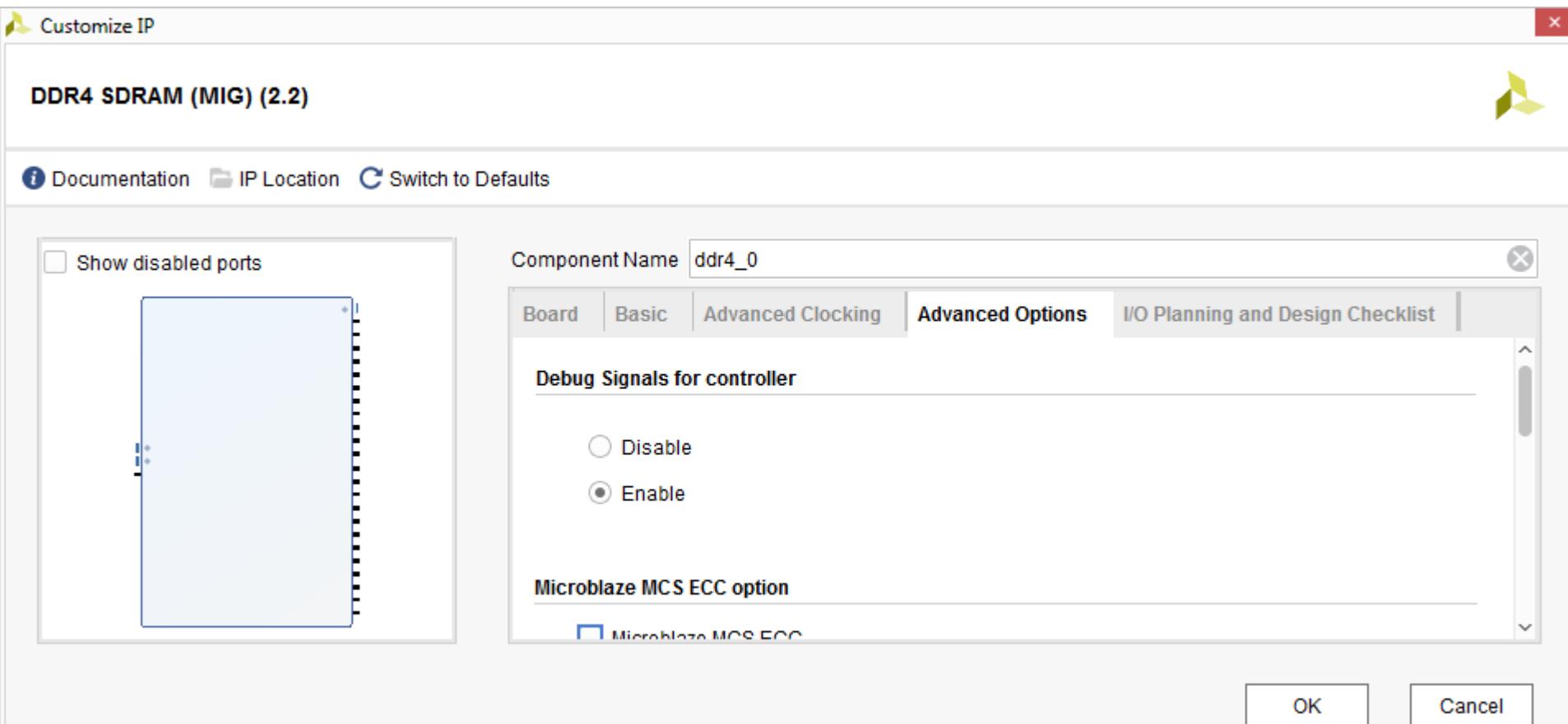
# Generate MIG DDR4 C2 Example Design

- Select the part **EDY4016AABG-DR-F**
- Set the Data Width to **80** and click the **Advanced Options** tab



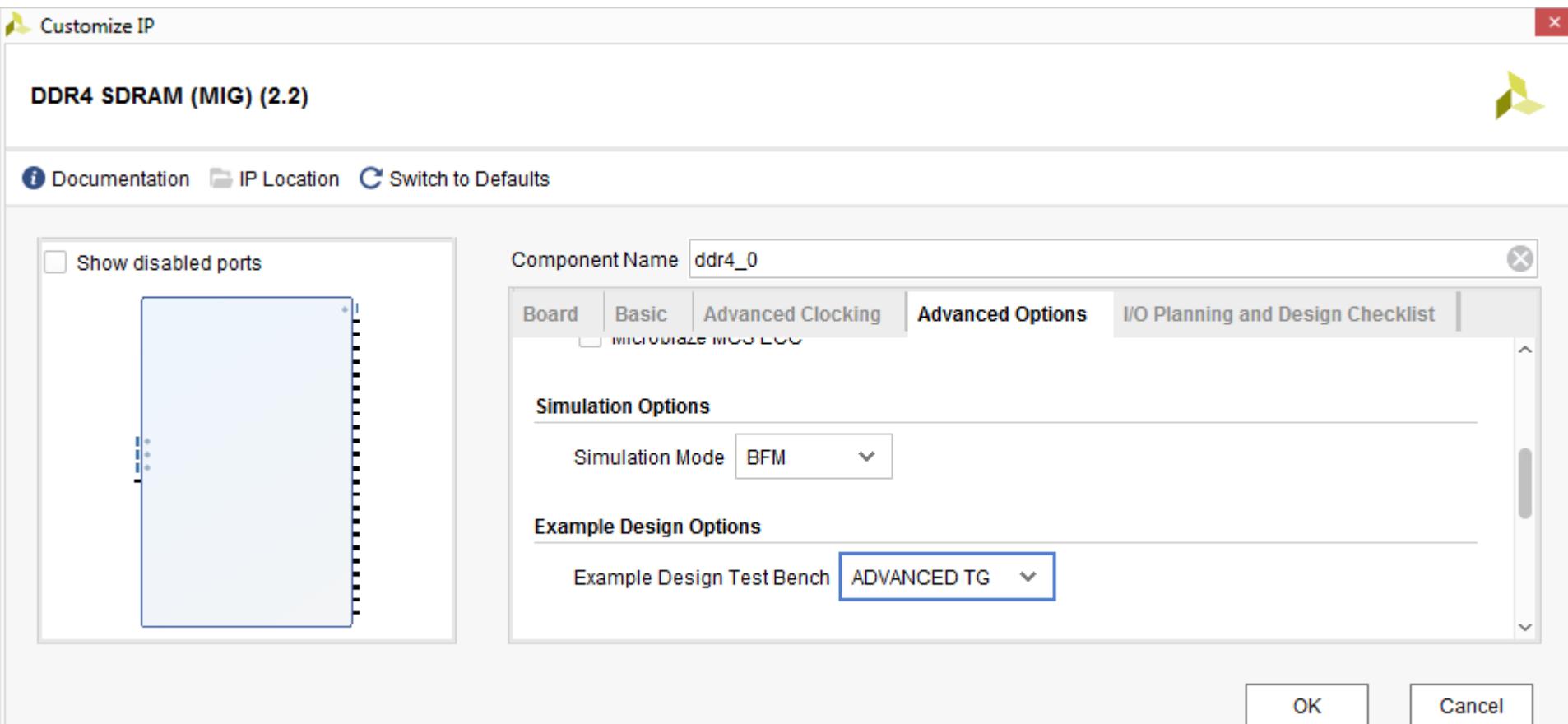
# Generate MIG DDR4 C2 Example Design

- Set the Debug Signals to **Enable**
- Scroll down



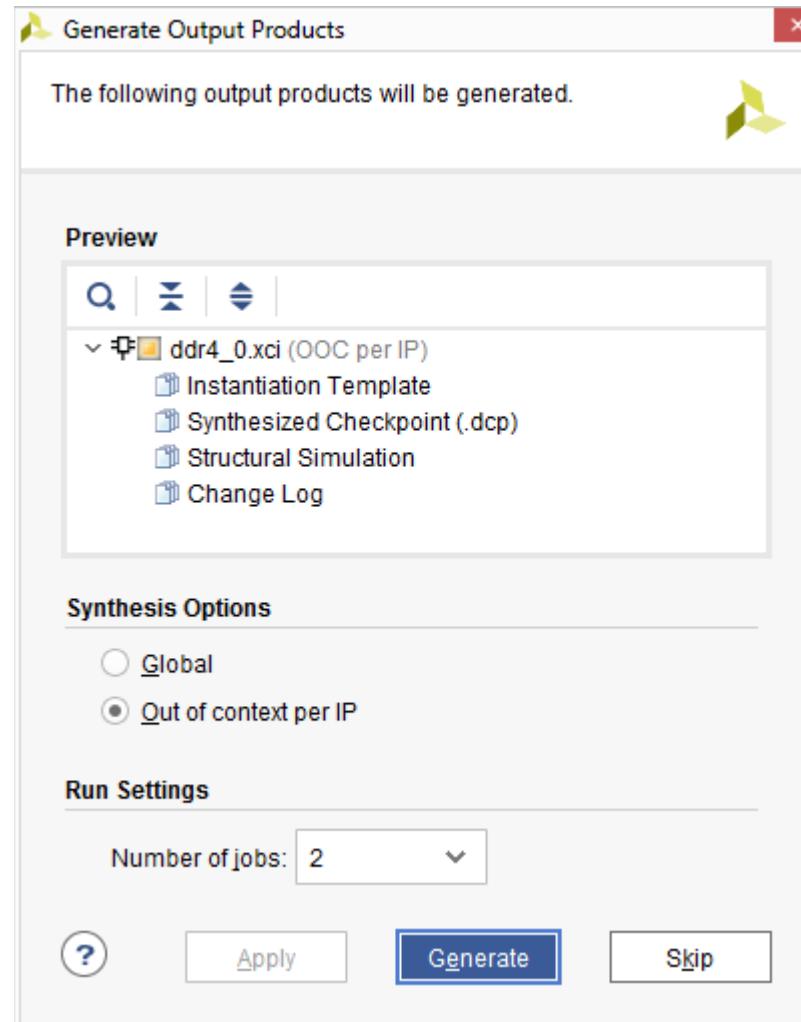
# Generate MIG DDR4 C2 Example Design

- Set the Example Design Test Bench to **ADVANCED TG**
- Click **OK**



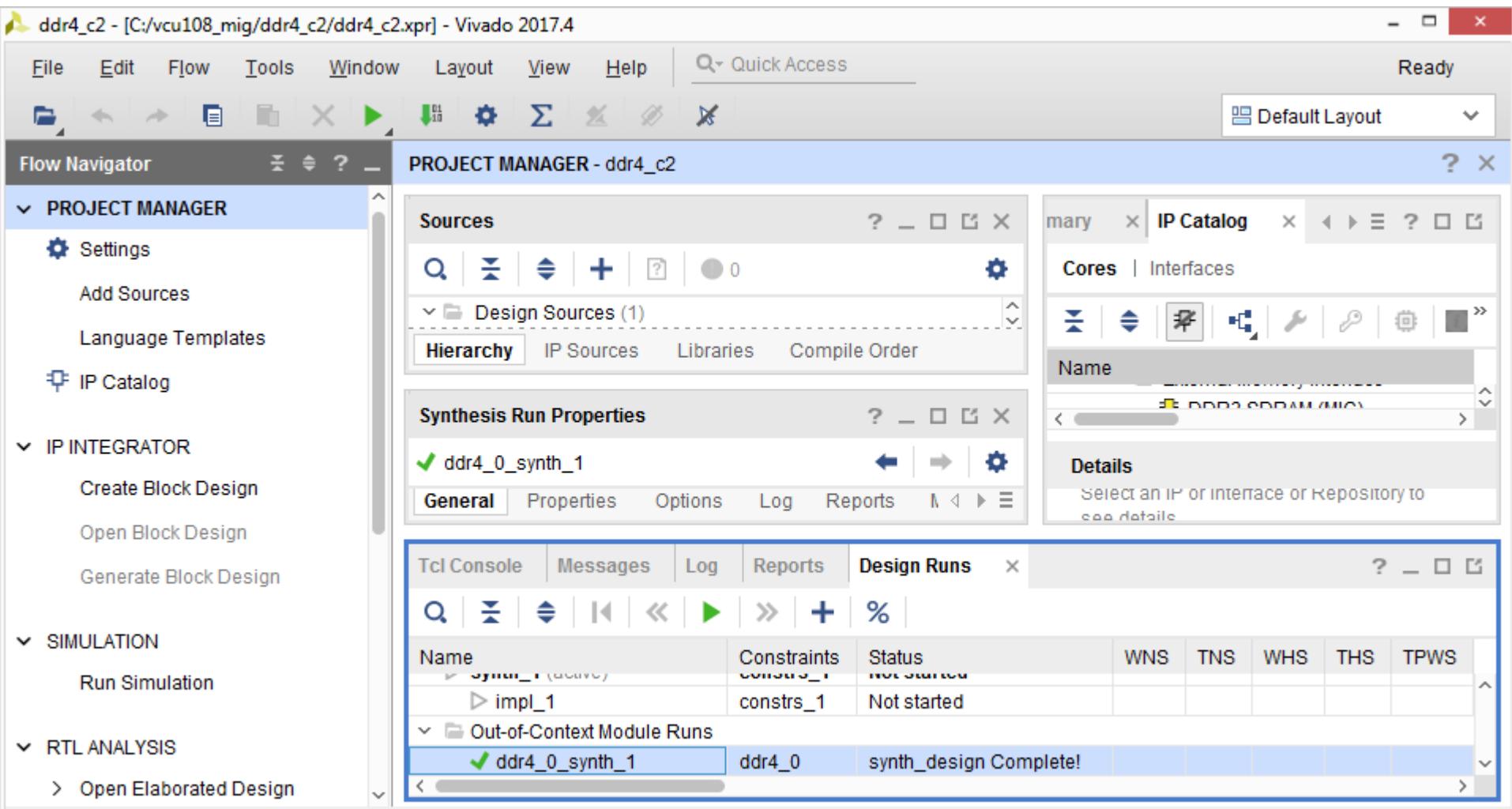
# Generate MIG DDR4 C2 Example Design

► Click Generate



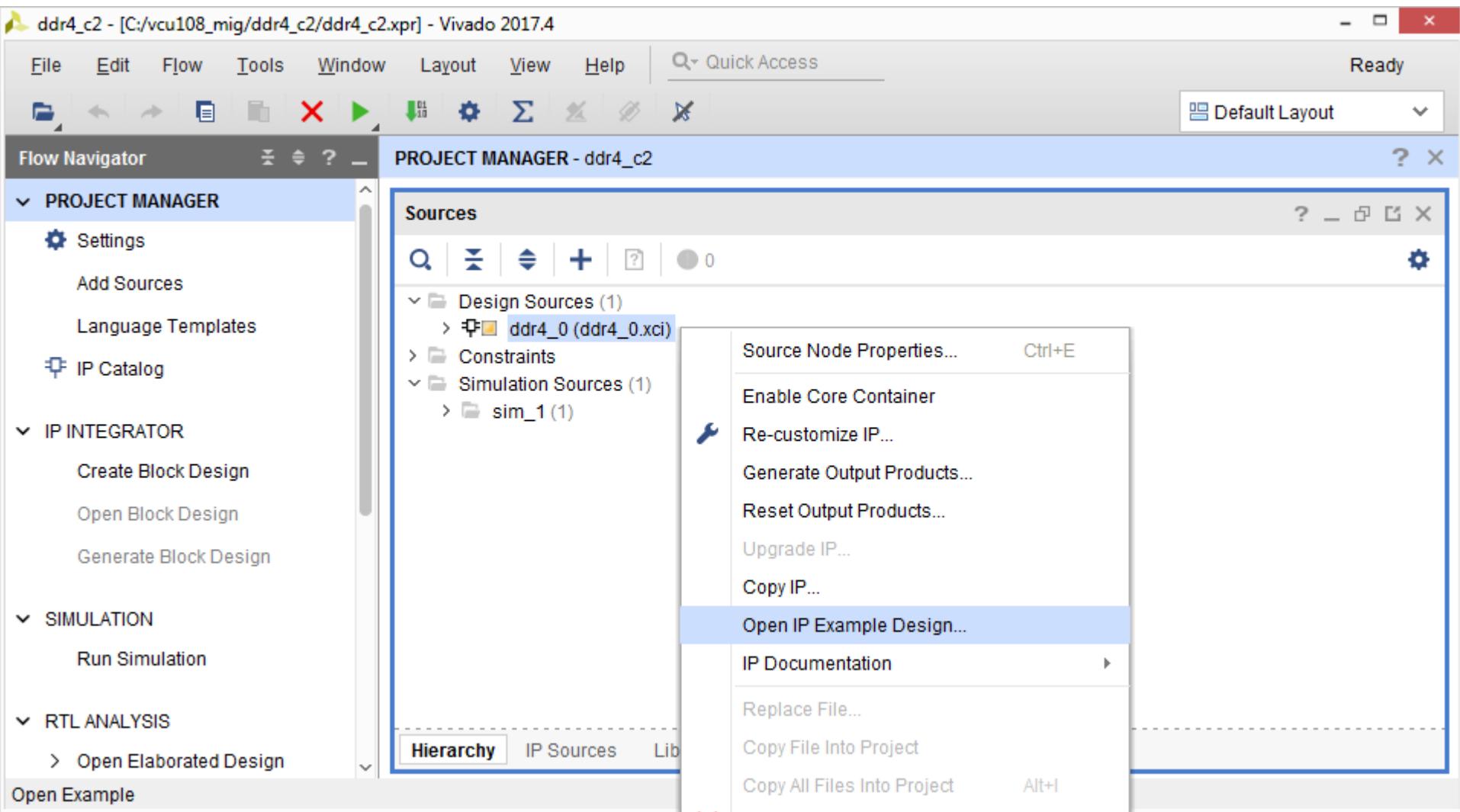
# Generate MIG DDR4 C2 Example Design

► Wait until checkmark appears on **ddr4\_0\_synth\_1**



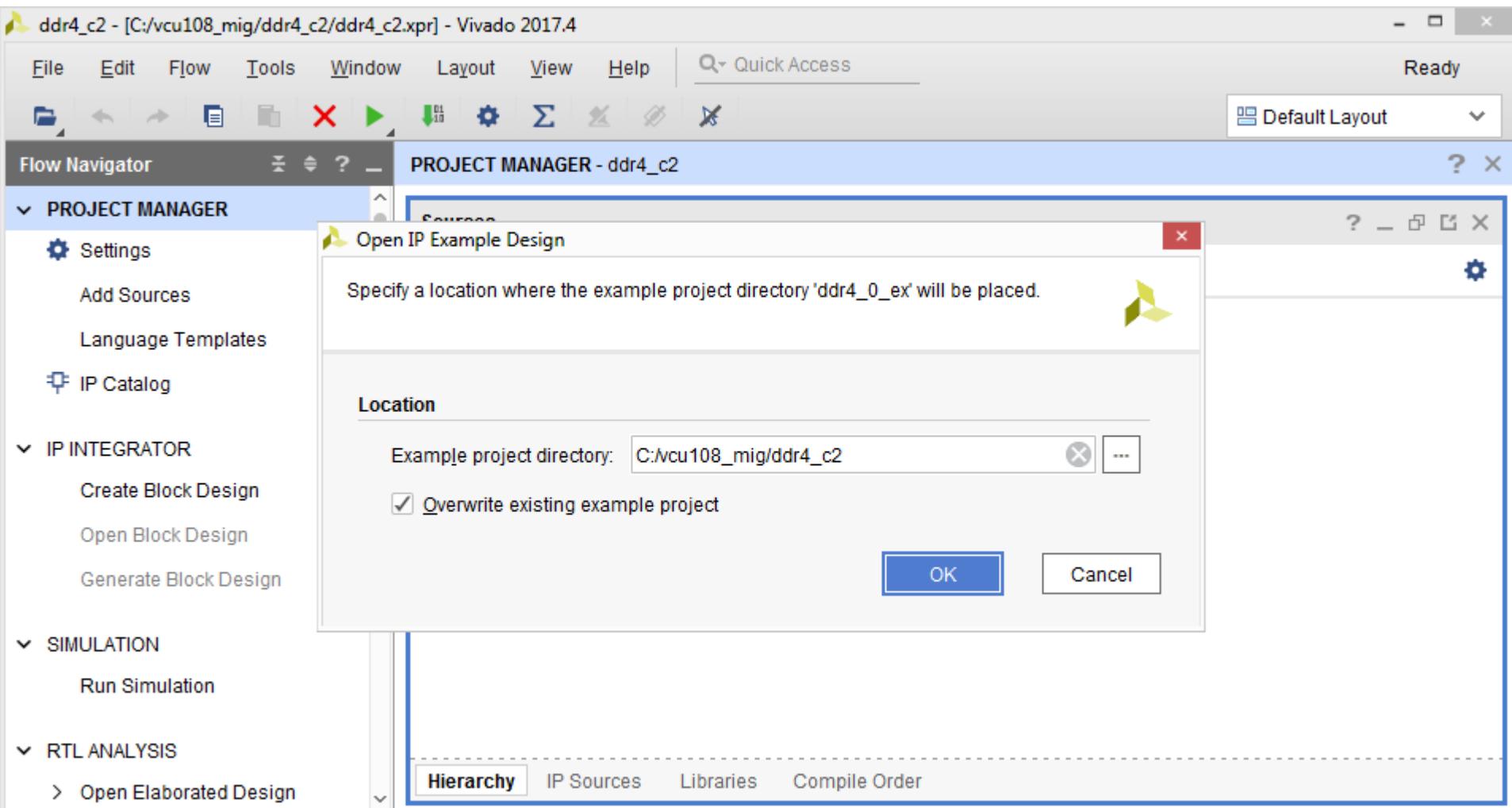
# Compile Example Design

► Right click on **ddr4\_0** and select **Open IP Example Design...**



# Compile Example Design

► Set the location to **C:/vcu108\_mig/ddr4\_c2** and click **OK**



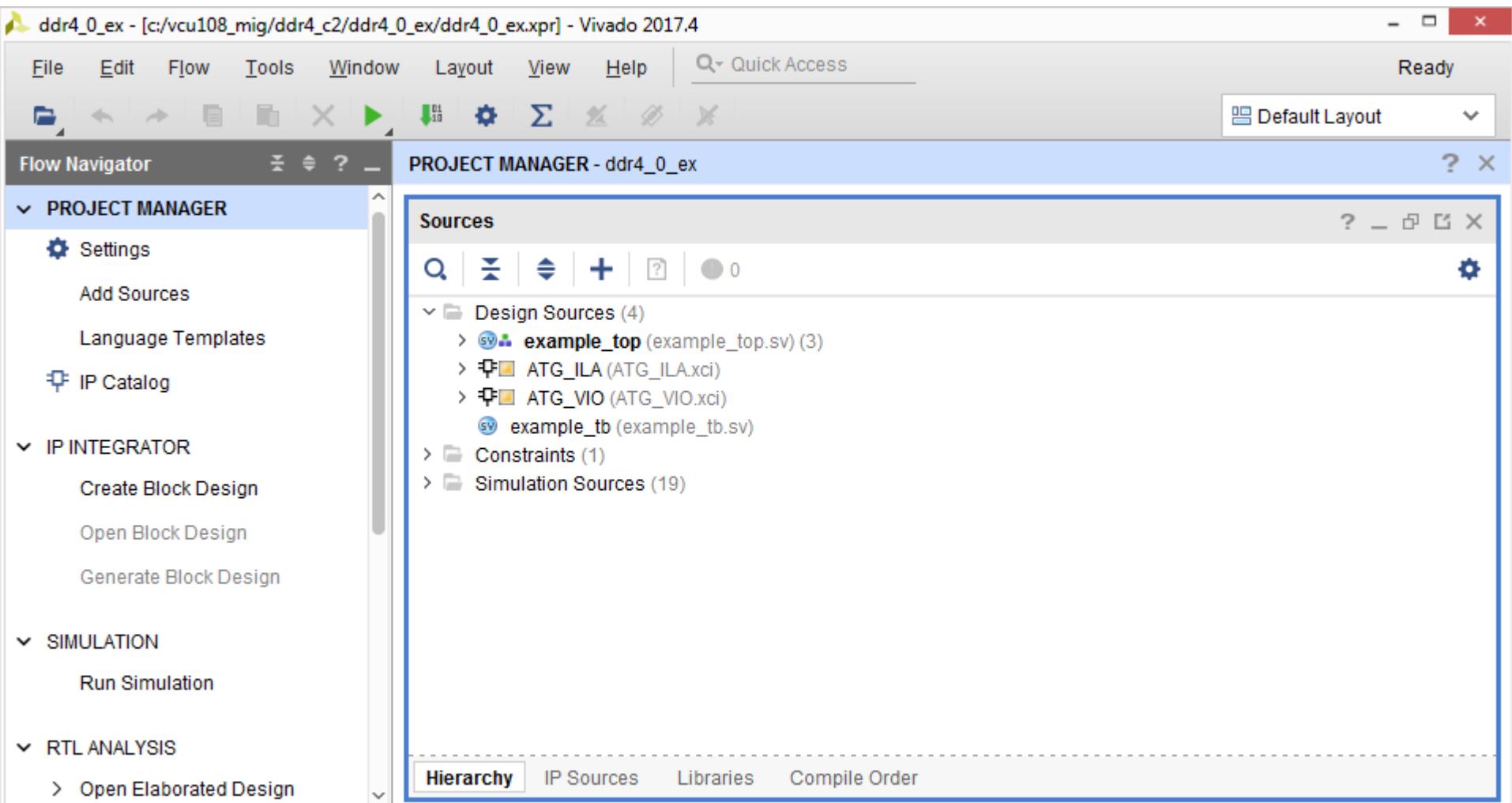
Open Example

Note: Presentation applies to the VCU108

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# Compile Example Design

► A new project is created under <design path>/



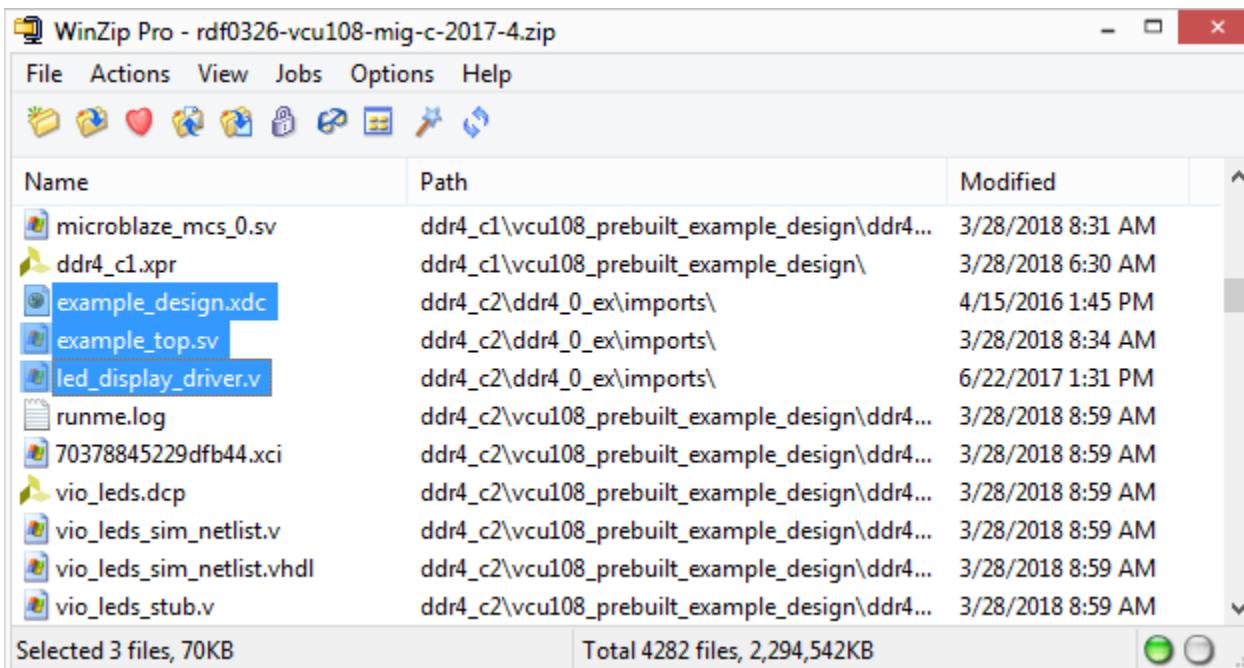
Note: The original project window can be closed

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# Modifications to Example Design

## ► From the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file

- Extract the **ddr4\_c2** files, **example\_design.xdc**, **example\_top.sv**, and **led\_display\_driver.v**
- Overwrite these three existing files in your **ddr4\_c2** MIG design
- Do this **after** creating the Example Design; changes only affect the Example Design



# Modifications to Example Design

## ► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs
- The following commands will add the led\_display\_driver.v and create the required VIO IP
- From the Tcl Console, run these commands:

```
add_files -norecurse
```

```
C:/vcu108_mig/ddr4_c2/ddr4_0_ex/imports/led_display_driver.v
```

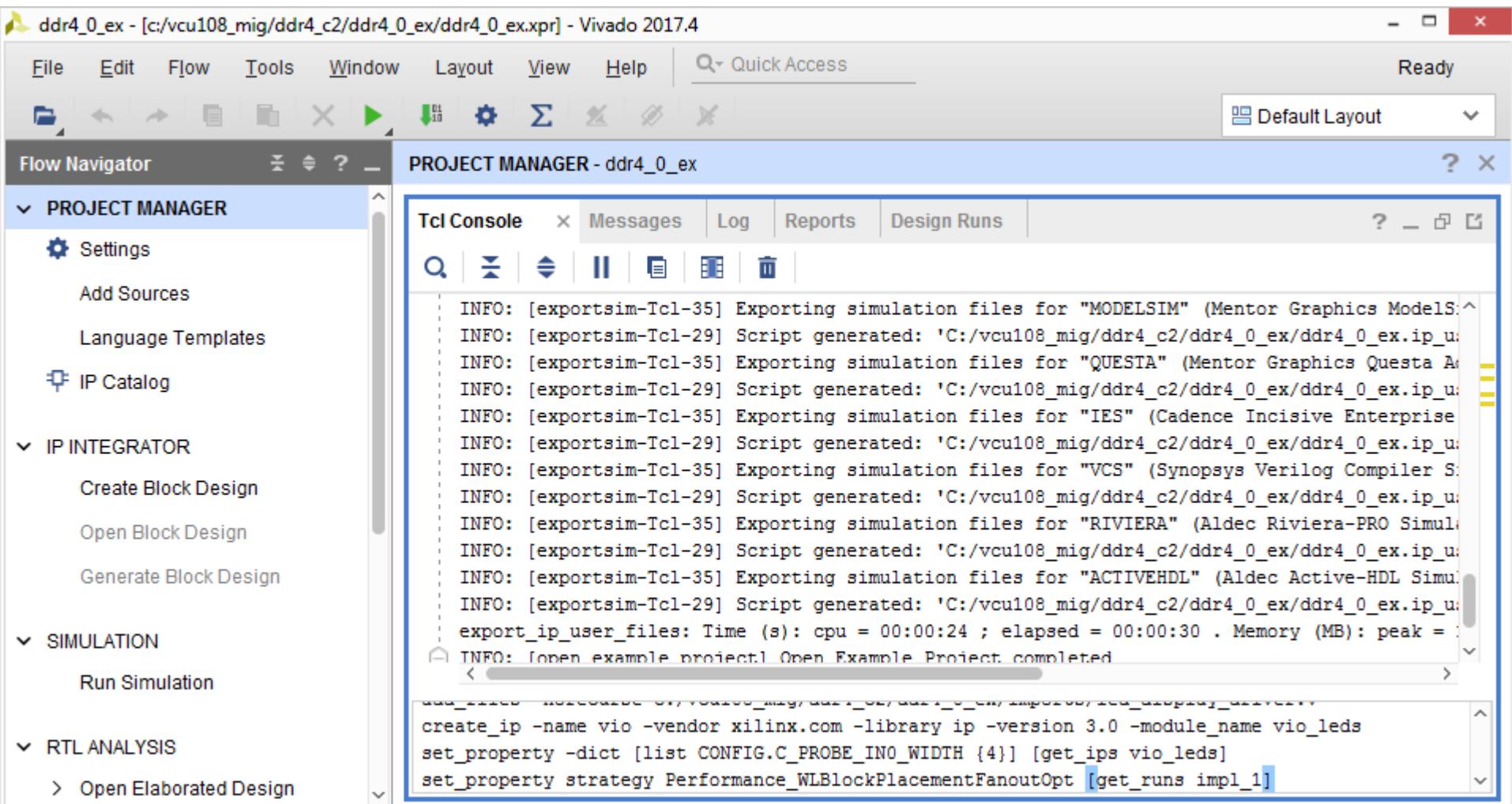
```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

```
set_property strategy Performance_WLBlockPlacementFanoutOpt [get_runs  
impl_1]
```

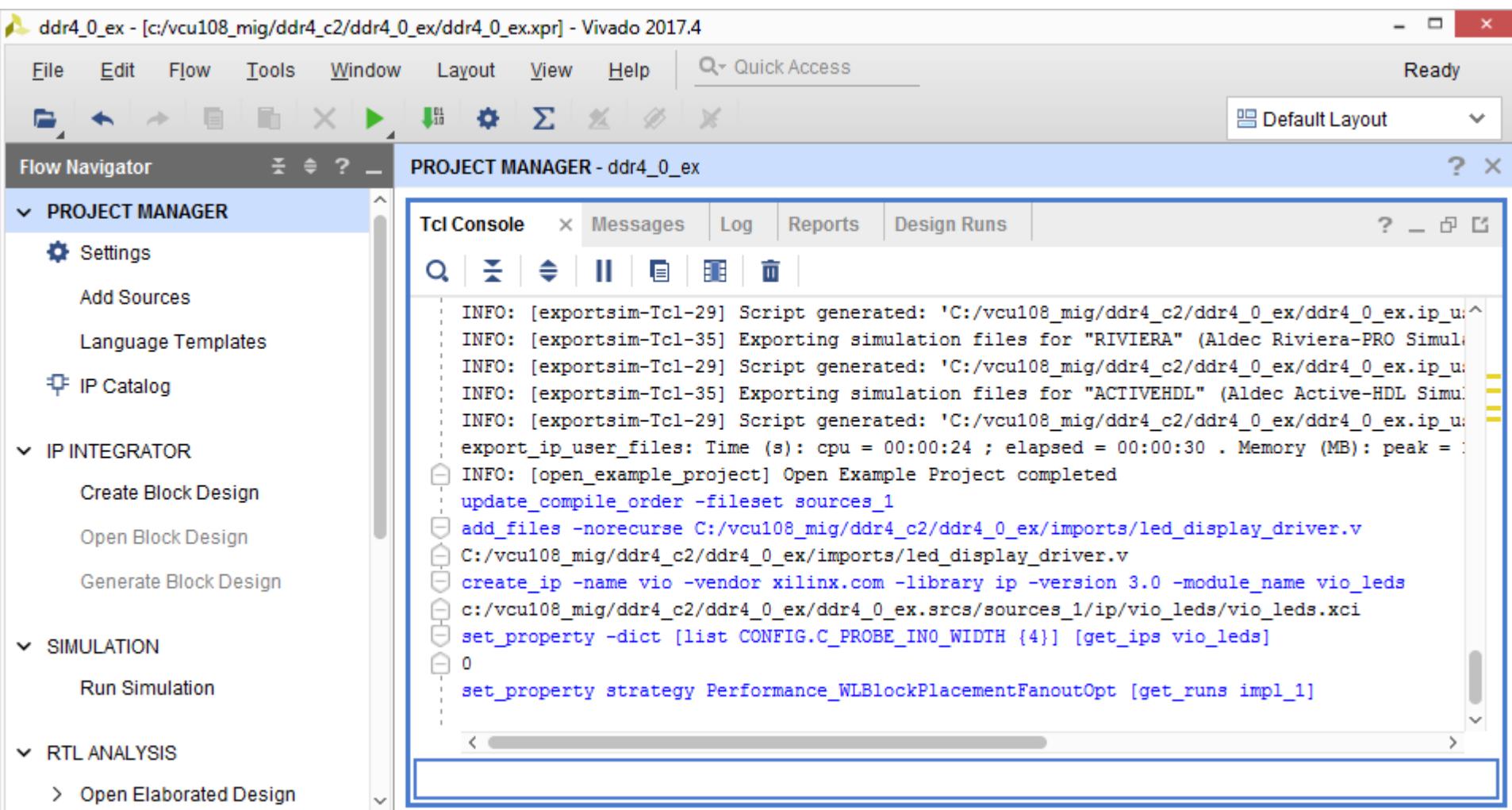
# Modifications to Example Design

► Press enter after entering Tcl commands



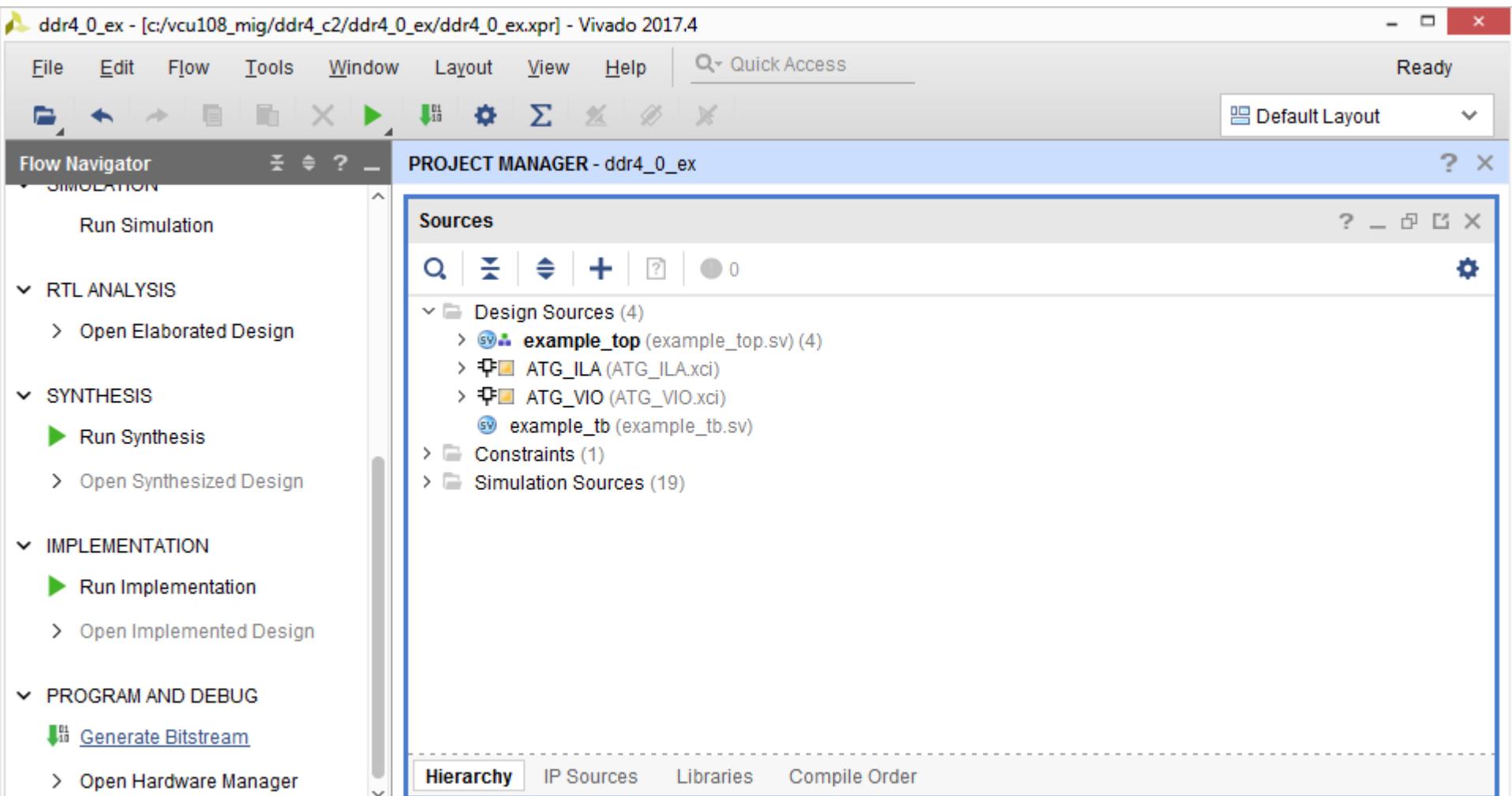
# Modifications to Example Design

► Tcl commands completed successfully



# Compile Example Design

► Click on **Generate Bitstream**



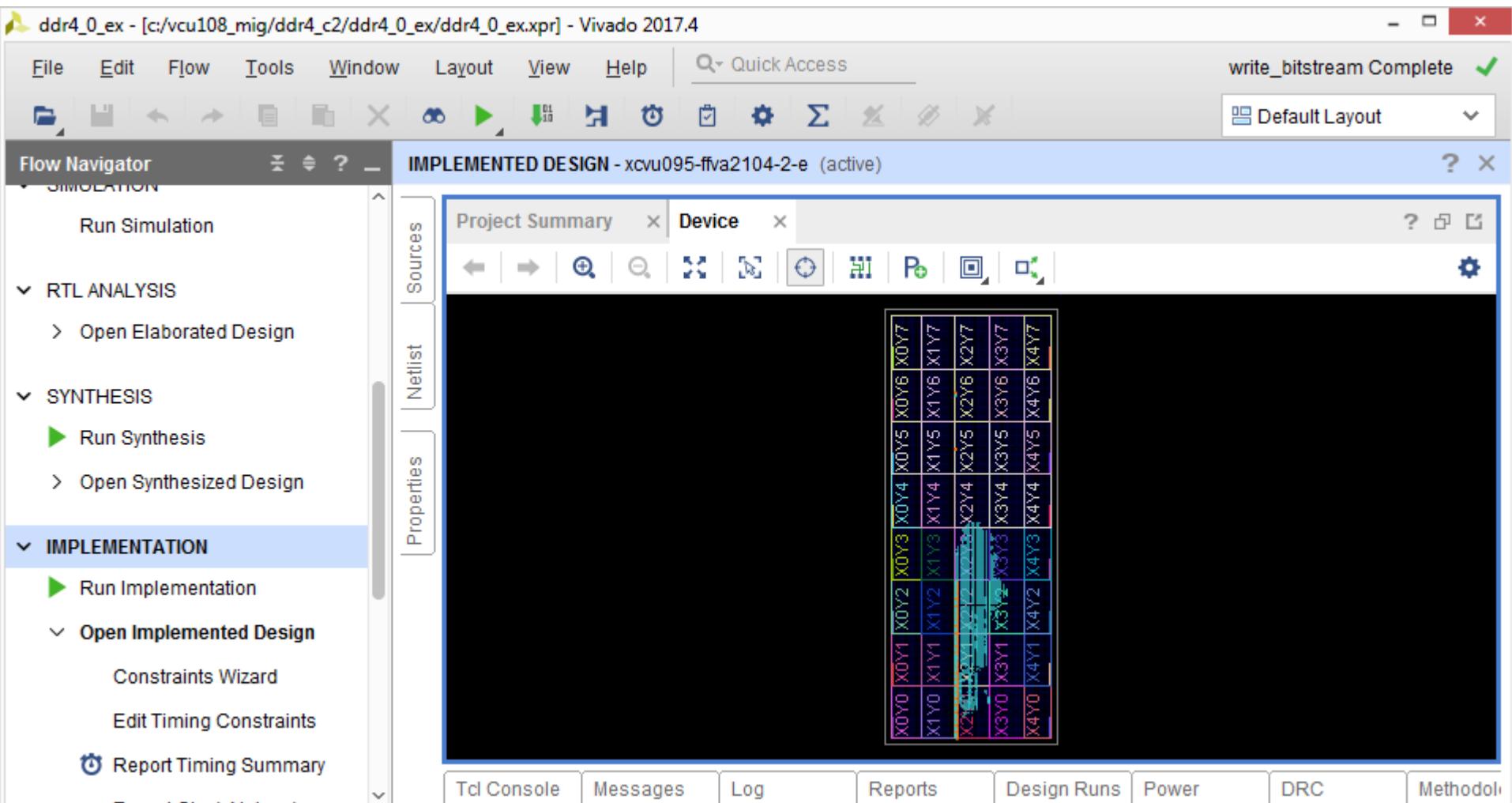
Generate a programming file after implementation

Note: Presentation applies to the VCU108

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# Compile Example Design

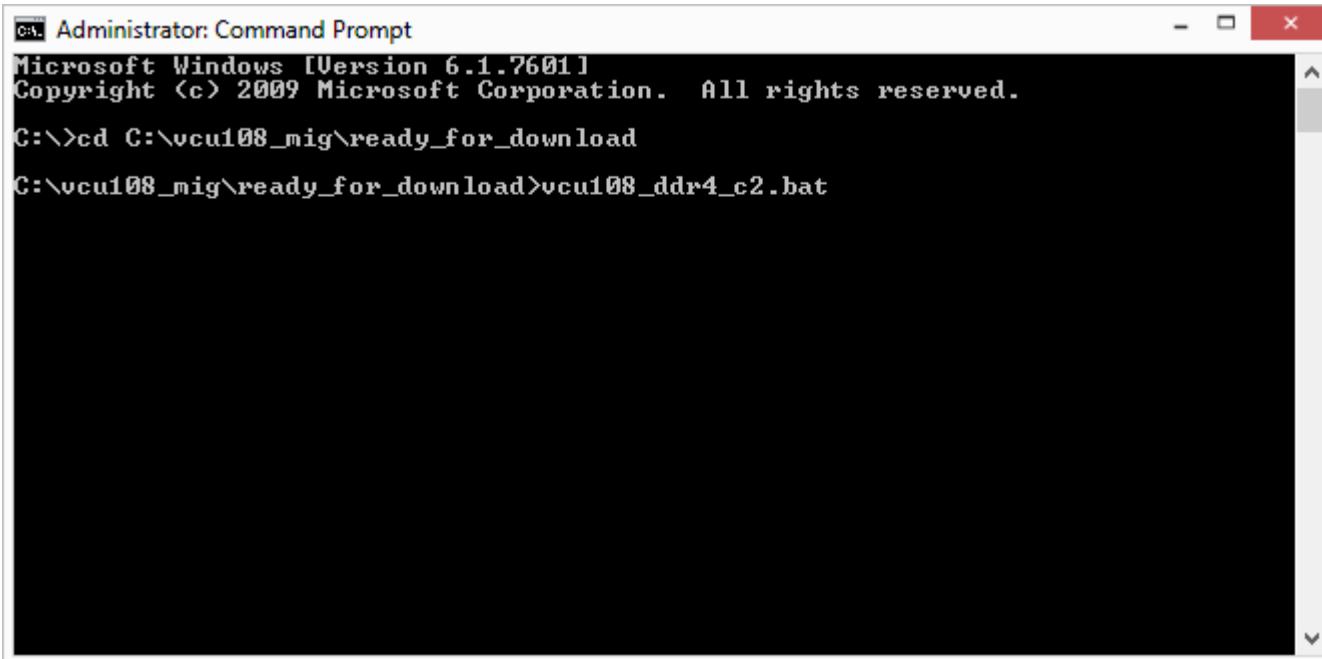
► Open and view the Implemented Design



# Run MIG Example Design

- ▶ From a Command Prompt, type:

```
cd C:\vcu108_mig\ready_for_download  
vcu108_ddr4_c2.bat
```

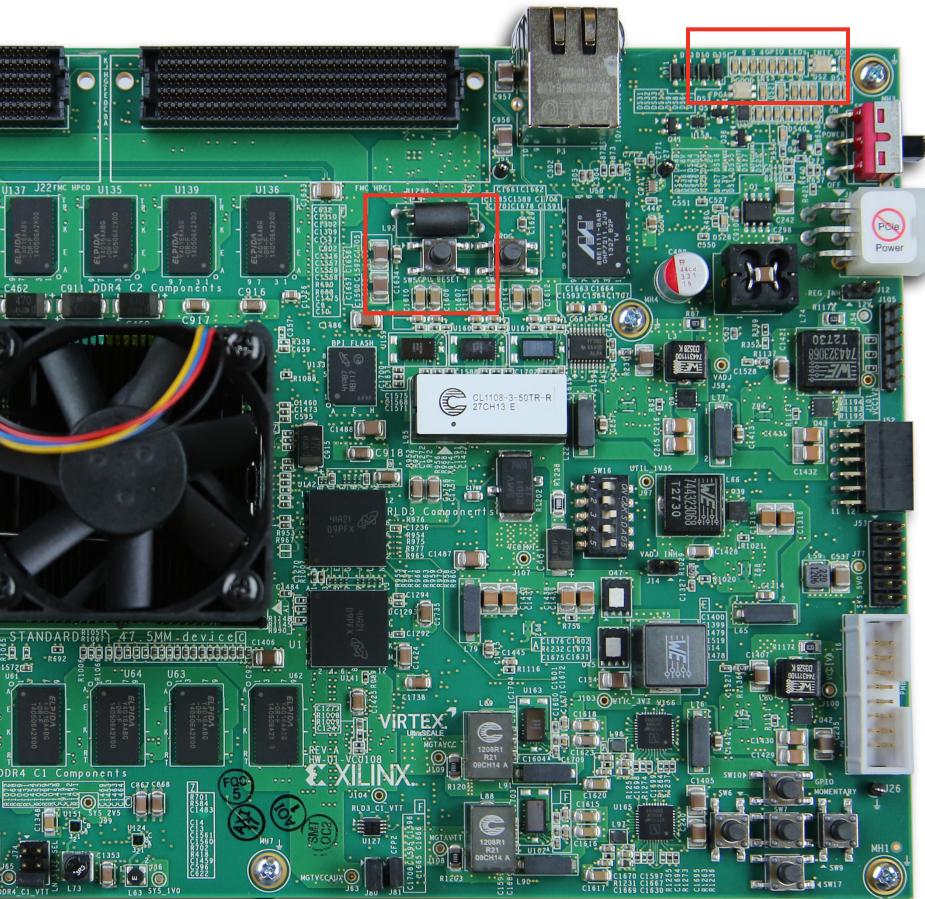


The screenshot shows a Windows Command Prompt window with the title "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu108_mig\ready_for_download
C:\vcu108_mig\ready_for_download>vcu108_ddr4_c2.bat
```

# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset

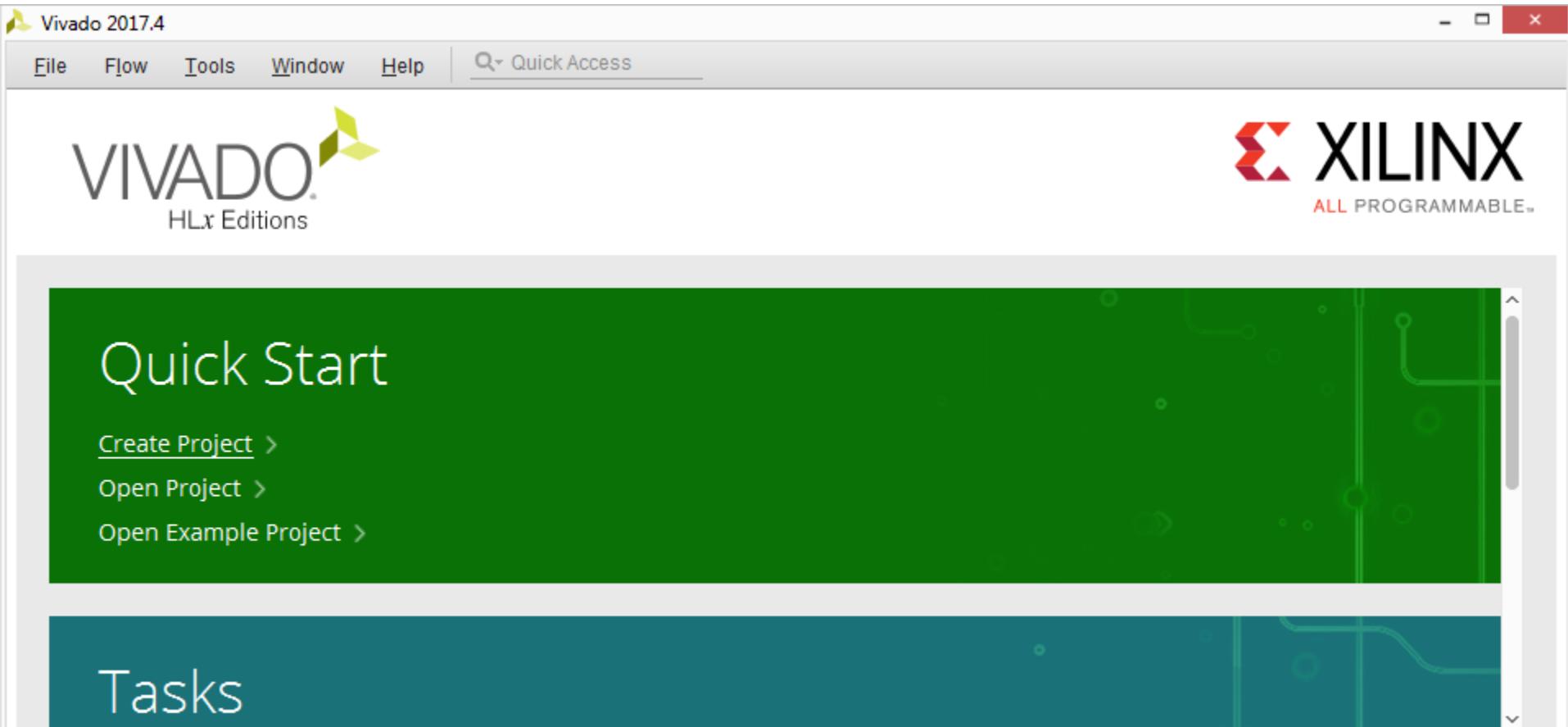
# Generate MIG RLD3 72 Bit Example Design

# Generate MIG RLD3 72 Bit Example Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.4 → Vivado

► Select Create Project



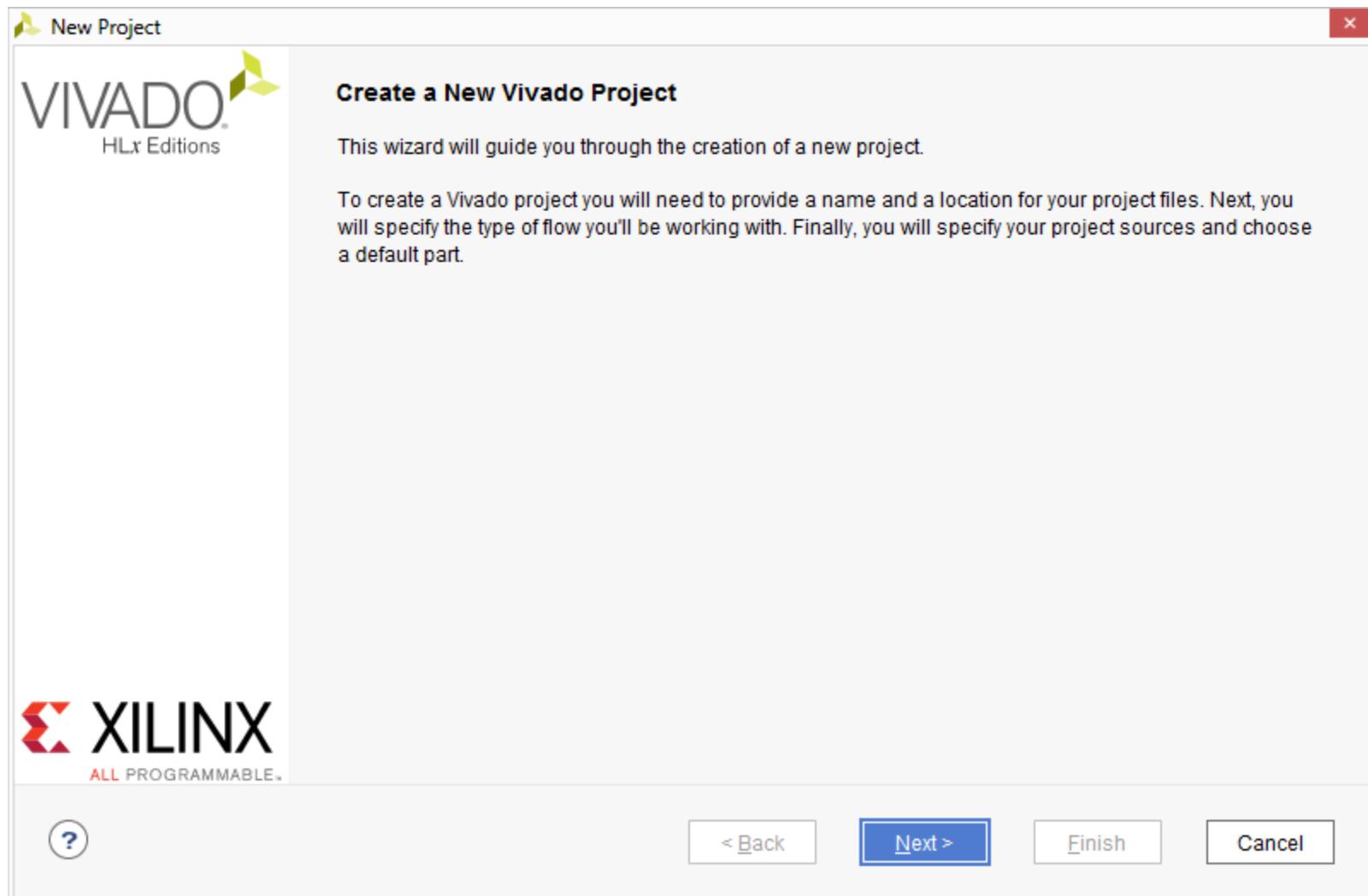
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU108

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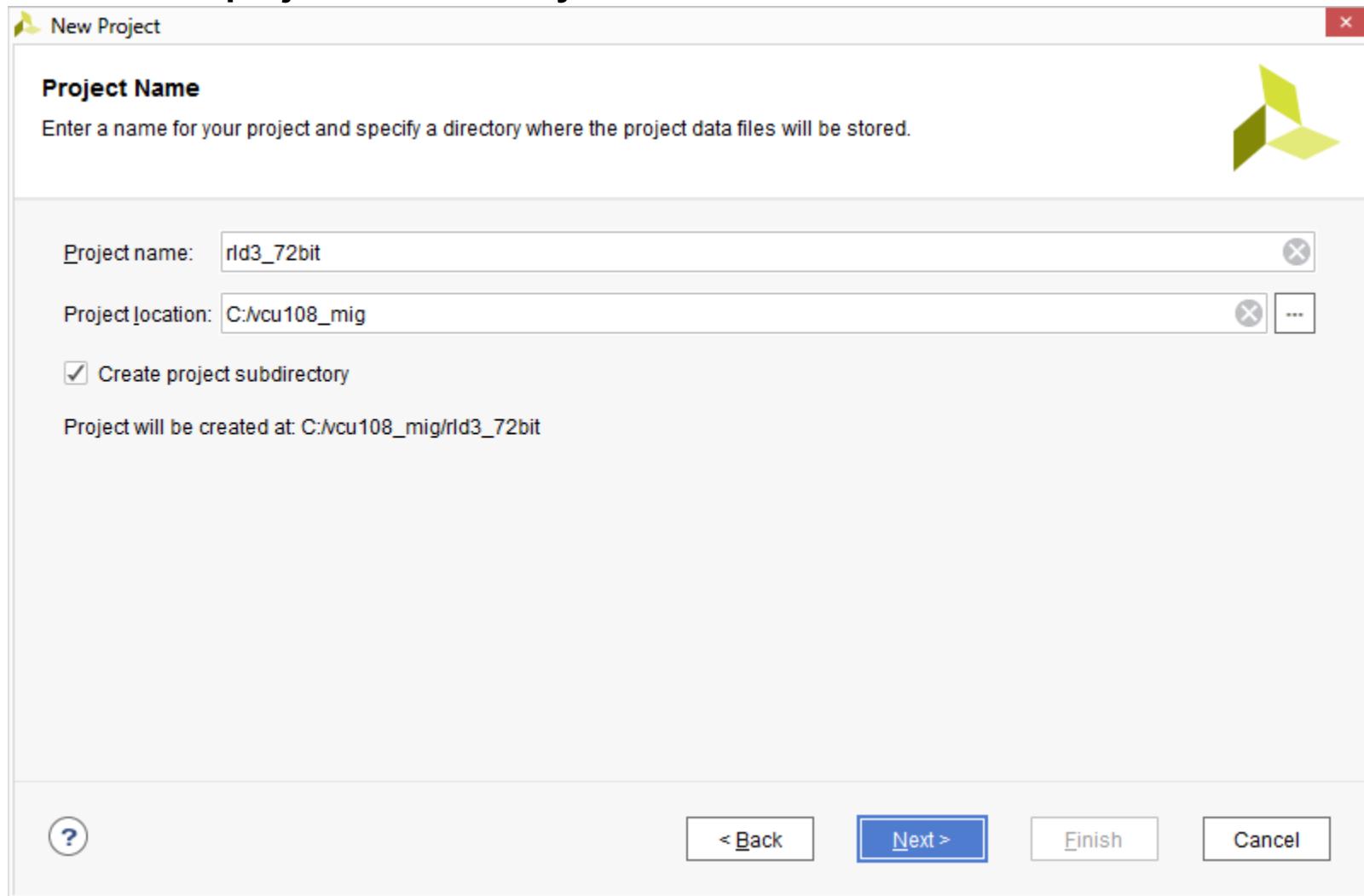
# Generate MIG RLD3 72 Bit Example Design

► Click Next



# Generate MIG RLD3 72 Bit Example Design

- Set the Project name to **rld3\_72bit** and location to **C:/vcu108\_mig**
  - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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# Generate MIG RLD3 72 Bit Example Design

## ► Select RTL Project

- Select **Do not specify sources at this time**

New Project

**Project Type**  
Specify the type of project to create.



RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Generate MIG RLD3 72 Bit Example Design

► Under Boards, select the VCU108 Evaluation Platform

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

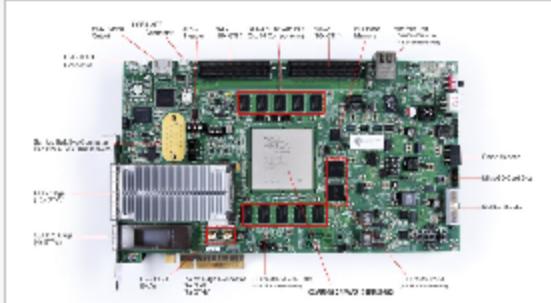
Select: Parts Boards

Filter/ Preview

Vendor: All  
Display Name: All  
Board Rev: Latest

Reset All Filters

Search:



Display Name	Vendor	Board Rev	Part
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2
<b>Virtex-UltraScale VCU108 Evaluation Platform</b>	xilinx.com	1.0	<b>xcvu095-ffa2104-2-e</b>
Virtex-UltraScale VCU110 Evaluation Platform	xilinx.com	1.0	xcvu190-flfc2104-2-e

No Board Connectors

?

< Back

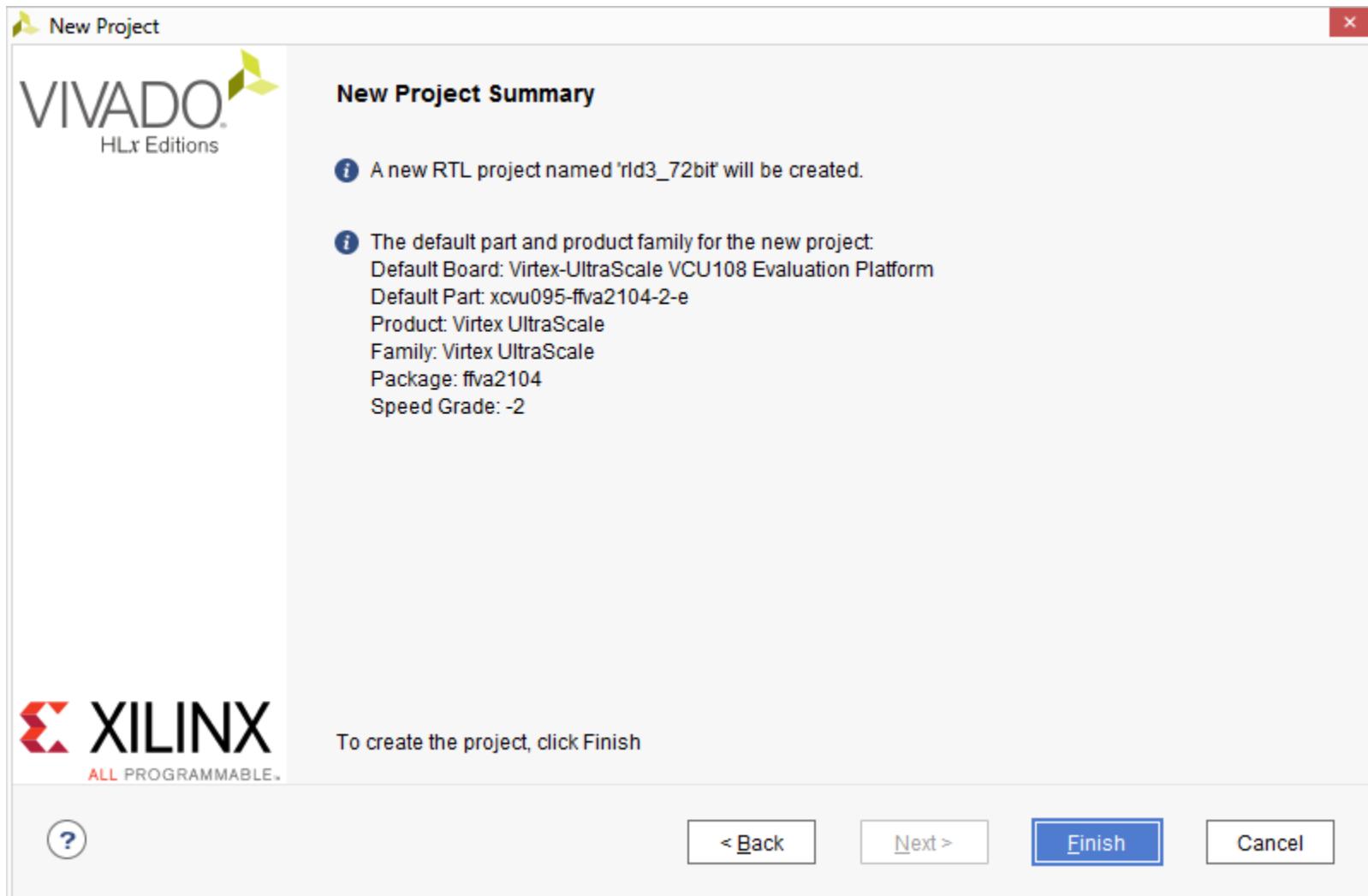
Next >

Finish

Cancel

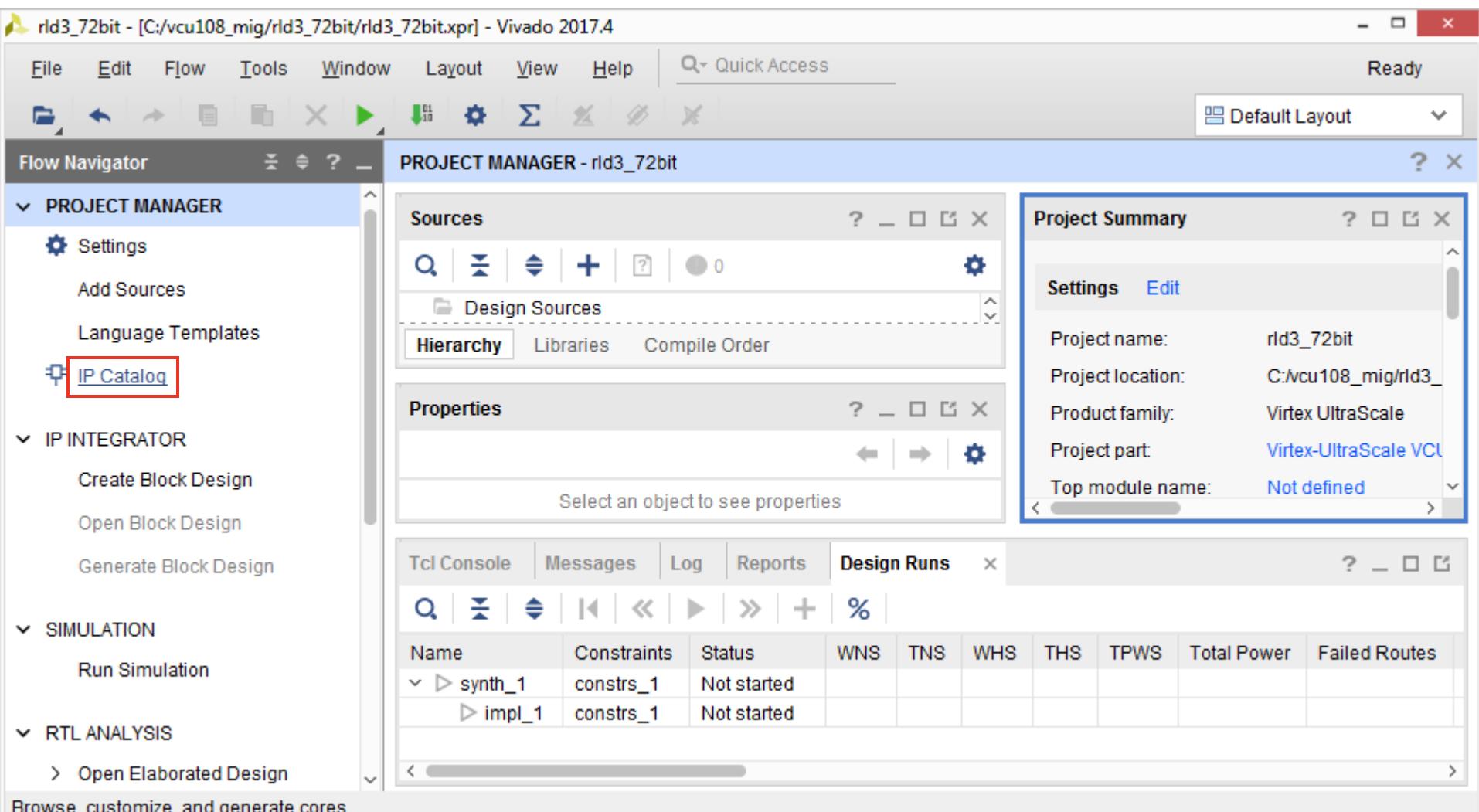
# Generate MIG RLD3 72 Bit Example Design

► Click Finish



# Generate MIG RLD3 72 Bit Example Design

► Click on IP Catalog



# Generate MIG RLD3 72 Bit Example Design

## ► Select **RLDRAM3 (MIG)**, v1.4

The screenshot shows the Vivado 2017.4 interface with the project "rld3\_72bit" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, RTL Analysis, and Flow Navigator. The main area is the Project Manager, which has tabs for Project Summary and IP Catalog. The IP Catalog tab is active, displaying the IP Catalog for the project. The catalog lists various cores and interfaces, with the "RLDRAM3 (MIG)" entry highlighted. The details panel at the bottom shows the version is 1.4 (Rev. 3). The bottom navigation bar includes Tcl Console, Messages, Log, Reports, and Design Runs.

Name	Status	License	VLI	
ECC	Production	Included	xilinx	
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)		Pre-Production	Included	xilinx
QDRII+ SRAM (MIG)		Production	Included	xilinx
QDRIV SRAM (MIG)		Production	Included	xilinx
<b>RLDRAM3 (MIG)</b>	Production	Included	xilinx	

# Generate MIG RLD3 72 Bit Example Design

► Right click on **RLDRAM3 (MIG)**

- Select **Customize IP**

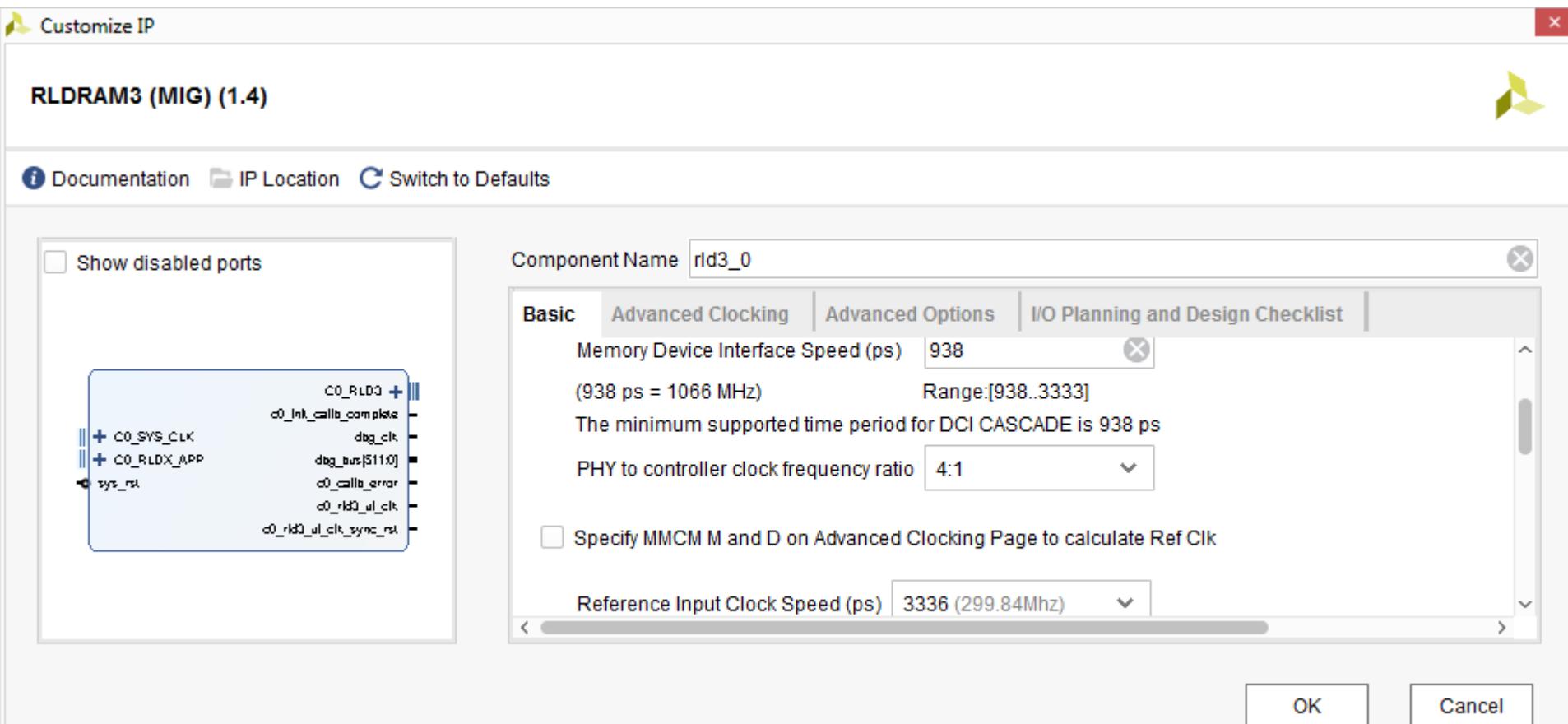
The screenshot shows the Vivado 2017.4 interface with the project "rld3\_72bit" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, RTL Analysis, and Flow Navigator. The main area is the Project Manager, which has tabs for Project Summary and IP Catalog. The IP Catalog tab is active, showing a list of cores under the "Cores" tab. The list includes AXI4, ECC, and several memory-related cores: DDR3 SDRAM (MIG), DDR4 SDRAM (MIG), LPDDR3 SDRAM (MIG), QDRII+ SRAM (MIG), QDRIV SRAM (MIG), and RLD3 (MIG). The RLD3 (MIG) item is highlighted with a blue selection bar. A context menu is open over the RLD3 (MIG) item, listing options: Properties..., IP Settings..., Add Repository..., Refresh All Repositories, Customize IP..., License Status, Compatible Families, and Compatible Simulators. The "Customize IP..." option is also highlighted with a blue selection bar.

Note: Presentation applies to the VCU108

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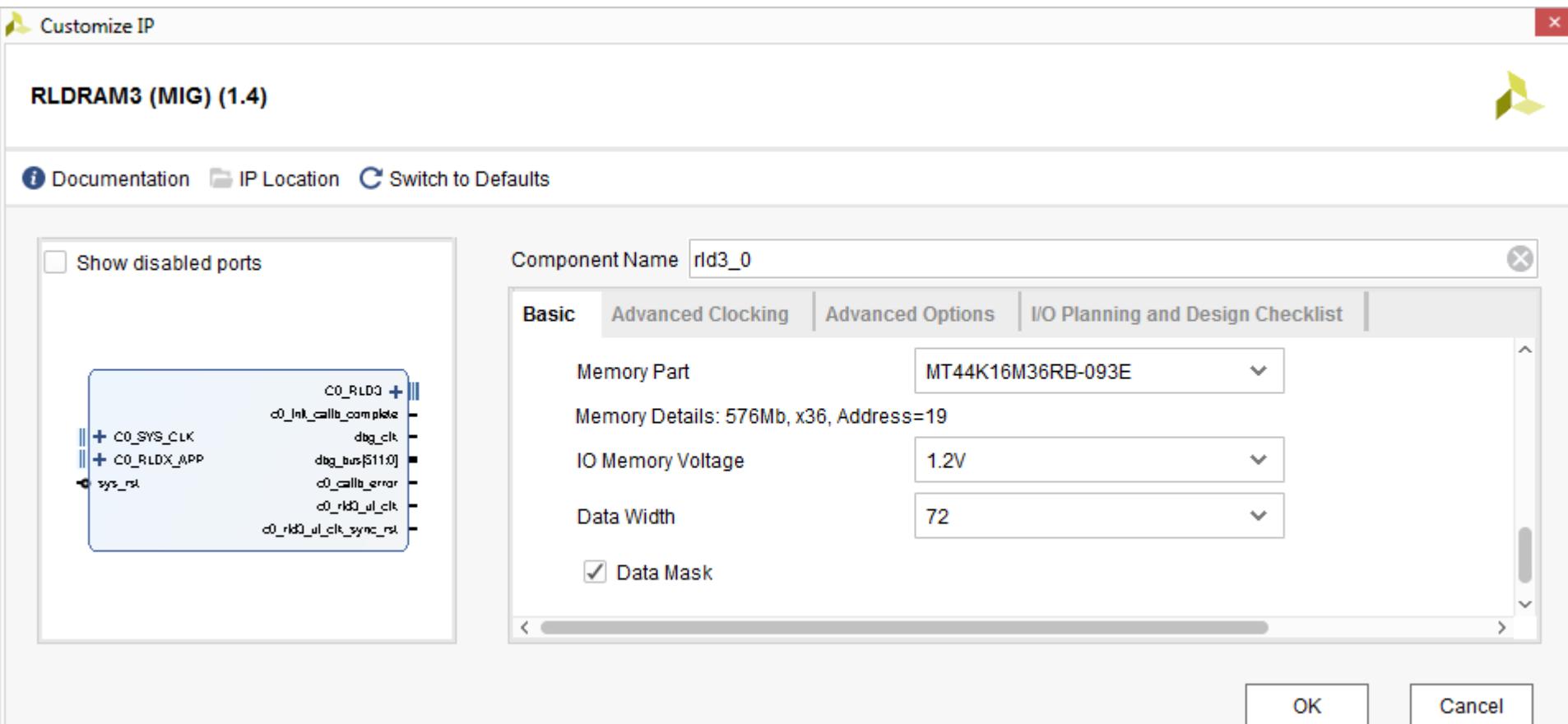
# Generate MIG RLD3 72 Bit Example Design

- Set Clock period to **938** for 2133 Mb/s operation.
- Set the Input Clock to **3336** ps for 300 MHz
- Scroll down



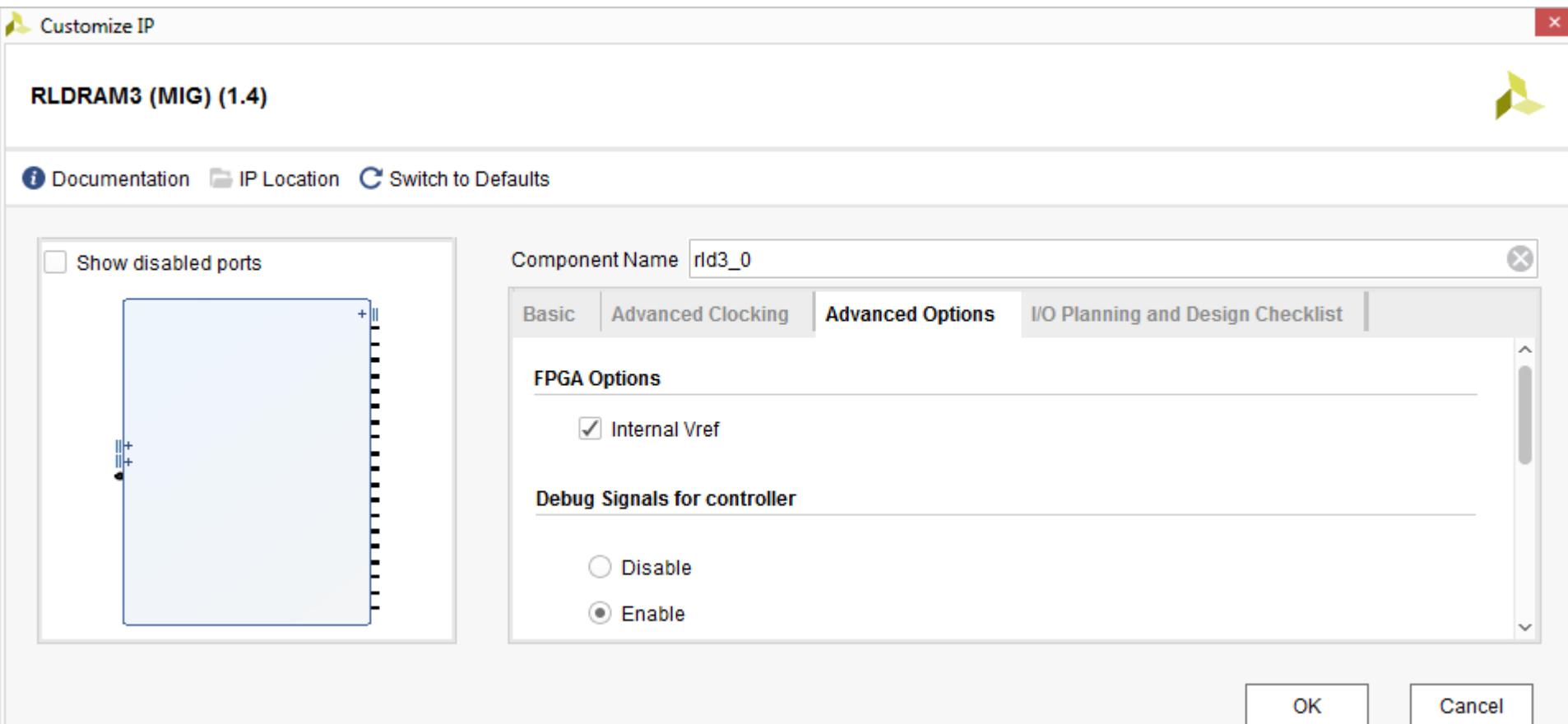
# Generate MIG RLD3 72 Bit Example Design

- Select the part **MT44K16M36RB-093E**
- Set the Data Width to **72** and click the **Advanced Options** Tab



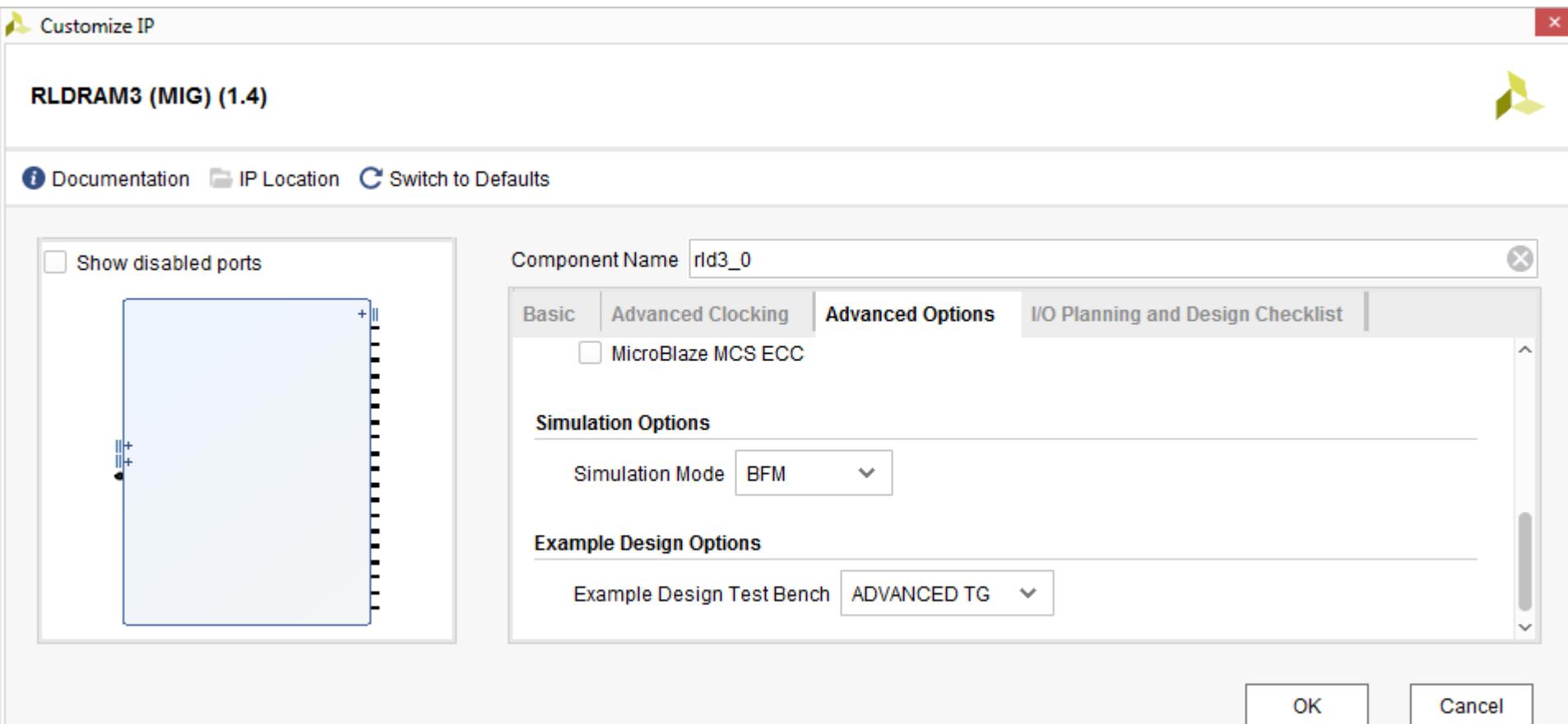
# Generate MIG RLD3 72 Bit Example Design

- Set the Debug Signals to **Enable**
- Scroll down



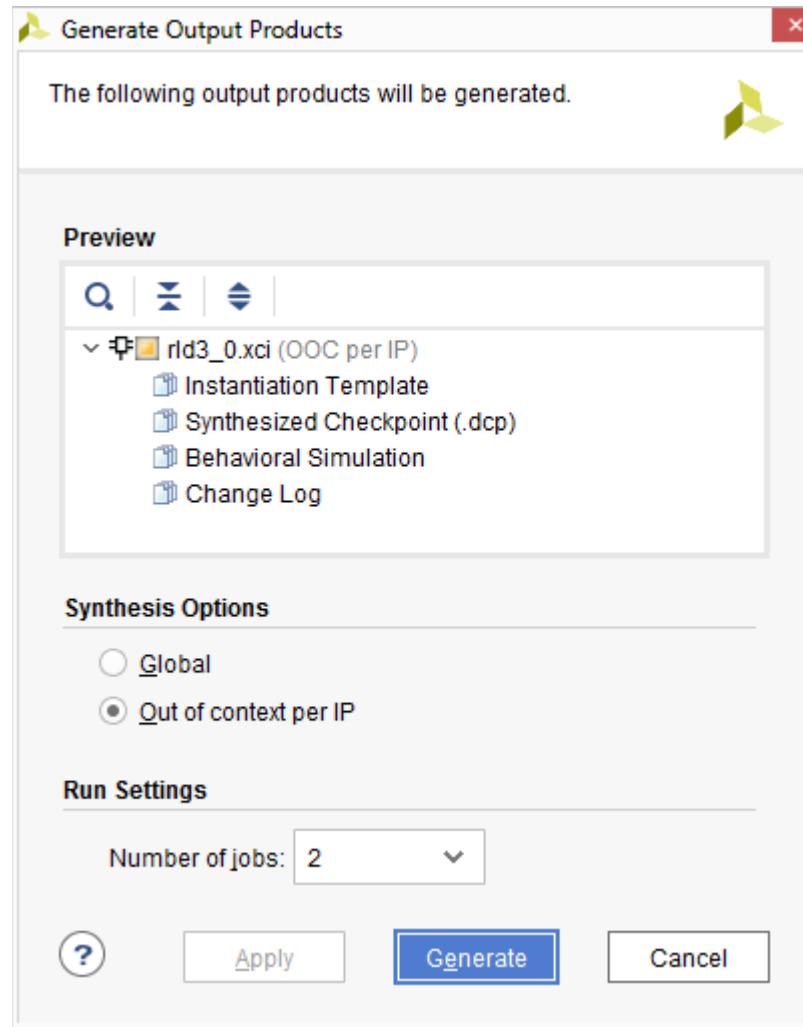
# Generate MIG RLD3 72 Bit Example Design

- Select ADVANCED TG
- Click OK



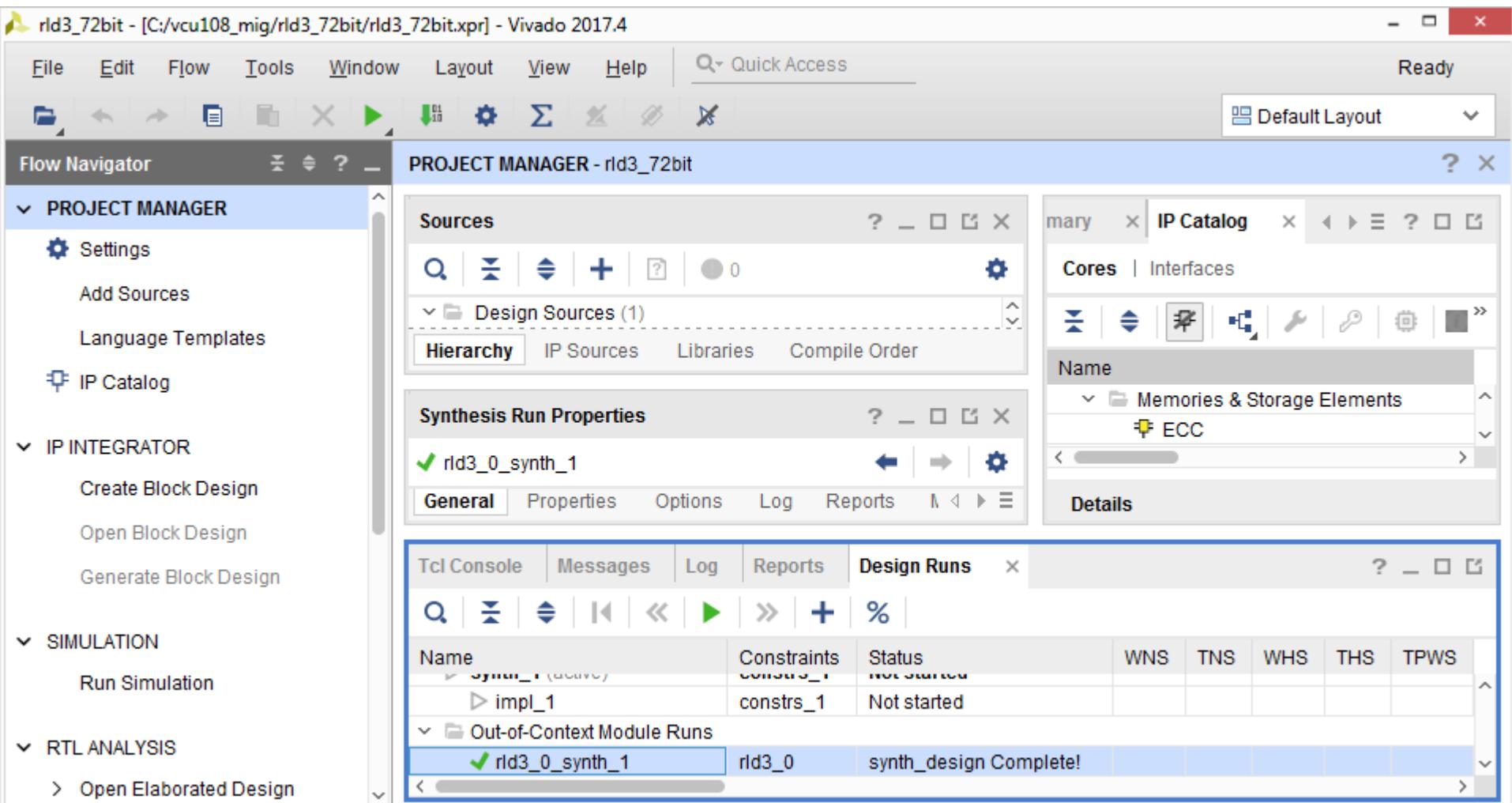
# Generate MIG RLD3 72 Bit Example Design

► Click Generate



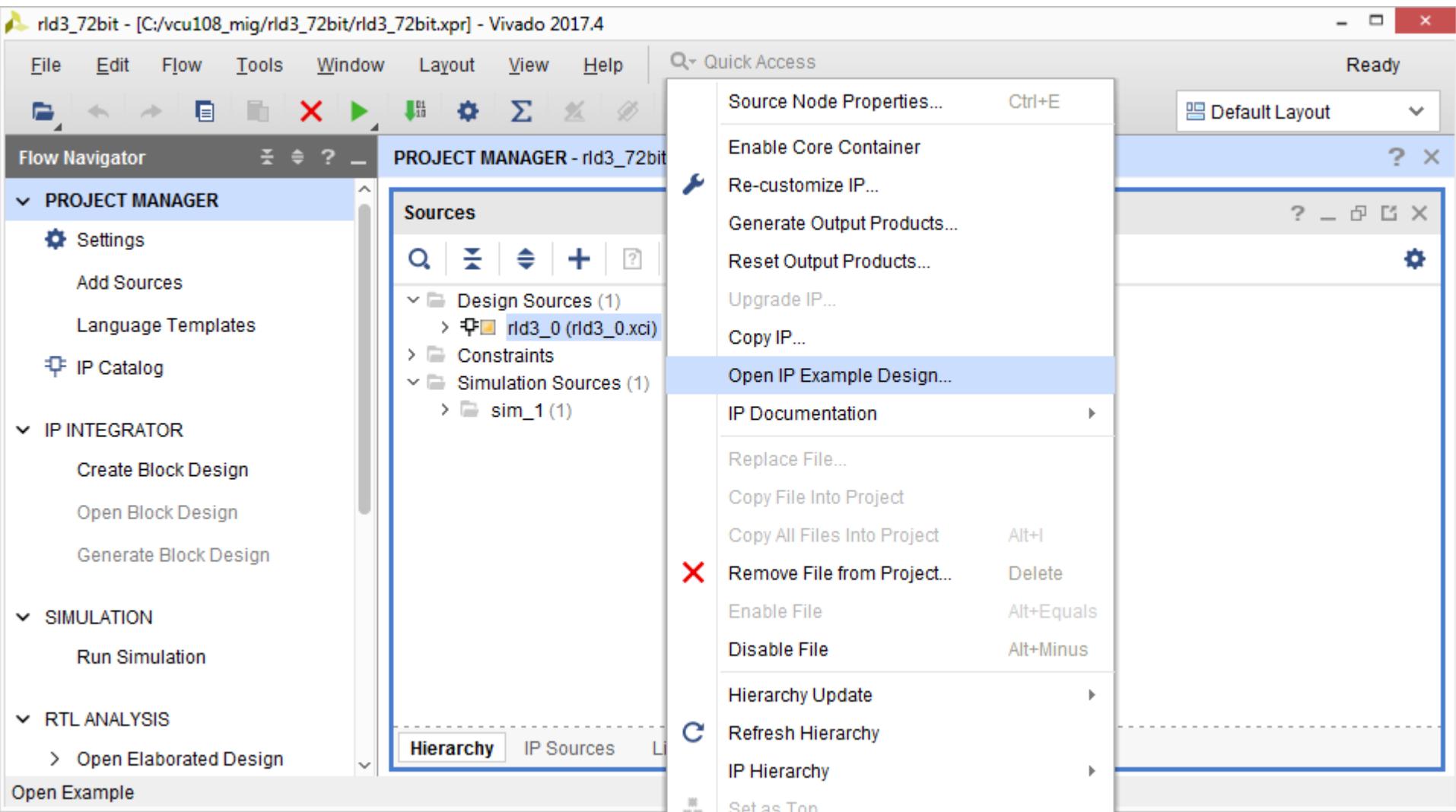
# Generate MIG RLD3 72 Bit Example Design

► Wait until checkmark appears on **rld3\_0\_synth\_1**



# Compile Example Design

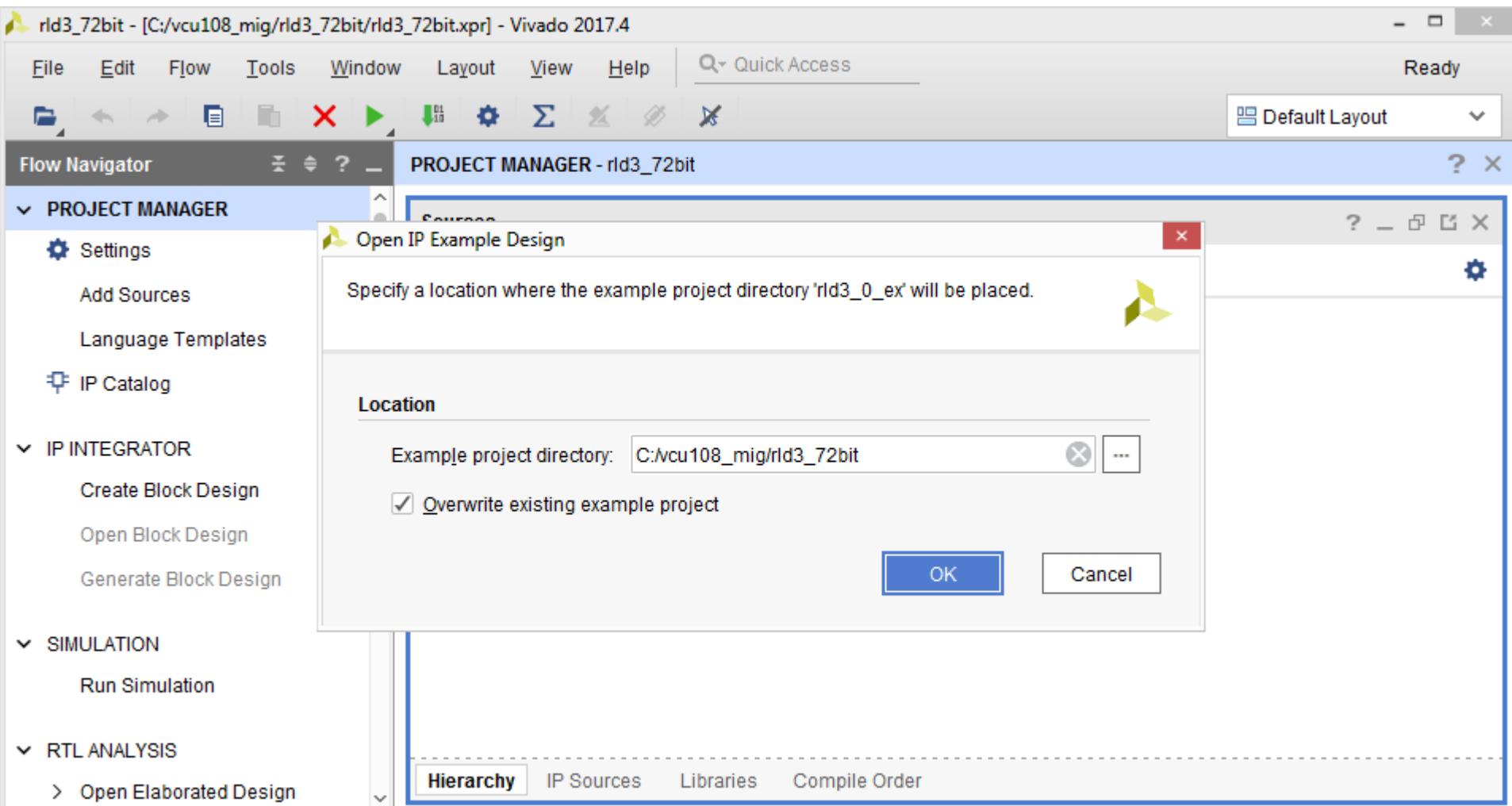
► Right click on **rld3\_0** and select **Open IP Example Design...**



Note: Presentation applies to the VCU108

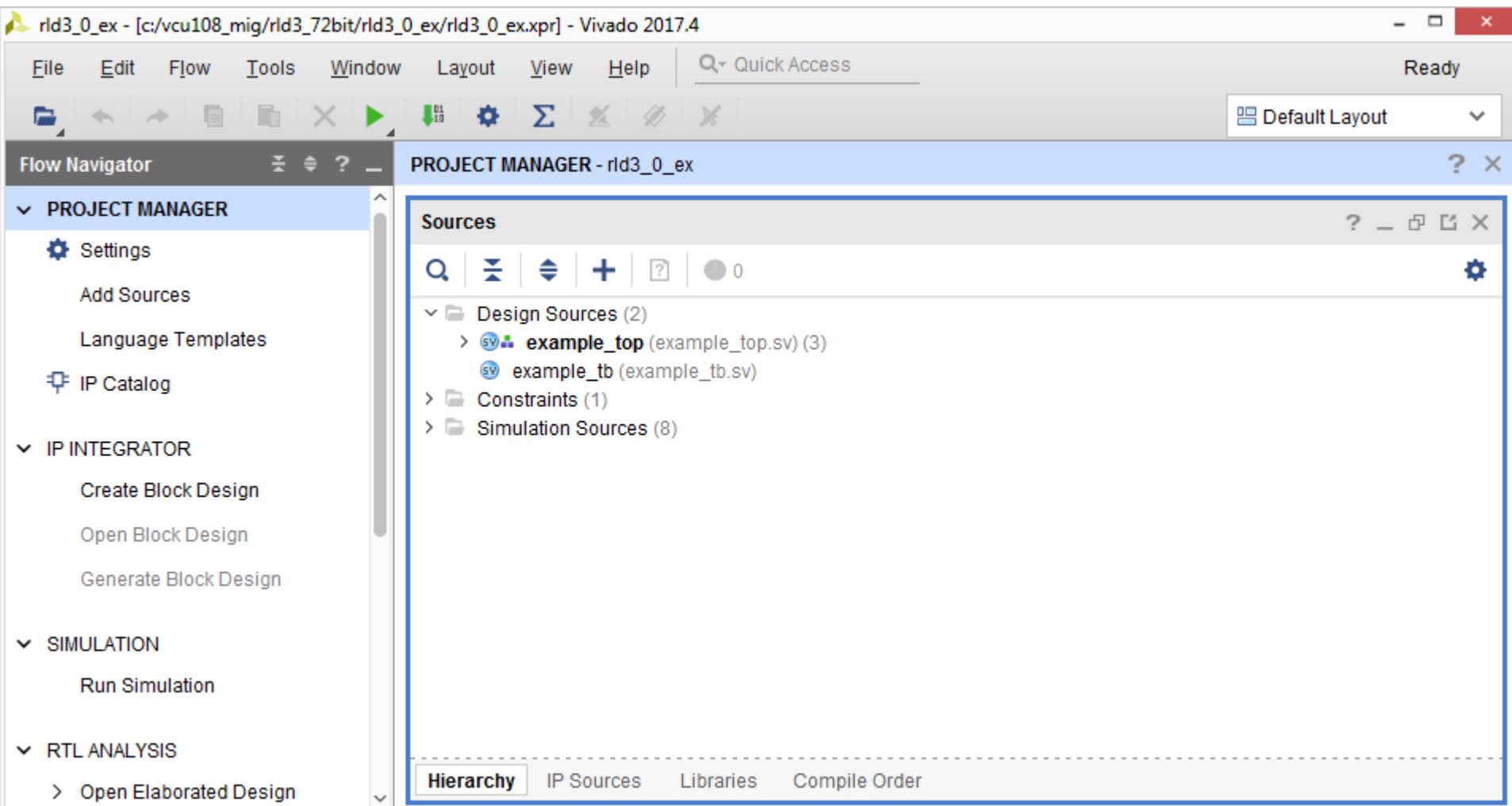
# Compile Example Design

► Set the location to **C:/vcu108\_mig/rld3\_72bit** and click **OK**



# Compile Example Design

► A new project is created under <design path>/



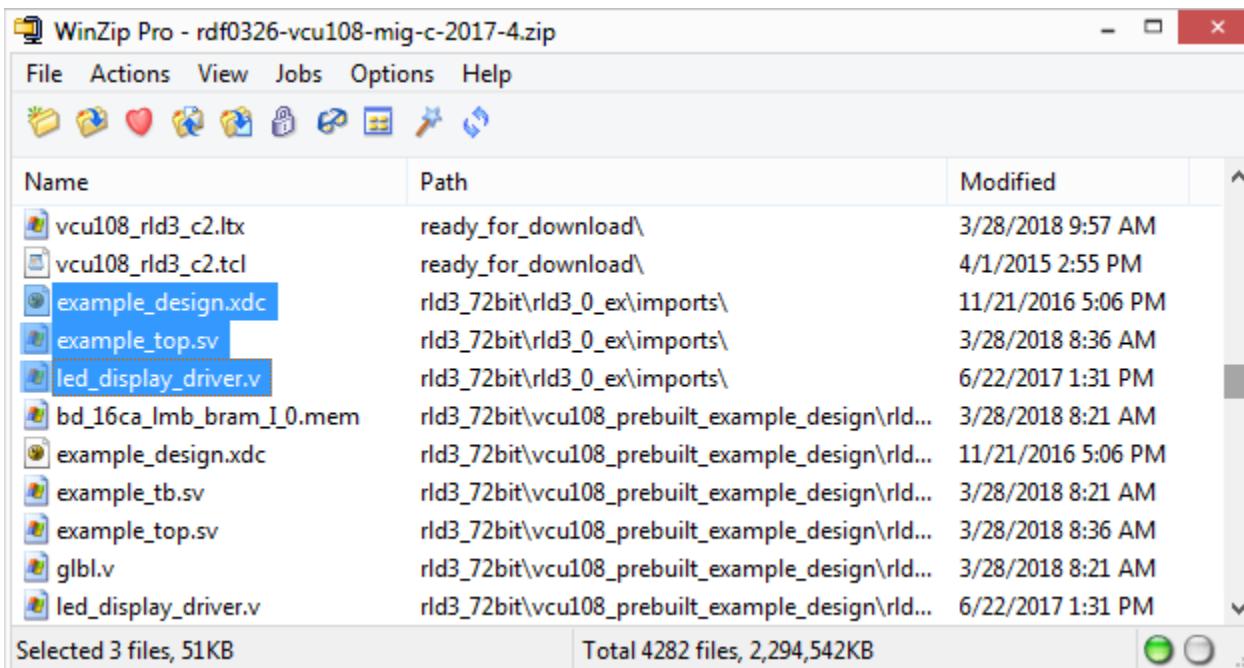
Note: The original project window can be closed

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# Modifications to Example Design

## ► From the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file

- Extract the **rld3\_72bit** files, **example\_design.xdc**, **example\_top.sv**, and **led\_display\_driver.v**
- Overwrite these three existing files in your **rld3\_72bit** MIG design
- Do this **after** creating the Example Design; changes only affect the Example Design



# Modifications to Example Design

## ► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs and AR66800
- The following commands will add the led\_display\_driver.v and create the required VIO IP
- From the Tcl Console, run these commands:

```
add_files -norecurse
```

```
C:/vcu108_mig/rld3_72bit/rld3_0_ex/imports/led_display_driver.v
```

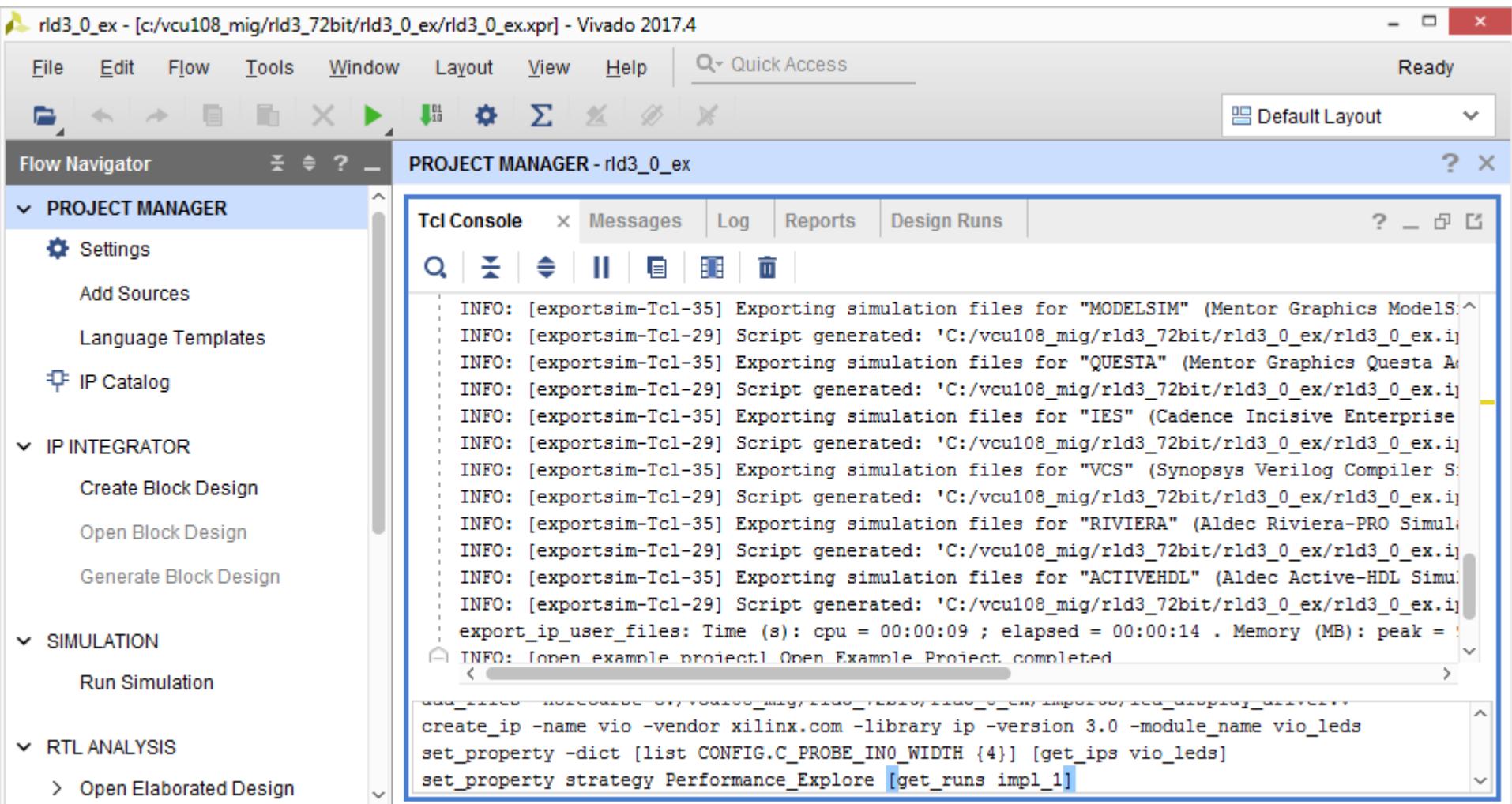
```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

```
set_property strategy Performance_Explore [get_runs impl_1]
```

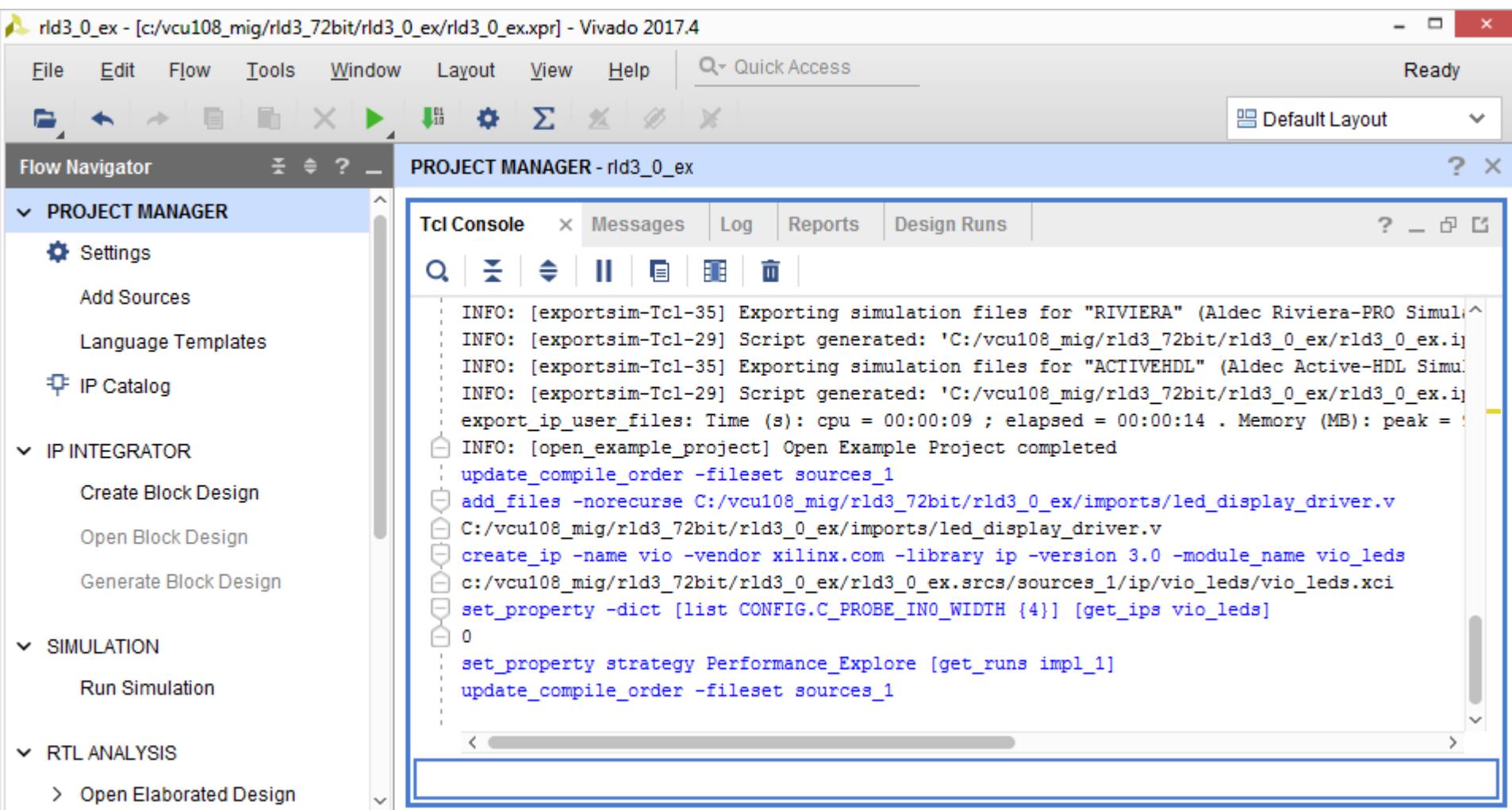
# Modifications to Example Design

► Press enter after entering Tcl commands



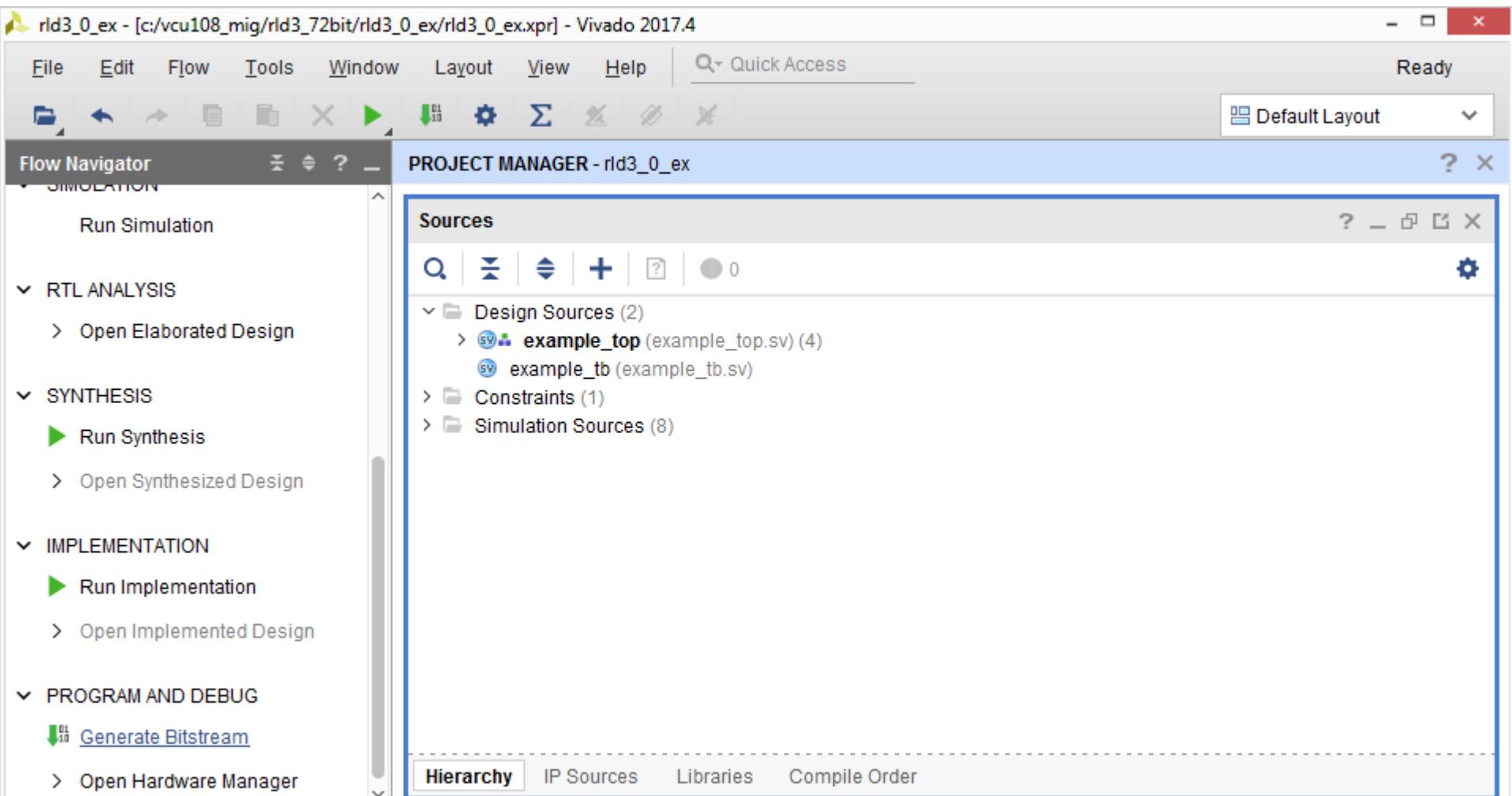
# Modifications to Example Design

► Tcl commands completed successfully



# Compile Example Design

► Click on **Generate Bitstream**



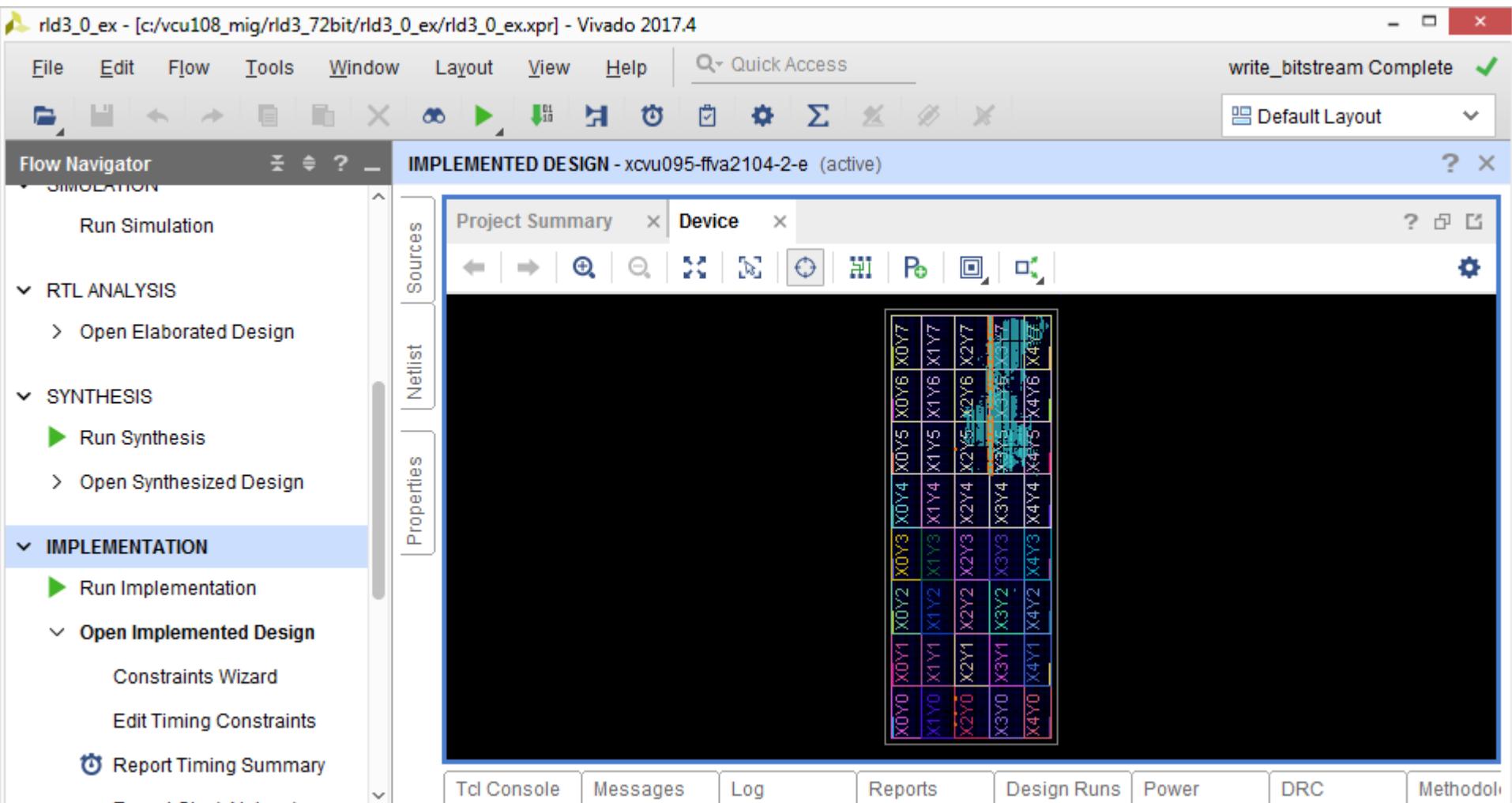
Generate a programming file after implementation

Note: Presentation applies to the VCU108

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# Compile Example Design

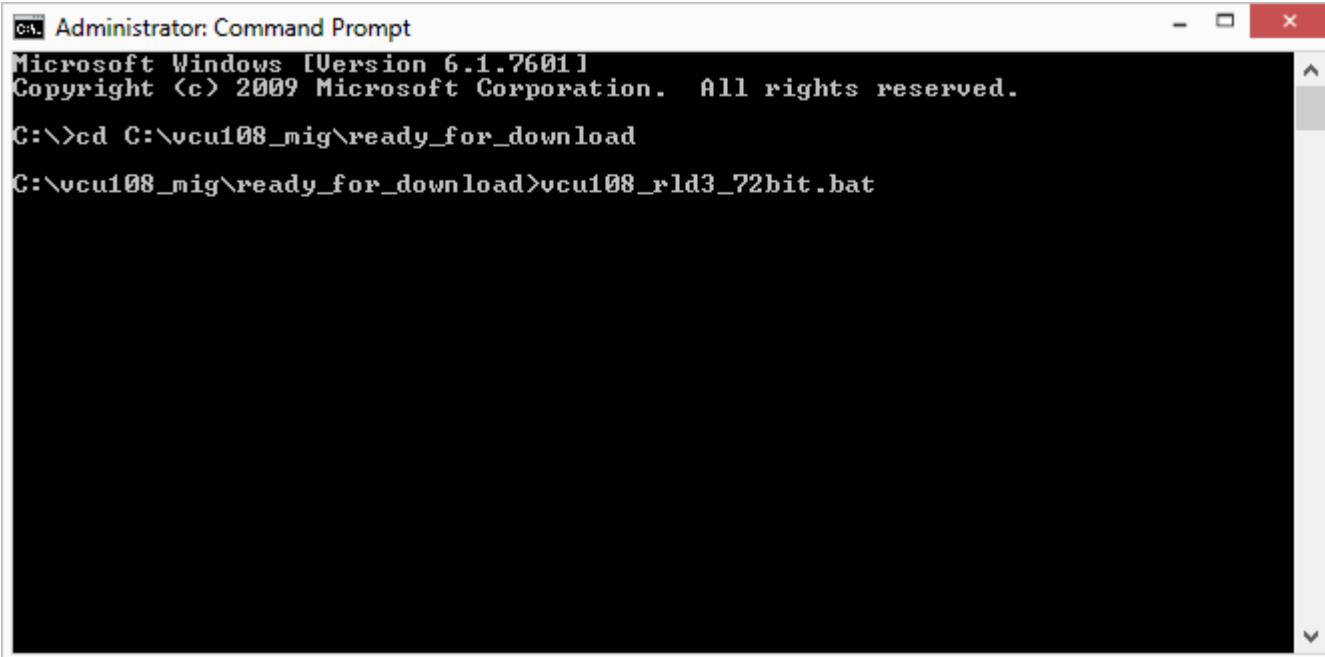
► Open and view the Implemented Design



# Run MIG Example Design

- ▶ From a Command Prompt, type:

```
cd C:\vcu108_mig\ready_for_download  
vcu108_rld3_72bit.bat
```

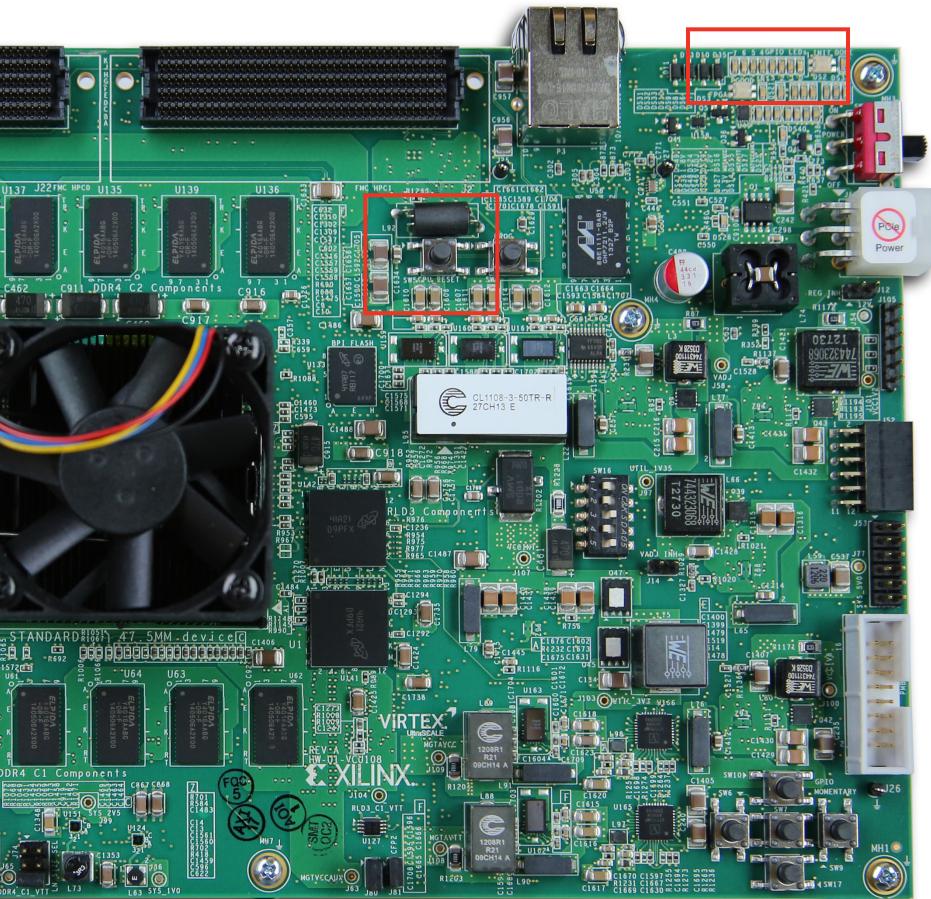


The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window displays the following text:

```
Microsoft Windows [Version 6.1.7601]
Copyright <c> 2009 Microsoft Corporation. All rights reserved.

C:>cd C:\vcu108_mig\ready_for_download
C:\vcu108_mig\ready_for_download>vcu108_rld3_72bit.bat
```

# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset

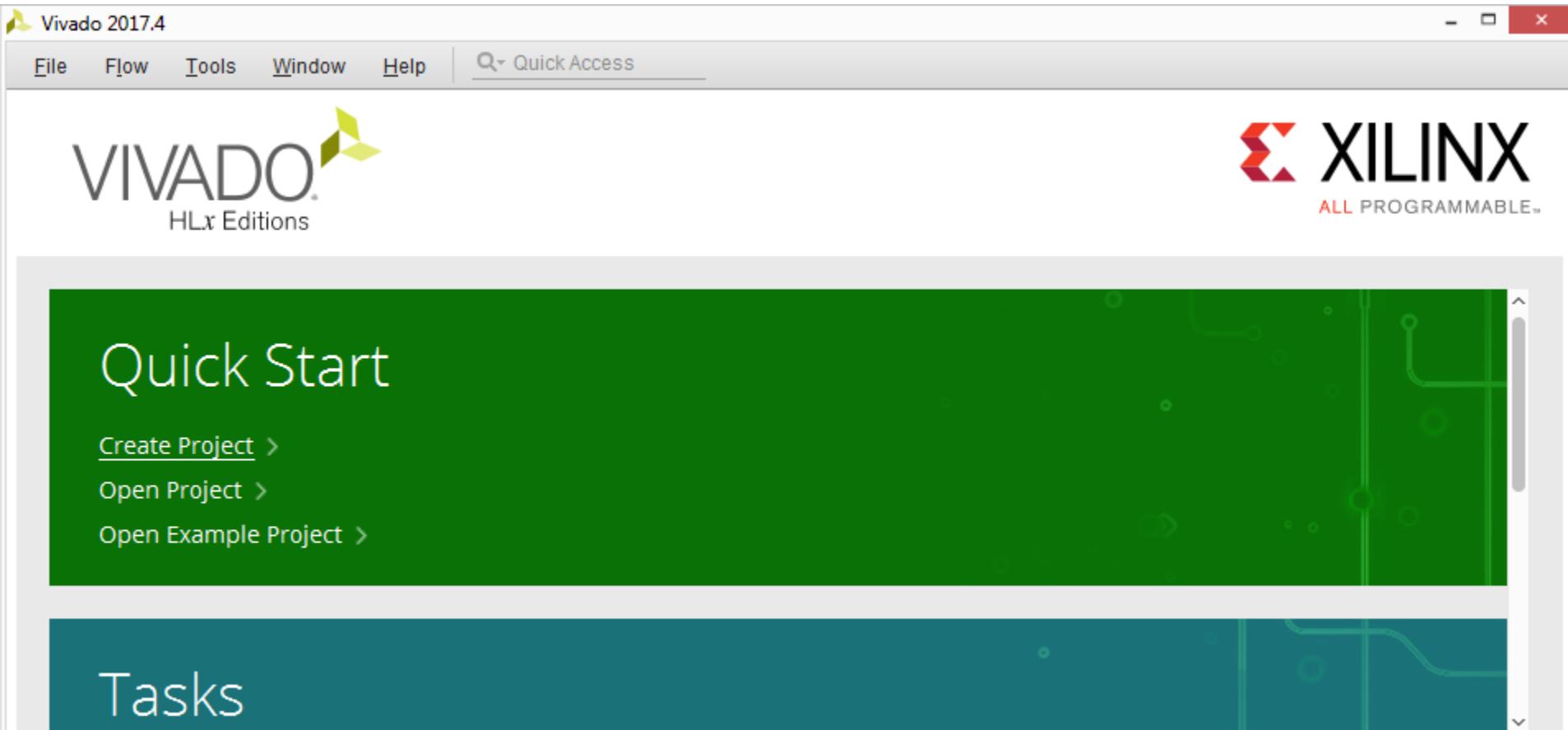
# Generate MIG RLD3 36 Bit C1 Example Design

# Generate MIG RLD3 36 Bit C1 Example Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.4 → Vivado

► Select Create Project



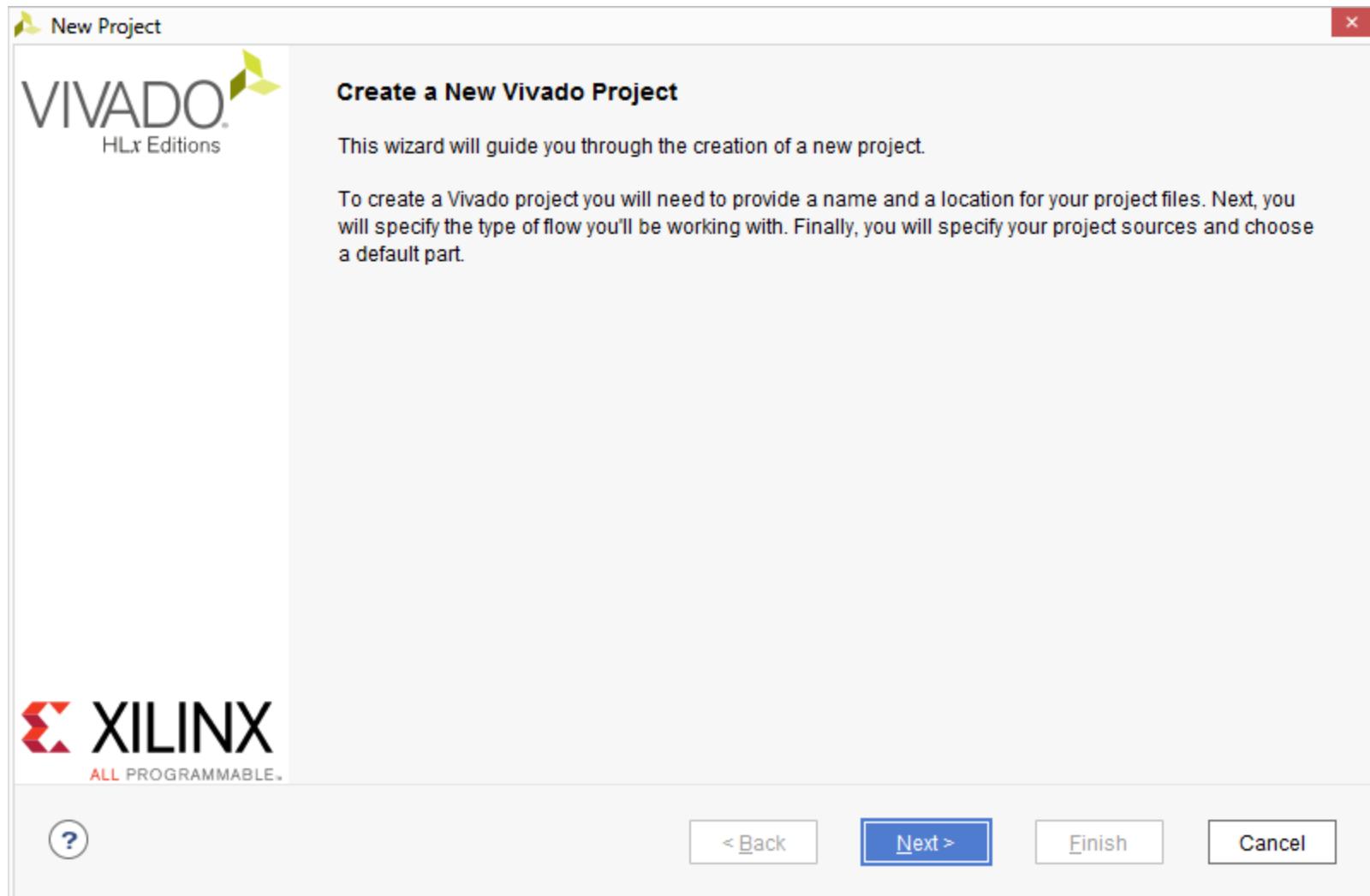
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU108

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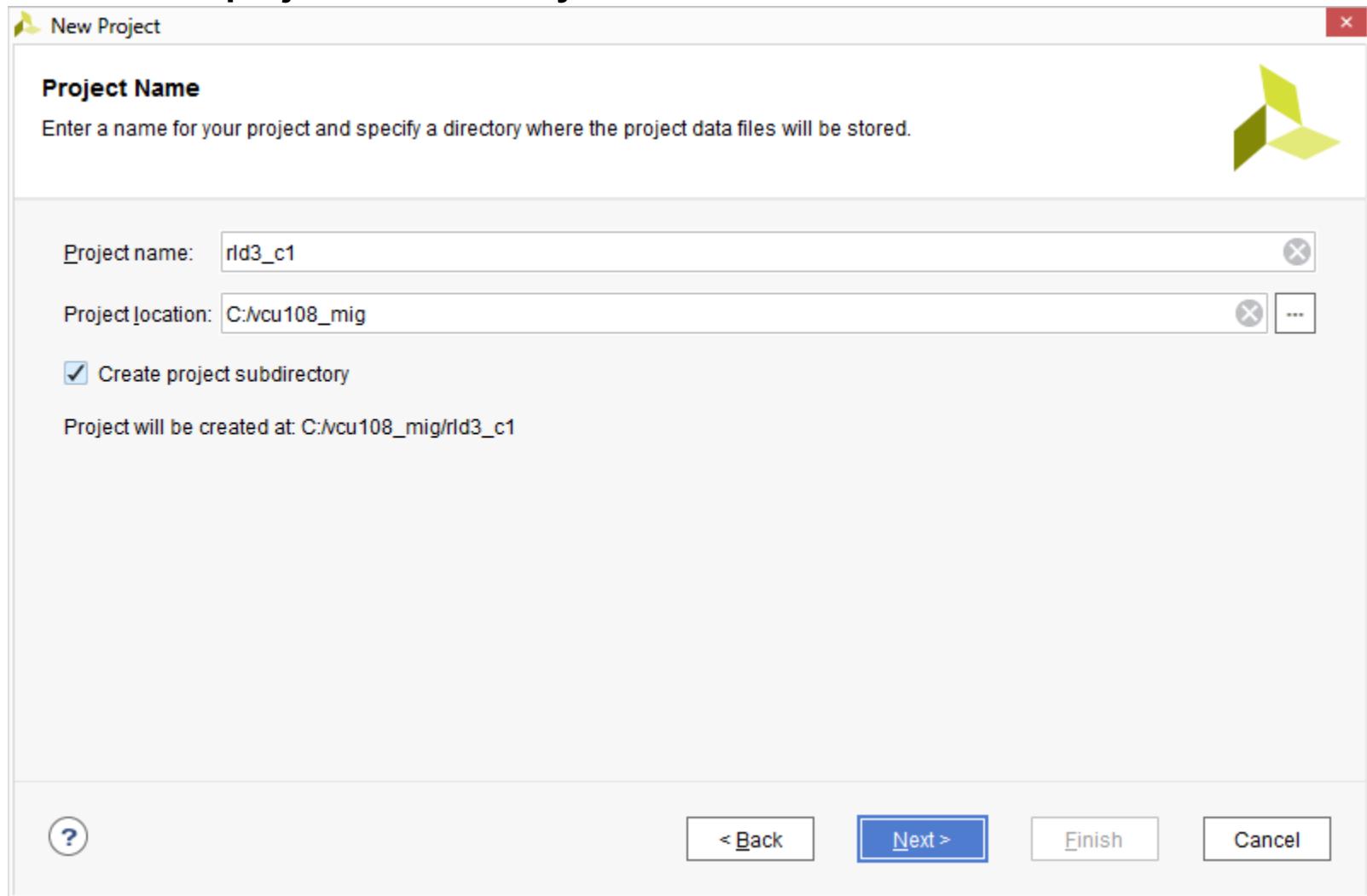
# Generate MIG RLD3 36 Bit C1 Example Design

► Click Next



# Generate MIG RLD3 36 Bit C1 Example Design

- Set the Project name to **rld3\_c1** and location to **C:/vcu108\_mig**
  - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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# Generate MIG RLD3 36 Bit C1 Example Design

## ► Select RTL Project

- Select **Do not specify sources at this time**

New Project

**Project Type**  
Specify the type of project to create.



RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Generate MIG RLD3 36 Bit C1 Example Design

► Under Boards, select the **VCU108 Evaluation Platform**

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

Filter/ Preview

Vendor: All  
Display Name: All  
Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2
<b>Virtex-UltraScale VCU108 Evaluation Platform</b>	xilinx.com	1.0	<b>xcvu095-ffa2104-2-e</b>
Virtex-UltraScale VCU110 Evaluation Platform	xilinx.com	1.0	xcvu190-flfc2104-2-e

No Board Connectors

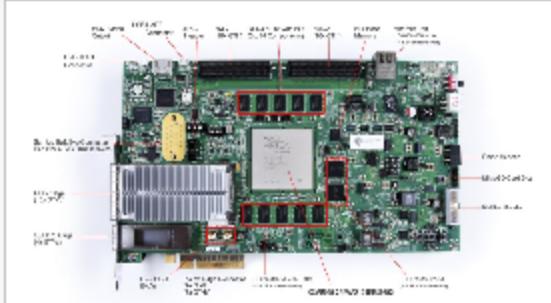
?

< Back

Next >

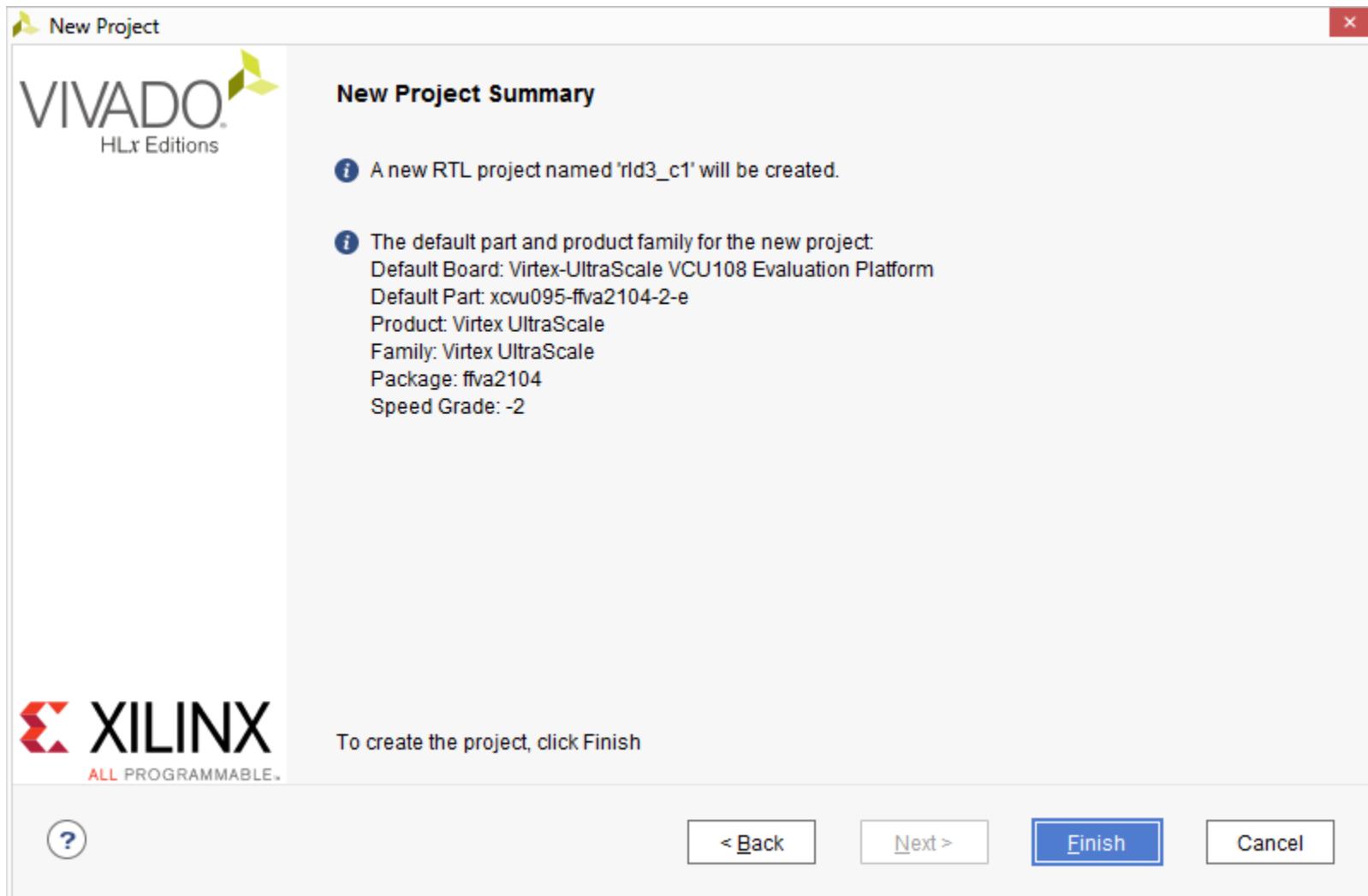
Finish

Cancel



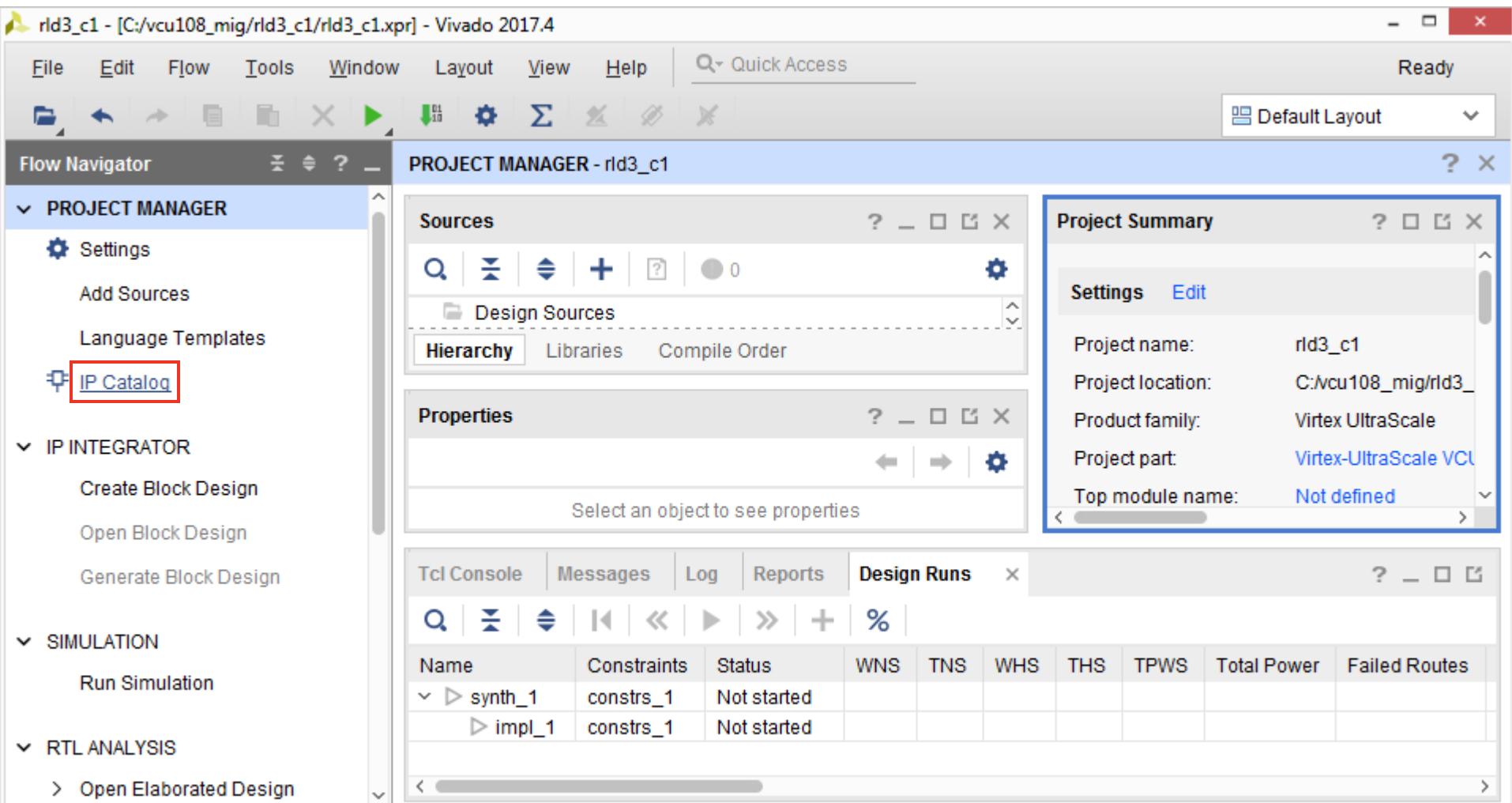
# Generate MIG RLD3 36 Bit C1 Example Design

► Click Finish



# Generate MIG RLD3 36 Bit C1 Example Design

► Click on IP Catalog



# Generate MIG RLD3 36 Bit C1 Example Design

## ► Select RLDRAM3 (MIG), v1.4

The screenshot shows the Vivado 2017.4 interface with the project "rld3\_c1" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, RTL Analysis, and Flow Navigator. The IP Catalog section is selected in the Project Manager. The main area displays the IP Catalog with tabs for Project Summary and IP Catalog. Under the IP Catalog tab, the "Cores" tab is selected. The table lists various memory components:

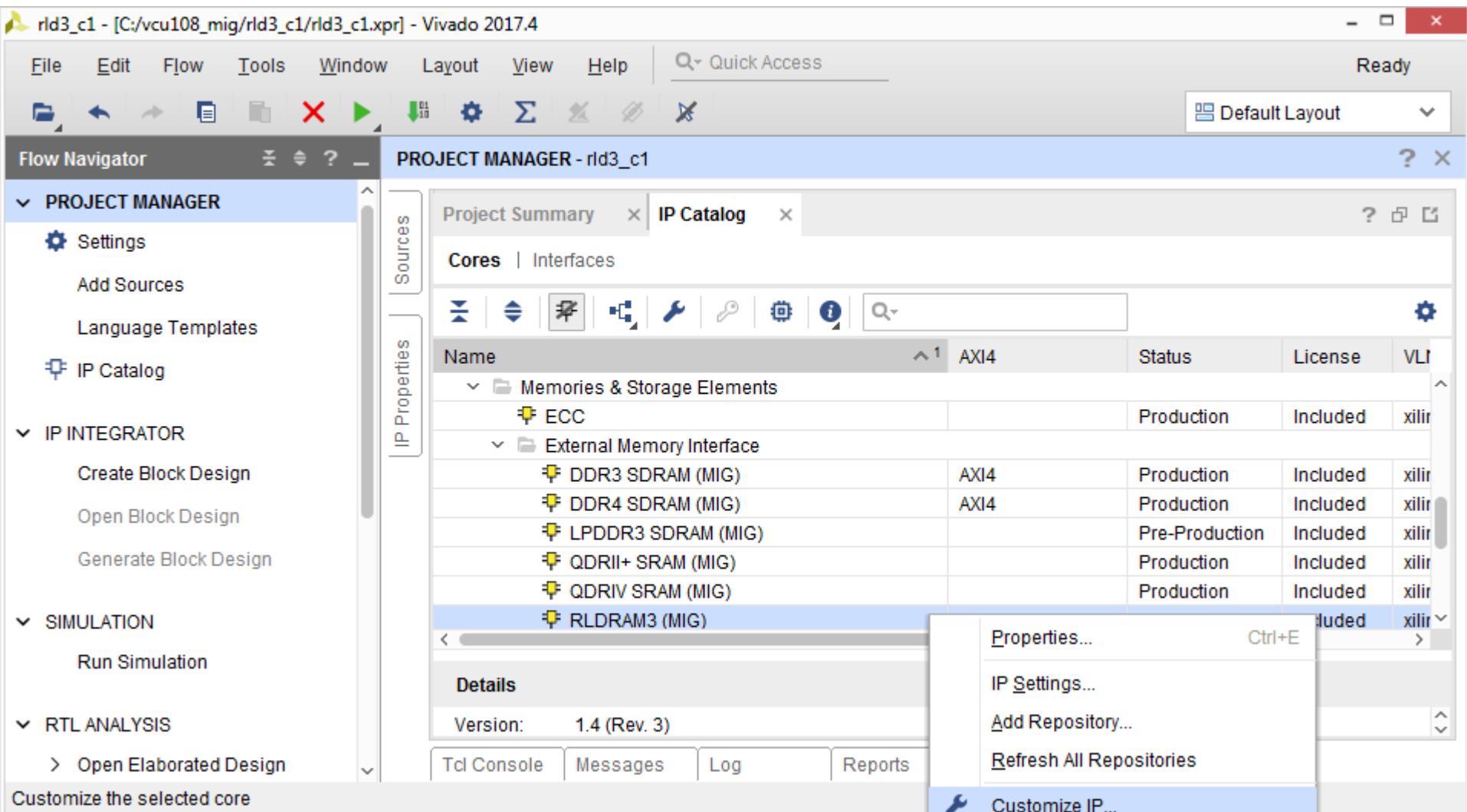
Name	Status	License	VLI	
ECC	Production	Included	xilinx	
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)		Pre-Production	Included	xilinx
QDRII+ SRAM (MIG)		Production	Included	xilinx
QDRIV SRAM (MIG)		Production	Included	xilinx
<b>RLDRAM3 (MIG)</b>	<b>Production</b>	<b>Included</b>	<b>xilinx</b>	

Details for the selected RLD3 component show Version: 1.4 (Rev. 3). The bottom navigation bar includes Tcl Console, Messages, Log, Reports, and Design Runs.

# Generate MIG RLD3 36 Bit C1 Example Design

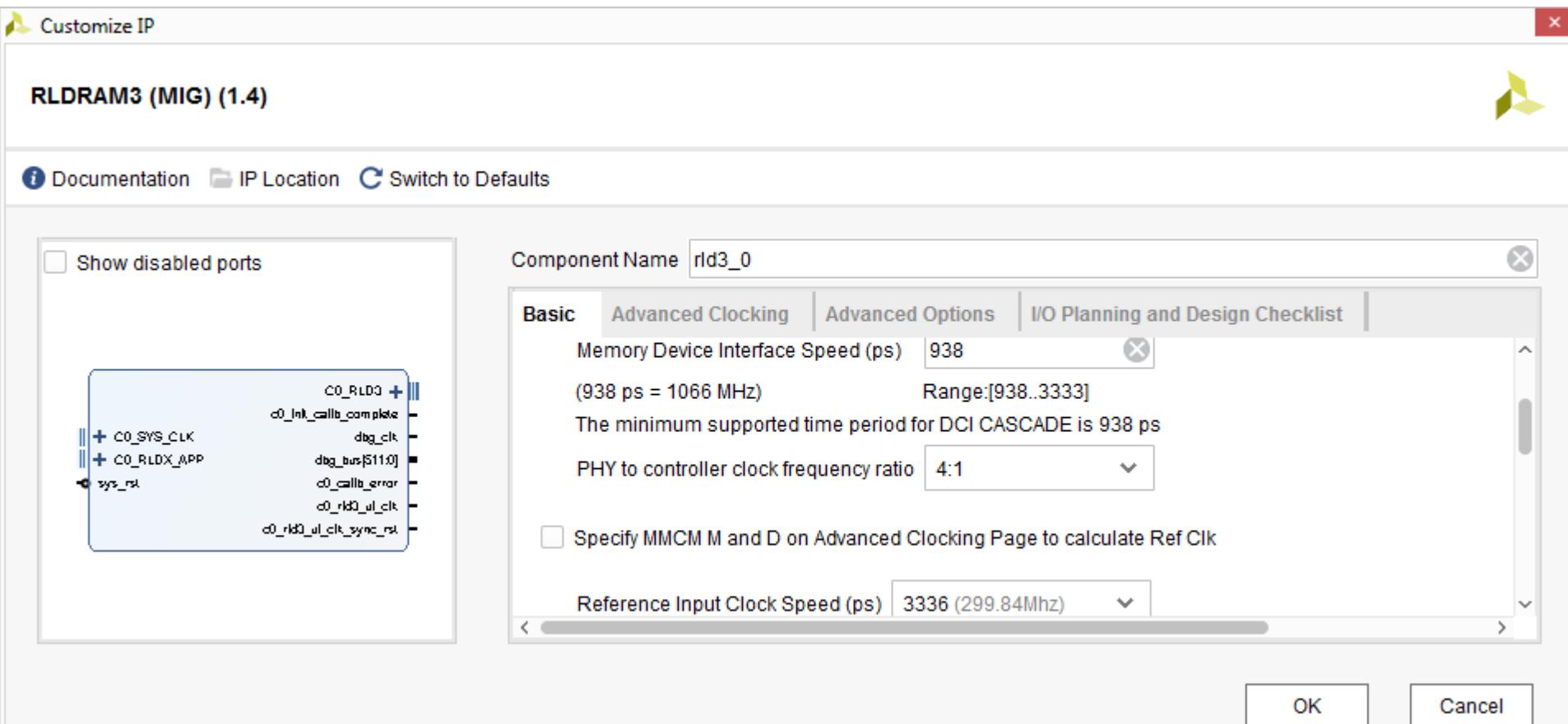
► Right click on **RLDRAM3 (MIG)**

- Select **Customize IP**



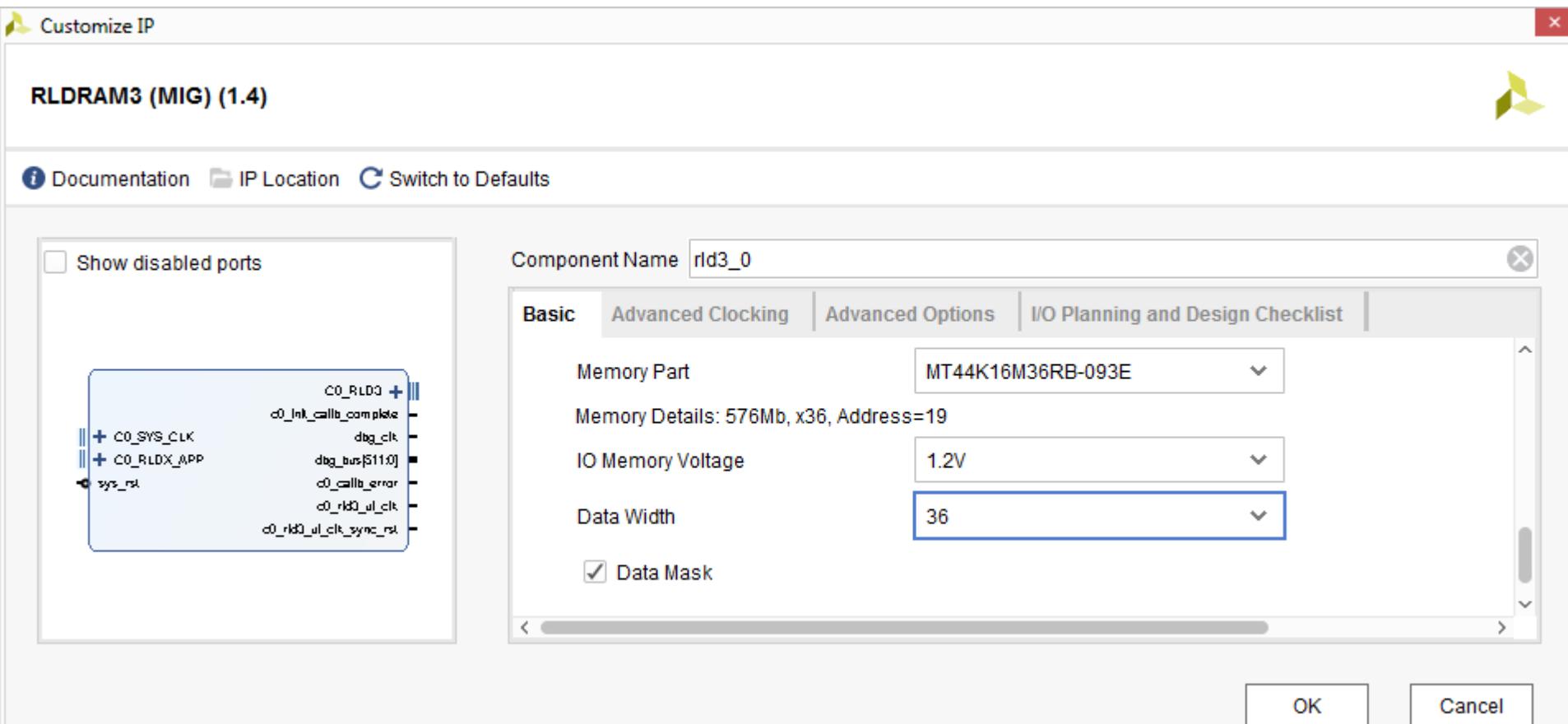
# Generate MIG RLD3 36 Bit C1 Example Design

- Set Clock period to **938** for 2133 Mb/s operation.
- Set the Input Clock to **3336** ps for 300 MHz
- Scroll down



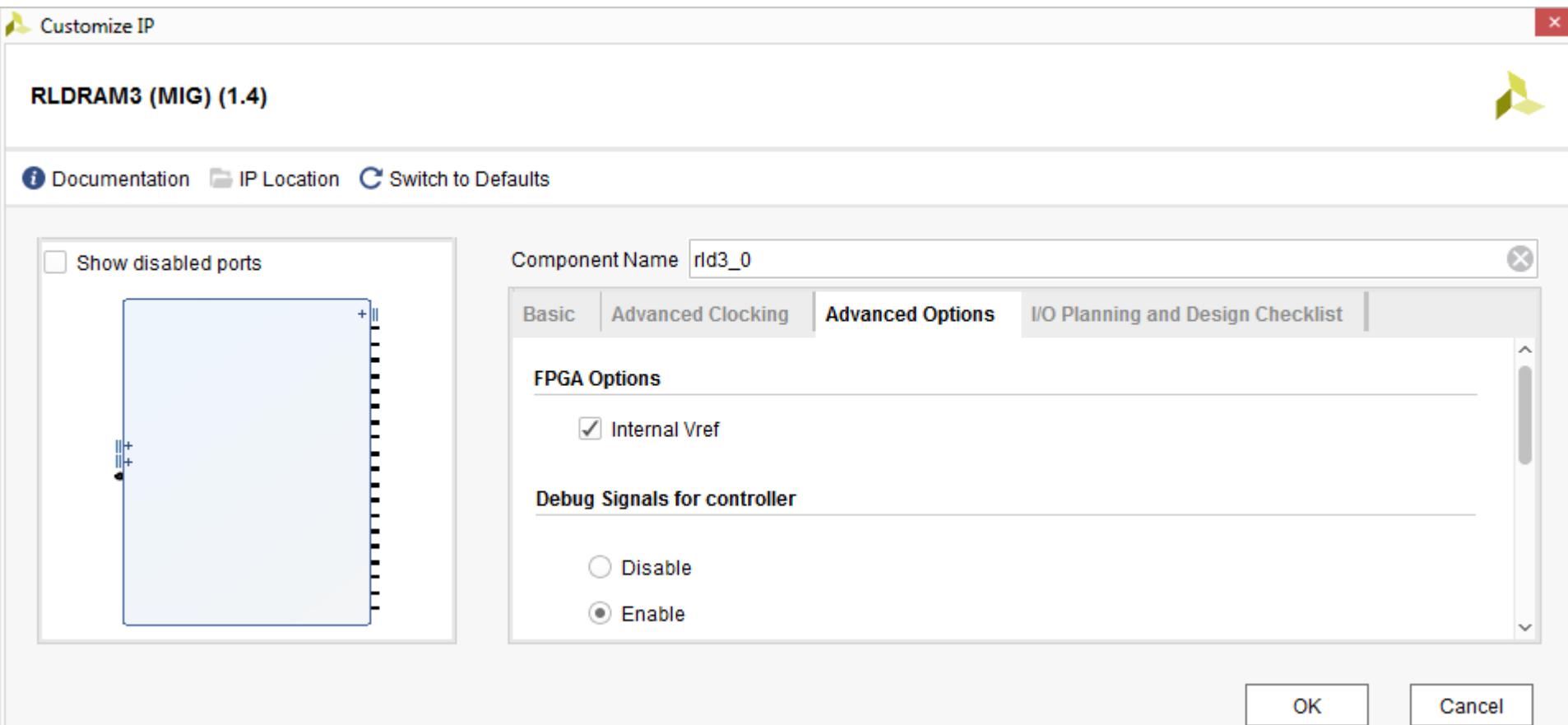
# Generate MIG RLD3 36 Bit C1 Example Design

- Select the part **MT44K16M36RB\_093E**
- Set the Data Width to **36** and click the **Advanced Options** Tab



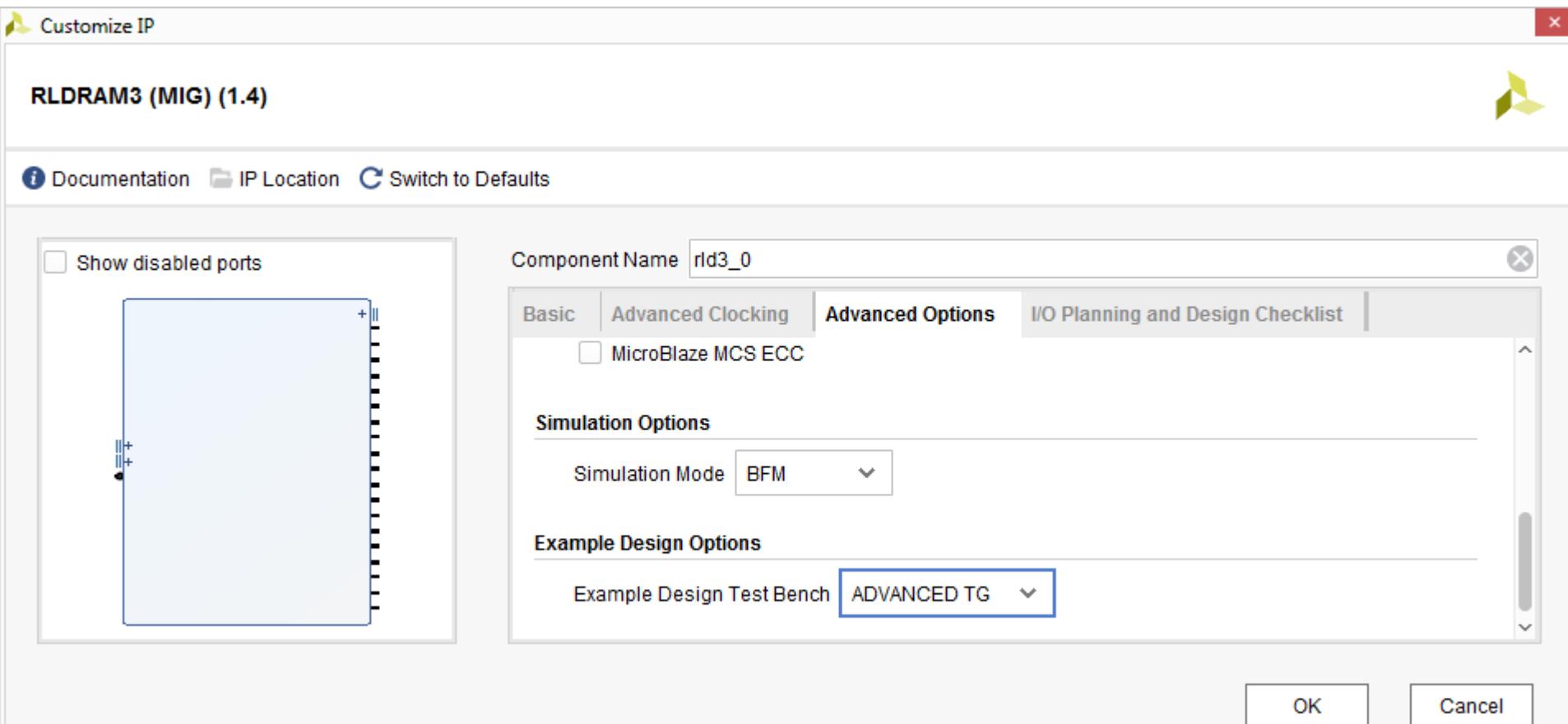
# Generate MIG RLD3 36 Bit C1 Example Design

- Set the Debug Signals to **Enable**
- Scroll down



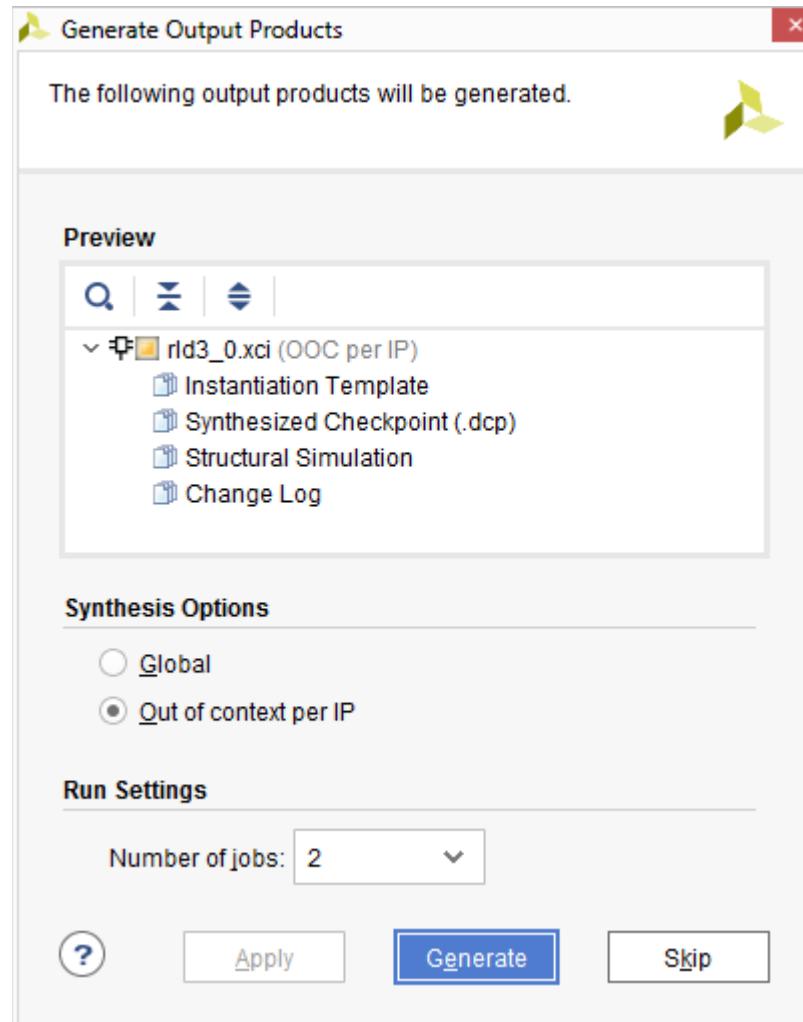
# Generate MIG RLD3 36 Bit C1 Example Design

- Select ADVANCED TG
- Click OK



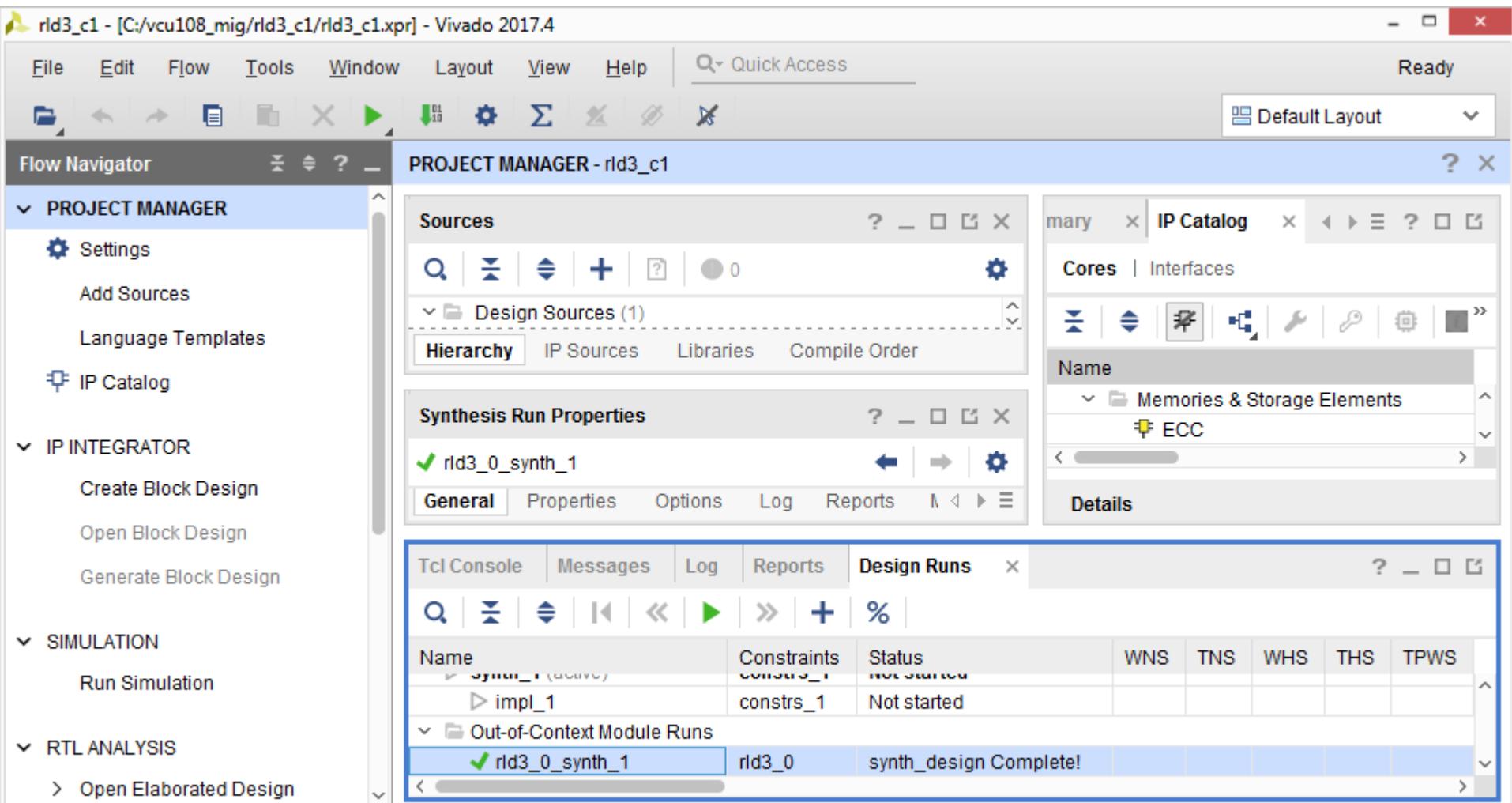
# Generate MIG RLD3 36 Bit C1 Example Design

► Click Generate



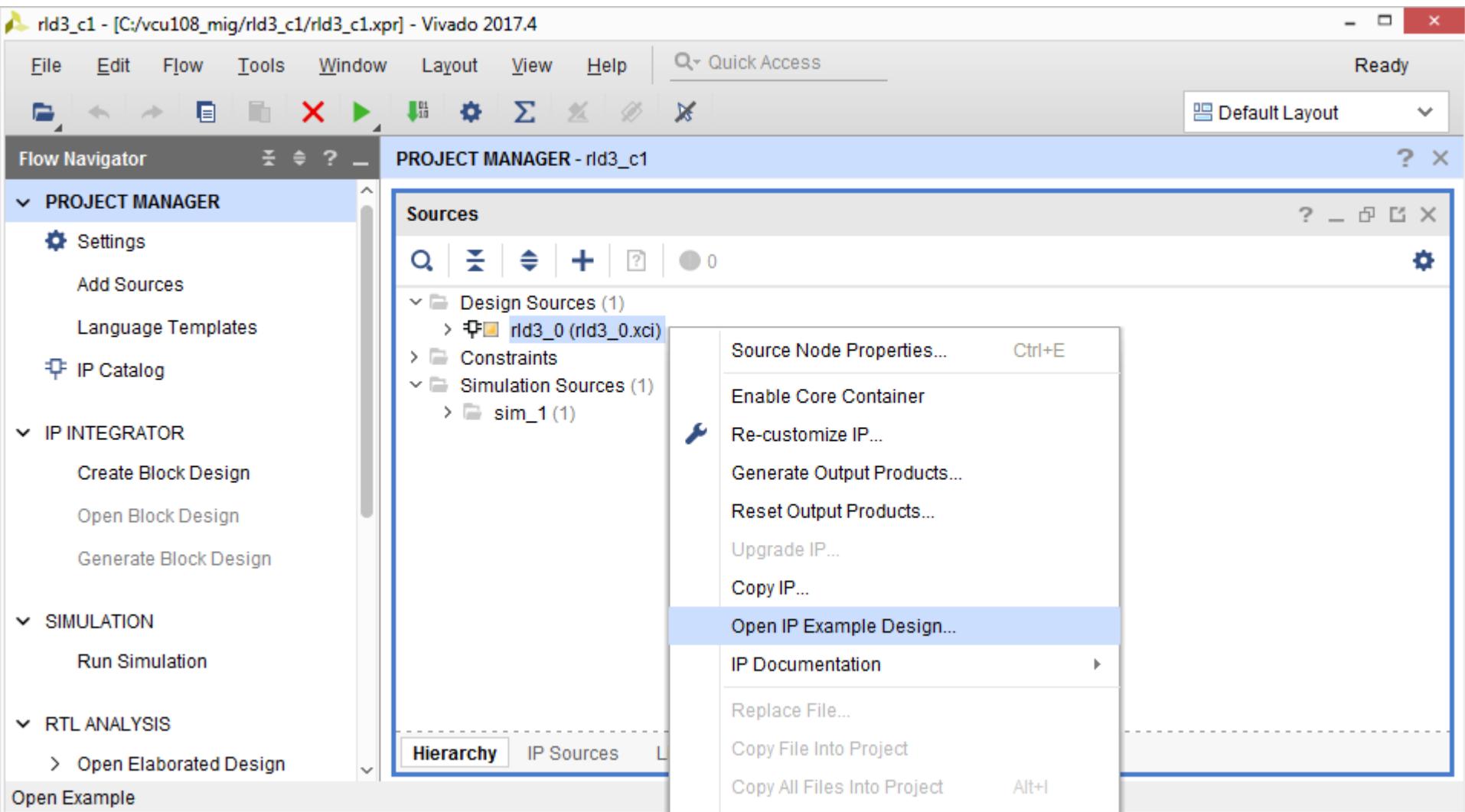
# Generate MIG RLD3 36 Bit C1 Example Design

► Wait until checkmark appears on **rld3\_0\_synth\_1**



# Compile Example Design

► Right click on **rld3\_0** and select **Open IP Example Design...**

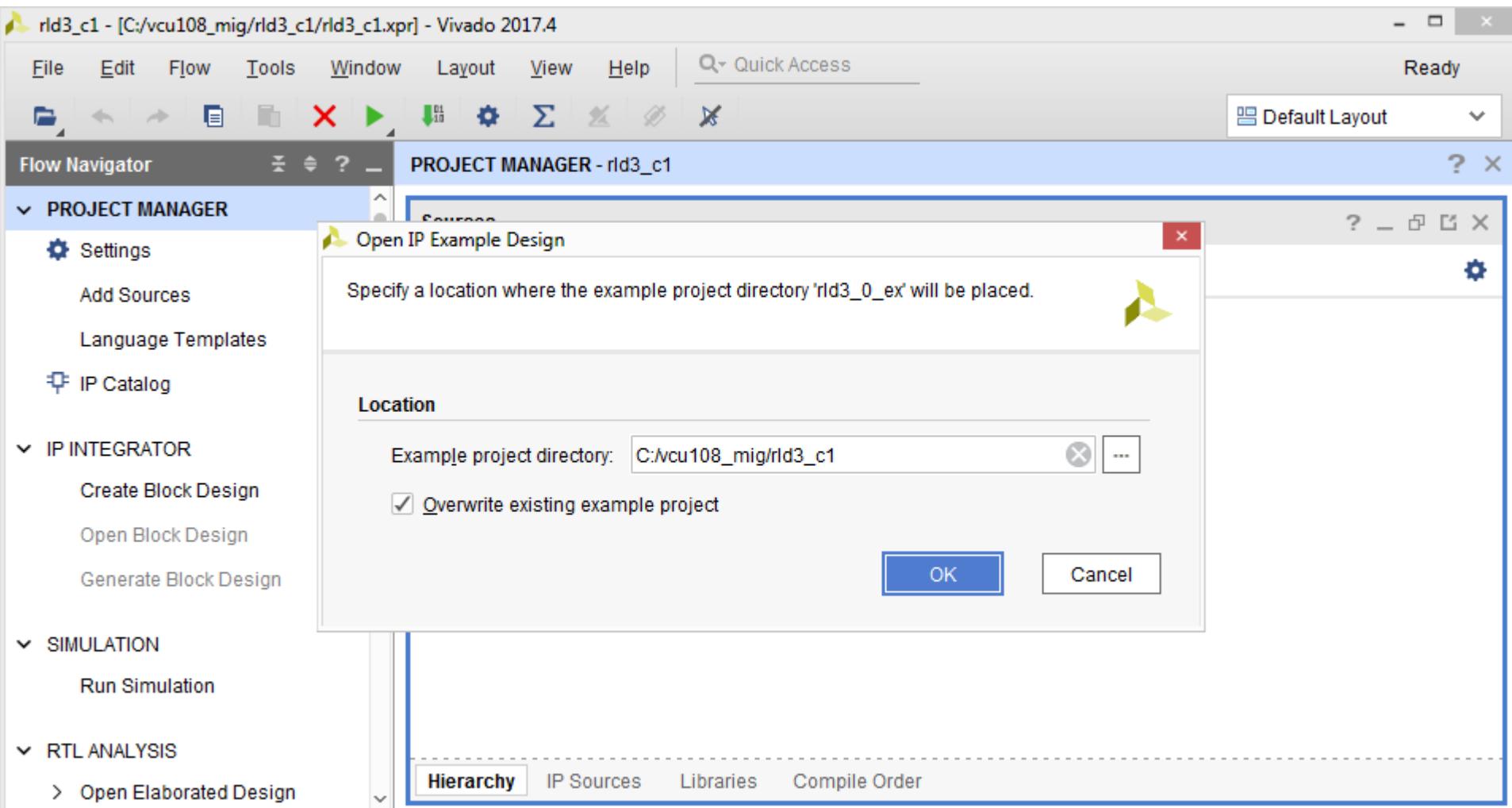


Note: Presentation applies to the VCU108

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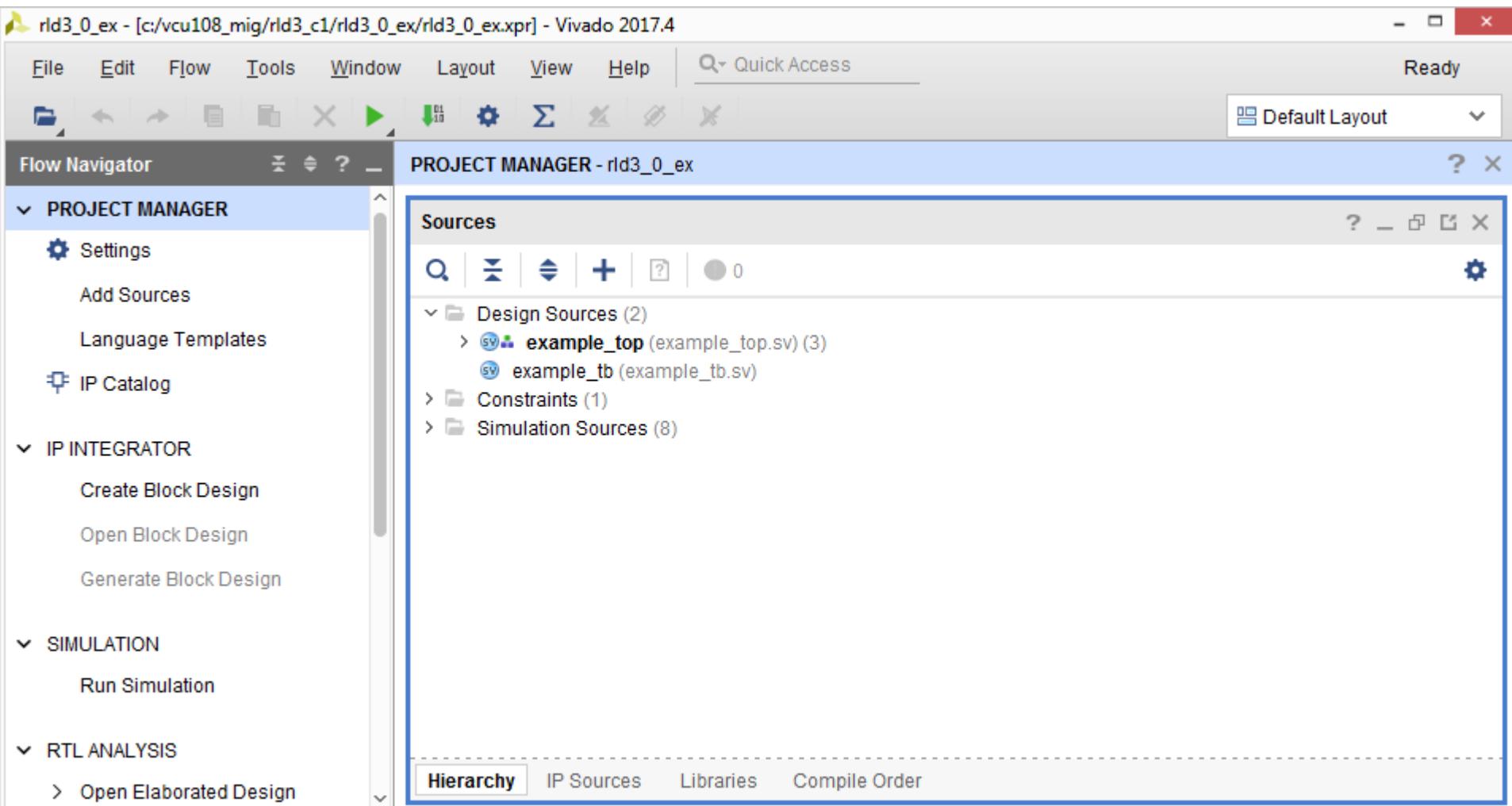
# Compile Example Design

► Set the location to **C:/vcu108\_mig/rld3\_c1** and click **OK**



# Compile Example Design

► A new project is created under <design path>/



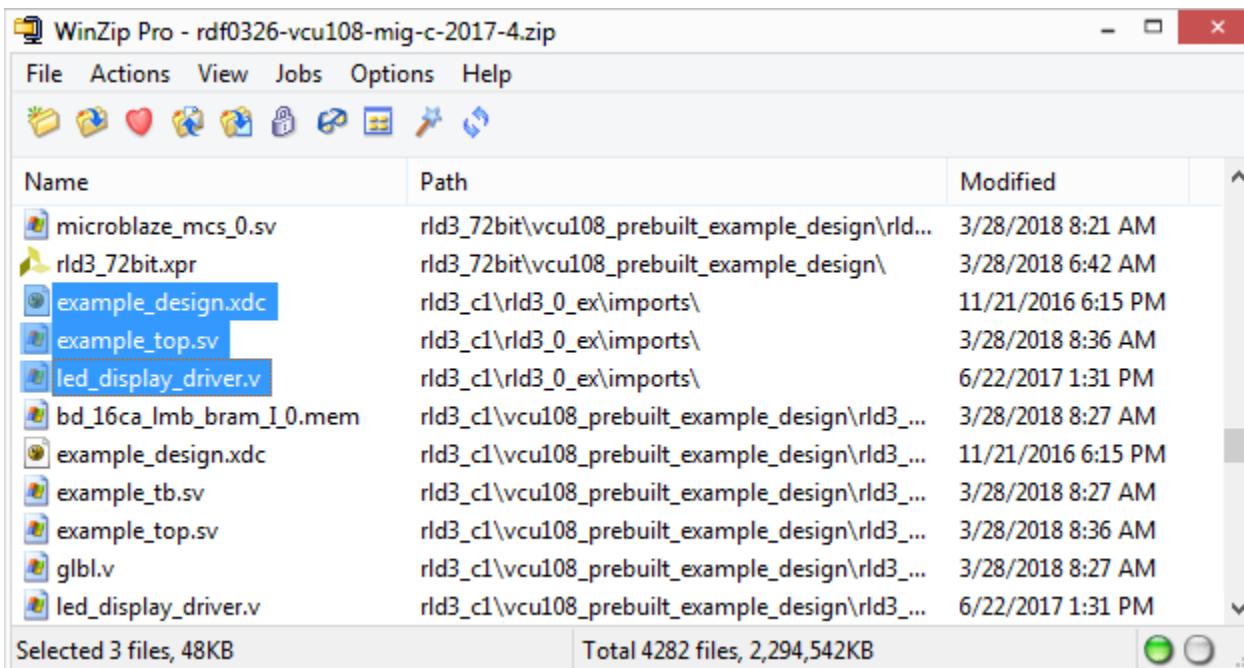
Note: The original project window can be closed

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# Modifications to Example Design

## ► From the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file

- Extract the **rld3\_c1** files, **example\_design.xdc**, **example\_top.sv**, and **led\_display\_driver.v**
- Overwrite these three existing files in your **rld3\_c1** MIG design
- Do this **after** creating the Example Design; changes only affect the Example Design



# Modifications to Example Design

## ► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs
- The following commands will add the led\_display\_driver.v and create the required VIO IP
- From the Tcl Console, run these commands:

```
add_files -norecurse
```

```
C:/vcu108_mig/rld3_c1/rld3_0_ex/imports/led_display_driver.v
```

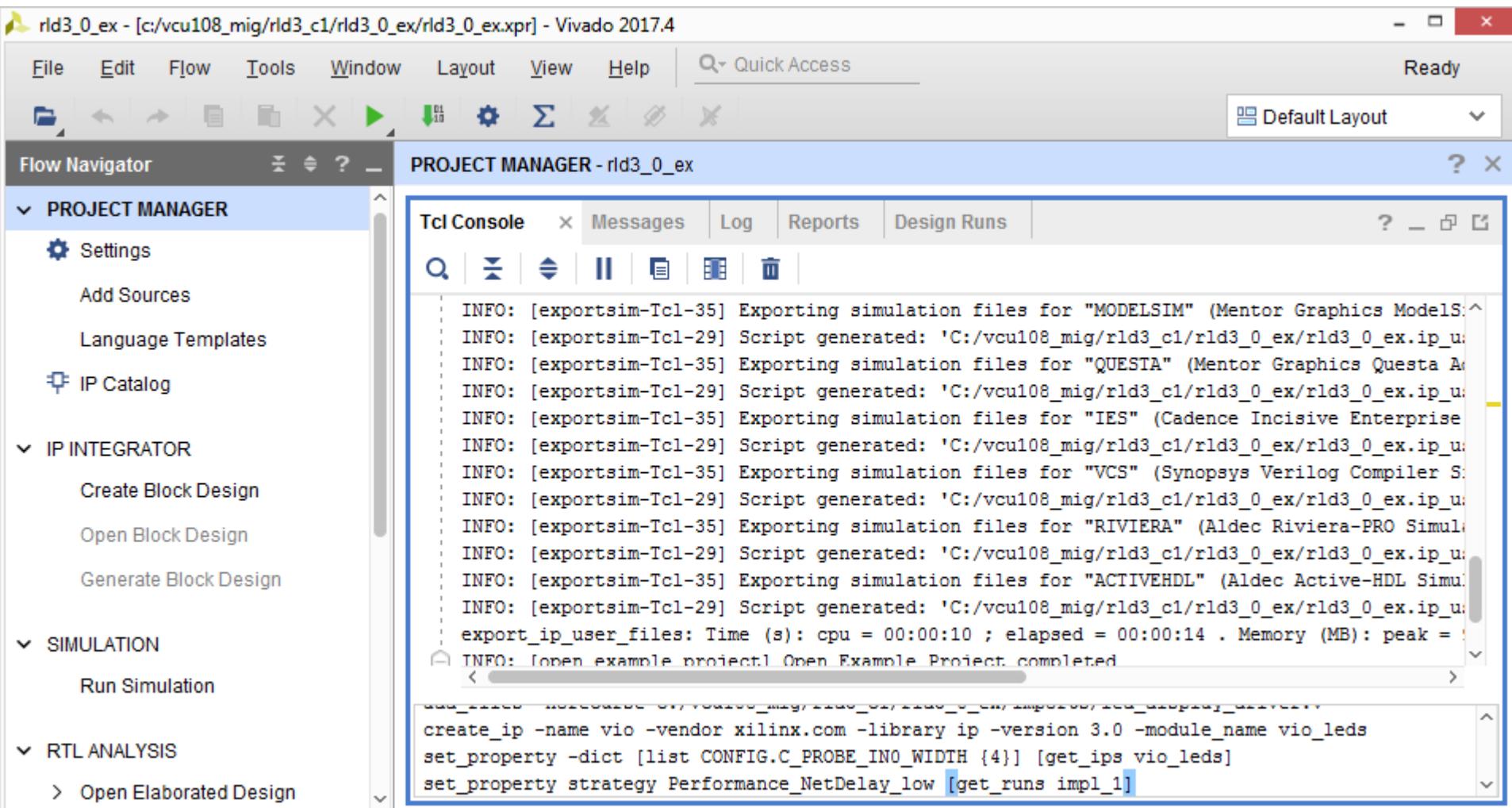
```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

```
set_property strategy Performance_NetDelay_low [get_runs impl_1]
```

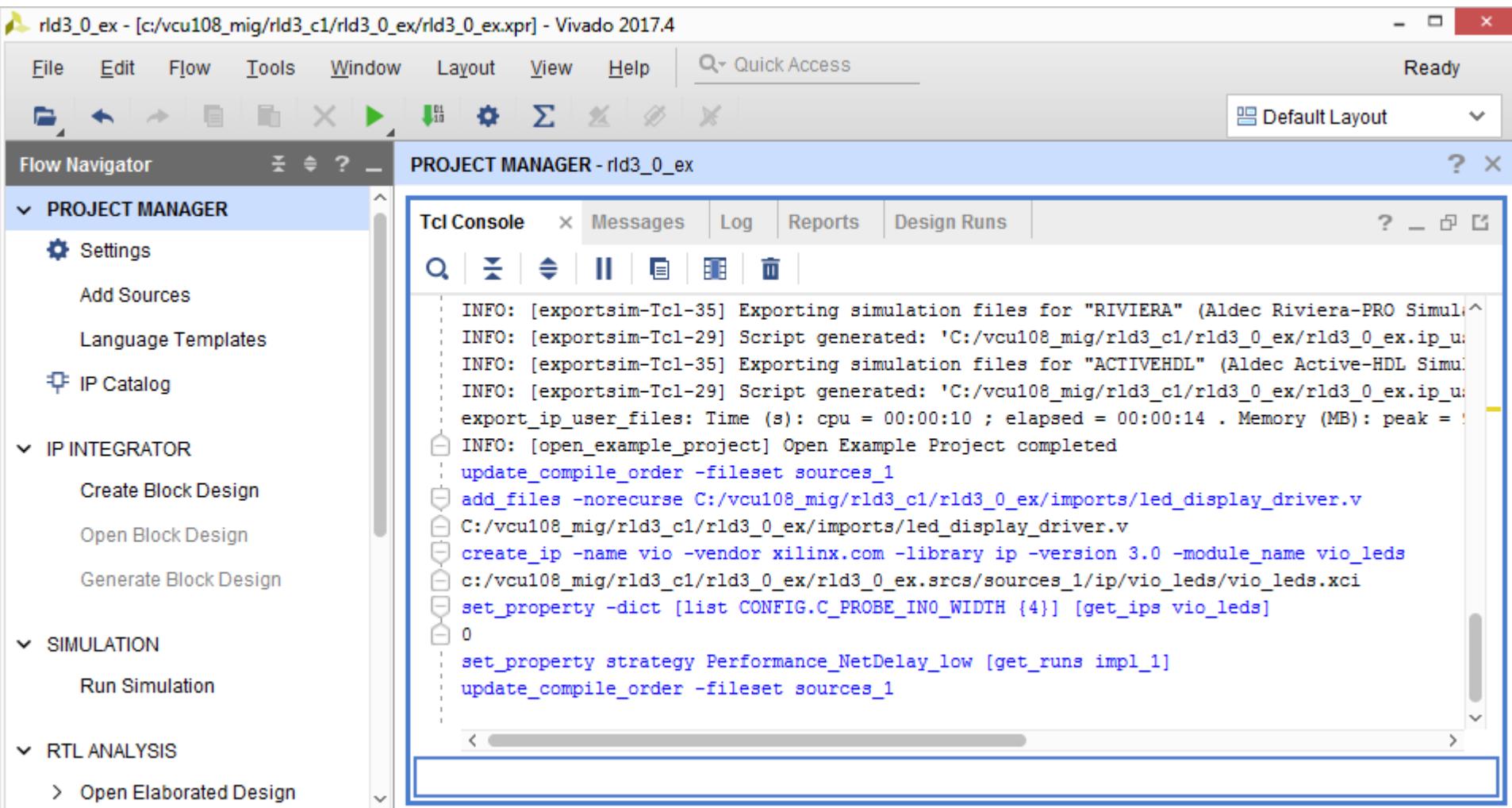
# Modifications to Example Design

► Press enter after entering Tcl commands



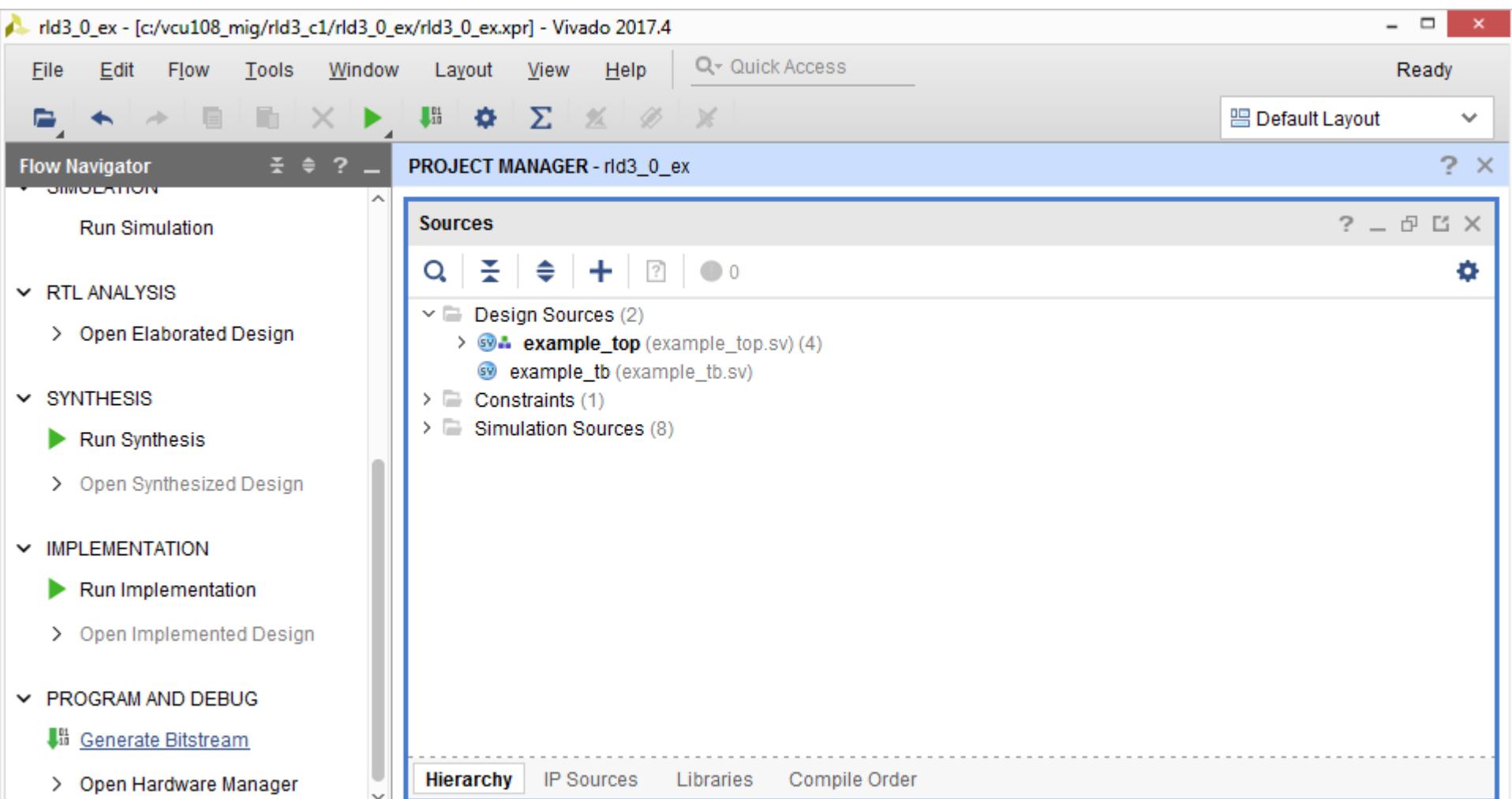
# Modifications to Example Design

► Tcl commands completed successfully



# Compile Example Design

► Click on **Generate Bitstream**



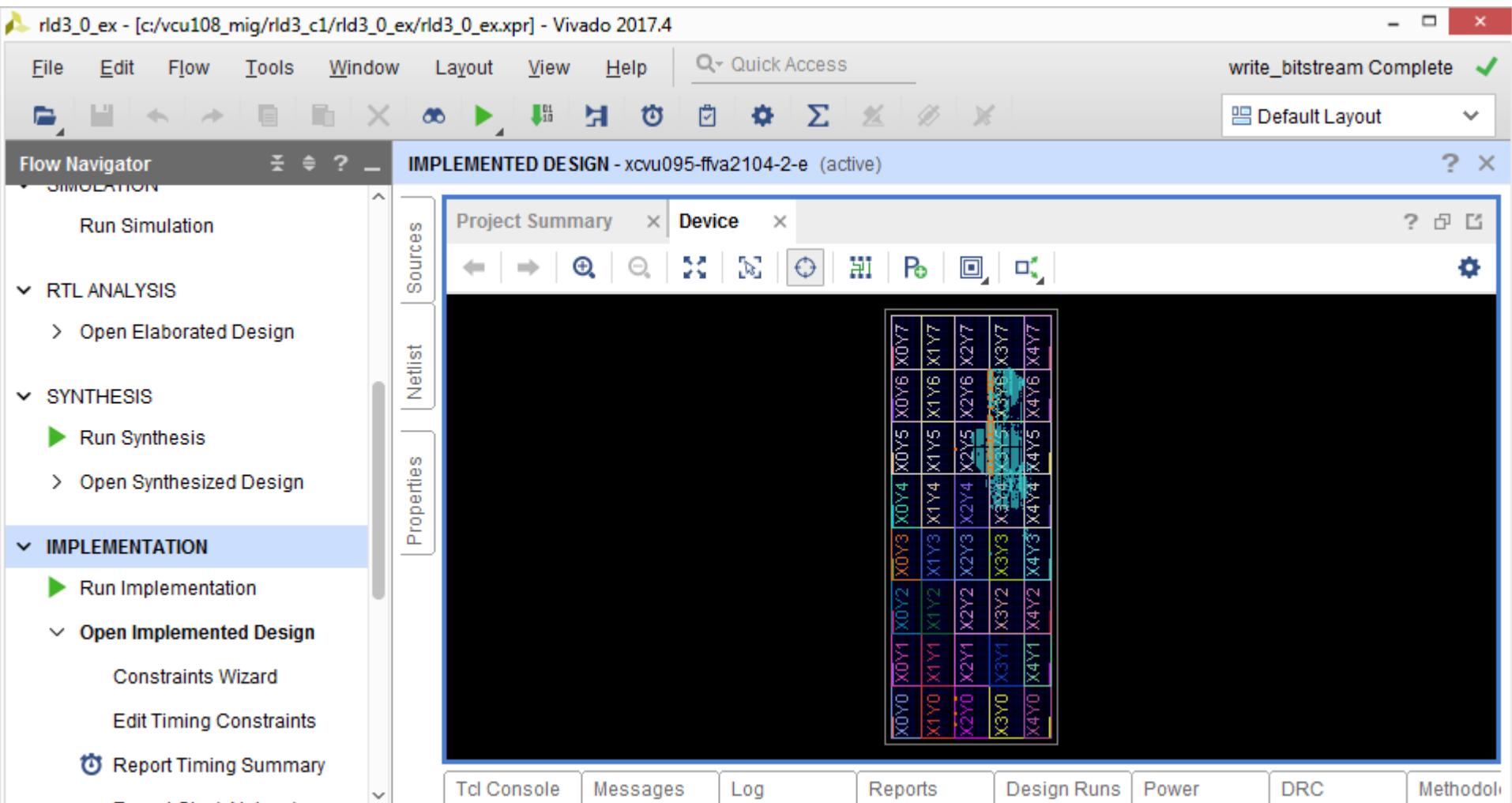
Generate a programming file after implementation

Note: Presentation applies to the VCU108

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# Compile Example Design

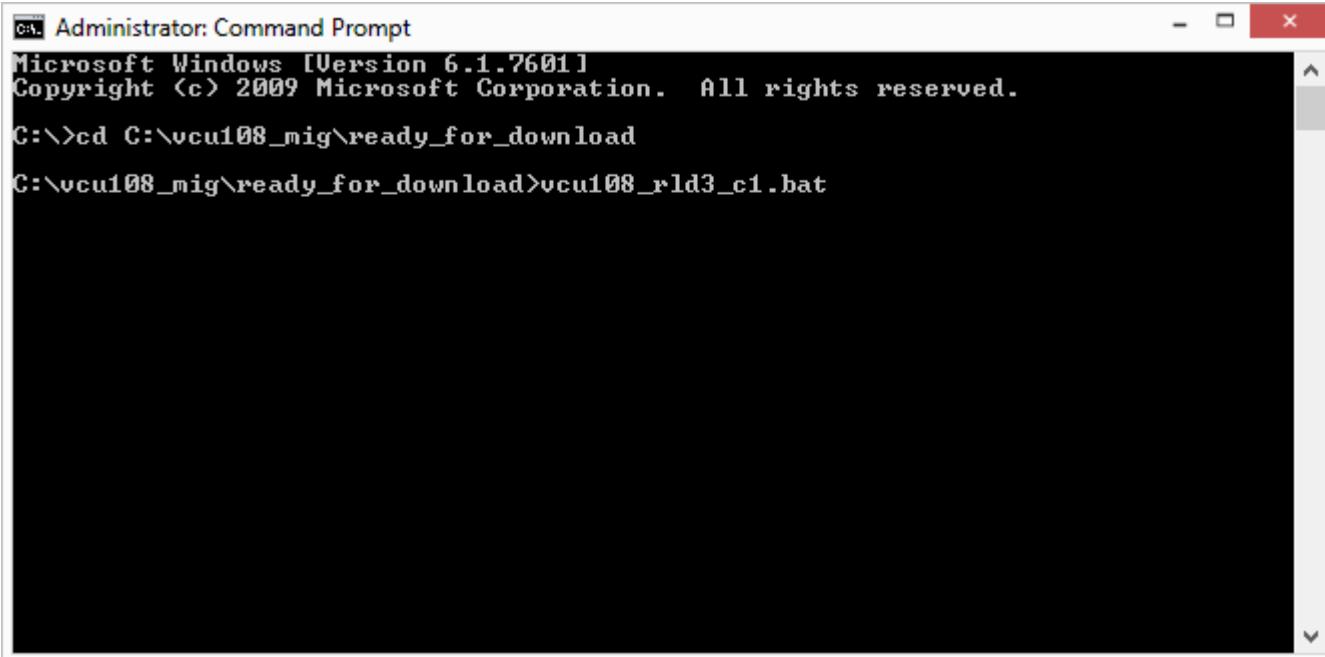
► Open and view the Implemented Design



# Run MIG Example Design

- ▶ From a Command Prompt, type:

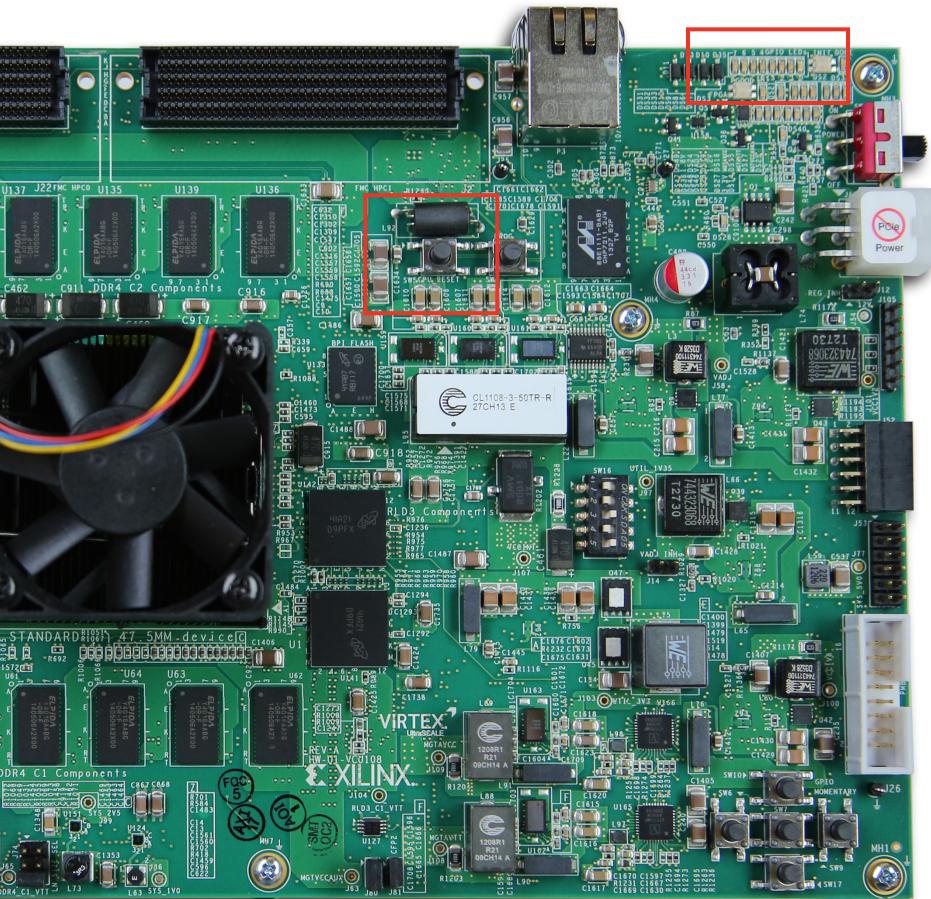
```
cd C:\vcu108_mig\ready_for_download  
vcu108_rld3_c1.bat
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window is running on Microsoft Windows [Version 6.1.7601]. The command history shows the user navigating to the directory C:\vcu108\_mig\ready\_for\_download and executing the batch file vcu108\_rld3\_c1.bat. The output of the batch file execution is completely blacked out.

```
C:\>cd C:\vcu108_mig\ready_for_download  
C:\vcu108_mig\ready_for_download>vcu108_rld3_c1.bat
```

# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset

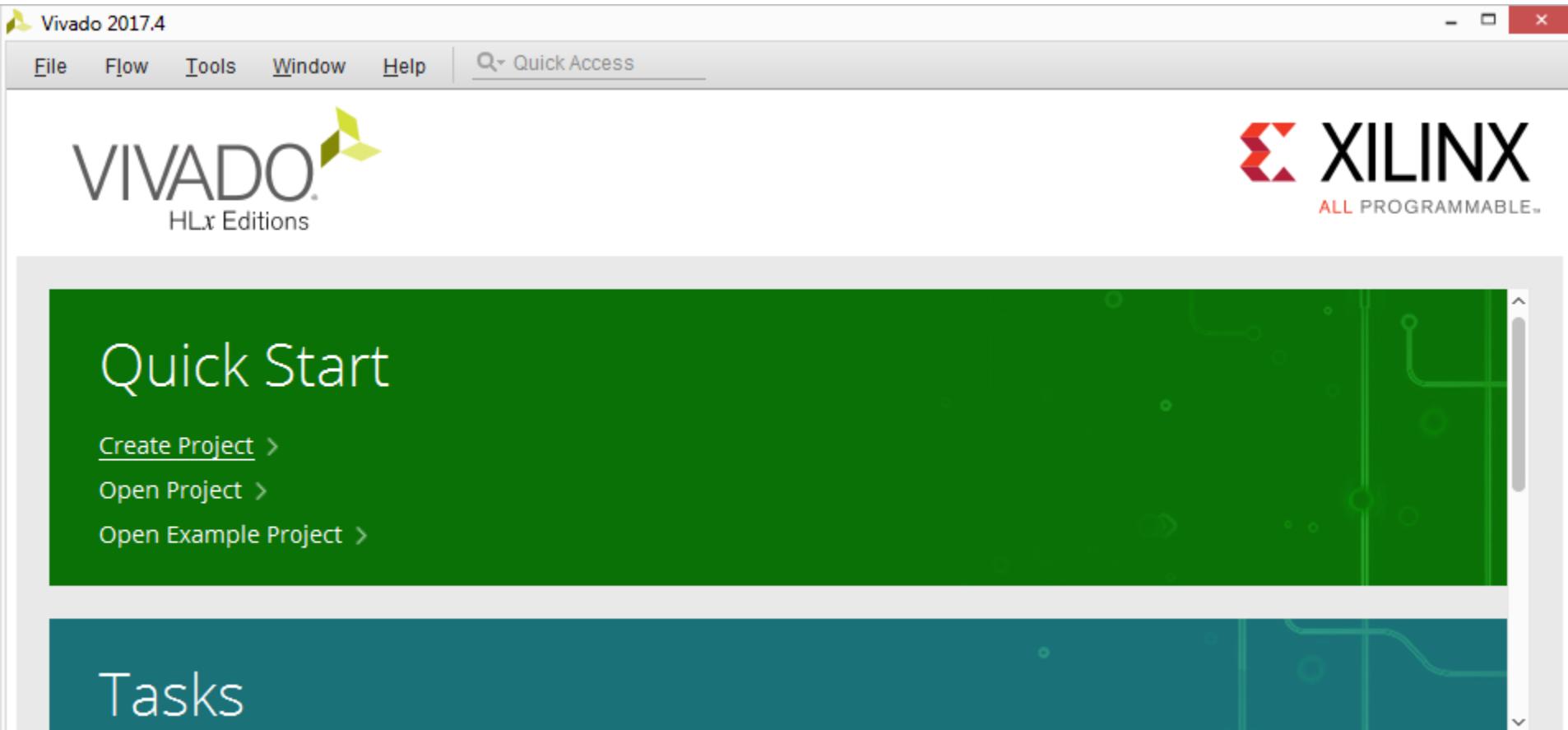
# Generate MIG RLD3 36 Bit C2 Example Design

# Generate MIG RLD3 36 Bit C2 Example Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.4 → Vivado

► Select Create Project



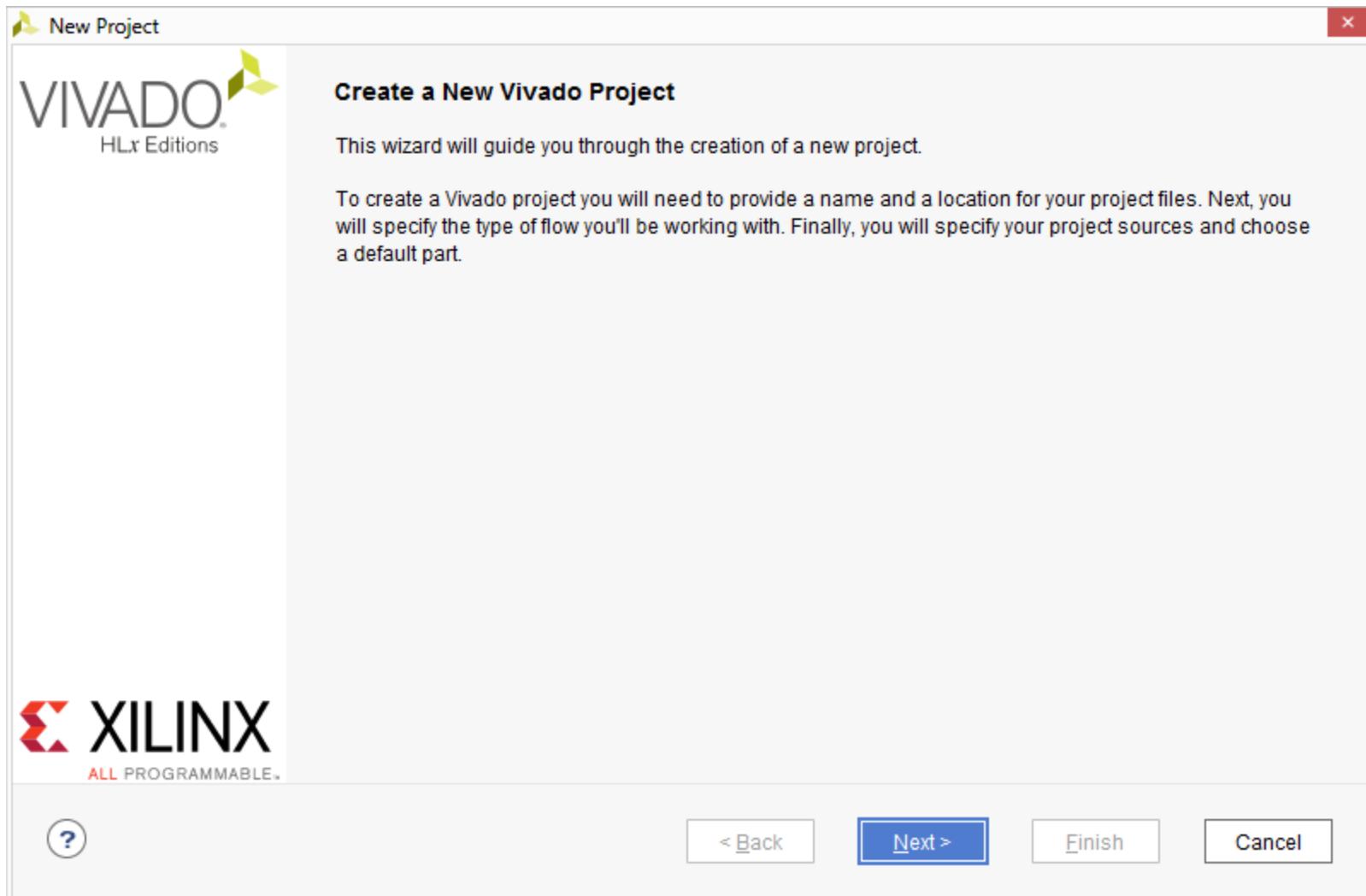
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the VCU108

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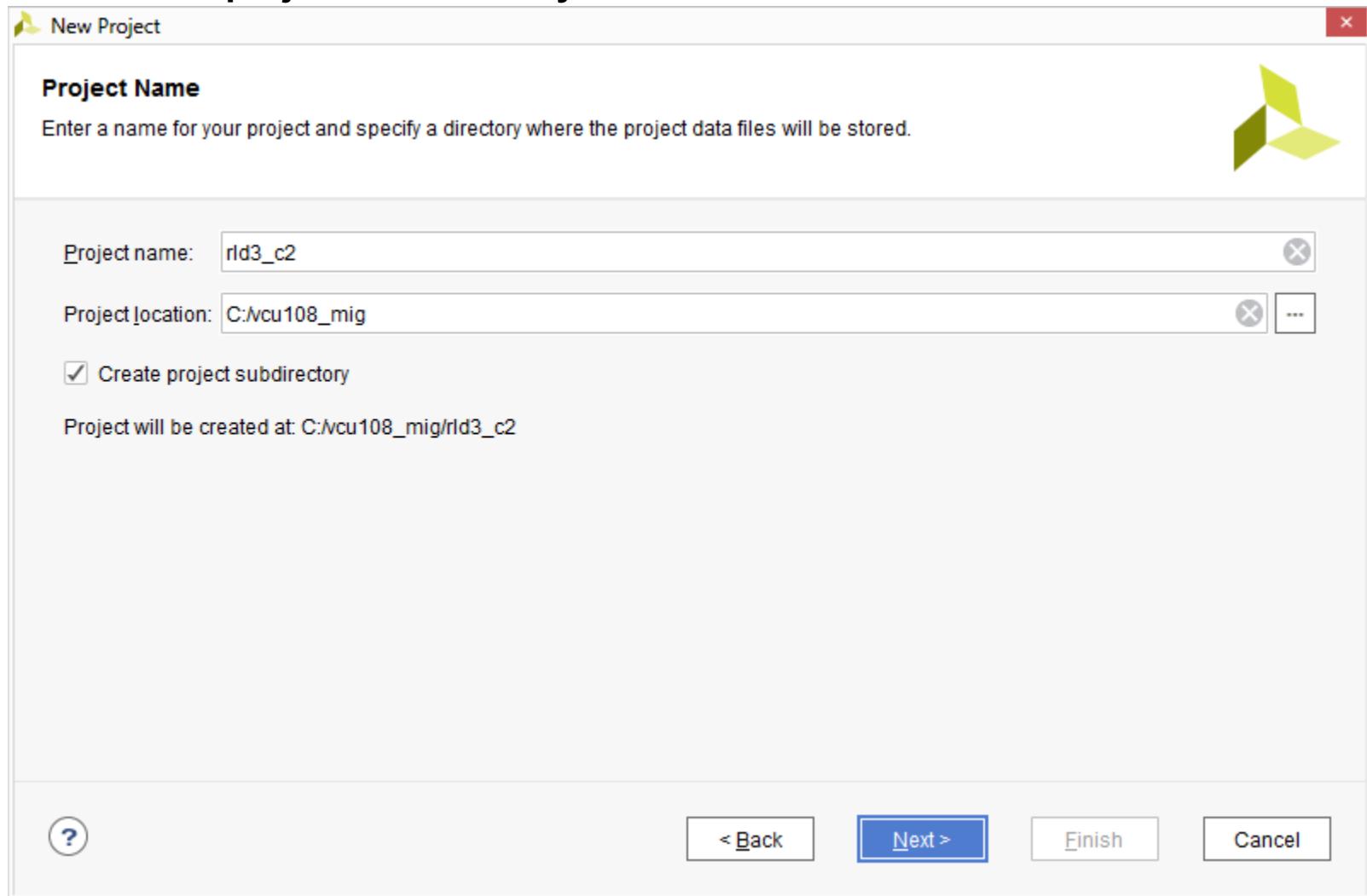
# Generate MIG RLD3 36 Bit C2 Example Design

► Click Next



# Generate MIG RLD3 36 Bit C2 Example Design

- Set the Project name to **rld3\_c2** and location to **C:/vcu108\_mig**
  - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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# Generate MIG RLD3 36 Bit C2 Example Design

## ► Select RTL Project

- Select **Do not specify sources at this time**

New Project

**Project Type**  
Specify the type of project to create.



RTL Project  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.  
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.  
 Do not specify sources at this time

I/O Planning Project  
Do not specify design sources. You will be able to view part/package resources.

Imported Project  
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project  
Create a new Vivado project from a predefined template.

[?](#)   [< Back](#)   [Next >](#)   [Finish](#)   [Cancel](#)

# Generate MIG RLD3 36 Bit C2 Example Design

► Under Boards, select the **VCU108 Evaluation Platform**

New Project

**Default Part**  
Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

Filter/ Preview

Vendor: All  
Display Name: All  
Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2
<b>Virtex-UltraScale VCU108 Evaluation Platform</b>	xilinx.com	1.0	<b>xcvu095-ffva2104-2-e</b>
Virtex-UltraScale VCU110 Evaluation Platform	xilinx.com	1.0	xcvu190-flac2104-2-e

No Board Connectors

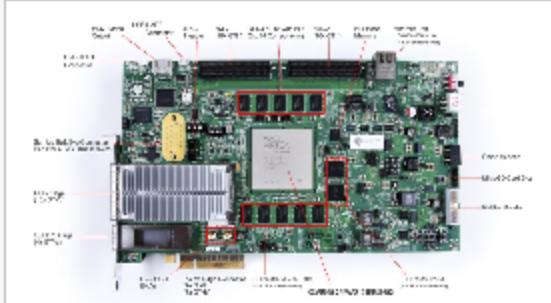
?

< Back

Next >

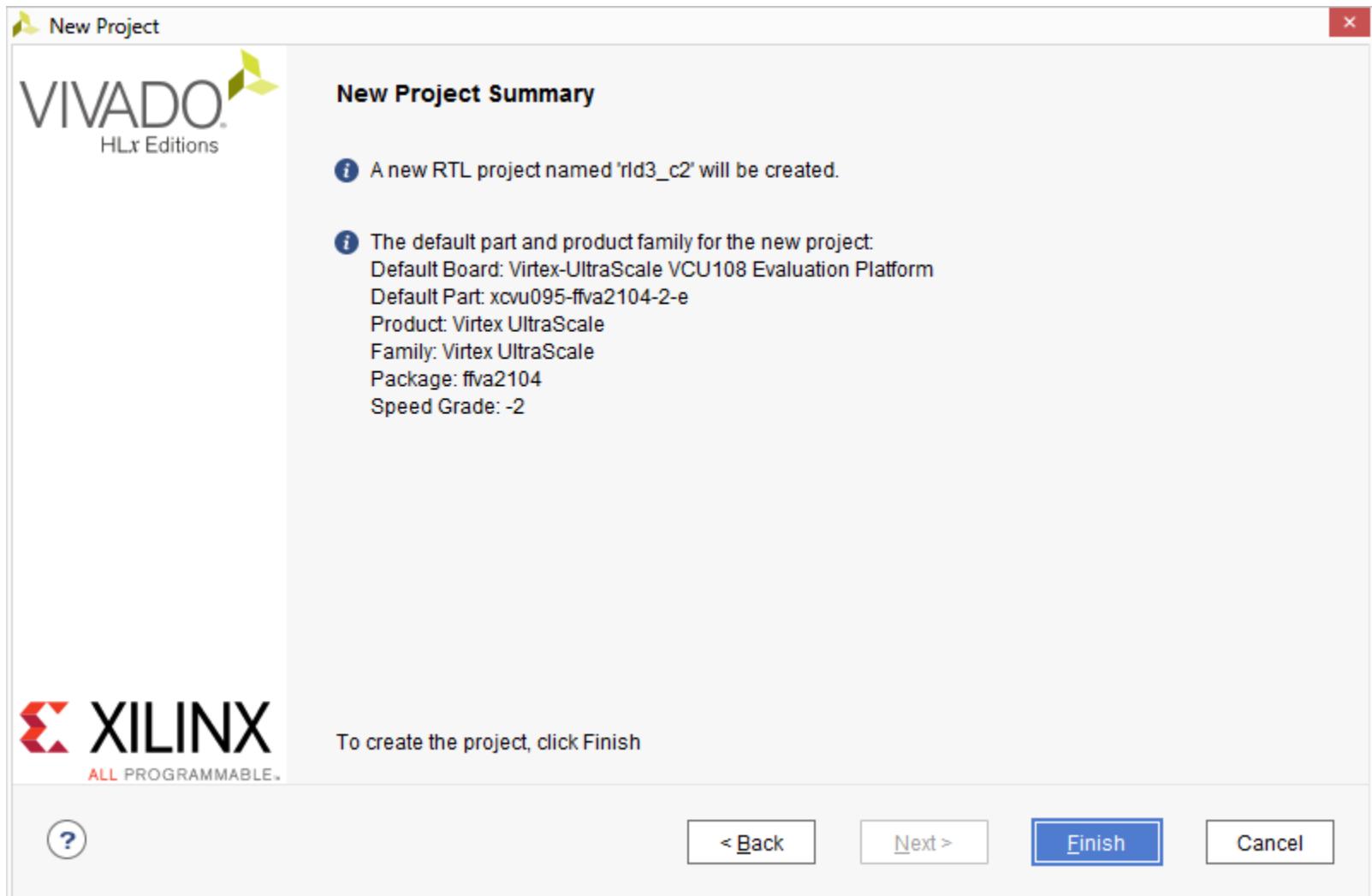
Finish

Cancel



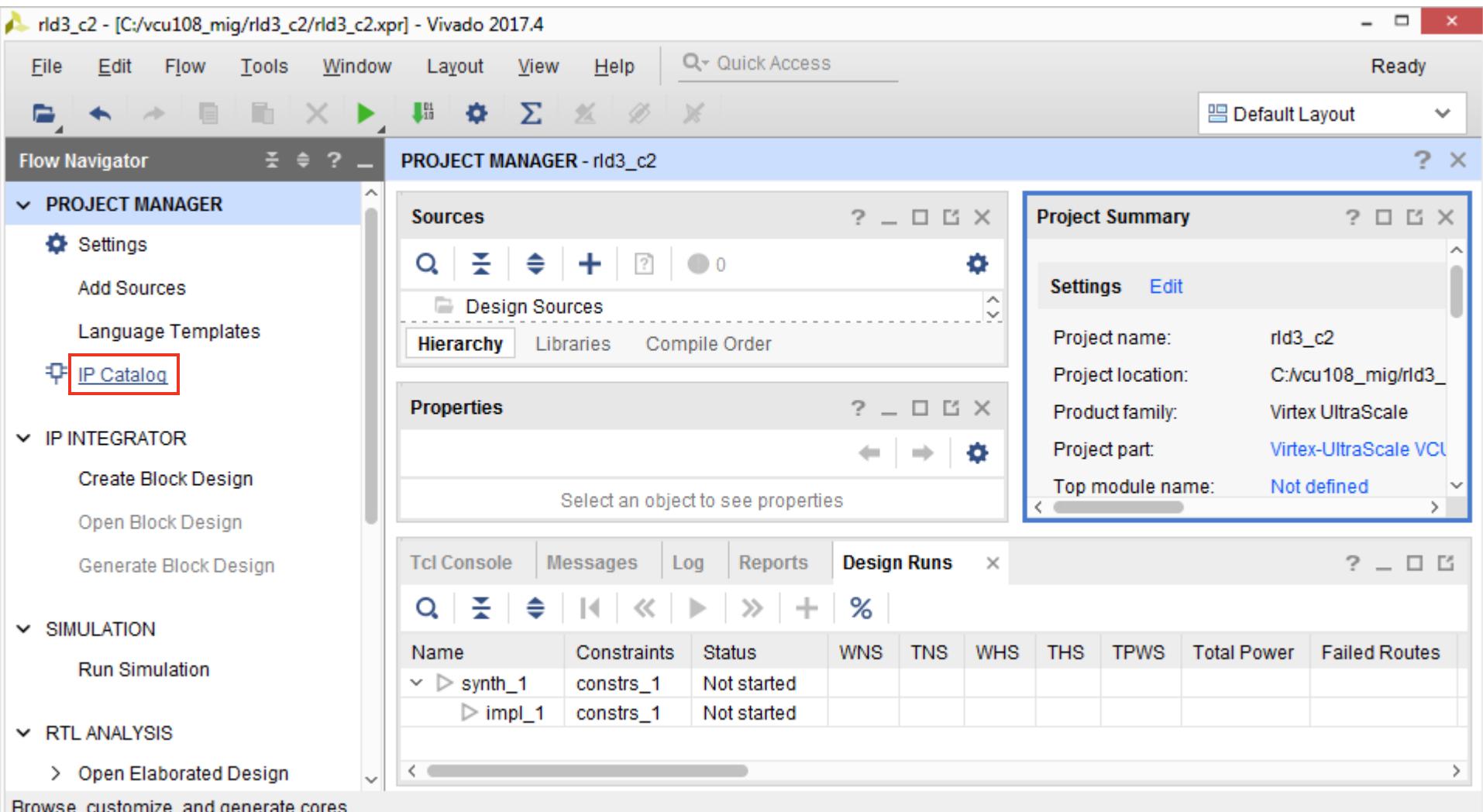
# Generate MIG RLD3 36 Bit C2 Example Design

► Click Finish



# Generate MIG RLD3 36 Bit C2 Example Design

► Click on IP Catalog



# Generate MIG RLD3 36 Bit C2 Example Design

## ► Select RLDRAM3 (MIG), v1.4

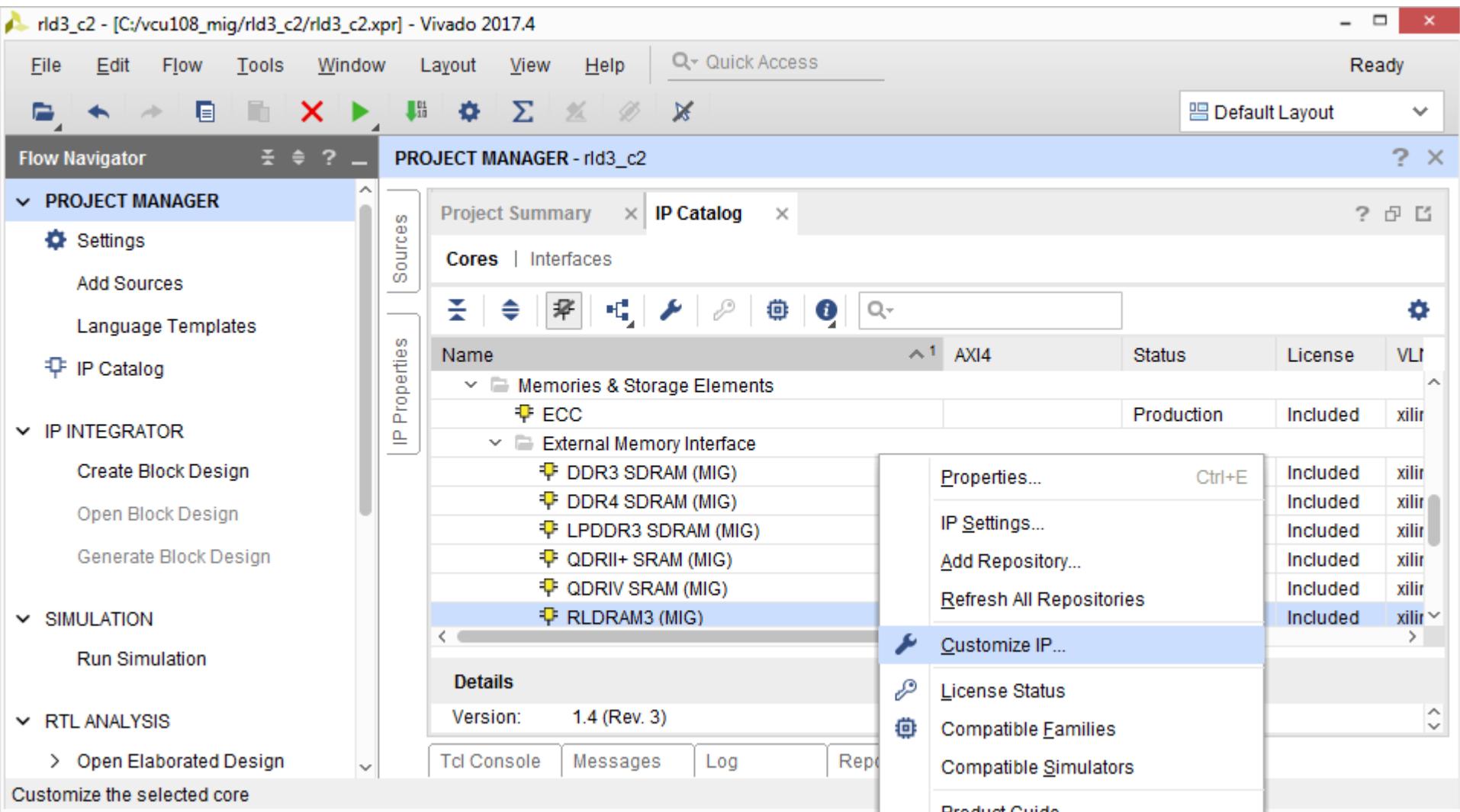
The screenshot shows the Vivado 2017.4 interface with the project "rld3\_c2" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The IP Catalog section is currently active, displaying the IP Catalog tab with the "Cores" tab selected. The catalog lists various memory components under "Memories & Storage Elements", including ECC, External Memory Interface, DDR3 SDRAM (MIG), DDR4 SDRAM (MIG), LPDDR3 SDRAM (MIG), QDRII+ SRAM (MIG), QDRIV SRAM (MIG), and RLDRAM3 (MIG). The RLDRAM3 (MIG) entry is highlighted with a blue selection bar. Below the catalog, a "Details" panel shows the version as "1.4 (Rev. 3)". The bottom navigation bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

Name	AXI4	Status	License	VLI
ECC		Production	Included	xilinx
External Memory Interface				
DDR3 SDRAM (MIG)	AXI4	Production	Included	xilinx
DDR4 SDRAM (MIG)	AXI4	Production	Included	xilinx
LPDDR3 SDRAM (MIG)		Pre-Production	Included	xilinx
QDRII+ SRAM (MIG)		Production	Included	xilinx
QDRIV SRAM (MIG)		Production	Included	xilinx
<b>RLDRAM3 (MIG)</b>		Production	Included	xilinx

# Generate MIG RLD3 36 Bit C2 Example Design

► Right click on **RLDRAM3 (MIG)**

- Select **Customize IP**

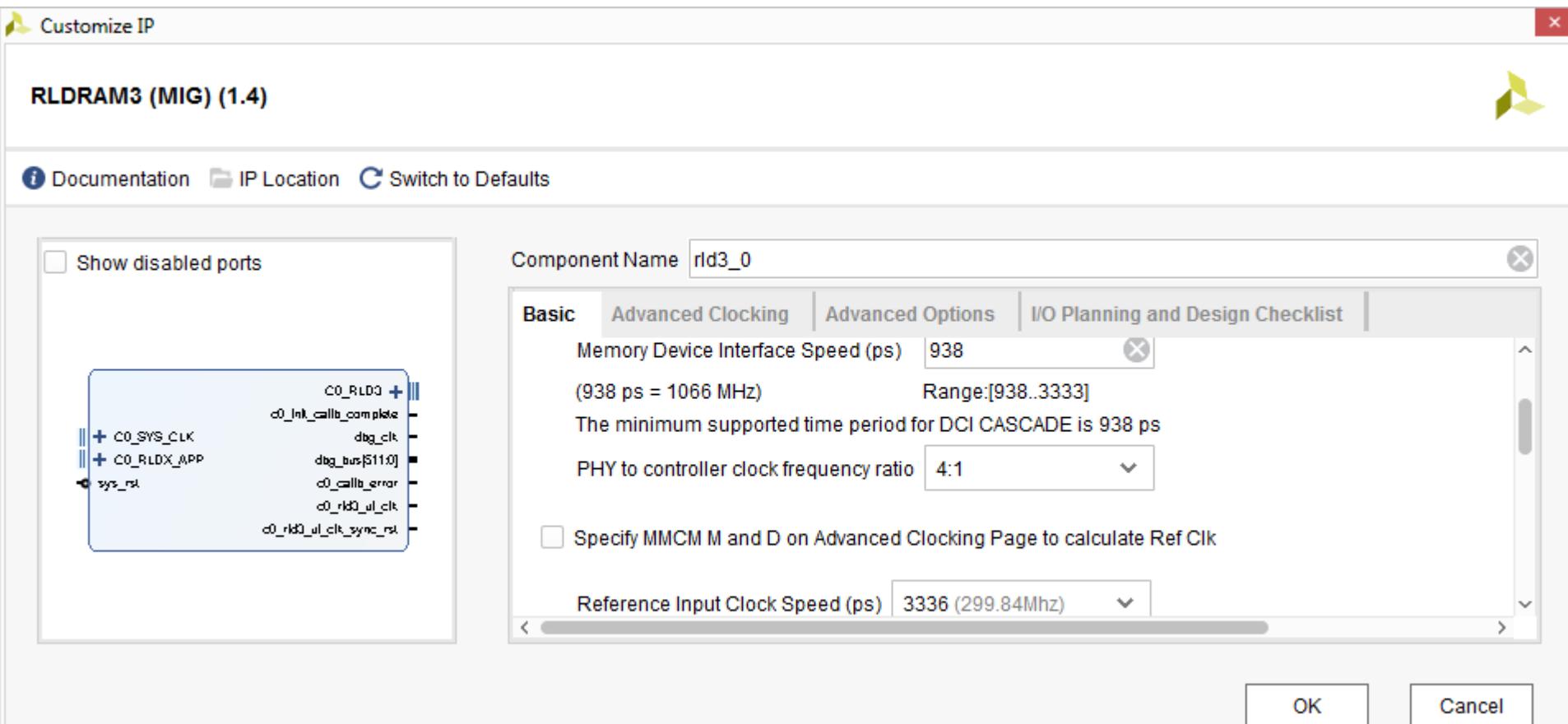


Note: Presentation applies to the VCU108

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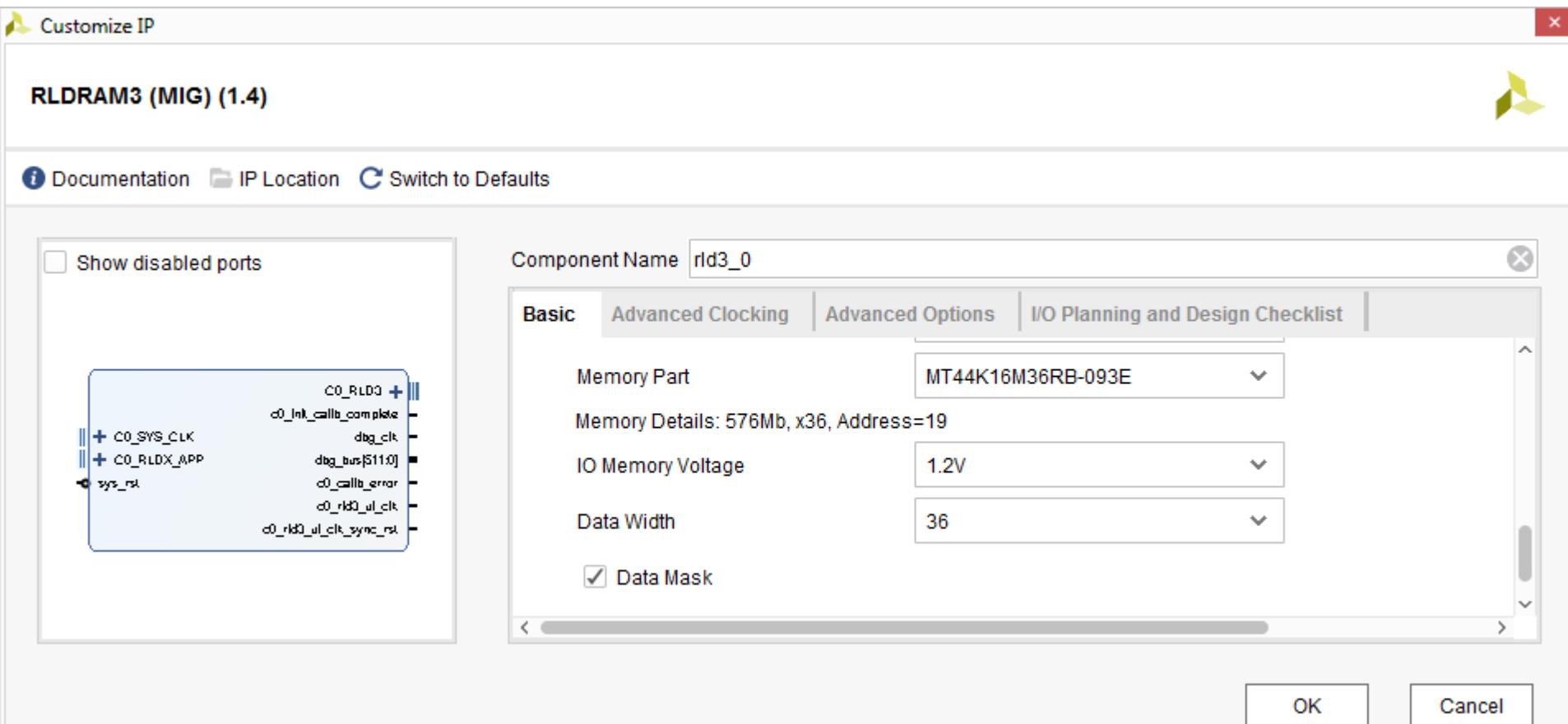
# Generate MIG RLD3 36 Bit C2 Example Design

- Set Clock period to **938** for 2128 Mb/s operation.
- Set the Input Clock to **3336** ps for 300 MHz
- Scroll down



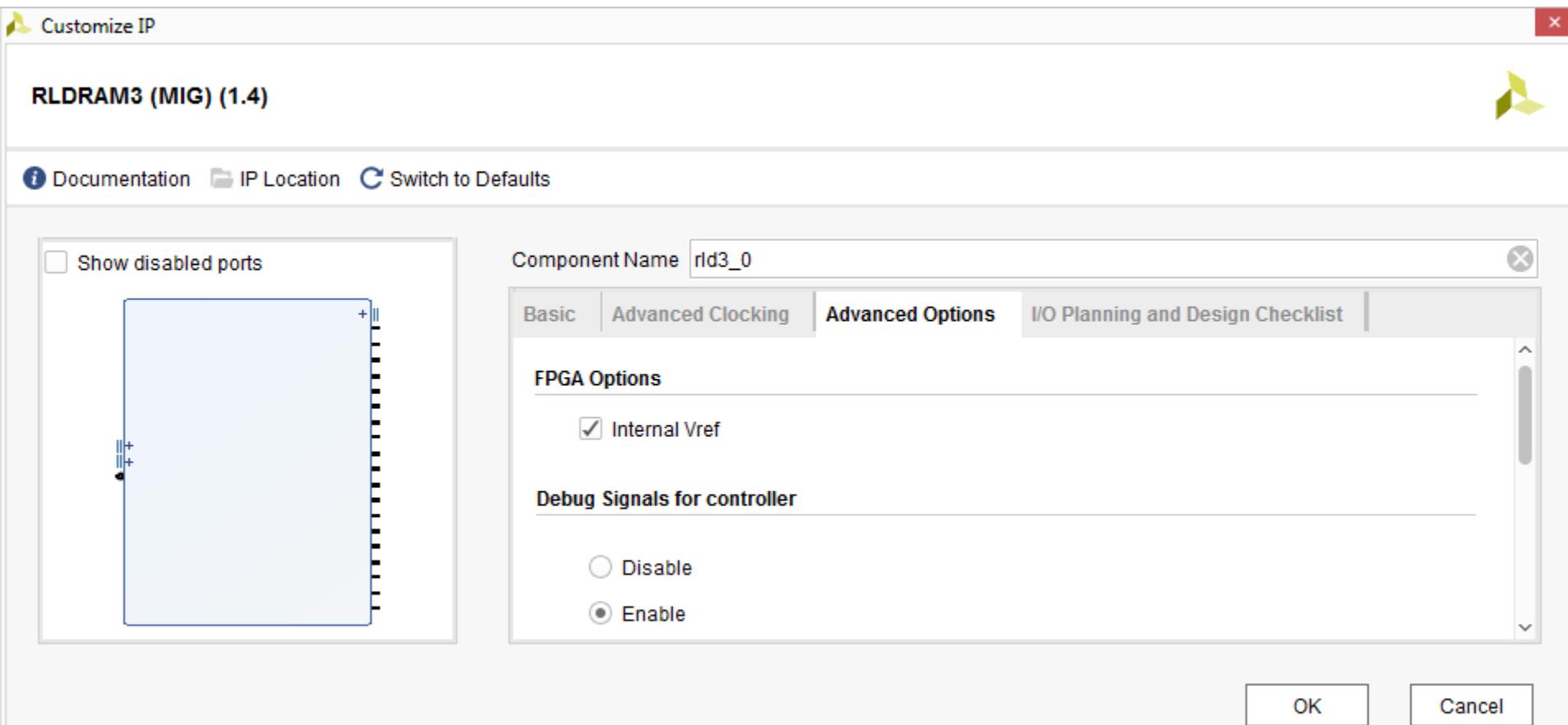
# Generate MIG RLD3 36 Bit C2 Example Design

- Select the part **MT44K16M36RB\_093E**
- Set the Data Width to **36** and click the **Advanced Options** Tab



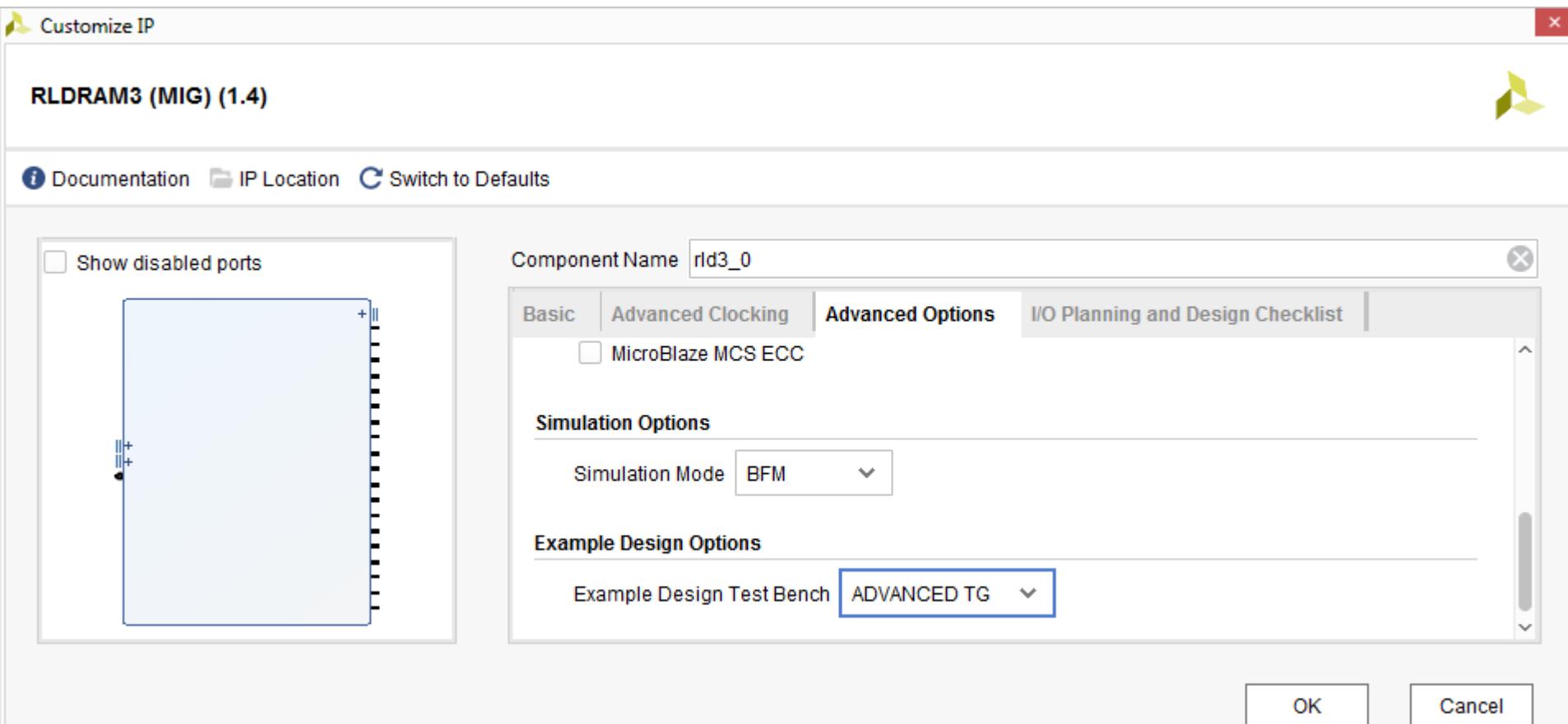
# Generate MIG RLD3 36 Bit C2 Example Design

- Set the Debug Signals to **Enable**
- Scroll down



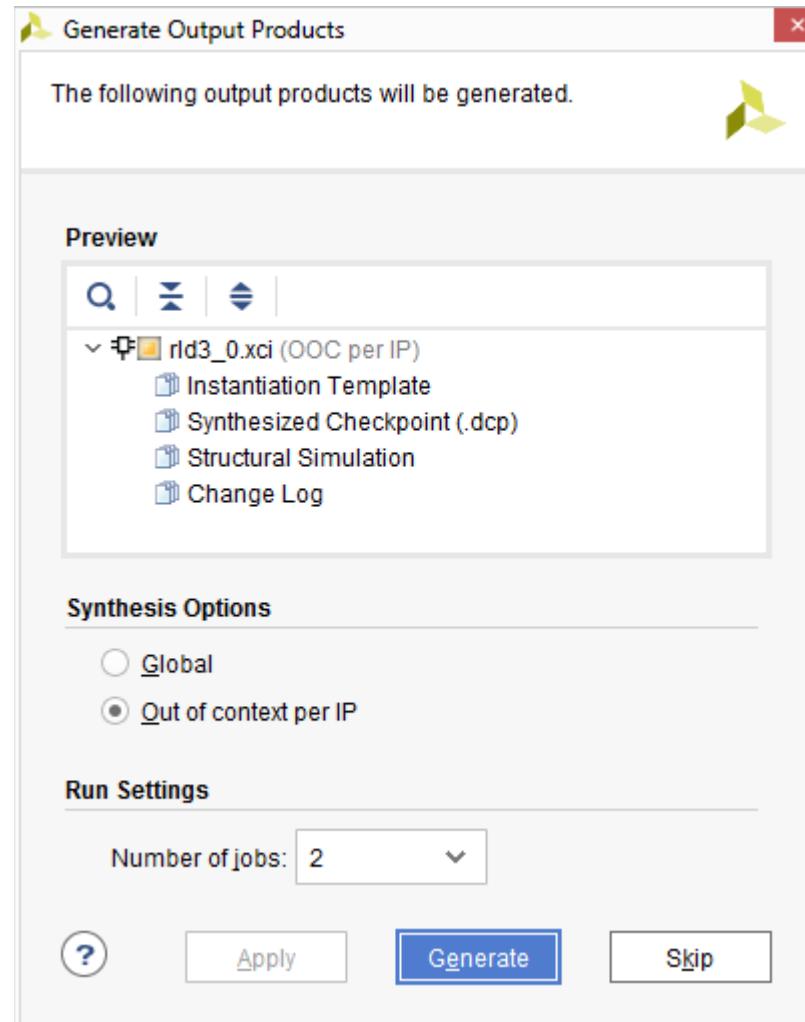
# Generate MIG RLD3 36 Bit C2 Example Design

- Select ADVANCED TG
- Click OK



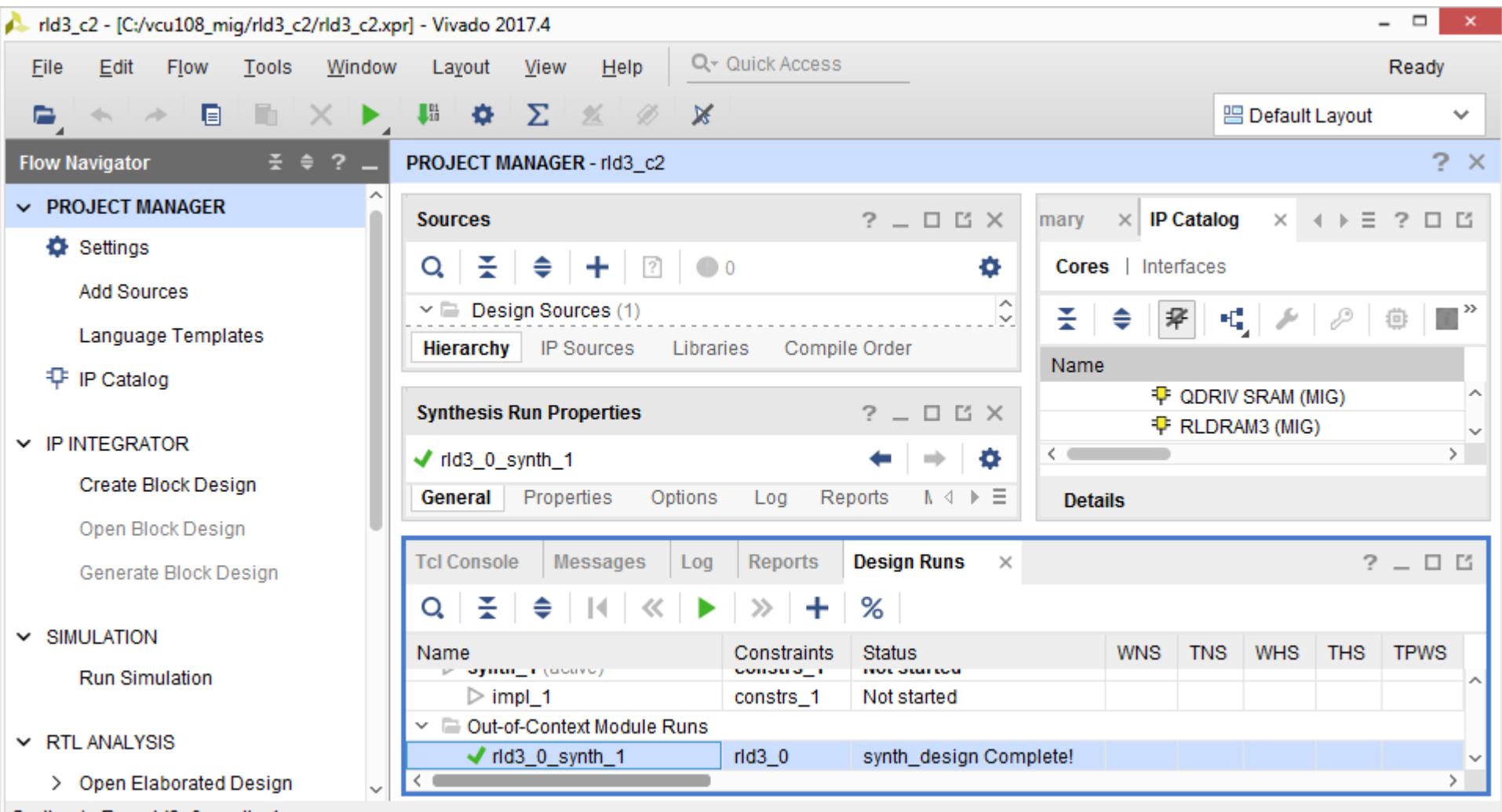
# Generate MIG RLD3 36 Bit C2 Example Design

► Click Generate



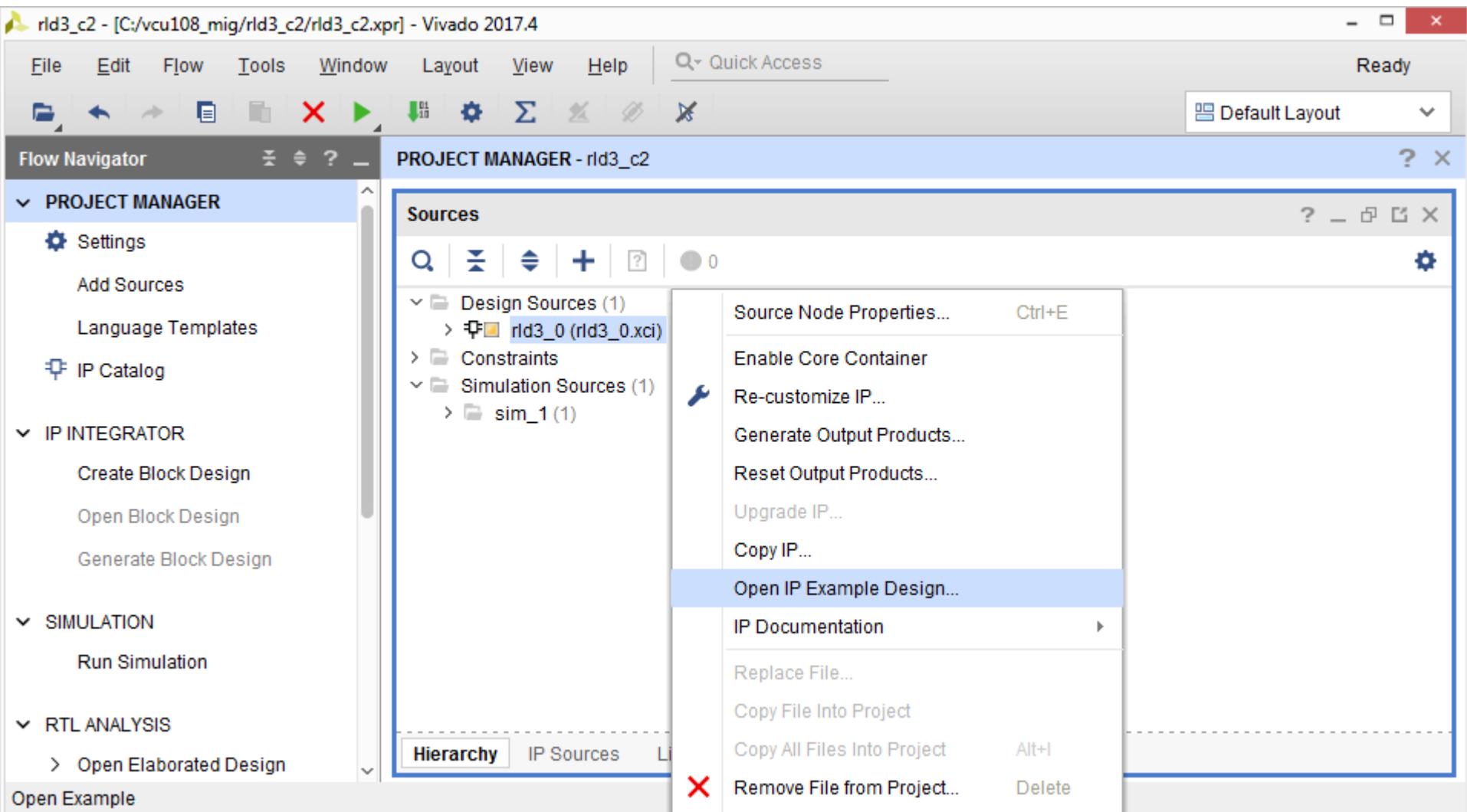
# Generate MIG RLD3 36 Bit C2 Example Design

► Wait until checkmark appears on **rld3\_0\_synth\_1**



# Compile Example Design

► Right click on **rld3\_0** and select **Open IP Example Design...**

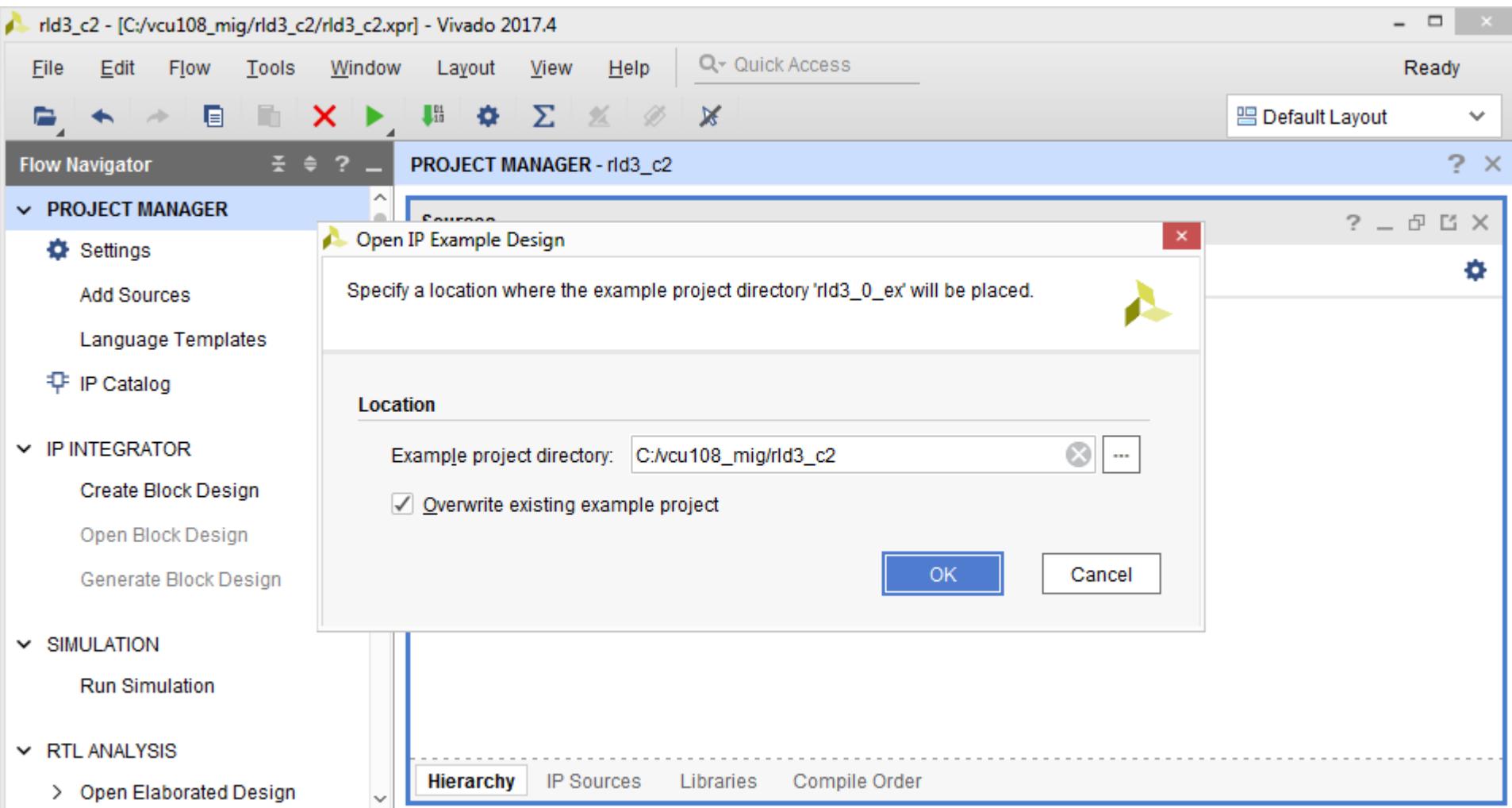


Note: Presentation applies to the VCU108

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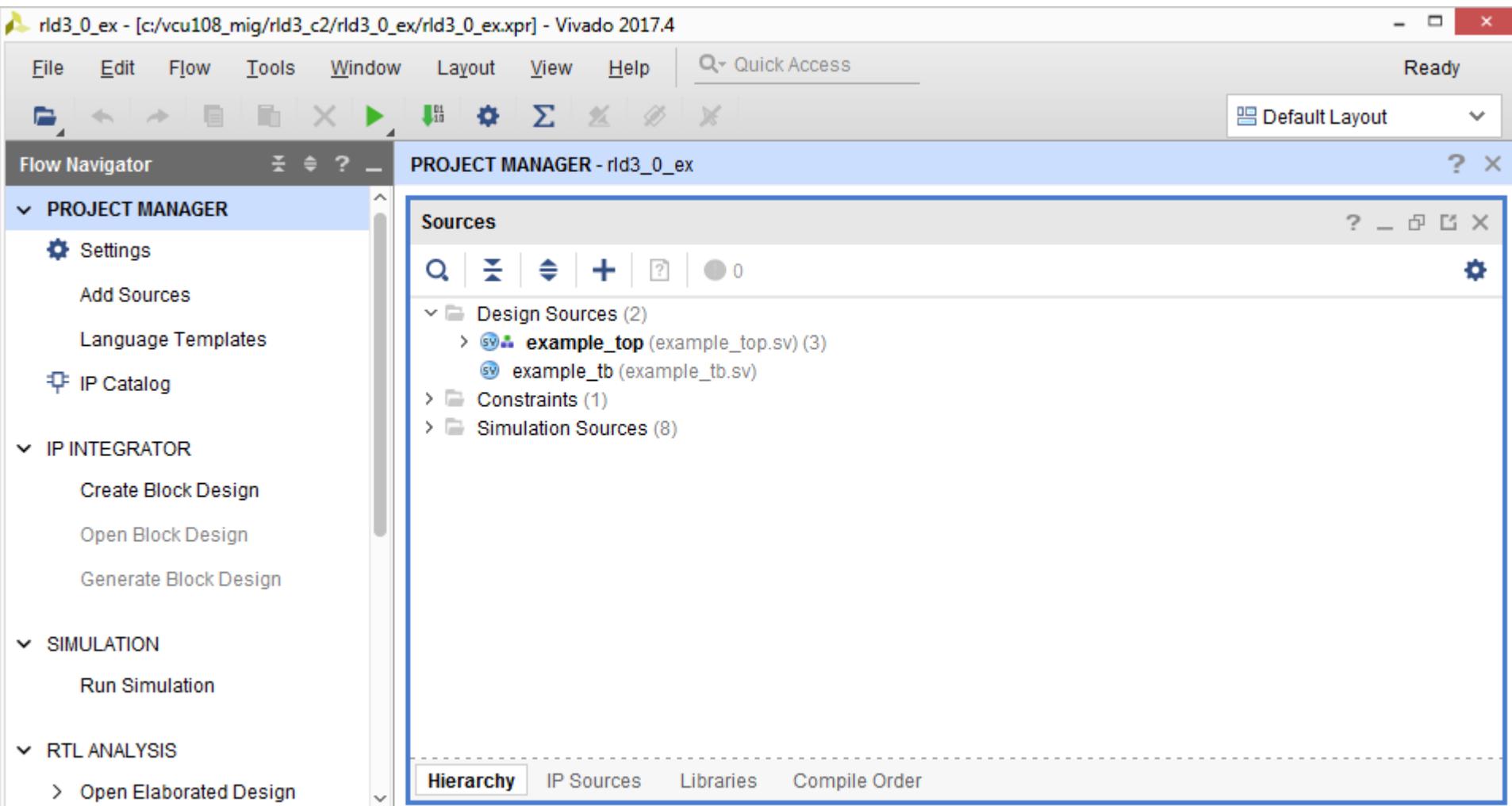
# Compile Example Design

► Set the location to **C:/vcu108\_mig/rld3\_c2** and click **OK**



# Compile Example Design

► A new project is created under <design path>/



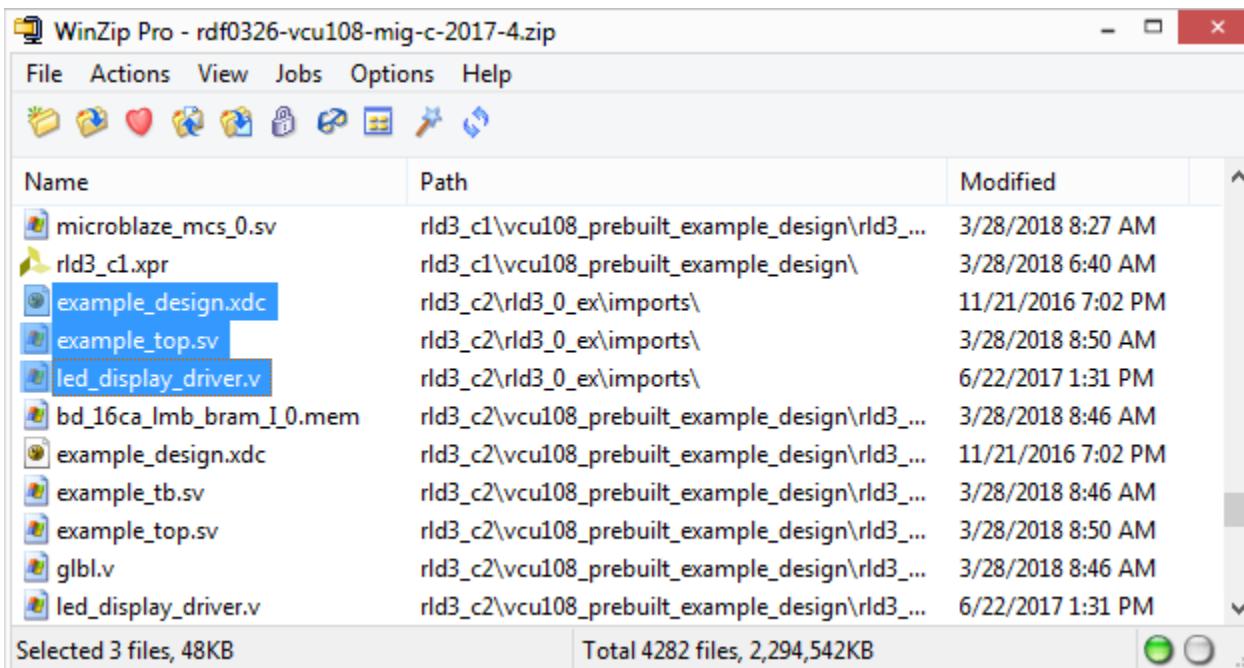
Note: The original project window can be closed

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# Modifications to Example Design

## ► From the RDF0326 - VCU108 MIG Design Files (2017.4 C) ZIP file

- Extract the **rld3\_c2** files, **example\_design.xdc**, **example\_top.sv**, and **led\_display\_driver.v**
- Overwrite these three existing files in your **rld3\_c2** MIG design
- Do this **after** creating the Example Design; changes only affect the Example Design



# Modifications to Example Design

## ► Modifications to the example design

- Added RTL and XDC modifications to drive LEDs and AR66800
- The following commands will add the led\_display\_driver.v and create the required VIO IP
- From the Tcl Console, run these commands:

```
add_files -norecurse
```

```
C:/vcu108_mig/rld3_c2/rld3_0_ex/imports/led_display_driver.v
```

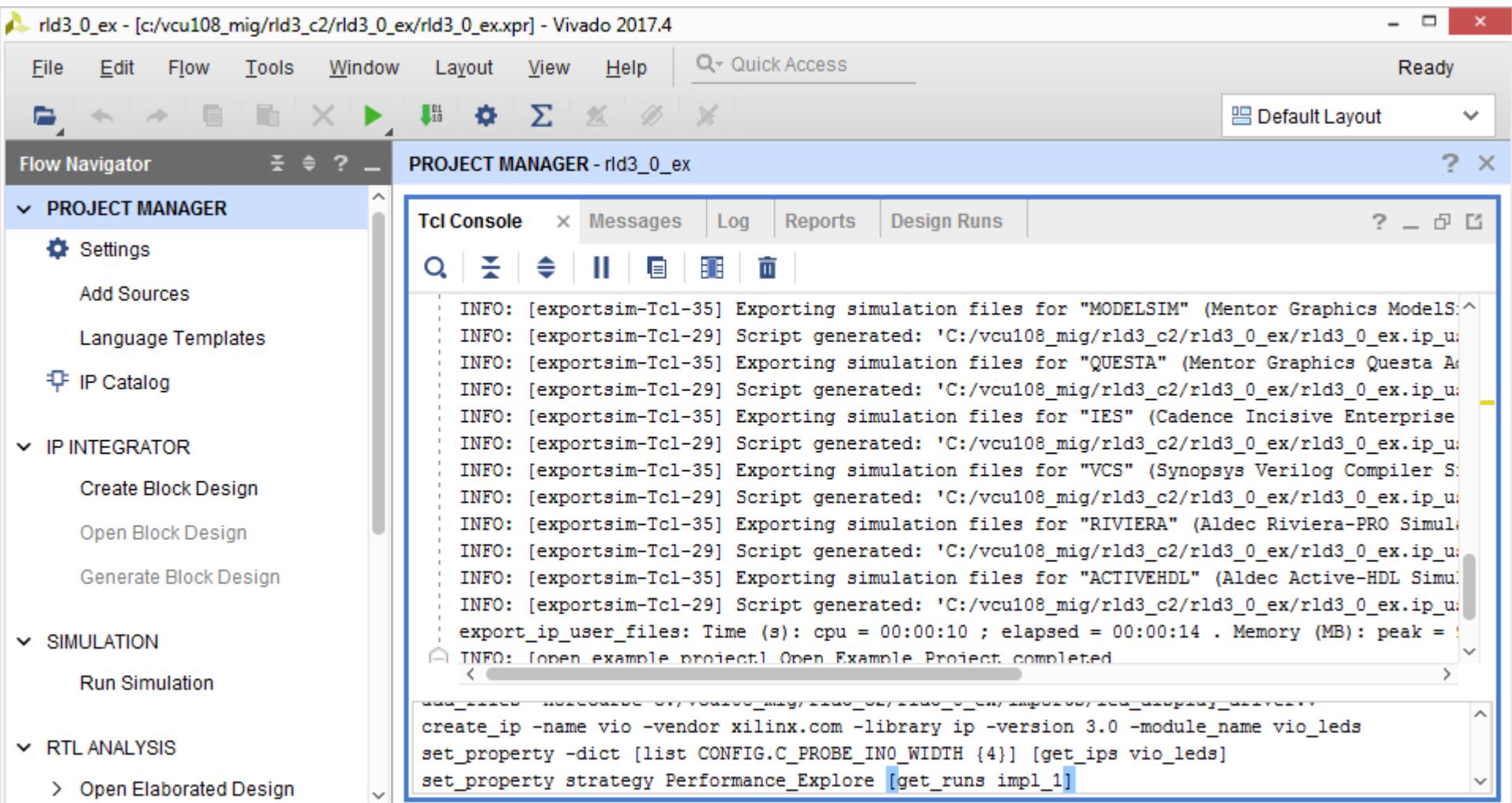
```
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name  
vio_leds
```

```
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

```
set_property strategy Performance_Explore [get_runs impl_1]
```

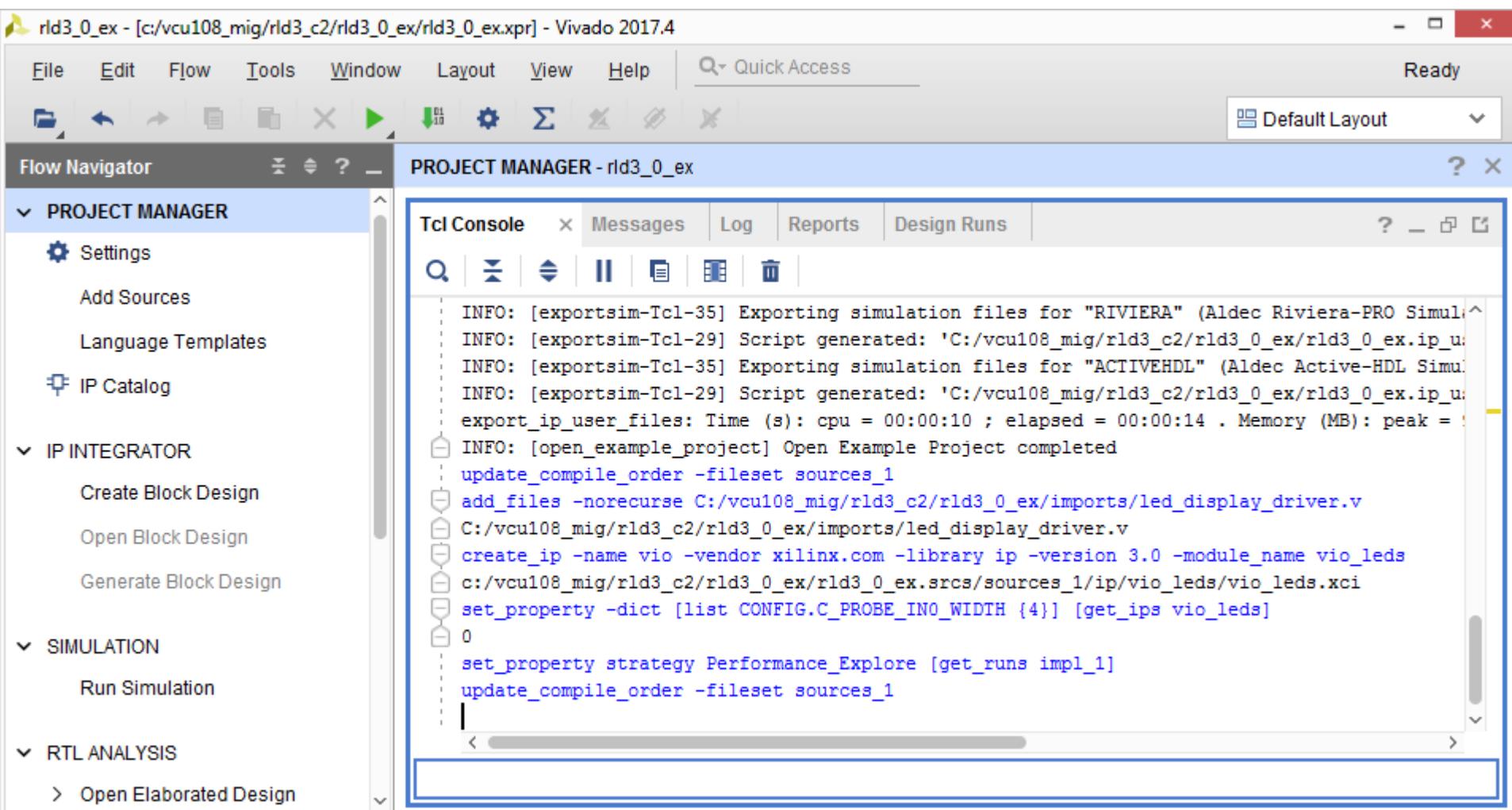
# Modifications to Example Design

► Press enter after entering Tcl commands



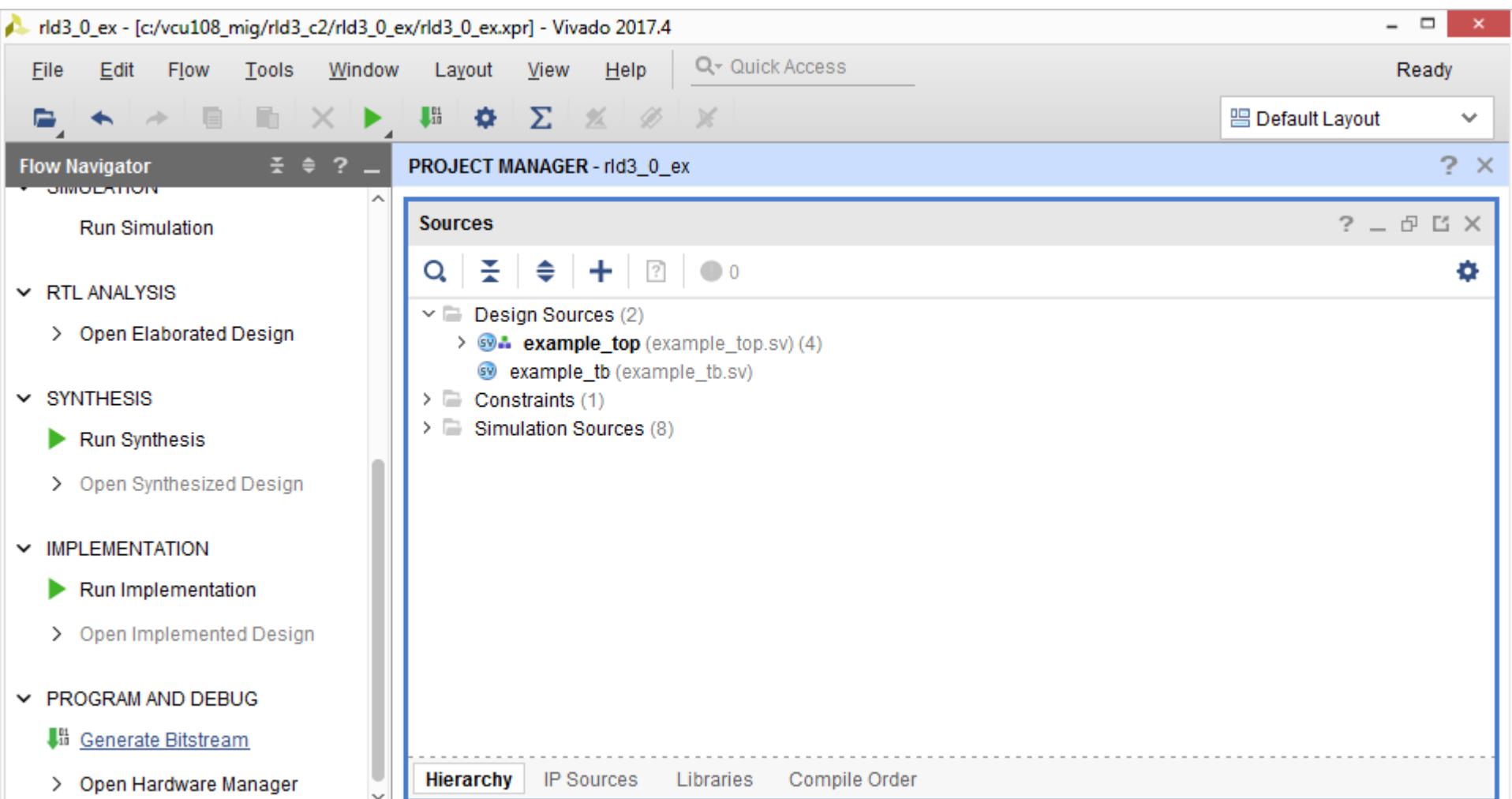
# Modifications to Example Design

► Tcl commands completed successfully



# Compile Example Design

► Click on **Generate Bitstream**



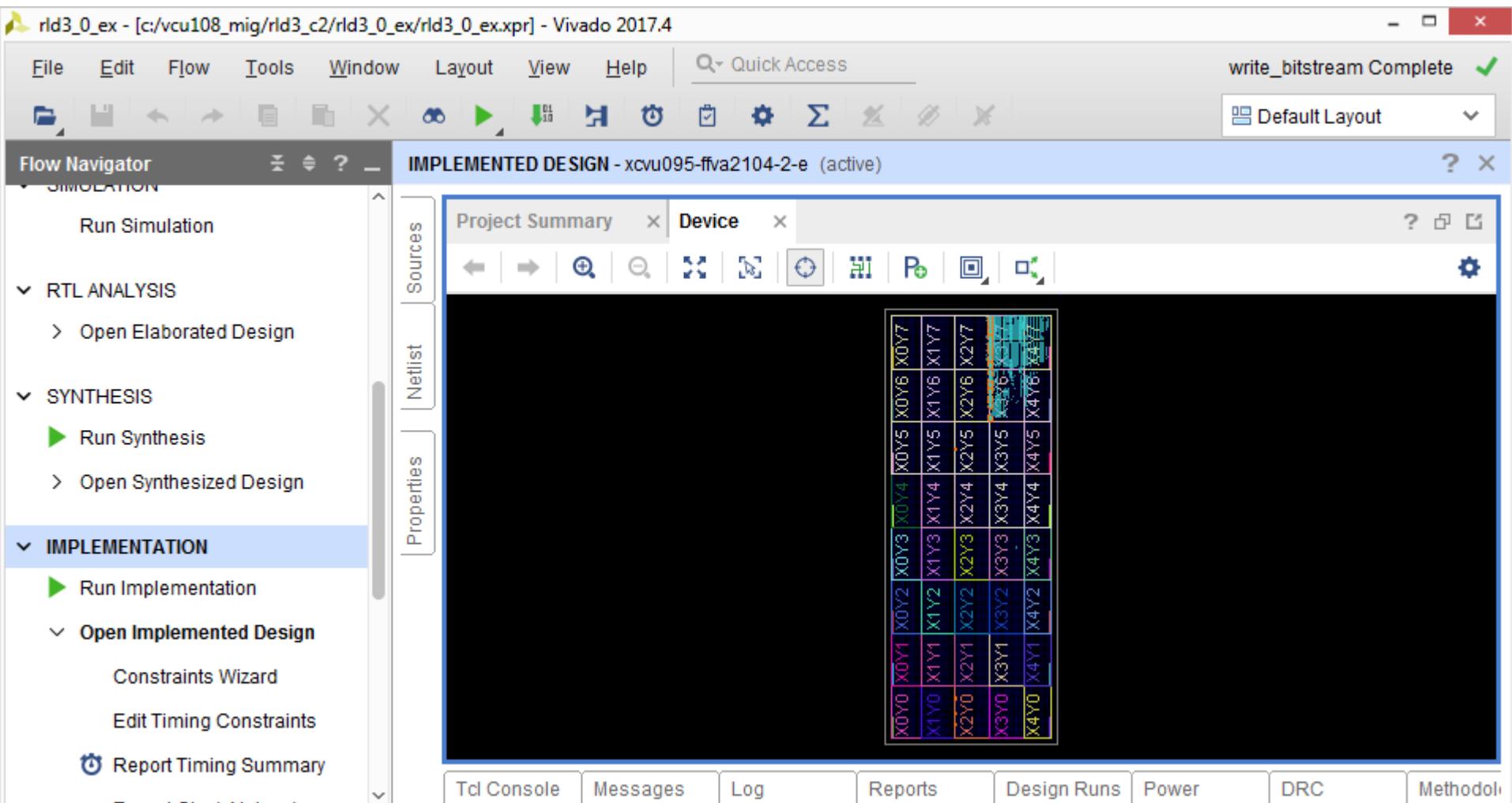
Generate a programming file after implementation

Note: Presentation applies to the VCU108

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# Compile Example Design

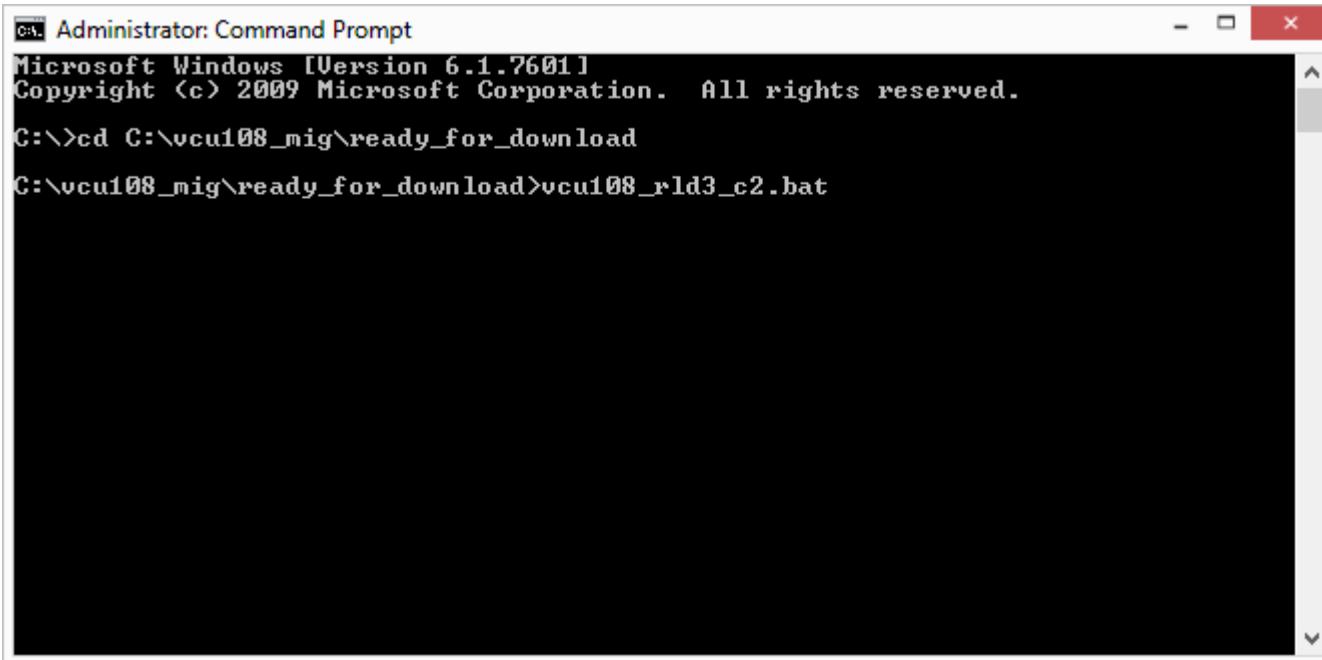
► Open and view the Implemented Design



# Run MIG Example Design

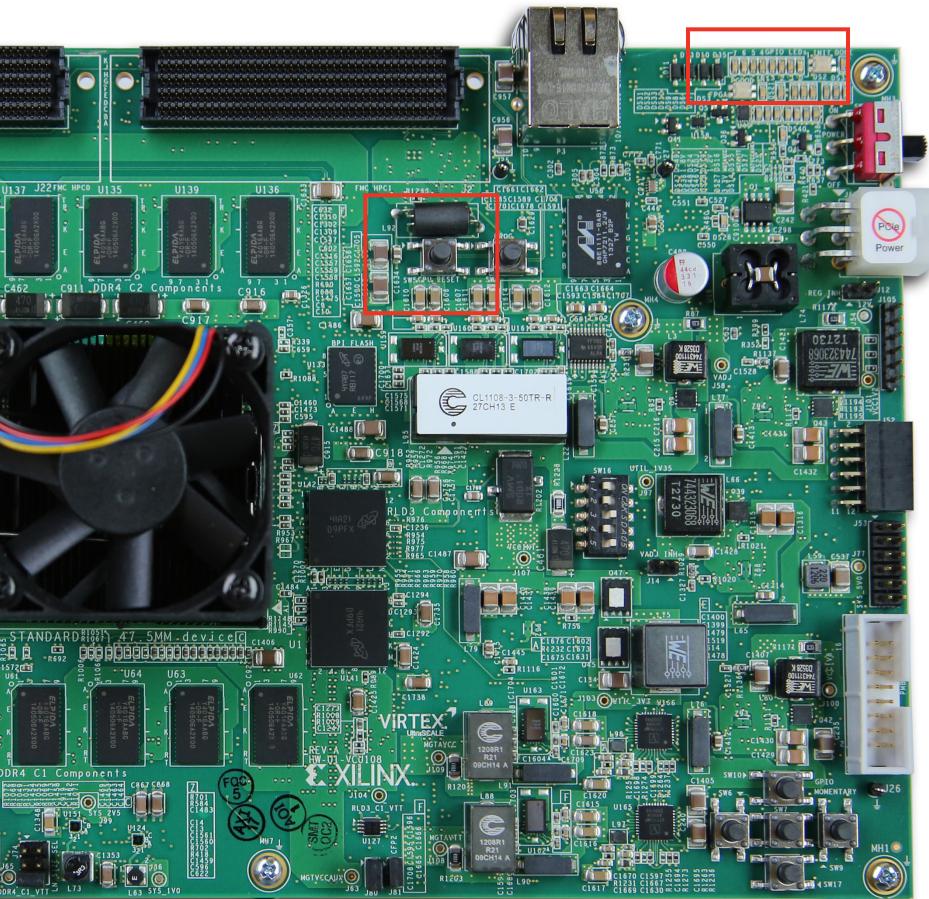
- ▶ From a Command Prompt, type:

```
cd C:\vcu108_mig\ready_for_download  
vcu108_rld3_c2.bat
```



```
C:\ Administrator: Command Prompt  
Microsoft Windows [Version 6.1.7601]  
Copyright <c> 2009 Microsoft Corporation. All rights reserved.  
  
C:>cd C:\vcu108_mig\ready_for_download  
C:\vcu108_mig\ready_for_download>vcu108_rld3_c2.bat
```

# Run MIG Example Design



- After bitstream loads, LED 0 (right most LED) will be lit, and LED1 will be blinking
- LED 3 will light and stay on
  - This indicates Calibration has completed
- If an error occurs, LED 0 will go out and LED 2 will light
  - The “CPU\_RESET” button, SW5, is the reset

# References

# References

## ➤ Virtex UltraScale Memory

- UltraScale FPGA Memory Interface Solutions Product Guide – PG150
  - [https://www.xilinx.com/support/documentation/ip\\_documentation/ultrascale\\_memory\\_ip/v1\\_4/pg150-ultrascale-memory-ip.pdf](https://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/v1_4/pg150-ultrascale-memory-ip.pdf)

## ➤ Vivado Release Notes

- Vivado Design Suite User Guide - Release Notes – UG973
  - [https://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2017\\_4/ug973-vivado-release-notes-install-license.pdf](https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug973-vivado-release-notes-install-license.pdf)
- Vivado Design Suite 2017 - Vivado Known Issues
  - <https://www.xilinx.com/support/answers/68923.html>

## ➤ Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [https://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2017\\_4/ug908-vivado-programming-debugging.pdf](https://www.xilinx.com/support/documentation/sw_manuals/xilinx2017_4/ug908-vivado-programming-debugging.pdf)

# Documentation

# Documentation

## ➤ Virtex UltraScale

- Virtex UltraScale FPGA Family
  - <https://www.xilinx.com/products/silicon-devices/fpga/virtex-ultrascale.html>

## ➤ VCU108 Documentation

- Virtex UltraScale FPGA VCU108 Evaluation Kit
  - <https://www.xilinx.com/products/boards-and-kits/ek-u1-vcu108-g.html>
- VCU108 User Guide – UG1066
  - [https://www.xilinx.com/support/documentation/boards\\_and\\_kits/vcu108/ug1066-vcu108-eval-bd.pdf](https://www.xilinx.com/support/documentation/boards_and_kits/vcu108/ug1066-vcu108-eval-bd.pdf)
- VCU108 Evaluation Kit Quick Start Guide User Guide – XTP400
  - [https://www.xilinx.com/support/documentation/boards\\_and\\_kits/vcu108/xtp400-vcu108-quickstart.pdf](https://www.xilinx.com/support/documentation/boards_and_kits/vcu108/xtp400-vcu108-quickstart.pdf)
- VCU108 - Known Issues Master Answer Record
  - <https://www.xilinx.com/support/answers/62603.html>