HLS Project 2

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1 RTL

We run RTL on Catapult.

Report: General

Solution	Latency...	Latency...	Throug...	Throug...	Total Area	Slack
wave_sort<6>.v1 (extract)	224	448.00	228	456.00	846.27	0.67

Figure 1: Table after RTL

1.1 Shedule

The images for shedule of "bubble 1","bubble 2" and "wave sort" loops are presented below.

Bubble 1

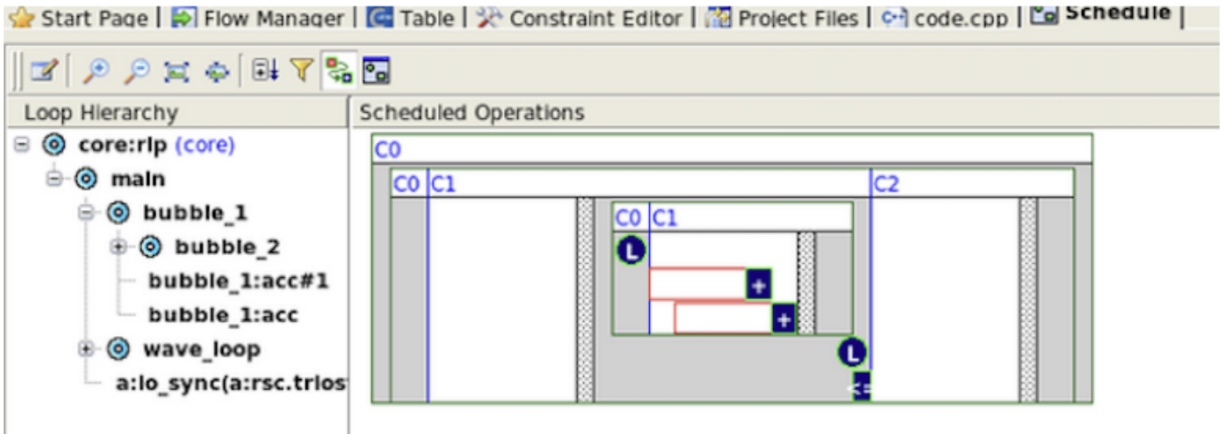

Figure 2: Shedule for "bubble 1" loop.

Bubble 2

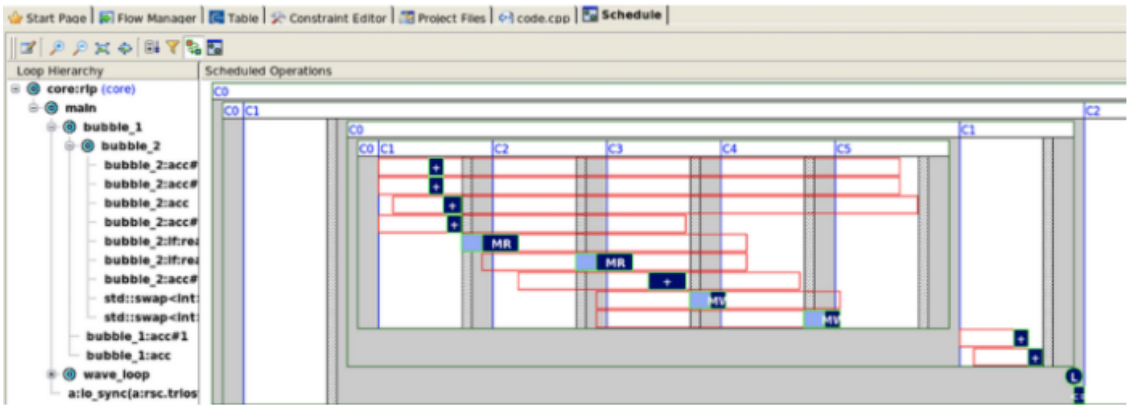

Figure 3: Shedule for "bubble 2" loop.

Wave sort

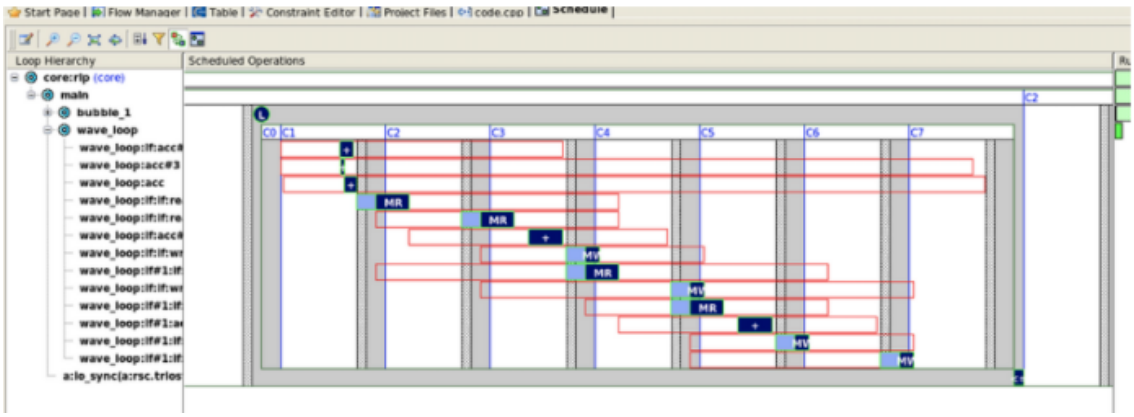

Figure 4: Shedule for "wave sort " loop.

2 RTL Loop Unroll

We run RTL after loop unroll.The modifications are shown in more detail in the image below.

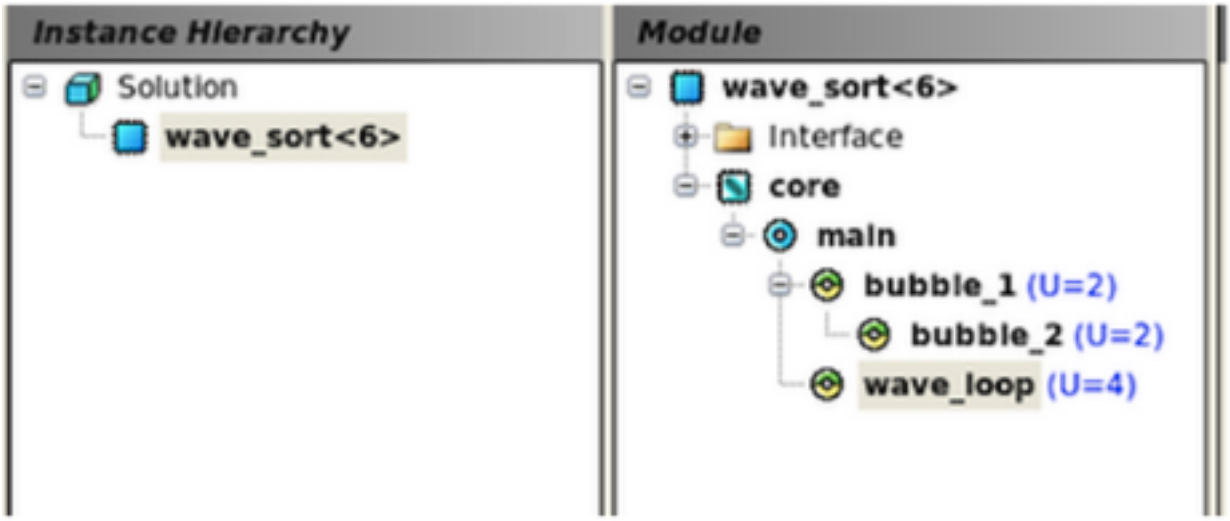

Figure 5: Loop Unroll

wave_sort<6>.v1 (extract)	224	448.00	228	456.00	850.29	0.66
wave_sort<6>.v2 (extract)	174	348.00	177	354.00	1944.59	0.58

Figure 6: Table for loop unroll

2.1 Shedule

Bubble 1

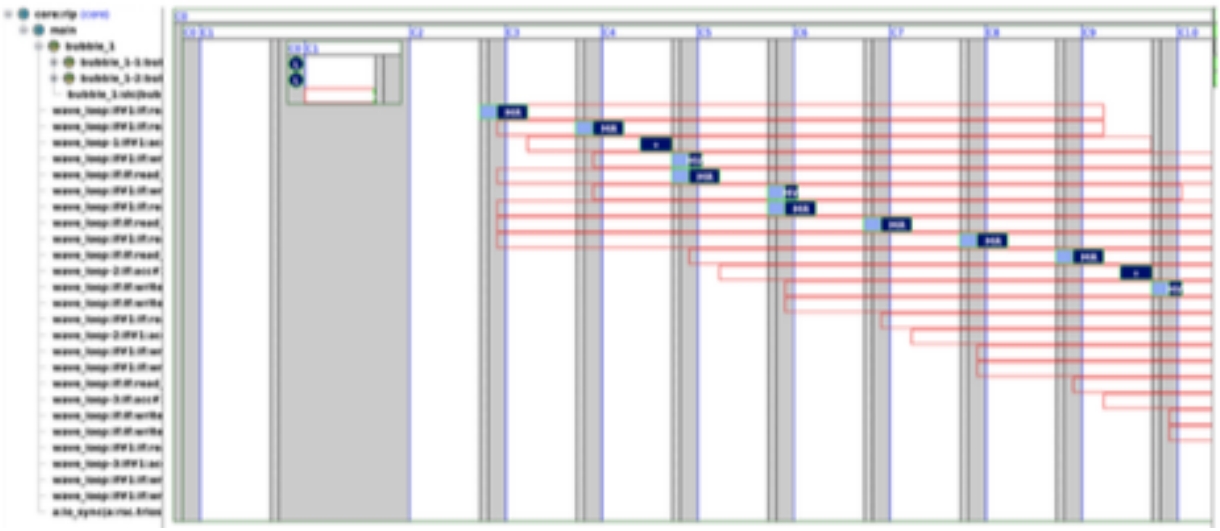

Figure 7: Shedule for "bubble 1" unrolled loop.

Bubble 2

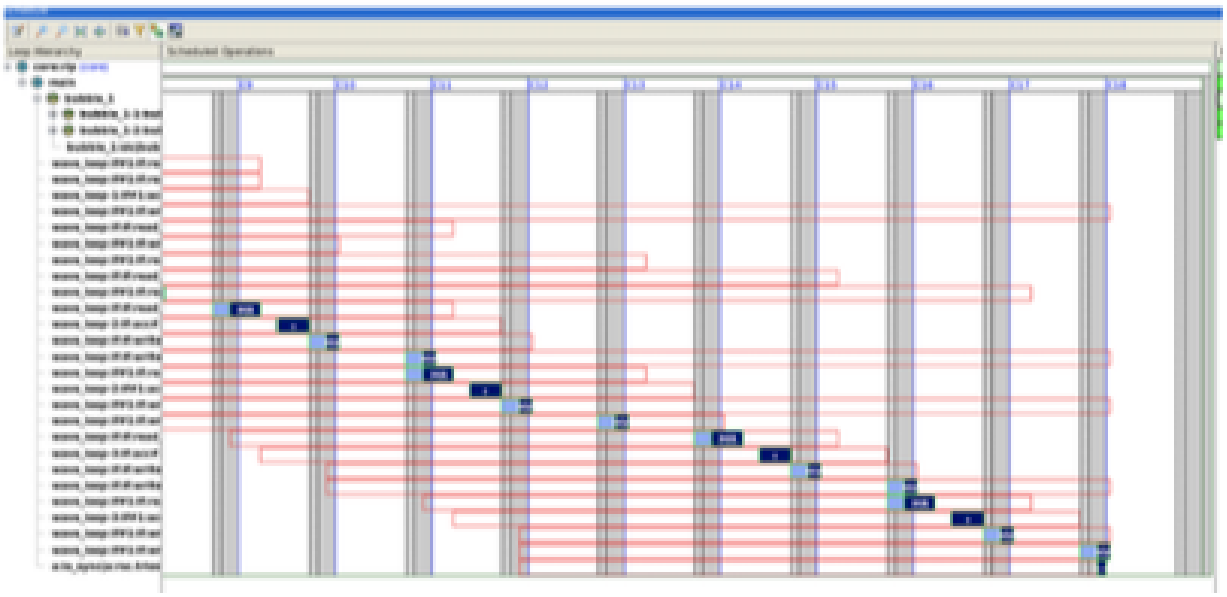

Figure 8: Shedule for "bubble 2" unrolled loop.

3 Questa Sim

We created a testbench in main function to make sure our final circuit is correct.This way we can monitor the correct mapping of the circuit's inputs to outputs.

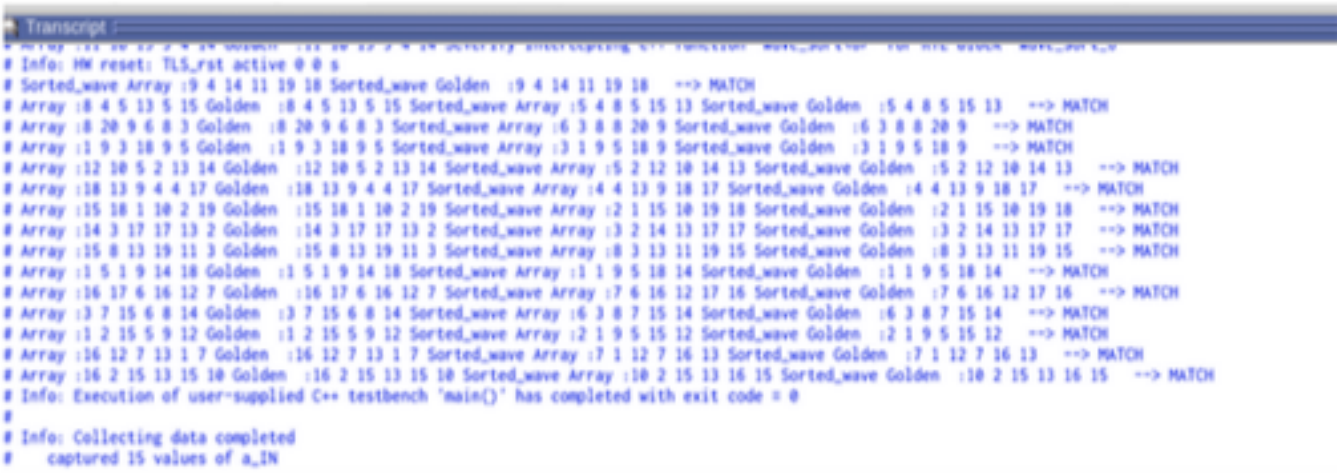

Figure 9: Co-simulation on Questa Sim