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EDUCATION

Ph.D., Engineering Applied Science, University of California Davis, Davis, CA (1988)
M.S., Engineering Applied Science, University of California Davis, Davis, CA (1984)
B.E.E., Electrical Engineering, *magna cum laude*, University of Dayton, Dayton, OH (1981)

PROFESSIONAL STATEMENT

U.S. patent agent, associate professor of electrical and computer engineering, inventor, and researcher. Over thirty years experience working with start-up companies, multinational corporations, government laboratories, and academia. More than fifteen years experience as an educator. Awarded 62 U.S. patents for inventions in microfabrication, microstructures, and semiconductor devices. Authored and co-authored more than 70 peer-reviewed research papers. Areas of technical expertise include: integrated circuit design, RF electronics, semiconductor materials, micro- and nano-electronic devices, microfabrication and process integration.

EMPLOYMENT

Blue Hill Innovation LLC, Orono, ME (2010 –)
Patent Agent (USPTO Registration #72,338) and **Engineer/Scientist**
University of Maine, Orono, ME (Sept 1999 –)
Associate Professor, Electrical and Computer Engineering
IBM Microelectronics Division, Hopewell Junction, NY (1988–1999)
Senior Engineer, DRAM Development Alliance, 1Gbit Integration Department (1997–1999), **Advisory Engineer**, Semiconductor Research & Development Center, Advanced Process Technology Department (1992–1997), **Staff Engineer**, Semiconductor Development Laboratory, CVD Technology Development Department (1988–1992)
Lawrence Livermore National Laboratory, Livermore, CA (1981–1988)
Student Engineer, Physics Department, (1984–1988), **Electronics Engineer**, Diagnostic Development Group, (1981–1984)
MacAulay Brown, Inc., Fairborn, OH (1980–1981)
Assistant Programmer (part-time)
NASA, Goddard Space Flight Center, Greenbelt, MD (1978–1980)
Engineering Intern, Instrument Electro-Optics Branch

AWARDS

Graduate Faculty Mentor Award, University of Maine (2015); Award for Service, IEEE Maine Section (2014); Graduate Faculty Mentor Award, University of Maine (2008); Dean's Award of Excellence, University of Maine (2005); Teaching and Technology Fellowship, University of Maine (2001) and 15 Invention Achievement Awards, IBM (1990-2000).

PROFESSIONAL AND HONORARY SOCIETIES

IEEE (senior member), American Physical Society (APS), National Association of Patent Practitioners (NAPP), American Society for Engineering Education (ASEE); *Tau Beta Pi*, (The Engineering Honor Society) and *Eta Kappa Nu*, (The Electrical and Computer Engineering Honor Society of the IEEE).

PROFESSIONAL AND PUBLIC SERVICE

Tau Beta Pi, (The Engineering Honor Society) Maine Alpha Chapter: Advisor (2006–2007), Chief Advisor (2008–2015), and Advisor (2016–present).

IEEE, Maine Section: Secretary (2001); Member at Large (2002); Vice Chair (2003); Chair (2004) and Treasurer (2006–2009); IEEE, University of Maine Student Branch Co-counselor (2003–2011).

Journal Reviewer: IEEE Transactions on Circuits & Systems; IEEE Electron Device Letters; IEEE Microwave & Wireless Components Letters; IEEE Journal of Solid State Circuits; Applied Physics Letters; Journal on Educational Resources in Computing; Journal of the American Ceramic Society; Journal of Vacuum Science & Technology; IET Circuits, Devices & Systems; and Journal of Circuits, Systems, and Computers; Analog Integrated Circuits and Signal Processing.

Proposal Reviewer: NSF panelist, Department of Defense SMART Scholarship panelist, Natural Sciences and Engineering Research Council of Canada (NSERC), and Civilian Research & Development Foundation (CRDF).

Book Reviewer: Prentice Hall and Oxford University Press.

University of Maine: Faculty Senator (2004–2007); Graduate School Executive Committee (2011); University of Maine New Faculty Mentor (2006–2009); Department of Electrical & Computer Engineering (ECE) Graduate Program Coordinator (2008–2011); Electrical Engineering Curriculum Committee Chair (2007–2011); Microelectronics Scholarship Consortium Chair (1999–2011); ECE Faculty Search Committee Chair (2000, 2001, 2006), ECE Graduate Board Representative (2000–2002, 2008–2011), and Member, Engineering and Science Building Committee (2001).

TEACHING EXPERIENCE - UNIVERSITY OF MAINE

ECE 209: Fundamentals of Electric Circuits (for non-ECE Majors)

ECE 210: Electric Circuits

ECE 214: Electric Circuits Laboratory

ECE 444: Analog Integrated Circuit Design

ECE 445: Digital Integrated Circuit Design

ECE 464: Microelectronics Science and Engineering

ECE 512: Linear Systems Analysis

ECE 543: Microelectronic Devices I

ECE 643: Microelectronics Devices II

ECE 547: Integrated Circuit Design and Layout

ECE 548: Integrated Circuit Characterization and Testing

ECE 598: Special Topics in Integrated Circuit Design

PUBLICATIONS

1. P. Gunturi and D. E. Kotecki, "Analysis of a Gaussian signal adder to increase the energy and spectral efficiency of a IR-UWB transmitter," *IEEE Trans. Signal Process.*, (submitted for publication, 2016).
2. P. Gunturi, N. Emanetoglu, and D. E. Kotecki, "IR-UWB BPK transmitter optimized for maximum distance of transmission," *IEEE Trans. Circuits Syst. I*, (submitted for publication, 2015).
3. P. Gunturi and D. E. Kotecki, "IR-UWB BPK transmitter optimized for maximum distance of transmission," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4.
4. P. Gunturi and D. E. Kotecki, "A PA for MBOFDM-UWB and IR-UWB transmitters," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4.
5. P. Gunturi and D. E. Kotecki, "Temperature and supply voltage insensitive OOK transmitter for outdoor UWB communications," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 733–736.
6. P. Gunturi and D. E. Kotecki, "A wideband Class E PA with more than 40% PAE and 800 MHz bandwidth," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 725–728.
7. P. Gunturi and D. E. Kotecki, "Class E power amplifiers with tuned RC output matching circuit," in *IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, San Diego, California, Sept. 2013.
8. Y. Lin and D. E. Kotecki, "A 127.3–133.6 GHz wide-locking low-power frequency-quadrupled phase-locked loop in 130nm SiGe BiCMOS," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '12)*, Boise, Idaho, Aug. 2012, pp. 754–757.
9. Y. Lin and D. E. Kotecki, "A 290 GHz frequency quadrupled SiGe voltage-controlled oscillator," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '11)*, Seoul, Korea, Aug. 2011, pp. 1–4.
10. Y. Lin and D. E. Kotecki, "2.9 – 30.3 GHz fourth-harmonic voltage-controlled oscillator in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 401–404.
11. Y. Lin and D. E. Kotecki, "A voltage-controlled oscillator with a 0.8–13.4 GHz tuning range in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 431–434.
12. Y. Lin and D. E. Kotecki, "312GHz fourth-harmonic voltage-controlled oscillator (VCO) designed using 130nm SiGe BiCMOS technology," in *Proc. IEEE International Conference on Electronics, Circuits and Systems, (ICECS '09)*, Yasmine, Tunisa, Dec. 2009, pp. 747–750, **(Best student paper award.)**.
13. B. C. Gierhart, D. G. Howitt, S. J. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, "Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA," *Sensors and Actuators, B: Chemical*, vol. 132, pp. 593–600, June 2008.

14. R. H. Bethel and D. E. Kotecki, "Low voltage BiCMOS circuit topologies for the design of a 19GHz, 1.2V, 4-bit accumulator in silicon-germanium," in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 1127–1130.
15. C. R. Kenney and D. E. Kotecki, "Microelectronic magnetic flux sensor for hearing aid application," in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 6–9.
16. B. Gierhart, D. Howitt, S. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, "Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA," in *Proc. 6th IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers '07)*, Lyon, France, June 2007, pp. 399–402.
17. S. Manandhar, S. E. Turner, and D. E. Kotecki, "36-GHz, 16x6 bit ROM in InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 451–456, Feb. 2007.
18. Z. Zhu, R. Tumati, S. Collins, R. Smith, and D. E. Kotecki, "A low-noise, low-offset operational amplifier in 0.35 μ m technology," in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 624–627.
19. S. Manandhar, S. E. Turner, and D. E. Kotecki, "A 20-GHz and 46-GHz, 32x6-bit ROM for DDS application in InP DHBT technology," in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 1003–1007.
20. S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with sine-weighted DAC at 32 GHz clock frequency in InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2284–2290, Oct. 2006.
21. D. E. Kotecki, T. Monk, V. Tkachuk, Z. Zhu, A. Delic-Ibukic, and S. E. Turner, "Custom analog and mixed-signal integrated circuit design at the undergraduate level – a university/industry collaboration," in *Proc. 6th International Workshop on Microelectronics Education*, Stockholm, Sweden, June 2006, pp. 47–50, ISBN: 91-7178-402-0.
22. S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with ROM-less architecture at 13-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, no. 5, pp. 296–298, May 2006.
23. S. E. Turner, R. B. Elder, Jr., D. S. Jansen, and D. E. Kotecki, "4-bit adder-accumulator at 41-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 15, no. 3, pp. 144–146, Mar. 2005.
24. S. E. Turner and D. E. Kotecki, "Benchmark results for high-speed 4-bit accumulators implemented in Indium Phosphide DHBT technology," *International Journal of High Speed Electronics and Systems*, vol. 14, no. 3, pp. 646–651, Sept. 2004.
25. F. Yang, D. E. Kotecki, G. Bernhardt, and M. Call, "Electrical and structural characterization of HfO₂ MIM capacitors," in *Novel Materials and Processes for Advanced CMOS, Proc. Mater. Res. Soc.*, vol. 745, 2003, pp. 203–208.
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53. C. M. Ransom, T. M. Jackson, J. DeGelormo, C. Zeller, D. E. Kotecki, C. Graimann, D. Sadana, and J. Benedict, "Shallow n⁺ junctions in silicon by arsenic gas-phase doping," *J. Electrochem. Soc.*, vol. 141, no. 5, pp. 1378–1381, May 1994.
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INVENTIONS (U.S. PATENTS)

1. Y. Park, H. Lee, D. E. Kotecki, and G. Costrini, "Contact plug formation for devices with stacked capacitors," U.S. Patent 6,753,252, issued June 22, 2004.
2. D. E. Kotecki and K. L. Saenger, "Method for fabricating a dual-diameter electrical conductor," U.S. Patent 6,727,174, issued April 17, 2004.
3. D. E. Kotecki and W. H. Ma, "Method of fabricating a stack capacitor DRAM," U.S. Patent 6,544,832, issued April 8, 2003.
4. J. P. Gambino, G. B. Bronner, D. E. Kotecki, and C. J. Radens, "Storage-capacitor electrode and interconnect," U.S. Patent 6,429,474, issued August 6, 2002.
5. H. Shen, D. E. Kotecki, S. D. Athavale, J. Lian, G. Kunkel, and N. Chaudhary, "Method for removal of hardmask used to define noble metal electrode," U.S. Patent 6,420,272, issued July 16, 2002.
6. D. E. Kotecki, C. J. Radens, J. P. Gambino, and G. B. Bronner, "Method for simultaneously forming a storage-capacitor electrode and interconnect," U.S. Patent 6,395,594, issued May 28, 2002.
7. H. Akatsu, D. E. Kotecki, J. J. Lian, and H. Shen, "Hydrogen peroxide and acid etchant for a wet etch process," U.S. Patent 6,357,577, issued April 30, 2002.
8. H. Shen, D. E. Kotecki, S. Athavale, J. Lian, L. Economikos, F. F. Jamin, G. Kunkel, and N. Chaudhary, "Semiconductor structure and manufacturing method," U.S. Patent 6,365,328, issued April 2, 2002.
9. S. D. Halle, P. C. Jamison, D. E. Kotecki, and R. S. Wise, "Retrograde openings in thin films," U.S. Patent 6,355,567, issued March 12, 2002.
10. Y. Y. Wang, R. Jammy, L. J. Kimball, D. E. Kotecki, J. Lian, C. Lin, J. A. Miller, N. Nagel, H. Shen, and H. S. Wildman, "Capacitor stack structure and method of fabricating," U.S. Patent 6,339,007, issued January 15, 2002.
11. P. Andricacos, G. Costrini, D. E. Kotecki, and K. L. Saenger, "Capacitor formed with Pt electrodes having a 3D cup-like shape with roughened inner and outer surfaces," U.S. Patent 6,323,127, issued November 27, 2001.

12. D. E. Kotecki and W. H. Ma, "Overhanging separator for self-defining stacked capacitor," U.S. Patent 6,268,259, issued July 31, 2001.
13. D. E. Kotecki and W. H. Ma, "DRAM stack capacitor with vias and conductive connection extending from above conductive lines to the substrate," U.S. Patent 6,262,450, issued July 17, 2001.
14. S. D. Athavale, H. Shen, D. E. Kotecki, and J. Lian, "Easy to remove hard mask layer for semiconductor device fabrication," U.S. Patent 6,261,967, issued July 17, 2001.
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