ECE 214 - Lab #10 — Villard Voltage Multiplier

17 April 2018

Pre-Lab: The operation of the Villard voltage doubler was described in class. One representation of this circuit is shown in Figure 1.

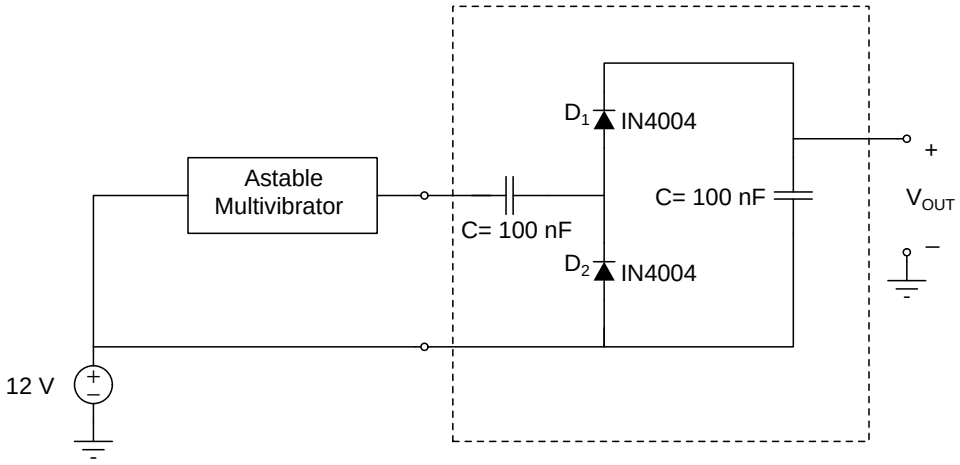

Figure 1: Villard voltage doubler.

1. Describe the operation of the voltage doubler shown in Figure 1.
2. Use NGspice to simulate the output of the voltage doubler when driven with the Astable Multivibrator circuit from Lab #8.
3. Run an extra long simulation ($\sim$ 200 ms) to verify you have reached the steady-state output voltage. How long does it take for the output voltage to reach a steady-state value?
4. Record the simulated output voltage, and the amplitude and frequency of the "ripple."
5. The output voltage from a Villard voltage doubler can be increased by cascading multiple stages together as shown in Figure 2. Describe the operation this circuit.
6. Use NGspice to simulate the output of the voltage multiplier when driven with the Astable Multivibrator circuit from Lab #8.
7. Run an extra long simulation ($\sim$ 200 ms) to verify you have reached the steady-state output voltage. How long does it take for the output voltage to reach a steady-state value?
8. Record the simulated output voltage, and the amplitude and frequency of the "ripple."

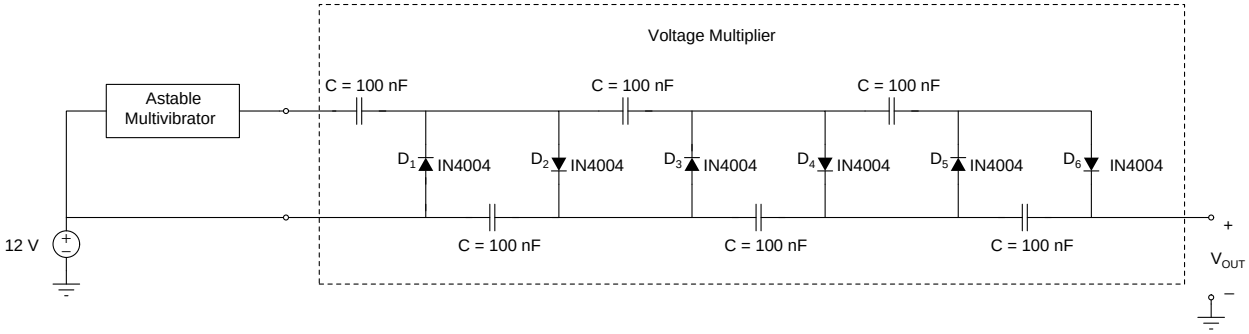

Figure 2: Cascaded Villard voltage multiplier circuit.

Lab Procedure:

1. Build the Villard voltage doubler circuit shown in Figure 1.
   (a) Measure and record the DC output voltage.
   (b) Measure and record the amplitude and fundamental frequency of the "ripple"
2. Build cascaded the Villard voltage multiplier in Figure 2.
   (a) Measure and record the DC output voltage.
   (b) Measure and record the amplitude and fundamental frequency of the "ripple"
3. Optional: try cascading your voltage multiplier with other team's voltage multipliers to further increase the output voltage. How high of an output voltage were you able to obtain?

Post Lab:

1. Compare the measured results to the simulated results.
2. Can the output voltage be increased by cascading voltage multiplier stages? Which component in your design will limit the maximum output voltage that can be obtained?
3. Reference this Post Lab in the table of contents of your notebook.