Test Case Name:	MFBP Filter Test	**Test ID #:**	MFBP-01
Description:	Verify that the MFBP filter meet gain (>1000 V/V) and frequency specifications (f_c = 20 kHz)	**Type:**	_**X**_ White box ___ Black box
Name of Tester:		**Date:**	
Hardware Rev.#:		**Time:**	

Test Equipment and Parts:

___ Digilent Analog Discovery (DAD) USB Instrument
___ Computer for controlling the DAD
___ Digital multimeter
___ Dual output power supply with ±12V output
___ 100:1 Voltage divider implemented with a 1 kΩ and a 10 Ω resistor
___ AWG 22 or 24 jumper wires for positive power rail (*VCC*), negative power rail (*VEE*), ground (*GND*), *signal_in*, *signal_out* and interconnections

Test Setup:

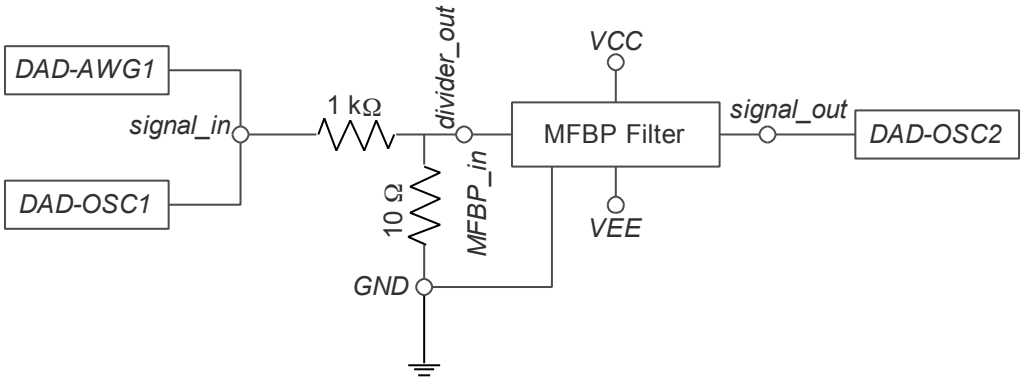
Isolate the MFBP filter from the rest of the receiver module by removing its input and output connections from the circuit. Build a 100:1 voltage divider with the 1 kΩ and 10 Ω resistors. See Test Note #1 for the justification of using a voltage divider. Connect the MFBP filter's VCC connector to the +12 V supply, and its VEE connector to the -12 V supply. Connect *DAD-AWG1* and *DAD-OSC1* to the input of the 100:1 voltage divider (*signal_in*). Connect power supply ground and *DAD-GND* to the ground connector of the MFBP. Connect the output of the voltage divider to the input of the MFBP filter. See connection diagram #1.

Step	**Action**	**Expected Result**	**Pass**	**Fail**	**N/A**	**Comments**
1	Turn on power supply				X	
2	Set *DAD-AWG1* output type to *DC offset* and value to 0V				X	
3	Run *DAD-AWG1*				X	
4	Measure the DC voltages at the *signal_in* and *signal_out* nodes	*signal_out* should be 0V ± 2 mV				

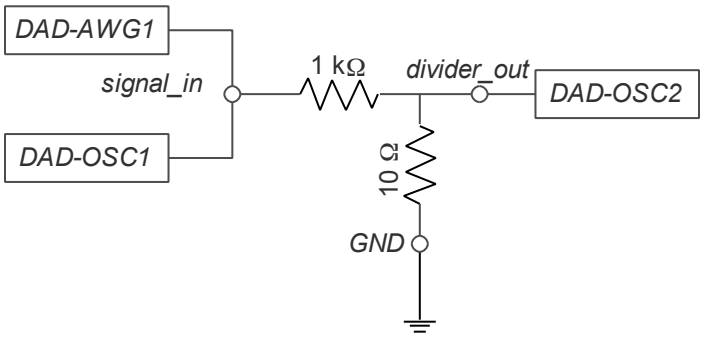
5	Connect *DAD-OSC2* to the output of the MFBP filter, *signal_out*				X	
6	Use the Oscilloscope to measure the time-domain output of the MFBP filter with *Ch2* set to 1 V per division, and set time base to 100 μs per division	The output should be flat, near 0V. Stop testing and see Test Note #2 if an oscillating signal at the MFBP's center frequency is present				
7	Stop *DAD-AWG1*	The output should be flat, near 0V.				
8	Set *DAD-AWG1* output type to *sine wave* with an amplitude of 100 mV, frequency of 20 kHz and DC offset of 0 V				X	
9	Run *DAD-AWG1*				X	
10	Use the Oscilloscope to measure the time-domain output of the MFBP filter with Ch2 set to 500 mV per division, and set time base to 100 μs per division	The output should be a 1V peak sine wave with minimal distortion (<1%)				
11	Export data as an ASCII file				X	
12	Stop *DAD-AWG1*				X	
13	Set Network Analyzer options to: Start 100 Hz, Stop 1 MHz, AWG Offset 0 V, Amplitude 100 mV, Steps 200, Max-Gain 50x				X	
14	Run the network analyzer once	A band pass filter with f_c = 20 kHz and maximum gain ≥ 20 dB (1000 V/V ÷ 100)				
15	Export data as an ASCII file, using magnitude units of Decibel				X	

16	Measure the center frequency	f_c = 20 kHz				
17	Measure the gain at center frequency	K ≥ 20 dB or 10 V/V				
18	Measure the 3 dB frequency bandwidth	1.5 kHz < BW < 3.0 kHz				
19	Turn off power supply				X	
20	Disconnect voltage divider from MFBP filter's input				X	
21	Disconnect *DAD-OSC2* from the output of the MFBP filter and connect it to the output of the voltage divider. See connection diagram #2.				X	
22	Set Network Analyzer Max-Gain 1x				X	
23	Run the network analyzer once	Flat characteristic with a magnitude of ~ -40 dB and phase of 0 deg				
24	Export data as a CSV file, using magnitude units of Decibel				X	
25	Import both data files to Matlab and plot				X	
26	Obtain the actual MFBP response by subtracting *Ch2* values of the resistive voltage divider from the overall measurement	A band pass filter with f_c = 20 kHz, maximum gain ≥ 60 dB (1000 V/V) and 3 dB frequency between 1.5 kHz and 2.5 kHz				
	Overall Test Result					

Test Setups for Measuring the Frequency Response of the MFBP Filter



Connection Diagram #1 Test setup for measuring the frequency response of the MFBP filter, including voltage divider interface circuit.



Connection Diagram #2 Test setup for measuring the frequency response of the voltage divider interface circuit.

Test Note #1: Using a Voltage Divider for the MFBP Active Filter Characterization

The MFBP filter specifications call for a voltage gain that is at least 60 dB (1000 V/V) at the center frequency, and power rails of ±12 V. The filter is implemented using LF347 op-amps, which has a maximum output voltage swing of ~ 21 $V_{p\text{-}p}$, or 10.5 V_p when powered with ±12 V supplies [1]. In order to avoid distortion of the output signal (which transfers energy to harmonic frequencies of the signal's fundamental frequency), the output signal magnitude should be kept small, less than 5 V_p.

This test setup is such that the output signal's peak voltage will be 1 V. The corresponding input voltage should have a peak magnitude of 1 mV_p. However, the resolution of the Digilent Analog Discovery's oscilloscope and arbitrary wave form generator are 500 μV. Hence, the DAD would essentially output a square wave at this low magnitude. In order to make an accurate measurement, the input signal peak magnitude should be larger than 50 mV_p. The test designer has chosen a peak amplitude of 100 mV_p for the AWG1 output.

A voltage divider is required to derive an approximately 1 mV_p input to the MFBP filter from a 100 mV_p signal. The required voltage division is 100:1. Using the standard voltage divider equation, we obtain:

$$\frac{R_2}{R_1 + R_2} = 0.01$$

Thus, $R_1 = 99\ R_2$. This could be achieved with good accuracy if 1% tolerance or better resistors are used. However, only 5% tolerance resistors are available to the test engineers. Hence, $R_1 = 100\ R_2$ is chosen, as standard value resistors are available in each decade.

The ideal signal source should have a signal source resistance of $R_{sig} = 0\ \Omega$. In practice, this value needs to be much smaller than the input resistance, R_{in}, of the following circuit. The MFBP's input resistance is likely to be in the 500 Ω to 2 kΩ range. Larger values are better as the output resistance of the LF347 itself is around 10 Ω at 10 kHz for $A_V = 100$ [1], close to the likely gain of a single stage in the two-stage MFBP filter.

The output resistance of the signal source and voltage divider will be $R_{sig} = R_1 // R_2 \cong R_2$, as $R_1 = 100R_2$. The resistance that the AWG drives is $R_1 + R_2 // R_{in} \cong R_1 + R_2 \cong R_1$ if $R_2 << R_{in}$. It would be good to choose $R_1 = 10\ \Omega$ and $R_2 = 0.1\ \Omega$, or even $R_1 = 100\ \Omega$ and $R_2 = 1\ \Omega$. However, the DAD's AWG units would not be able to drive such small resistances at high (or even low) frequencies.

A good compromise is choosing $R_1 = 1$ kΩ and $R_2 = 10\ \Omega$ for $R_{in} = 1$ kΩ, resulting in $R_{sig} \cong 10\ \Omega < R_{in}$, and the AWG would drive a 1 kΩ resistance with a 100 mV_p signal. The resulting peak output current from the AWG would be 100 μA_p, and the input signal magnitude could be safely increased to 1 V_p in order to accurately measure the MFBP filter characteristics in the stop band.

[1] LF347 Datasheet, National Semiconductor, 1995

Test Note #2: Circuit Layout and Supply Bypass for High Gain Amplifiers

The two stage MFBP active filter will have a voltage gain between 1000 V/V (60 dB) to 10000 V/V (80 dB) at the center frequency of the filter. When the active filter is powered, it will start drawing bias current from the power supplies, at approximately 7.2 mA per LF347. This will cause a ripple of approximately 0.1 Ω x 7 mA = 700 μV on the power leads (a wire resistance of 0.1 Ω is assumed for the breadboard). The positive supply rejection ratio (PSRR) of the LF347 at 10 kHz is approximately 80 dB, but the PSRR of the negative supply is only about 46 dB. Thus, for most of the MFBP designs, this 700 μV ripple will be amplified by 14 dB to 34 dB, causing the op-amps to draw more current from the power supply, which will further increase the ripple. Thus, a positive feedback loop will be formed through the negative power supply rail, and potentially the ground connection as well.

A further complication can come from the power supplies themselves. Most modern power supplies are switching power supplies, and they inject noise into the power rails. This noise will also be amplified and cause an oscillation if the switching frequency is within the amplifying bandwidth (not just the 3 dB bandwidth) of the MFBP active filter.

The positive feedback through the power rails will cause the circuit to oscillate at the center frequency of the MFBP filter. Thus, the circuit will become an oscillator instead of a filter. There are several precautions that can be taken to eliminate the oscillation problem.

1. ***Clean layout:*** Avoid cross-talk by eliminating spaghetti wiring. Keep power leads as short as possible. Feeding the power to the breadboard at one end and having amplifiers at the other end of the breadboard is one probable cause of oscillation. If you are using an LF347 quad op-amp package, try the steps described below in 2 through 4. If they don't work, replace the LF347 with however many LF356s or TL071s as you need. Try feeding power rails into the breadboard from the middle of the board instead, or provide the each LF356 (or TL071) op-amp with its own wire connection to the power supply if all else (described below) fails.
2. ***Supply bypass capacitors:*** Use supply bypass capacitors (described in ECE 210) to reduce the voltage ripple caused by current drawn from the supplies. Each positive and negative supply pin should have at least one supply bypass capacitor between it and GND. These should be placed as close as possible to the power pins on the ICs. It might be necessary to use a large value (1 μF – 100 μF) electrolytic capacitor for low frequencies, and a smaller (30 nF – 300 nF) ceramic or other type capacitor for high frequencies. Check the data sheet of the capacitor to determine its self-resonant frequency. Typical aluminum electrolytic capacitors have a self-resonance frequency around 10 kHz, and larger capacitors have smaller self-resonance frequencies if lead lengths are equal.
3. ***Chokes, i.e. inductors:*** An inductor connected in series between the power supply and the power pin will act as a low pass filter in conjunction with the supply bypass capacitor, further reducing ripple.
4. ***Voltage regulators:*** It might be necessary to use voltage regulators, such as the LM7812 and the LM7912 linear drop-out voltage regulators for +12 V and -12 V, respectively. The voltage regulators would be used with each LF347 (or LF356) IC. As the voltage regulators need larger magnitude input voltages than their output voltages, the power supplies would need to be adjusted to ±15 V. Avoid using switching voltage regulators, as most have switching frequencies that are near the center frequency of the MFBP. They would make the problem worse.