The University of Maine
Department of Electrical and Computer Engineering
ECE 445 – Design and Analysis of Digital Integrated Circuits

Fall 2019

Design and Analysis of Digital Integrated Circuits

Course Number : ECE 445
Credits: 3
Lecture : 2:00 - 3:15 pm, Tuesday and Thursday; Barrows 119
Prerequisite: ECE 342 - Electronics I
Course Website: http://web.eece.maine.edu/kotecki/ECE445

Instructor

Dr. David E. Kotecki
Office: 277 Barrows / ESRB
e-mail: kotecki@maine.edu
Tel: 207 581-2248

Office Hours

9:30 - 11:30 am, Monday and Wednesday
1:00 – 2:00 pm, Tuesday and Thursday
You are encouraged to drop by my office to ask questions and discuss labs related to this course. If you are unable to meet with me during these times, e-mail me to set up an appointment.

Primary Text

“Analysis and Design of Digital Integrated Circuits In Deep Submicron Technology, (3rd edition)”
Authors: David A. Hodges, Horace G. Jackson, and Resve A. Saleh
Publisher: McGraw Hill
Year: 2004
ISBN: 0-07-228365-3

Reference Texts

"Digital Integrated Circuits, (2nd Edition)"
Authors: Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic
Publisher: Prentice Hall Electronics and VLSI Series
Year: 2003
ISBN-10: 0130909963

"CMOS Digital Integrated Circuits, (4th edition)"
Authors: Sung-Mo Kang, Yusuf Leblebici and Chulwoo Kim
Publisher: McGraw Hill
Year: 2015
ISBN: 978-0-07-338062-9

Course Material and Goals

The challenge for the digital integrated circuit designer is to design circuits that implement the required logic function while achieving high reliability of operation and a good balance between cost, performance and power. The circuit must operate properly in the presence of process variations, supply voltage fluctuations, and changes in environmental conditions.

Topics to be discussed: technology nodes and MOSFET device scaling; characteristics of short channel MOSFET devices and device models; interconnect strategy and interconnect scaling; parasitic resistance, capacitance and inductance associated with interconnects; the inverter; static logic gates; dynamic logic gates; sizing gates using the method of logic effort; trade-offs between performance, power, reliability, noise immunity and cost among various logic families including CMOS, pseudo–NMOS, domino logic, pass–gate logic and differential cascade voltage swing logic (DCVSL); fundamentals of combinational logic circuits; fundamentals of sequential logic circuits; adder circuits and pipelining; memory circuits including ROM, E^2PROM, DRAM, SRAM, MRAM, FLASH and PCM; timing characteristics; and low power design techniques.

Fundamental Goal: Provide an understanding of the fundamentals of Digital Integrated Circuit Design from the transistor–level point of view with an emphasis on **design trade–offs** required for optimization of Circuit Performance, Cost, Power Consumption, Noise Immunity and Reliability.

Most of the course material will follow the text book. Additional material may be provided and will be posted on the course website.

Homework Assignments

Homework problems are located at the end of each chapter. Assigned problems are listed below. Homework will neither be collected nor graded. If you have questions about any of the problems either stop by my office to discuss them or we can go over them in class. I recommend you do as many of the homework problems as possible; some of the exam questions will be similar to, or the same as, the homework problems.

Assignment	Problems
Homework #1	1.1, 1.3, 1.7, 1.8, 1.10
Homework #2	2.2, 2.3, 2.4, 2.5, 2.9
Homework #3	3.2, 3.8, 3.11, 3.12, 3.12
Homework #4	4.1, 4.4, 4.7, 4.9, 4.14
Homework #5	5.1, 5.3, 5.8, 5.11, 5.14
Homework #6	6.7, 6.8, 6.9, 6.12, 6.14
Homework #7	7.2, 7.4, 7.6, 7.9, 7.14
Homework #8	8.1, 8.4, 8.7, 9.8, 9.11
Homework #9	10.1, 10.3, 10.9

Design Projects

To provide understanding and insight into fundamental issues in deep–submicron digital design, a two-part design and simulation project is assigned. Details of the project are found on the web page at http://web.eece.maine.edu/kotecki/ECE445/docs/ECE445_2019_Project.pdf. The project will utilize a 65nm CMOS processes and involve the design and simulation of a 4-bit ripple carry adder.

Exams

There will be two Preliminary Exams and a Final Exam. The preliminary exams are open–book, open–notes and will consist of an in–class portion and a possible take–home portion. The Final Exam will be open–book, open–notes and will be an in–class exam during final exam week.

Tentative Exam dates:

Exam 1: 17 October 2019
Exam 2: 21 November 2019

Grading:

The final course grade is determined as follows:

Design Project	40% each
Preliminary Exams (2)	20% each
Final Exam	20%
Total	100%

Letter grades are assigned as follows:

$\geq 90\%$	A
87% – 90%	B +
80% – 87%	B
77% – 80%	C +
70% – 77%	C
67% – 70%	D +
60% – 67%	D
$< 60\%$	F

Academic Honesty Statement

Academic honesty is very important. It is dishonest to cheat on exams, to copy term papers, to submit papers written by another person, to fake experimental results, or to copy or reword parts of books or articles into your own papers without appropriately citing the source. Students committing or aiding in any of these violations may be given failing grades for an assignment or for an entire course, at the discretion of the instructor. In addition to any academic action taken by an instructor, these violations are also subject to action under the University of Maine Student Conduct Code. The maximum possible sanction under the student conduct code is dismissal from the University.

Students with Disabilities Statement

If you have a disability for which you may be requesting an accommodation, contact Student Accessibility Services, 121 East Annex, 581.2319, as early as possible. Students who have already been approved for accommodations by SAS and have a current accommodation letter should provide a copy of the letter to me as soon as possible.

Course Schedule Disclaimer (Disruption Clause)

In the event of an extended disruption of normal classroom activities, the format for this course may be modified to enable its completion within its programmed time frame. In that event, you will be provided an addendum to the syllabus that will supersede this version.

Sexual Violence Policy: Sexual Discrimination Reporting

The University of Maine is committed to making campus a safe place for students. Because of this commitment, if you tell a teacher about an experience of sexual assault, sexual harassment, stalking, relationship abuse (dating violence and domestic violence), sexual misconduct or any form of gender discrimination involving members of the campus, your teacher is required to report this information to the campus Office of Sexual Assault & Violence Prevention or the Office of Equal Opportunity.

If you want to talk in confidence to someone about an experience of sexual discrimination, please contact these resources:

For confidential resources on campus: Counseling Center: 207-581-1392 or Cutler Health Center: at 207-581-4000.

For confidential resources off campus: Rape Response Services: 1-800-310-0000 or Spruce Run: 1-800-863-9909.

Other resources: The resources listed below can offer support but may have to report the incident to others who can help: For support services on campus: Office of Sexual Assault & Violence Prevention: 207-581-1406, Office of Community Standards: 207-581-1409, University of Maine Police: 207-581-4040 or 911. Or see the OSAVP website for a complete list of services at http://www.umaine.edu/osavp/