ECE 445 Design Project – 4-bit Carry-Ripple Adder

Part A: Design an inverter, ring oscillator, and buffer which meet the following specifications, and determine the power requirement of the ring oscillator and digital buffer:

1. Limitations
   (a) Temperature = 27 C.
   (b) $V_{DD} \leq 1.2$ V.
2. 1X Inverter
   (a) $L_n = L_p = 65$ nm; $W_n = 100$ nm; $W_p \geq W_n$.
   (b) Switching voltage (V_S) $\approx V_{DD}/2$.
   (c) $t_{P_{HL}} \approx t_{P_{LH}}$.
3. Ring Oscillator (using 1X inverters)
   (a) f $= 1$ GHz ± 3%.
   (b) Power = ?
4. Digital Buffer
   (a) Buffer should allow the Ring Oscillator to drive a load capacitance of 5 pF.
   (b) Power = ?

Due: 10 October 2019

Part B: Design a 4-bit carry-ripple adder configured as a counter using the 65nm CMOS process which meets the following specifications:

1. Performance and Limitations:
   (a) The 4-bit counter increments by “1” each clock cycle.
   (b) Clock frequency = 5 GHz.
   (c) Temperature = 27 C.
   (d) $L_n = L_p = 65$ nm; $W_n = 100$ nm; $W_p \geq W_n$.
   (e) Average power consumption = minimum. The design with the lowest average power consumption wins a prize!!!
2. Inputs (3):
   (a) Single ground node labeled: “gnd”.
   (b) Single DC voltage source $V_{sup} \leq 1.2$ V - labeled as “vsup”.
   (c) Ideal clock using the PULSE generator input to a sequence of three 1X-inverters. The output the tjord inverter is labeled as “clk”.
      i. Period = 0.2 ns.
      ii. Voltage levels: 0 and V_{sup}.
      iii. Rise time, fall time, and duty cycle: up to the designer.
3. Outputs (4):
   (a) Most significant bit - labeled as “s3”.
   (b) Next most significant bit - labeled as “s2”.
   (c) Next most significant bit - labeled as “s1”,
   (d) Least significant bit - labeled as “s0”.

Due: Last week of class.