ECE 445 Design Project – 5-bit Carry-Ripple Adder

Part A: Design an inverter, ring oscillator, and buffer using the 65nm CMOS process that meet the following specifications.

1. Limitations
   (a) Temperature = 27 C.
   (b) $V_{DD} \leq 1.2$ V.
2. 1X Inverter
   (a) $L_n = L_p = 65$ nm, $W_n \geq 100$ nm, $W_p \geq 100$ nm.
   (b) Switching voltage (V_S) $\approx V_{DD}/2$.
   (c) $t_{P_{HL}} \approx t_{P_{LH}}$.
3. Ring Oscillator and Digital Buffer
   (a) Oscillation frequency $f = 5$ GHz $\pm 3\%$.
   (b) Digital buffer must allow the Ring Oscillator to drive a load capacitance of 1 pF.

Simulate the power consumed by the ring oscillator and the digital buffer. Submit a short (less than 5 page) report describing the design and simulation results.

Tentative due date: October 15, 2020.

Part B: Design a 5-bit carry-ripple adder, configured as a counter, using the 65nm CMOS process that meets the following specifications:

1. Performance and Limitations:
   (a) The 5-bit counter increments by “1” each clock cycle.
   (b) Clock frequency = 5 GHz.
   (c) Temperature = 27 C.
   (d) $L_n = L_p = 65$ nm, $W_n \geq 100$ nm, $W_p \geq 100$ nm.
   (e) Average power consumption = minimum. The design with the lowest average power consumption wins!!!
2. Inputs (3):
   (a) Single ground node labeled: “gnd”.
   (b) Single DC voltage source $V_{sup} \leq 1.2$ V.
   (c) Clock generated by the ring oscillator designed in Part A. The output of the ring oscillator should be labeled “clk”.
3. Outputs (4):
   (a) Most significant bit - labeled as “s4”.
   (b) Next most significant bit - labeled as “s3”.
   (c) Next most significant bit - labeled as “s2”.
   (d) Next most significant bit - labeled as “s1”,
   (e) Least significant bit - labeled as “s0”.

Final Report: Submit a final report, similar to an ECE 342 lab report, describing the 5-bit carry ripple adder.

Tentative due date: December 17, 2020.