ECE 445 – Design Project
4-bit Carry-Ripple Adder

October 4, 2016

Goal: Design a 4-bit carry-ripple adder configured as a counter using the 65nm_bulk CMOS process which meets the following specifications:

1. Performance:
   (a) The 4-bit counter increments by "1" at each clock cycle.
   (b) Clock frequency = 5 GHz.
   (c) Temperature = 27 C.
   (d) Average power consumption = minimum. The design with the lowest average power consumption wins!!!
2. Inputs (3):
   (a) Single ground node - labeled as "gnd".
   (b) Single DC voltage source $V_{sup} \leq 1.2$ V - labeled as "vsup".
   (c) Ideal clock using the PULSE generator input to a single 1X-inverter - label the output of the inverter as "clkinv".
      i. Period = 0.2 ns.
      ii. Voltage levels: 0 and V_{sup}.
      iii. Rise time, fall time, and duty cycle: up to the designer.
3. Outputs (4):
   (a) Most significant bit - labeled as "s3".
   (b) Next most significant bit - labeled as "s2".
   (c) Next most significant bit - labeled as "s1",
   (d) Least significant bit - labeled as "s0".

Due: 1 December 2016.

Submit: E-mail the `ngspice.netlist` and `test.hspc` files for the top-level design to: kotecki@maine.edu. These two files are located in the "CppSim/SimRuns/LibraryName/TopLevelDesignName" directory.