12-bit Digital to Analog Converter

Jason Beaulieu

ABSTRACT

A CMOS design of a 12-bit DAC for the AMI C5N process. Simulation results show the design can operates on a 4MHz clock and can produce a 1.6V_{pp} output sine wave up to 2MHz centered at 2.2V. The chip is a dual packaged DAC, with isolated opamp and resistor segment (for testing purposes). The DAC accepts a 0-5V 12-bit digital input signal in binary format. The DAC topology is a Wide-Swing Current-Mode Segmented R-2R with a R=40kΩ. The design has a maximum capacitive load of 50pF in parallel with a minimum resistive load of 500Ω. Spectral analysis of the simulation output shows the fundamental signal strength of a 250KHz signal to be approximately 70dB higher than the nearest overtone.

CONTENTS

I.

A. Project Objectives

The objective of this design was to build a 12-bit Digital to Analog Converter (DAC). The DAC takes a digital representation of a waveform in a binary format and outputs an analog version of the waveform. The specifications of the DAC are as follows:

Voltage Supply Rails	Vdd=5v Gnd=0v
Clock Frequency	4MHz
Output Range	1.6V$_{pp}$
Drive Strength	50pF parallel with 500Ω
Topology	Wide-Swing Current-Mode R-2R

TABLE I

SPECIFICATIONS

B. Design Methodology

The design implements the DAC using a wide-swing current-mode R-2R topology. This was done to take advantage of the wide output swing of a voltage-mode R-2R DAC, while at the same time having a fixed input common mode voltage as in a current-mode R-2R DAC. A R-2R DAC is a form of Binary Weighted DAC which creates each analog output voltage through a repeating resistor structure of value R and $2*R$. This requires very high precision resistors and is usually limited to a max of 8-bit resolution. To use the R-2R structure and keep the resolution of 12-bits this design uses a thermometer decoder circuit to segment the top 4 bits of the DAC. This allows for a 12-bit resolution while only needing the accuracy of a 8-bit DAC.

A thermometer decoder is a logic circuit that has n inputs and $2^n - 1$ outputs. Each output corresponds to a base 10 value of the possible binary inputs. Figure 1 below shows an example of a 3-bit thermometer decoder.

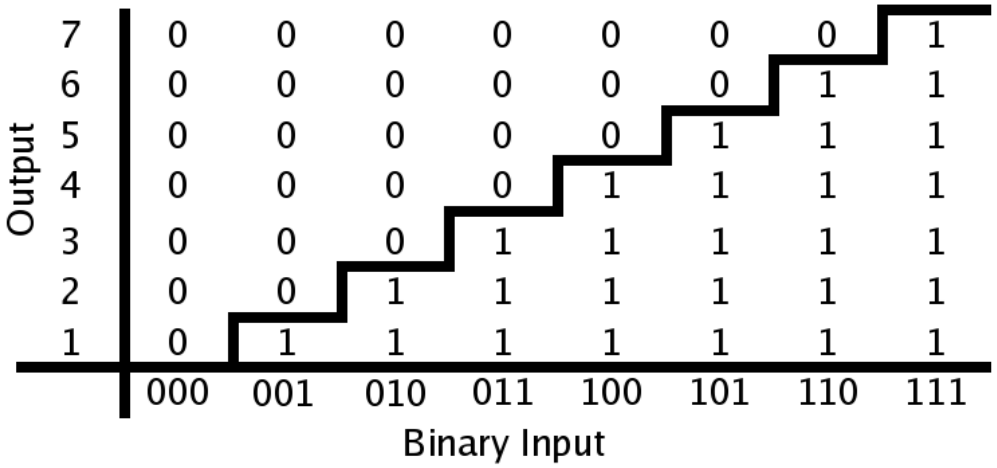

Fig. 1. 3-bit Thermometer Decoder Output.

The output of the combination of the 8-bit resistor ladder and 4-bit thermometer decoder go into a opamp in the inverting configuration with the non-inverting input set to $V_{cm} = \frac{VDD}{2}$.

II.

A. Design Schematics

This section will discuss the various schematics of the design.

1) Resistor Network: Figure 2 below is the schematic for the resistor network. The first 8-bits go into a normal R-2R network, then the top 4-bits, after going through a 4-bit thermometer decoder, go into the top 15 resistors. For this DAC R=40$k\Omega$.

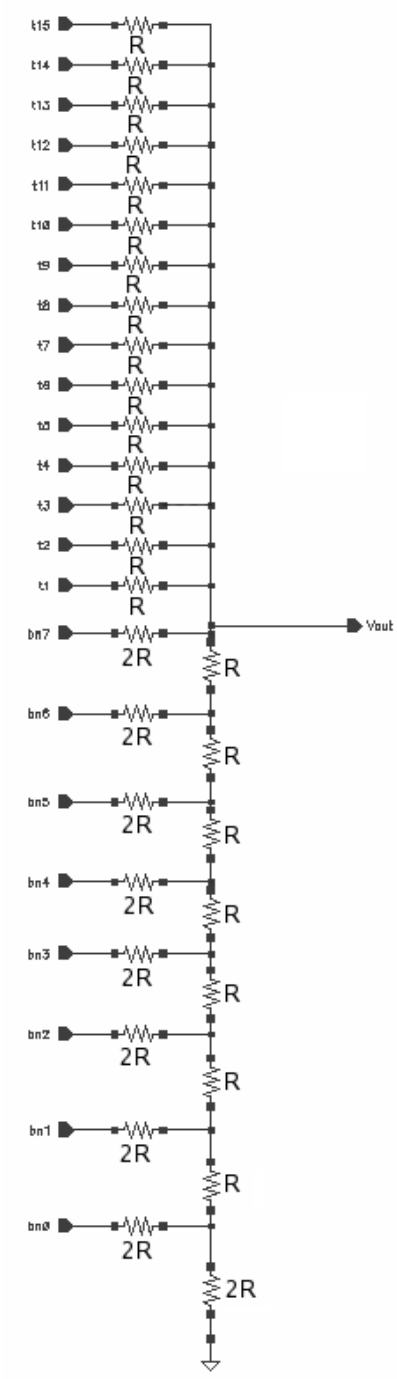

Fig. 2. Resistor Ladder Network.

2) Thermometer Decoder: Figure 3 below is the schematic for the thermometer decoder. This is a 4-bit thermometer decoder. Each logic gate is built from a reference invert with NMOS W=1.5μm and L=0.6μm. The output gates all have a 4x digital buffer to give them the drive strength to drive the resistor network.

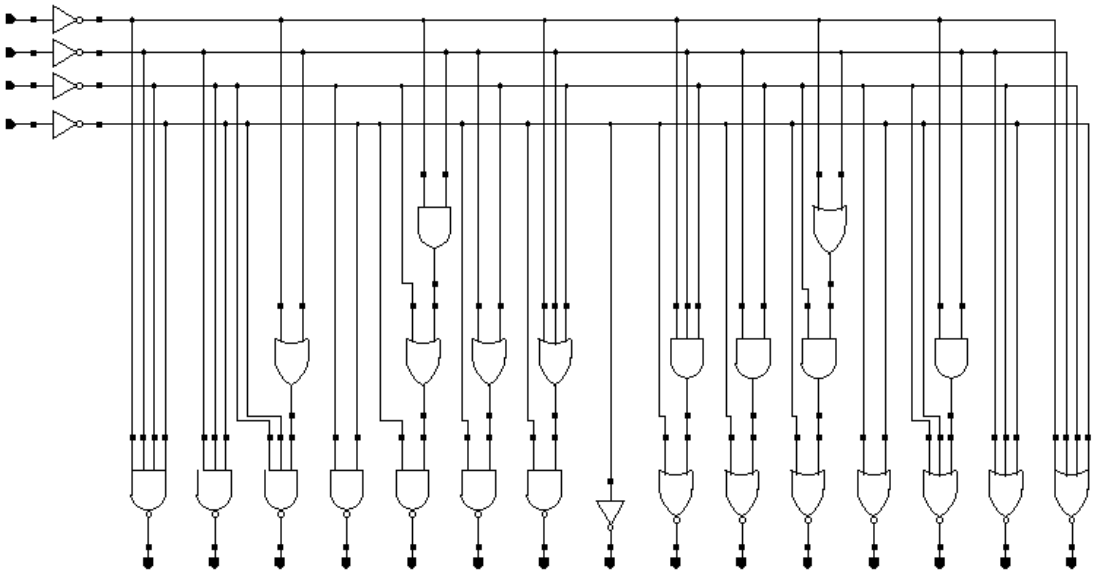

Fig. 3. Thermometer Decoder Schematic.

3) 3-Stage Opamp: Figure 4 below is the schematic for the 3-stage opamp. The first stage is a bias network that includes a 7k resistor and 2 diode connected NMOS devices. This generates the 384μA bias current for the rest of the opamp. The second stage is a Differential Pair with active load. Finally the third stage is a common source gain stage with output buffer. The output buffer is a simple push-pull driver which was needed to drive the DAC output off chip.

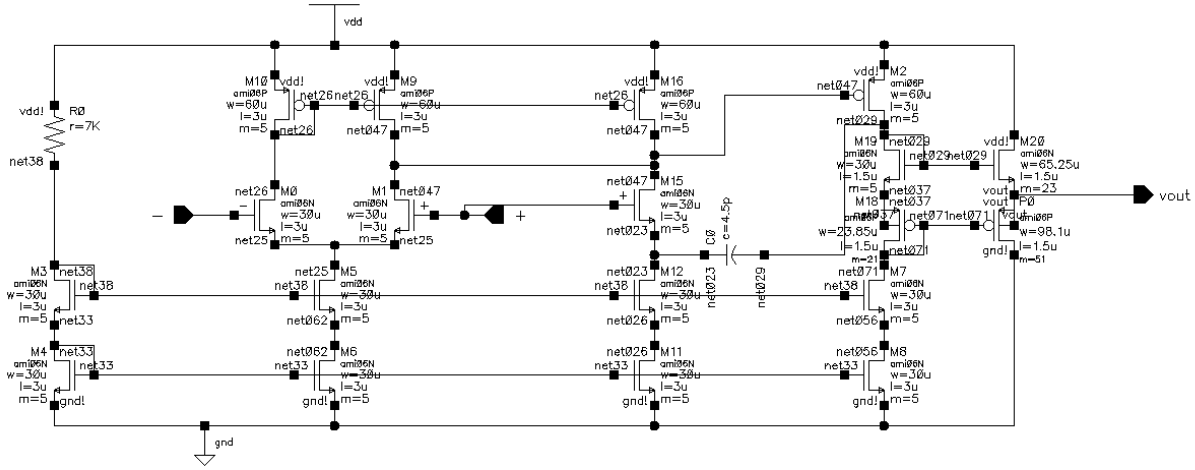

Fig. 4. 3-Stage Opamp Schematic.

4) Complete Schematic: Figure 5 below is the complete schematic for the DAC. The input signals get inverted and buffered with a 4x digital buffer before getting driven to the resistor network which drives the opamp that has a feedback resistor of 800Ω. The non-inverting terminal of the opamp is biased by a resistor divider to around 2.2V.

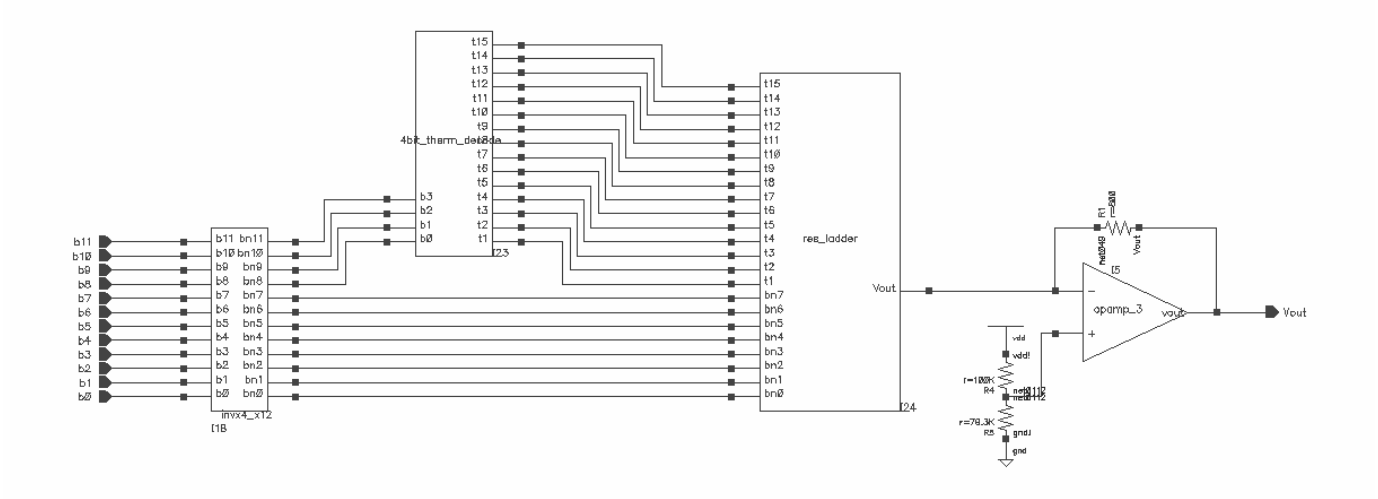

Fig. 5. Complete Schematic.

5) Top Level Schematic: Figure 6 below shows the top chip level schematic. The chip includes 2 12-bit DACs, isolated Opamp, and isolated 20k resistor segment. The resistor segment is the same as what is used for the resistor network. Both the isolated opamp and resistor segment are for testing purposes.

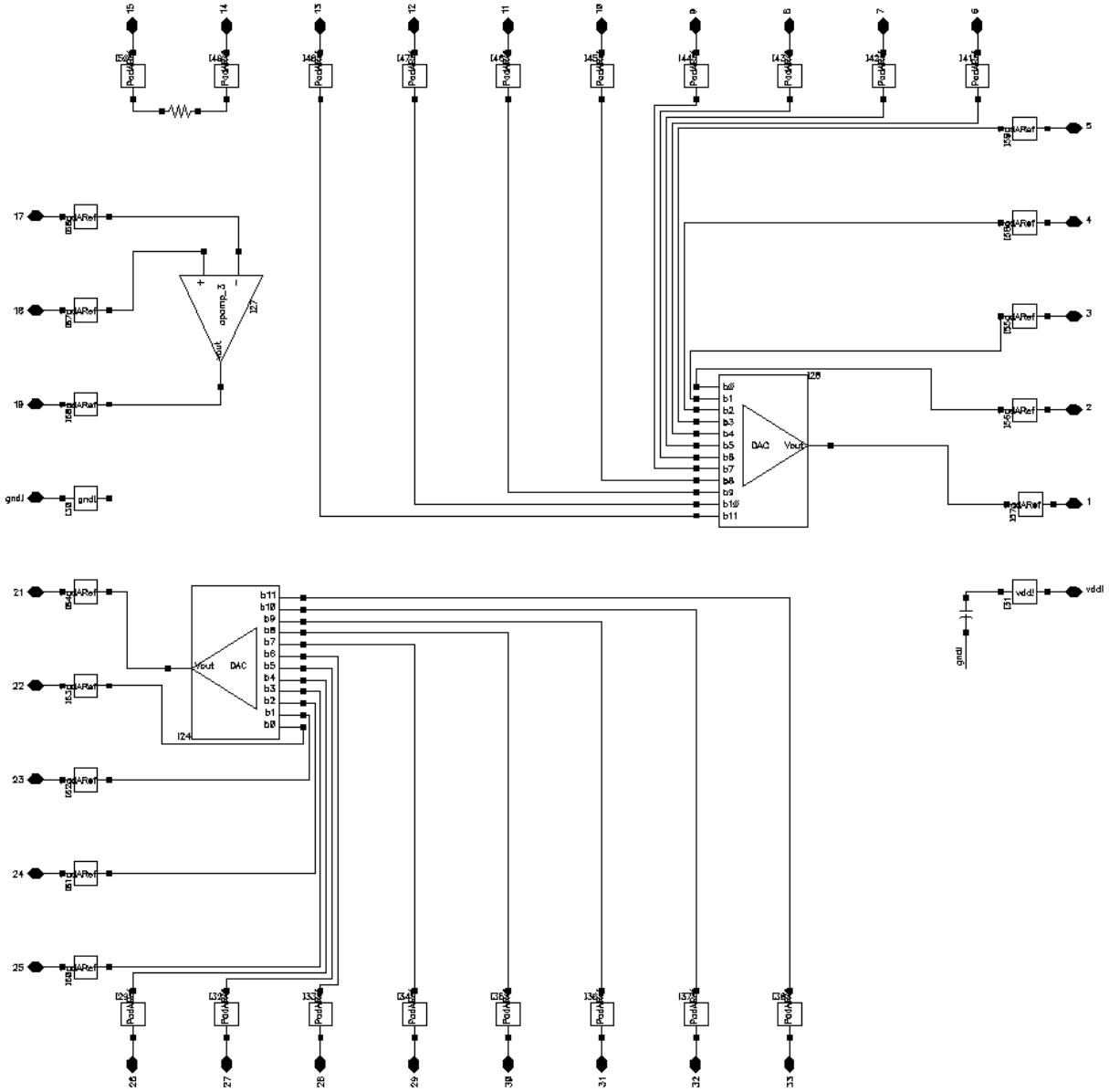

Fig. 6. Top Level Schematic.

B. Design Layout

1) Resistor Network: The resistor network layout was done using a $20k\Omega$ segment resistor and some resistor matching techniques. Each R-2R pair was matched using the common-centroid technique and then matched to each other pair. The thermometer decoder resistors were also matched together using the common-centroid technique.

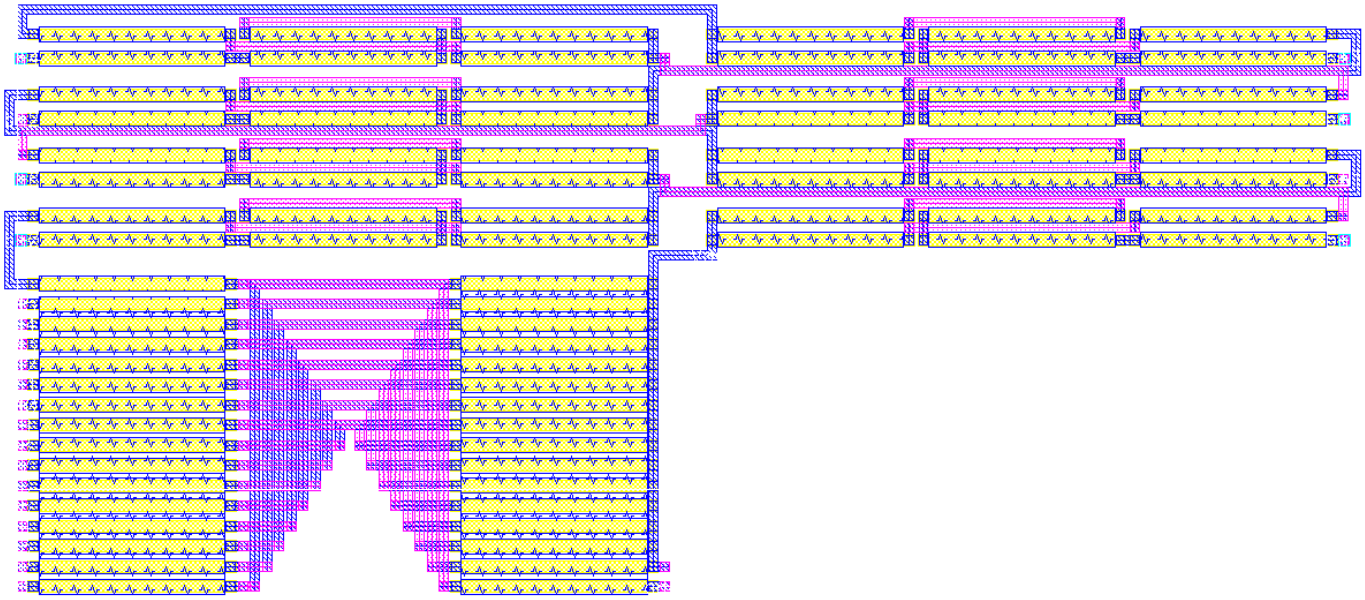

Fig. 7. Resistor Ladder Network.

2) Thermometer Decoder: The thermometer decoder layout was done with custom standard cells that could be placed next to one another to interconnect the power and ground rails. This made laying out the entire thermometer decoder much simpler.

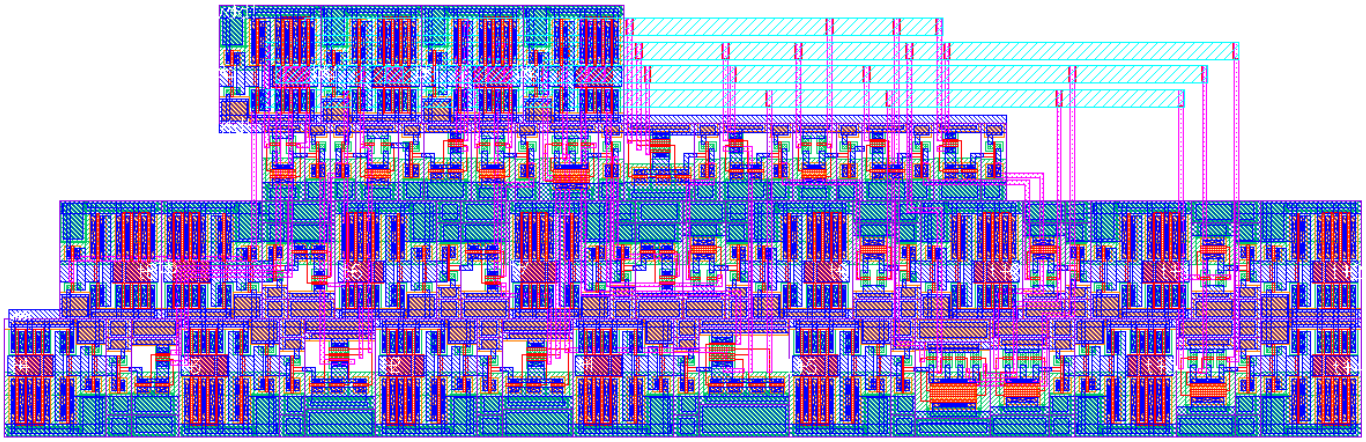

Fig. 8. Thermometer Decoder Layout.

3) 3-Stage Opamp: The Opamp layout was done to minimize space. Multipliers were used on the large output driver devices.

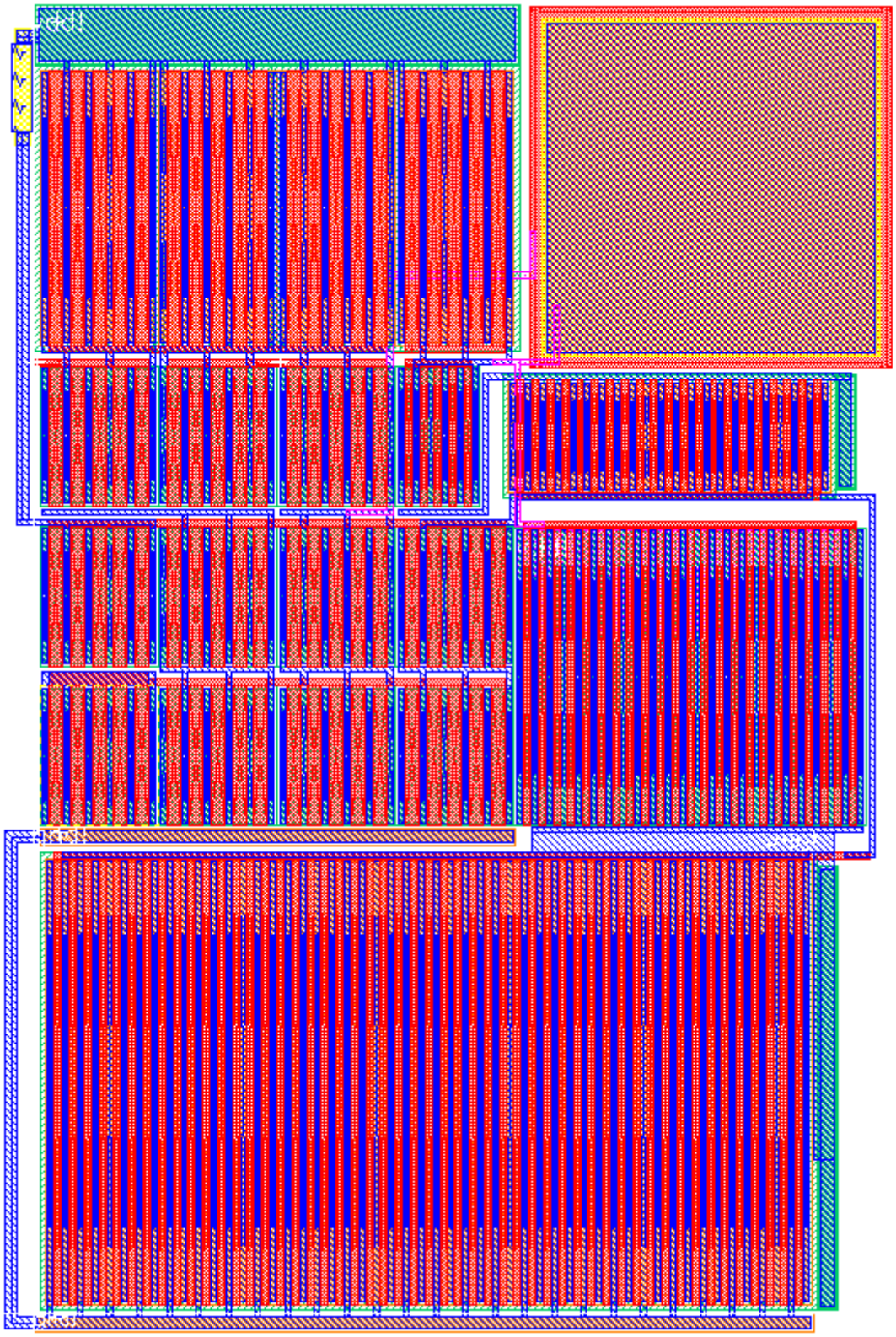

Fig. 9. 3-Stage Opamp Layout.

4) Top Level Layout: On the top level layout each piece was placed to make routing of signals easier. The space that was left over after placing everything needed was used to make power rail decoupling capacitors. There is a total of 135pF of decoupling capacitance.

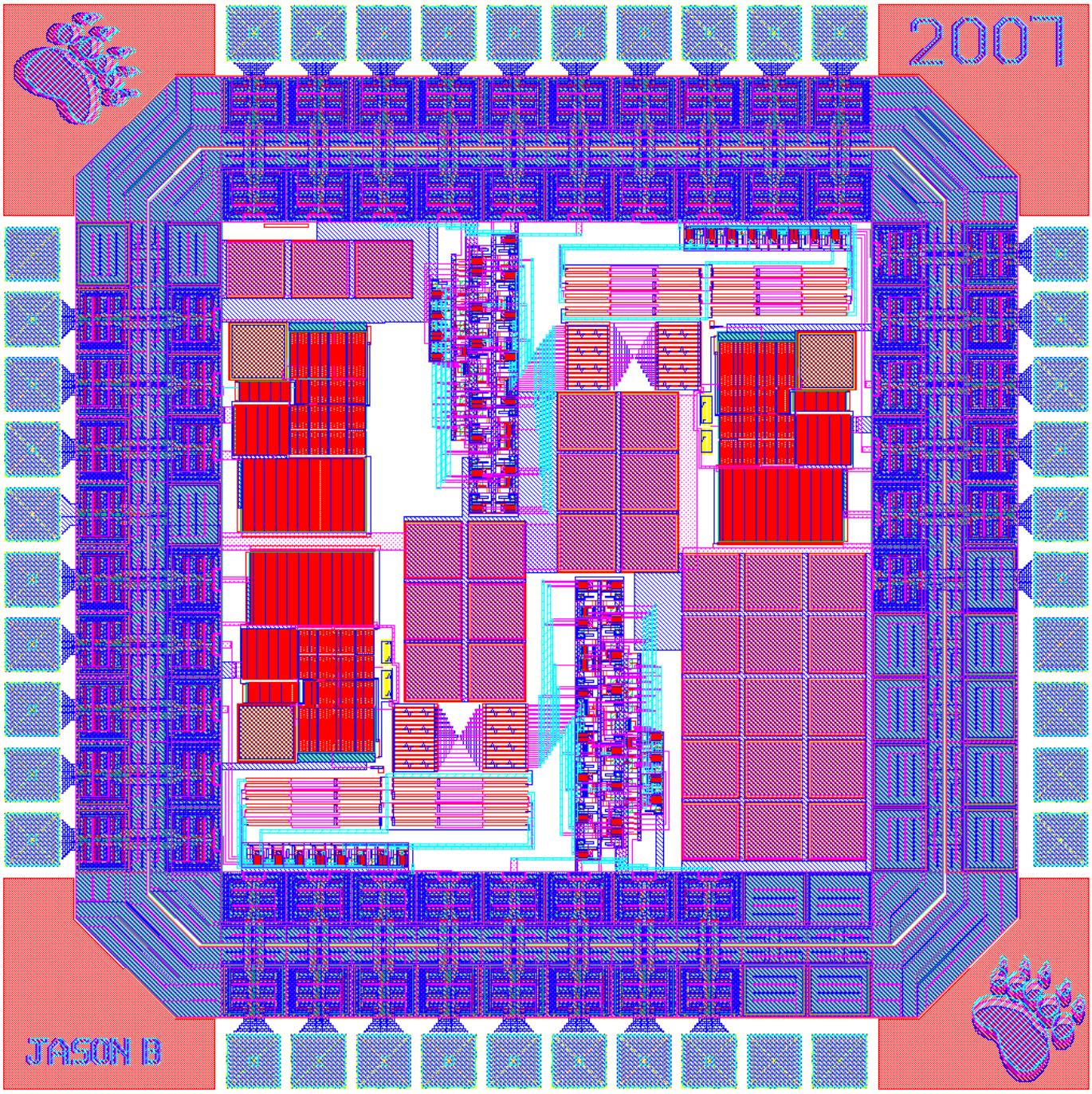

Fig. 10. Top Level Layout.

C. Simulations

1) Opamp Response: This simulation shows the frequency response of the 3-Stage Opamp. It has 82dB of flatband gain and 71° of phase margin.

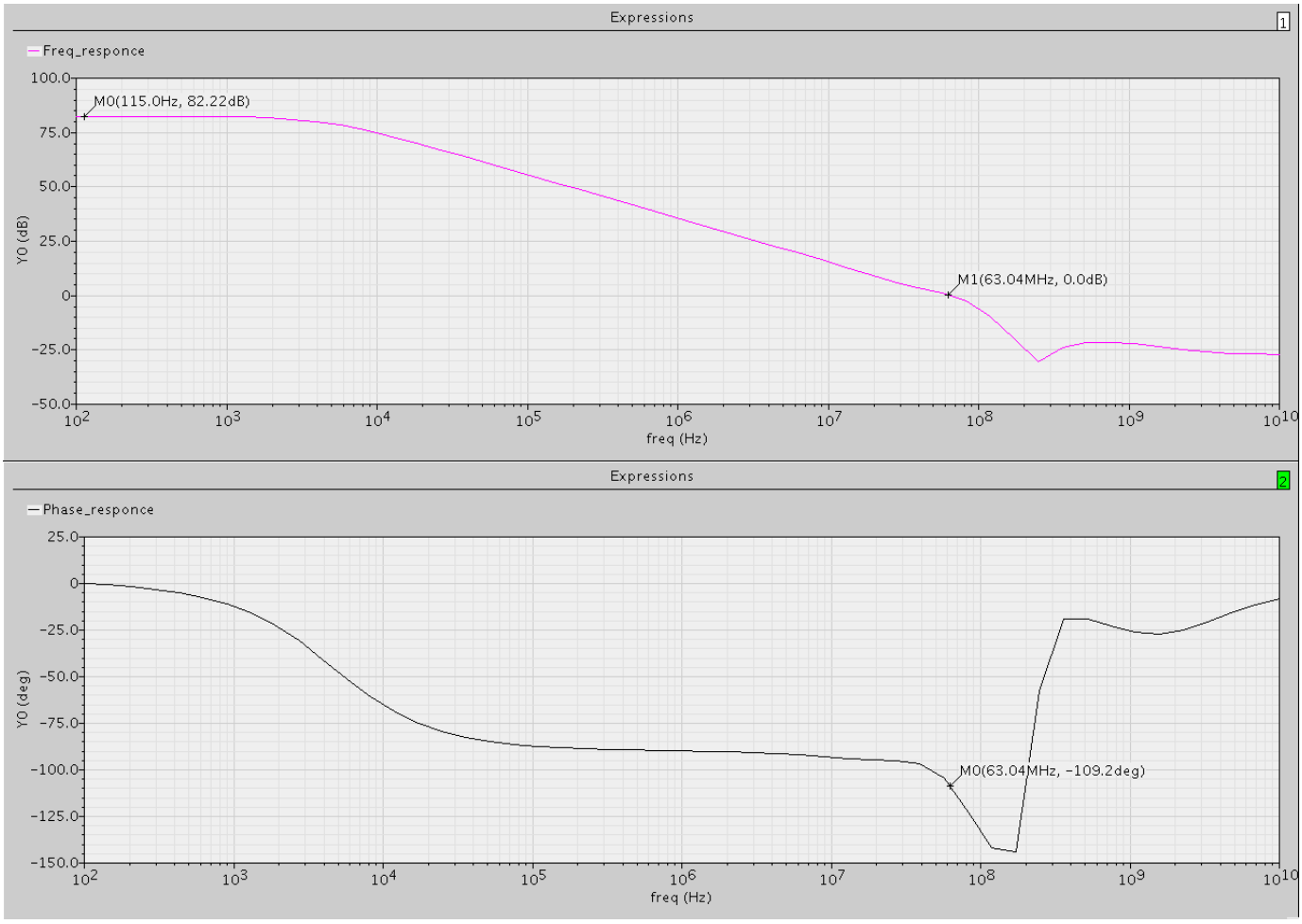

Fig. 11. Opamp Frequency Response.

This simulation shows the output of the opamp to a square wave input.

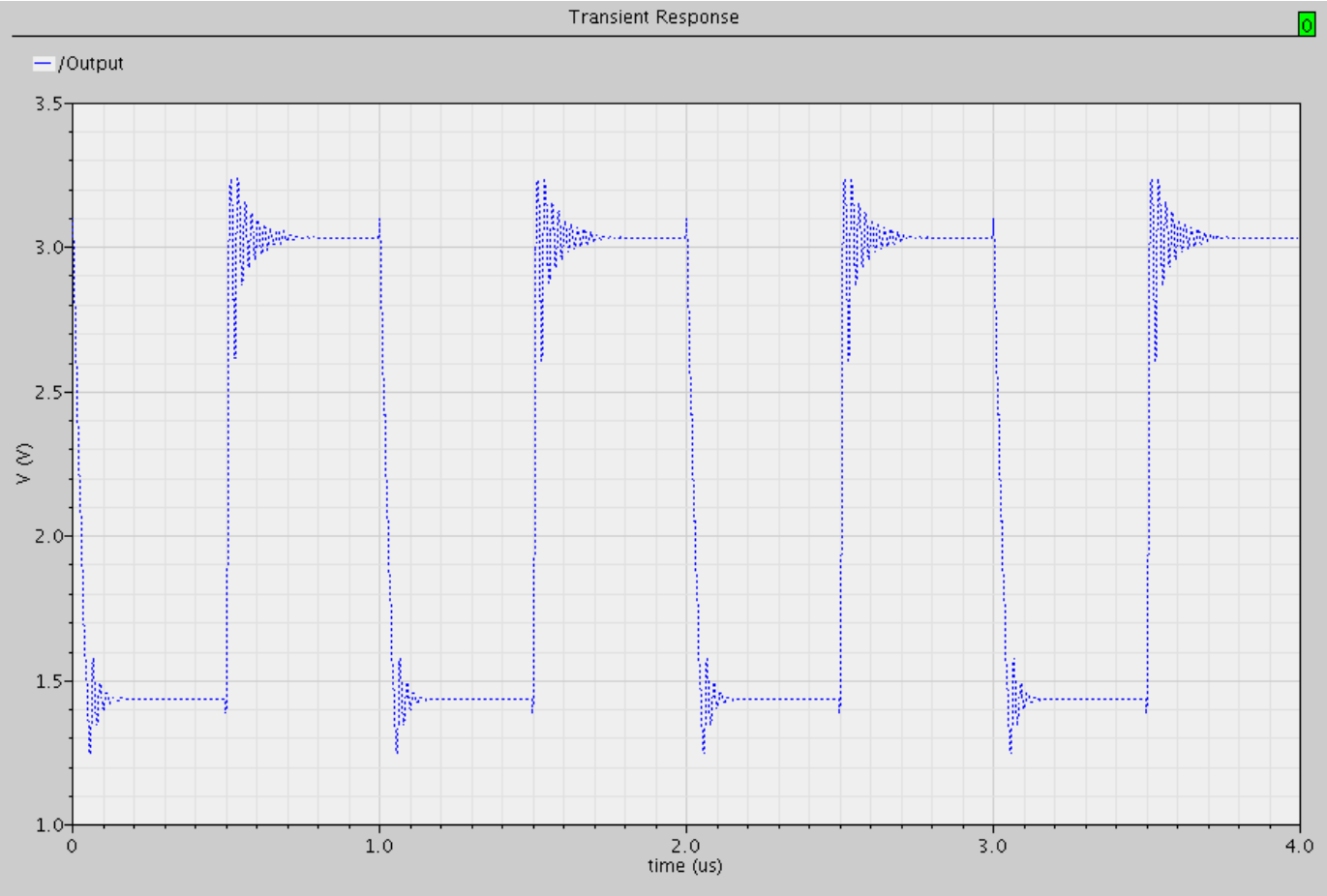

Fig. 12. Opamp Output.

2) DAC Performance: This simulation shows the individual steps of the DAC output along with the input digital signals b_0 - b_3.

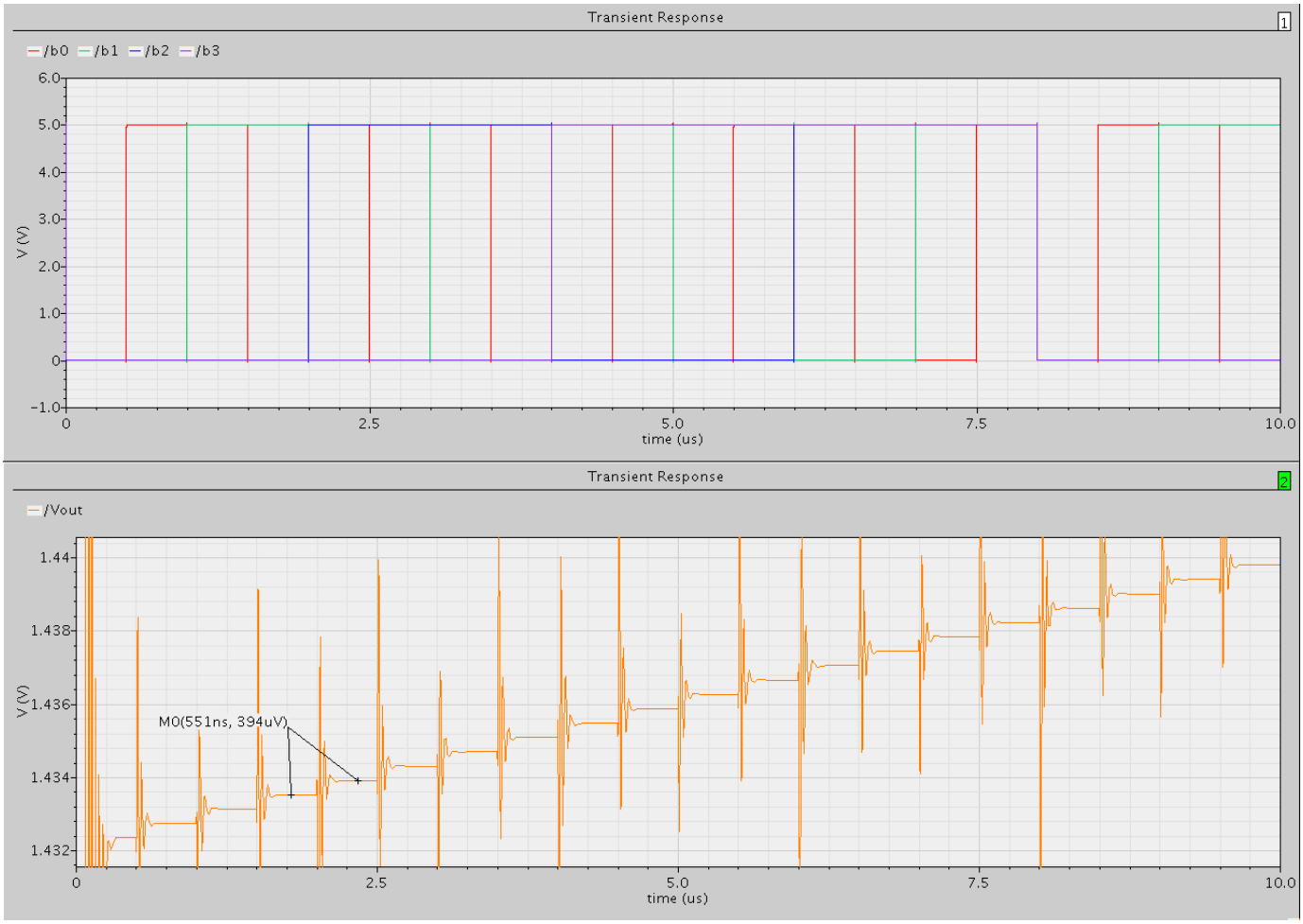

Fig. 13. Individual DAC Step Response.

This siumulation shows the DAC cylcling through all of its steps.

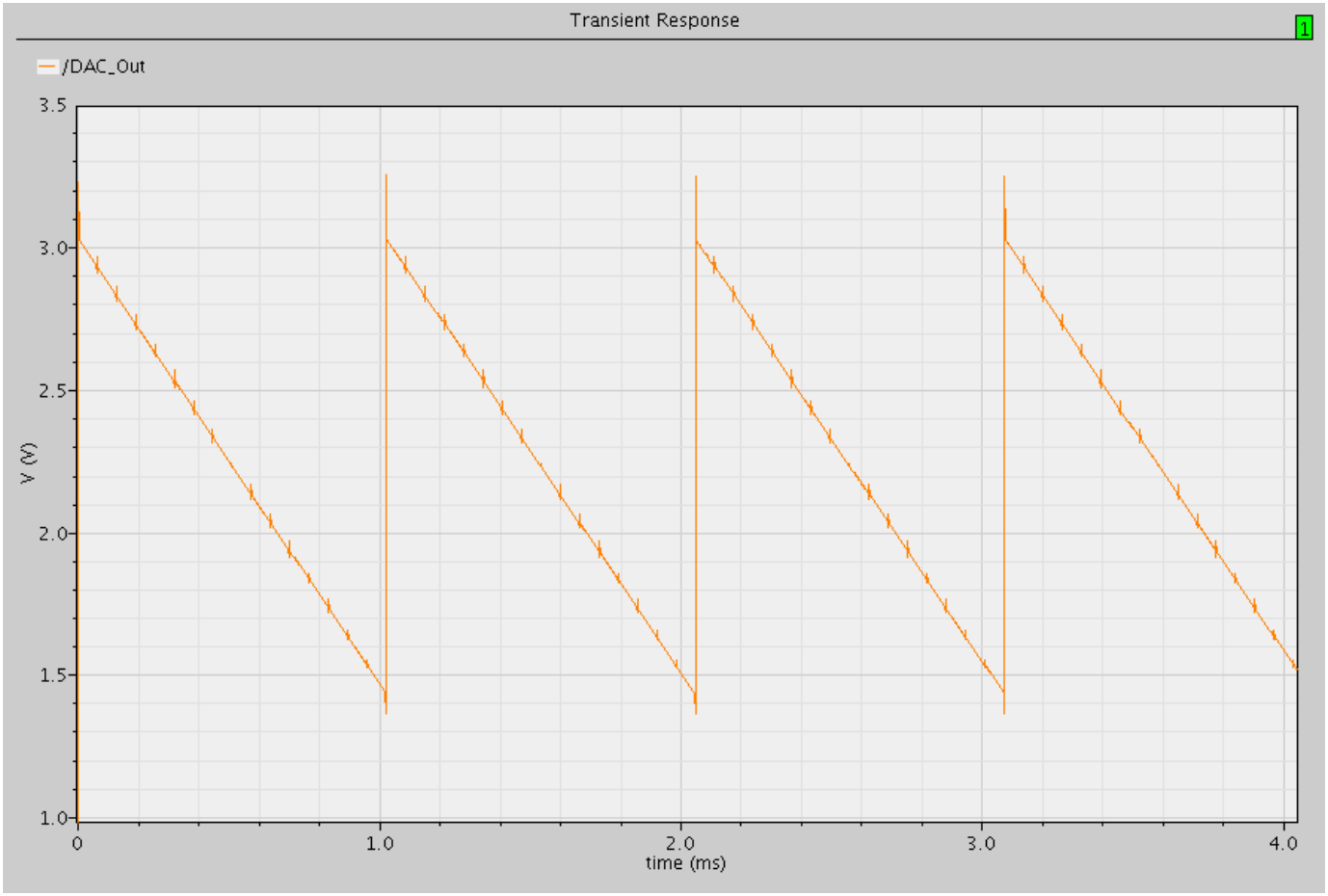

Fig. 14. DAC Ramp Response.

3) 32KHz DAC Sine Output: This simulation shows the output and spectral view of a 32KHz sine wave from the DAC. The output of the DAC was passed through a low pass filter to smooth out the edges.

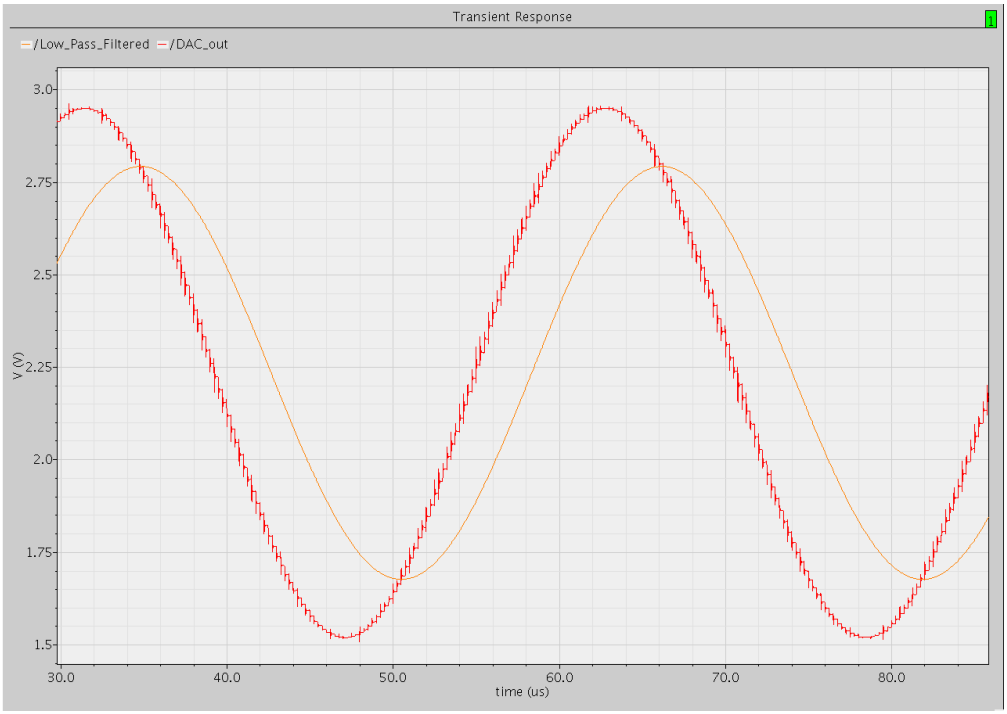

Fig. 15. 32KHz Sine Wave.

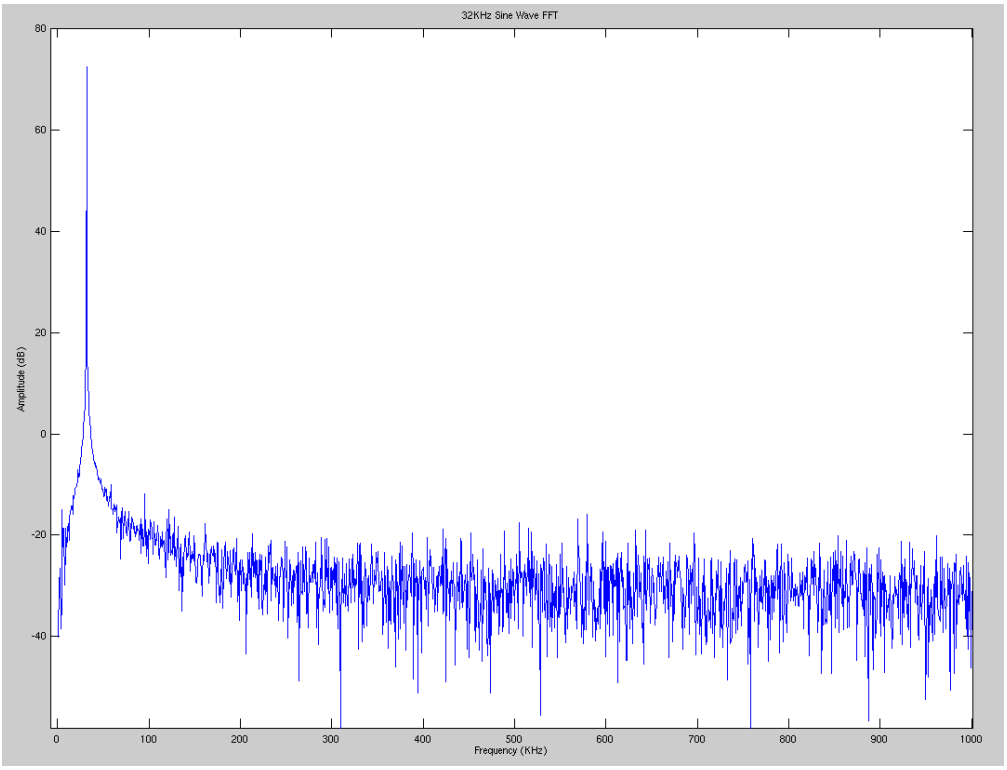

Fig. 16. 32KHz Sine Wave FFT.

4) 250KHz DAC Sine Output: This simulation shows the output and spectral view of a 250KHz sine wave from the DAC. The output of the DAC was passed through a low pass filter to smooth out the edges.

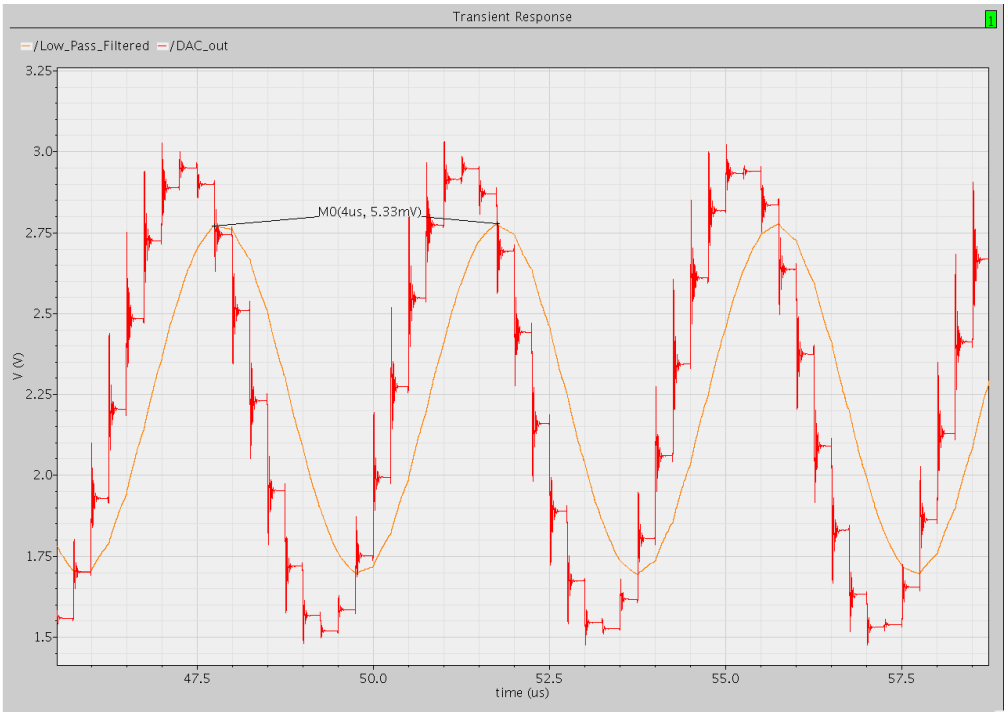

Fig. 17. 250KHz Sine Wave.

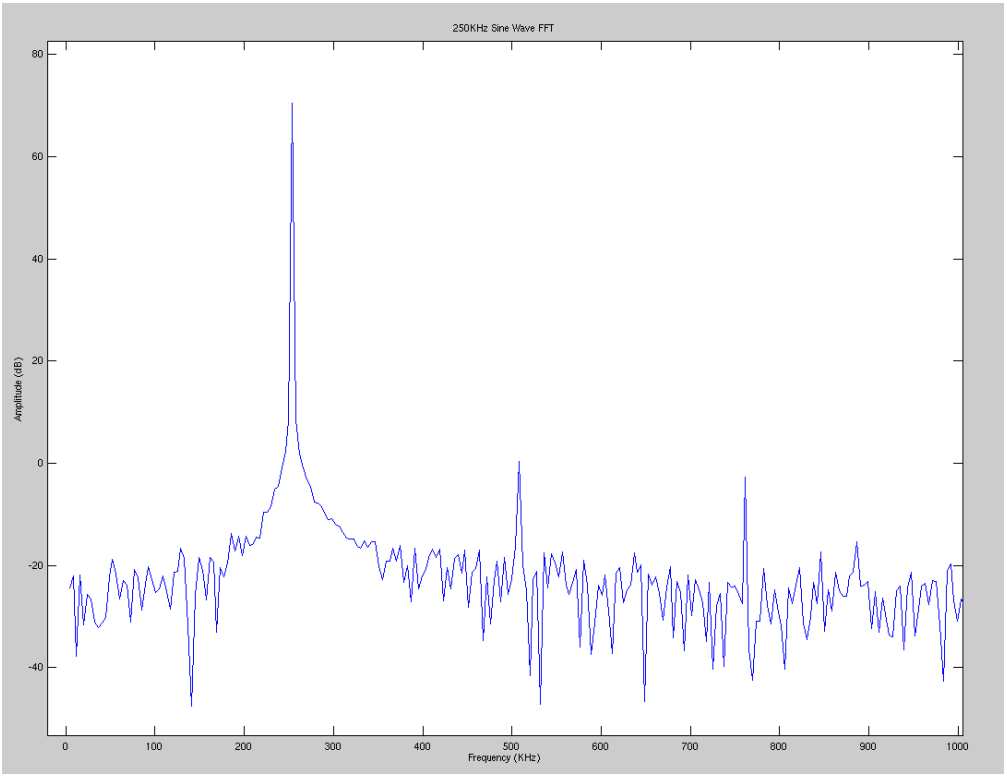

Fig. 18. 250KHz Sine Wave FFT.

5) Power Dissipation: The following simulations show the power dissipation of the design for various operating conditions.

- *Static Power:* Power Consumption of powered device in a idle state.
  - 70.52mW
- *Isolated Opamp Alone:* Average Power Consumption of isolated opamp.
  - 92.9mW
- *Single DAC:* Average Power Consumption of a single DAC running alone.
  - 73.4mW
- *Both DACs:* Average Power Consumption of Both DACs running.
  - 78.2mW
- *All Devices:* Average Power Consumption of Both DACs and isolated opamp running.
  - 102.6mW

D. Verification

Several procedures were used to verify the top-level functionality of the DAC. Before layout, all components were simulated and verified functional. All higher level cells were tied together and the output at this level was verified. During layout of the circuit, Design Rule Checks (DRC) were performed on individual cells. Layout versus Schematic (LVS) was run to verify that the circuit components generated during layout logically matched the components in the original schematic.

'The net-lists match'

The top level layout passed DRC checking with 0 errors.

III.

A. Test Procedures and Protocols

The following section discusses procedures for testing of the physically implemented chip.

1) Chip Pin Out: The following table shows a pin out of the chip.

Pin #	Purpose	Pin #	Purpose
1	DAC_1 Out	21	DAC_2 Out
2	DAC_1 b0	22	DAC_2 b0
3	DAC_1 b1	23	DAC_2 b1
4	DAC_1 b2	24	DAC_2 b2
5	DAC_1 b3	25	DAC_2 b3
6	DAC_1 b4	26	DAC_2 b4
7	DAC_1 b5	27	DAC_2 b5
8	DAC_1 b6	28	DAC_2 b6
9	DAC_1 b7	29	DAC_2 b7
10	DAC_1 b8	30	DAC_2 b8
11	DAC_1 b9	31	DAC_2 b9
12	DAC_1 b10	32	DAC_2 b10
13	DAC_1 b11	33	DAC_2 b11
14	R_{20k_1}	34	NC
15	R_{20k_2}	35	NC
16	NC	36	NC
17	Opamp -	37	NC
18	Opamp +	38	NC
19	Opamp Out	39	NC
20	GND	40	VDD

TABLE II
PIN OUT

2) Test 1: Static Power Dissipation: This test is a simple test to determine if there are power supply shorts to ground.

- **Procedure**
  - Tie output pins low with dummy load of 100kΩ, input pins to ground.
  - Ramp VDD supply to 5V, observing current draw from power supply.
  - If current draw is excessive, it most likely means shorts in circuit design or faulty device. If similar results are found on multiple devices suspect a short in design.

- If current draw is not excessive, compare results to that of section II-C.5

3) Test 2: Resistance Verification: This test verifies the on-chip resistors used in the R-2R network across temperature. No power need be applied to device for this test.

- **Procedure**
  - Measure resistance of the isolated $20k\Omega$ resistor on pins 14 and 15.
  - Repeat over various temperatures and observe any changes.

4) Test 3: Opamp Operation: This test verifies the opamp design used in the DAC.

- **Procedure**
  - Tie output pins of both DACs low with dummy load of 100kΩ, and DAC input pins to ground.
  - Connect isolated opamp (pins 17-19) as shown in Figure 19
  - Drive input with a 0-5V square wave at 1MHz.
  - Observe output on oscilloscope and compare to Figure 12 on page 12.
  - Observe power consumption and compare to that of section II-C.5.

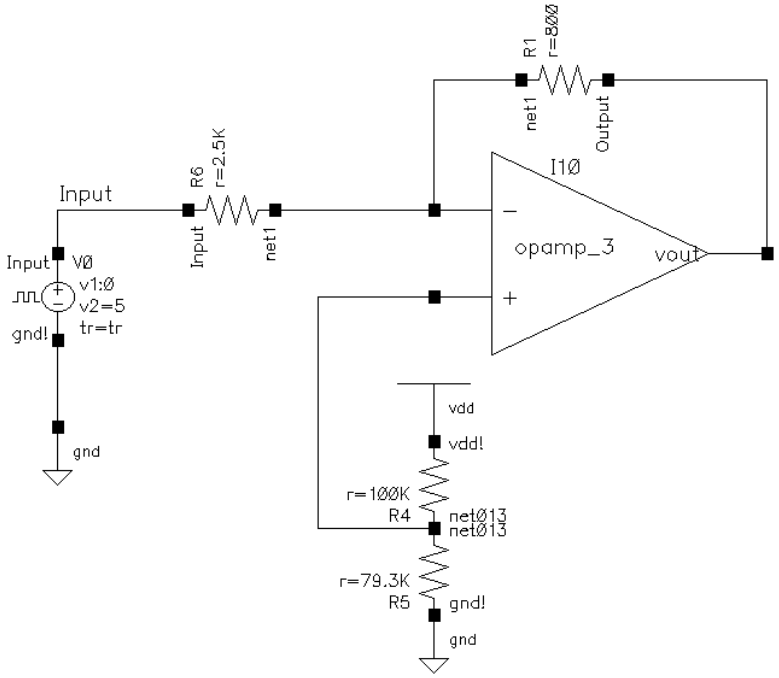

Fig. 19. Opamp Test Bench Schematic.

5) Test 4: DAC Operation: This test verifies the DAC design. This test can be done on either DAC_1, DAC_2, or both, adjust the pins used accordingly.

- **Procedure**
  - Tie output pins of isolated Opamp and DAC not in use low with a dummy load of 100kΩ.
  - Tie input pins of isolated Opamp and DAC not in use to ground.
  - Apply 0-5V binary input signal to input pins.
  - Observe output of DAC on oscilloscope and compare to Figures 15 and 17. A low pass filter may be applied to output to smooth edges.
  - Observer power consumption and compare to that of section II-C.5.

IV.

A. Summary and Conclusion

Using a .5μm process, a 1.5mm x 1.5mm die, and 40 pin package, two 12-bit DACs were constructed. Simulations with extracted parasitics and package models indicate the device functions according to specs. Fabrication of the device will reveal if the design operates as expected. The design is modular enough that it could be used in a number of applications that need a relatively high speed 12-bit resolution DAC.

B. Suggestions For Future Work

Future improvements to the design could be done in increasing input clock frequency. The current clock speed is due to settling times of the opamp. So improvements of the opamp design would focus on increasing settling time and output range.

Other improvements would be to further optimize the layout to take up less space. The number of DACs possible in the package is currently limited by the number of pins on the package, but if space had been available, other DSP circuitry could have been implemented.

Finally the biggest constraint for the design was time. I would have preferred to take the class during the summer when time would not be such a issue and the design could have been much improved.

C. Biography

Jason Beaulieu was born in Lewiston, Maine. He graduated from Oak Hill High School in Sabattus, Maine in 2003. He is currently a fourth-year student at the University of Maine studying toward a BS in Electrical Engineering and will be graduating December, 2007. He has spent three summers as an intern for Tundra Semiconductor, a systems interconnect company in South Portland, Maine. His interests include analog, digital, and mixed signal circuit design.

V.

A. Appendix A

1) Schematics: .

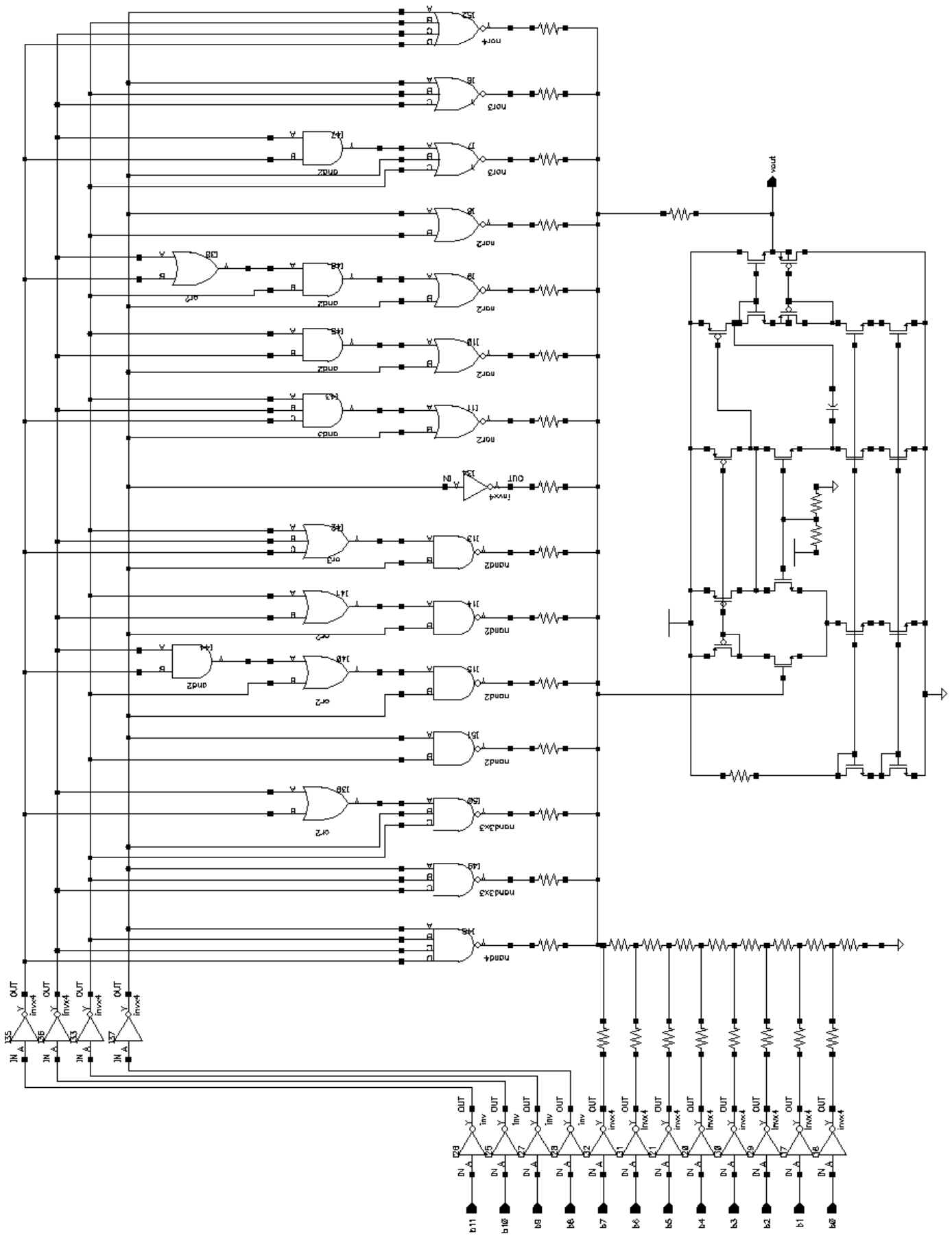

Fig. 20. DAC Top Level Schematic

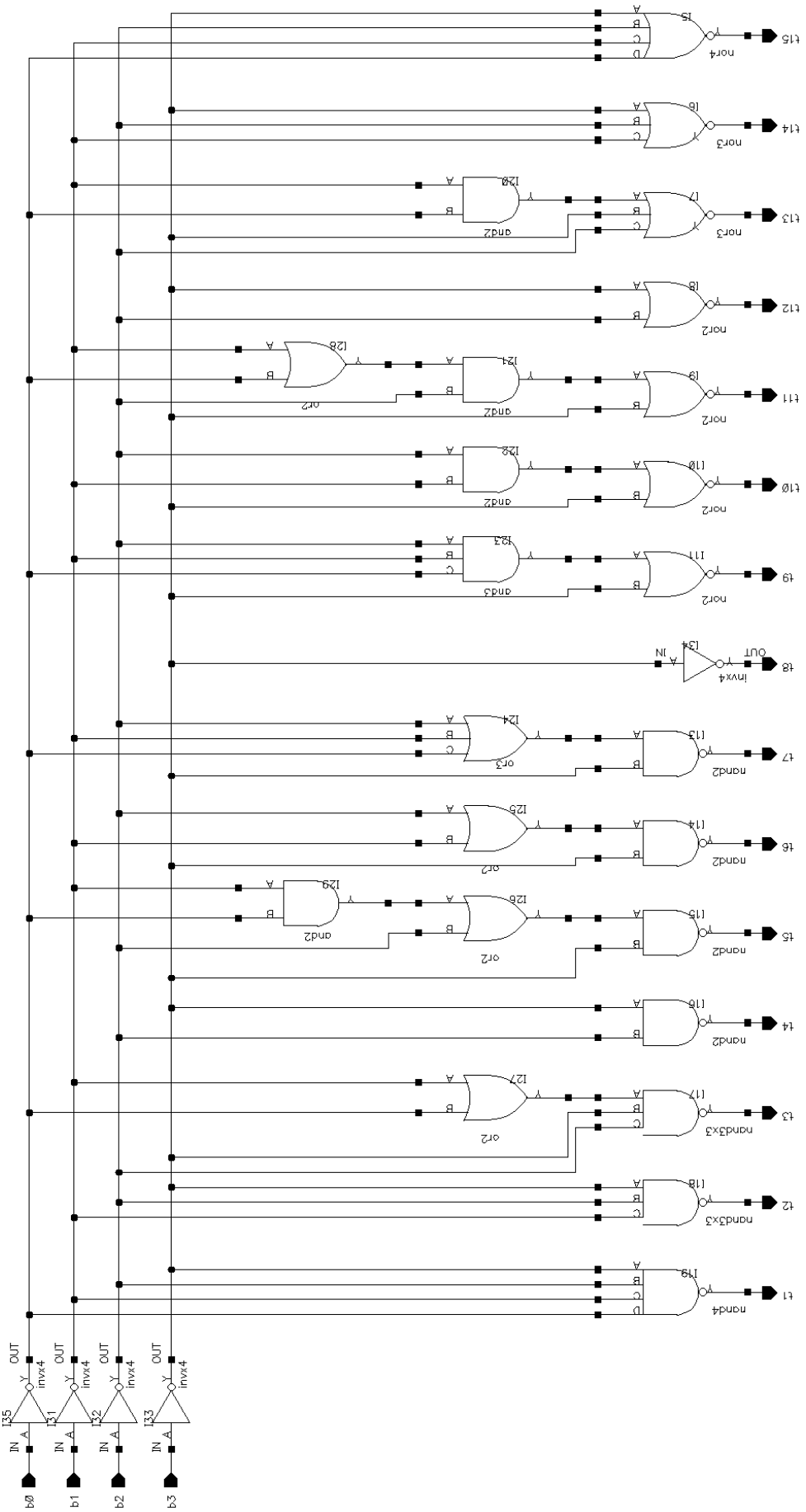

Fig. 21. 4-bit Thermometer Decoder Schematic

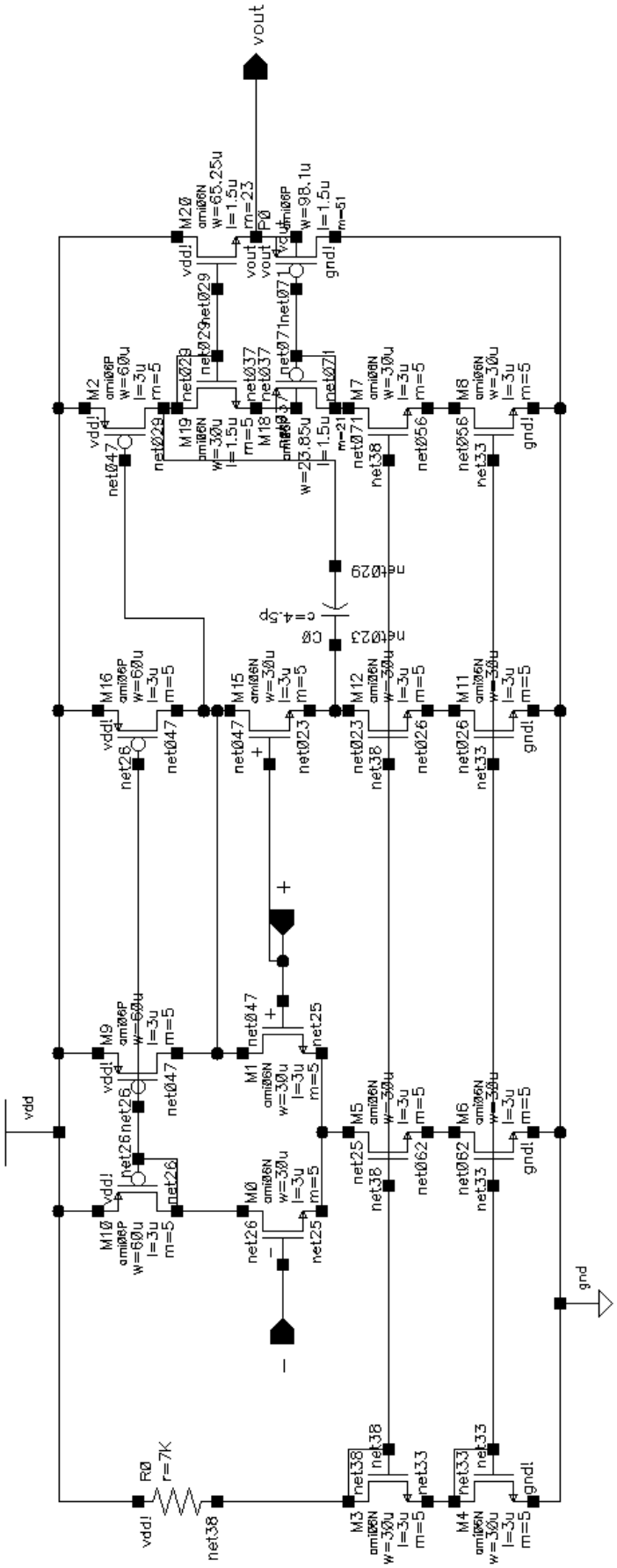

Fig. 22. 3-Stage Opamp Schematic

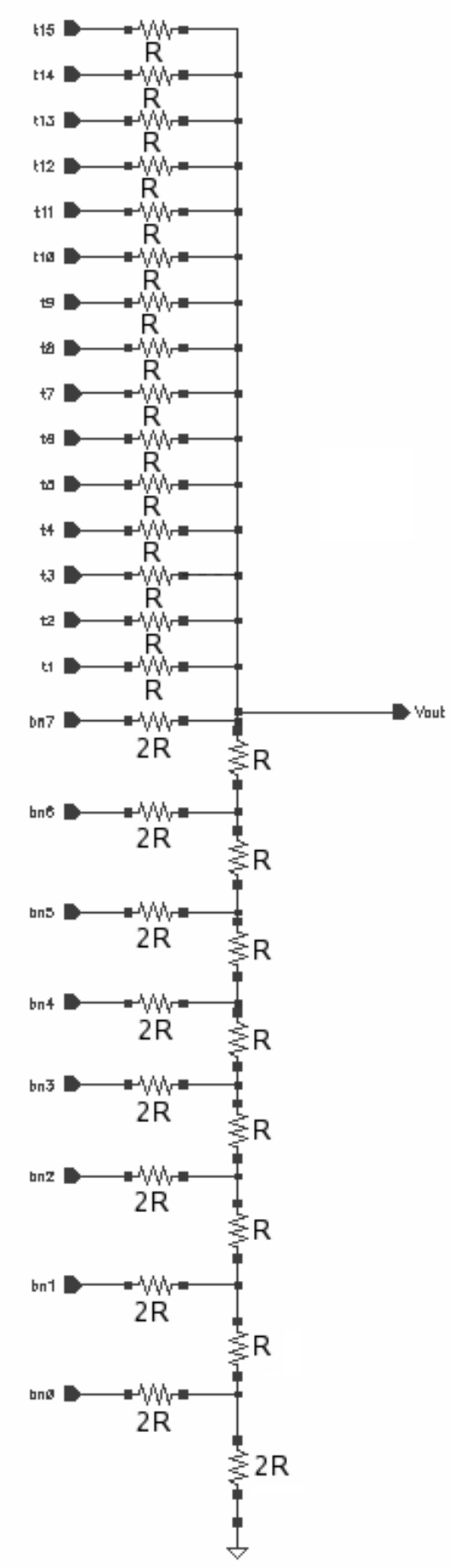

Fig. 23. Resistor Ladder Schematic

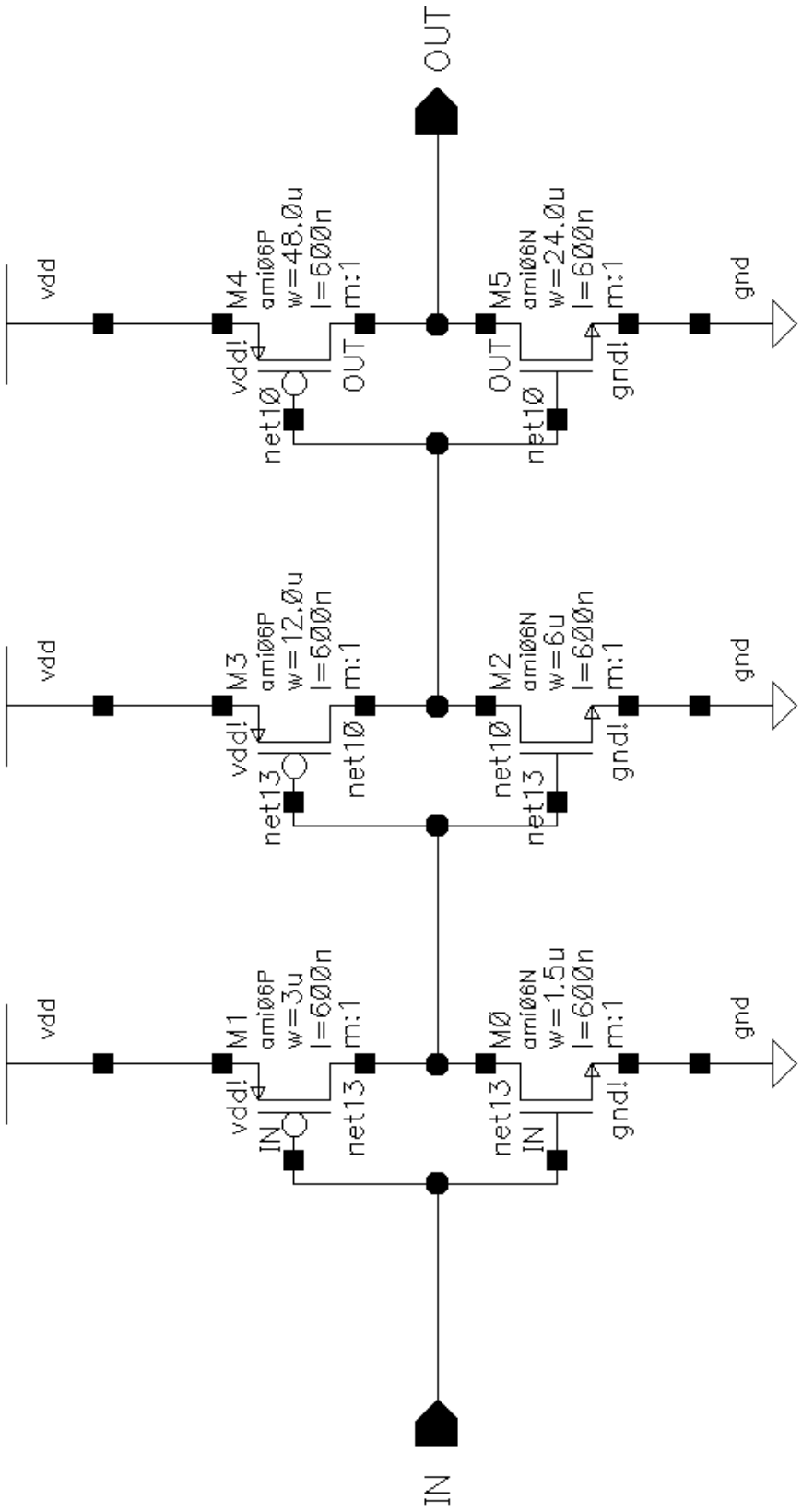

Fig. 24. 4x Digital Buffer Schematic

2) *Physical Design:* .

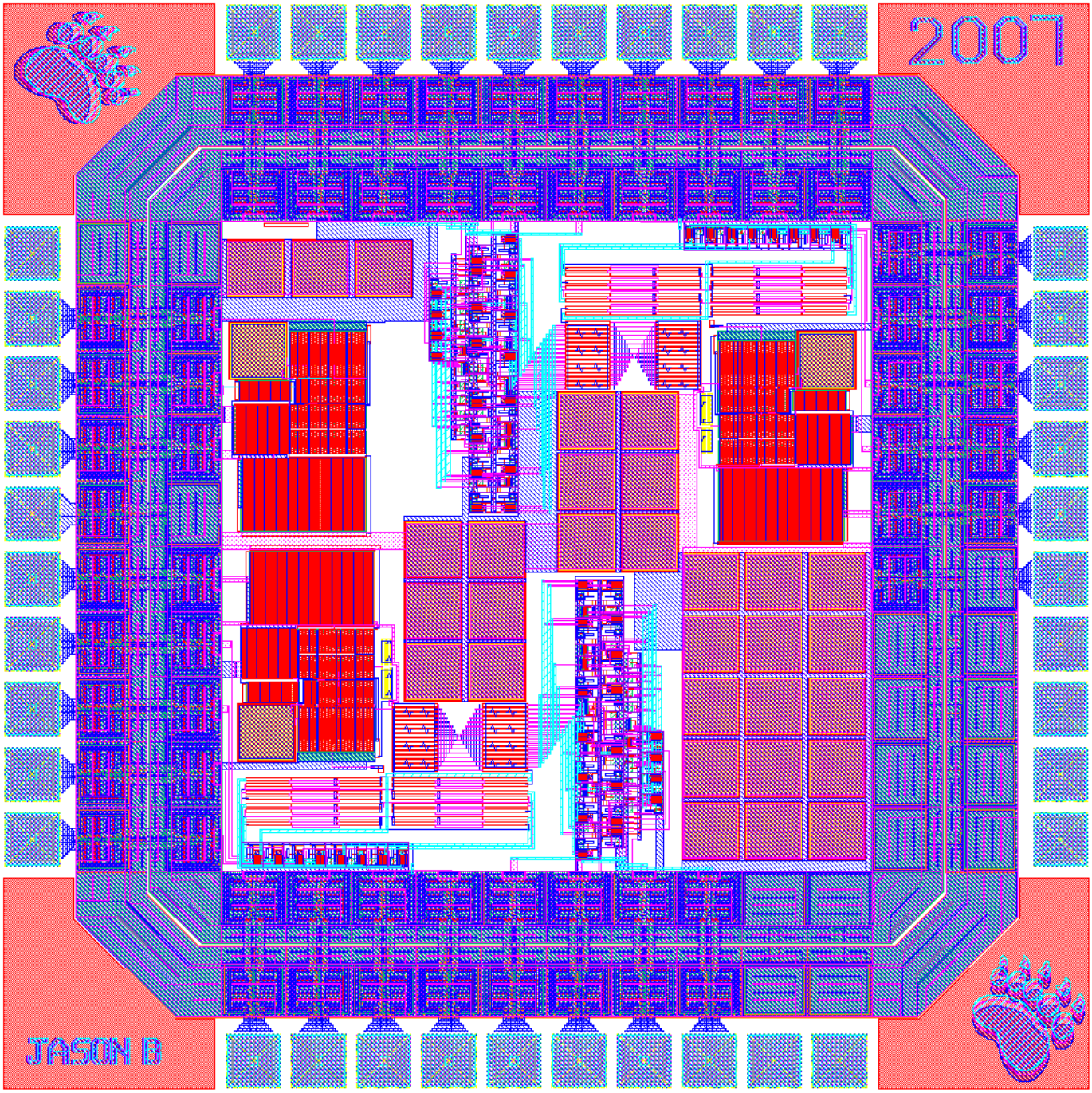

Fig. 25. Top Level Layout.

3) Packaged Device: .

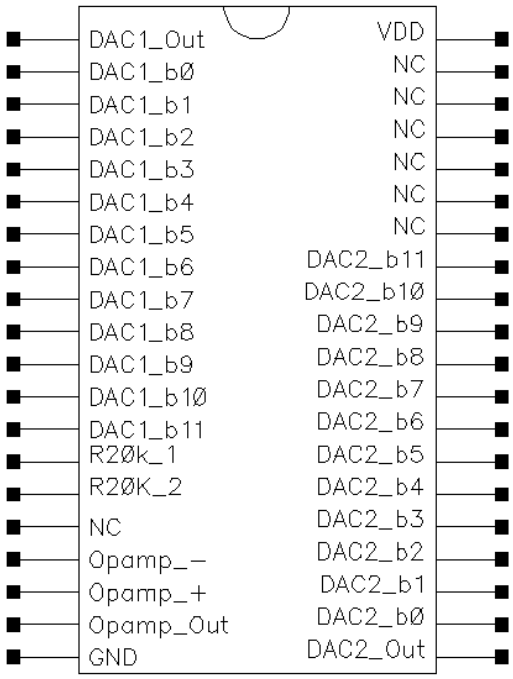

Fig. 26. Package Pinout

Pin #	Purpose
1	DAC_1 Out
2	DAC_1 b0
3	DAC_1 b1
4	DAC_1 b2
5	DAC_1 b3
6	DAC_1 b4
7	DAC_1 b5
8	DAC_1 b6
9	DAC_1 b7
10	DAC_1 b8
11	DAC_1 b9
12	DAC_1 b10
13	DAC_1 b11
14	R_{20k_1}
15	R_{20k_2}
16	NC
17	Opamp -
18	Opamp +
19	Opamp Out
20	GND

Pin #	Purpose
21	DAC_2 Out
22	DAC_2 b0
23	DAC_2 b1
24	DAC_2 b2
25	DAC_2 b3
26	DAC_2 b4
27	DAC_2 b5
28	DAC_2 b6
29	DAC_2 b7
30	DAC_2 b8
31	DAC_2 b9
32	DAC_2 b10
33	DAC_2 b11
34	NC
35	NC
36	NC
37	NC
38	NC
39	NC
40	VDD

TABLE III
PIN OUT