

David E. Kotecki, Ph.D.

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EDUCATION

Ph.D., Engineering Applied Science, University of California Davis, Davis, CA (1988)

M.S., Engineering Applied Science, University of California Davis, Davis, CA (1984)

B.E.E., Electrical Engineering, *magna cum laude*, University of Dayton, Dayton, OH (1981)

PROFESSIONAL STATEMENT

U.S. patent agent, associate professor of electrical and computer engineering, inventor, and researcher. Over thirty years experience working with start-up companies, multinational corporations, government laboratories, and academia. More than fifteen years experience as an educator. Authored or co-authored more than 70 peer-reviewed research papers; awarded 60 U.S. patents. Interested in microelectronics, circuits, advanced semiconductor devices, patent preparation and prosecution, patent portfolio development, and IP education. Areas of technical expertise include: electronics, circuits, micro- and nano-electronics, integrated circuit design, RF electronics, semiconductor materials and processes, DRAM, semiconductor memory, and process integration.

EMPLOYMENT

University of Maine, Orono, ME (1999 –)

Associate Professor, Electrical and Computer Engineering

Blue Hill Innovation LLC, Orono, ME (2010 –)

Patent Agent (USPTO Registration #72,338) and **Consultant**

IBM, Microelectronics Division, Hopewell Junction, NY (1988–1999)

Senior Engineer, DRAM Development Alliance, 1Gbit Integration Department (1997–1999); **Advisory Engineer**, Semiconductor Research & Development Center, Advanced Process Technology Department (1992–1997); **Staff Engineer**, Semiconductor Development Laboratory, CVD Technology Development Department (1988–1992)

Lawrence Livermore National Laboratory, Livermore, CA (1981–1988)

Student Engineer, Physics Department, (1984–1988); **Electronics Engineer**, Diagnostic Development Group, (1981–1984)

MacAulay Brown, Inc., Fairborn, OH (1980–1981)

Assistant Programmer (part-time)

NASA, Goddard Space Flight Center, Greenbelt, MD (1978–1980)

Engineering Intern, Instrument Electro-Optics Branch

AWARDS

Graduate Faculty Mentor Award, University of Maine (2008, 2015); Award for Service, IEEE Maine Section (2014); Dean's Award of Excellence, University of Maine (2005); Teaching and Technology Fellowship, University of Maine (2001) and 15 Invention Achievement Awards, IBM (1990-2000).

PROFESSIONAL AND HONORARY SOCIETIES

IEEE (senior member), American Physical Society (APS), National Association of Patent Practitioners (NAPP), American Society for Engineering Education (ASEE); *Tau Beta Pi*, (The Engineering Honor Society) and *Eta Kappa Nu*, (The Electrical and Computer Engineering Honor Society of the IEEE).

PROFESSIONAL AND PUBLIC SERVICE

Tau Beta Pi, (The Engineering Honor Society) Maine Alpha Chapter: Advisor (2006–2007, 2016–present); Chief Advisor (2008–2015).

IEEE, Maine Section: Secretary (2001); Member at Large (2002); Vice Chair (2003); Chair (2004) and Treasurer (2006–2009); IEEE, University of Maine Student Branch Co-counselor (2003–2011).

Journal Reviewer: IEEE Transactions on Circuits & Systems; IEEE Electron Device Letters; IEEE Microwave & Wireless Components Letters; IEEE Journal of Solid State Circuits; IEEE Journal on Emerging and Selected Topics in Circuits and Systems; Applied Physics Letters; Journal on Educational Resources in Computing; Journal of the American Ceramic Society; Journal of Vacuum Science & Technology; IET Circuits, Devices & Systems; Journal of Circuits, Systems, and Computers; and Analog Integrated Circuits and Signal Processing.

Proposal Reviewer: NSF panelist (2016), Department of Defense SMART Scholarship panelist (2014–2015), Natural Sciences and Engineering Research Council of Canada (NSERC), and Civilian Research & Development Foundation (CRDF).

Book Reviewer: Prentice Hall and Oxford University Press.

University of Maine: Faculty Senator (2004–2007); Graduate School Executive Committee (2011); University of Maine New Faculty Mentor (2006–2009); Department of Electrical & Computer Engineering (ECE) Graduate Program Coordinator (2008–2011); Electrical Engineering Curriculum Committee Chair (2007–2011); Microelectronics Scholarship Consortium Chair (1999–2011); ECE Faculty Search Committee Chair (2000, 2001, 2006), ECE Graduate Board Representative (2000–2002, 2008–2011), and Member, Engineering and Science Building Committee (2001).

TEACHING EXPERIENCE (UNIVERSITY OF MAINE)

ECE 209: Fundamentals of Electric Circuits

ECE 210: Electric Circuits I

ECE 214: Electric Circuits Laboratory

ECE 342: Electronics I

ECE 444: Analog Integrated Circuit Design

ECE 445: Digital Integrated Circuit Design

ECE 464: Microelectronics Science and Engineering

ECE 512: Linear Systems Analysis

ECE 543: Microelectronic Devices I

ECE 643: Microelectronics Devices II

ECE 547: Integrated Circuit Design and Layout

ECE 548: Integrated Circuit Characterization and Testing

ECE 598: Special Topics in Integrated Circuit Design

PUBLICATIONS

1. P. Gunturi and D. E. Kotecki, "Analysis and implementation of a gaussian addition transmitter (GAT) for increased spectral efficiency," *Springer, Wireless Personal Communications*, pp. 1–12, 2018. Available: <https://doi.org/10.1007/s11277-018-5851-x>
2. P. Gunturi, N. W. Emanetoglu, and D. E. Kotecki, "A 250-Mb/s data rate IR-UWB transmitter using current-reused technique," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4255–4265, Nov 2017. Available: <https://doi.org/10.1109/tmtt.2017.2695189>
3. P. Gunturi and D. E. Kotecki, "IR-UWB BPK transmitter optimized for maximum distance of transmission," in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '15)*, Fort Collins, Colorado, Aug 2015, pp. 1–4. Available: <https://doi.org/10.1109/MWSCAS.2015.7282069>
4. P. Gunturi and D. E. Kotecki, "A PA for MBOFDM-UWB and IR-UWB transmitters," in *Proc. IEEE International Midwest Symposium on Circuits and Systems (MWSCAS '15)*, Fort Collons, Colorado, Aug 2015, pp. 1–4. Available: <https://doi.org/10.1109/MWSCAS.2015.7282193>
5. P. Gunturi and D. E. Kotecki, "Temperature and supply voltage insensitive OOK transmitter for outdoor UWB communications," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 733–736. Available: <https://doi.org/10.1109/mwscas.2014.6908519>
6. P. Gunturi and D. E. Kotecki, "A wideband Class E PA with more than 40% PAE and 800 MHz bandwidth," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 725–728. Available: <https://doi.org/10.1109/mwscas.2014.6908517>
7. P. Gunturi and D. E. Kotecki, "Class E power amplifiers with tuned RC output matching circuit," in *IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, San Diego, California, Sept. 2013.
8. Y. Lin and D. E. Kotecki, "A 126.9-132.4 GHz wide-locking low-power frequency-quadrupled phase-locked loop in 130nm SiGe BiCMOS," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '12)*, Boise, Idaho, Aug. 2012, pp. 754–757. Available: <https://doi.org/10.1109/mwscas.2012.6292130>
9. Y. Lin and D. E. Kotecki, "A 290 GHz frequency quadrupled SiGe voltage-controlled oscillator," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '11)*, Seoul, Korea, Aug. 2011, pp. 1–4. Available: <https://doi.org/10.1109/mwscas.2011.6026637>
10. Y. Lin and D. E. Kotecki, "2.9 – 30.3 GHz fourth-harmonic voltage-controlled oscillator in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 401–404. Available: <https://doi.org/10.1109/icecs.2010.5724536>
11. Y. Lin and D. E. Kotecki, "A voltage-controlled oscillator with a 0.8–13.4 GHz tuning range in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference*

- on *Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 431–434. Available: <https://doi.org/10.1109/icecs.2010.5724540>
12. Y. Lin and D. E. Kotecki, “A 312GHz fourth-harmonic voltage-controlled oscillator (VCO) designed using 130nm SiGe BiCMOS technology,” in *Proc. IEEE International Conference on Electronics, Circuits and Systems, (ICECS '09)*, Yasmine, Tunisa, Dec. 2009, pp. 747–750, **(Best student paper award.)**. Available: <https://doi.org/10.1109/icecs.2009.5410799>
 13. B. C. Gierhart, D. G. Howitt, S. J. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, “Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA,” *Sensors and Actuators, B: Chemical*, vol. 132, pp. 593–600, June 2008. Available: <https://doi.org/10.1016/j.snb.2007.11.054>
 14. R. H. Bethel and D. E. Kotecki, “Low voltage BiCMOS circuit topologies for the design of a 19GHz, 1.2V, 4-bit accumulator in silicon-germanium,” in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 1127–1130. Available: <https://doi.org/10.1109/icecs.2007.4511193>
 15. C. R. Kenney and D. E. Kotecki, “Microelectronic magnetic flux sensor for hearing aid application,” in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 6–9. Available: <https://doi.org/10.1109/icecs.2007.4510917>
 16. B. Gierhart, D. Howitt, S. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, “Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA,” in *Proc. 6th IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers '07)*, Lyon, France, June 2007, pp. 399–402. Available: <https://doi.org/10.1109/sensor.2007.4300152>
 17. S. Manandhar, S. E. Turner, and D. E. Kotecki, “36-GHz, 16x6 bit ROM in InP DHBT technology,” *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 451–456, Feb. 2007. Available: <https://doi.org/10.1109/jssc.2006.889361>
 18. Z. Zhu, R. Tumati, S. Collins, R. Smith, and D. E. Kotecki, “A low-noise, low-offset operational amplifier in 0.35 μ m technology,” in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 624–627. Available: <https://doi.org/10.1109/icecs.2006.379866>
 19. S. Manandhar, S. E. Turner, and D. E. Kotecki, “A 20-GHz and 46-GHz, 32x6-bit ROM for DDS application in InP DHBT technology,” in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 1003–1007. Available: <https://doi.org/10.1109/icecs.2006.379960>
 20. S. E. Turner and D. E. Kotecki, “Direct digital synthesizer with sine-weighted DAC at 32 GHz clock frequency in InP DHBT technology,” *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2284–2290, Oct. 2006. Available: <https://doi.org/10.1109/jssc.2006.881552>
 21. D. E. Kotecki, T. Monk, V. Tkachuk, Z. Zhu, A. Delic-Ibukic, and S. E. Turner, “Custom analog and mixed-signal integrated circuit design at the undergraduate level – a university/industry collaboration,” in *Proc. 6th International Workshop on Microelectronics Education*, Stockholm, Sweden, June 2006, pp. 47–50, ISBN: 91-7178-402-0.

22. S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with ROM-less architecture at 13-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, no. 5, pp. 296–298, May 2006. Available: <https://doi.org/10.1109/lmwc.2006.873490>
23. S. E. Turner, R. B. Elder, Jr., D. S. Jansen, and D. E. Kotecki, "4-bit adder-accumulator at 41-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 15, no. 3, pp. 144–146, Mar. 2005. Available: <https://doi.org/10.1109/lmwc.2005.844199>
24. S. E. Turner and D. E. Kotecki, "Benchmark results for high-speed 4-bit accumulators implemented in Indium Phosphide DHBT technology," *International Journal of High Speed Electronics and Systems*, vol. 14, no. 3, pp. 646–651, Sept. 2004. Available: <https://doi.org/10.1142/s0129156404002612>
25. F. Yang, D. E. Kotecki, G. Bernhardt, and M. Call, "Electrical and structural characterization of HfO₂ MIM capacitors," in *Novel Materials and Processes for Advanced CMOS*, *Proc. Mater. Res. Soc.*, vol. 745, 2003, pp. 203–208. Available: <https://doi.org/10.1557/proc-745-n5.16>
26. J. L. Cousins and D. E. Kotecki, "Simulation of the variability in microelectronic capacitors having polycrystalline dielectrics," *IEEE Electron Device Lett.*, vol. 16, no. 5, pp. 267–269, May 2002. Available: <https://doi.org/10.1109/55.998872>
27. R. Schmitt, D. McCann, B. Marquis, and D. E. Kotecki, "Dielectric relaxation of WO₃ thick films from 10 Hz to 1.8 GHz," *J. Appl. Phys.*, vol. 91, no. 10, pp. 6775–6777, May 2002. Available: <https://doi.org/10.1063/1.1468276>
28. J. L. Cousins and D. E. Kotecki, "Simulation of the variability in next-generation microelectronic capacitors with polycrystalline dielectrics," in *Ferroelectric Thin Films X*, *Proc. Mater. Res. Soc.*, vol. 695, 2002, pp. 247–252. Available: <https://doi.org/10.1557/proc-688-c7.24.1>
29. K. L. Saenger, G. Costrini, D. E. Kotecki, K. Kwietniak, and P. C. Andricacos, "Submicrometer platinum electrodes by through-mask plating," *J. Electrochem. Soc.*, vol. 148, no. 11, pp. 758–761, Nov. 2001. Available: <https://doi.org/10.1149/1.1410971>
30. C. C. Cabral, Jr., K. L. Saenger, D. E. Kotecki, and J. M. Harper, "Optimization of Ta-Si-N thin films for use as oxidation-resistant diffusion barriers," *J. Mater. Res. Soc.*, vol. 15, no. 1, pp. 194–198, Jan. 2000. Available: <https://doi.org/10.1557/jmr.2000.0031>
31. D. E. Kotecki, J. D. Baniecki, H. Shen, R. B. Laibowitz, K. L. Saenger, J. J. Lian, T. M. Shaw, S. D. Athavale, C. C. Cabral, Jr., P. R. Duncombe, M. Gutsche, G. Kunkel, Y.-J. Park, Y.-Y. Want, and R. Wise, "(Ba,Sr)TiO₃ dielectrics for future stacked-capacitor DRAM," *IBM J. of Res. and Dev.*, vol. 43, no. 3, pp. 367–382, May 1999. Available: <https://doi.org/10.1147/rd.433.0367>
32. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, K. L. Saenger, P. R. Duncombe, C. C. Cabral, Jr., D. E. Kotecki, H. Shen, J. Lian, and Q. Ma, "Effects of annealing conditions on charge loss mechanisms in MOCVD Ba_{0.7}Sr_{0.3}TiO₃ thin film capacitors," *J. European Ceramic Soc.*, vol. 19, no. 6-7, pp. 1457–1461, 1999. Available: [https://doi.org/10.1016/s0955-2219\(98\)00449-x](https://doi.org/10.1016/s0955-2219(98)00449-x)

33. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, P. R. Duncombe, D. E. Kotecki, H. Shen, J. Lian, and Q. Ma, "Nonlinear dielectric relaxation of Mn doped polycrystalline (Ba,Sr)TiO₃ thin films over the temperature range of 4.2 - 473K," in *Ferroelectric Thin Films VII, Proc. Mater. Res. Soc.*, vol. 541, 1999, pp. 23–28. Available: <https://doi.org/10.1557/proc-541-23>
34. M. Copel, J. D. Baniecki, P. R. Duncombe, D. E. Kotecki, R. Laibowitz, D. A. Neumayer, and T. M. Shaw, "Compensation doping of Ba_{0.7}Sr_{0.3}TiO₃ thin films," *Appl. Phys. Lett.*, vol. 73, no. 13, pp. 1832–1834, Sept. 1998. Available: <https://doi.org/10.1063/1.122297>
35. K. L. Saenger, A. Grill, and D. E. Kotecki, "Buried, self-aligned barrier layer structures for perovskite-based memory devices comprising Pt or Ir bottom electrodes on silicon-contributing substrates," *J. Appl. Phys.*, vol. 83, no. 2, pp. 802–813, Jan. 1998. Available: <https://doi.org/10.1063/1.366761>
36. J. D. Baniecki, R. L. Laibowitz, T. M. Shaw, P. R. Duncombe, D. A. Neumayer, D. E. Kotecki, H. Shen, and Q. Ma, "Dielectric relaxation of Ba_{0.7}Sr_{0.3}TiO₃ thin films from mHz to 20 GHz," *Appl. Phys. Lett.*, vol. 72, no. 4, pp. 498–500, Jan. 1998. Available: <https://doi.org/10.1063/1.120796>
37. K. L. Saenger, A. Grill, and D. E. Kotecki, "Oxygen-induced inhibition of noble metal silicide formation: Implications for electrode/barrier structures used with perovskite materials," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 143–151. Available: <https://doi.org/10.1557/proc-493-143>
38. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, P. R. Duncombe, D. A. Neumayer, D. E. Kotecki, H. Shen, and Q. Ma, "Electrical and microwave properties of Mn–implanted (Ba,Sr)TiO₃ thin films," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 27–32. Available: <https://doi.org/10.1557/proc-493-27>
39. H. Shen, D. E. Kotecki, R. Murphy, M. Zaitz, R. B. Laibowitz, T. M. Shaw, K. L. Saenger, J. D. Baniecki, G. Beitel, V. Klueppel, and H. Cerva, "Microstructure control of (Ba,Sr)TiO₃ films for gigabit DRAM," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 33–38. Available: <https://doi.org/10.1557/proc-493-33>
40. T. M. Shaw, R. B. Laibowitz, J. D. Baniecki, M. Copel, P. R. Duncombe, H. Shen, and D. E. Kotecki, "The effect of electrode interfaces on the properties of barium strontium titanate thin films," in *Proc. US–Japan Workshop on Electrically Active Ceramic Interfaces, MIT*, vol. 57, 1998.
41. S. Hamaguchi, A. Mayo, S. M. Rossnagel, , D. E. Kotecki, K. R. Milkove, C. Wang, and C. E. Farrell, "Numerical simulation of etching and deposition processes," *Jap. J. Appl. Phys., Part 1*, vol. 36, no. 7B, pp. 4762–4768, July 1997. Available: <https://doi.org/10.1143/jjap.36.4762>
42. D. E. Kotecki, "A review of high dielectric materials for DRAM capacitors," *Integr. Ferroelectrics*, vol. 16, no. 1-4, pp. 1–20, 1997. Available: <https://doi.org/10.1080/10584589708013025>
43. C. E. Farrell, K. R. Milkove, C. Wang, and D. E. Kotecki, "A reactive ion etch study for producing patterned platinum structures," *Integr. Ferroelectrics*, vol. 16, no. 1-4, pp. 109–138, 1997. Available: <https://doi.org/10.1080/10584589708013034>

44. D. E. Kotecki, "High-K dielectric materials for DRAM capacitors," *Semiconductor International*, vol. 19, no. 12, pp. 109–110, 112, 114, 116, Nov. 1996.
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48. K. A. Olson, D. E. Kotecki, A. Ricci, S. Lassig, and A. Hussain, "Characterization, modeling and design of an electrostatic chuck with improved wafer temperature uniformity," *Review of Sci. Instr.*, vol. 66, no. 2, pp. 1108–1114, Feb. 1995. Available: <https://doi.org/10.1063/1.1145988>
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51. D. E. Kotecki, S. G. Barbee, T. D. Cacouris, J. D. Chapple-Sokol, R. Eschbach, D. Wilson, J. Wong, and S. Zuhoski, "Applications of computational fluid dynamics for improved performance in chemical-vapor-deposition reactors," *J. Vac. Sci. Technol. B*, vol. 12, no. 4, pp. 2752–2757, July/Sept. 1994. Available: <https://doi.org/10.1116/1.587187>
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58. D. E. Kotecki and R. A. Conti, "Temperature distribution in an ideal azimuthally symmetric chemical-vapor-deposition reactor," *J. Vac. Sci. Technol. A*, vol. 10, no. 5, pp. 3136–3142, Sept./Oct. 1992. Available: <https://doi.org/10.1116/1.577877>
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