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EDUCATION

Ph.D., Engineering Applied Science, University of California Davis, Davis, CA (1988)
M.S., Engineering Applied Science, University of California Davis, Davis, CA (1984)
B.E.E., Electrical Engineering, *magna cum laude*, University of Dayton, Dayton, OH (1981)

EMPLOYMENT

University of Maine, Orono, ME (Sept 1999 –)
Associate Professor, Electrical and Computer Engineering

Blue Hill Innovation LLC, Orono, ME (2010 –)
Patent Agent (USPTO Registration #72,338) and **Consultant**

IBM Microelectronics Division, Hopewell Junction, NY (1988–1999)
Senior Engineer, DRAM Development Alliance, 1Gbit Integration Department (1997–1999), **Advisory Engineer**, Semiconductor Research & Development Center, Advanced Process Technology Department (1992–1997), **Staff Engineer**, Semiconductor Development Laboratory, CVD Technology Development Department (1988–1992)

Lawrence Livermore National Laboratory, Livermore, CA (1981–1988)
Student Engineer, Physics Department, (1984–1988), **Electronics Engineer**, Diagnostic Development Group, (1981–1984)

MacAulay Brown, Inc., Fairborn, OH (1980–1981)
Assistant Programmer (part-time)

NASA, Goddard Space Flight Center, Greenbelt, MD (1978–1980)
Co–op Engineer, Instrument Electro-Optics Branch

AWARDS

Graduate Faculty Mentor Award, University of Maine (2015); Award for Service, IEEE Maine Section (2014); Graduate Faculty Mentor Award, University of Maine (2008); Dean's Award of Excellence, University of Maine (2005); Teaching and Technology Fellowship, University of Maine (2001) and 15 Invention Achievement Awards, IBM (1990-2000).

PROFESSIONAL AND HONORARY SOCIETIES

IEEE (senior member), American Physical Society (APS), National Association of Patent Practitioners (NAPP), American Society for Engineering Education (ASEE); *Tau Beta Pi*, (The Engineering Honor Society) and *Eta Kappa Nu*, (The Electrical and Computer Engineering Honor Society of the IEEE).

PROFESSIONAL AND PUBLIC SERVICE

Tau Beta Pi, Maine Alpha Chapter: Advisor (2006–2007) and Chief Advisor (2007 – present).

IEEE, Maine Section: Secretary (2001); Member at Large (2002); Vice Chair (2003); Chair (2004) and Treasurer (2006–2009). IEEE, University of Maine Student Branch Co–Counselor (2003 – 2011).

Journal Reviewer: IEEE Transactions on Circuits & Systems; IEEE Electron Device Letters; IEEE Microwave & Wireless Components Letters; IEEE Journal of Solid State Circuits; Journal on Educational Resources in Computing; Journal of the American Ceramic Society; Journal of Vacuum Science & Technology; IET Circuits, Devices & Systems; and Journal of Circuits, Systems, and Computers.

Proposal Reviewer: Civilian Research & Development Foundation (CRDF) and SMART Scholarship Evaluation Panel.

Book Reviewer: Prentice Hall and Oxford University Press.

University of Maine: Faculty Senator (2004 – 2007); Graduate School Executive Committee (2011); University of Maine New Faculty Mentor (2006 – 2009); Department of Electrical & Computer Engineering (ECE) Graduate Program Coordinator (2008 – 2011); Electrical Engineering Curriculum Committee Chair (2007 – 2011); Microelectronics Scholarship Consortium Chair (1999 – 2011); ECE Faculty Search Committee Chair (2000, 2001, 2006), ECE Graduate Board Representative (2000-2002, 2008–2011), and Member, Engineering and Science Building Committee (2001).

TEACHING EXPERIENCE - UNIVERSITY OF MAINE

ECE 209: Fundamentals of Electric Circuits (for non-ECE Majors)
ECE 210: Electric Circuits
ECE 214: Electric Circuits Laboratory
ECE 444: Analog Integrated Circuit Design
ECE 445: Digital Integrated Circuit Design
ECE 464: Microelectronics Science and Engineering
ECE 512: Linear Systems Analysis
ECE 543: Microelectronic Devices I
ECE 643: Microelectronics Devices II
ECE 547: Integrated Circuit Design and Layout
ECE 548: Integrated Circuit Characterization and Testing
ECE 598: Special Topics in Integrated Circuit Design

PUBLICATIONS

1. P. Gunturi and D. E. Kotecki, "Analysis of a Gaussian signal adder to increase the energy and spectral efficiency of a IR-UWB transmitter," *IEEE Trans. Signal Process.*, (submitted for publication, 2016).
2. P. Gunturi, N. Emanetoglu, and D. E. Kotecki, "IR-UWB BPK transmitter optimized for maximum distance of transmission," *IEEE Trans. Circuits Syst. I*, (submitted for publication, 2015).
3. P. Gunturi and D. E. Kotecki, "IR-UWB BPK transmitter optimized for maximum distance of trans-

mission," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4.

4. P. Gunturi and D. E. Kotecki, "A PA for MBOFDM-UWB and IR-UWB transmitters," in *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug 2015, pp. 1–4.
5. P. Gunturi and D. E. Kotecki, "Temperature and supply voltage insensitive OOK transmitter for outdoor UWB communications," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 733–736.
6. P. Gunturi and D. E. Kotecki, "A wideband Class E PA with more than 40% PAE and 800 MHz bandwidth," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '14)*, Austin, Texas, Aug. 2014, pp. 725–728.
7. P. Gunturi and D. E. Kotecki, "Class E power amplifiers with tuned RC output matching circuit," in *IEEE Topical Workshop on Power Amplifiers for Wireless Communications*, San Diego, California, Sept. 2013.
8. Y. Lin and D. E. Kotecki, "A 127.3-133.6 GHz wide-locking low-power frequency-quadrupled phase-locked loop in 130nm SiGe BiCMOS," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '12)*, Boise, Idaho, Aug. 2012, pp. 754–757.
9. Y. Lin and D. E. Kotecki, "A 290 GHz frequency quadrupled SiGe voltage-controlled oscillator," in *Proc. IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '11)*, Seoul, Korea, Aug. 2011, pp. 1–4.
10. Y. Lin and D. E. Kotecki, "2.9 – 30.3 GHz fourth-harmonic voltage–controlled oscillator in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 401–404.
11. Y. Lin and D. E. Kotecki, "A voltage–controlled oscillator with a 0.8–13.4 GHz tuning range in 130nm SiGe BiCMOS technology," in *Proc. of the IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Athens, Greece, Dec. 2010, pp. 431–434.
12. Y. Lin and D. E. Kotecki, "312GHz fourth–harmonic voltage–controlled oscillator (VCO) designed using 130nm SiGe BiCMOS technology," in *Proc. IEEE International Conference on Electronics, Circuits and Systems, (ICECS '09)*, Yasmine, Tunisa, Dec. 2009, pp. 747–750, **(Best student paper award.)**.
13. B. C. Gierhart, D. G. Howitt, S. J. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, "Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA," *Sensors and Actuators, B: Chemical*, vol. 132, pp. 593–600, June 2008.
14. R. H. Bethel and D. E. Kotecki, "Low voltage BiCMOS circuit topologies for the design of a 19GHz, 1.2V, 4-bit accumulator in silicon-germanium," in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 1127–1130.
15. C. R. Kenney and D. E. Kotecki, "Microelectronic magnetic flux sensor for hearing aid application," in *Proc. 14th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '07)*, Marrakech, Morocco, Dec. 2007, pp. 6–9.

16. B. Gierhart, D. Howitt, S. Chen, Z. Zhu, D. E. Kotecki, R. L. Smith, and S. D. Collins, "Nanopore with transverse nanoelectrodes for electrical characterization and sequencing of DNA," in *Proc. 6th IEEE International Conference on Solid-State Sensors, Actuators and Microsystems (Transducers '07)*, Lyon, France, June 2007, pp. 399–402.
17. S. Manandhar, S. E. Turner, and D. E. Kotecki, "36-GHz, 16x6 bit ROM in InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 42, no. 2, pp. 451–456, Feb. 2007.
18. Z. Zhu, R. Tumati, S. Collins, R. Smith, and D. E. Kotecki, "A low-noise, low-offset operational amplifier in 0.35μm technology," in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 624–627.
19. S. Manandhar, S. E. Turner, and D. E. Kotecki, "A 20-GHz and 46-GHz, 32x6-bit ROM for DDS application in InP DHBT technology," in *Proc. 13th IEEE International Conference on Electronics, Circuits and Systems, (ICECS '06)*, Nice, France, Dec. 2006, pp. 1003–1007.
20. S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with sine-weighted DAC at 32 GHZ clock frequency in InP DHBT technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2284–2290, Oct. 2006.
21. D. E. Kotecki, T. Monk, V. Tkachuk, Z. Zhu, A. Delic-Ibukic, and S. E. Turner, "Custom analog and mixed–signal integrated circuit design at the undergraduate level – a university/industry collaboration," in *Proc. 6th International Workshop on Microelectronics Education*, Stockholm, Sweden, June 2006, pp. 47–50, ISBN: 91-7178-402-0.
22. S. E. Turner and D. E. Kotecki, "Direct digital synthesizer with ROM-less architecture at 13-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 16, no. 5, pp. 296–298, May 2006.
23. S. E. Turner, R. B. Elder, Jr., D. S. Jansen, and D. E. Kotecki, "4-bit adder-accumulator at 41-GHz clock frequency in InP DHBT technology," *IEEE Microwave Wireless Compon. Lett.*, vol. 15, no. 3, pp. 144–146, Mar. 2005.
24. S. E. Turner and D. E. Kotecki, "Benchmark results for high-speed 4-bit accumulators implemented in Indium Phosphide DHBT technology," *International Journal of High Speed Electronics and Systems*, vol. 14, no. 3, pp. 646–651, Sept. 2004.
25. F. Yang, D. E. Kotecki, G. Bernhardt, and M. Call, "Electrical and structural characterization of HfO_2 MIM capacitors," in *Novel Materials and Processes for Advanced CMOS, Proc. Mater. Res. Soc.*, vol. 745, 2003, pp. 203–208.
26. J. L. Cousins and D. E. Kotecki, "Simulation of the variability in microelectronic capacitors having polycrystalline dielectrics," *IEEE Electron Device Lett.*, vol. 16, no. 5, pp. 267–269, May 2002.
27. R. Schmidtt, D. McCann, B. Marquis, and D. E. Kotecki, "Dielectric relaxation of WO_3 thick films from 10 Hz to 1.8 GHz," *J. Appl. Phys.*, vol. 91, no. 10, pp. 6775–6777, May 2002.
28. J. L. Cousins and D. E. Kotecki, "Simulation of the variability in next-generation microelectronic capacitors with polycrystalline dielectrics," in *Ferroelectric Thin Films X, Proc. Mater. Res. Soc.*, vol. 695, 2002, pp. 247–252.
29. K. L. Saenger, G. Costrini, D. E. Kotecki, K. Kwietniak, and P. C. Andricacos, "Submicrometer platinum electrodes by through-mask plating," *J. Electrochem. Soc.*, vol. 148, no. 11, pp. 758–761, Nov. 2001.

30. C. C. Cabral, Jr., K. L. Saenger, D. E. Kotecki, and J. M. Harper, "Optimization of Ta-Si-N thin films for use as oxidation-resistant diffusion barriers," *J. Mater. Res. Soc.*, vol. 15, no. 1, pp. 194–198, Jan. 2000.

31. D. E. Kotecki, J. D. Baniecki, H. Shen, R. B. Laibowitz, K. L. Saenger, J. J. Lian, T. M. Shaw, S. D. Athavale, C. C. Cabral, Jr., P. R. Duncombe, M. Gutsche, G. Kunkel, Y.-J. Park, Y.-Y. Want, and R. Wise, "(Ba,Sr)TiO_3 dielectrics for future stacked-capacitor DRAM," *IBM J. of Res. and Dev.*, vol. 43, no. 3, pp. 367–382, May 1999.

32. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, K. L. Saenger, P. R. Dumcombe, C. C. Cabral, Jr., D. E. Kotecki, H. Shen, J. Lian, and Q. Ma, "Effects of annealing conditions on charge loss mechanisms in MOCVD $Ba_{0.7}Sr_{0.3}TiO_3$ thin film capacitors," *J. European Ceramic Soc.*, vol. 19, no. 6-7, pp. 1457–1461, 1999.

33. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, P. R. Dumcombe, D. E. Kotecki, H. Shen, J. Lian, and Q. Ma, "Nonlinear dielectric relaxation of Mn doped polycrystalline (Ba,Sr)TiO_3 thin films over the temperature range of 4.2 - 473K," in *Ferroelectric Thin Films VII, Proc. Mater. Res. Soc.*, vol. 541, 1999, pp. 23–28.

34. M. Copel, J. D. Baniecki, P. R. Duncombe, D. E. Kotecki, R. Laibowitz, D. A. Neumayer, and T. M. Shaw, "Compensation doping of $Ba_{0.7}Sr_{0.3}TiO_3$ thin films," *Appl. Phys. Lett.*, vol. 73, no. 13, pp. 1832–1834, Sept. 1998.

35. K. L. Saenger, A. Grill, and D. E. Kotecki, "Buried, self-aligned barrier layer structures for perovskite-based memory devices comprising Pt or Ir bottom electrodes on silicon-contributing substrates," *J. Appl. Phys.*, vol. 83, no. 2, pp. 802–813, Jan. 1998.

36. J. D. Baniecki, R. L. Laibowitz, T. M. Shaw, P. R. Duncombe, D. A. Neumayer, D. E. Kotecki, H. Shen, and Q. Ma, "Dielectric relaxation of $Ba_{0.7}Sr_{0.3}TiO_3$ thin films from mHz to 20 GHz," *Appl. Phys. Lett.*, vol. 72, no. 4, pp. 498–500, Jan. 1998.

37. K. L. Saenger, A. Grill, and D. E. Kotecki, "Oxygen-induced inhibition of noble metal silicode formation: Implications for electrode/barrier structures used with perovskite materials," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 143–151.

38. J. D. Baniecki, R. B. Laibowitz, T. M. Shaw, P. R. Duncombe, D. A. Neumayer, D. E. Kotecki, H. Shen, and Q. Ma, "Electrical and microwave properties of Mn–implanted (Ba,Sr)TiO_3 thin films," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 27–32.

39. H. Shen, D. E. Kotecki, R. Murphy, M. Zaitz, R. B. Laibowitz, T. M. Shaw, K. L. Saenger, J. D. Baniecki, G. Beitel, V. Klueppel, and H. Cerva, "Microstructure control of (Ba,Sr)TiO_3 films for gigabit DRAM," in *Ferroelectric Thin Films VI, Proc. Mater. Res. Soc.*, vol. 493, 1998, pp. 33–38.

40. T. M. Shaw, R. B. Laibowitz, J. D. Baniecki, M. Copel, P. R. Duncombe, H. Shen, and D. E. Kotecki, "The effect of electrode interfaces on the properties of barium strontium titanate thin films," in *Proc. US–Japan Workshop on Electrically Active Ceramic Intermaces, MIT*, vol. 57, 1998.

41. S. Hamaguchi, A. Mayo, S. M. Rossnagel, , D. E. Kotecki, K. R. Milkove, C. Wang, and C. E. Farrell, "Numerical simulation of etching and deposition processes," *Jap. J. Appl. Phys., Part 1*, vol. 36, no. 7B, pp. 4762–4768, July 1997.

42. D. E. Kotecki, "A review of high dielectric materials for DRAM capacitors," *Integr. Ferroelectrics*, vol. 16, no. 1-4, pp. 1–20, 1997.

43. C. E. Farrell, K. R. Milkove, C. Wang, and D. E. Kotecki, "A reactive ion etch study for producing patterned platinum structures," *Integr. Ferroelectrics*, vol. 16, no. 1-4, pp. 109–138, 1997.

44. D. E. Kotecki, "High-K dielectric materials for DRAM capacitors," *Semiconductor International*, vol. 19, no. 12, pp. 109–110, 112, 114, 116, Nov. 1996.

45. L. Economikos, D. E. Kotecki, and R. Surprenant, "Controlling the dimensions of laser chemical vapor deposited metallurgy [MCM-D]," *Trans. ASME, J. Electr. Pkg.*, vol. 118, no. 1, pp. 7–10, Mar. 1996.

46. T. Nguyen, H. L. Ho, D. E. Kotecki, and T. D. Nguyen, "Reaction study of cobalt and silicon dioxide," *J. Appl. Phys.*, vol. 72, no. 2, pp. 1123–1128, Jan. 1996.

47. D. E. Kotecki and J. D. Chapple-Sokol, "Hydrogen incorporation in silicon nitride films deposited by remote electron-cyclotron-resonance chemical vapor deposition," *J. Appl. Phys.*, vol. 77, no. 3, pp. 1284–1293, Feb. 1995.

48. K. A. Olson, D. E. Kotecki, A. Ricci, S. Lassig, and A. Hussain, "Characterization, modeling and design of an electrostatic chuck with improved wafer temperature uniformity," *Review of Sci. Instr.*, vol. 66, no. 2, pp. 1108–1114, Feb. 1995.

49. E. G. Colgan, C. C. Cabral, Jr., and D. E. Kotecki, "Activation energy for CoSi and $CoSi_2$ formation measured during rapid thermal annealing," *J. Appl. Phys.*, vol. 77, no. 2, pp. 614–619, Jan. 1995.

50. S. R. Summerfelt, D. E. Kotecki, A. Kingon, and H. Al-Shareef, "Pt hillock formation and decay," in *Ferroelectric Thin Films IV, Proc. Mater. Res. Soc.*, vol. 361, 1995, pp. 257–262.

51. D. E. Kotecki, S. G. Barbee, T. D. Cacouris, J. D. Chapple-Sokol, R. Eschbach, D. Wilson, J. Wong, and S. Zuhoski, "Applications of computational fluid dynamics for improved performance in chemical-vapor-deposition reactors," *J. Vac. Sci. Technol. B*, vol. 12, no. 4, pp. 2752–2757, July/Sept. 1994.

52. C. M. Ransom, T. N. Jackson, J. DeGelormo, D. E. Kotecki, C. Graimann, and D. K. Sadana, "Arsenic gas-phase doping of polysilicon," *J. Vac. Sci. Technol. B*, vol. 12, no. 3, pp. 1390–1393, May/June 1994.

53. C. M. Ransom, T. M. Jackson, J. DeGelormo, C. Zeller, D. E. Kotecki, C. Graimann, D. Sadana, and J. Benedict, "Shallow n^+ junctions in silicon by arsenic gas-phase doping," *J. Electrochem. Soc.*, vol. 141, no. 5, pp. 1378–1381, May 1994.

54. J. Stathis, D. A. Buchanan, D. Quinlan, A. Parsons, and D. E. Kotecki, "Interface defects of ultrathin-rapid-thermal oxide on silicon," *Appl. Phys. Lett.*, vol. 62, no. 21, pp. 2682–2684, May 1993.

55. T. Nguyen, H. L. Ho, D. E. Kotecki, and T. D. Nguyen, "Reaction study of cobalt and silicon nitride," *J. Mater. Res. Soc.*, vol. 8, no. 9, pp. 2354–2361, Sept. 1993.

56. D. E. Kotecki, E. G. Colgan, and A. Rose, "Reactor issues important for the deposition of selective tungsten by chemical vapor deposition using the SiH_4 reduction of WF_6," in *Chemical Perspectives of Microelectronic Materials III, Proc. Mater. Res. Soc.*, vol. 282, 1993, pp. 371–377.

57. D. E. Kotecki and S. G. Barbee, "Temperature optimization in an azimuthally symmetric single-wafer chemical-vapor-deposition reactor," *J. Vac. Sci. Technol. A*, vol. 10, no. 4, pp. 843–949, July/Aug. 1992.

58. D. E. Kotecki and R. A. Conti, "Temperature distribution in an ideal azimuthally symmetric chemical-vapor-deposition reactor," *J. Vac. Sci. Technol. A*, vol. 10, no. 5, pp. 3136–3142, Sept./Oct. 1992.

59. J. D. Chapple-Sokol and D. E. Kotecki, "High quality silicon nitride films prepared by ECR-enhanced CVD," in *Proc. Electrochem. Soc.*, vol. 92-18, 1992, pp. 545–555.

60. S. J. Jeng, D. E. Kotecki, J. Kanicki, C. C. Parks, , and J. Tien, "Structure, characterization, and the application of phosphorus doped hydrogenated microcrystalline silicon," in *Wide Band Gap Semiconductors, Proc. Mater. Res. Soc.*, vol. 242, 1992, pp. 693–697.

61. S. J. Jeng, D. E. Kotecki, J. Kanicki, C. C. Parks, and J. Tien, "Stucture, properties, and thermal stability of *in situ* phosphorus-doped hydrogenated microcrystalline silicon prepared by plasma-enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 58, no. 15, pp. 1632–1634, Apr. 1991.

62. D. E. Kotecki, J. Blouse, C. C. Parks, and R. Sarkozy, "Properties of *in situ* doped amorphous and polycrystalline silicon deposited by chemical vapor deposition from tertiarybutylarsine and tertiarybutylphosphine," in *Chemical Perspectives of Microelectronic Materials II, Proc. Mater. Res. Soc.*, vol. 204, 1991, pp. 295–302.

63. D. E. Kotecki, J. Jeng, J. Kanicki, C. Parks, W. Rausch, K. Seshan, and J. Tien, "Correlations between optical, electrical, and structural properties of *in situ* phosphorus-doped hydrogenated microcrystalline silicon – effects of rapid thermal annealing on materials properties," in *Materials Issues in Microcrystalline Semiconductors, Proc. Mater. Res. Soc.*, vol. 164, 1990, pp. 353–358.

64. J. Kanicki, E. Hasan, D. E. Kotecki, T. Takamori, and J. Griffith, "Properties and applications of undoped hydrogenated microcrystalline silicon thin films," in *Amorphous Silicon Technology, Proc. Mater. Res. Soc.*, vol. 149, 1989, pp. 173–179.

65. D. E. Kotecki and I. P. Herman, "A real time Monte Carlo simulation of thin film nucleation in localized-laser chemical vapor deposition," *J. Appl. Phys.*, vol. 64, no. 10, pp. 4920–4942, Nov. 1988.

66. D. E. Kotecki, "Nucleation and growth of silicon thin film microstructures by localized laser chemical vapor deposition," Ph.D. dissertation, Univ. of California, Davis, CA, June 1988, (Also published as UCRL 53896, Lawrence Livermore National Laboratory, June, 1988.).

67. D. E. Kotecki and I. P. Herman, "Initial stages of silicon growth on the (100) surface of silicon by localized laser CVD," in *Laser and Particle-Beam Chemical Processing for Microelectronics Proc. Mater. Res. Soc.*, vol. 101, 1988, pp. 119–124.

68. D. E. Kotecki and I. P. Herman, "Nucleation and growth of silicon microstructures by direct-laser writing," in *Photon, Beam, and Plasma Stimulated Chemical Processes at Surfaces Proc. Mater. Res. Soc.*, vol. 75, 1987, pp. 65–73.

69. I. P. Herman, F. Magnotta, and D. E. Kotecki, "Direct-laser writing of silicon microstructures: Raman microprobe diagnostics and modeling of the nucleation phase of deposition," *J. Vac. Sci. Technol. A*, vol. 4, no. 3, pp. 659–664, May/June 1986.

70. H. A. Koehler and D. E. Kotecki, "Developments of optical fast-gated imaging systems," in *Proc. Intern. Soc. for Optical Engineer. (SPIE)*, vol. 491, 1984, pp. 243–251.
71. B. A. Jacoby, D. E. Kotecki, and R. D. Lear, "Direct gating of microchannel plates," *IEEE Trans. Nucl. Sci.*, vol. NS-30, no. 6, pp. 4624–4627, Dec. 1983.
72. D. E. Kotecki and R. D. Lear, "Optical shutters using microchannel plate (MCP) intensifier tubes," in *Proc. Intern. Soc. for Optical Engineer. (SPIE)*, vol. 427, 1983, pp. 62–78.

INVENTIONS (U.S. PATENTS)

1. Y. Park, H. Lee, D. E. Kotecki, and G. Costrini, "Contact plug formation for devices with stacked capacitors," U.S. Patent 6,753,252, issued June 22, 2004.
2. D. E. Kotecki and K. L. Saenger, "Method for fabricating a dual-diameter electrical conductor," U.S. Patent 6,727,174, issued April 17, 2004.
3. D. E. Kotecki and W. H. Ma, "Method of fabricating a stack capacitor DRAM," U.S. Patent 6,544,832, issued April 8, 2003.
4. J. P. Gambino, G. B. Bronner, D. E. Kotecki, and C. J. Radens, "Storage–capacitor electrode and interconnect," U.S. Patent 6,429,474, issued August 6, 2002.
5. H. Shen, D. E. Kotecki, S. D. Athavale, J. Lian, G. Kunkel, and N. Chaudhary, "Method for removal of hardmask used to define noble metal electrode," U.S. Patent 6,420,272, issued July 16, 2002.
6. D. E. Kotecki, C. J. Radens, J. P. Gambino, and G. B. Bronner, "Method for simultaneously forming a storage–capacitor electrode and interconnect," U.S. Patent 6,395,594, issued May 28, 2002.
7. H. Akatsu, D. E. Kotecki, J. J. Lian, and H. Shen, "Hydrogen peroxide and acid etchant for a wet etch process," U.S. Patent 6,357,577, issued April 30, 2002.
8. H. Shen, D. E. Kotecki, S. Athavale, J. Lian, L. Economikos, F. F. Jamin, G. Kunekl, and N. Chaudhary, "Semiconductor structure and manufacturing method," U.S. Patent 6,365,328, issued April 2, 2002.
9. S. D. Halle, P. C. Jamison, D. E. Kotecki, and R. S. Wise, "Retrograde openings in thin films," U.S. Patent 6,355,567, issued March 12, 2002.
10. Y. Y. Wang, R. Jammy, L. J. Kimball, D. E. Kotecki, J. Lian, C. Lin, J. A. Miller, N. Nagel, H. Shen, and H. S. Wildman, "Capacitor stack structure and method of fabricating," U.S. Patent 6,339,007, issued January 15, 2002.
11. P. Andricacos, G. Costrini, D. E. Kotecki, and K. L. Saenger, "Capacitor formed with Pt electrodes having a 3D cup-like shape with roughened inner and outer surfaces," U.S. Patent 6,323,127, issued November 27, 2001.
12. D. E. Kotecki and W. H. Ma, "Overhanging separator for self-defining stacked capacitor," U.S. Patent 6,268,259, issued July 31, 2001.
13. D. E. Kotecki and W. H. Ma, "DRAM stack capacitor with vias and conductive connection extending from above conductive lines to the substrate," U.S. Patent 6,262,450, issued July 17, 2001.
14. S. D. Athavale, H. Shen, D. E. Kotecki, and J. Lian, "Easy to remove hard mask layer for semiconductor device fabrication," U.S. Patent 6,261,967, issued July 17, 2001.

15. L. L. Hsu, D. Kotecki, and J. A. Mandelman, "Method for forming a ferroelectric capacitor under the bit line," U.S. Patent 6,255,157, issued July 3, 2001.
16. R. E. Acosta, J. H. Comfort, A. Grill, D. E. Kotecki, and K. L. Saenger, "Structure and fabrication method for non-planar memory elements," U.S. Patent 6,242,321, issued June 5, 2001.
17. J. P. Gambino and D. E. Kotecki, "Crown capacitor using a tapered etch of a damascene lower electrode," U.S. Patent 6,222,219, issued April 24, 2001.
18. H. Shen, D. E. Kotecki, R. Laibowitz, K. L. Saenger, S. D. Athavale, J. Lian, M. Gutsche, Y. Y. Wang, and T. Shaw, "High dielectric constant material deposition to achieve high capacitance," U.S. Patent 6,207,584, issued March 27, 2001.
19. D. E. Kotecki, C. J. Radens, J. P. Gambino, and G. B. Bronner, "Method for simultaneously forming a storage-capacitor electrode and interconnect," U.S. Patent 6,201,272, issued March 13, 2001.
20. D. E. Kotecki and W. H. Ma, "Overhanging separator for self-defining discontinuous film," U.S. Patent 6,191,469, issued February 20, 2001.
21. M. S. Farooq, D. E. Kotecki, R. A. Rita, and S. M. Rossnagel, "High temperature, conductive thin film diffusion barrier for ceramic/metal systems," U.S. Patent 6,178,082, issued January 23, 2001.
22. J. P. Gambino, M. A. Jaso, and D. E. Kotecki, "Integrated circuit having a via and a capacitor," U.S. Patent 6,166,423, issued December 26, 2000.
23. H. Shen, N. Joachim, C. J. Radens, and D. E. Kotecki, "Tapered electrode for stacked capacitors," U.S. Patent 6,165,864, issued December 26, 2000.
24. D. E. Kotecki and W. H. Ma, "Overhanging electrode for self-defining discontinuous film," U.S. Patent 6,153,491, isued November 28, 2000.
25. D. E. Kotecki and W. H. Ma, "Trench separator for self-defining discontinuous film," U.S. Patent 6,150,230, issued November 21, 2000.
26. L. Economikos, D. E. Kotecki, and J. A. Mandelman, "Filling of high aspect ratio trench isolation," U.S. Patent 6,136,664, issued October 24, 2000.
27. K. L. Saenger, J. H. Comfort, A. Grill, and D. E. Kotecki, "Sidewall capacitor with L-shaped dielectric," U.S. Patent 6,131,258, issued October 17, 2000.
28. J. P. Gambino, G. B. Bronner, D. E. Kotecki, and C. J. Radens, "Method for simultaneously forming a storage-capacitor electrode and interconnect," U.S. Patent 6,124,199, issued September 16, 2000.
29. P. R. Duncombe, D. E. Kotecki, R. B. Laibowitz, W. Natzle, and C. Yu, "Method for cleaning the surface of a dielectric," U.S. Patent 6,054,328, issued April 25, 2000.
30. K. L. Saenger, J. H. Comfort, A. Grill, and D. E. Kotecki, "Isolated sidewall capacitor," U.S. Patent 6,027,966, issued February 21, 2000.
31. J. P. Gambino, M. A. Jaso, and D. E. Kotecki, "Method of forming a capacitor and a capacitor formed using the method," U.S. Patent 6,025,226, issued February 15, 2000.
32. H. L. Ho, D. E. Kotecki, and C. J. Radens, "Deep trench with enhanced sidewall surface area," U.S. Patent 6,015,985, issued January 18, 2000.
33. P. C. V. Buskirk, J. A. Fair, and D. E. Kotecki, "Method of delivering source reagent vapor mixtures for chemical vapor deposition using interiorly partitioned injector," U.S. Patent 6,010,748, issued January 4, 2000.

34. D. E. Kotecki and W. H. Ma, "Adherent separator for self-defining discontinuous film," U.S. Patent 6,002,575, issued December 14, 1999.
35. P. C. Andricacos, D. E. Kotecki, and K. L. Saenger, "Compound electrode stack capacitor," U.S. Patent 5,998,250, issued December 7, 1999.
36. D. E. Kotecki and S. V. Nguyen, "Semiconductor device with high dielectric constant insulator material," U.S. Patent 5,973,391, issued October 26, 1999.
37. D. E. Kotecki and W. H. Ma, "Trench separator for self-defining discontinuous film," U.S. Patent 5,955,756, issued September 21, 1999.
38. A. Grill, D. E. Kotecki, and K. L. Saenger, "Method, materials, and structures for noble metal electrode contacts to silicon," U.S. Patent 5,932,907, issued August 3, 1999.
39. K. L. Saenger, J. H. Comfort, A. Grill, and D. E. Kotecki, "Isolated sidewall capacitor," U.S. Patent 5,914,851, issued June 22, 1999.
40. J. P. Gambino and D. E. Kotecki, "Crown capacitor using a tapered etch of a damascene lower electrode," U.S. Patent 5,879,985, issued March 9, 1999.
41. H. L. Ho, D. E. Kotecki, and C. Radens, "Deep trench with enhanced sidewall surface area," U.S. Patent 5,849,638, issued December 15, 1998.
42. P. C. Andricacos, D. E. Kotecki, and K. L. Saenger, "Compound electrode stack capacitor," U.S. Patent 5,825,609, isued October 20, 1998.
43. D. E. Kotecki and W. H. Ma, "Overhanging separator for self-defining stacked capacitor," U.S. Patent 5,796,573, issued August 18, 1998.
44. P. C. Andricacos, J. H. Comfort, A. Grill, D. E. Kotecki, W. W. Patel, K. L. Saenger, and A. G. Schrott, "Plating of noble metal electrodes for DRAM and FRAM," U.S. Patent 5,796,320, issued August 4, 1998.
45. R. E. Acosta, J. H. Comfort, A. Grill, D. E. Kotecki, and K. L. Saenger, "Structure and fabrication method for non-planar memory elements," U.S. Patent 5,757,612, issued May 26, 1998.
46. P. C. V. Buskirk, J. A. Fair, and D. E. Kotecki, "Interiorly partitioned vapor injector for delivery of source reagent vapor mixtures for chemical vapor deposition," U.S. Patent 5,741,363, issued April 21, 1998.
47. K. L. Saenger, J. H. Comfort, A. Grill, and D. E. Kotecki, "Sidewall capacitor with L-shaped dielectric," U.S. Patent 5,712,759, issued January 27, 1998.
48. K. L. Saenger and D. E. Kotecki, "Method for making an isolated sidewall capacitor having a compound plate electrode," U.S. Patent 5,701,647, issued December 30, 1997.
49. D. E. Kotecki, "Characterization, modeling, and design of an electrostatic chuck with improved wafer temperature uniformity," U.S. Patent 5,675,471, issued October 7, 1997.
50. C. Yu, D. E. Kotecki, and W. C. Natzle, "Sealed chamber with heating lamps provided within transparent tubes," U.S. Patent 5,636,320, issued June 3, 1997.
51. K. L. Saenger and D. E. Kotecki, "Isolated sidewall capacitor having a compound plate electrode," U.S. Patent 5,633,781, issued May 27, 1997.
52. D. E. Kotecki, W. H. Ma, and K. L. Saenger, "Isolated sidewall capacitor with dual dielectric," U.S. Patent 5,585,998, issued December 17, 1996.

53. A. Husain, D. E. Kotecki, S. E. Lassig, K. A. Olson, and A. J. Ricci, "Characterization, modeling, and design of an electrostatic chuck with improved wafer temperature uniformity," U.S. Patent 5,548,470, issued August 20, 1996.
54. R. A. Conti, D. E. Kotecki, D. L. Wilson, J. W. Wong, and S. P. Zuhoski, "Removable gas injectors for use in chemical vapor deposition of aluminum oxide," U.S. Patent 5,425,810, issued June 20, 1995.
55. S. J. Jeng, J. Kanicki, D. E. Kotecki, C. C. Parks, and Z. J. Tien, "Polyemitter structure with improved interface control," U.S. Patent 5,374,481, issued December 20, 1994.
56. K. D. Beyer, C. M. Hsieh, L. L. Hsu, T. D. Yuan, and D. E. Kotecki, "Bonded wafer structure having a buried insulation layer," U.S. Patent 5,366,923, issued November 22, 1994.
57. K. D. Beyer, C. M. Hsieh, L. L. Hsu, D. E. Kotecki, and T. D. Yuan, "Thermal dissipation of integrated circuits using diamond paths," U.S. Patent 5,313,094, isued May 17, 1994.
58. K. D. Beyer, C. M. Hsieh, L. L. Hsu, T. D. Yuan, and D. E. Kotecki, "Bonded wafer structure having a buried insulation layer," U.S. Patent 5,276,338, issued June 4, 1994.
59. J. D. Chapple-Sokol, R. A. Conti, D. E. Kotecki, A. H. Simon, and M. Tejwani, "Safe method for etching silicon dioxide," U.S. Patent 5,268,069, issued December 7, 1993.
60. J. L. Blouse, J. O. Chu, B. Cunningham, J. P. Gambino, L. L. Hsu, D. E. Kotecki, S. Subbanna, and Z. J. Tien, "Low temperature emitter process for high performance bipolar devices," U.S. Patent 5,266,504, issued November 30, 1993.
61. K. Beyer, E. C. Fredericks, L. L. Hsu, D. E. Kotecki, and C. C. Parks, "Sub-layer contact technique using in situ doped amorphous silicon and solid phase recrystallization," U.S. Patent 5,192,708, issued March 9, 1993.
62. S. G. Barbee, J. D. Chapple-Sokol, R. A. Conti, and D. E. Kotecki, "LPCVD reactor for high efficiency, high uniformity deposition," U.S. Patent 5,134,963, issued August 4, 1992.

SELECTED PRESENTATIONS

1. Y. Lin and D. E. Kotecki, "A 290 GHz frequency quadrupled SiGe voltage-controlled oscillator," presented at the IEEE International Midwest Symposium on Circuits and Systems, (MWSCAS '11), Seoul, South Korea, 2011.
2. Y. Lin and D. E. Kotecki, "A voltage–controlled oscillator with a 0.8–13.4 GHz tuning range in 130nm SiGe BiCMOS technology," presented at the IEEE International Conference on Electronics, Circuits and Systems (ICECS), Athens, Greece, 2010.
3. Y. Lin and D. E. Kotecki, "2.9 – 30.3 GHz fourth-harmonic voltage–controlled oscillator in 130nm SiGe BiCMOS technology," presented at the IEEE International Conference on Electronics, Circuits and Systems (ICECS), Athens, Greece, 2010.
4. Y. Lin and D. E. Kotecki, "312GHz fourth–harmonic voltage–controlled oscillator (VCO) designed using 130nm SiGe BiCMOS technology," presented at the 16th IEEE International Conference on Electronics, Circuits and Systems, Yasmine, Tunisa, 2009.
5. C. R. Kenney and D. E. Kotecki, "Microelectronic magnetic flux sensor for hearing aid application," presented at the 14th International Conference on Electronics, Circuits and Systems, Marrakech, Morocco, 2007.

6. R. H. Bethel and D. E. Kotecki, "Low voltage BiCMOS circuit topologies for the design of a 19GHz, 1.2V, 4-bit accumulator in silicon-germanium," presented at the 14th International Conference on Electronics, Circuits and Systems, Marrakech, Morocco, 2007.
7. R. Tumati, D. Steward, S. D. Collins, W. Ahmed, R. L. Smith, and D. E. Kotecki, "Simulation of a nanopore sequencer using maxwell 3d and simplorer," presented at the Ansoft User's Meeting, Boston, MA, 2007.
8. Z. Zhu, R. Tumati, S. Collins, R. Smith, and D. Kotecki, "A low–noise, low–offset operational amplifier in 0.35μm technology," presented at the 13th International Conference on Electronics, Circuits and Systems, Nice, France, 2006.
9. S. Manandhar, S. Turner, and D. Kotecki, "A 20–GHz and 46–GHz, 32x6-bit ROM for DDS application in InP DHBT technology," presented at the 13th International Conference on Electronics, Circuits and Systems, Nice, France, 2006.
10. D. Kotecki, T. Monk, V. Tkachuk, Z. Zhu, A. Delic-Ibukic, and S. Turner, "Custom analog and mixed–signal integrated circuit design at the undergraduate level – a univeristy/industry collaboration," presented at the 6th International Workshop on Microelectronics Education, Stockholm, Sweden, 2006.
11. S. Turner and D. Kotecki, "Benchmark results for high–speed 4–bit accumulators implimented in Indium Phosphide DHBT technology," presented at the IEEE Lester Eastman Conference on High Performance Devices, Troy, NY, 2004.
12. F. Yang, D. Kotecki, G. Bernhardt, and M. Call, "Electrical and structural characterization of HfO_2 MIM capacitors," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 2003.
13. J. Cousins and D. Kotecki, "Simulation of the vairability in next–generation microelectronics capacitors with polycrystalline dielectrics," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 2002.
14. K. L. Saenger, G. Costrini, D. E. Kotecki, K. Kwietniak, and P. C. Andricacos, "Submicrometer platinum electrodes by through-mask plating," presented at the 199th Meeting of the Electrochemical Society, Washington, DC, Apr. 2001.
15. D. E. Kotecki, "High-dielectric thin films for DRAM - continued challenges," presented at International Conference on Metallurgical Coatings and Thin Films, San Diego, CA, Apr. 2000, **(Invited presentation)**.
16. C. Cabral, Jr., K. Saenger, D. Kotecki, and J. Harper, "Optimization of oxidation–resistant Ta–Si–N diffusion barriers," presented at the Advanced Metallization Conference (AMC), Orlando, FL, 1999.
17. J. Lian, H. Shen, M. Gutsche, G. Kunkel, Y. Park, Y. Wang, C. Lin, D. Kotecki, R. Laibowitz, J. Baniecki, K. Saenger, T. Shaw, S. Athavale, C. Cabral, P. Duncombe, and R. Wise, "BSTO thin film for a DRAM capacitor: Materials requirements and issues," presented at the International Symposium on Integrated Ferroelectrics, Colorado Springs, CO, 1999.
18. J. Baniecki, Q. Ma, R. Laibowitz, T. Shaw, D. Kotecki, H. Shen, and J. Lian, "Electrical properties of (Ba,Sr)TiO_3 thin films doped by ion implantation," presented at the International Symposium on Integrated Ferroelectrics, Colorado Springs, CO, 1999.

19. T. Shaw, J. Baniecki, R. Laibowitz, D. Kotecki, H. Shen, and J. Lian, "The temperature dependence of the dielectric properties of (Ba,Sr)TiO_3 thin films," presented at the International Symposium on Integrated Ferroelectrics, Colorado Springs, CO, 1999.

20. R. Laibowitz, J. Baniecki, T. Shaw, P. Duncombe, K. Saenger, D. Kotecki, H. Shen, J. Lian, and Q. Ma, "Dielectric relaxation and charge loss mechanisms in thin films of Barium Strontium Titante," presented at the American Physical Society Centennial Meeting, Atlanta, GA, 1999.

21. D. E. Kotecki, "A review of (Ba,Sr)TiO_3 dielectrics for DRAM capacitors," presented at Fall Meeting of the Materials Research Society, Boston, MA, Dec. 1998, **(Invited presentation)**.

22. T. Shaw, E. Liniger, R. Laibowitz, Z. Suo, M. Huang, D. Kotecki, and H. Shen, "The effects of stress on the dielectric properties of Barium Strontium Titanate thin films," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1998.

23. J. Baniecki, R. Laibowitz, T. Shaw, P. Duncombe, D. Kotecki, H. Shen, J. Lian, and Q. Ma, "Non–linear dielectric relaxation of as deposited and doped polycrystalline $Ba_xSr_{1-x}TiO_3$ thin films over the temperature range of 4.2 – 496K," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1998.

24. J. Baniecki, R. Laibowitz, T. Shaw, K. Saenger, P. Duncombe, C. Cabral, D. Kotecki, H. shen, J. Lian, and Q. Ma, "Effects of annealing conditions on charge loss mechanisms of MOCVD $Ba_{0.7}Sr_{0.3}TiO_3$ thin film capacitors for DRAM memory applications," presented at the Electroceramics VI, Montreux, Switzerland, 1998.

25. J. Baniecki, R. Laibowitz, T. Shaw, P. Duncombe, D. Neumayer, D. Kotecki, H. Shen, and Q. Ma, "Dielectric relaxation of $Ba_{0.7}Sr_{0.3}TiO_3$ thin films," presented at the 10th International Symposium on Integrated Ferroelectrics, Monterey, CA, 1998.

26. J. Baniecki, R. Laibowitz, T. Shaw, P. Duncombe, K. Saenger, D. Neumayer, D. Kotecki, H. Shen, and Q. Ma, "Frequency and temperature dependent properties and applications of Barium Strontium Titanate thin films," presented at the March Meeting of the American Physical Society, Los Angeles, CA, 1998.

27. R. Laibowitz, T. Shaw, J. Baniecki, P. Duncombe, K. Saenger, D. Neumayer, D. Kotecki, H. Shen, and Q. Ma, "Electrical and microstructural characteristics of high–permittivity materials for DRAM memories," presented at the March Meeting of the American Physical Society, Los Angeles, CA, 1998.

28. T. Shaw, R. Laibowitz, J. Baniecki, P. Duncombe, H. Shen, and D. Kotecki, "The effect of electrode interfaces on the properties of Barium Strontium Titanate thin films," presented at the US–Japan Workshop on Electrically Active Interfaces, Cambridge, MA, 1998.

29. M. Copel, J. Baniecki, P. Duncombe, D. Kotecki, D. Neumayer, R. Laibowitz, and T. Shaw, "Depletion depths of $SrTiO_3$ and $Ba_{0.7}Sr_{0.3}TiO_3$ thin films measured with photoemission spectroscopy," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1997.

30. J. Baniecki, R. Laibowitz, T. Shaw, P. Duncombe, D. Neumayer, M.Copel, D. Kotecki, H. Shen, and Q. Ma, "Electrical and microwave properties of Mn implanted (Ba,Sr)TiO_3 thin films," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1997.

31. K. L. Saenger, A. Grill, and D. E. Kotecki, "Oxygen-induced inhibition of noble metal silicide structures during annealing: Process integration implications for electrodes in perovskite–based

devices," presented at Fall Meeting of the Materials Research Society, Boston, MA, Dec. 1997, **(Invited presentation)**.

32. H. Shen, D. Kotecki, R. Laibowitz, T. Shaw, K. Saenger, R. Murphy, M. Zaitz, C. Parks, and L. Tai, "Microstructural control of (Ba,Sr)TiO_3 films for gigabit DRAM application," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1997.
33. D. E. Kotecki, "Issues related to incorporating high–permittivity films in a DRAM capacitor," presented at 2nd International Symposium on Low and High Dielectric Materials, 191st Meeting of the Electrochemical Society, Montreal, Canada, May 1997, **(Invited presentation)**.
34. R. Laibowitz, T. Shaw, P. Duncombe, D. Neumayer, A. Grill, D. Kotecki, K. Saenger, J. Baniecki, and Q. Ma, "Dielectric and structural properties of Barium Strontium Titanate (BST) and Bismuth Titanate (BiTi) sol–gel thin films," presented at the March Meeting of the American Physical Society, Kansas City, MO, 1997.
35. D. Kotecki, S. Hamaguchi, K. Milkove, C. Wang, and C. Farrell, "A model of the surface evolution of Pt during dry etching," presented at the American Vacuum Society Meeting, Philadelphia, PA, 1996.
36. S. Bilodeau, R. Carl, P. V. Buskirk, and D. Kotecki, "Composition control of MOCVD BST," presented at the American Vacuum Society Meeting, Philadelphia, PA, 1996.
37. R. Laibowitz, T. Shaw, D. Kotecki, S. Tiwari, A. Gupta, A. Grill, P. Duncombe, D. Beach, and S. Bilodeau, "Properties and applications of thin films of lead lanthanum titanate (PLT) and barium strontium titanate (BST)," presented at the March Meeting of the American Physical Society, St. Louis, MO, 1996.
38. D. E. Kotecki, "A review of high–dielectric materials for DRAM," presented at 1996 Annual Symposium of the New England Chapter of the American Vacuum Society, Boston, MA, June 1996, **(Invited presentation)**.
39. C. Farrell, K. Milkove, C. Wang, and D. Kotecki, "A reactive ion etch study for producing patterned platinum structures," presented at the 8th International Symposium on Integrated Ferroelectrics, Tempe, AZ, 1996.
40. D. E. Kotecki, "A review of perovskite–type dielectrics for DRAMs," presented at 8th International Symposium on Integrated Ferroelectrics, Tempe, AZ, Mar. 1996, **(Invited presentation)**.
41. S. Streiffer, C. Basxeri, A. Kingon, S. Bilodeau, R. Carl, P. V. Buskirk, P. Kirlin, P. McIntyre, S. Summerfelt, M. Anthony, M. Schumacher, G. Dietz, R. Waser, B. Zheng, D. Olson, J. Fair, D. Kotecki, C. Farrell, and R. Laibowitz, "Phenomenology of the dielectric response of CVD (BaSr)TiO_3 thin films," presented at the 8th International Symposium on Integrated Ferroelectrics, Tempe, AZ, 1996.
42. S. Summerfelt, D. E. Kotecki, A. Kingon, and H. A. Shareef, "Pt hillock formation and decay," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1995.
43. J. Chapple-Sokol, S. Barbee, D. Kotecki, S. Bilodeau, P. V. Buskirk, P. Kirlin, S. Summerfelt, B. Gnade, and R. Tsu, "Characterization of MOCVD BST films by spectroscopic ellipsometry," presented at the 6th International Synposium on Integrated Ferroelectrics, Monterey, CA, 1994.

44. S. Barbee, D. Kotecki, J. Chapple-Sokol, S. Bilodeau, P. V. Buskirk, and P. Kirlin, "Process optimization of MOCVD BST for advanced DRAM," presented at the 6th International Symposium on Integrated Ferroelectrics, Monterey, CA, 1994.

45. D. E. Kotecki, R. A. Conti, S. G. Barbee, T. Cacouris, J. Chapple-Sokol, R. Eschbach, D. Wilson, J. Wong, and S. Zuhoski, "Application of computational fluid dynamics for improved performance of chemical vapor deposition reactors," presented at the 40th Annual Symposium of the American Vacuum Society, Orlando, FL, 1993.

46. D. E. Kotecki, E. G. Colgan, and A. Rose, "Reactor issues important for the deposition of selective tungsten by chemical vapor deposition using the SiH_4 reduction of WF_6," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1992.

47. D. E. Kotecki and J. D. Chapple-Sokol, "High quality silicon nitride films prepared by remote ECR chemical vapor deposition," presented at the 39th Annual Symposium of the American Vacuum Society, Chicago, IL, 1992.

48. S. Barbee, D. Kotecki, and W. Patrick, "Influence of reactor geometry and process conditions on the temperature distrubition in a single–wafer CVD reactor," presented at the 39th Annual Symposium of the American Vacuum Society, Chicago, IL, 1992.

49. H. Ho, T. Nguyen, J. Chang, M. Gibson, and D. Kotecki, "Oxide damage in cobalt silicide processing," presented at the 182nd Meeting of the Electrochemical Society, Toronto, Canada, 1992.

50. J. Chapple-Sokol and D. E. Kotecki, "Deposition of silicon nitride films by ECR–enhanced CVD," presented at the 181st Meeting of the Electrochemical Society, St. Louis, MI, 1992.

51. S. Jeng, D. E. Kotecki, J. Kanicki, C. Parks, and J. Tien, "Sturcture, characteristics, and the application of phosphorus doped hydrogenated microcrystalline silicon," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1991.

52. D. E. Kotecki, S. G. Barbee, and R. A. Conti, "Temperature optimization in an azimuthally–symmetric single–wafer chemical vapor deposition reactor," presented at the 38th Annual Symposium of the American Vacuum Society, Seattle, WA, 1991.

53. D. E. Kotecki, "Computational fluid dynamics as a tool for optimizing CVD reactors," presented at the 4th FIDAP Users Conference, Evanston, IL, 1991.

54. D. E. Kotecki, J. Blouse, C. Parks, and R. Sarkozy, "Properties of *in situ* doped amorphous and polycrystalline silicon deposited by chemical vapor deposition from tertiarybutylarsine and tertiaryutylphosphine," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1990.

55. D. E. Kotecki, "Computational fluid dynamics as a tool for optimizing chemical vapor deposition reactors," presented at the SEMATECH Workshop on Equipment/Process Modeling for Micro–Electronics, Gaithersburg, MD, 1990.

56. D. E. Kotecki, S. Jeng, J. Kanicki, C. C. Parks, W. Rausch, K. Seshan, and J. Tien, "Correlations between optical, electrical, and structural properties of *in situ* phosphorus–doped hydrogenated microcrystalline silicon — effects of rapid thermal annealing on material properties," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1989.

57. D. E. Kotecki, "Nucleation and growth of thin film silicon microstructures deposited by localized chemical vapor deposition," presented at Oak Ridge National Laboratory; Oak Ridge, TN; IBM

Research Division, Yorktown Heights, NY; IBM General Technology Division, Hopewell Junction, NY; Lawrence Livermore National Laboratory, Livermore, CA, Mar.–June 1988, **(Invited presentation)**.

58. D. E. Kotecki, "Localized chemical vapor deposition of silicon microstructures," presented at 25th Anniversary of the Applied Science Department at the University of California, Davis, Davis, CA, Mar. 1988, **(Invited presentation)**.
59. D. E. Kotecki and I. P. Herman, "Initial stages of silicon growth on the (100) surface of silicon by localized laser CVD," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1987.
60. D. E. Kotecki and I. P. Herman, "Nucleation and growth of silicon microstructure by direct–laser writing," presented at the Fall Meeting of the Materials Research Society, Boston, MA, 1986.
61. I. P. Herman, F. Magnotta, and D. E. Kotecki, "Direct–laser writing of silicon microstructures — Raman microporbe diagnostics and modeling of the nucleation phase of deposition," presented at the 32nd Annual Symposium of the American Vacuum Society, Houston, TX, 1985.
62. H. A. Koehler and D. E. Kotecki, "Developments of optical fast–gated imaging systems," presented at the SPIE, San Diego, CA, 1984.
63. D. E. Kotecki and R. D. Lear, "Optical shutters using microchannel plate (MCP) intensifier tubes," presented at the SPIE, San Diego, CA, 1983.