Key Features

Bluetooth Spec v2.0+EDR Compliant

* Enhanced Data Rate (EDR) compliant with V2.0.E.2 of specification for both 2Mbps and 3Mbps modulation modes

Class 2 type Output Power

* Full Speed Bluetooth Operation with Full Piconet Support

* Scatternet Support

* 3.3V operation

* Minimum External Components

* USB,UART,SPI,PCM interface

* Support for 8Mbit External Flash Onboard

* Support for 802.11Co-Existence

* RoHS Compliant

CSR,BC417143 B-IRN-E4 Rev.2.0 July, 2005



Product Description

BTM400_6B module is a Class 2 Bluetooth module using BlueCore4-Exteanl chipset from leading Bluetooth chipset supplier Cambridge Silicon Radio.

BTM400_6B module interfaces up to 8Mbit of 16-bit external Flash memory. When used with the CSR Bluetooth software stack, it provides a Bluetooth specification V2.0+EDR fully compliant system for data and voice communications.

Applications

- * Bluetooth carkit
- * PCs
- * Personal Digital Assistants (PDAs)
- * Computer Accessories (compact Flash Cards, PCMCIA Cards, SD Cards and USB Dongles)
- * Acess Points
- * Digital Cameras

Specifications

Operating Frequency Band	2.4GHz -2.48GHz unlicensed ISM band
Bluetooth Specification	V2.0+EDR
Output Power Class	Class 2
Operating Voltage	3.3V
Host Interface	USB 1.1/2.0 or UART
Audio Interface	PCM and Analog interface
Flash Memory Size	8Mbit
Dimension	26.9mm (L) x 13 (W) mm x 2.2mm (H)

^{*} Specifications are subject to change without prior notice

Electrical Characteristics

Absolute Maximum Ratings			
Rating	Min	Max	
Storage temperature	-40°C	+150°C	
Supply voltage: VBAT	-0.4V	5.6V	
Other terminal voltages	VSS-0.4V	VDD+0.4V	

Recommended Operating Conditions		
Operating Condition	Min	Max
Operating temperature range	-40℃	+150℃
Guaranteed RF performance range ^(a)	-40°C	+150°C
Supply voltage: VBAT	2.2V	4.2V ^(b)

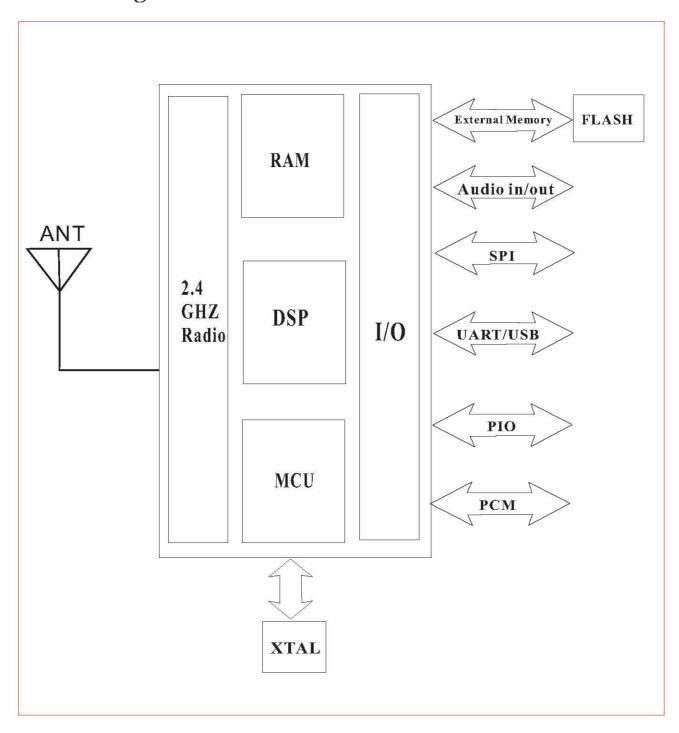
^{*} Typical figures are given for RF performance between -40°C and +105°C.

Power Consumption

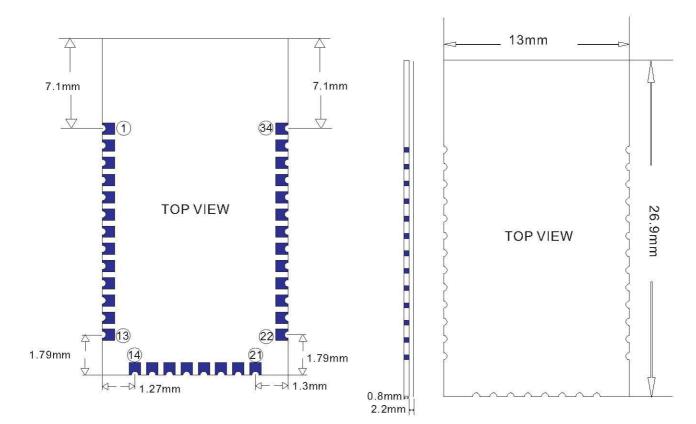
Operation Mode	Connection Type	UART Rate (kbps)	Average	Unit
Page scan	=	115.2	0.42	mA
ACL No traffic	Master	1152	4.60	mA
ACL With file transfer	Master	2	10.3	mA
ACL 1.28s sniff	Master	38.4	0.37	mA
ACL 1.28s sniff	Slave	38.4	0.42	mA
SCO HV3 30ms sniff	Master	38.4	19.8	mA
SCO HV3 30ms sniff	Slave	38.4	19.0	mA
Standby Host connection ^(a)	-	38.4	40	μΑ

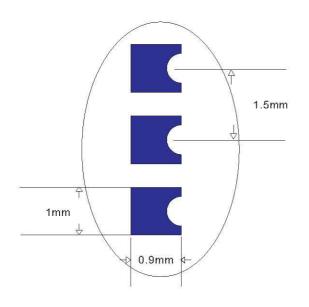
^{*} Low power mode on the linear regulator is entered and exited antomatically when the chip enters/leaves Deep Sleep mode. For more information about the electrical characteristics of the linear regulator, see section 4 in this document.

Block Diagram



BTM400_6B Module





NO	PIN NAME	NO	PIN NAME
1	UART-TX	18	SPI-MISO
1 2	UART-RX	19	SPI-CLK
3	UART-CTS	20	USB D+
4	UART-RTS	21	GND
4 5 6	PCM-CLK	22	GND
6	PCM-OUT	23	PIO(0)
7	PCM-IN	24	PIO(1)
8	PCM-SYNC	25	PIO (2)
9	AIO(0)	26	PIO(3)
10	AIO(1)	27	PIO(4)
11	RESET	28	PIO(5)
12	3. 3V	29	PIO(6)
13	GND	30	PIO(7)
14	GND	31	PIO(8)
15	USB D-	32	PIO(9)
16	SPI-CSB	33	PIO(10)
17	SPI-MOSI	34	PIO(11)

Pin Configurations

PIN NO.	NAME	ТҮРЕ	FUNCTION	RE-MARK
1	\$1000 PM	337-100-1000-1000-100-100	Secret Mathematic Adjustic Color of the Benefit April 2000.	
2	UART-TX UART-RX	CMOS Output CMOS Input	UART Data Output UART Data Input	2 N
3	UART-CTS	CMOS Input	UART Clear To Send Active Low	5
4	UART-RTS	CMOS Output	UART Request To Send Active Low	
5	PCM-CLK	Bi-directional	Synchronous Data Clock	
6	PCM-OUT	CMOS Output	Synchronous Data Cuck Synchronous Data Output	
7	PCM-IN	CMOS Input	Synchronous Data Output Synchronous Data Input	
8	PCM-SYNC	Bi-directional	Synchronous Data Sync	
9	AIO(0)	Bi-directional	Programmable Input/Output Line	
10	AIO(0) AIO(1)	Bi-directional	Programmable Input/Output Line	
		Drunctional	Reset if low.Input debounced so must be	
11	RESETB	CMOS Input		
12	3.3V	POWER	low for>5ms to cause a reset +3.3V Supply	For 3.3V Version
13	GND	GND	Ground	TOLOGOV VCISION
14	GND	GND	Ground	
15	USB D-	Bi-directional	USB Data Minus	
	30.4.40.000		Chip Select For Synchronous Serial	
16	SPI-CSB	CMOS Input	Interface	
17	SPI-MOSI	CMOS Input	Serial Peripheral Interface Data Input	
18	SPI-MISO	CMOS Output	Serial Peripheral Interface Data Output	
19	SPI-CLK	CMOS Input	Serial Peripheral Interface Clock	
		**	USB Data Plus with selectable internal 1.5K	
20	USB D+	Bi-directional	Q	
21	GND	GND	Ground	
22	GND	GND	Ground	
		Bi-directional with		
23	PIO(0)	programmable	Control output for external LNA (if fitted)	
	/	strength		
		Bi-directional with		
24	DIO(1)			
24	PIO(1)	programmable	Control output for external PA (if fitted)	
	2011	strength		
25	PIO(2)	Bi-directional	Programmable Input/Output Line	
26	PIO(3)	Bi-directional	Programmable Input/Output Line	
		Bi-directional with	Programmable Input/Output Line or	
27	PIO(4)	programmable	optional	
		strength	BT Priority/CH Clk output for co-	
		Bi-directional with	Programmable Input/Output Line or	
20	DIO(5)	102 Fig.		
28	PIO(5)	programmable	optional	
		strength	BT_Active output for co-existence	
		Bi-directional with	Programmable Input/Output Line or	
29	PIO(6)	programmable	optional	
	120 M	strength	WLAN Active/Ch Data input for co-	
30	PIO(7)	Bi-directional	Programmable Input/Output Line	
31	PIO(8)	Bi-directional	Programmable Input/Output Line	
32	PIO(9)	Bi-directional	Programmable Input/Output Line	
33	PIO(10)	Bi-directional	Programmable Input/Output Line	
34	PIO(11)	Bi-directional	Programmable Input/Output Line	