

- IC fabrication } Backend
- HDL - Hardware Description Language }
- VHDL }
- Verilog - Verification Language } Frontend
 - supports testing
- System verilog (OOPS)
- UVM - Universal Verification Methodology
 - for verifying integrated circuit Designs
(+Python
+matlab)
- FPGA - Field Programmable Gate Array
 - It is an IC that consists of internal hardware blocks with user programmable interconnects to customize operation for a specific application.
 - FPGA's are used in place of microprocessors.
- Verilog ... Drawback : Precision

Units: ① Fabrication

② Parametric Analysis - V, I, Figure of merits, ID, IO, RC(C), delay, frequency

③ Logic

④ Latest Trends

Basics:

→ EDC : BJT - Working, VI characteristics

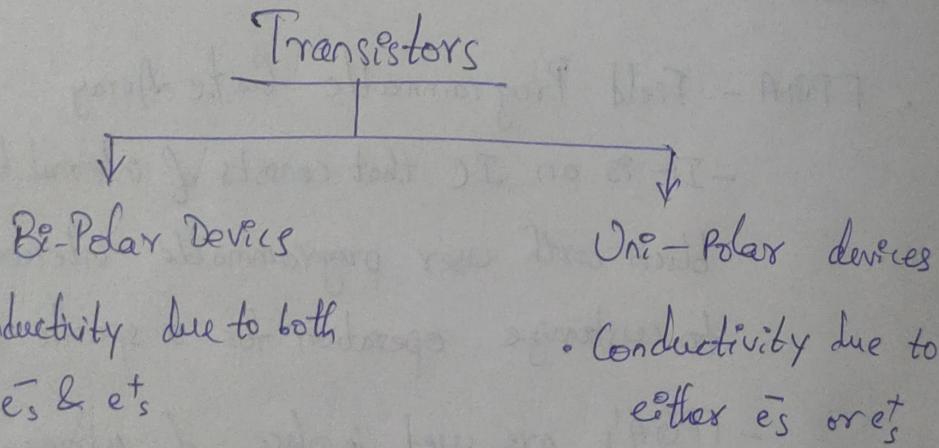
FET (MOSFET) - Working, Symbol,

VI characteristics

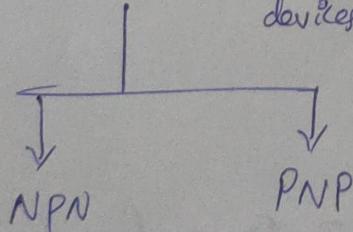
→ DSD :- MUX, De-mux, flip-flops, Adders, Encoders,
Decoders

- Variable devices

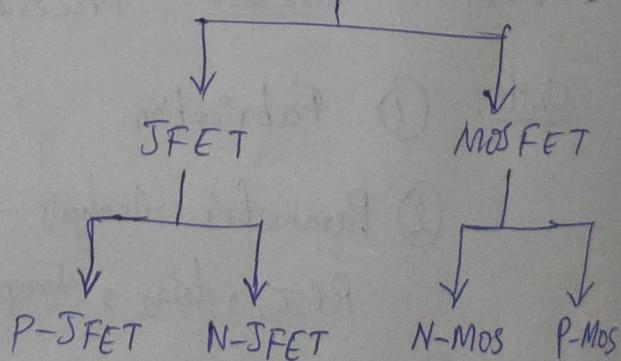
- Transistors : Trans - multiple & estors - terminals
(electronics) → from Greek



BJT (current controlled devices)



Unipolar (voltage controlled devices)



. In core-semiconductor industries : MOSFET's (77%)
BJT's (11%)

- JFET used as Driver cards
- BJT as integrator circuit for integration
- MOSFET - Building blocks of semi-conductors.
- IC - integration of circuits
- BJT - drives the load (Bi-polar Junction Transistor)
- MOSFET - Evaluates the Logic
 - Metal Oxide Semiconductor Field Effect Transistor
- IGFET - Insulated Gate FET

→ Logical evaluation by MOSFET, this output should be driven properly and it is taken care by BJT.

03/01/2023

MOSFET / IGFET :

- Metal Oxide Semiconductor Field Effect Transistor
- Insulated Gate Field Effect Transistor
- Based on type of substrates : (mobility)
 - MOSFET
 - N-MOSFET ($1200 \text{ cm}^2 \cdot \text{V/sec}$)
 - P-MOSFET ($700 \text{ cm}^2 \cdot \text{V/sec}$)
- Spec, Effect/Efficiency, Power Utilization, Noise immunity,
• 100% nullification of noise is not possible.
- Speed, Low power consumption, Noise immunity
(Expectations / Required ones of an electronic circuit)]
- Building Blocks of Electronics - MOSFET's
- Substrate : Pure Si wafer
- $\mu_e > \mu_h \Rightarrow$ Switching speed is high
(mobility) Max. current can be drawn \Rightarrow Saturated state
- So N-MOSFET preferable over P-MOSFET, as majority carriers are e^- & minority carriers are holes in N-MOSFET.
- $I_{CE(\text{sat})}$ - In saturation state, max. current can be drawn and it can be used as a switch (in active region)
 $I_{C(\text{max})}$ (ON)

• Reverse Recovery time : from $I_{C(sat)}$ to 0

• Active region : The region from 0 to $I_{C(sat)}$
~~Cut~~ (for an amplifier)

→ In Active region, no clipping of signal occurs.

• High mobility - switching speed increases.

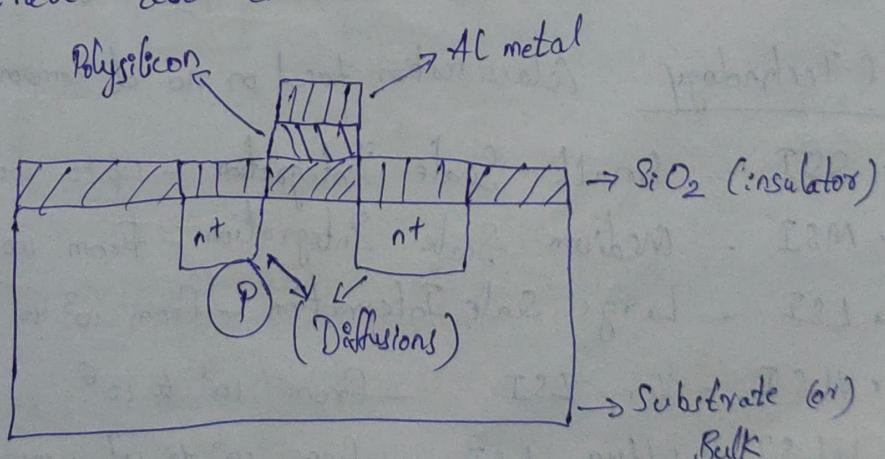
N-MOSFET : (Drain current is due to e^-) (Uni-polar device) (I_D)

• B, Al, In, Ga - Trivalent elements (P-type elements)

• P, As, Sb (Antimony) - Pentavalent element (N-type elements)

• Dope substrate with P-type impurity.

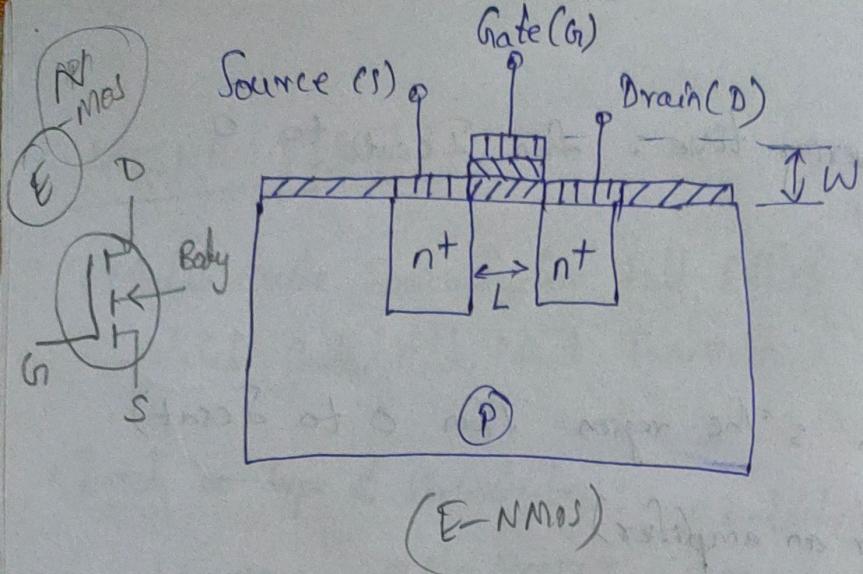
• Substrate also called as Bulk.



• n⁺ → means highly doped

• Diffusions or Implant

• n++ → very highly doped



→ Al metal
 → Poly silicon
 → SiO₂

- Length of Channel 'L' → Distance b/w Source implant & Drain implant.

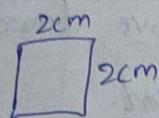
H.W

- SSI, VLSI, Scaling Integrations, Mealy, Masley Laws
- Moore's Law : states that every 2 years the no. of transistors in a chip should double.
- Size of Transistor : Parameters
 - Length of channel (L) Ex: 5 nm
5 × 10⁻⁹ m
 - Width of Gate ~~Resistor~~ (W)
 - Scaling - changing . Scale means to change

IC Technology Classification based on no. of components integrated

- SSI - Small Scale Integration - up to 100 components
- MSI - Medium Scale Integration - from 100 to 10³ "
- LSI - Large Scale Integration - from 10³ to 10⁵
- VLSI - Very LSI - from 10⁵ to 10⁶
- ULSI - Ultra LSI - from 10⁶ to 10⁹ components
- GLSI - Giant LSI
- Nano Technology

- No. of transistors accommodation in the given chip of area 'A' has been increased over the years



In 1960 - 10 Transistors accommodated

1970 - 40

1980 - 50

1990 - 100

2000 - 1000

2010 - \rightarrow 2000 \diamond

2020 - \rightarrow 1 lakh

- Over the years, size of transistor made smaller & smaller.

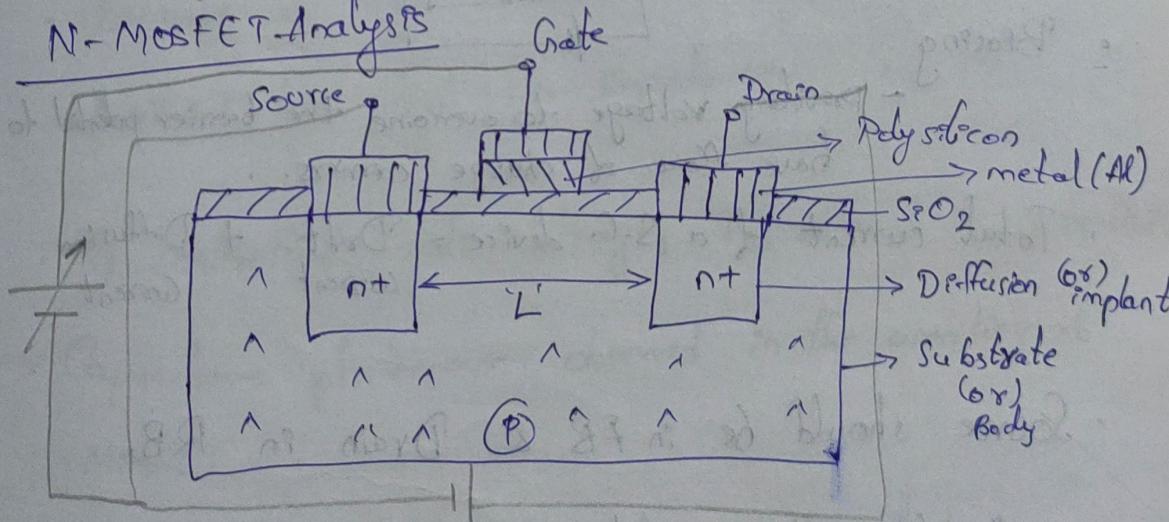
- Increase or Decrease 'Z' w.r.t the aspect ratio of W.

- $Z = \frac{W}{L}$ • Z' - Aspect ratio

- Scaling: \sqrt{L} - to increase speed of operation

04/01/2023

N-MOSFET Analysis



(E-NMOS) MOSFET (Based on structure)

Enhancement MOSFET

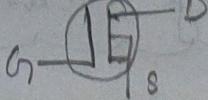
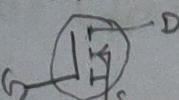
E-NMOSFET

E-PMOSFET

Depletion MOSFET

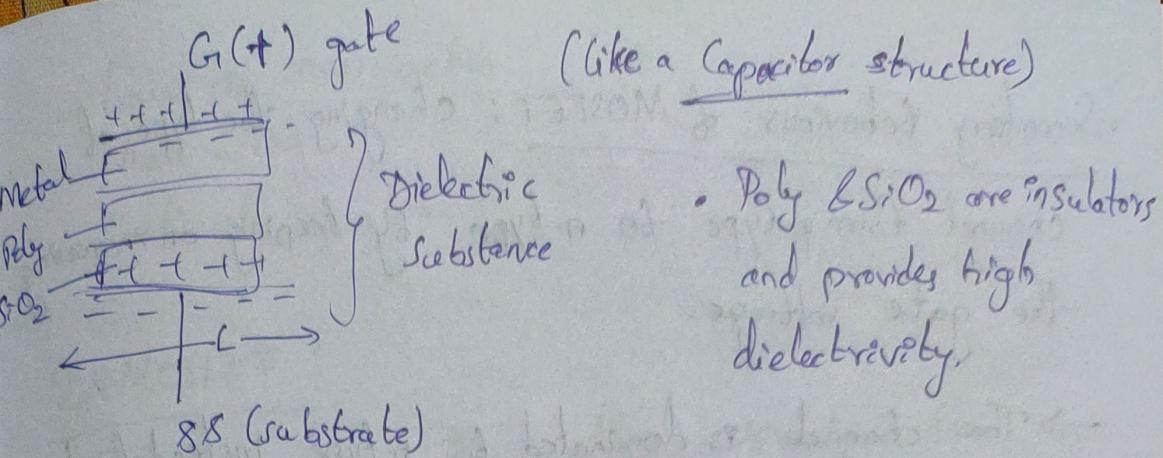
D-NMOSFET

D-PMOSFET



04/01/2023

- Source : Pumps out the carriers.
 → Where charge carriers take birth.
 → These charge carriers tries to move towards the drain and this causes current.
- Drain : I_D (or) I_{DS} → Drain Current
- Charge carriers move from source to drain via channel.
- Distance b/w source & drain - Length of channel.
- Diffusion current : (happens by nature, by attraction.)
 (by virtue of potential difference) \Rightarrow recombination of e^- & h^+ takes place.
- Barrier Potential
- Biasing - Providing voltage to overcome the barrier potential to have flow of charge carriers.
- Total current of a S.C. device = Drift current + Diffusion current
- Source should be in FB & Drain in RB.
- Gate terminal is like a tap of water
- By controlling Gate voltage, we can control flow of charge carriers & so called the device is called as Voltage controlled device

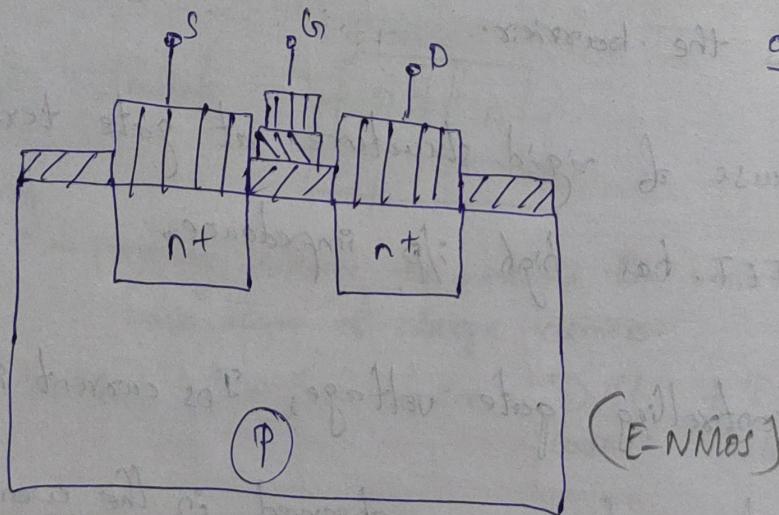


- Poly & SiO_2 are insulators and provides high dielectrivity.

- Input Impedance of MOSFET is very high ($\approx \infty$)
- Input i.e. Analog or Digital information comes through Gate terminal.
- The input has a hurdle / barrier, input need to cross the barrier.
- Because of rigid structure at gate terminal, MOSFET has high i/p impedance.
- By controlling gate voltage, I_{DS} current is controlled.
- Capacitance phenomenon observed in the working of MOSFET.
- The voltage (at gate terminal) at which drain current observed is called threshold voltage.
- Gate voltage $< V_{TH}$; electrons get recombined by the holes (in substrate) in channel.

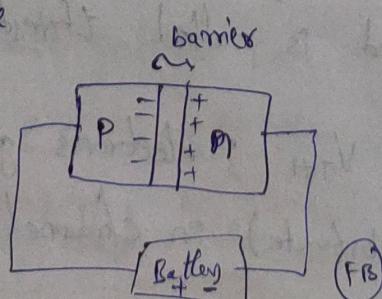
- Secondary behaviour of MOSFET: changing the type of channel from p-type to n-type by keeping on increasing the gate voltage.
- The channel is dominated by n-type instead of p-type
- Mobility of ϵ_s i.e. speed of charge carriers by Forward biasing Source and Reverse biasing Drain.

★ Increasing or Decreasing i.e. Modulating the length of channel is called as Channel Length Modulation



In P-N junction

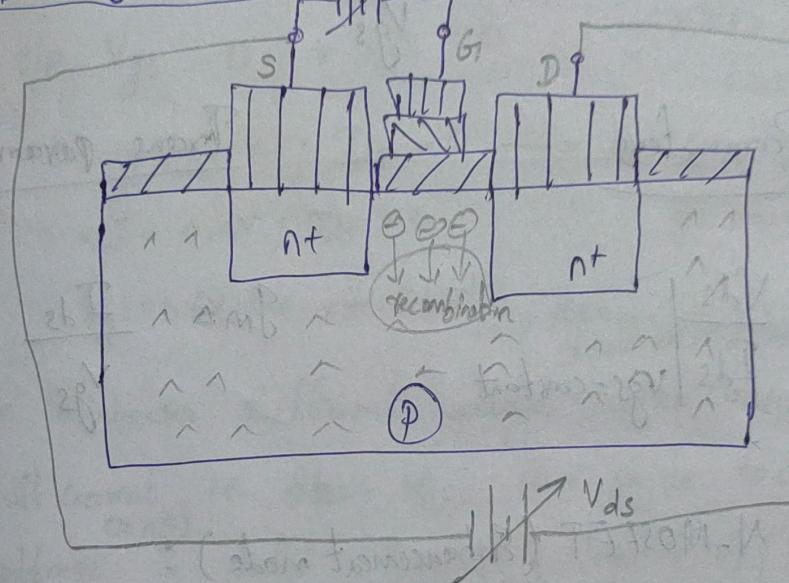
- As immobile ions get accumulated, free e^- & h^+ cannot pass through this barrier & so some biasing need to be given i.e. some supply voltage



- Laws of mass action
- Hall action
- Continuity equation

P-N-MOSFET :

- N_t , V_{gs} , V_{ds} , I_{ds} $\rightarrow V_{gs} \rightarrow$ AC analysis - (use low caps)



(E-NMOS)

- $V_{gs} \rightarrow$ Variable voltage \rightarrow gate-source voltage

- Diffusion Current : it is by virtue of potential difference and recombination of e^- & e^+ takes place.

- Initially, I_{ds} must remain zero, if it is non-zero then it is dangerous. (i.e. diffusion current must be maintained zero, as drift current will be zero without supply)

. I/P voltage : V_{gs}

. O/P voltage : V_{ds}

. O/P Current : I_{ds}

} 3 parameters

For Analysis

- Do differentiation
- If 2 parameters

- Do partial differentiation
If more than 2 parameters

$$\rightarrow \text{O/P Resistance} = \frac{V_{ds}}{I_{ds}} \quad | \quad V_{gs} = \text{constant}$$

$$\cdot \text{Dynamic Resistance} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \quad \left| \begin{array}{l} \\ \\ V_{gs} = \text{constant} \end{array} \right.$$

Transfer characteristics

$$\text{Static resistance} = \frac{\Delta V_{ds}}{\Delta I_{ds}}$$

$$\cdot \text{Trans Conductance: } g_m = \frac{I_{ds}}{V_{gs}}$$

Output Parameters

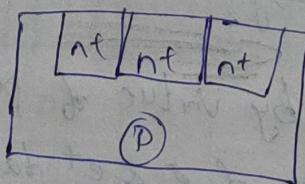
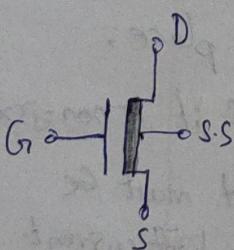
$$\text{O/P Resistance} = \frac{V_{ds}}{I_{ds}} \quad \left| \begin{array}{l} \\ \\ V_{gs} = \text{constant} \end{array} \right.$$

$$g_m = \frac{I_{ds}}{V_{gs}}$$

Trans parameters

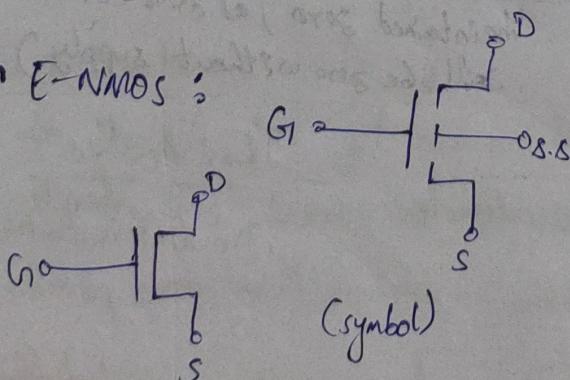
Working of N-MOSFET (Enhancement mode):

D-NMOS:



- Continuous channel
- Even without supply, there is a flow of drain-current (due to diffusion current)
- And so not preferred for industrial purpose.

E-NMOS:



• Discontinuous channel

• Hence, preferred

In D-NMOSFET, there is a continuous channel and even without V_{gs} , I_{ds} is observed.

I_{ds} is observed even ^{when} input voltage V_{gs} is not supplied
i.e. $V_{gs} = 0$ in D-MOSFET

Hence, E-MOSFET preferred over D-MOSFET

Working of E-NMOS:

O/P
 $V_{gs} = 0 \Rightarrow I_{ds} = 0 \rightarrow V_{ds}$ is maintained constant.

$V_{gs} = 0.2V ; I_{ds} = 0 \rightarrow$ As holes of p-substrate
 $V_{gs} = 0.4V ; I_{ds} = 0$ get recombined with e^-

$V_{gs} = 0.6V = V_t ; I_{ds} = i_0(nA)$ (that should be supplied)

The minimum sufficient voltage which causes a small drift current i.e. efflow of e^- from source to drain, such voltage is called threshold voltage ($V_t / V_s / V_{cat-en}$)

$V_{gs} = 0.8V ; I_{ds} \uparrow$

MOSFET
Source-Drain

$V_{gs} \uparrow$ then $I_{ds} \uparrow$

$$(2\mu C_s V_F)^2 = C_s(V) + \text{constant}$$

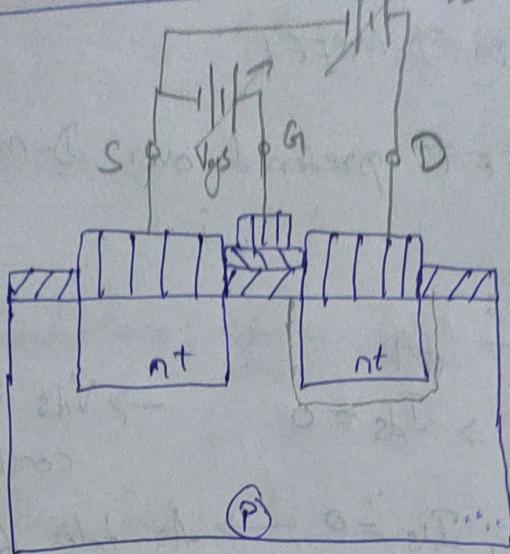
At particular point I_{ds} remains constant, as the channel completely filled with e^-

channel: Ptype to ntype

Secondary behaviour of MOSFET

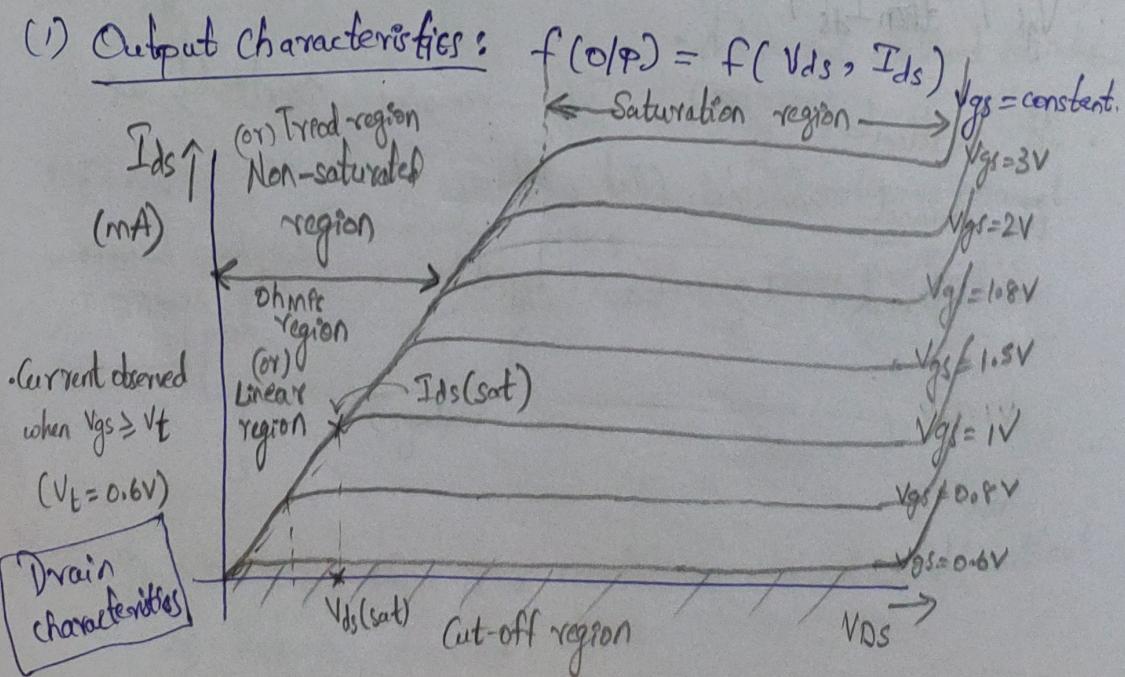
N-MOSFET characteristics

10/01/2023



1. Capacitance phenomenon at Gate terminal.
 2. Input given at Gate terminal, power supply or ground connected to Drain terminal.
- # MOSFET is a Bi-directional device i.e. source and drain terminals are interchangeable.
→ No deviation: in structure, in working phenomena & in I-V characteristics.

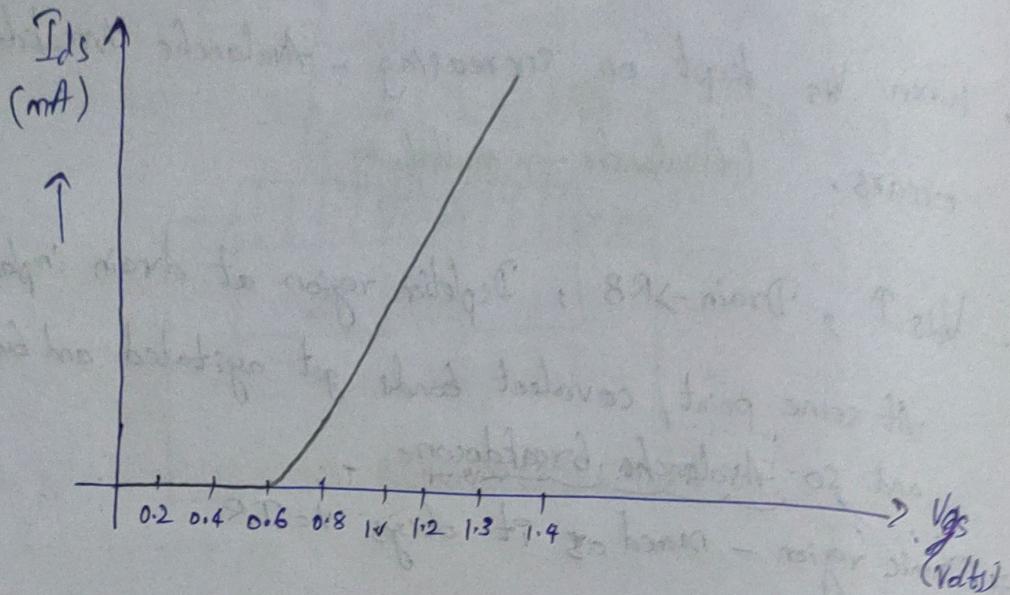
(1) Output characteristics:



- I_{ds} is independent of V_{ds} . (approximately) (when $V_{gs} = 0V$)
- When V_{ds} kept on increasing - Avalanche breakdown occurs. (Avalanche \rightarrow multiplying)
- $V_{ds} \uparrow$, Drain \rightarrow RB, Depletion region at drain implant \uparrow , At some point, covalent bonds get agitated and burst out and so Avalanche breakdown.
 → Ohmic region - named as it obeys $V = IR$
- MOSFET used in applications like in amplifying to avoid high noise effects.
- For designing amplifier, we operate MOSFET in Ohmic region.
- For switch purposes, operated in Saturation region (ON) and Cut-off region (OFF).
- Output characteristics other name Drain Characteristics.

- $V_{ds(\text{sat})}$ - point at which $I_{ds(\text{sat})}$ obtained i.e. $I_{ds(\text{maximum})}$ or saturated.
 - $I_{ds(\text{sat})}$ - maximum I_{ds} at fixed V_{gs}
 - $V_{ds(\text{sat})}$ is dependent on V_{gs}
 $V_{gs} \uparrow$ then $V_{ds(\text{sat})} \uparrow$
 - $V_{ds(\text{sat})}$ - value of Drain-source voltage at which I_{ds} saturates
- $V_{ds(\text{sat})}$ always calculated at fixed V_{gs} and by $I_{ds(\text{sat})}$

(2) Transfer characteristics : I_{ds} vs V_{gs}

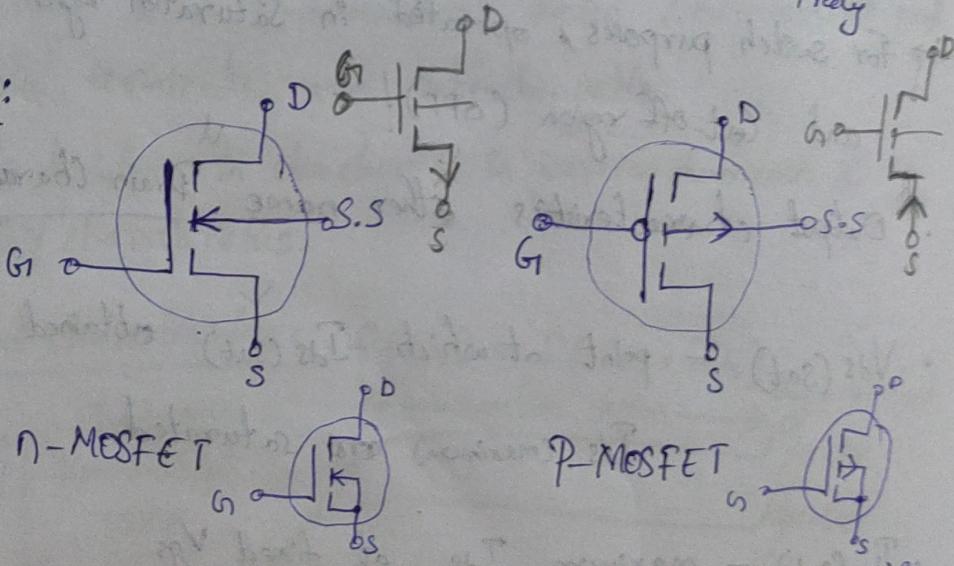


- $V_{gs} \uparrow \rightarrow$ mobility of charge carriers $\uparrow \rightarrow$ Velocity saturation state?

- Drain barrier induced i.e. no barrier $\Rightarrow e^-$ moves freely

Symbol:

Enhancement mode



- Bubble is given in P-MOS symbol, bubble means NOT (-ve), as in P-MOS we give -ve V_{gs} .

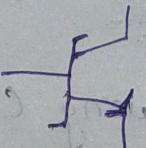
① D-MOSFET

Assignment

② Moore's Law

③ N-MOSFET
(Refresher)

Technologies (Logics)

- 1) R-R Logic
 - 2) D-R Logic
 - 3) DDL - ^{more} power dissipations
 - 4) DTL
 - 5) TTL ^{got an idea} \rightarrow ^{Reverse Recovery time is high (dead time of TTL)} I_G
- Shaky transistor :  good reverse recovery time
- ✓ 6) ECL - Emitter Coupled Logic (fastest logic)
 - 7) NMOS Logic
 - 8) PMOS Logic
 - ✓ 9) CMOS Logic (Low Power consumption)
 - 10) P-PMOS Logic (Pseudo-PMOS)
 - 11) P-NMOS Logic
 - 12) CCMOS / C²MOS Logic (clocked CMOS)
 - 13) Domino Logic
 - ✓ 13) BiCMOS (High Driving capability & Low Power consumption)

12/01/2023

Introduction

① MOSFET

↳ n-MOSFET }
↳ p-MOSFET } V-I characteristics

② Technologies

* ③ Logic Design - (*) ~~and~~ nMOS, PMOS, CMOS

(*) Inverter / NOT gate Design.

(*) " " " Analysis

④ Logic Gates Design using CMOS Logic

⑤ Fabrication process

(i) nMOSFET (ii) p-MOSFET (iii) CMOS

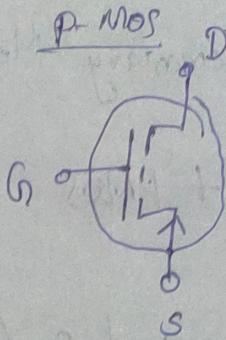
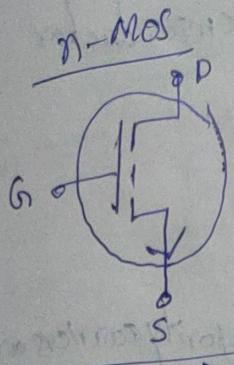
⑥ Stick Diagrams and Layout Design

⑦ CMOS Analysis & Driving Circuits

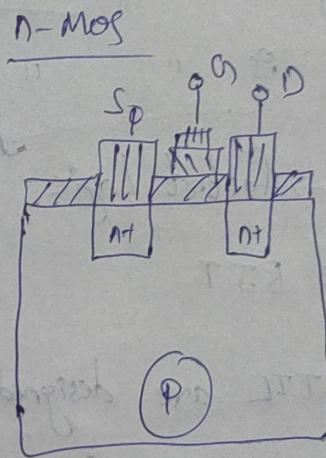
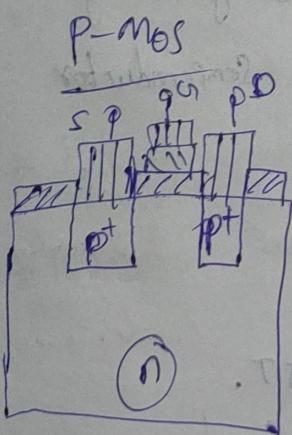
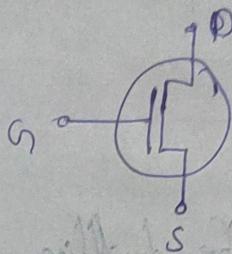
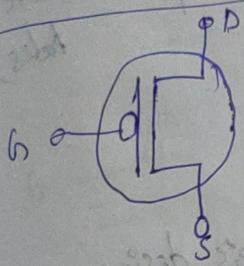
Brings

Crayons

Sketch
Pens



Enhancement Mode



$V_{GS} \rightarrow$ (-ve)

$V_S \rightarrow$ +ve terminal

$V_D \rightarrow$ -ve terminal

Si on chip 1cm x 1cm



• Around 200 ICs need to be fabricated on the Si chip

• For every IC, equal powersupply, and same clockpulse need to be given.

• All IC's should be in equilibrium

• Sometimes due to long wiring, ICs at distant may not receive same powersupply \rightarrow This is dangerous

$$V_{PP} = 12V \rightarrow 11.9V$$

$$f = 10 \text{ MHz} \rightarrow 9.99$$

- CMOS : Complementary Metal-Oxide Semiconductor

- CMOS = NMOS + PMOS

Drawbacks

- PMOS : Switching speed is low (as majority carriers are holes)
- NMOS : Continuous ON

→ 'NOT' gate is the building block of logic design.

→ MOSFET is a Semiconductor

→ ECL → fastest Logic BJT

→ TTL → BJT

→ ECL & TTL are designed using BJT.

Q. Why ECL is the fastest logic : due to avoidance of saturation region for application.

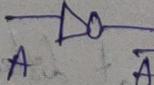
★ LOGIC DESIGN ★

- Power rails

(Power supply) ————— V_{DD} (Pull-up Transistor/Region)

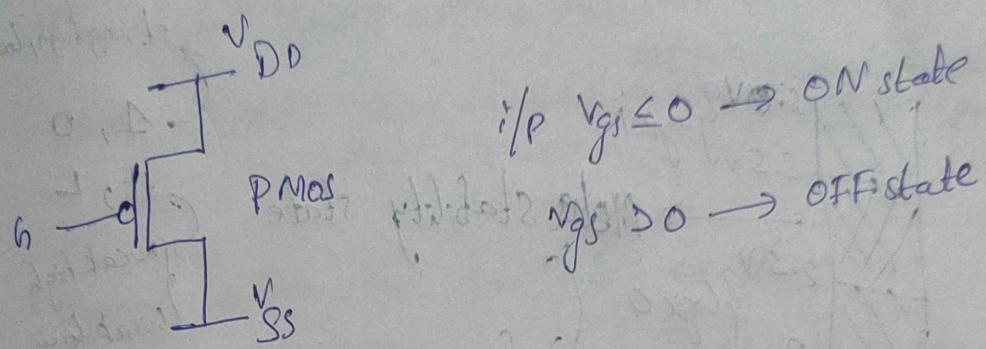
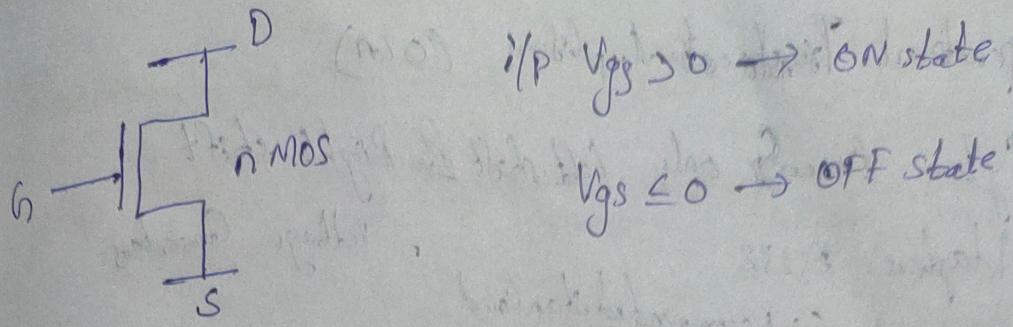
(Substrate) ————— V_{SS} (Pull-down Transistor/Region)

- NOT gate



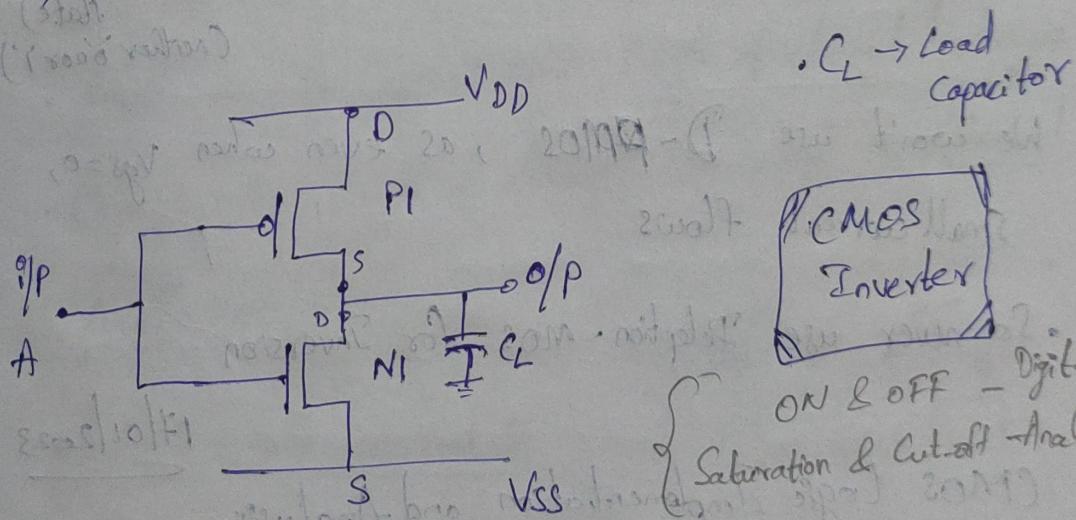
A	Y = \bar{A}
0	1
1	0

Inverter, Negation, Complementary



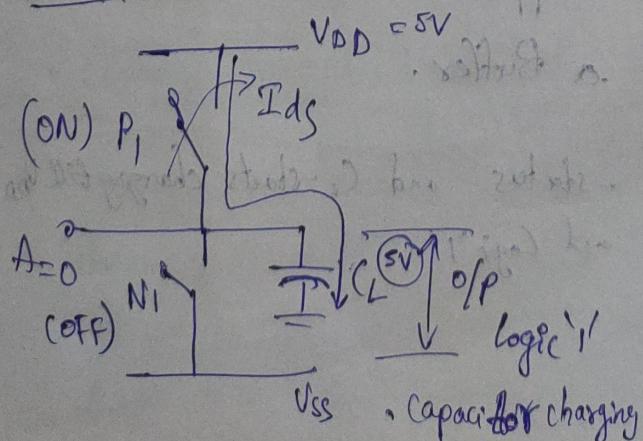
→ Pull-up Transistor : → Always PMOS used

→ Pull-down Transistor : → Always nMOS used

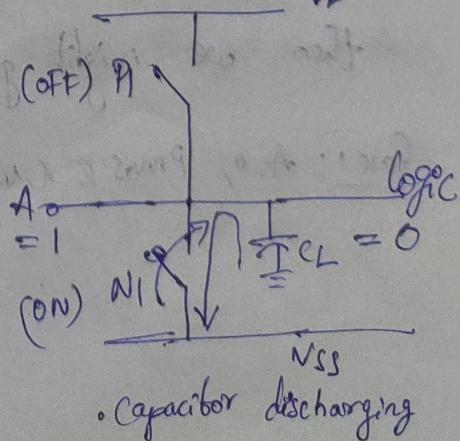


Switching Diagrams / Circuit / network

Case(i) $A=0$:

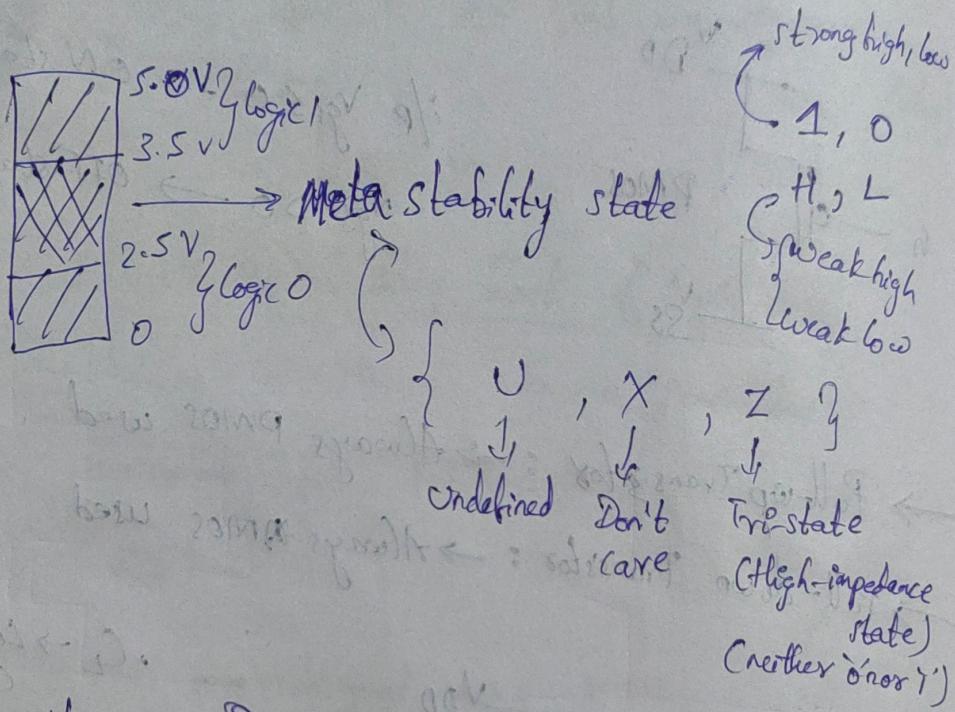


Case(ii) $A=1$



• Operational Transistor Logic (OTL)

- System knows only Left shift & Right shift.
- Adapters, RS232 → Voltage Converters
- Recommended Standard



- We won't use D-MOS, as even when $V_{GS} = 0$, small current flows.
- So never use Depletion-MOS for Inversion

17/01/2023

CMOS Logic Implementation and Analysis

- If P-MOS & N-MOS swapped in the inverter circuit, then we might get a Buffer.

Case 1: A=0, PMOS & NMOS - statics and C_c-constants changing till V_{DD} and logic '1'

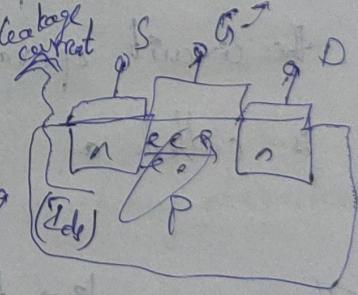
17/01/2023

Power dissipations:

$$P_{\text{Total}} = P_{\text{static}} + P_{\text{dynamic}} + P_{\text{leakage}}$$

- The total power dissipations in a circuit is the sum of static power, dynamic power dissipation & leakage power dissipation.

- Dynamic Power \rightarrow Transition from one form to other
- Static Power \rightarrow circuit in a single state for a long time.
- Leakage Power \rightarrow When L' - length of channel is then leakage current doubles.
- Based on V_{GS} applied, the length of channel changes.
- Changing the length of channel is called as Channel Length Modulation
- Sub-threshold current:
 \rightarrow Current due to recombination of e^- & e^+ (e^- in p substrate)
- Leakage current: Current goes out through some cracks, when $V_G < V_S$.
- The sub-threshold current need to go out, but it cannot go out through gate or drain and so it comes out through SiO_2 from substrate.

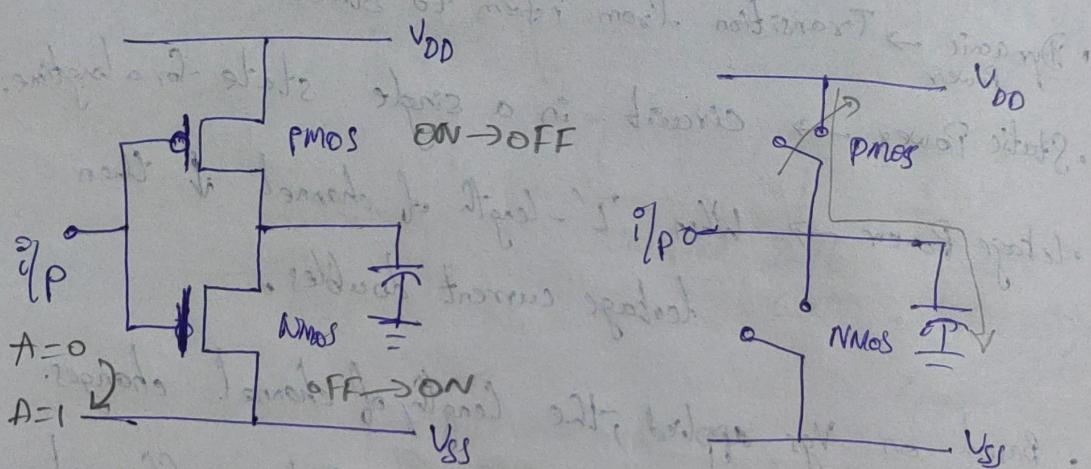


- Substrate terminal comes to picture to avoid reduce body effects and controls leakage currents.

- MOSFET is a 4 terminal device.

Static Power Dissipation :

(CMOS Inverter Logic)



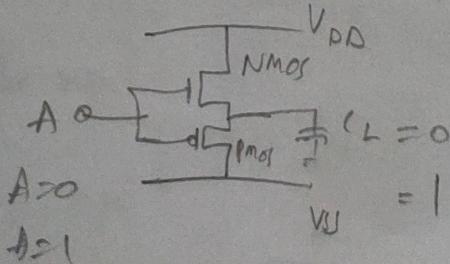
- The power dissipation observed in a circuit, when the circuit operating in a single state continuously is called as Static Power dissipation.

- The power dissipation observed when circuit continuously changing from different states, is called as Dynamic Power Dissipation.

- When Transition of one state to other state

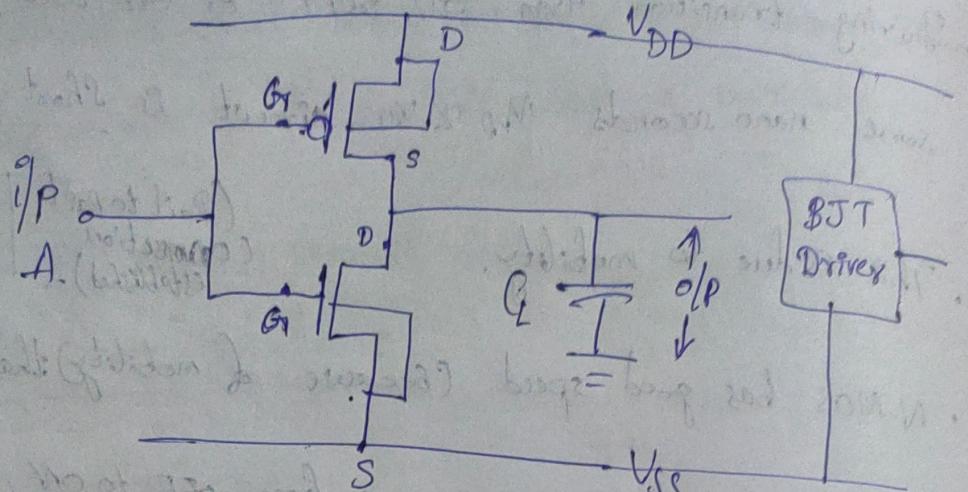
- During transition, from ON to OFF or OFF to ON, for some nano seconds V_{DD} & V_{SS} circuit is short circuited.
- This is due to mobility.
- N-MOS has good speed (because of mobility) than PMOS
- During transition, NMOS goes from OFF to ON, but the PMOS will be in ON state i.e. continuing to come to OFF state.
- Switching characteristics does not match.
- Capacitor charging and discharging does not happen desirably.
- And so, Inverter logic cannot be achieved.
- To avoid this and match the switching characteristics, we need to change the geometry of transistors.
- Design in such a way that both switching characteristics matches.

Aspect ratio: $Z = \frac{W}{L}$



D-Slope

A=0	A=1
0	1



- Body effects of Substrate: $V_{BS} > 0$ efficiency

- While fabrication, by proper doping concentration, we can avoid/control the body effects. (at fabrication level)
- By using substrate terminals, we can control body effects in the circuit

In figure, Substrate connected to V_{DD} in Pull-up transistor terminal and substrate terminal connected to V_{SS} in Pull-down transistor and so overall body effect of the circuit is nullified.

- Power dissipated when circuit operated in a single steady state continuously — P_{static} .

o/p of 1 circuit should be given to next circuit as the input, for this Driver circuit is used.

$$\text{CMOS} + \text{BJT} \implies \text{BiCMOS}$$

Logic Design Driver circuit

In BJT, high power dissipation happens

20/01/2023

Implementation of cascode logic for different circuits :

Implementation of any logic using CMOS, then the o/p of the circuit is the complementary function.

Ex: $f = a(b+c)$ - Implement using CMOS logic
 $\rightarrow P' \rightarrow \text{CMOS} \rightarrow f$ (NOT gate)

$a(b+c) \rightarrow \text{CMOS} \rightarrow \overline{(a)(b+c)} \rightarrow \text{Do } a(b+c)$
 \rightarrow But using inverter logic/NOT gate
 after CMOS logic is not suggestible, as →
 (Jitters - noise - transistors)

→ So, apply inverter logic at the input.

Input : $f = \overline{a(b+c)}$

- ↳ Delay increased
- ↳ Burden on power supply P
- ↳ IC area \uparrow
- ↳ No. of Transistor T (as to implement inverter logic $\rightarrow 2$ transistors are required)
- ↳ Power dissipation \uparrow
- ↳ Die size \uparrow

20/01/2023

De Morgan's Law : $\overline{a \cdot b} = \overline{a} + \overline{b}$

$$\overline{a+b} = \overline{a} \cdot \overline{b}$$

Sol: $f = \overline{a(b+c)}$

$$f = \overline{a} + \overline{(b+c)}$$

$$\Rightarrow \boxed{\overline{f} = \overline{a} + \overline{b} \cdot \overline{c}} \rightarrow (\text{MOS}) \rightarrow f = a(b+c)$$

Formulae

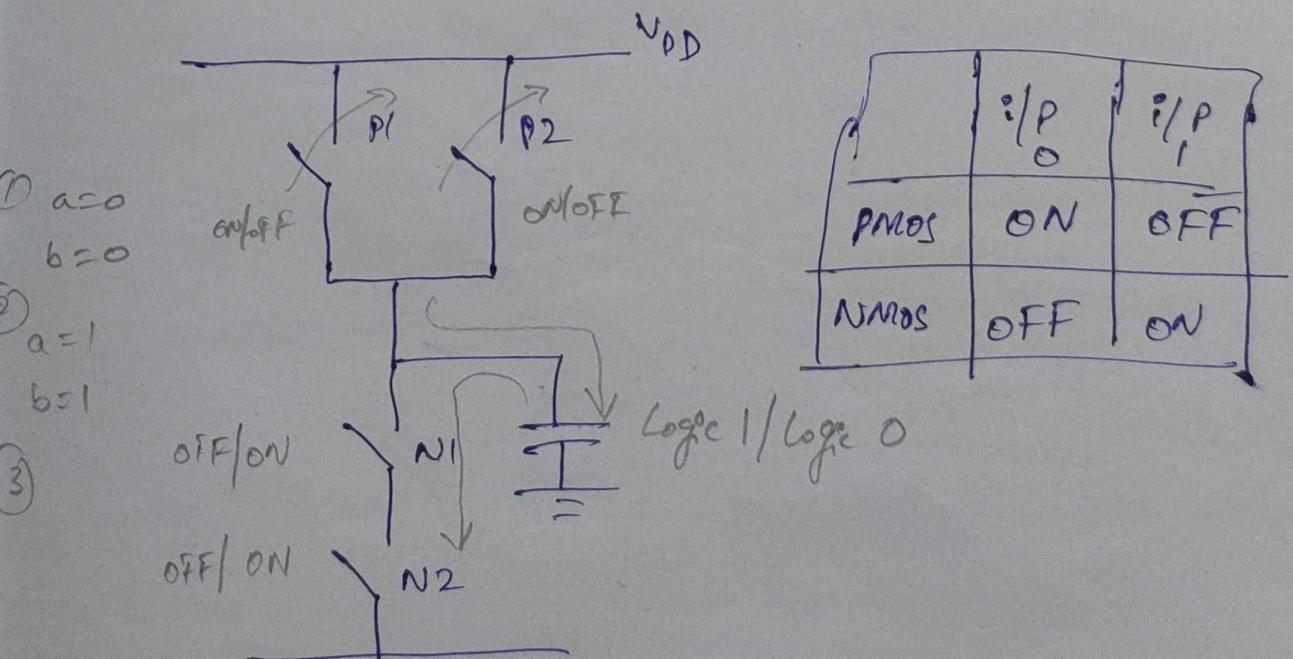
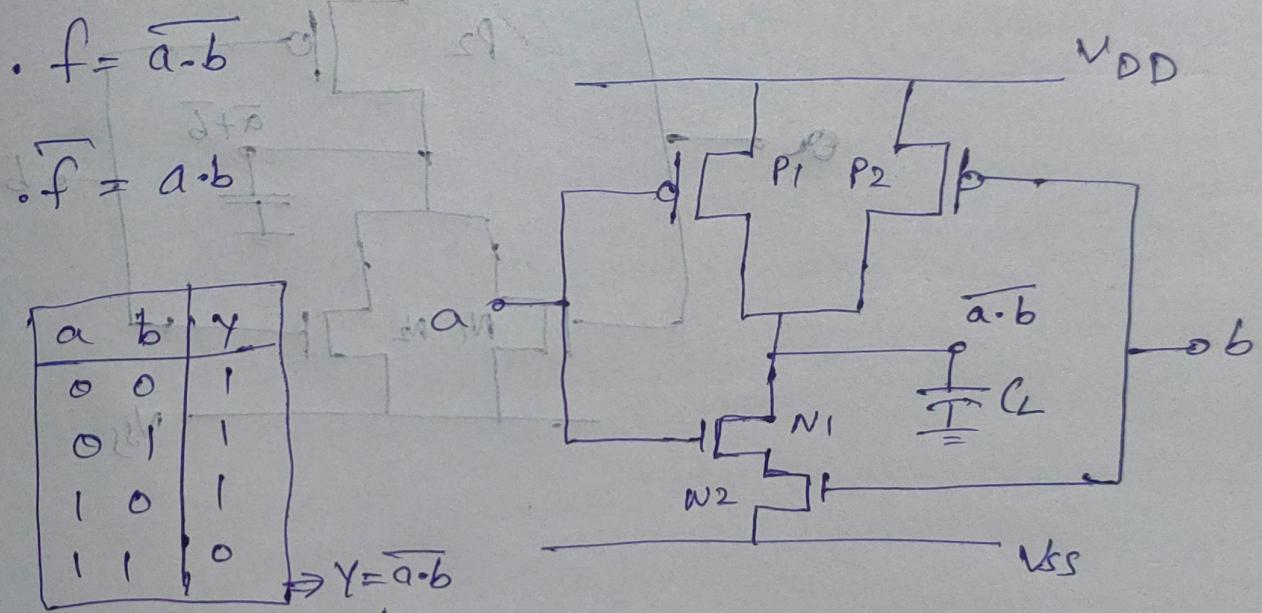
Rule 1: If in the given boolean function/ expression, (terms are in) the variables are in product then PMOS transistors should be connected in parallel, and NMOS transistors should be connected in series.

Rule 2: If in the given boolean expression, the variables are in summation then, PMOS should be connected in series and NMOS should be connected in parallel.

NOTE: $\star \star \star P - P - P$ (product - PMOS - Parallel)

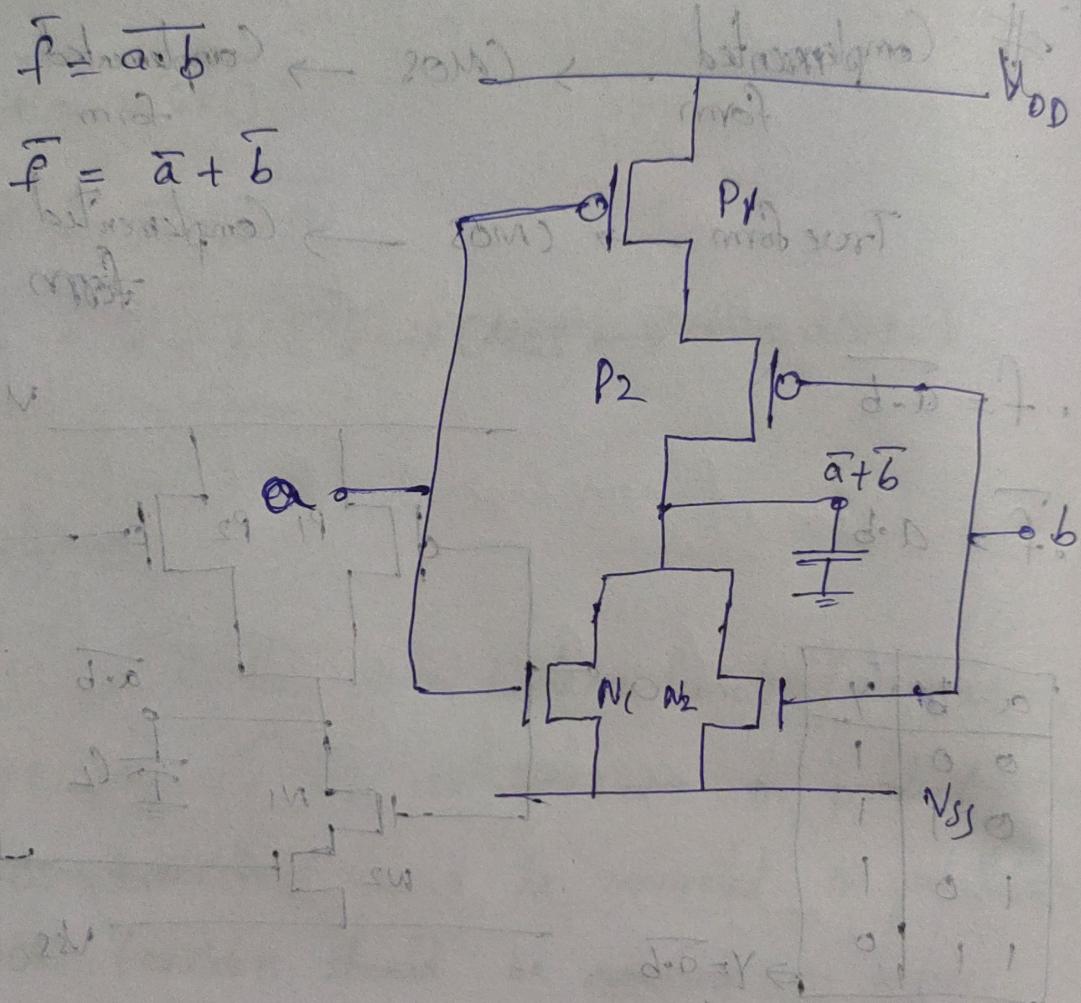
Eg: Implement $f = \overline{a \cdot b}$ (The boolean expression) using CMOS logic.

Sol: # Complemented form \rightarrow CMOS \rightarrow Complemented form
 True form \rightarrow CMOS \rightarrow Complemented form

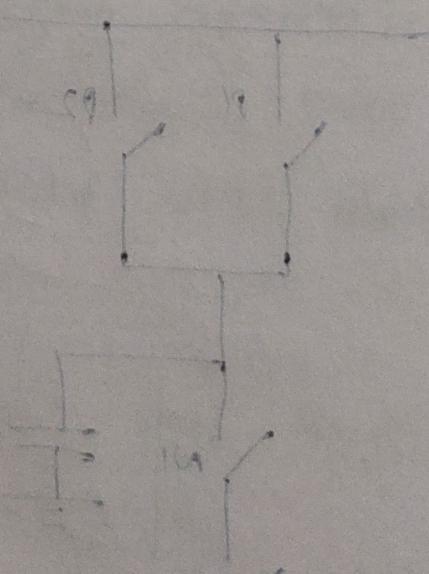


Ex: Implement $f = a \cdot b$ using CMOS Logic

so $f = a \cdot b$ (using De Morgan's Law) (\because it is in true form)



111	111	
110	110	20MΩ
101	101	



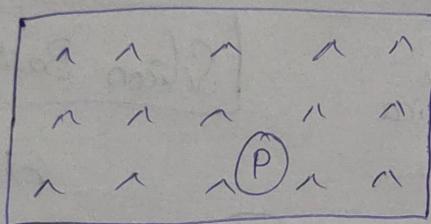
① On nMOS fabrication : p-substrate i.e. dope Si with trivalent elements like B, Al.

→ Pure Silicon chip using PVD or CVD process, it is doped.

→ nMOS has p-type substrate.

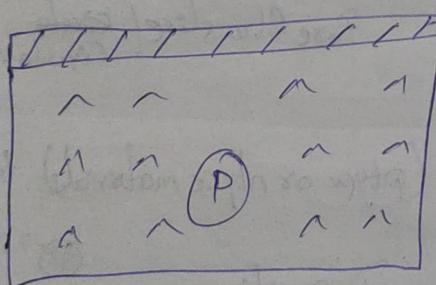
→ p-type : Dope Si chip with trivalent elements like B, Al

Step 1 :



- Pure Si is taken and doped with B/Al using PVD or CVD process.
- p-type substrate formed.

Step 2 :

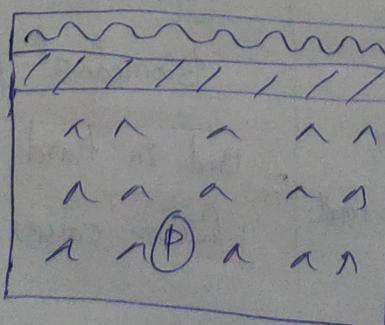


$\rightarrow \text{SiO}_2$ layer is grown deposited over the surface of p-type substrate.

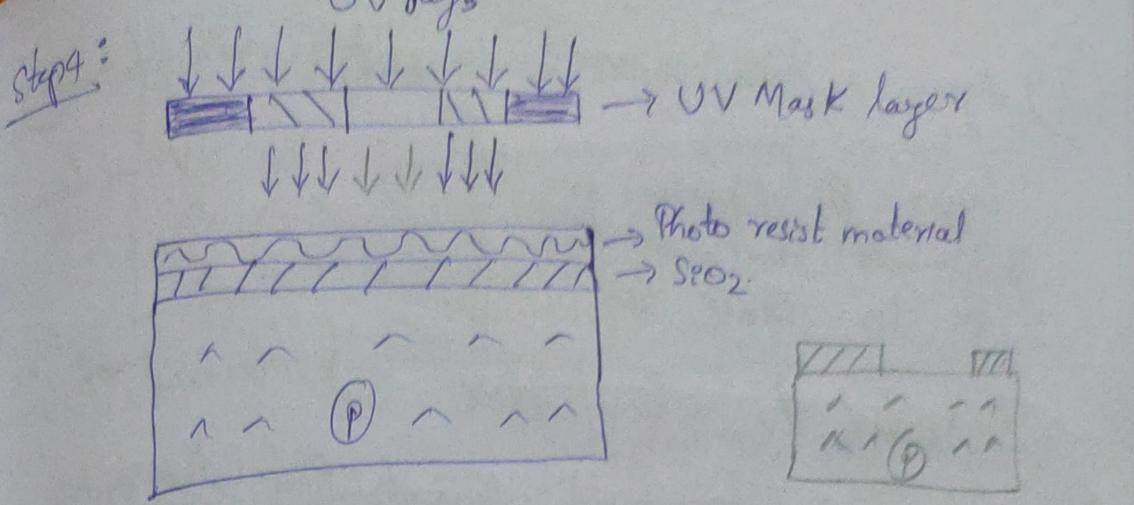
. SiO_2 has crystalline structure.

- Photo resistive material used, as SiO_2 properties may change if direct exposure to UV rays.
- Over the SiO_2 layer, photo resistive material is deposited and then subjected to spinning process.

Step 3 :



→ Photo resist layer
→ SiO_2
- after spinning process, it is uniformly distributed on SiO_2 layer.

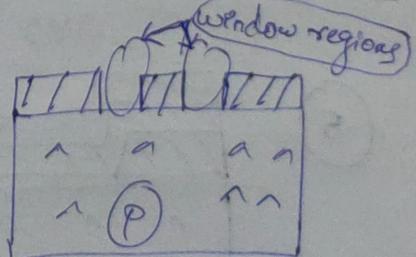


(UV rays are exposed through UV mask layer)

- In order to create ^{define} window regions for source and drain and gate terminal respectively, the p-type substrate is exposed to the UV rays through UV mask layer.
- Once, UV rays are exposed at the defined window regions, SiO₂ layer becomes very hard, then it has been hatched off.
- This complete phenomenon is called "Photo-Lithography process"

• Window region - The space where Drain, Source, Gate need to be created

• Laying a layer on SiO₂ & setup exposed to UV rays through UV mask layer & SiO₂ layer is hatched off
- Photo Lithography Process



⑤ Again a SiO_2 layer is deposited, again photoresist layer is exposed to UV rays via UV mask layer & so gate terminal is achieved

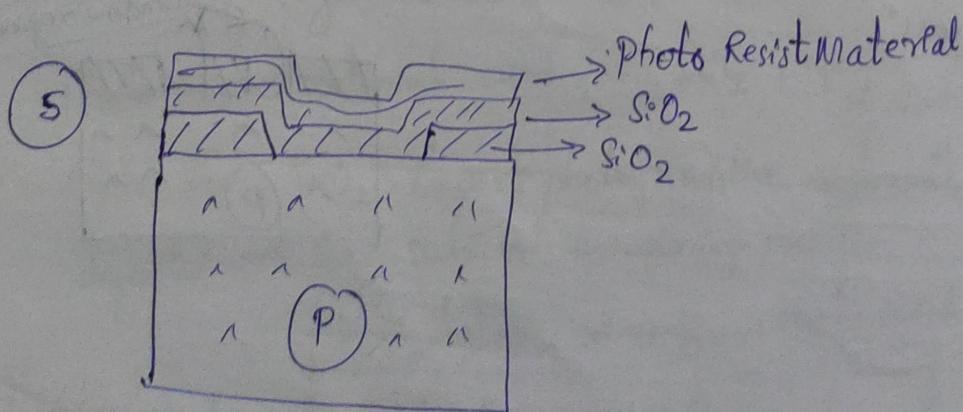
→ In order to achieve define gate terminal, it is again processed through Photolithographic process

⑦ PolySilicon deposited - Photo Lethographic process

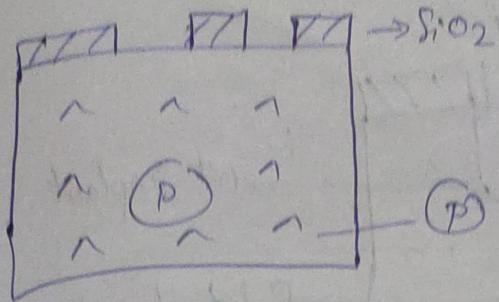
⑧ Poly deposited on gate terminal Region

⑨ n^+ implant, CVD/PVD process is used for n^+ implantation. n^+ implants are diffused

⑩ Al layer deposited over the layer.

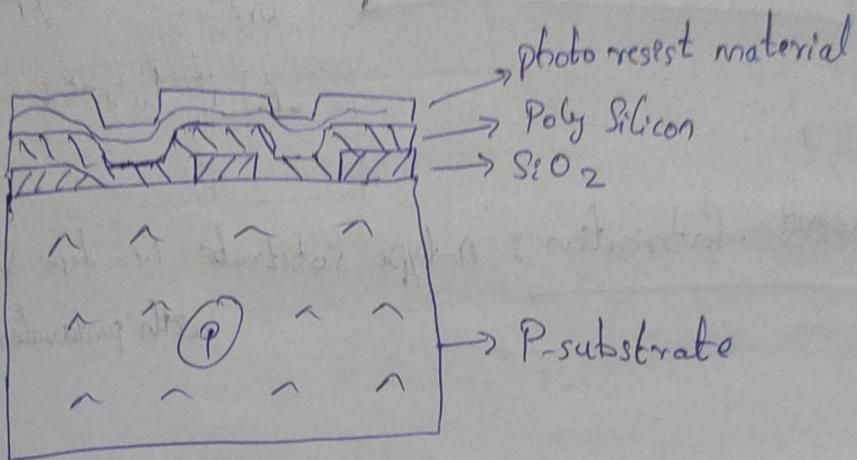


⑥

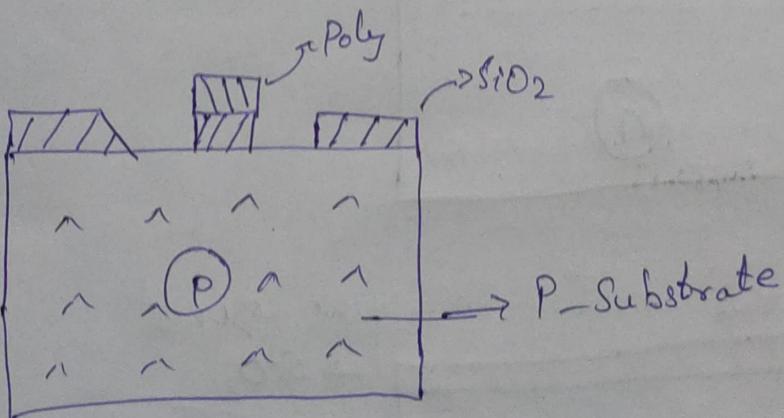


⑥ Substrate / Body / Bulk

⑦

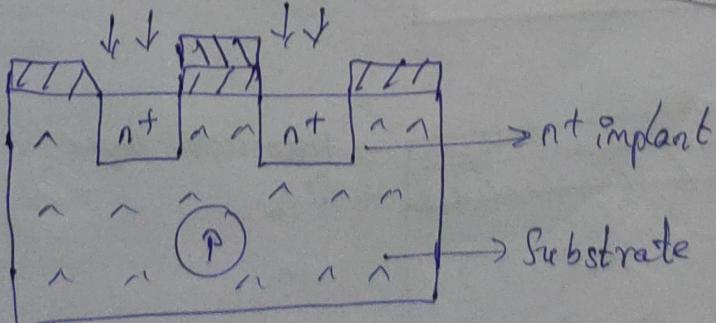
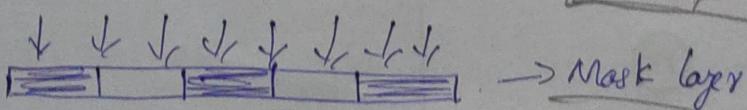


⑧

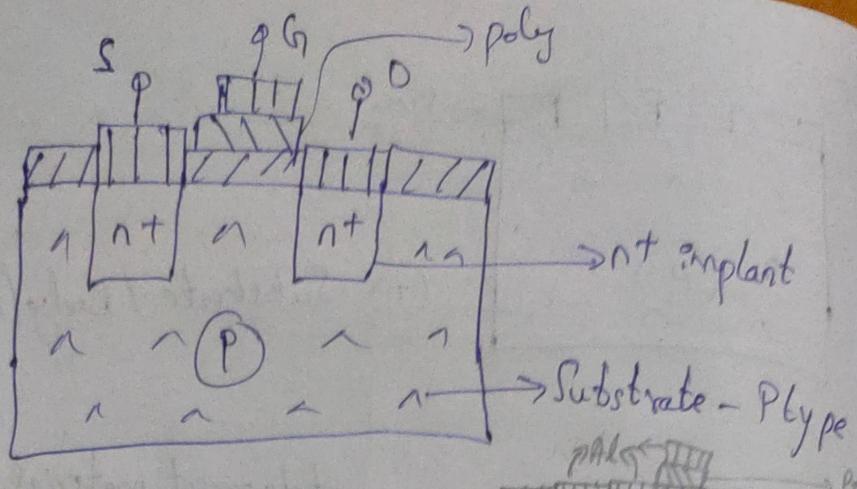


CVD process

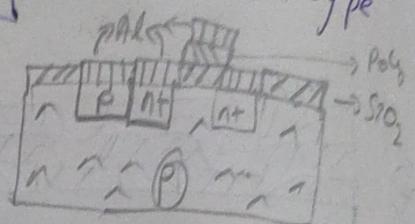
⑨



(10)

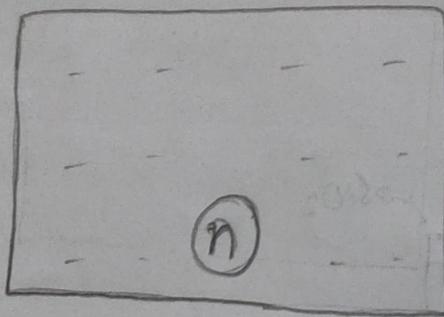


S.S terminal :

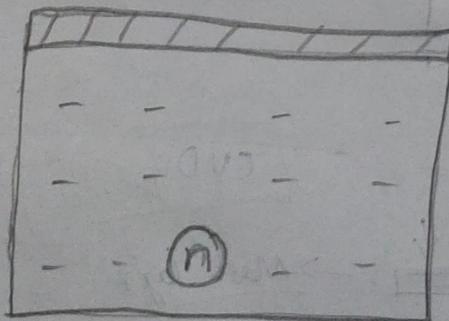


P-MOS fabrication : n-type substrate i.e. doped Si with pentavalent elements

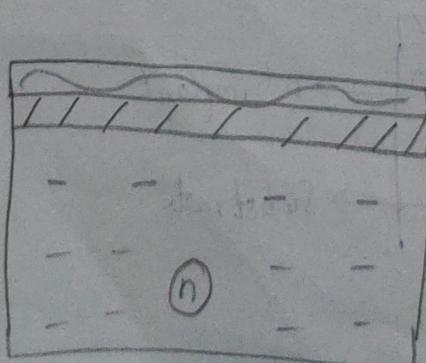
(1)

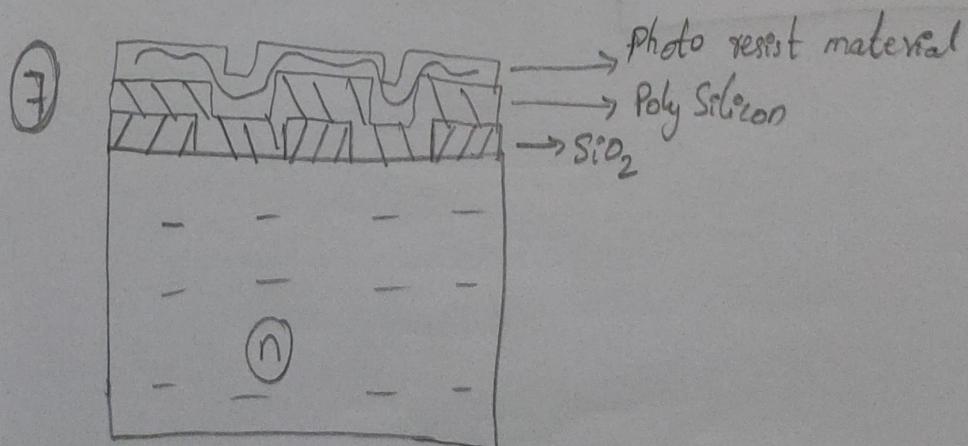
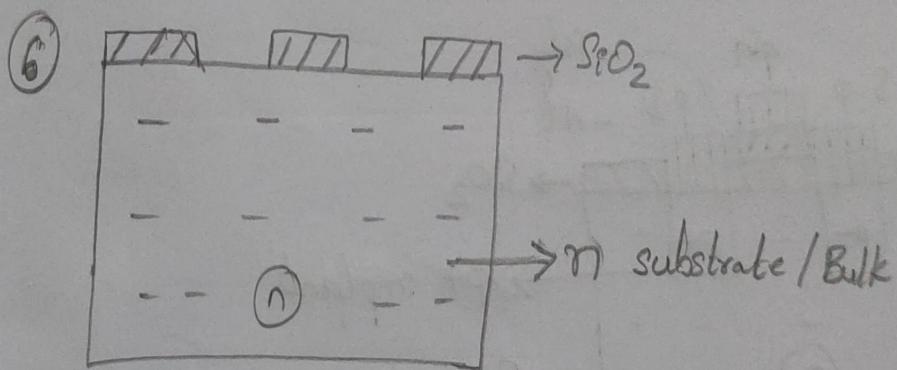
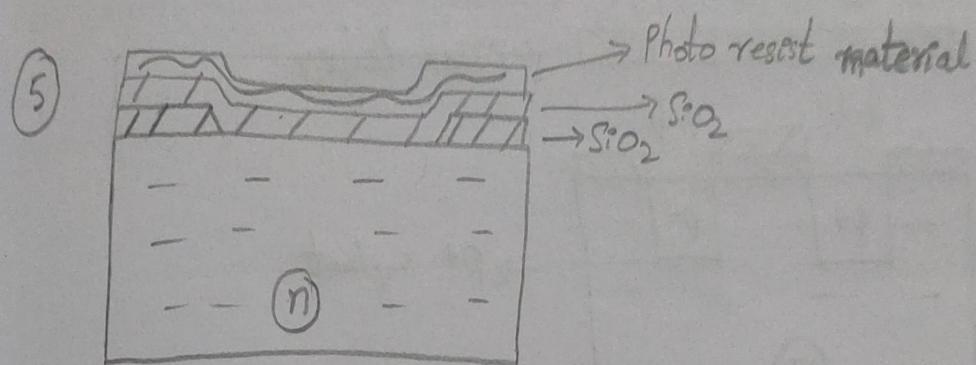
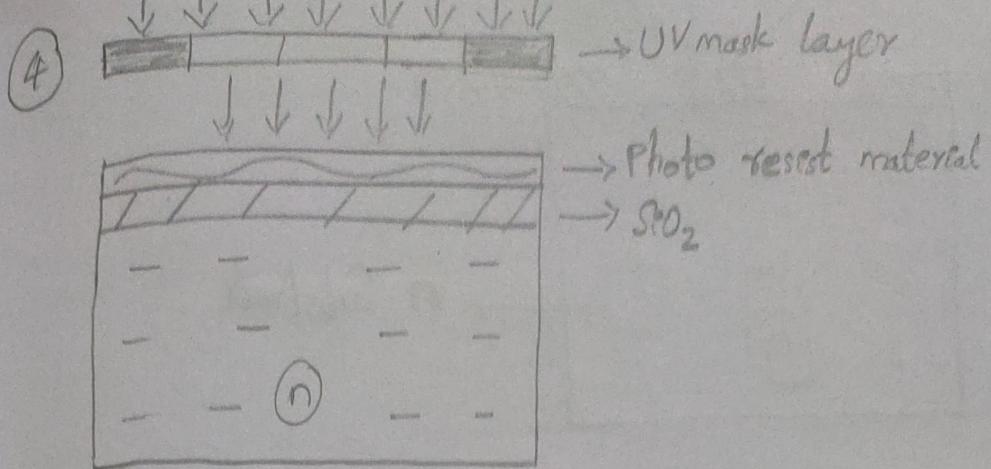


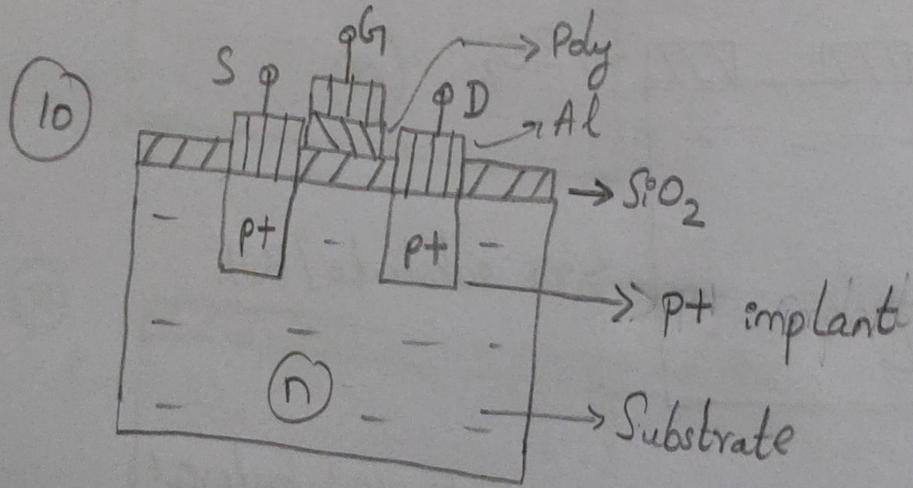
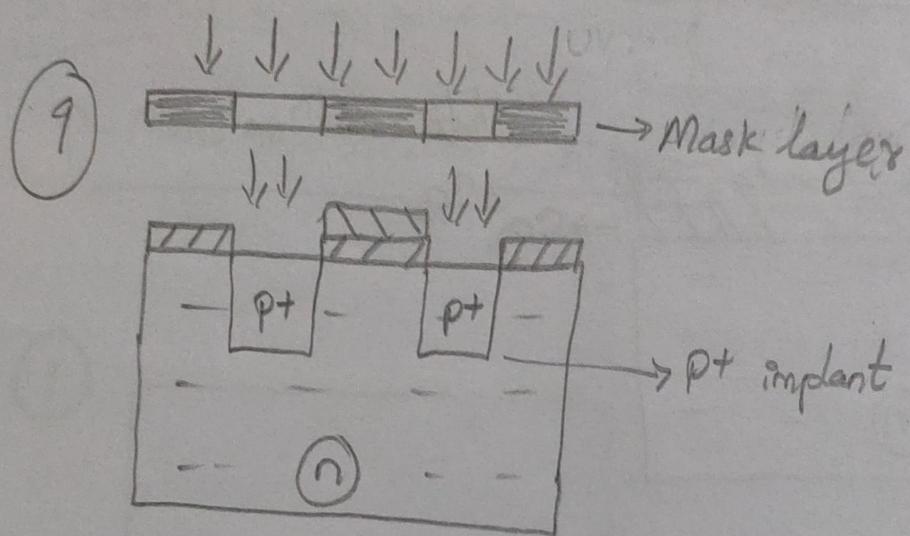
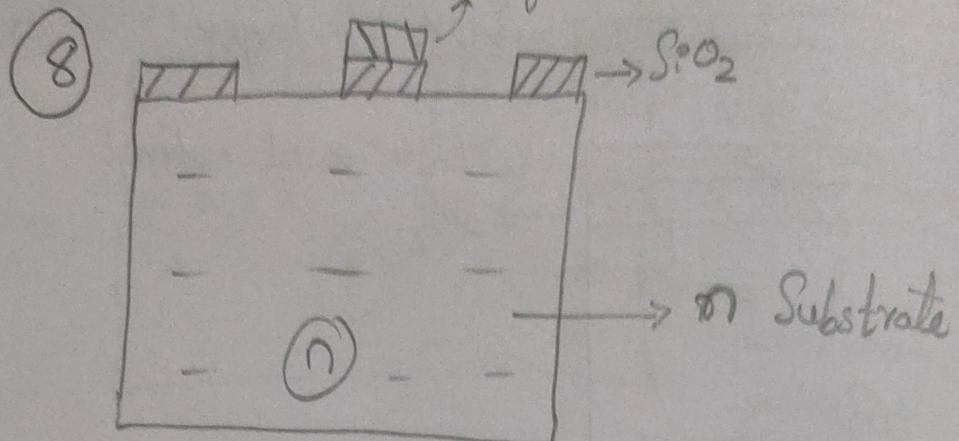
(2)



(3)



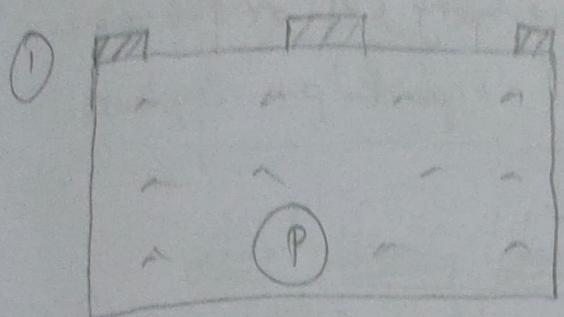




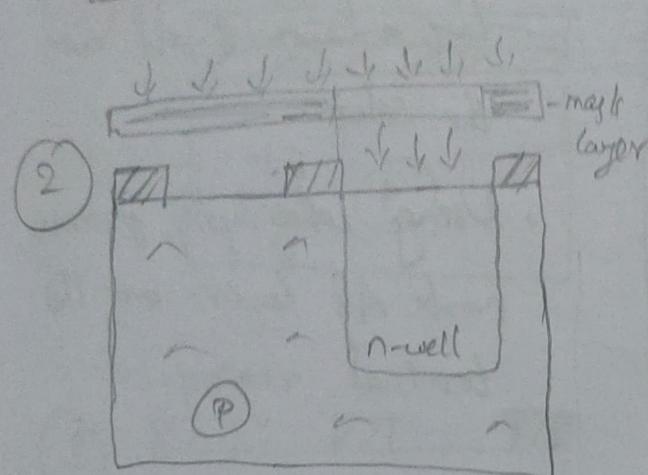
③ CMOS Fabrication process

30/01/2023

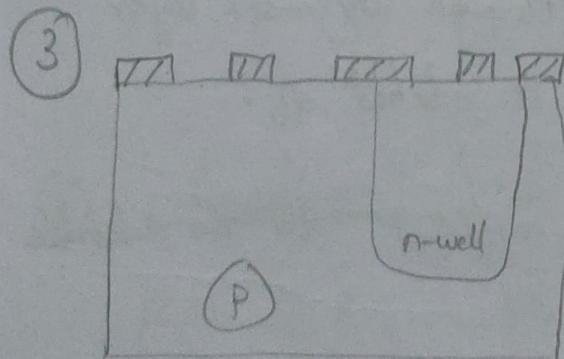
(i) n-well process :



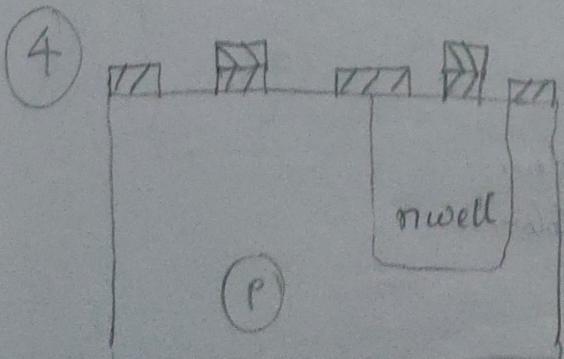
- Take a p-type substrate
- Lay SiO_2 layer over the substrate surface
- Using Photolithography process, create window regions



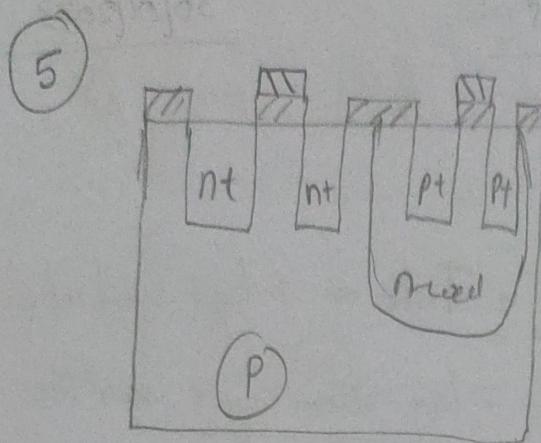
- Using CVD or PVD process, implant n-well



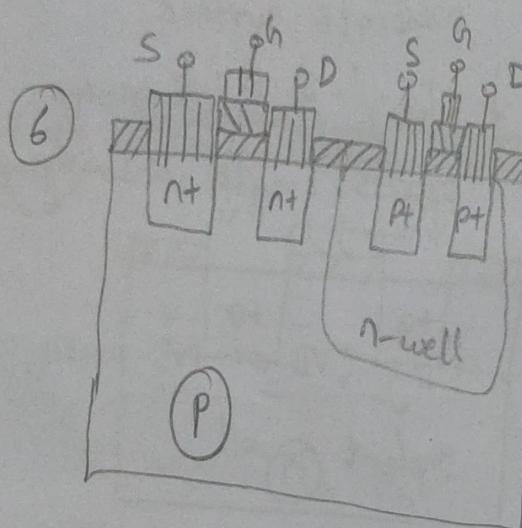
- Lay a layer of SiO_2 over the setup
- Using Photolithography process create gate terminal regions



- Lay a layer of poly silicon
- Using photolithography process create poly layer on gate terminal regions



- Using CVD or PVD process
implant pt implants
 - Using CVD or PVD process
implant pt implants



- Lay a layer of Al over the setup.
 - Using ^{Photo}Lithography process, create Al layers over the terminal regions.

Photo Lethography process: laying a layer & exposing the setup to UV rays, through UV mask layer and the unnecessary layer is etched off.

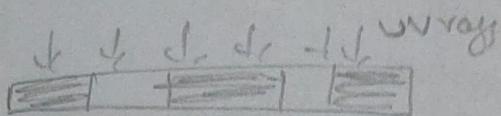
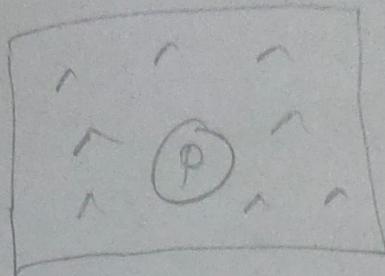
→ CVD process: n+ / p+ implants implanted into the substrate via mask layer

- 2 Types of SiO_2 
 - Thin ($0.1\text{ }\mu\text{m}$)
 - Thick ($1\text{ }\mu\text{m}$)

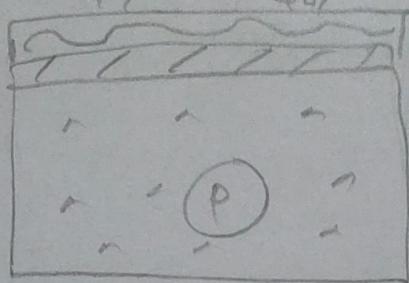
- 2 Types of Poly silicon - I - Red colour
- II - Orange colour

N-well process

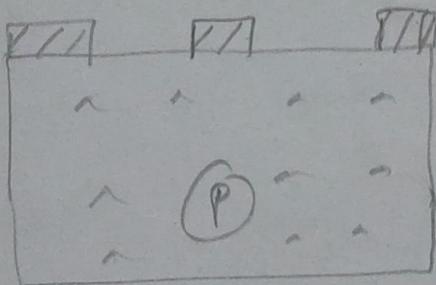
(1)



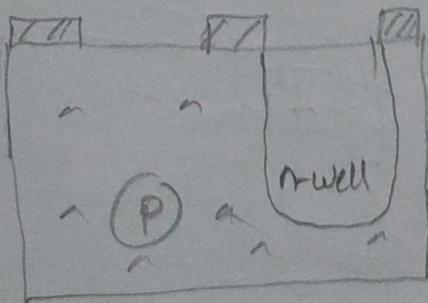
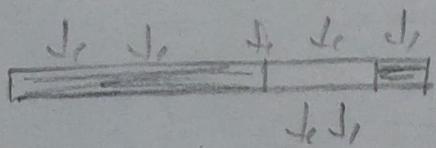
(2)

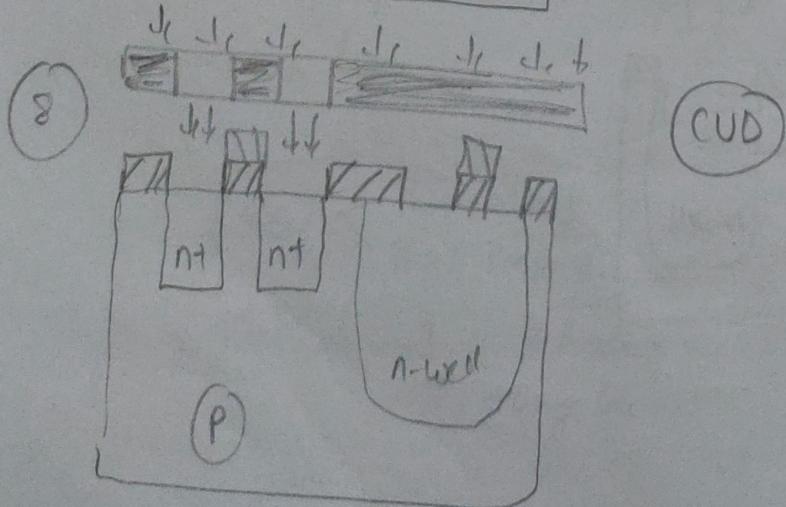
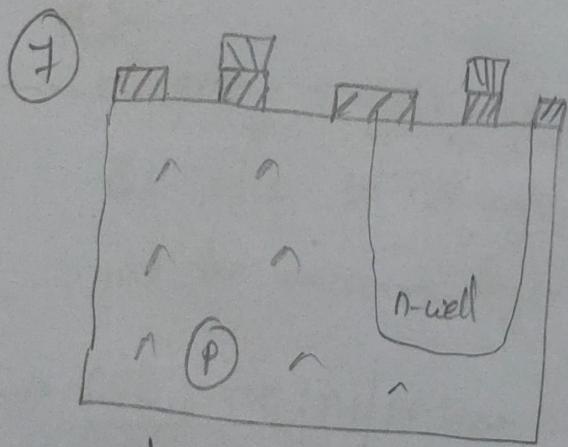
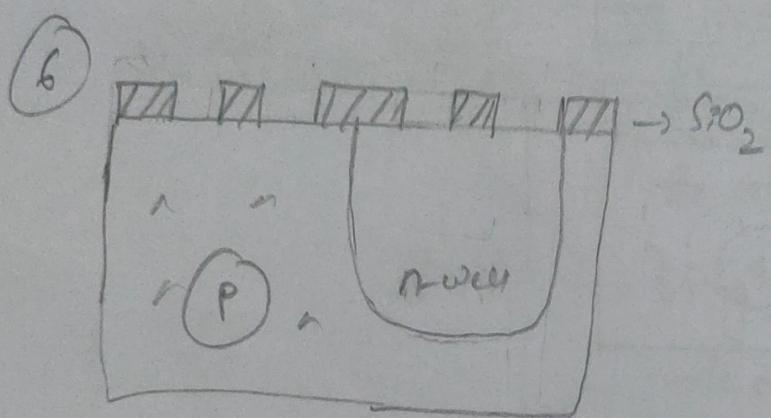
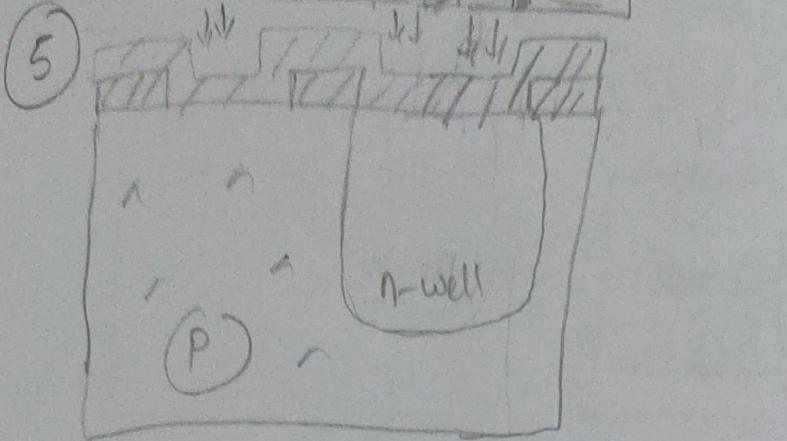


(3)

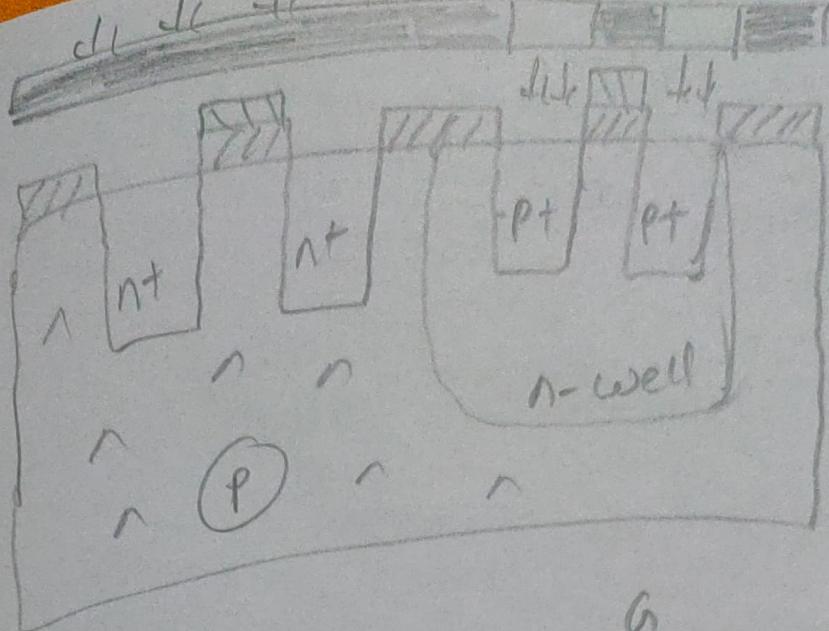


(4)



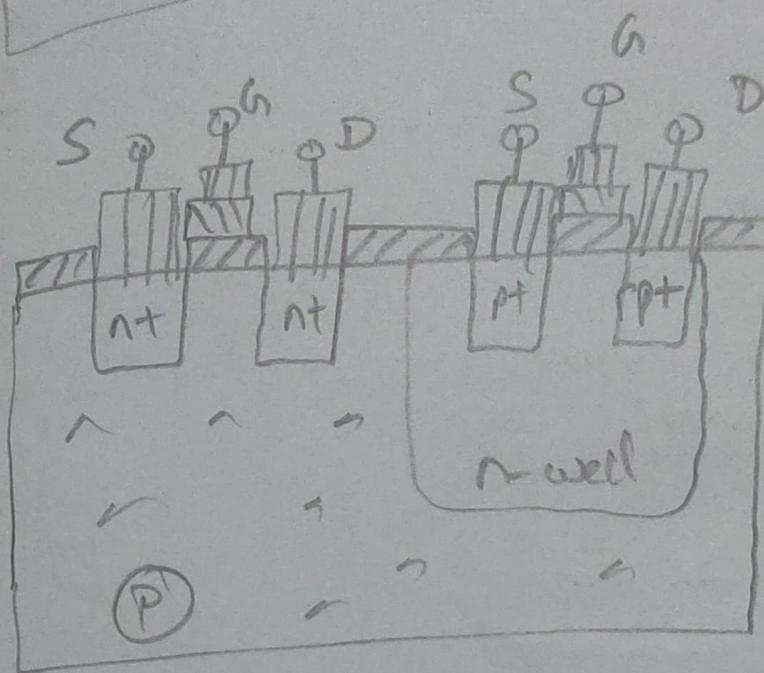


⑨

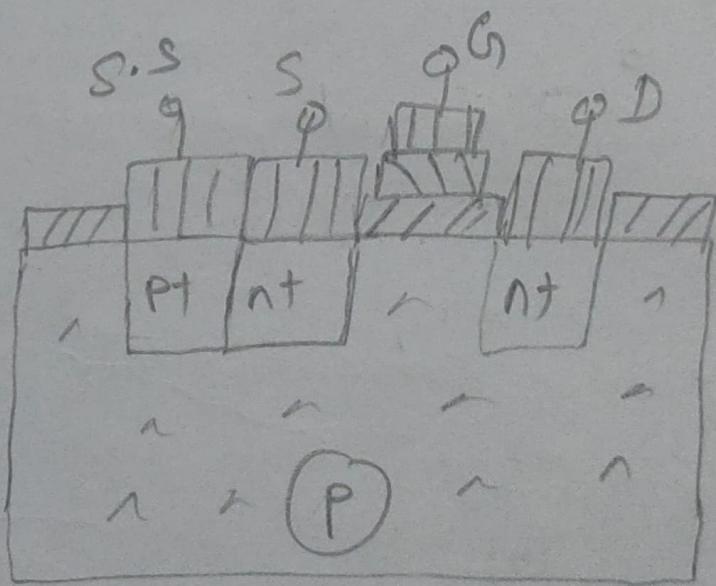


CVD

⑩

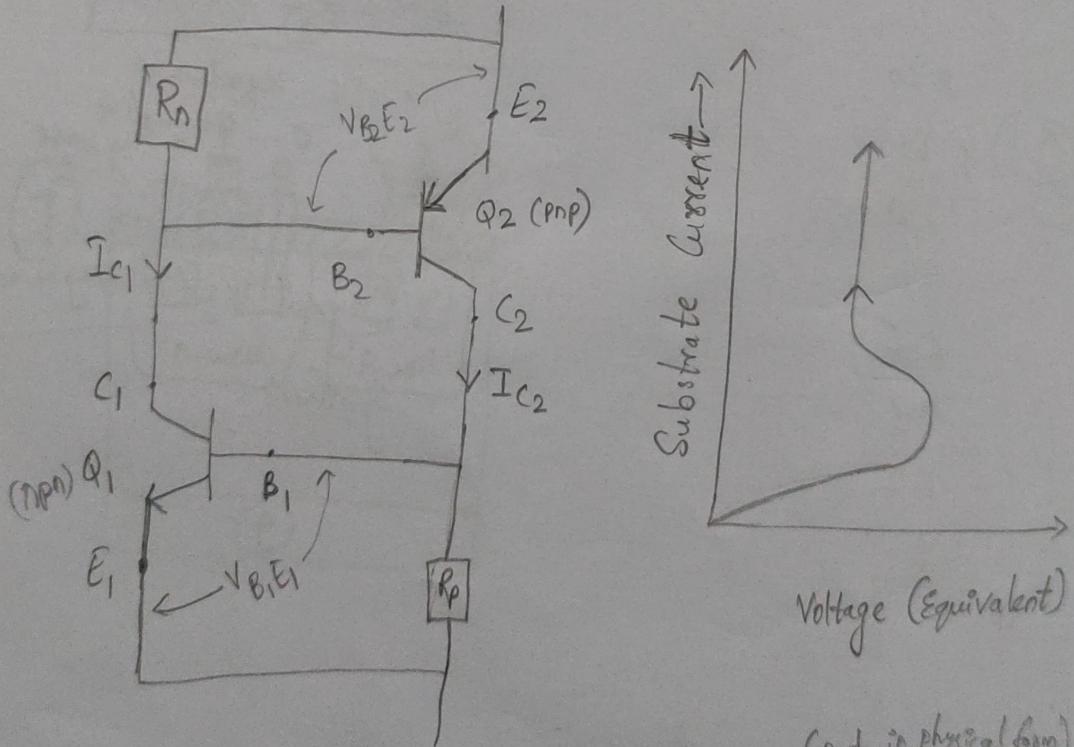
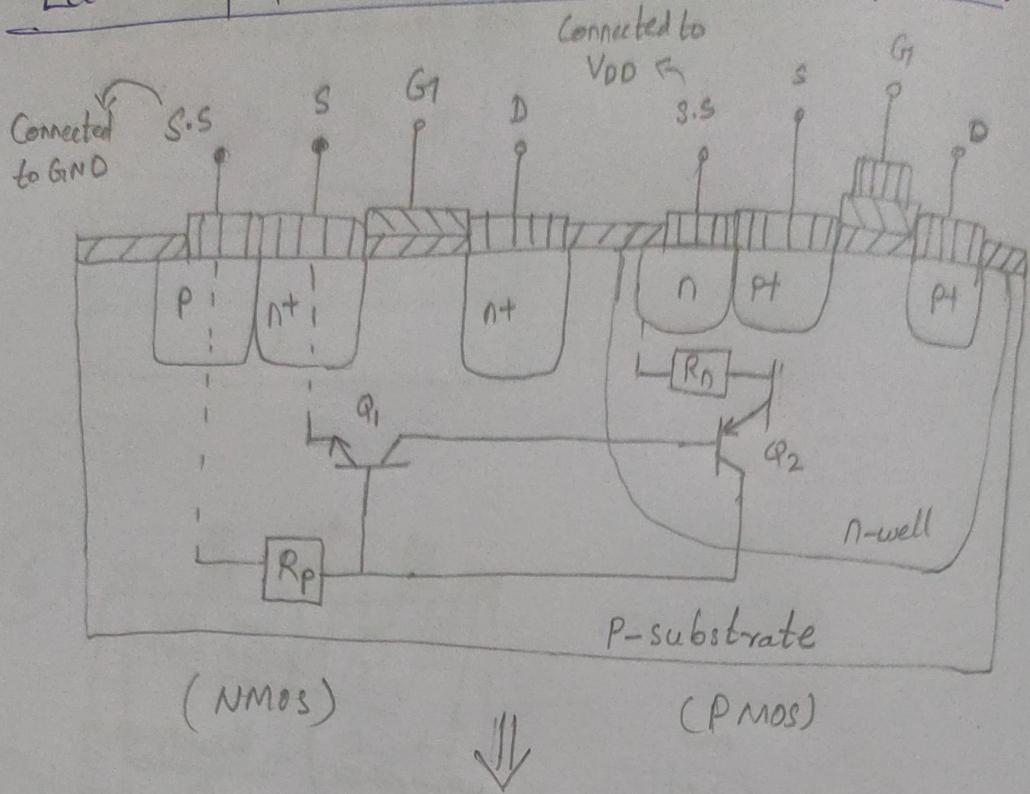


(NMOS -



- We come across with latch-up problem in case of n-well & p-well process.
- n-type & p-type implants in n-well or p-well process has a virtue of formation of npn & pnp BJT transistors.
- A closed path observed.
- If one transistor starts triggering, it triggers the other transistor.
- Transistor-2 comes to ON state, it again triggers Transistor-1.
- Transistor-1 comes to saturation state and triggers Transistor-2.
- Transistor-1 & 2 in saturation state, & so leads to damage of IC.
- This Latch-up problem is overcome in Twin-Tub process.
- Using Isolation Technique, virtual transistor formation is avoided, this is achieved by using Epitaxial layer
Crystalline SiO₂

Latch-up problem in CMOS fabrication process.

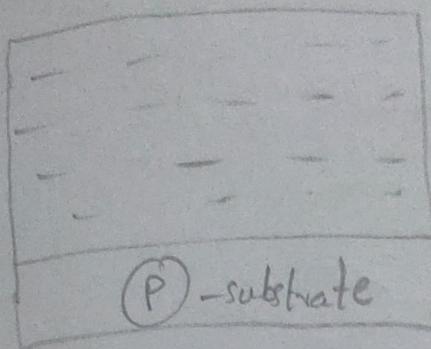


- R_p - Equivalent resistance in p-substrate } (not in physical form)
- R_n - Equivalent resistance in n-well } formed at the fabrication level

↳ depends on doping conc. & depth of implants
↳ litho

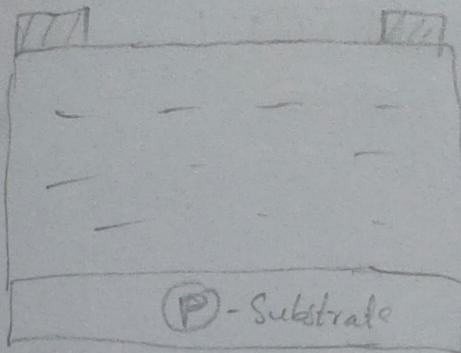
Twin-Tub process

①

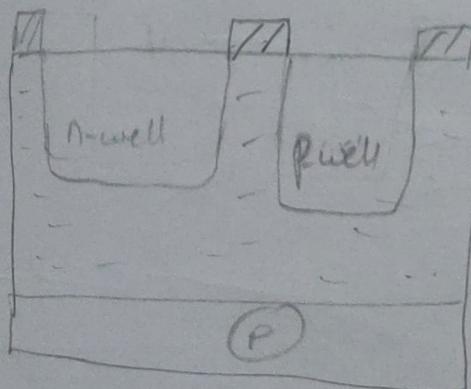


→ 75% of p-substrate
is grown with a
Epitaxial layer.
↳ (Has neither +ve nor -ve
potential)

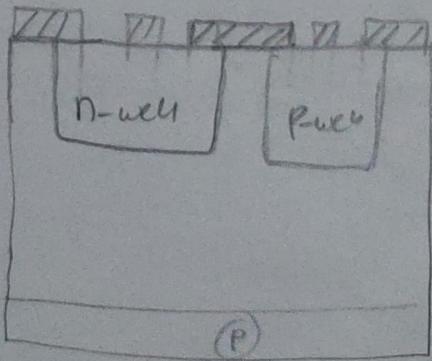
②



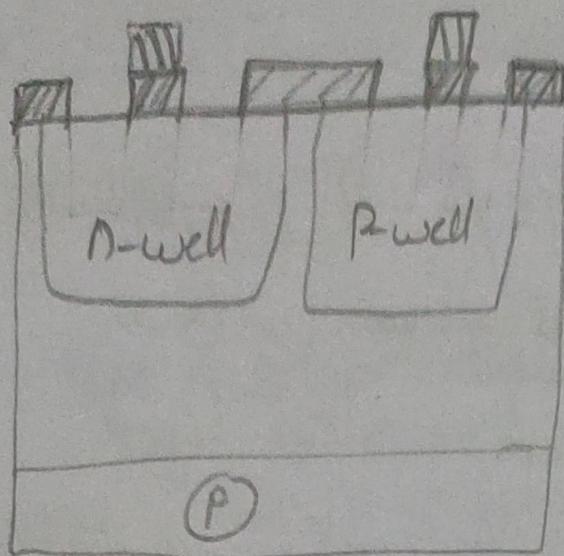
③



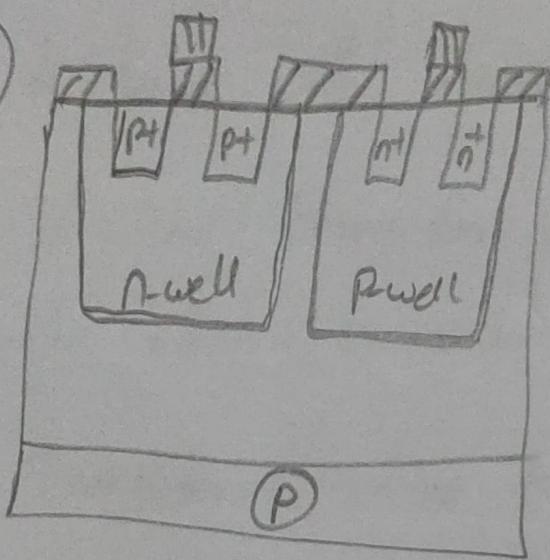
④



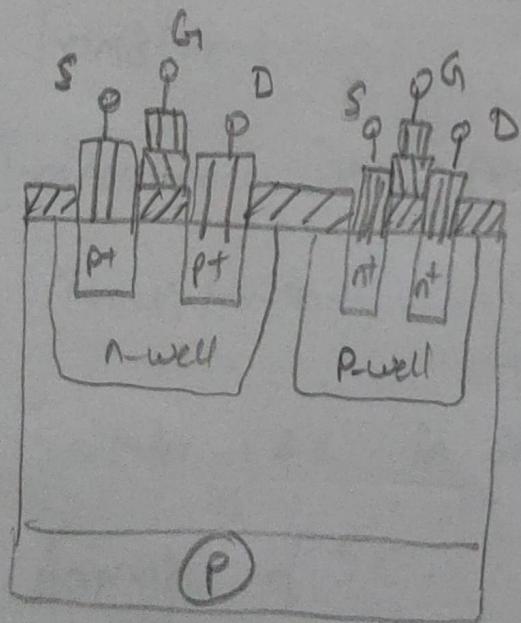
(5)



(6)



(7)



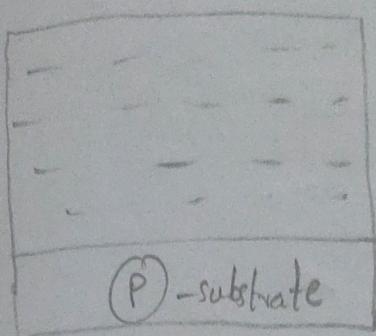
- We come across with latch-up problem in case of n-well & p-well process.
- n-type & p-type implants in n-well or p-well process has a virtue of formation of npn & pnp BJT transistors.
- A closed path observed.
- If one transistor starts triggering, it triggers the other transistor.
- Transistor-2 comes to ON state, it again triggers Transistor-1.
- Transistor-1 comes to saturation state and triggers Transistor-2.
- Transistor-1 & 2 in saturation state, so leads to damage of IC.

\Rightarrow This Latch-up problem is overcome in Twin-Tub process.

- Using Isolation Technique, virtual transistor formation is avoided, this is achieved by using Epi-taxial layer
 \hookrightarrow Crystalline SiO_2

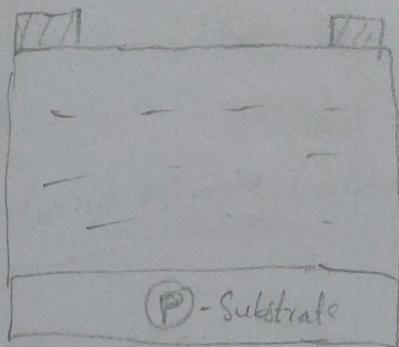
Twin-Tub process

(1)

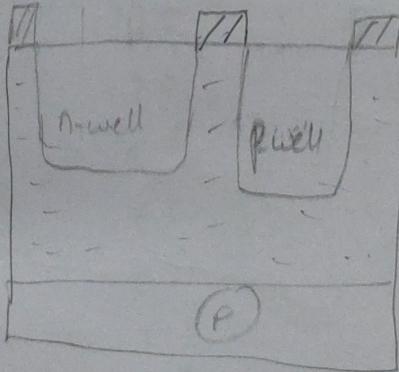


→ 75% of p-substrate
is grown with a
Epitaxial layer.
↳ (has neither +ve nor -ve
potential)

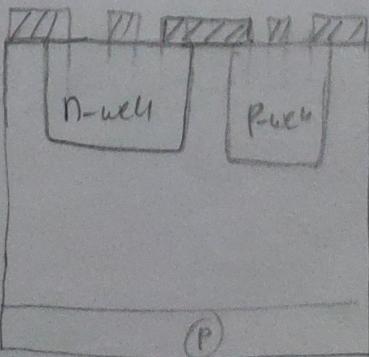
(2)



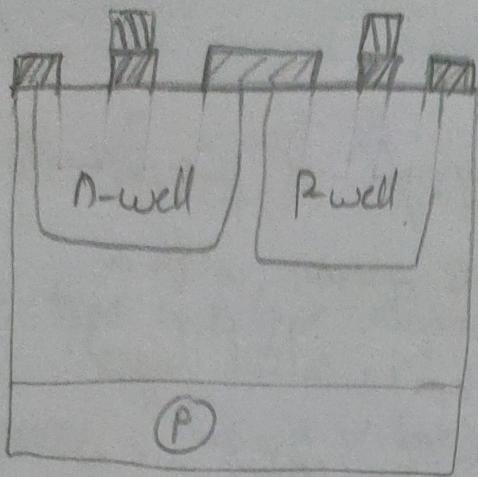
(3)



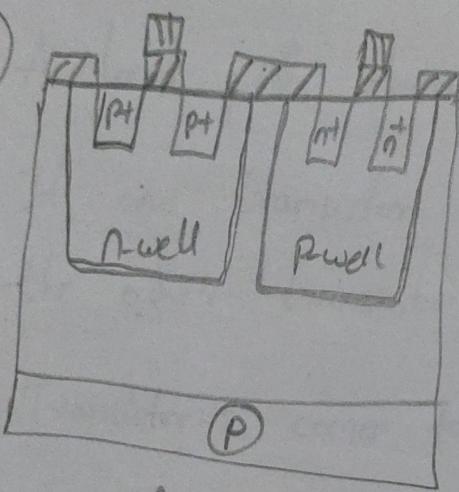
(4)



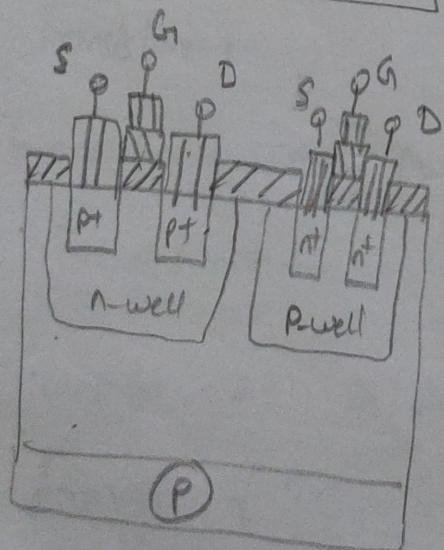
(5)



(6)

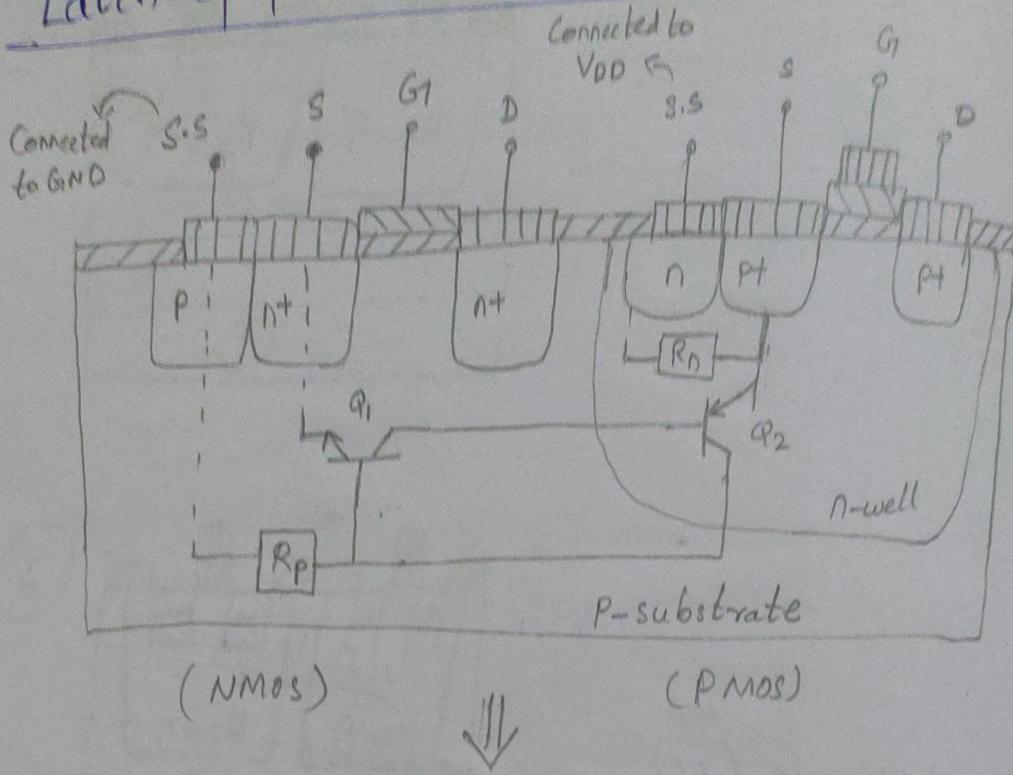


(7)



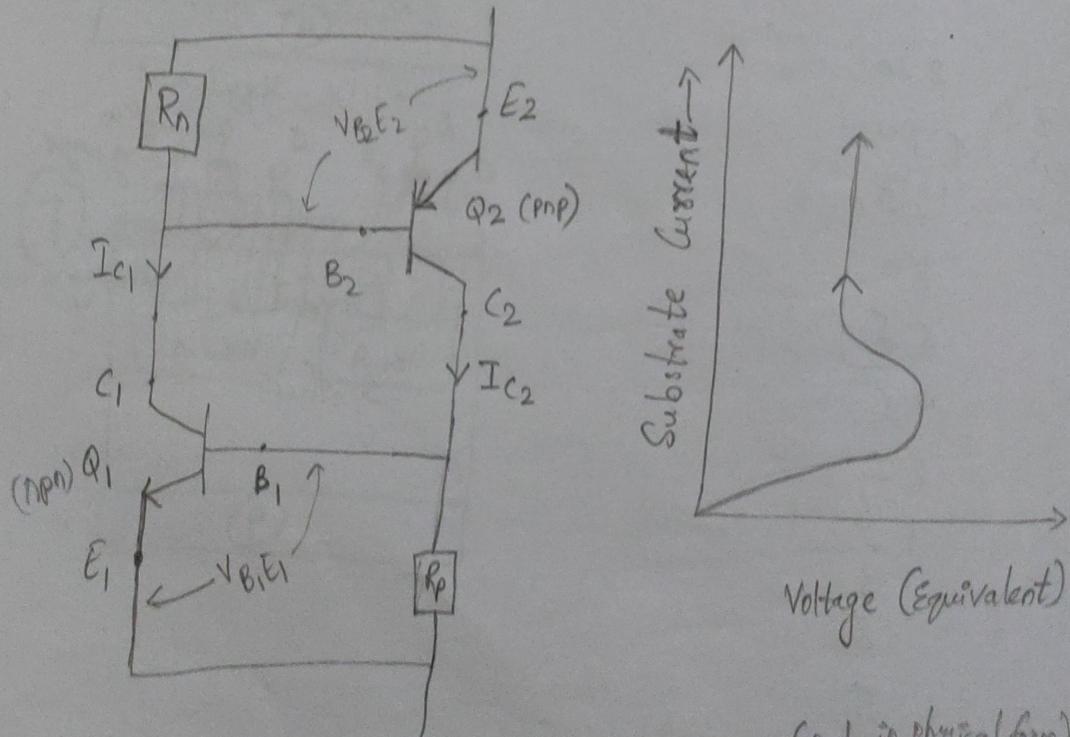
07/02/2023

Latch-up problem in CMOS fabrication process:



(NMOS)

(PMOS)



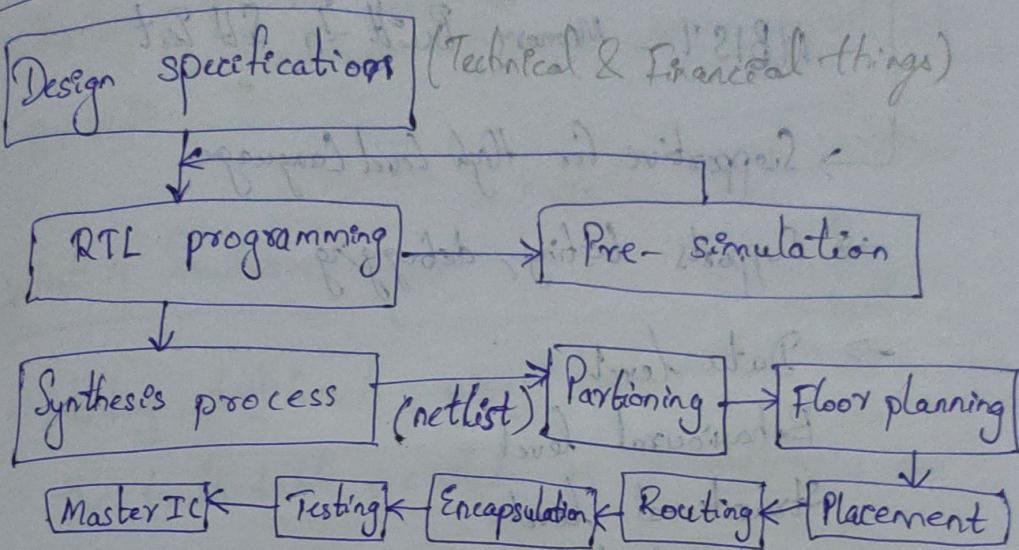
- R_p - Equivalent resistance in p-substrate } (not in physical form)
- R_n - Equivalent resistance in n-well } formed at the fabrication level

↳ depends on doping conc. & depth of implants

↳ glitch

27/02/2022

VLSI Design flow:



- Register - Transfer Level Programming - RTL

RTL programming:

- Language: ABEL



PASCAL



HDL (Hardware Descriptive Language) (1950s-1960s)

VVM



VHDL (Very High speed HDL /



Very Large Scale IC HDL)

System Verilog
(OOPS) ← Verilog

- VHDL → fails to support OOPS concept

→ fails to debug

→ not user friendly (not a HLL)

→ The header file here called as Package → Library → keyword

- Verilog : Verification Language

- Verilog : has rigorous testing
 - MBIST - Memory Built-In Self Test
 - Supportive for High Level Language
 - Supports testing, debugging
 - Data level
 - Behavioural level
 - Structural level
 - Gate level
 - Transistor
 - Scatter
 - MOS
 - Does not support OOPs concept
- System Verilog supports OOPs concept

Nanometer Technology :

220 nm

180

120 (outdated)

90

65

45

22

16

13

7

5

3nm

Verilog

cannot be used

(not comfortable)

(easier)

problem of Jitter

shorter time for

and difficult to do

interfacing ; problem

UVM - User Verified Methodology

→ Verilog + MATLAB + PYTHON

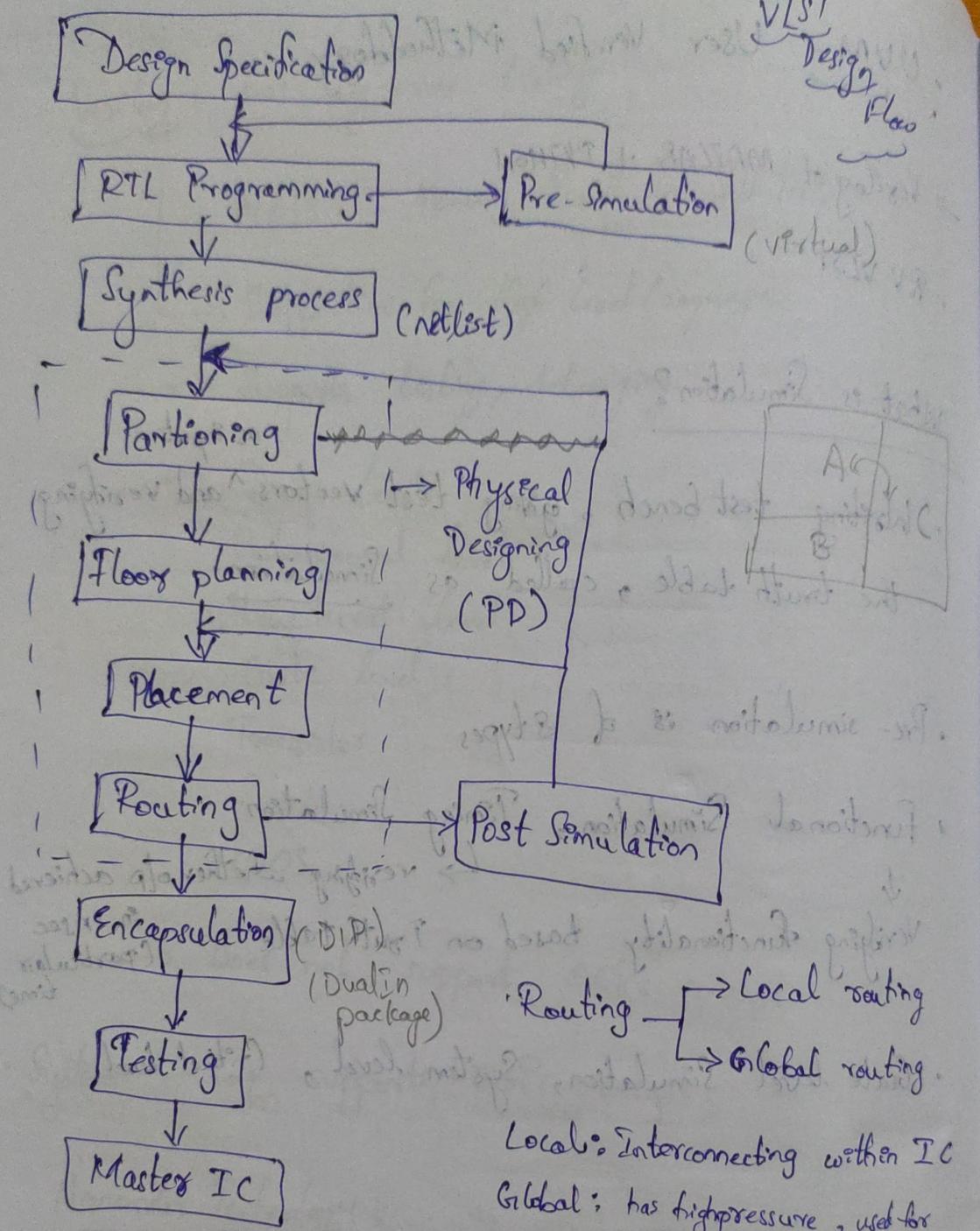
RV VLSI

What is Simulation?

- Writing test bench, giving test vectors[^] and verifying the truth table, called as Simulation.
- Pre-simulation is of 8 types
- Functional Simulation → Timing Simulation
 ↳ verifying whether op achieved Verifying functionality based on Truth table in 1sec (particular time)
- Gate level Simulation, System level, Critical level.

Synthesis process:

- Generation of netlist is so called as Synthesis process.
- Synthesizer synthesis the process code & generates the netlist.
- Netlist is list of components.



Partitioning, Floor planning, Placement - these 3 steps go in parallel i.e. hand-in-hand.

Stick Diagram & Layout Design

28/02/2023

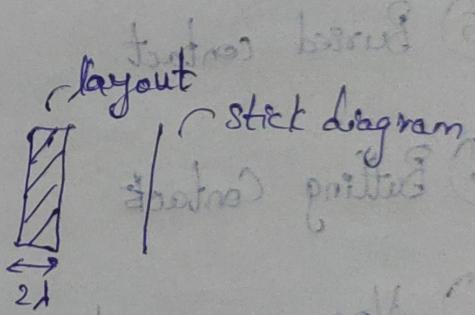
- Layout is an area or space for construction/fabrication.
- Layout deals with size/dimensions of space.
- ↳ Speaks about all geometry of the circuit.

① Cartoon representation of layout is called Stick Diagram

• Stick diagrams do not represent geometry but represents layout.

Ex: P-diffusion \rightarrow yellow colour

n-diffusion \rightarrow green colour



② Stick diagrams do not have geometry, whereas layout speaks about geometry.

③ Layout speaks about geometry (of the circuit).

• Stick Diagrams

• Layout

↳ Rules (Lambda rules)

μ-Rules (Microm rules)

Color codings of different Mask layers

(based on 220/180nm)

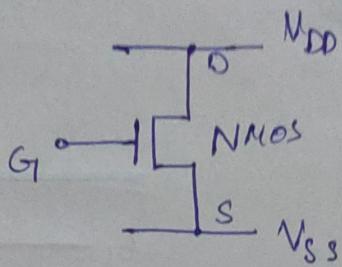
① P-diffusion	Yellow
Mask layer	Colour
② n-diffusion	Green
③ polysilicon-1	Red
④ Polysilicon-2	Orange
⑤ Buried contact	Black
⑥ Butting Contact	Brown
⑦ N _{DD} power supply (Metal-1)	Dark Blue/Purple
⑧ V _{SS} / Ground	Dark Blue
⑨ Via contact	(Just a cross) 
⑩ Internal Routing (Metal-2)	Light Blue
⑪ n-well / implant	Dashed Yellow box (square one) (Discontinuous)
⑫ De-Marcation line	Discontinuous Brown line

Line which bisects the pull-up & pull-down region

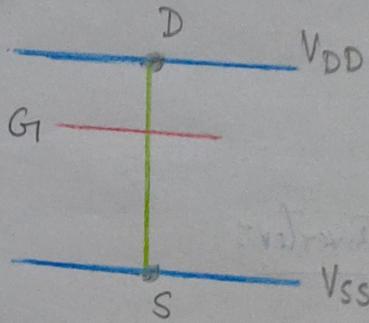
There is no separate representation for pull.
(screen itself is pull?)

① N-MOS transistor:

Circuit Diagram:



Stick Diagram:

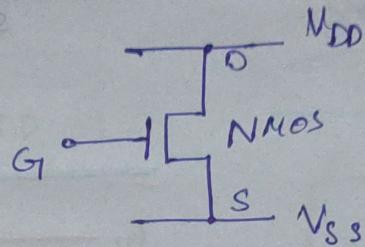


- These colour coding used for upto 45nm technology
- Different technology has different colour coding.
- Technology Foundry
- 7 metals - different colour
- Each metal has different sheet resistance
- Cat tools

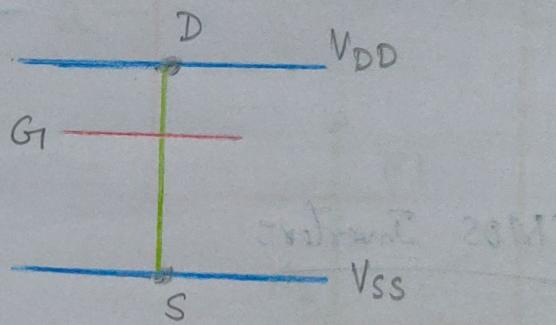
- Line which bisects the pull-up & pull-down region.
- There is no separate representation for pwell.
(screen itself is pwell?)

① N-MOS transistor:

Circuit Diagram:



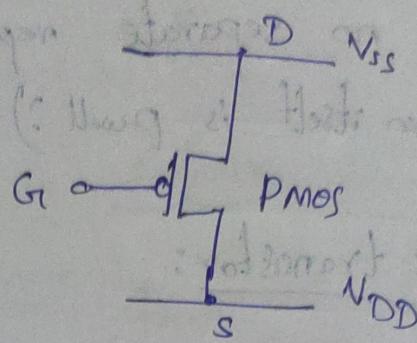
Stack Diagram:



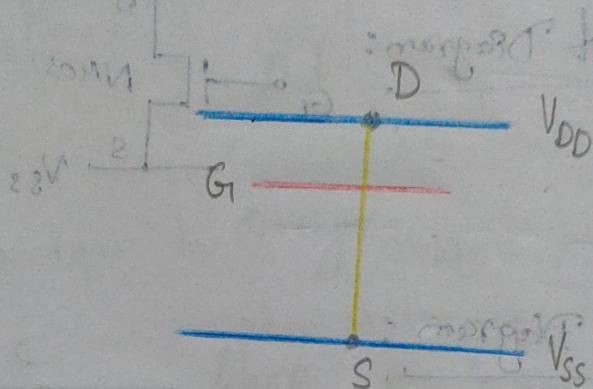
- The colour coding used for upto 45nm technology.
- Different technology has different colour coding.
- Technology Foundry
- 7 metals - different colour
- Each metal has different sheet resistance
- Cat tools

PMOS transistor

Circuit diagram:



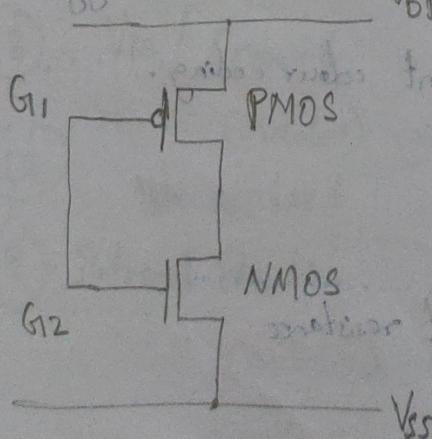
Stick Diagram:



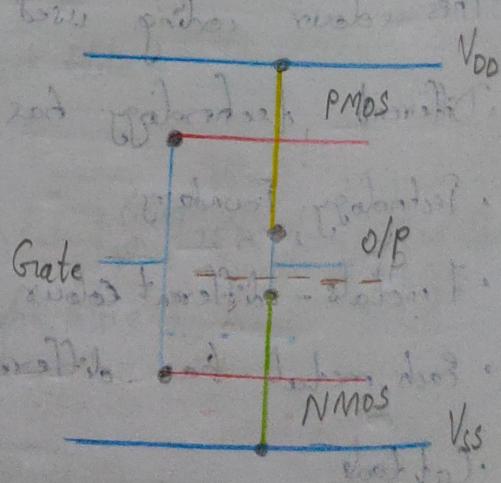
03/03/2023

CMOS Inverter:

Circuit Diagram:



Stick Diagram:



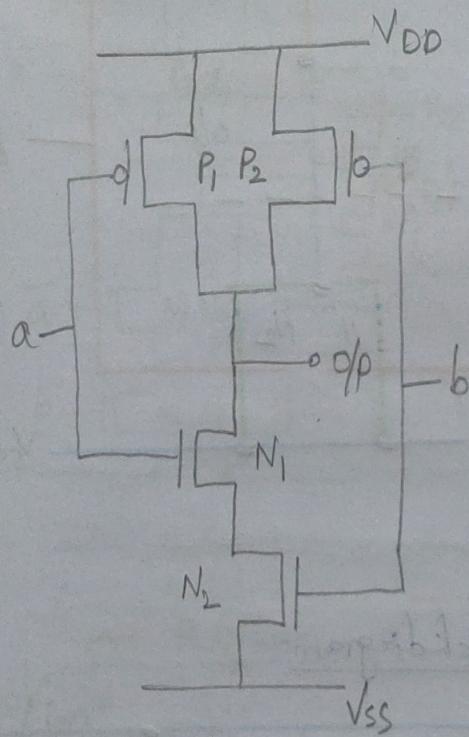
- Linear resistance
- Sheer resistance

- Optimized utilization of materials usage and ~~size~~ size.

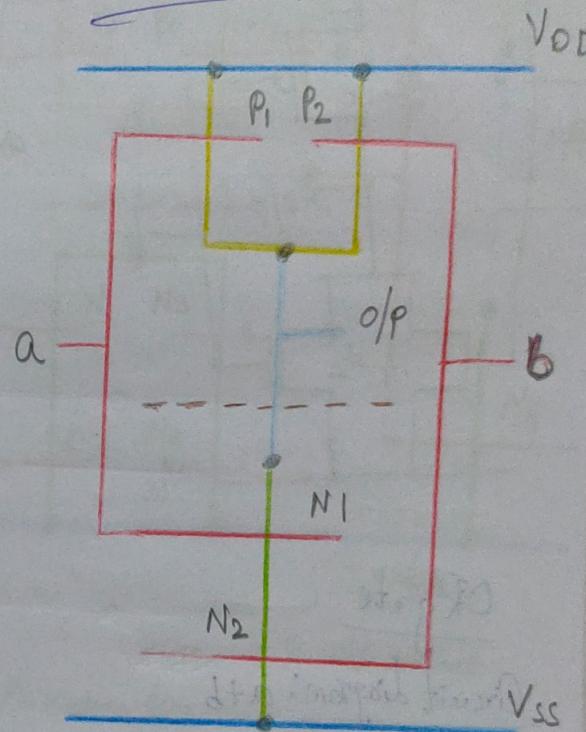
— Metal-1
 — Metal-2
 — P-diffusion
 — n-diffusion
 — poly
 - Buried contact
 - - - DeMocration Line

NAND gate:

Circuit diagram: $\overline{a \cdot b}$



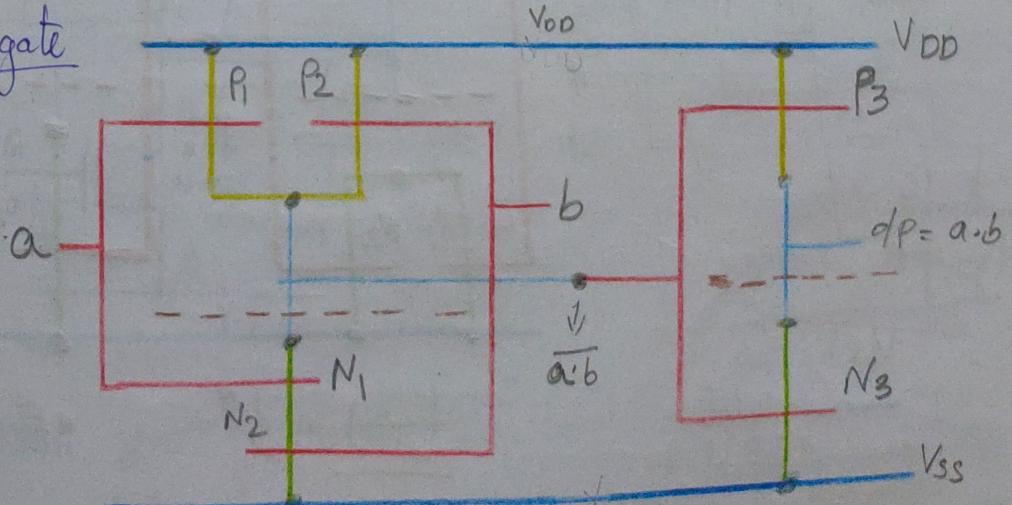
Steck Diagram:



— Metal-1
 — Metal-2
 — P-diffusion

— n-diffusion
 — poly
 - Buried contact
 - - - De Mocration line

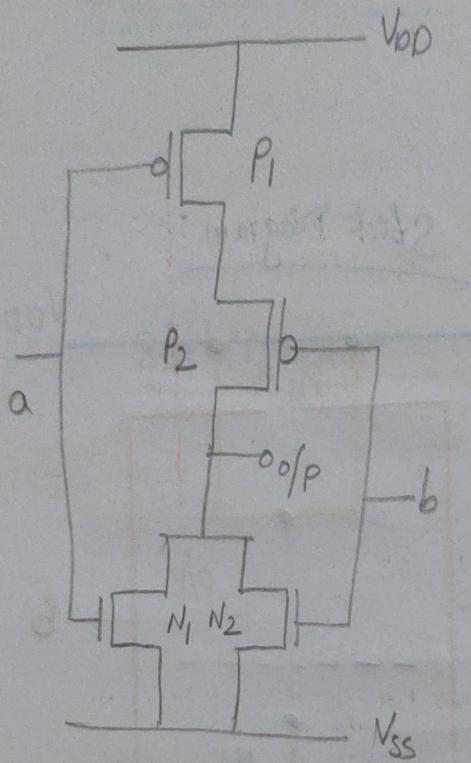
AND gate ($a \cdot b$)



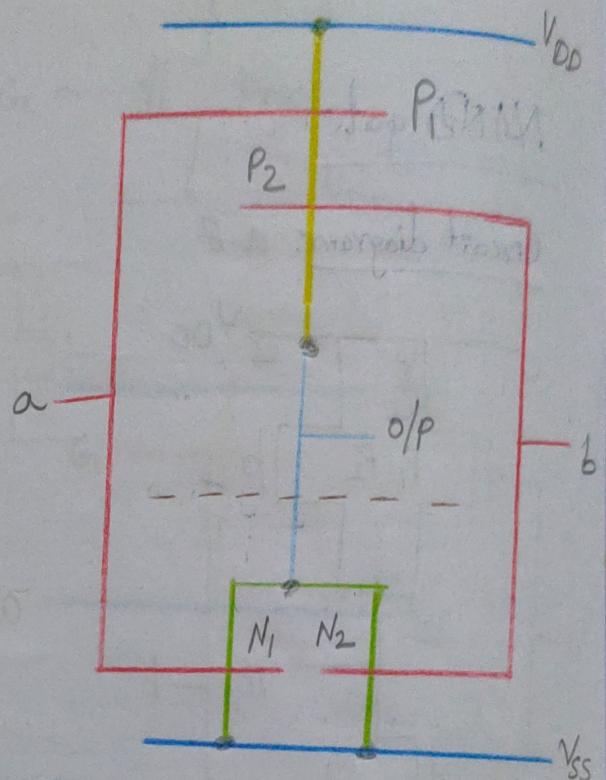
NOR gate

06/03/2023

Circuit diagram: $\overline{a+b}$

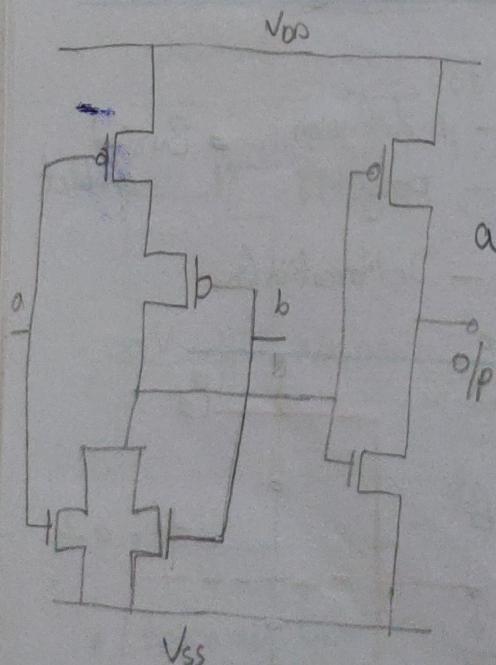


Stick Diagram:

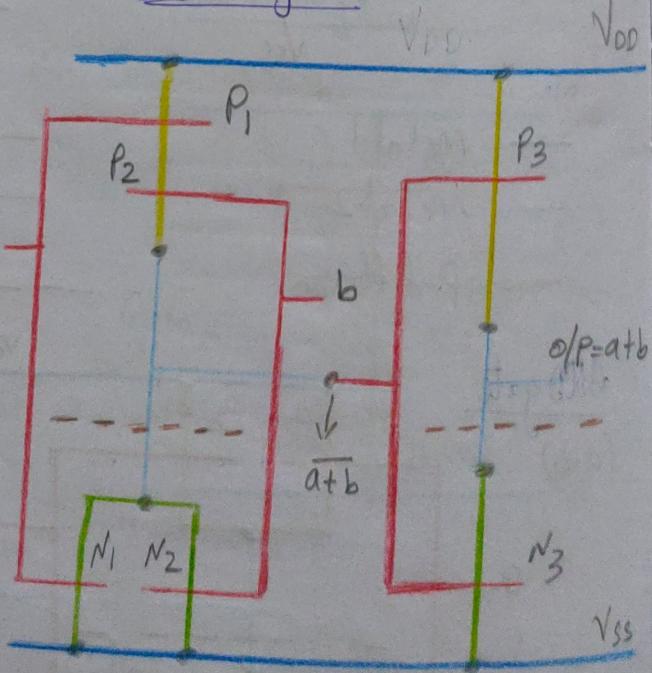


OR gate

Circuit diagram: $a+b$



Stick diagram:



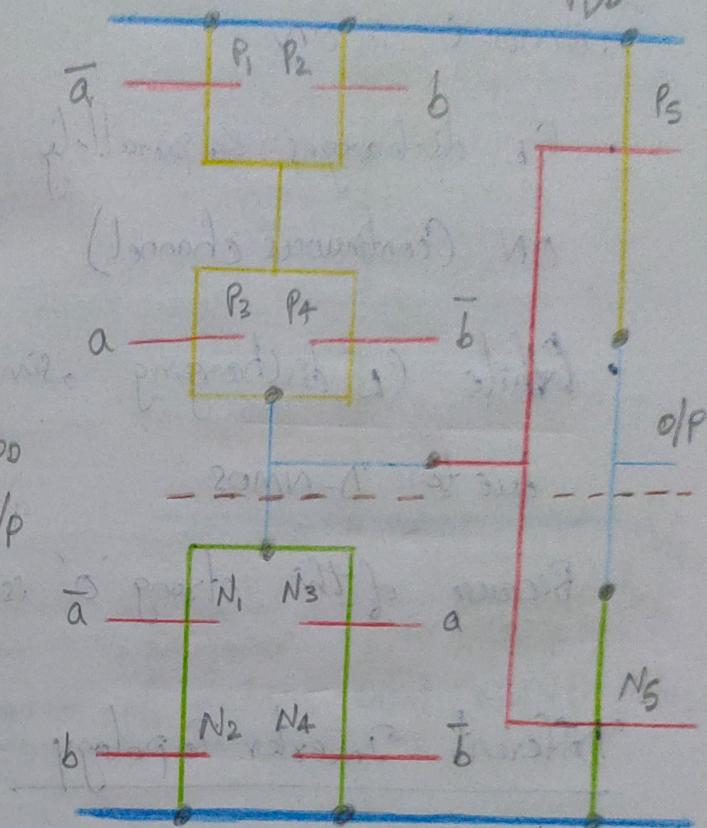
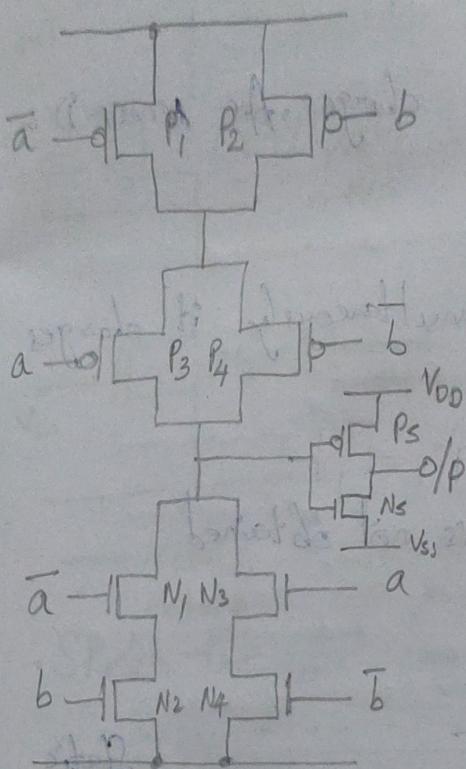
Metal-1
Metal-2
P-diffusion

n-diffusion
poly
De-Marcation line
Buried contact

Ex-OR gates: ($\bar{a}b + a\bar{b}$)

Circuit Diagram

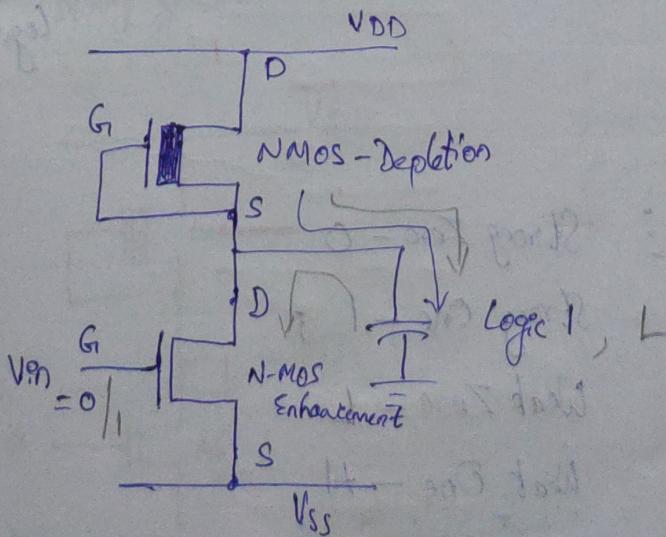
Stick Diagram:



Metal-1 (M1) — N-diffusion
 Metal-2 — Poly
 (Buried contact)
 P-diffusion — De-Marcation line

Buried contact

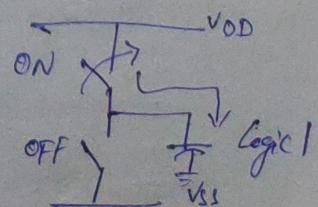
Depletion NMOS Inverter:



N-MOS - Enhanced	
Vin = 0	OFF
Vin = 1	ON

Case 1: Vin = 0

- NMOS-D is conduction
- NMOS-E is in OFF

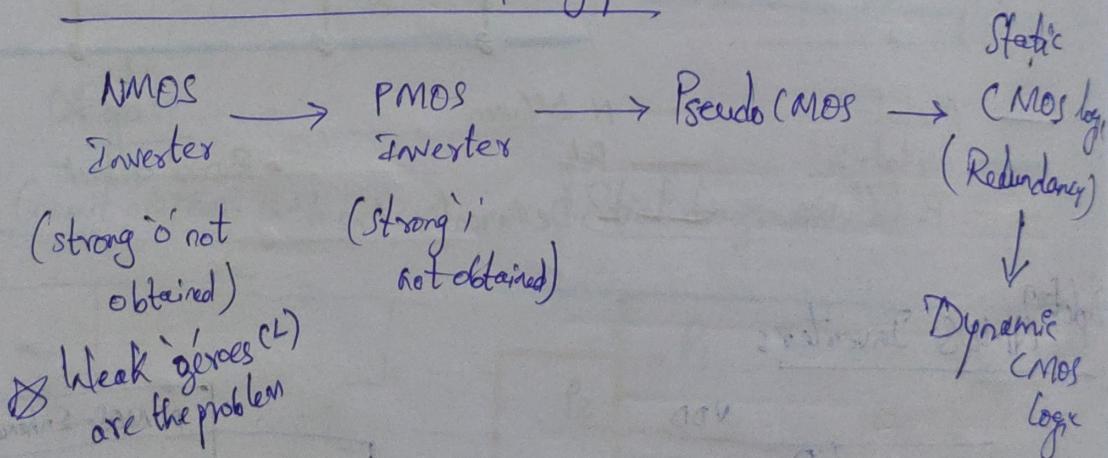


Weak zero is obtained

Case 2: $V_{in} = 1$

- NMOS-D in ON
- NMOS-E in ON
- C_L discharges & parallelly charges, ~~as NMOS~~,
ON (continuous channel)
- While C_L discharging, simultaneously it charges
due to D-NMOS
- Because of this strong '0' is not obtained

Different Inverter Topology



• Metal Stable states: Strong Zero - 0

Strong One - 1

Weak Zero - L

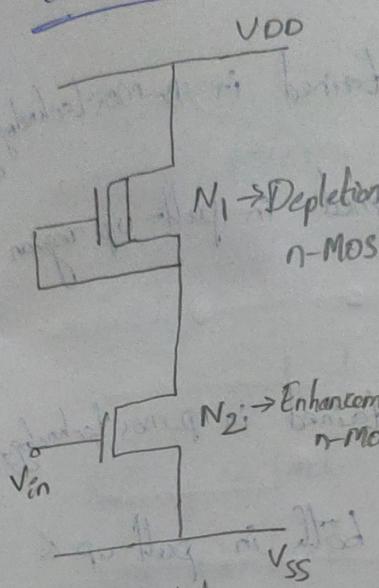
Weak One - H

Tri-State - Z

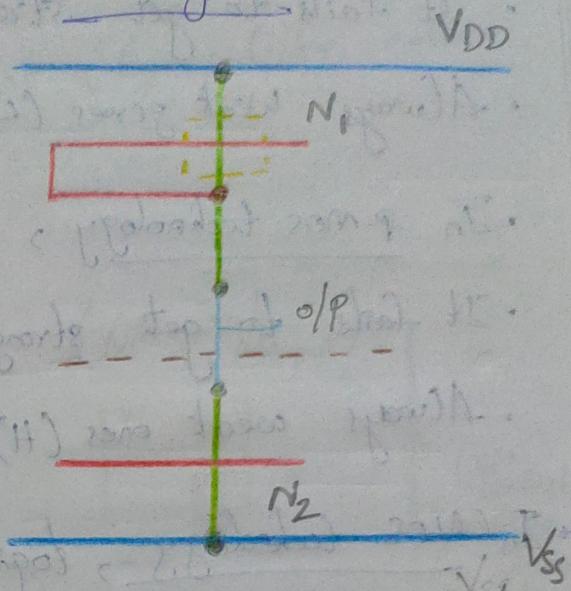
NMOS Inverter

07/03/2023

Circuit diagram:



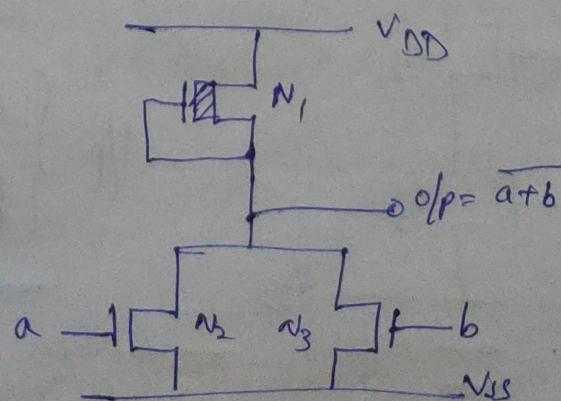
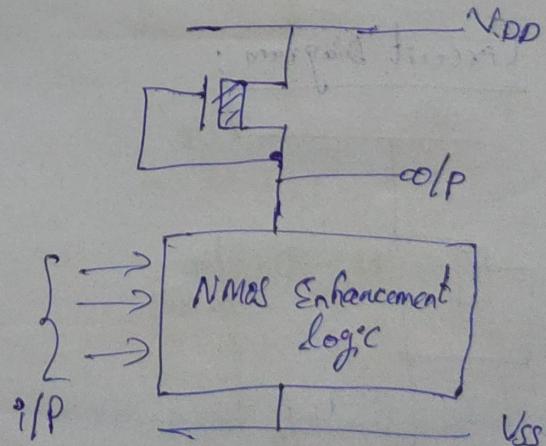
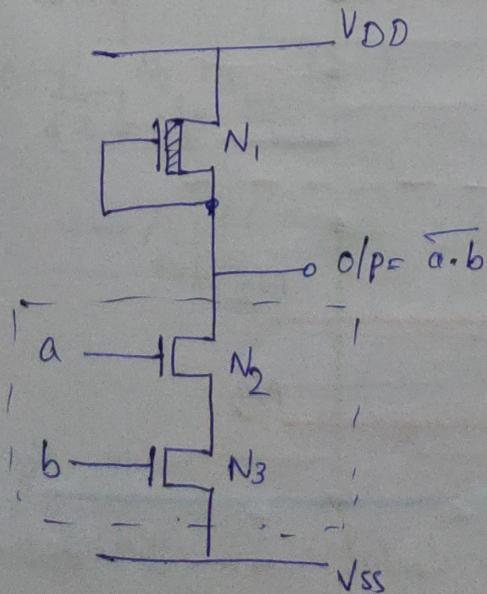
Stick Diagram



Sketch the stick diagram of n-MOS based NAND gate.

Circuit Diagram:

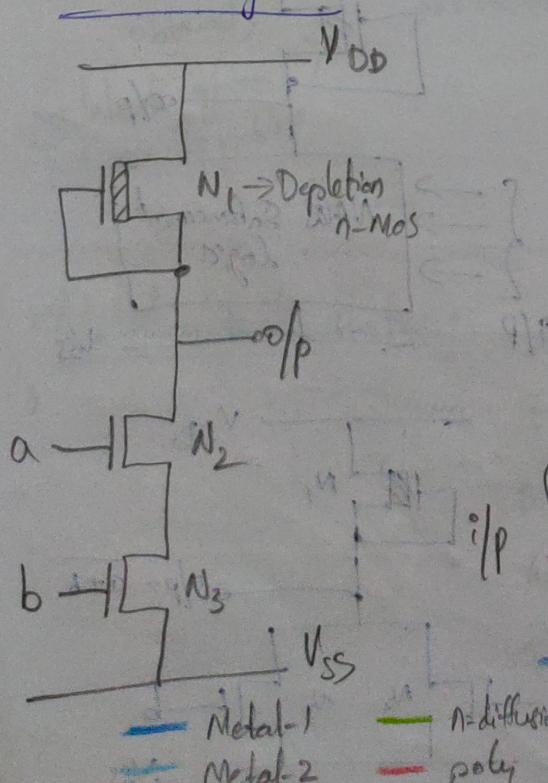
→ Apply the logic only in pull-down regions as it is the n-MOS technology
n-MOS technology fails to get strong zeroes.



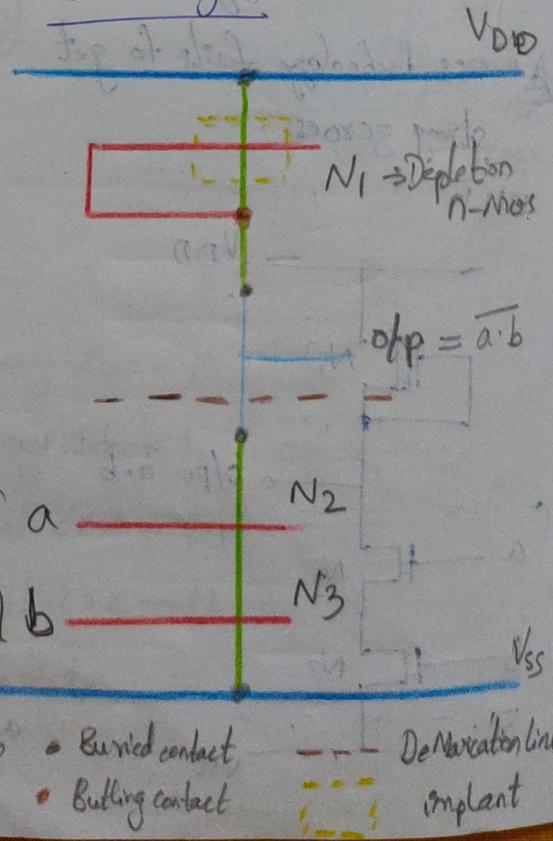
- In n-MOS technology, logic designed in pull-down region.
- It fails to get strong zeroes.
- Always weak zeroes (L) are obtained in n-MOS technology.
- In p-MOS technology, logic designed in pull-up region.
- It fails to get strong ones.
- Always weak ones (H) are obtained in p-MOS technology.
- In CMOS technology, logic applied both in pull-up & pull-down region and so logic is achieved.
- It fails in optimizing i.e. redundancy of logic, more no. of transistors are used.

NMOS to NAND gate

Circuit Diagram:



Stick Diagram:



• 7nm+ deep sub-micron technology

(Goal: Low power consumption, high power backup)

• Depending on technology, no. of layers differ, colour coding differs.

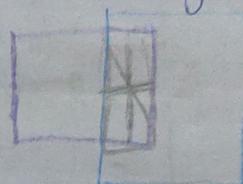
Contacts

• Buried contact

• Butting contact

• Via Contact

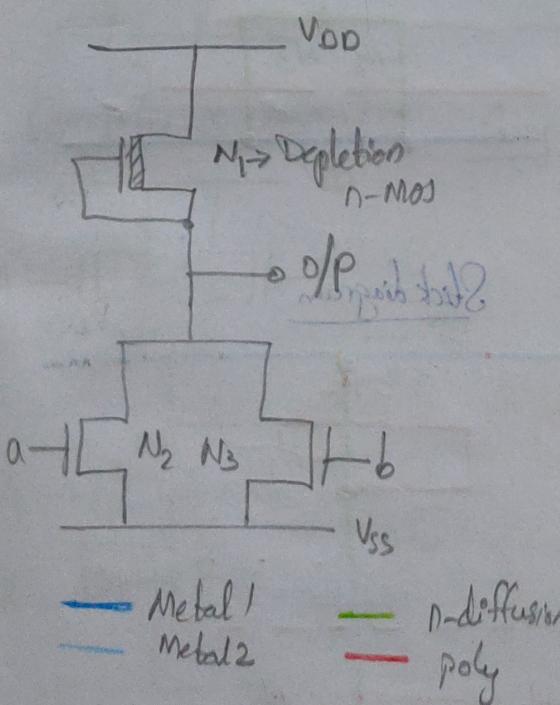
(Via contact layout)



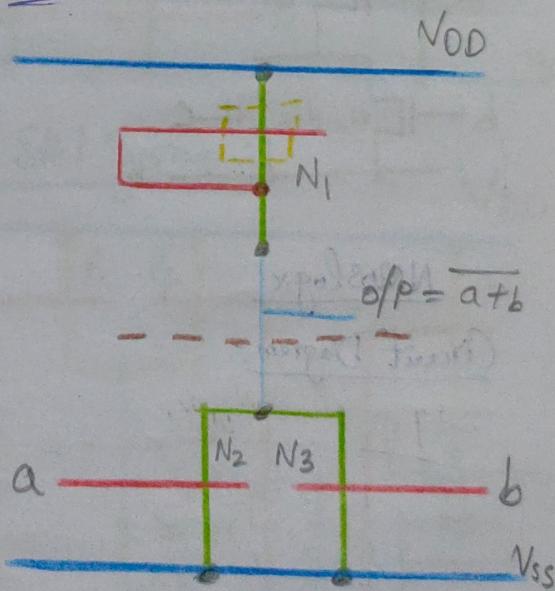
(via contact
on stack
Diagram)

NMOS NOR gate

Circuit Diagram:



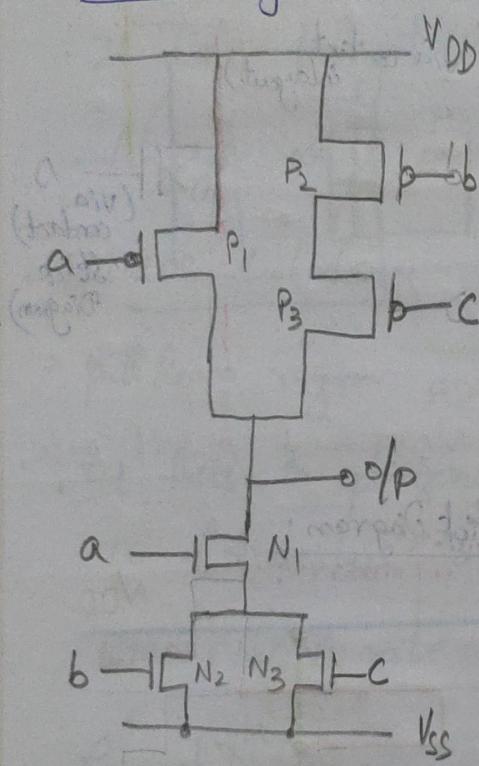
Stick Diagram:



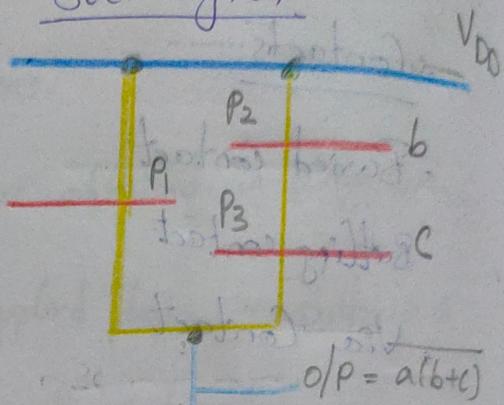
Implement the Boolean expression $f = \overline{a(b+c)}$ in CMOS and NMOS logic and sketch the stick diagrams.

Sol: (CMOS logic: $f = \overline{a(b+c)}$)

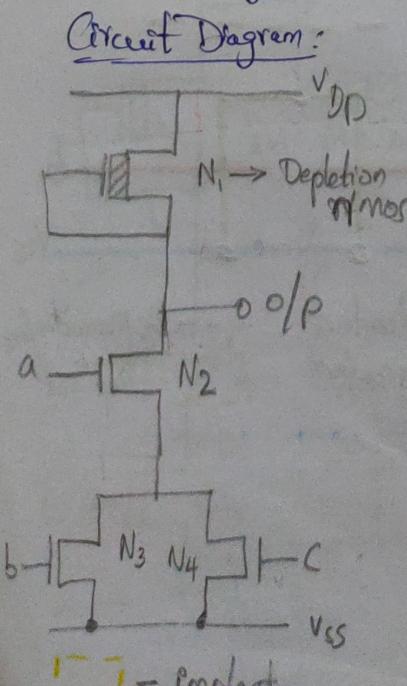
Circuit diagram



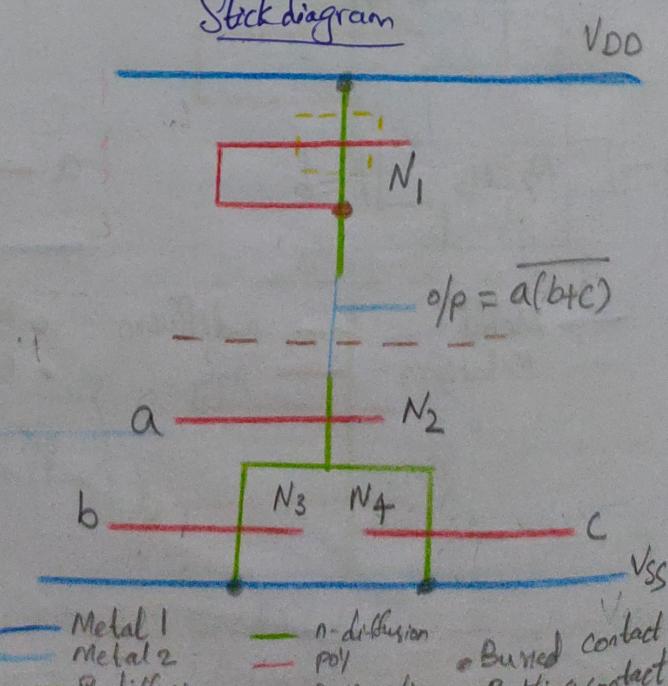
Stick Diagram:



NMOS logic



Stick diagram:



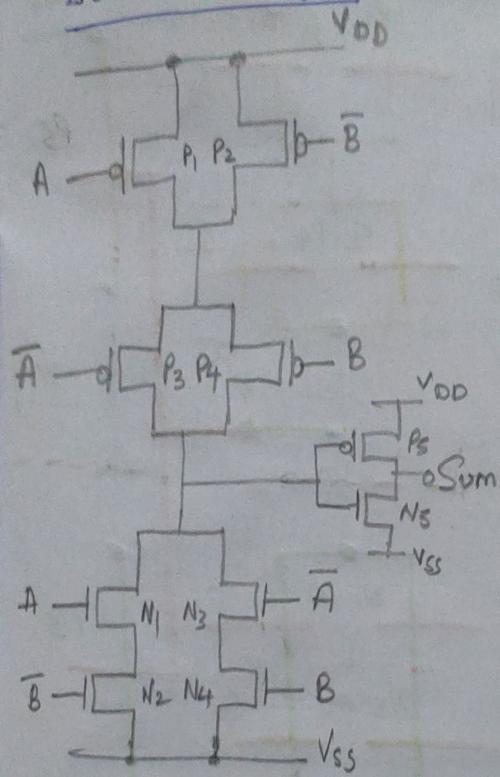
[] - Implant

Metal 1	n-diffusion	Burned contact
Metal 2	poly	Butting contact
P-diffusion	De-marcation	

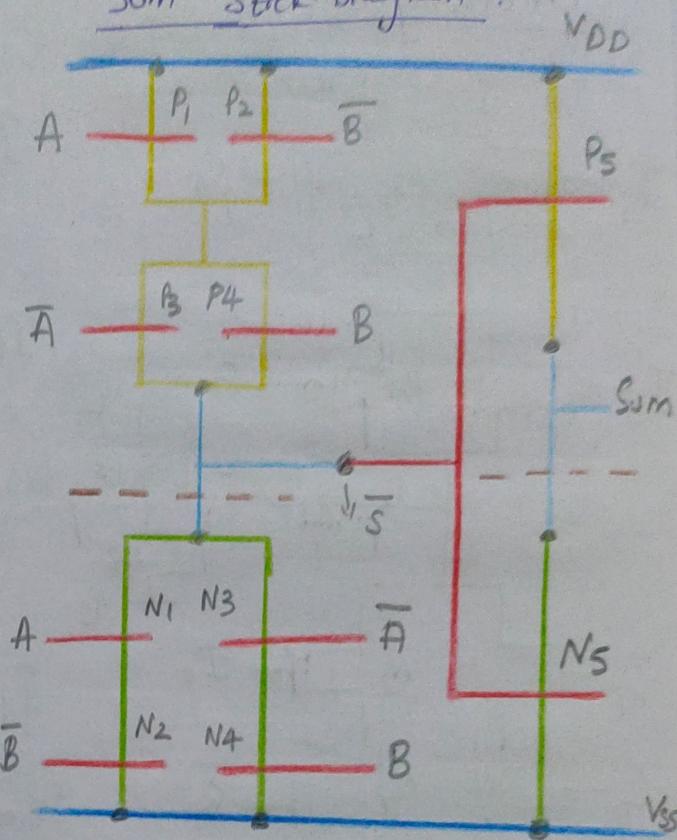
Sketch the stick diagram of half adder in CMOS logic.

Sol: Half adder : Sum : $S = A\bar{B} + \bar{A}B$ Carry : $C = A \cdot B$
 [CMOS logic]

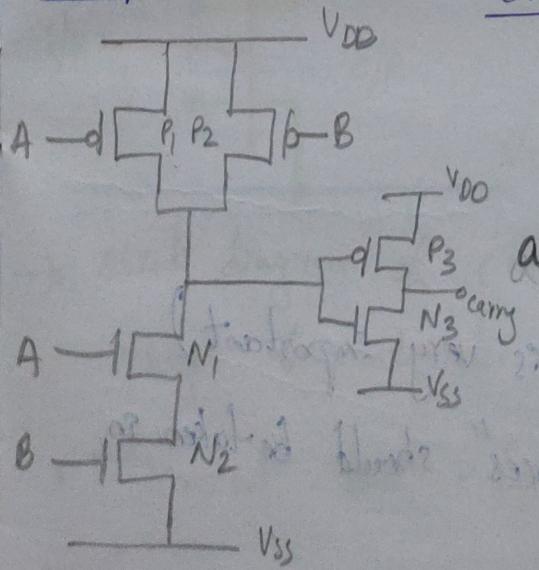
Sum-Circuit diagram:



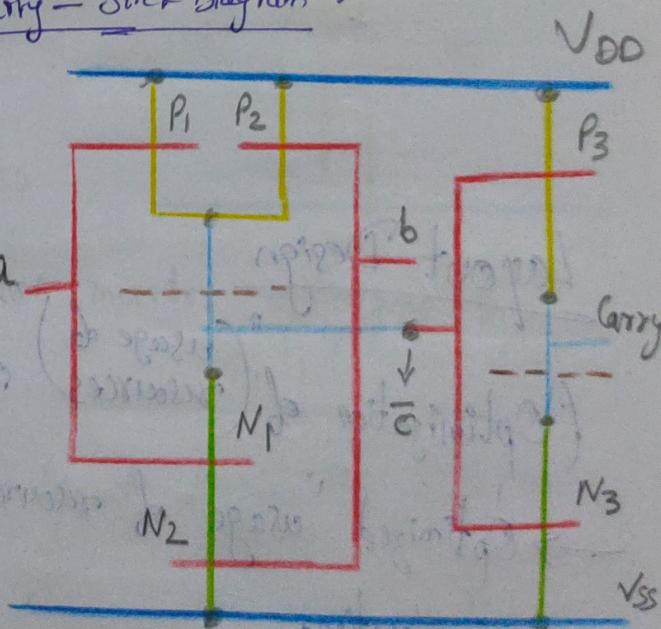
Sum - Stick Diagram :



Carry-Circuit Diagram:



Carry - Stick Diagram :



Metal-1
Metal-2

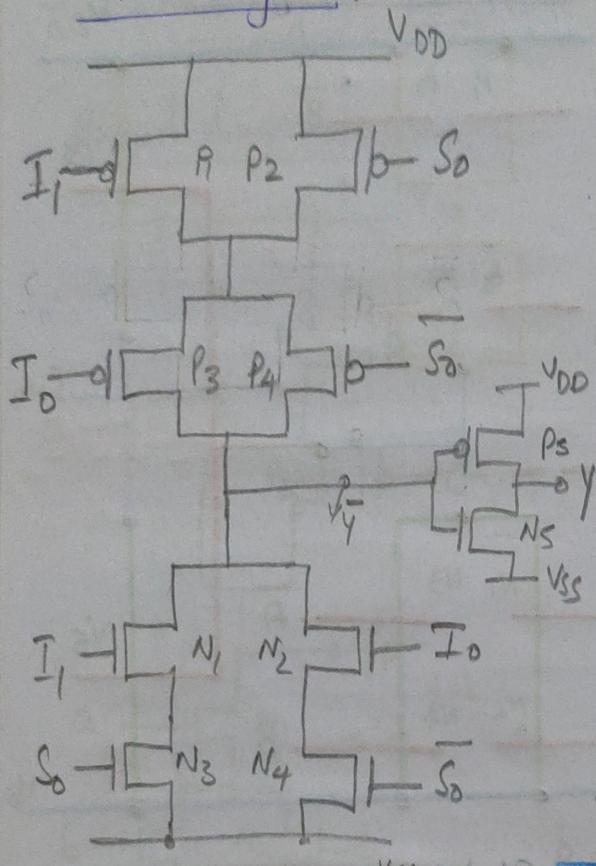
P-diffusion
n-diffusion

Poly
Buried Contact
De-Marcation line

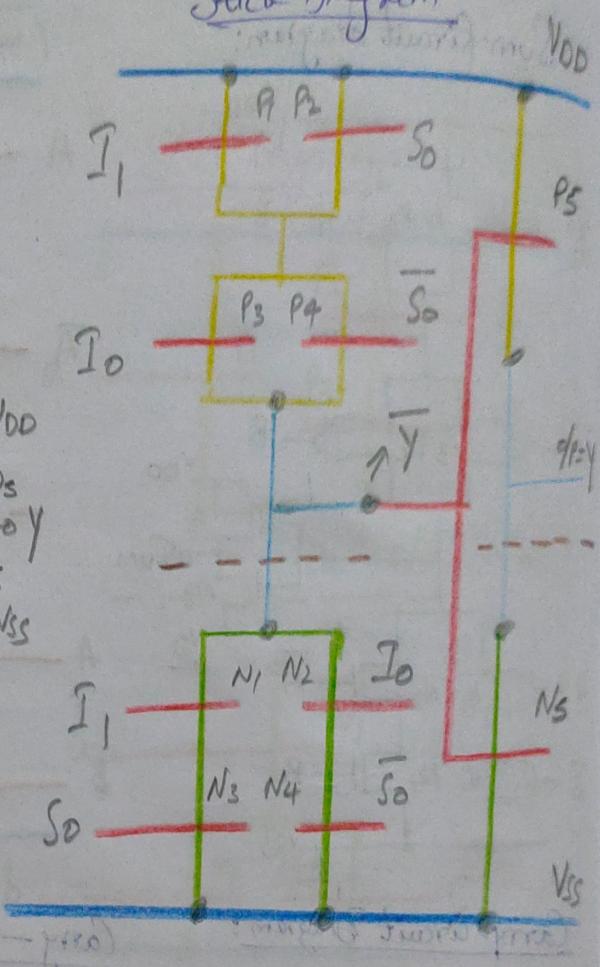
Sketch 2x1 MUX using CMOS logic 10/08/2023

Eq: $Y = I_1 S_0 + I_0 \bar{S}_0$

Circuit Diagram:



Sick Diagram



Layout Design

(Optimization of "usage of resources" is very important)

→ Optimized "usage of resources" should be taken in considerations

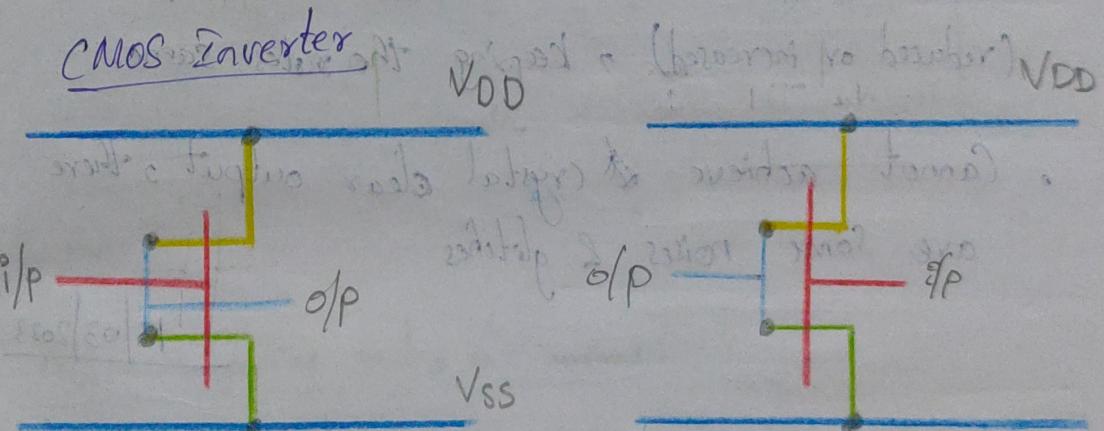
1. Usage of materials

2. Minimum spacing rules

Spacing rules: for b/w p & n-diffusions, the poly & metal, size of buried contacts, width of metal 1 in power rails

- If minimum spacing b/w pull-up & pull-down region given as $6t$ \Rightarrow we cannot choose $5t$ and also not even $7t$ as it may increase usage of resources.
- Also we cannot have butting contact of metal 1, metal 2, metal 3, metal 4 ~~and it increases the capacitance.~~

CMOS Inverter



→ Stick diagram of CMOS inverter optimizing the usage of materials.

- Microcad - tool - for layout designs

- Palette

- IBM based rules

Layout Design Rules

- 2 Types : (1) λ -based layout design rules
(lambda)
- (2) μ -based layout design rules
(micron)

Accurate & precise

λ -rules

- Scalable
- Feasible ~~rule~~ for the designer
- It is also called as Mead & Conway rules
- For each new process technology, λ is scaled (reduced or increased), keeping the scales same.
- Cannot achieve ~~a~~ crystal clear output, there are some noises & glitches

13/03/2023

- Scaling can be used in λ -rules, while in μ -rules the geometry is fixed.
- For any transistor (mos), the minimum size of transistor is 2λ .
- λ -rules does not give information about parasitics
- Parasitics - calculating resistance, capacitance of particular material

- Sheet resistance, doping - doping levels, capacitance, time constant
- L-rules does not specify about Parasitics.
- L-rules deals only with width (λ).
- Power Delay Product (PDP), Power consumption, noise

Minimum width rules for wires:

1. Min. width of n-diffusion : 2λ

2. Min. " " p-diffusion : 2λ

3. Min. " " polysilicon₍₁₎ : 2λ

4. Min. " " metal-1 : 3λ

5. Min. " " metal-2 : 4λ

Minimum Spacing rules for wires:

1. Min. spacing $\frac{1}{2}\lambda$ of n-diff to n-diff : 3λ

2. Min. " " p-diff to p-diff : 3λ

3. Min. " " n-diff to p-diff : 3λ

4. Min. " " diffusion to polysilicon : 1λ
(n or p)

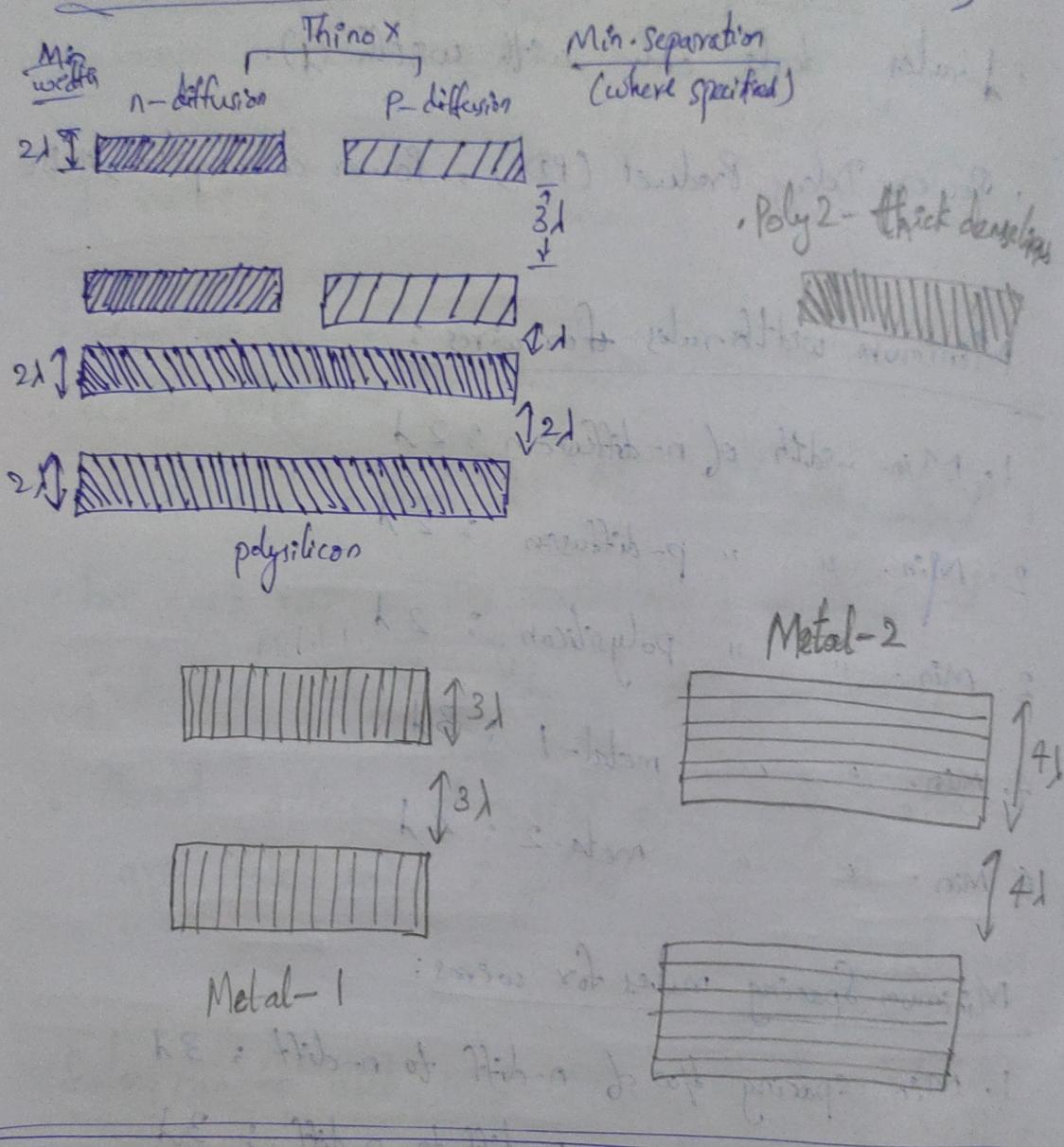
5. Min. " " metal-1 to metal-1 : 3λ

6. Min. " " poly to poly : 2λ

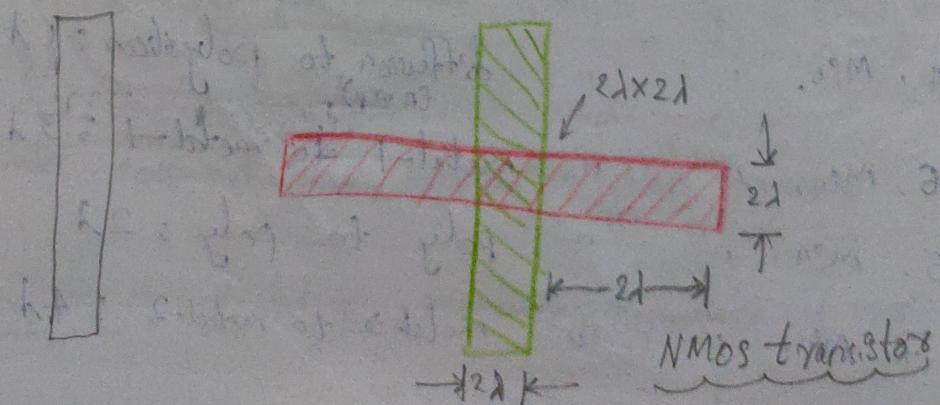
7. Min. " " metal-2 to metal-2 : 4λ

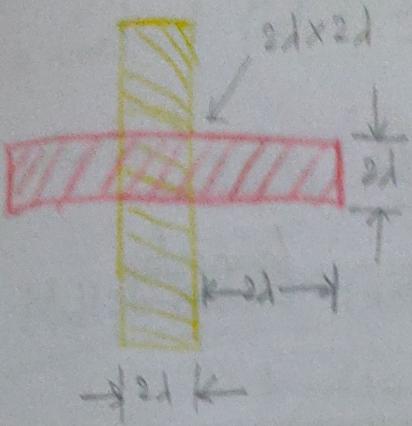
Width: $W \uparrow$

N based Design rules for wires (n-mos & pmos)



Design rules for transistors: Dimensions of the transistors





How much poly should cross the distance? $2d$

PMOS-transistor

Example 1:

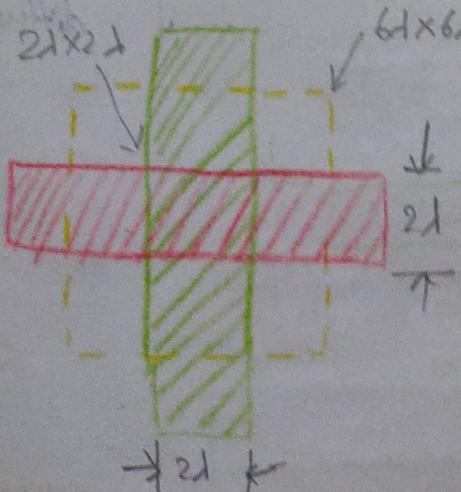
In VLSI, Designing :

- Speed of circuit - f' (frequency) \rightarrow considered for Digital/Mixed circuits
- Power consumption - P'
- Figure of merit - w' \rightarrow only for analog circuits

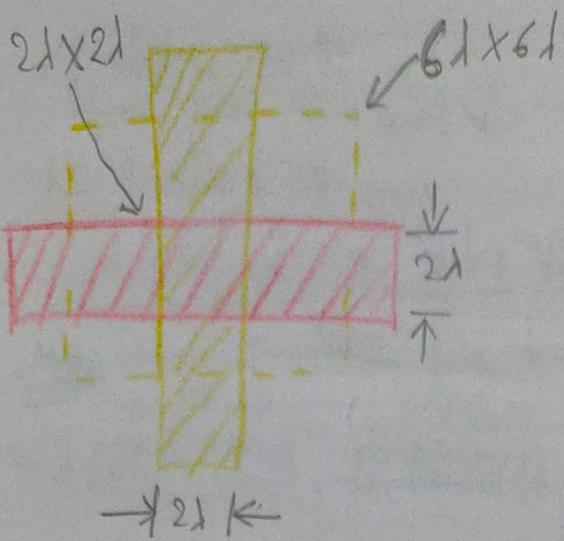
$$f = \frac{1}{T} = \frac{1}{R_s C} ; R_s - \text{sheet resistance} - \frac{\text{Width of wire}}{\text{length}}$$

Linear resistance comes into picture in Routing
 \hookrightarrow (length of wire)

Length of wire $\uparrow \rightarrow$ Propagation delay $\uparrow \rightarrow$ Power Consumption \uparrow



Depletion NMOS Transistor

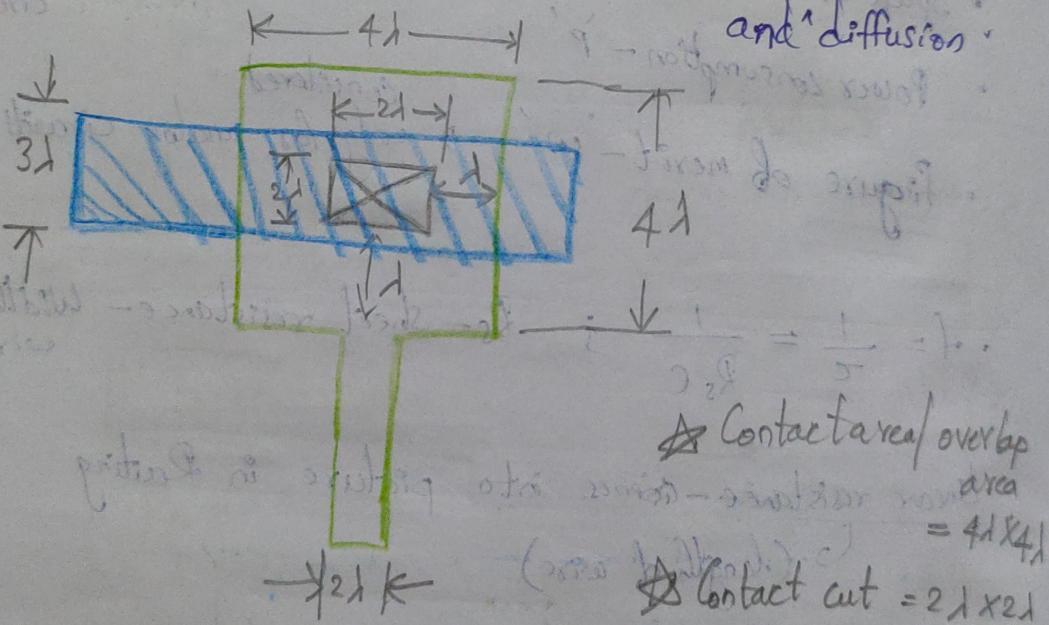


Depletion PMOS
transistor

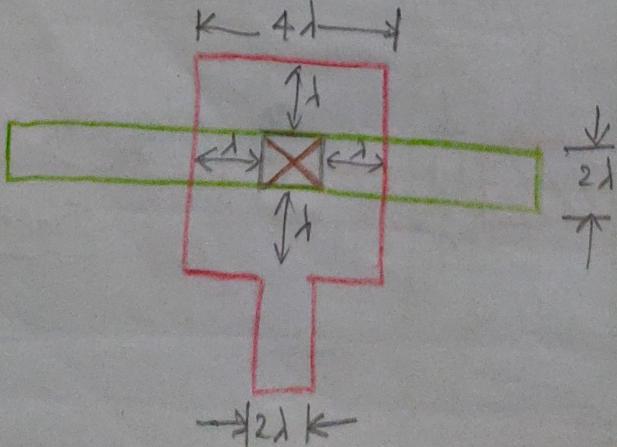
Design rules for contact cuts :

14/02/2023

- Buried contact: contact formed b/w a metal and diffusion.



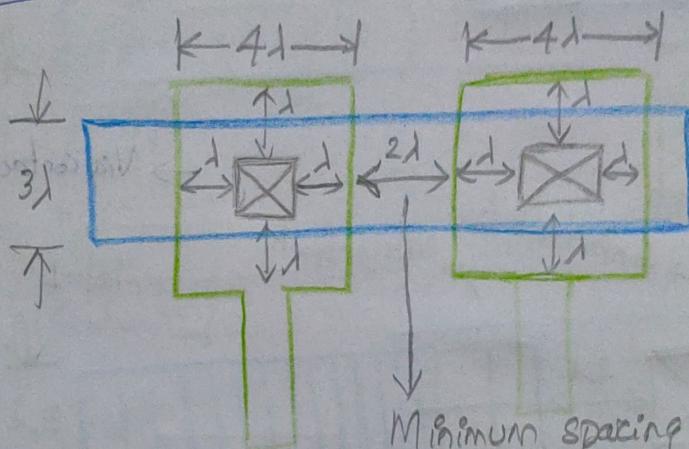
- Butting contact: contact formed b/w polysilicon and diffusion.



→ Contact Cut - $2\lambda \times 2\lambda$

→ Contact area / overlap area - $4\lambda \times 4\lambda$

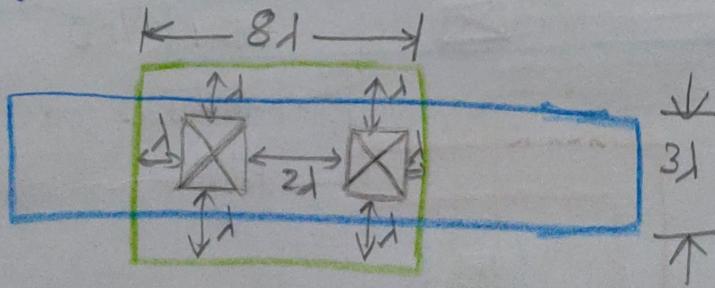
Multiple contacts: (without merging)



Minimum spacing b/w contact areas is 2λ

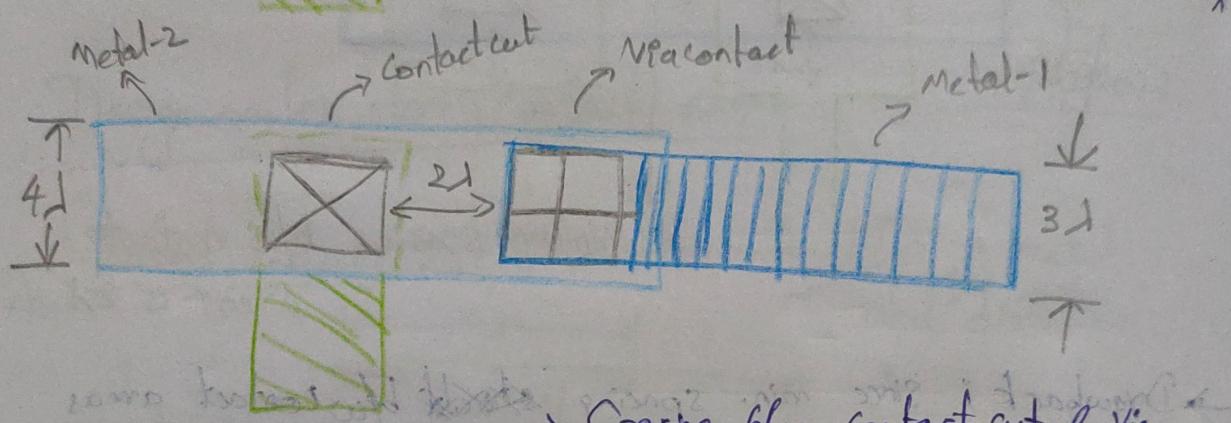
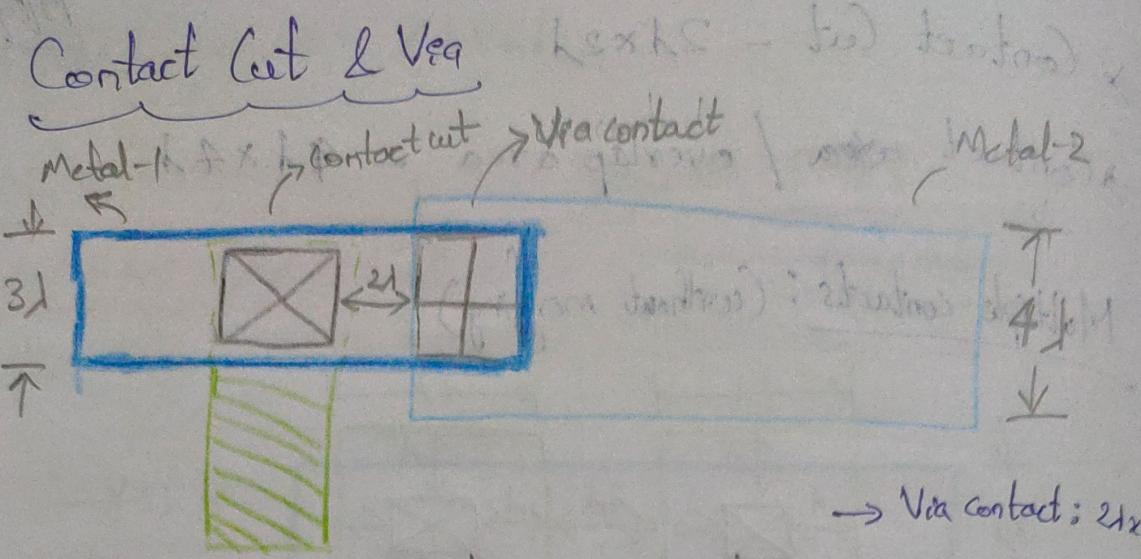
→ Drawback: since min. spacing b/w contact areas should be maintained, area increases in multiple contacts (without merging). → Min. spacing b/w contact areas is 2λ .

Merged contact area:



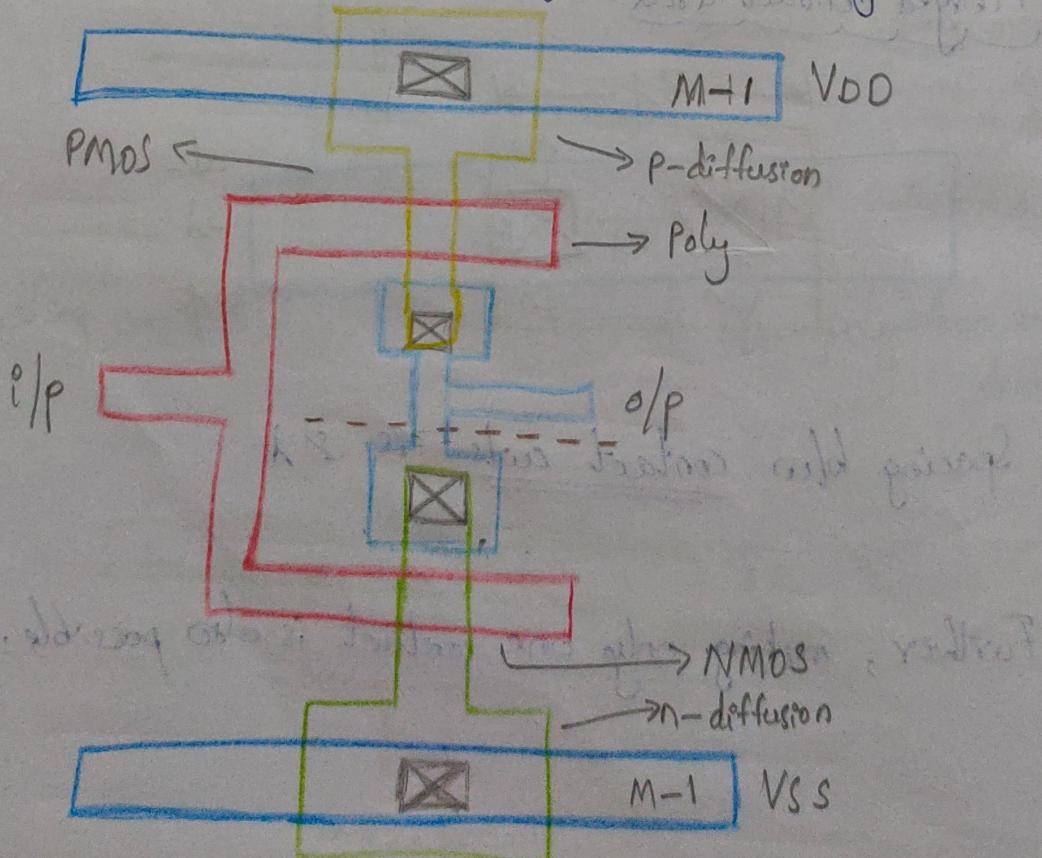
- Spacing b/w contact cuts is 2λ

- Further, making only one contact is also possible.

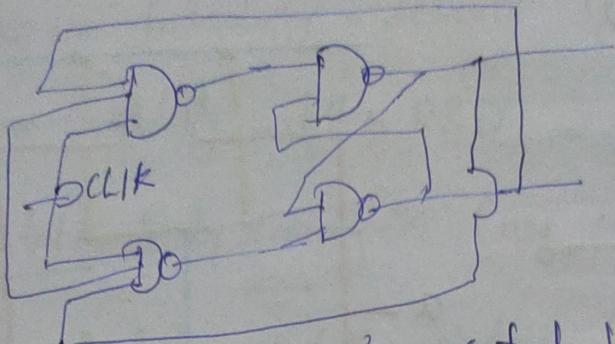


Layout Diagram of a CMOS NOT gate (Inverter):

1. Circuit Diagram 2. Stick Diagram 3. Layout



• D-flipflop \rightarrow Common collector (unity gain) 17/03/2023
(Digital) ~~analog~~ (Analog)



• Analog ~~analog~~
Designers

\curvearrowleft (Evaluation) \curvearrowright (Steering) control direction

17/03/2023

★ DRC Verification - Design Rule Checker

★ ERC Verification - Electrical Rule Checker

→ During layout designing, after each and every step -
DRC verification should be done. (spacing)

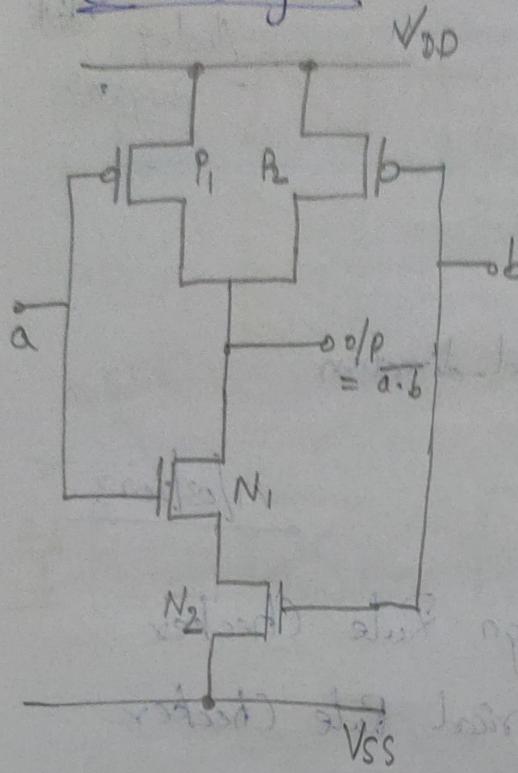
→ ERC verification: R_s , C , τ , f , L , Z , Power
(consumption)

(Inductor has behaviour of both resistor - resisting and
capacitor - storing)

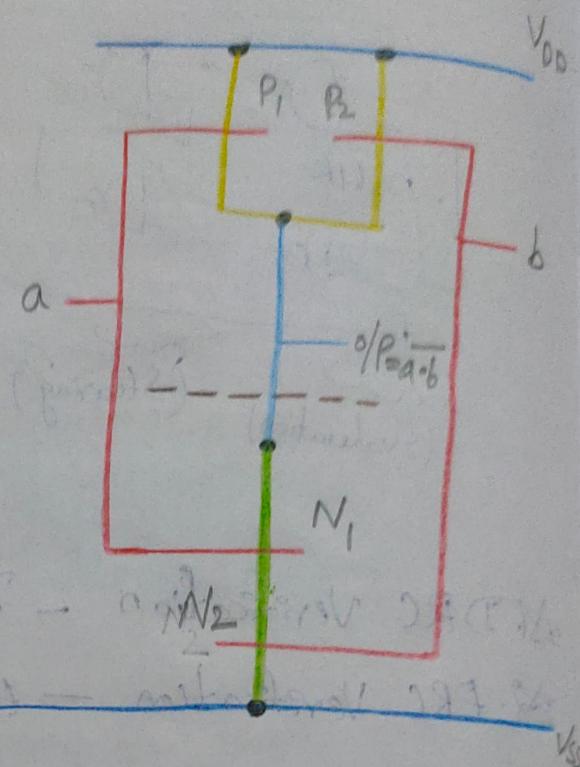
→ DRC is done parallelly along with layout designing.

NAND gate: $\bar{a} \cdot \bar{b}$

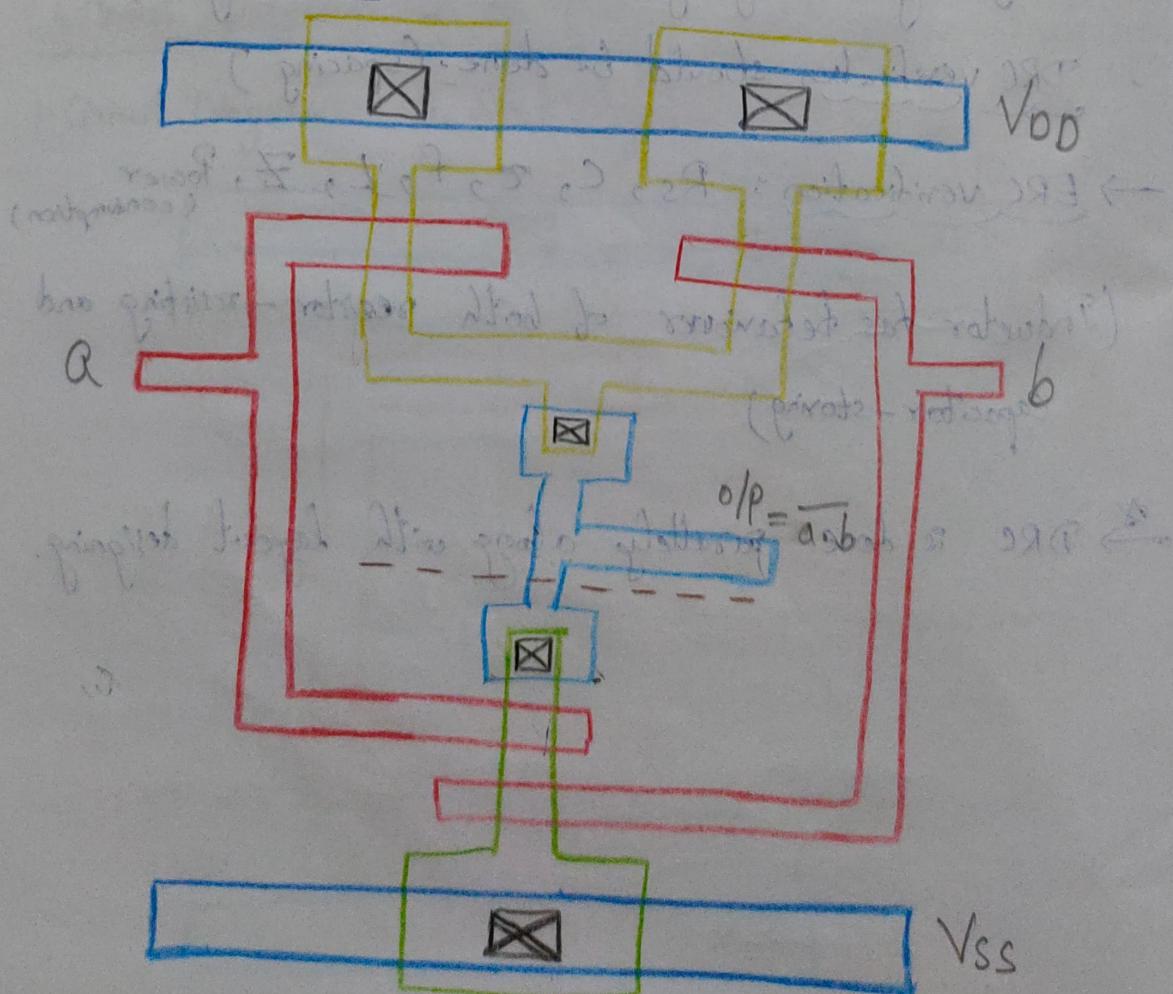
Circuit Diagram:



Stick diagram:



Layout Diagram



ANALOG VLSI

(VLSI design principle)

by Pucknell

28/03/2023

Relation between I_{ds} vs V_{ds} : (Mathematical modelling)

- I_{ds} , V_{ds} , V_{gs} , V_t
- For Integrated Concepts ($i(s)$) - I_{ds} , N_{ds}
- There won't be any drop
- Lagging - due to clock supply, or current drop (I_{ds} drop)
- Current has to be constant

I_{ds} vs V_{ds} Relation:

Quantitative Analysis - Mathematical Modeling

→ 3 points from MOSFET characteristics

→ Conditions for Cut-off, Linear region, Saturation region

$$\textcircled{1} \quad V_{gs} < V_t$$

→ No current flows, Cut-off region

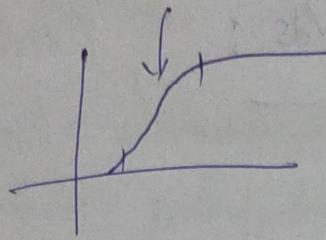
$$\textcircled{2} \quad (V_{gs} > V_t) \& (V_{ds} < V_{gs} - V_t)$$

→ MOSFET working/operating in the non-saturated region
(Linear region)

Current flowing in non-saturated region is $\propto V_{gs} \& V_{ds}$

→ amount of current is roughly proportional to V_{gs} & V_{ds}

→ Non-saturated region / linear region / Ohmic region



(as it obeys ohm's law)

④ ~~MOSFET behaves like a voltage controlled resistor.~~

⑤ $(V_{gs} > V_t) \& (V_{ds} \geq V_{gs} - V_t)$

→ MOSFET operating in saturation region. ($I_{ds\text{sat}}$)

→ Average input voltage = $V_{gs} - V_t$

→ The amount of I_{ds} is proportional to the square of V_{gs} and independent of V_{ds}

→ If V_{ds} is kept on increasing it leads to breakdown (breaking of covalent bonds)

→ MOSFET behaves as a voltage controlled current source

Mathematical Modeling of I_{ds} vs V_{ds} :

We know that, current is rate of flow of charge i.e.

$$I = \frac{Q}{t}$$

Therefore, drain current : $I_{ds} = \frac{\text{Charge induced in channel}}{\text{Electron transient time}}$

$$I_{ds} = \frac{Q_c}{\tau} \rightarrow ①$$

Electron transient time (τ):

$$\tau = \frac{\text{Length of channel (L)}}{\text{Electron velocity (v)}} = \frac{L}{v} \rightarrow ②$$

$$v = \mu E_{ds} \rightarrow ③ \quad (\text{From Hall effect})$$

μ -mobility of a charged particle

E_{ds} - applied electric field

$$E_{ds} = \frac{V_{ds}}{L} \rightarrow ④ \quad (\because E = \frac{V}{d})$$

Substitute ④ in ③:

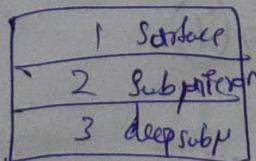
$$v = \mu \frac{V_{ds}}{L} \rightarrow ⑤$$

Substitute ⑤ in ②:

$$\tau = \frac{L}{\left(\frac{\mu V_{ds}}{L}\right)} = \frac{L^2}{\mu V_{ds}}$$

$\rightarrow ⑥$

MOSFET:



J_2 Bessel's function

μ -mobility changes from region to region

$$\therefore \tau = \frac{L^2}{\mu V_{DS}}$$

$\rightarrow ⑥$

$$\mu_n = 650 \text{ cm}^2 \text{V/sec}$$

(Surface region)

$$\mu_p = 250 \text{ cm}^2 \text{V/sec}$$

$$\mu_n = 1250 \text{ cm}^2 \text{V/sec}$$

$$\mu_p = 750 \text{ cm}^2 \text{V/sec}$$

(in
Substrate
region)

Charge induced in channel (Q_c):

(i) Q_c in non-saturation region (ii) Q_c in saturation region

CASE I: Q_c in non-saturation region

$$Q_c = E_g A \epsilon_{ins} \epsilon_0 \rightarrow ⑦$$

E_g - Electric field at gate
 A - Area of the gate terminal

ϵ_{ins} - Permittivity of insulating material b/w gate & channel

ϵ_0 - permittivity of free space]

where E_g - avg. electric field at the gate terminal

\rightarrow What is permittivity?

$\epsilon_{ins} \approx 4$ (for Silica)

$$\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$$

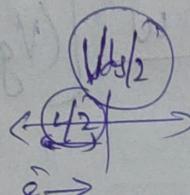
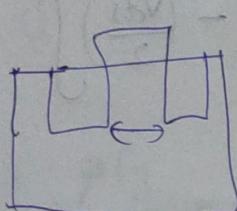
$$\rightarrow Q_c = E_g (WL) \epsilon_{in} \epsilon_0 \rightarrow ⑦$$

$$E_g = \frac{V}{D} \rightarrow \text{"thickness of an oxide layer"}$$

$$E_g = \frac{[(V_{gs} - V_t) - (\frac{V_{ds}}{2})]}{D} \quad (\because E = \frac{V}{d})$$

→ ⑧

$$\cdot E_g = \frac{|V_{in}| - |V_{out}|}{D} \rightarrow \text{average potential}$$



if e⁻ voltage < $V_{ds}/2$
 $\Rightarrow e^-$ travelled more than half of the channel.

$$\rightarrow 0 - \frac{V_{ds}}{2} \} \text{ non-saturation region}$$

e⁻ covered almost half of the channel

→ In saturation region, e⁻ voltage is $> \frac{V_{ds}}{2}$ & if travelled more than half of the channel.

Substitute ⑧ in ⑦ :

$$Q_c = \frac{[(V_{gs} - V_t) - \frac{V_{ds}}{2}](WL)}{D} \epsilon_{in} \epsilon_0$$

$$\therefore Q_c = \frac{\epsilon_{in} \epsilon_0}{D} WL \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \rightarrow ⑨$$

Substitute ⑥ & ⑨ in ①

$$I_{ds} = \frac{\epsilon_0 \epsilon_r}{D} W L \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right] \quad \text{for this expression book}$$

$\left(\frac{L^2}{\mu V_{ds}} \right)$

$$I_{ds} = \frac{\epsilon_0 \epsilon_r \mu V_{ds} W}{D L} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]$$

$$= \frac{\mu \epsilon_0 \epsilon_r}{D} \cdot \frac{W}{L} \cdot V_{ds} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]$$

$$I_{ds} = \frac{\mu \epsilon_0 \epsilon_r}{D} \cdot \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$\therefore I_{ds} = \frac{\mu \epsilon_0 \epsilon_r}{D} \cdot \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad \rightarrow 10$$

→ The above expression is simplified as

$$I_{ds} = K \cdot \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]; \quad k = \frac{\mu \epsilon_0 \epsilon_r}{D}$$

→ K is called technology dependent parameter
(acts as amplification factor)

$$I_{ds} = \beta \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]; \quad \beta = \frac{k_w}{L}$$

→ (12)

I_{ds} vs V_{ds} relation in terms of gate capacitance (C_g):

$$C_g = \frac{\epsilon_{ins} \epsilon_0 (WL)}{D} \quad (\because C = \frac{\epsilon A}{d})$$

$$\Rightarrow \frac{\mu C_g}{WL} = \left(\frac{\mu \epsilon_{ins} \epsilon_0}{D} \right) = k \quad \Rightarrow \quad k = \frac{\mu C_g}{WL}$$

Substitute this 'K' value in (12)

$$\therefore I_{ds} = \frac{\mu C_g}{WL} \cdot \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$I_{ds} = \frac{\mu C_g}{L^2} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \rightarrow (13)$$

I_{ds} in terms of C_g per unit area :

$$C_0 = \frac{C_g}{A} = \frac{C_g}{WL} \quad \Rightarrow \quad C_g = C_0 WL \quad \text{substitute this} \\ \rightarrow (14) \quad (14) \text{ in } (13)$$

$$I_{ds} = \frac{\mu C_0 (WL)}{L^2} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$\therefore I_{ds} = \frac{\mu C_0 W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right] \rightarrow (15)$$

• Figure of merit (FOM): how much frequency, switching speed / is detected
circuit speed

: It helps in determining PDP (Power Delay Product)
(Robust nature)

- VLSI design challenges

(ii) For saturation condition: Substitute $V_{ds} = V_{gs} - V_F$
(Saturation expression)

(Case 2)

Saturation Region: $V_{ds} \geq V_{gs} - V_t$

31/08/2023

$$I_{ds} = k \cdot \frac{W}{L} \cdot \frac{(V_{gs} - V_t)^2}{2}$$

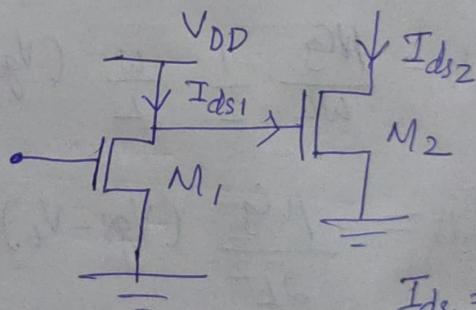
$$I_{ds} = \beta \frac{(V_{gs} - V_t)^2}{2}; \beta = \frac{kW}{L}$$

$$I_{ds} = \frac{C \mu}{L^2} \frac{(V_{gs} - V_t)^2}{2}$$

$$I_{ds} = \frac{C \mu W}{L} \frac{(V_{gs} - V_t)^2}{2}$$

→ μ depends on temperature

Current Mirrors



$$I_{ds1} = I_{ds2} \text{ (ideal)}$$

$$I_{ds} = \frac{\mu \epsilon_{ins} C_0}{D} \times \frac{W}{L} \times \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

- In ideal case, $I_{ds1} = I_{ds2}$ but practically they won't be equal because? even by small changes in I_{ds} parameters, I_{ds} will change
- We need to make I_{ds} constant

Calculation of Transconductance (g_m) for a
Mos transistor:

$$\text{g}_m = \frac{\delta I_{ds}}{\delta V_{gs}} \quad \left| \text{const} = V_{ds} \right. \rightarrow ①$$

$$W.k.T, \delta I_{ds} = \frac{\delta Q_c}{\tau} \rightarrow ② \quad (Q = I\tau)$$

$$W.k.T, \tau = \frac{L^2}{\mu V_{ds}} \rightarrow ③ \quad [\text{from previous derivation}]$$

③ in ②

$$\boxed{\delta I_{ds} = \frac{\delta Q_c \times \mu V_{ds}}{L^2}} \rightarrow ④$$

• But, change in charge, $\delta Q_c = C_g \delta V_{gs} \rightarrow ⑤ \quad (Q = CV)$

⑤ in ④

$$\delta I_{ds} = \frac{C_g \times \delta V_{gs} \times \mu \times V_{ds}}{L^2}$$

$$\Rightarrow \frac{\delta I_{ds}}{\delta V_{gs}} = \frac{C_g \mu V_{ds}}{L^2}$$

$$\boxed{\text{g}_m = \frac{\mu C_g V_{ds}}{L^2}} \rightarrow ⑥$$

Figure of merit: Frequency (ω) = $\frac{\text{g}_m}{C_g} = \frac{\mu V_{ds}}{L^2}$

• Switching speed \rightarrow W_0 (figure of merit)

"In Saturation": $[V_{ds} = V_{gs} - V_t]$

$$\text{Frequency} = \frac{g_m}{C_g} = \frac{\mu (V_{gs} - V_t)}{L^2}$$

WKT, from the previous derivation

$$g_m = \frac{\epsilon_{ins} \epsilon_0 W L}{D} \rightarrow ⑧$$

⑧ in ⑥

$$g_m = \frac{\mu \epsilon_{ins} \epsilon_0 W L V_{ds}}{D L^2} = k \times \frac{W}{L} \times V_{ds}$$

(in Saturation) $g_m = \frac{\mu \epsilon_{in} \epsilon_0 W L (V_{gs} - V_t)}{D L^2}$

$$g_m = k \times \frac{W}{L} (V_{gs} - V_t); k = \frac{\mu \epsilon_{in} \epsilon_0}{D}$$

~~SWITCHING~~

$$g_m = \beta (V_{gs} - V_t)$$

$$g_m = \beta (V_{gs} - V_t)$$

Figure of merit :- (MOSFET) (ω_0)

$$\omega_0 = \frac{g_m}{C_g} = \frac{1}{\tau} = \frac{\mu V_{ds}}{L^2}$$

, where ' ω ' represents the switching speed of a MOSFET, for a fast device , the g_m should be as high as possible and C_g should be as low as possible.

$\downarrow C_g$ is difficult , because $\downarrow C_g = \frac{\epsilon_0 \epsilon_{air} A}{D}$

$D \uparrow$ should high , Mosfet size $\uparrow \rightarrow$ not desirable
(VLSI rule violation)

03/04/2023

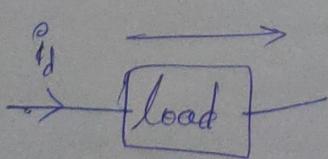
Current Mirrors :

* Analog IC design - by Behzad Razavi

* Microelectronics - by Zetra & Smith

→ Don't consider channel length modulation in current mirrors

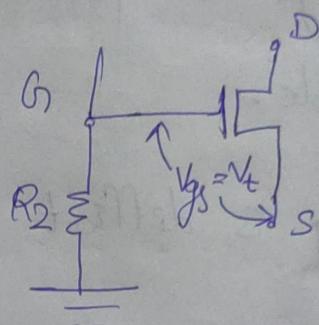
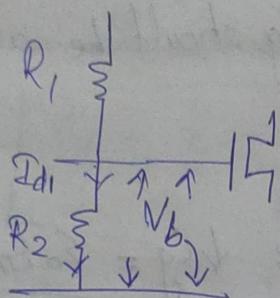
Analysis : ① without channel length modulation
② with channel length modulation



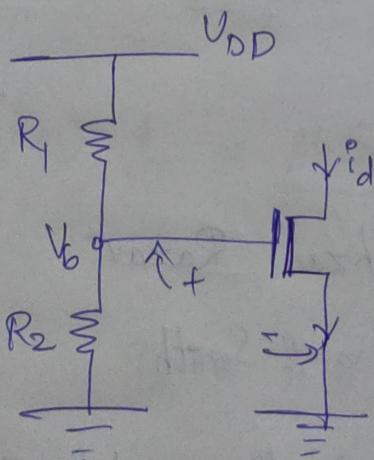
If I_D maintained constant, then voltage is also maintained constant

03/04/2022

- Current only handles the load.
- Current is the deciding factor to drive the load.
- When there is a drop around active element like transistor, biasing is created



• V_b - biasing voltage



• i_d varies if R_2 is changed

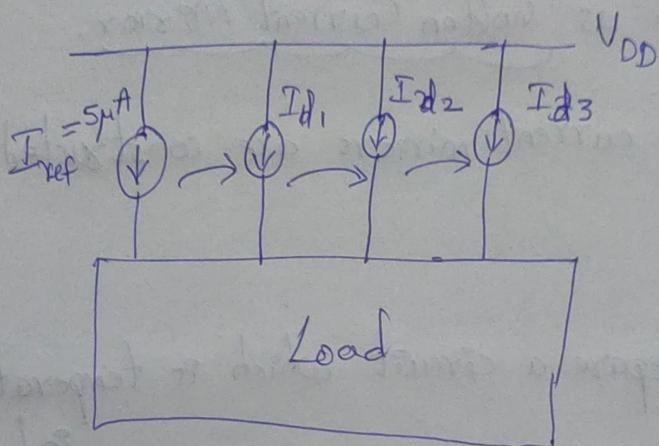
(?) What is current mirroring

(?) Purpose of current mirroring

(?) Types of current mirroring

$$\#1 :- I_{ds} = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

- Copying the current I_{ds} in the cascading circuit.
- Aim / Motto: maintaining constant I_{ds}



- w.r.t Temperature - μ, V_t
 ↓ mobility changes $T \uparrow \Rightarrow \mu \uparrow \Rightarrow I_{ds} \text{ changes}$
- μ depends on applied Electric field & Temperature
- V_t - Threshold voltage - depends on temperature
 $T \uparrow \Rightarrow e^- \text{ get excited} \Rightarrow \mu \uparrow \Rightarrow V_t \downarrow$
 → The minimum sufficient voltage at which MOSFET is in ON state.

Golden Current Mirror:

- Main motto of current mirroring is to create a constant current (rigid / robust circuit - which is having a constant current mirroring phenomenon), this is called as Golden Current Mirror.
- But Golden current mirrors are constructed using bandgaps
- Need to prepare a circuit which is temperature independent.

#2 Basic concept of Current Mirror

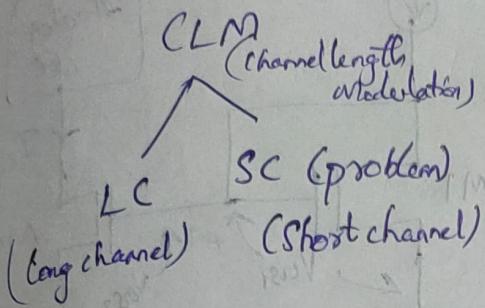
10/04/2023

Need of current mirrors :

- Current Mirrors are ^{very} important to distribute the current all over the circuit.
- In IC, cascading of circuits is very important.
- O/P of circuit is given as I/p to the next circuit
- Because of ^{the} process variation / validation, you will not be able to accurately replicate the current to different location.
- MOSFET operated in saturation region.
$$I_{D(\text{sat})} = \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^2$$

Current Mirror

(challenging parameter)



Temperature

Solution

Stabilize process

$$\mu \propto (V_{GS} - V_0)^2$$

temp.
dependent

BJT - has fast switching speeds (ECL)

- has high impact due to noise

MOSFET - high input impedance (at gate terminal)

Biasing - giving applying external voltage i.e. giving some push to the circuit.

- maintaining proper resistance

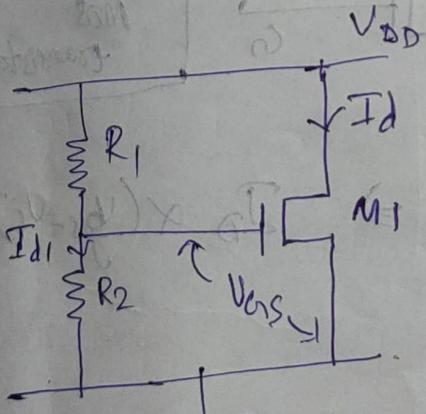


Fig. 1

(fixed biasing)

(Voltage divider)

Resistor
based
Voltage
Divider

$$\frac{R_2}{R_1 + R_2} V_{DD}$$

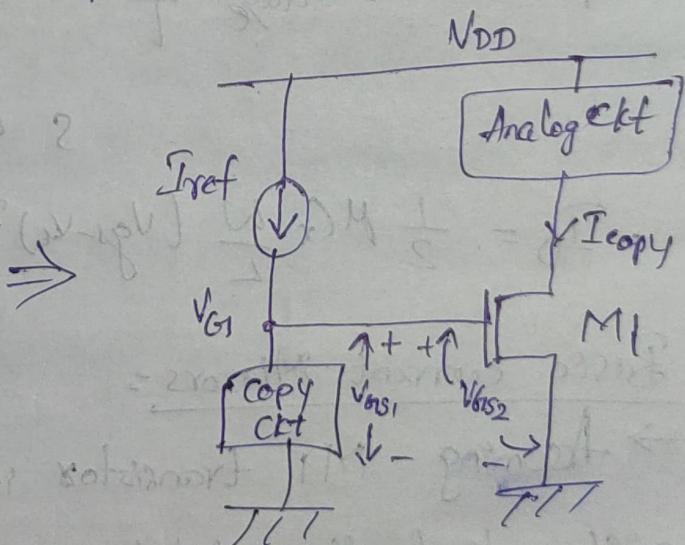
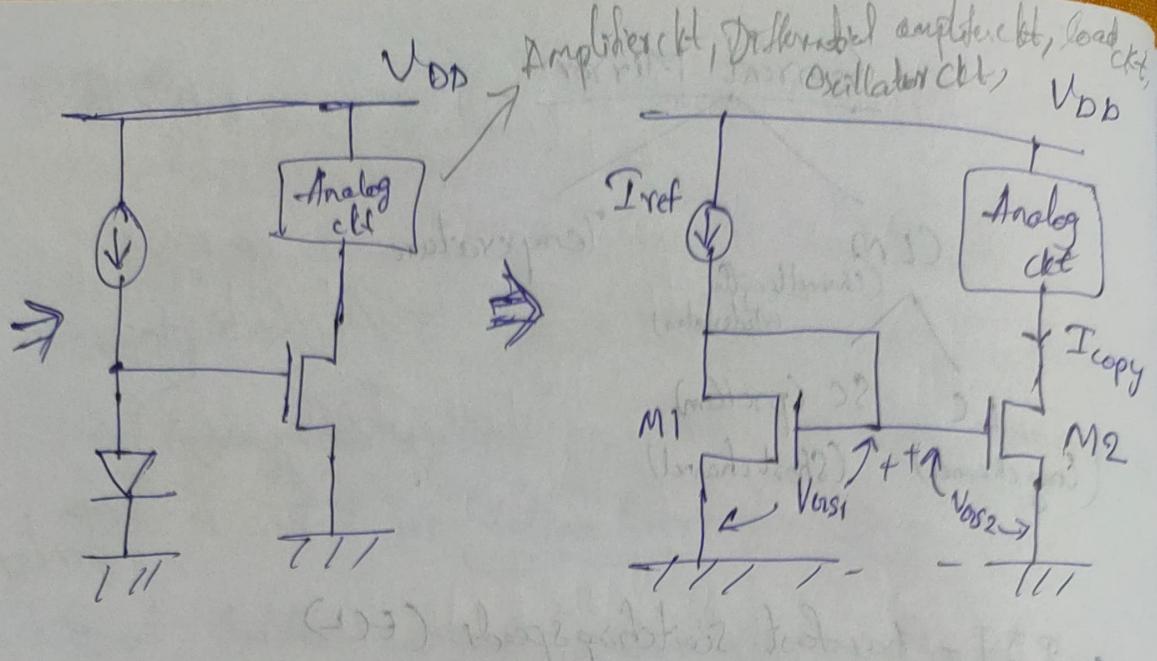


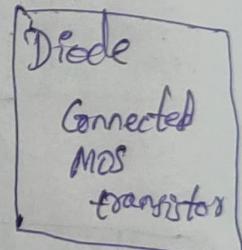
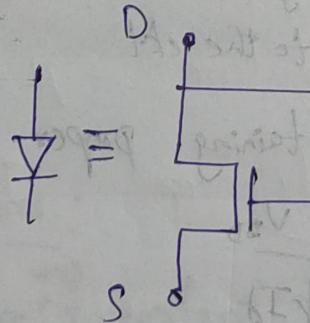
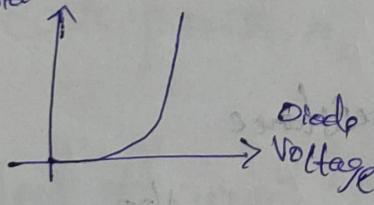
Fig. 2

Basic Block diagram
of GM



- Problem arises, when of sub T_{on} . Also, fabrication is difficult temperature & voltage parameter which involves diode & changes leading to changes in diode characteristics.

Diode current

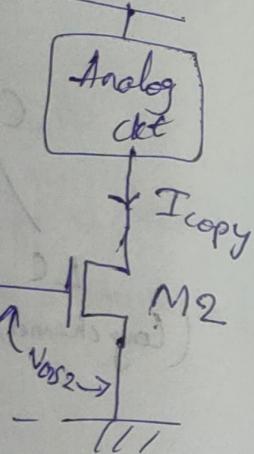


$$I_D = \frac{1}{2} \mu C_x \frac{W}{L} (V_{GS} - V_t)^2 \Rightarrow I_D \propto (V_{GS} - V_t)^2$$

Basic current Mirrors:

- Assuming M1 transistor in saturation (Fig.1)
- Channel length modulation is not considered.
- $\lambda=0 \Rightarrow$ Channel length modulation is constant.
- Always in the CM, all the (MOS transistors) should be operated in saturation region only.

analog, load
or Ckt, V_{DD}



tion is difficult
uses diode &
FET
t's.

Diode
Connected
MOS
transistor

$$\propto (V_{GS} - V_t)^2$$

(Fig.1)
ed.
stant-
los
asitors) should
T.

→ Basic CM circuits, all the MOS transistors
considered as Long Channel devices.

→ In the Fig. 1, drop across R₂ is equal to
 $\left(\frac{R_2}{R_1+R_2} \cdot V_{DD} \right)$.

→ Therefore, the current I_D which is flowing in
circuit i.e. Fig. 1 is equal to $\frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_t]^2$

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L} [V_{GS} - V_t]^2$$

$$= \frac{1}{2} \mu C_{ox} \frac{W}{L} \left[\frac{R_2}{R_1+R_2} V_{DD} - V_t \right]^2$$

→ In the Fig. 1, fixed biasing method is incorporated
through resistive elements (passive elements) which
is not suggestible in IC's.

• As temp. changes, it will effect the IC.

→ Therefore, I_D depends on process parameters like
 μ , V_{GS}, V_t, R₂, R₁, etc., which vary with
process and temperature.

→ Therefore, we design a current source in analog
circuits based on "Mirroring phenomenon", from

a precisely defined Reference Current Mirror

Source¹, i.e reference current; $I_{ref} = I_{copy}$

11/04/2023

→ In the Fig.2, $V_{GSI_1} = V_{GSI_2}$

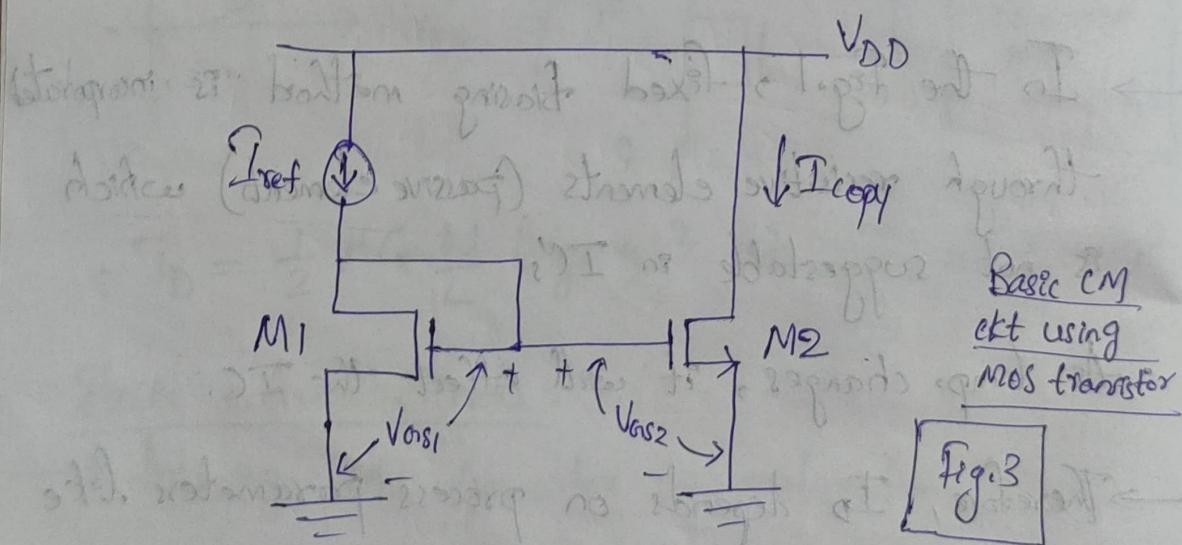
→ Let us consider, $I_{ref} = f(V_{GSI_1}) \rightarrow ①$

→ $I_{copy} = f(V_{GSI_2}) \rightarrow ②$

⇒ $I_{copy} = f(f^{-1}I_{ref})$ [∴ $V_{GSI_1} = V_{GSI_2}$]

⇒ $I_{copy} = f(f^{-1}I_{ref})$ [∴ from eq ①: $V_{GSI_1} = f^{-1}I_{ref}$]

$$\Rightarrow I_{copy} = I_{ref}$$



① In Fig.3, consider M1 & M2 are identical MOS transistors.

→ Identical means same V_{GSI} , V_t , v_{ds} , doping concentration and same mobility(μ). (99% is achieved) → process validation parameters.

Memory

I_{copy}

04/2023

(eta)^{ij}, b_{fe}/ β making temperature independent.

② M₁ & M₂ should be operated in Saturation region.

③ M₁ & M₂ should be of Long Channel (LC) devices.

$$I_{ref(sat)} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_1 (V_{gs1} - V_{t1})^2 \rightarrow ①$$

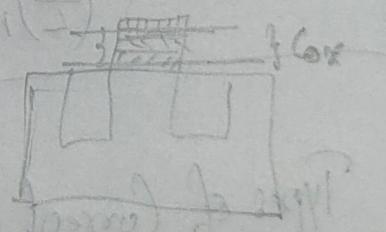
$$I_{copy(sat)} = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_2 (V_{gs2} - V_{t2})^2 \rightarrow ②$$

$$\frac{I_{copy}}{I_{ref}} = \frac{\frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_2 (V_{gs2} - V_{t2})^2}{\frac{1}{2} \mu C_{ox} \left(\frac{W}{L}\right)_1 (V_{gs1} - V_{t1})^2}$$

$$\Rightarrow \frac{I_{copy}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \quad [\because M_1 \& M_2 \text{ are identical}]$$

$$\therefore I_{copy} = \frac{(W/L)_2}{(W/L)_1} * I_{ref}$$

$\frac{W_2}{W_1}$ - aspect ratio



→ Challenges: ① Fabrication of identical MOS transistors is very difficult. → In CM design

② Maintaining temperature independent circuit is difficult.

③ Making/Maintaining μ , C_{ox} same is difficult

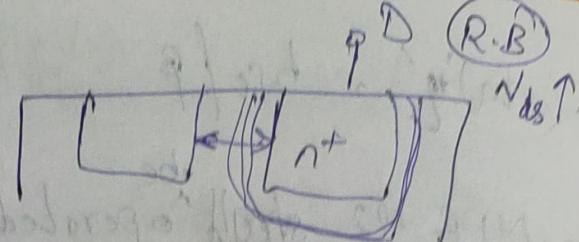
Basic CM
circuit using
MOS transistor

g.3

MOS transistors

concentration
process validation
parameters.

Short channel devices:



- At saturation region, I_{DS} is independent of V_{DS} & only dependent on V_{GS} .
- $R.B \uparrow \Rightarrow$ Depletion region $\uparrow \Rightarrow$ channel narrows down ($V_{DS} \uparrow$)
- VI characteristics ^{solar study, no more} valid here (CLM)
- Channel Length Modulation: Scaling the length of channel in MOS transistors, by increasing or decreasing V_{DS} , V_{GS}

$$I_{\text{copy}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \times \frac{(1 + \alpha V_{DS2})}{(1 + \alpha V_{DS1})} \times I_{\text{ref}}$$

- Valid when
CLM
is considered

Types of Current Mirrors: Design-based
Application based

- (1) Wilson Current Mirror
- (2) Cascaded CM
- (3) Giddens CM - compound SC are used - expensive fabrication

Designed based (Ms)

Application-based types of CM:

(1) Passive CMs

(2) Active CMs

— by means of current replication.

Dual gates \rightarrow Floating gates
used for memory devices

