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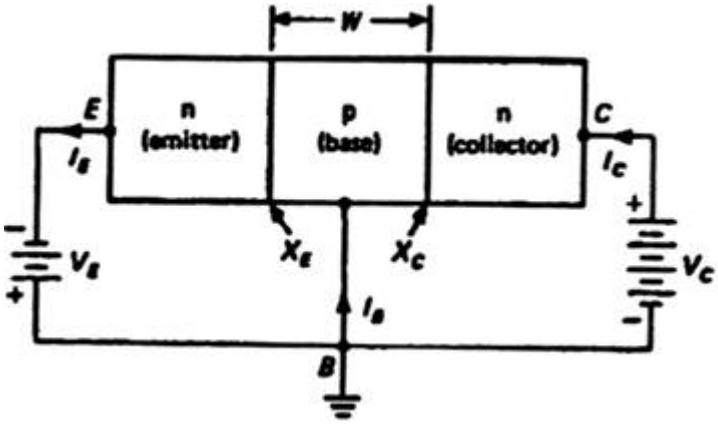
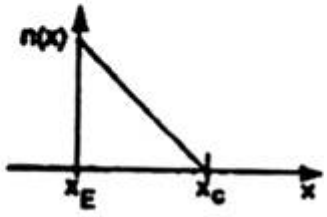
PROBLEM 01 – 0032: The p−type base region of an n−p−n bipolar silicon transistor of the type shown below has a width of 2.0×10^{-6}m and is doped with 1.0×10^{21} acceptors/m^3. Electrons are injected into this region from the emitter at x_E, producing a uniform gradient of electrons there. The electron concentration drops to zero at the collector at x_c. If 2.0×10^{20} electrons/m^3 are present at the emitter edge of the base region (x_E), calculate the diffusion current density of electrons through this base region under steady−state conditions. What electric field must be present in this base region to yield an electron drift current density just equal to the diffusion current density just calculated? Determine the voltage drop across the base width corresponding to this field.





Solution: From Einstein relation for electrons,

$$D_n = (kT / q)\,\mu_n$$
$$= 0.026\ V^{-1}\ (0.14\ m^2 / V\text{−sec})$$
$$= 0.0036\ m^2 / sec,$$

Here k is the gas constant, q the electronic charge, and T the absolute temperature. μ_n is the electron mobility and $\mu_n = 0.14\ m^2$ / V−sec for the element silicon.

$$(J_n)_{diffusion} = qD_n\,(dn / dx)$$
$$= 1.6 \times 10^{-19} C(0.0036\ m^2/sec)[\{2.0 \times 10^{20}\} / \{2.0 \times 10^{-6}\}]m^{-4}$$
$$= 5.8 \times 10^4\ A/m^2.$$
$$(J_n)_{drift} = qn\mu_n\varepsilon = (J_n)_{diffusion}$$

Hence,

$$\varepsilon = [\{(J_n)_{diffusion}\} / \{qn\mu_n\}]$$
$$5.8 \times 10^4\ A/m^2 = 1.6 \times 10^{-19}\ C(1.0 \times 10^{21}\ m^{-3})\ (0.14 m^2 / V\text{−sec})(\varepsilon)V/m$$
$$\varepsilon = 2.6 \times 10^3 V/m.$$

The voltage drop is $V = \varepsilon W = 2.6 \times 10^3\ (2.0 \times 10^{-6})$

$$= 5.2 \times 10^{-3}\ V.$$

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PROBLEM 01 – 0033: A silicon p^+–n–p transistor has a base width of 2.0×10^{-6} m and base resistivity of 0.0010 Ω–m. The hole lifetime in the base region is 0.10 μsec. The emitter region has thickness 1.0×10^{-6} m and resistivity 0.000010 Ω–m. The emitter and collector areas are both 2.5×10^{-9} m^2.
a) Show that the component of the base current necessary for supplying electrons for recombining holes in the base region is small compared to the collector current.
b) Calculate the injection efficiency of holes for the emitter of this transistor.

Solution: a) It seems reasonable to assume that if small base current is needed for recombining holes in the base, then the diffusion length L_p ought to be much larger than the base width. It can be shown that if the electron current for recombining holes is negligible, it is necessary that $(W^2 / 2L_p^2) << 1$, where $L_p^2 = D_p\tau_p$. Now

$$(W^2 / 2L_p^2) = [\{(2.0 \times 10^{-6})^2 m^2\} / \{2(1.25 \times 10^{-3}\ m^2/sec)(1.0 \times 10^{-7}\ sec)\}]$$
$$= 1.6 \times 10^{-2} << 1.$$

b) The injection efficiency is given by

$$\gamma = [1 / \{1 + \sigma_n W / \sigma_p W_E\}]$$
$$= [1 / \{1 + [1 / (0.0010)](\Omega\text{–m})^{-1} (2.0 \times 10^{-6}\ m) / [1 / (0.000010)](\Omega\text{–m})^{-1}(1.0 \times 10^{-6}\ m)\}]$$
$$= [1 / \{1 + 2.0 \times 10^{-2}\}] = 0.98 \quad \text{or} \quad 98 \text{ percent.}$$

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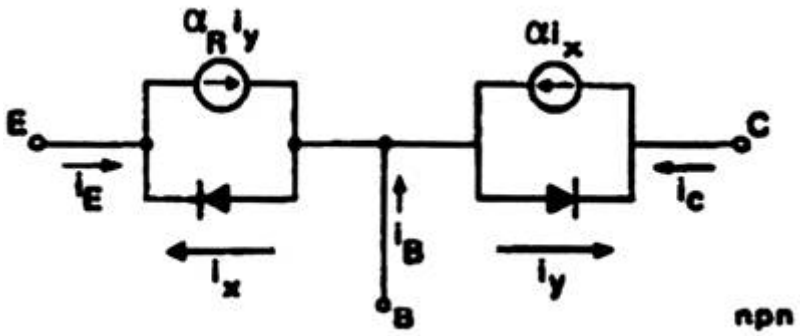
PROBLEM 01 – 0034: For an npn transistor, find i_B in terms of v_{BC} and i_C using the Ebers−Moll model.



Solution: The Ebers−Moll model is shown. The currents through the diodes are given conventionally by

$$i_x = I_{ES}[\exp\{(qv_{BE}) / (kT)\} - 1] \quad (1)$$

$$i_y = I_{CS}[\exp\{(qv_{BC}) / (kT)\} - 1] \quad (2)$$

and the other currents are

$$i_E = \alpha_R i_y - i_x \quad (3)$$

$$i_C = \alpha i_x - i_y \quad (4)$$

$$i_B = -i_E - i_C \quad (5)$$

It is desired to find an expression for i_B that contains only v_{BC} and i_C as terminal variables. From Eq. (4),

$$i_x = [\{i_C + i_y\} / \{\alpha\}] \quad (6)$$

and substitution in Eq. (3) gives

$$i_E = \alpha_R i_y - [\{i_C + i_y\} / \{\alpha\}] \quad (7)$$

or

$$i_E = \alpha_R I_{CS}[\exp(qv_{BC} / kT) - 1] - [\{i_C + I_{CS}[\exp(qv_{BC} / kT) - 1]\} / \alpha] \quad (8)$$

We substitute this value for i_E into Eq. (5) and gather terms to obtain

$$i_B = -i_E - i_C$$

$$= [(1 - \alpha) / \alpha]\, i_C + [\{1 - \alpha\alpha_R\} / \alpha]\, I_{CS}\, [\exp(qv_{BC} / kT) - 1] \quad (9)$$

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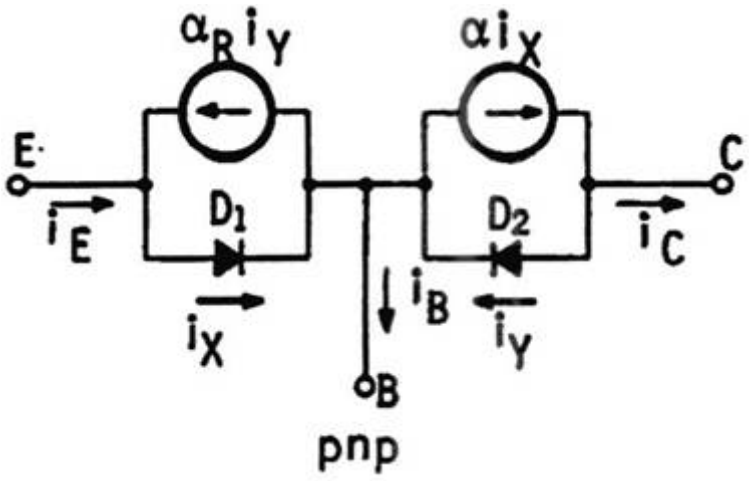
PROBLEM 01 – 0035: A pnp transistor has $\alpha = \alpha_R = 0.9$ and $I_{CO} = I_{EO} = 10\ \mu A$ at room temperature.
a) Find the collector current when the transistor is off. Assume that for an off transistor, v_{EB} and v_{CB} are large and negative with respect to kT/q. (At T = 25°C, kT/q ≈ 0.025 V.)
b) Find the collector current when the transistor is on. Assume that for an on transistor $v_{EB} = 0.25$ V and v_{CB} is large and negative.



Solution: The Ebers−Moll model for a pnp transistor is shown. When C is open and EB is reverse-biased, the currents are defined as $i_E = I_{EO}$ and $i_x = I_{ES}$. When E is open and CB is reverse-biased, the currents are $i_C = I_{CO}$ and $i_y = I_{CS}$. When C is open, we have the equations

$$i_y = \alpha i_x = \alpha I_{ES}$$
$$i_E = I_{EO} = i_x - \alpha_R I_y$$

Thus $$I_{EO} = I_{ES}(1 - \alpha\alpha_R) \quad (1)$$

Similarly, from the case where E is open,

$$I_{CO} = I_{CS}(1 - \alpha\alpha_R) \quad (2)$$

The current through any diode is given by

$$i_D = I_{DO}\,(e^{qv/kt} - 1)$$

where I_{DO} is the reverse−bias current, v is the voltage across the diode, and q/kT is a temperature−dependent constant. Therefore, from the figure and the definitions of I_{ES} and I_{CS}, we have

$$i_x = I_{ES}\,(e^{[\{q(v)EB\}\,/\,kT]} - 1)$$
$$i_y = I_{CS}\,(e^{[\{q(v)CB\}\,/\,kT]} - 1)$$

and so

$$i_E = I_{ES}\,(e^{[\{q(v)EB\}\,/\,kT]} - 1) - \alpha_R I_{CS}(e^{[\{q(v)CB\}\,/\,kT]} - 1) \quad (3)$$
$$i_C = \alpha I_{ES}\,(e^{[\{q(v)EB\}\,/\,kT]} - 1) - I_{CS}(e^{[\{q(v)CB\}\,/\,kT]} - 1) \quad (4)$$

a) The solution is obtained directly from the second Ebers−Moll equation, eq. 4.

$$i_C = \alpha I_{ES}\,(e^{[\{q(v)EB\}\,/\,kT]} - 1) - I_{CS}(e^{[\{q(v)CB\}\,/\,kT]} - 1)$$

Since both v_{EB} and $_{CB} \ll kT/q$, each expression in parentheses reduces to − 1. and so

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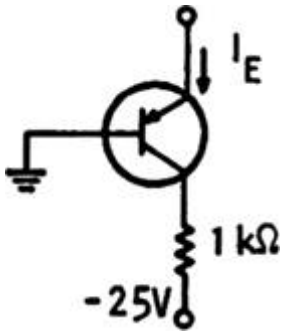
PROBLEM 01 – 0036: The transistor in the circuit shown has $\alpha_0 = 0.9$ and $I_{EO} = I_{CO} = 10\ \mu A$.
a) Find the critical emitter current that just saturates the transistor.
b) Determine the saturation voltage and its polarity.



Solution: a) With the E−B junction forward biased, the transistor will just enter saturation when the C−B junction (which was assumed to have been reverse biased) just becomes forward biased, i.e. when $V_{CB} = 0$, which with $v_B = V_B = 0$ V requires $V_C = 0$ V. The collector current is given by $I_C = [(V_C + 25) / 1]$. As I_E is increased, I_C increases. The I_C required to raise V_C to 0 is $I_C = [(V_C + 25) / 1] = 25$ mA. The corresponding input emitter current needed is $I_E = [I_C / \alpha_0] = 27.8$ mA.

b) The Ebers−Moll equations for a pnp transistor are

$$i_E = [1 / (1 - \alpha\alpha_R)] [i_{EO} (e^{[\{q(v)EB\} / kT]} - 1) - \alpha_R I_{CO}(e^{[\{q(v)CB\} / kT]} - 1)] \quad (1)$$

$$i_C = [1 / (1 - \alpha\alpha_R)] [\alpha I_{EO} (e^{[\{q(v)EB\} / kT]} - 1) - I_{CO}(e^{[\{q(v)CB\} / kT]} - 1)] \quad (2)$$

Equations 1 and 2 may be solved simultaneously for v_{EB} and v_{CB}. If i_E and i_C are both considered in absolute value, the junction voltages are given by

$$v_{EB} = (kT / q) \ln [1 + \{(i_E \alpha_R i_C) / (I_{EO})\}] \quad (3)$$

$$v_{CB} = (kT / q) \ln [1 + \{(- i_C + \alpha i_E) / (I_{CO})\}] \quad (4)$$

The saturation voltage is $v_{CE} = v_{CB} = v_C - v_E$. By definition of the edge of saturation $v_{CB} = 0$ which, with $v_B = 0$ reduces to $v_C = 0$. In this case the saturation voltage $v_{CE} = - v_E$. Substitution into eq. 3 yields

$$V_{EB} = V_E = 40 \ln (1 + 528) = 163 \text{ mV}$$

from which the saturation voltage is $v_{CE} = - 0.163$ V or $v_E > v_C$ for a pnp transistor at the edge of saturation.

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PROBLEM 01 – 0037: Establish that the transistor in the circuit in Fig. 1 is operating in the active mode. Assume that β equals 99 for this transistor. Find i_B and i_C.

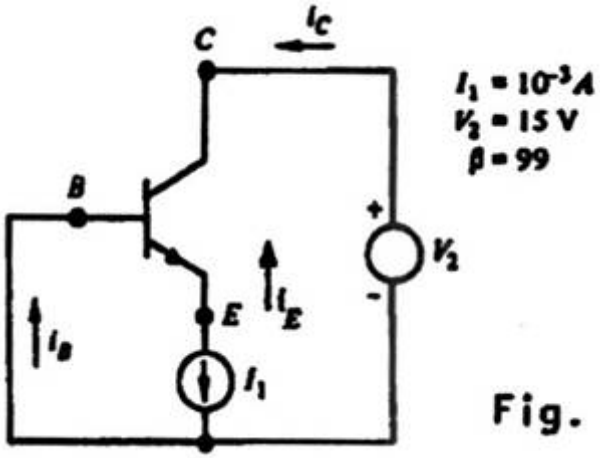


Fig. 1

Solution: In the active mode the emitter–base junction is forward biased and the collector–base junction reverse biased. The current source I_1 causes a negative emitter current to flow. The base–emitter junction resembles a diode, so that

$$i_E \approx - I_{ES}[\exp\{(qV_{BE}) / (kT)\} - 1]$$

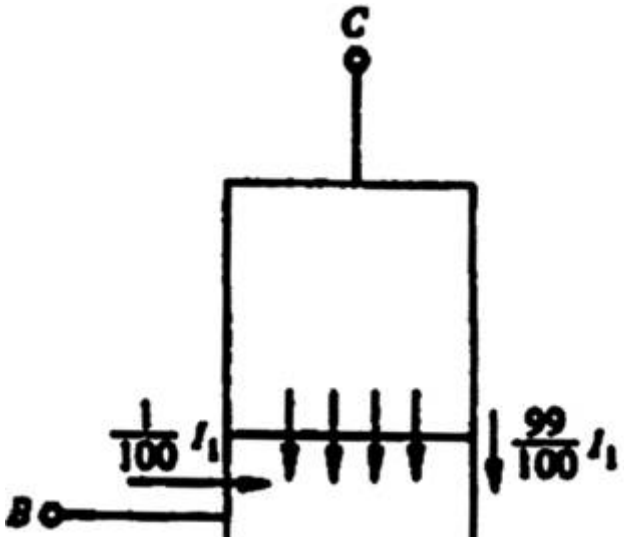
where I_E is considered as flowing into the emitter. Since, as we said, I_E is negative, then the exponential term must be greater than 1, and therefore V_{BE} must be positive, and so forward–biased. The collector–base voltage is simply V_2. Hence the collector junction is reverse biased by 15 volts. With the emitter–base junction forward biased, and the collector–base junction reverse biased, the transistor is indeed operating in the active region. We may solve for i_B

$$i_B = - [\{i_E\} / \{\beta + 1\}] = - [\{- I_1\} / \{\beta + 1\}]$$

$$i_B = - [\{- 10^{-3}\} / \{100\}] = 10^{-5}\ A$$

We may also find i_C

$$i_C = \beta i_B$$



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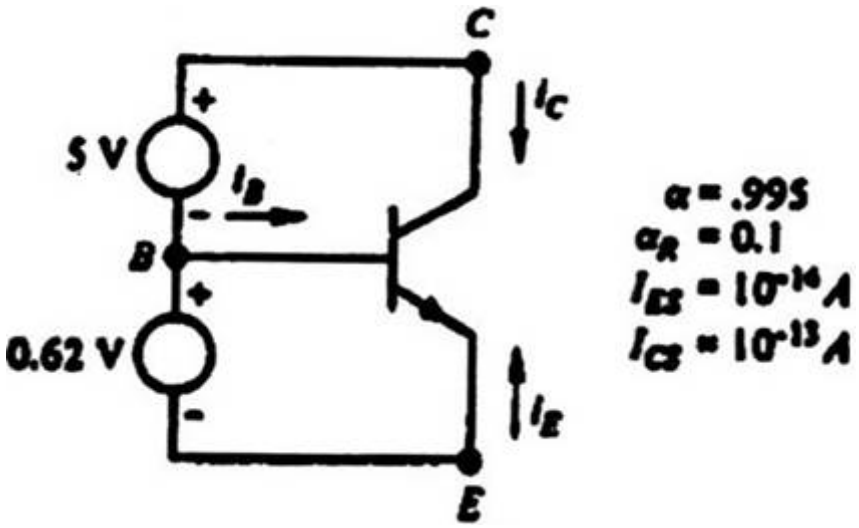
PROBLEM 01 – 0038: The transistor below has voltage sources applied between emitter and base and between base and collector; thus v_{BE} and v_{BC} are specified. Determine v_{CE}, i_E, i_B and i_C.



Solution: First, by a direct addition of voltages, $v_{CE} = 5.62$ V. To solve for i_C and i_E, we simply evaluate the following two equations governing i_C and i_E of a n–p–n transistor in the active region:

$$i_C = \alpha I_{ES} [\exp \{(qv_{BE}) / kT\} - 1] - I_{CS} [\exp \{(qv_{BC}) / kT\} - 1] \quad (1)$$

$$i_E = - I_{ES} [\exp\{(qv_{BE}) / kT\} - 1] + \alpha_R I_{CS}[\exp\{(qv_{BC}) / kT\} - 1] \quad (2)$$

At room temperature $kT/q = 0.026$ V. From equation (1)

$$i_C = 0.995 \times 10^{-14} \times [\exp(0.62 / 0.026) - 1] - 10^{-13}[\exp\{(-5.0) / 0.026\} - 1]$$

$$= 0.995 \times 10^{-14} \times 2.3 \times 10^{-10} + 10^{-13}$$

$$i_C = 2.3 \times 10^{-4} \text{ A}$$

From Equation (2)

$$i_E = - 10^{-14} (2.3 \times 10^{10}) - 10^{-14}$$

$$i_E = - 2.3 \times 10^{-4} \text{ A}$$

We obtain i_B by subtraction, that is

$$i_B = - i_C - i_E \cong 0$$

Now in reality i_B is not zero; the error stems from the approximation that $0.995 \times 2.3 \times 10^{-14} \times 10^{10}$ equals 2.3×10^{-4} in calculating i_C. Thus

$$i_B = - 0.995 \times 2.3 \times 10^{-4} + 2.3 \times 10^{-4}$$

$$i_B = 1.15 \times 10^{-6} \text{ A}$$

For the values $v_{BC} = - 5$ V, $v_{BE} = 0.62$ V.

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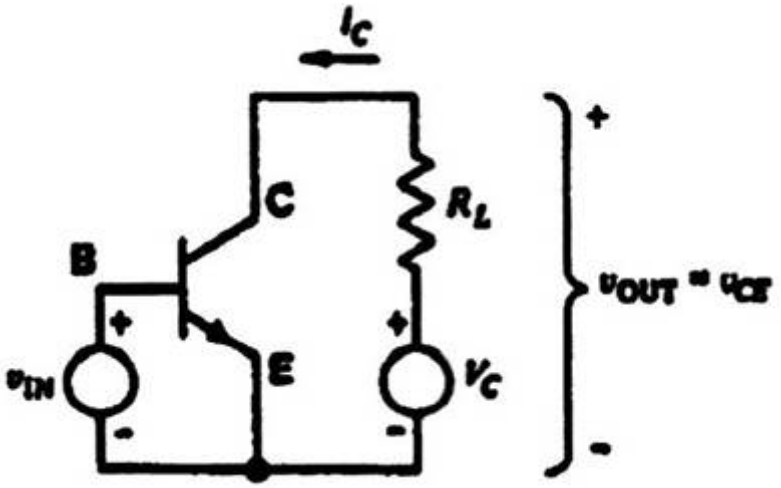
PROBLEM 01 – 0039: The transistor in the following circuit is operating in the active mode. Find the base current, collector current, and collector–to–emitter voltage, assuming that $I_{ES} = 10^{-14}$ A. Find the change in collector–to–emitter voltage assuming that the input voltage increases by 0.018 V. $v_{IN} = 0.7$ V; $R_L = 1000\ \Omega$; $V_C = 15$ V; $\beta = 200$; $kT/q = 0.026$ V. (This value corresponds to T = 300°K, that is, room temperature.)



Solution: The emitter–base junction is forward biased by 0.7 V. Furthermore the emitter current is related to the emitter-base voltage by the relationship

$$i_E = -I_{ES}[\exp\{(qv_{BE}) / (kT)\} - 1] \text{ [npn]} \qquad (1)$$

Hence,

$$i_E = -10^{-14} \exp\{(0.7) / (0.026)\} = -5 \times 10^{-3} \text{ A}$$

Since $\beta = 200$, alpha is close to one, in fact, $\alpha = [\beta / (1 + \beta)] = 0.995$. Thus i_C is nearly equal in magnitude to i_E, that is, $i_C \approx 5 \times 10^{-3}$ A. We can solve for v_{CE} by a single loop equation:

$$v_{CE} - V_C + i_C R_L = 0$$

Thus

$$v_{CE} = 15 - 5 \times 10^{-3} \times 1000 = 10 \text{ V}$$

This voltage is sufficient to assure that the transistor is indeed biased in the active region because $v_{CB} = v_{CE} - v_{BE} = 9.3$ V, and the collector–base junction is therefore reverse biased. The base current is given by

$$(i_C / \beta) = 2.5 \times 10^{-5} \text{ A}$$

We now recompute the output voltage with an 18–mV increase in the input voltage. Such an increase approximately doubles the emitter current.

$$i_E = -10^{-14} \exp\{(0.718) / (0.026\} = -10^{-2} \text{ A}$$

Therefore the base current and collector current double. From the loop equation given above $v_{CE} = 15 - 10^{-2} \times 10^3 = 5$V. (Note that the transistor remains in the active mode.) It is interesting that for a change in v_{BE} of 0.018 V, there is a change in v_{CE} of − 5 V. That is, input voltages are multiplied by a factor of $[(-5) / (0.018)] = -280$.

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PROBLEM 01 – 0040: The measured collector and base currents of a certain transistor are

$I_C = 5.202$ mA, $I_B = 50$ μA, $I_{CBO} = 2$ μA

(a) Calculate α_{dc}, β_{dc}, and I_E.

(b) Find the new level of I_B required to make $I_C = 10$ mA.

Solution: (a) In a transistor,

$$I_C = \alpha_{dc} I_E + I_{CBO}$$ (I_{CBO} is the collector leakage current)

and

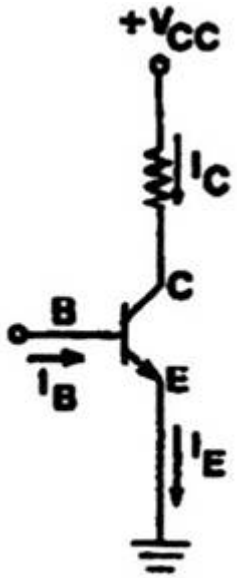
$$I_E = I_B + I_C$$

Substituting and solving for I_C, we have

$$I_C = [\{\alpha_{dc}\} / \{1 - \alpha_{dc}\}]\, I_B + [1 / \{1 - \alpha_{dc}\}]\ I_{CBO}$$

or since $\beta_{dc} = [\{\alpha_{dc}\} / \{1 - \alpha_{dc}\}]$,

$$I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO}.$$



Thus, $5.202 \text{ mA} = (\beta_{dc} \times 50\ \mu\text{A}) + (\beta_{dc} + 1)2\ \mu\text{A}$

$= \beta_{dc} (50\ \mu\text{A} + 2\ \mu\text{A}) + 2\ \mu\text{A}$

and

$$\beta_{dc} = [\{5.202 \text{ mA} - 2\ \mu\text{A}\} / \{52\ \mu\text{A}\}] = 100$$

$$I_E = I_C + I_B.$$

Therefore, $I_E = 5.202 \text{ mA} + 50\ \mu\text{A} = 5.252$ mA

$$I_C = \alpha_{dc} I_E + I_{CBO}.$$

Thus, $5.202 \text{ mA} = (\alpha_{dc} \times 5.252 \text{ mA}) + 2\ \mu\text{A}$

$$\alpha_{dc} = [\{5.202 \text{ mA} - 2\ \mu\text{A}\} / \{5.252 \text{ mA}\}] = 0.99$$

(b) $I_C = \beta_{dc} I_B + (\beta_{dc} + 1)\, I_{CBO}.$

Therefore, $10 \text{ mA} = (100 \times I_B) + (101 \times 2\ \mu\text{A})$

$$I_B = [\{10 \text{ mA} - 202\ \mu\text{A}\} / \{100\}] = 97.98\ \mu\text{A}$$

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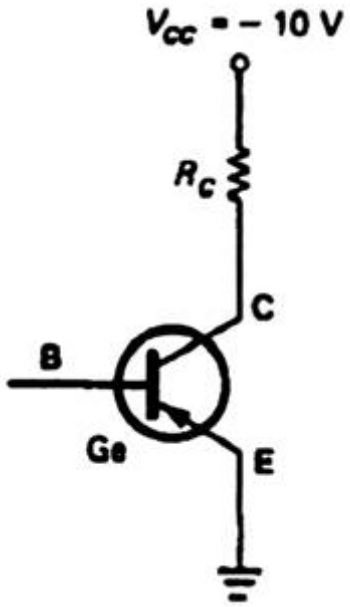
PROBLEM 01 – 0041: The transistor in the circuit shown has a maximum I_{CBO} specified at 5 μA and a beta of 25 min, 180 max. Find a value of collector resistor which will ensure that the collector voltage does not drop below 9 V with the base open−circuited.



Solution: The maximum I_{CEO} leakage current is

$$I_{CEO} = \beta I_{CBO} = 180 \times 5\ \mu A = 900\ \mu A = 0.9\ mA$$

The maximum allowable voltage drop across R_C is 10 − 9 = 1 V:

$$R_C = (V/I) = [\{1\ V\} / \{0.9\ mA\}] = 1.1.\ K$$

A 1−K resistor would be used at R_C.

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PROBLEM 01 – 0042: A transistor has the CE output characteristics drawn in Figure 2.
a) Find I_C and V_{CE} for $I_B = 50\ \mu A$, with $V_{CC} = 12$ V and $R_C = 1\ k\Omega$.
b) Repeat using $I_B = 0$.
c) Repeat using $I_B = 125\ \mu A$ and $I_B = 150\ \mu A$.
For each case, in which mode is the transistor operating?

Solution: a) The load−line equation is

$$12\ V = I_C \times 1\ k\Omega + V_{CE}$$

and is plotted as shown in Figure 2. The intersection of this load line and the $I_B = 50\ \mu A$ curve is thus $I_C = 5$ mA and $V_{CE} = 7$ V. The voltage across the 1−kΩ resistor is 5 mA × 1 kΩ = 5 V. These values can be checked by substituting into the load-line equation. In this case, the operating point lies in the active region of the transistor characteristics.

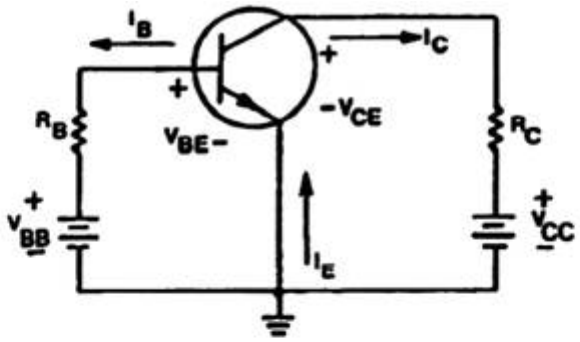

Fig. 1

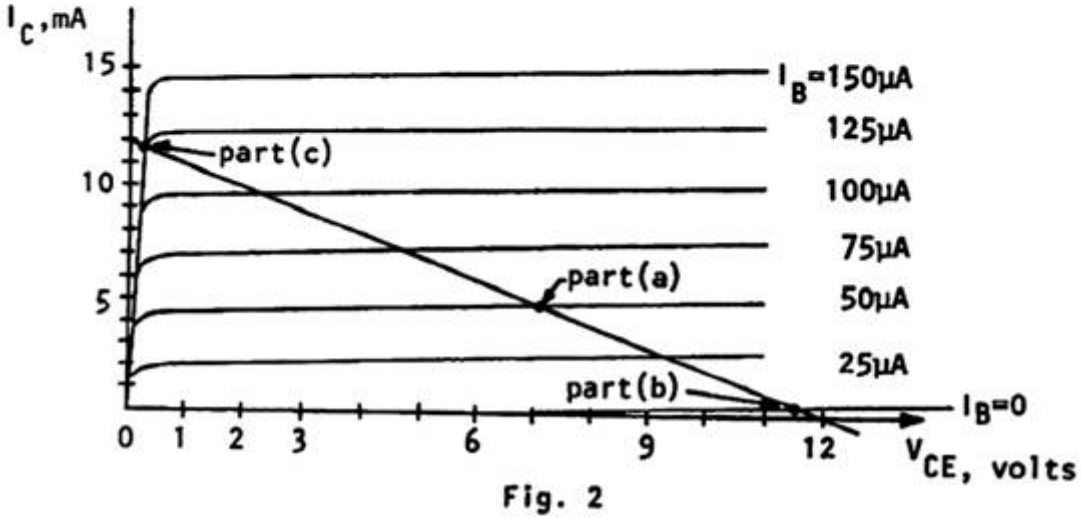

Fig. 2

b) The intersection of the load line and the $I_B = 0$ curve gives the new operating point as $I_C \approx 0$ and $V_{CE} = 12$ V. Since the transistor is in cutoff, only a small leakage current (I_{CEO}) flows and the voltage dropped across the series resistor is essentially zero. Thus $V_{CE} = V_{CC}$.
c) The intersection of the load line and the $I_B = 125\ \mu A$ curve gives the operating point as $I_C = 11.8$ mA and $V_{CE} = 0.2$ V. This operating point lies

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PROBLEM 01 – 0043: The silicon transistor of Figure 1 has the output characteristic curves drawn in Figure 2.
a) Find I_C and V_{CB} for I_E = 20 mA if V_{CC} = 40 volts and R_C = 1.6 kΩ.
b) Repeat using I_E = 0.
c) Repeat for I_E = 30 mA and I_E = 40 mA.

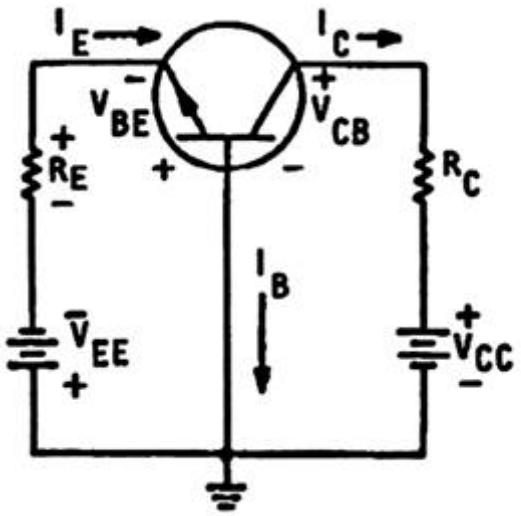

Fig. 1

Solution: a) The load−line equation is 40 V = I_C × 1.6 kΩ + V_{CB}. The plot of this line on the characteristic curvesis shown in Figure 2. Note that the two points used to plot the load line are (I_C = 0, V_{CB} = 40 V) and (I_C = 40 V/1.6 kΩ = 25 mA, V_{CB} = 0).

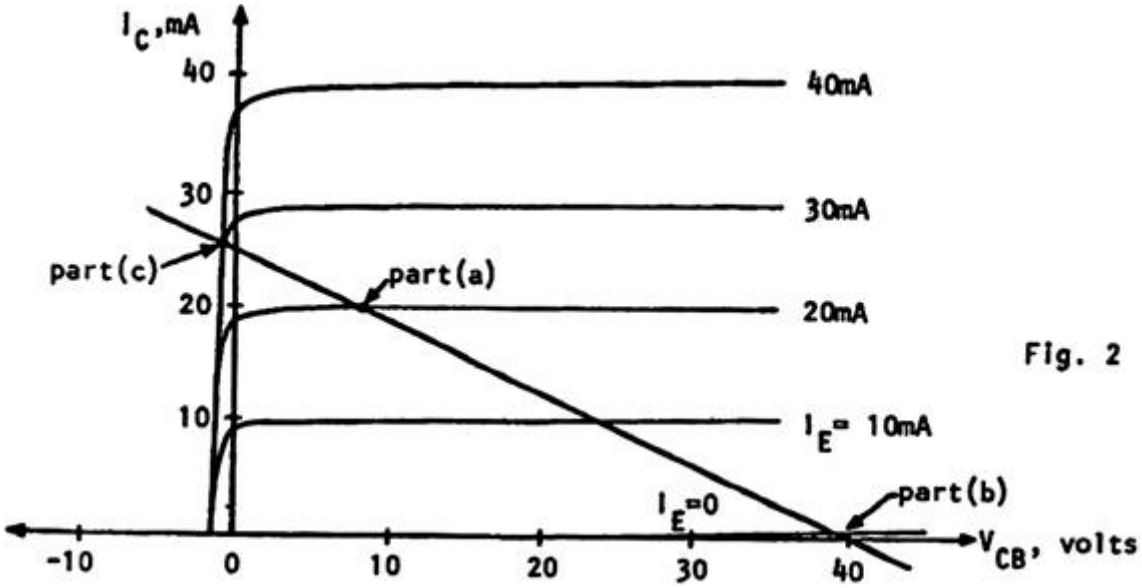

Fig. 2

The intersection of this load line and the output curve for I_E = 20 mA is the operating point. It is seen to be I_C = 19.5 mA and V_{CB} = 8.8 volts. The voltage across the 1.6−kΩ resistor is 19.5 mA × 1.6 kΩ = 31.2 V. This can be checked by substituting these values into the load−line equation. In this case, the operating point lies in the active region of the transistor

SUBJECTS HOME

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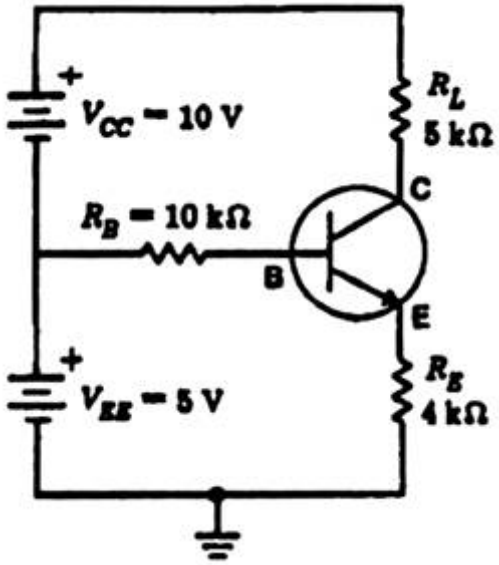
PROBLEM 01 – 0044: Find the V_{CE} for the circuit shown. Neglect V_{BE}.



Solution:

1. Find I_E

$I_E = [(V_{EE}) / (R_E)] = [(5\ V) / (4\ k\Omega)] = 1.25\ mA$

2. Find V_{CE}

$V_{CE} = V_{CC} - I_E R_L = 10\ V - (1.25\ mA)\ 5\ k\Omega$

$V_{CE} = 10\ V - 6.25\ V = 3.75\ V$

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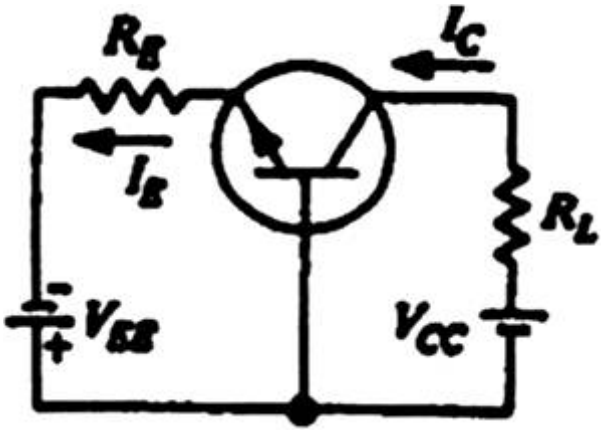
PROBLEM 01 – 0045: In the circuit shown, I_E is chosen to be 2.0 mA. If V_{EE} = 12.0 volts, V_{CC} = 12.0 volts, and R_L = 5.0 kΩ, determine (a) R_E, (b) I_C,(c) $I_C R_L$, and (d) V_{CB}.



Solution:

(a) $R_E \approx [\{V_{EE}\} / \{I_E\}] = [\{12\} / \{2(10^{-3})\}] = 6$ kΩ

(b) $I_C \approx I_E \approx 2$ mA

(c) $I_C R_L = 2.0(10^{-3})\ (5.0)(10^3) = 10$ volts

(d) $V_{CB} = V_{CC} - I_C R_L = 12 - 10 = 2.0$ volts

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PROBLEM 01 – 0046: (a) Find the transistor currents in the circuit of Fig. 1. A silicon transistor with $\beta = 100$ and $I_{CO} = 20$ nA $= 2 \times 10^{-5}$ mA is used.
(b) Repeat part (a) if a 2−kΩ emitter resistor is added to the circuit, as in Fig. 2.

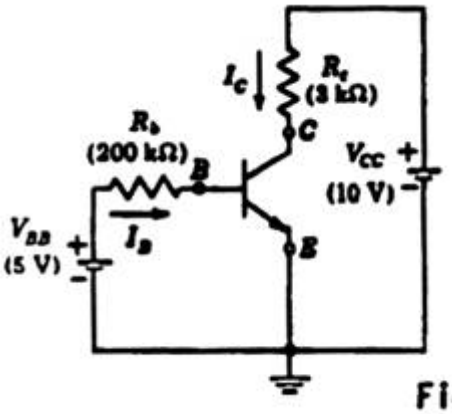

Fig. 1

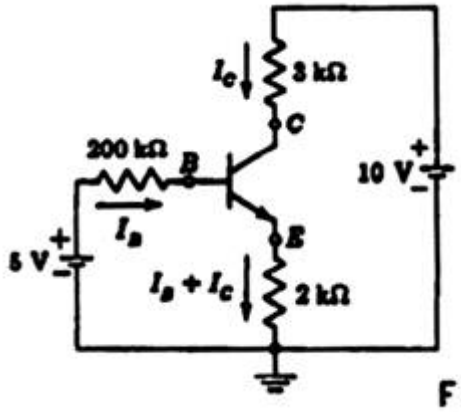

Fig. 2

Solution: (a) Since the base is forward−biased, the transistor is not cut off. Hence it must be either in its active region or in saturation. Assume that the transistor operates in the active region. From KVL applied to the base circuit of Fig. 1 (with I_B expressed in milli−amperes), we have

$$-5 + 200\, I_B + V_{BE} = 0$$

A reasonable value for V_{BE} is 0.7 V in the active region, and hence

$$I_B = [\{5 - 0.7\} / \{200\}] = 0.0215 \text{ mA}$$

Since $I_{CO} << I_B$, then $I_C \approx \beta I_B = 2.15$ mA.
We must now justify our assumption that the transistor is in the active region, by verifying that the collector junction is reverse−biased. From KVL applied to the collector circuit we obtain

$$-10 + 3\, I_C + V_{CB} + V_{BE} = 0$$

or

$$V_{CB} = 10 - (3)(2.15) - 0.7 = +2.85 \text{ V}$$

For an n−p−n device a positive value of V_{CB} represents a reverse−biased collector junction, and hence the transistor is indeed in its active region. Note that I_B and I_C in the active region are independent of the collector circuit resistance R_c. Hence, if R_c is increased sufficiently above 3 kΩ, then V_{CB} changes from a positive to a negative value, indicating that the transistor is no longer in its active region.
(b) The current in the emitter resistor of Fig. 2 is

$$I_B + I_C \approx I_B + \beta I_B = 101\, I_B$$

assuming $I_{CO} << I_B$. Applying KVL to the base circuit yields

$$-5 + 200 I_B + 0.7 + (2)(101\, I_B) = 0$$

or

$$I_B = 0.0107 \text{ mA} \quad I_C = 100\, I_B = 1.07 \text{ mA}$$

Note that $I_{CO} = 2 \times 10^{-5}$ mA $<< I_B$, as assumed.
To check for active circuit operation, we calculate V_{CB}. Thus

$$V_{CB} = -3I_C + 10 - (2)(101\, I_B) - 0.7$$

SUBJECTS HOME

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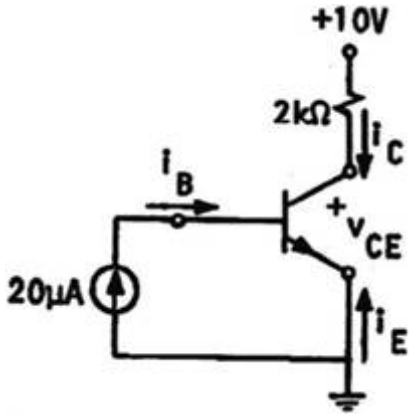
PROBLEM 01 – 0047: A silicon npn transistor with $\alpha = 0.99$ and $I_{CBO} = 10^{-11}$ A is connected as shown. Predict i_C, i_E, and v_{CE}, (Note: It is convenient and customary in drawing electronic circuits to omit the battery, which is assumed to be connected between the +10–V terminal and ground.)

Solution: For this transistor,

$$\beta = [\alpha / (1 - \alpha)] = [(0.99) / (1 - 0.99)] = [(0.99) / (0.01)] = 99$$



and the collector cutoff current is

$$I_{CEO} = (1 + \beta)I_{CBO} = (1 + 99)\ 10^{-11} = 10^{-9}\ \text{A}$$

The collector current is

$$i_C = \beta i_B + I_{CEO} = 99 \times 2 \times 10^{-5} + 10^{-9} \cong 1.98\ \text{Ma}$$

As expected for a silicon transistor, I_{CEO} is a very small part of i_C.

The emitter current is

$$i_E = -(i_B + i_C) = -(0.02 + 1.98)10^{-3} = -2\ \text{mA}$$

The collector-emitter voltage is

$$v_{CE} = 10 - i_C R_C \cong 10 - 2\ (\text{mA}) \times 2\ (\text{k}\Omega) = 6\ \text{V}$$

Since $v_{CB} = v_{CE} - v_{BE} \cong 6 - 0.7 = +5.3$ V, the collector- base junction is reverse biased.

SUBJECTS HOME

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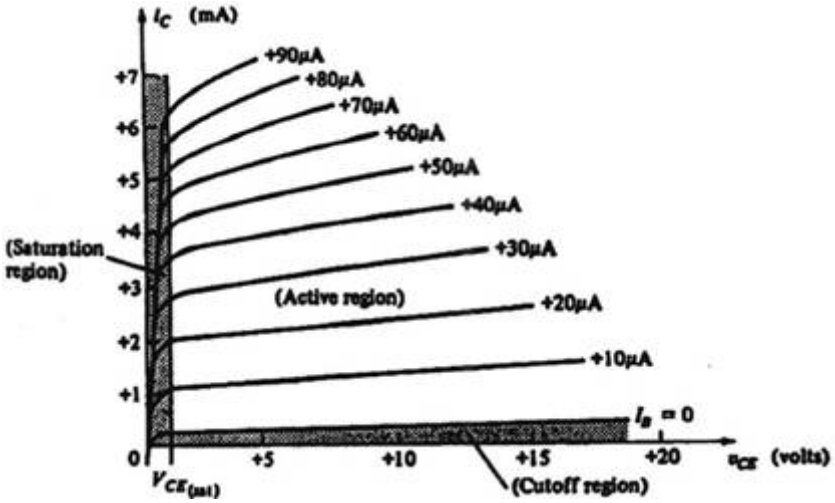
PROBLEM 01 – 0048: (a) Find the dc beta at an operating point of V_{CE} = +10 V and I_C = +3 mA on the characteristics given.
(b) Find the value of α corresponding with this operating point.
(c) At V_{CE} = +10 V find the corresponding value of I_{CEO}.
(d) Calculate the approximate value of I_{CBO} using the β_{dc} obtained in part (a).

Solution: (a) At the intersection of V_{CE} = +10 V and I_C = +3 mA, I_B = +25 μA, so that

$$\beta_{dc} = (I_C / I_B) = [(3 \times 10^{-3}) / (25 \times 10^{-6})] = 120$$

(b) $\alpha = [\beta / (\beta + 1)] = (120 / 121) \cong 0.992$



(c) I_{CEO} is the emitter current (equal to the collector current) that flows when I_B = 0. From the characteristics, we find

$$I_{CEO} = 300\ \mu A$$

(d) $I_{CBO} \cong (I_{CEO} / \beta) = [(300\ \mu A) / 120] = 2.5\ \mu A$

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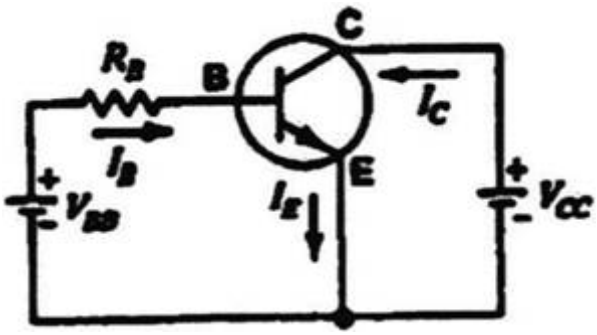
PROBLEM 01 – 0049: A silicon transistor is used in the circuit shown. If V_{BB} is 4 volts, and $I_B = 50\ \mu A$,
(a) determine with $V_{BE} = 0.7$ and $V_{BE} = 0$.
(b) Repeat (a) for $V_{BB} = 12$ V.

Solution: (a) With $V_{BE} = 0.7$ V,

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(4.0 - 0.7) / \{50(10^{-6})\}] = 66\ k\Omega$$

With $V_{BE} = 0$ V,

$$R_B = [V_{BB} / I_B] = [(4.0) / \{50(10^{-6})\}] = 80\ k\Omega$$



From the above, we can conclude that the second solution might be too approximate. Actually, it contains a 21 percent error.

(b) With $V_{BE} = 0.7$ V,

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(12 - 0.7) / \{50(10^{-6})\}] = 226\ k\Omega$$

With $V_{BE} = 0$ V,

$$R_B = [V_{BB} / I_B] = [12 / \{50(10^{-6})\}] = 240\ k\Omega$$

Here we have only a 6.2 percent discrepancy, so when the battery voltage is much greater than the base-emitter voltage drop then the approximation of $V_{BE} = 0$ is appropriate.

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PROBLEM 01 – 0050: Calculate I_B and I_C in the circuit of Figure 1 at 25°C and at 55°C if the transistor is silicon and has $\beta_{DC} = 100$ and $I_{CBO} = 0.1\ \mu A$ at 25°C.

Solution: (a) At 25°C:

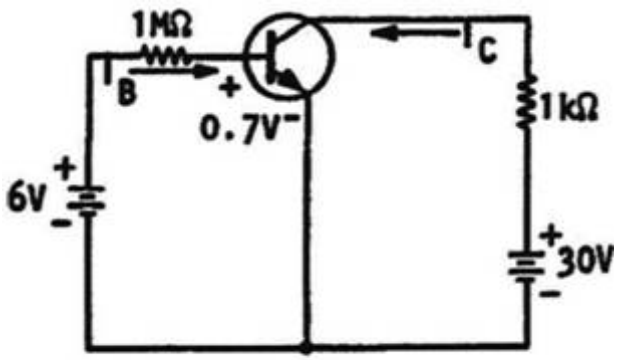

Fig. 1

$I_B = [(6\ V - 0.7\ V) / (1\ M\Omega)] = 5.3\ \mu A$

$I_C = \beta_{DC} \times I_B + I_{CEO}$

$= 100 \times 5.3\ \mu A + 101 \times 0.1\ \mu A$

$= 530\ \mu A + 10.1\ \mu A = 540.1\ \mu A$

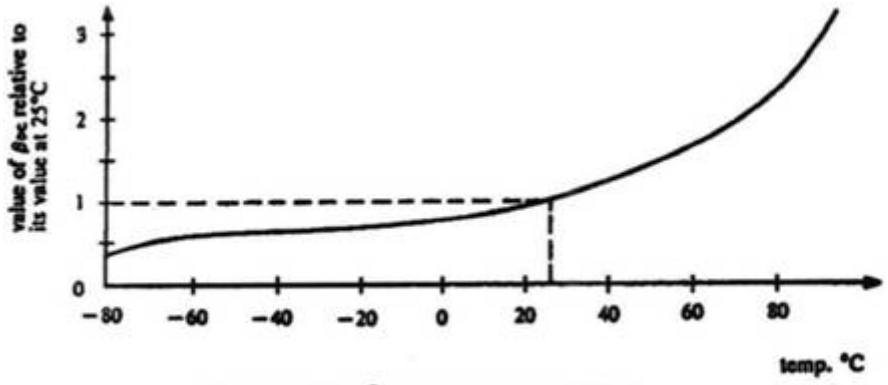

Fig. 2

VARIATION OF β_{DC} WITH TEMPERATURE

(b) At 55°C:

$V_{BE} = 0.7\ V - (30) \times (2\ mV) = 0.64\ V$

$I_{CBO} = 0.1\ \mu A$ doubled 3 times $= 0.8\ \mu A$

$\beta_{DC} = 1.45 \times 100 = 145$ (from Figure 2)

Thus

$I_B = [(6\ V - 0.64\ V) / (1\ M\Omega)] = 5.36\ \mu A$

$I_C = 145 \times 5.36\ \mu A + 146 \times 0.8\ \mu A$

$= 777\ \mu A + 116.8\ \mu A = 893.8\ \mu A$

SUBJECTS HOME

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PROBLEM 01 – 0051: A certain transistor has $h_{FE} = 50$. If the base current is 0.1 mA, and we ignore the small leakage current, what is the collector current? What happens if the base current is changed to 0.2 mA?

Solution:

$$h_{FE} = (I_C / I_B)$$

so that

$$I_C = h_{FE} I_B$$

$$I_C = (50)\ (0.1)\ (10^{-3}) = 5.0 \text{ mA}$$

If the base current is changed to 0.2 mA, the collector current becomes

$$I_C = (50)\ (0.2)\ (10^{-3})$$

$$I_C = 10.0 \text{ mA}$$

The parameter h_{FE} is the low-mid frequency short-circuit CE current gain, which will be discussed extensively in Chapter 4.

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PROBLEM 01 – 0052: Fig. 1 shows an Si transistor in the grounded emitter configuration. The transistor has $h_{FE} = 30$ and the reverse cutoff current is negligible. The base can be shifted to five different positions. Estimate for these positions, the values of I_C and V_{CE} .

Solution: First note that the transistor is PNP (emitter arrow points inwards). This is important in determining the state of the transistor.

A: $V_{BE} = +1$ V which is reverse biased for a PNP transistor .The transistor is in cutoff and the collector current, I_C is 0. Using KVL,

$V_{CE} = V_{CC} = -15$ V. Fig. 2 shows the location of point A and the other point.

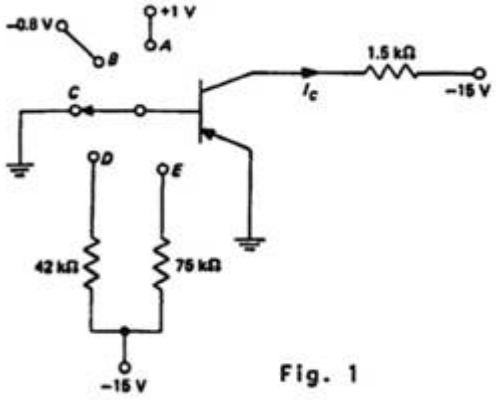

Fig. 1

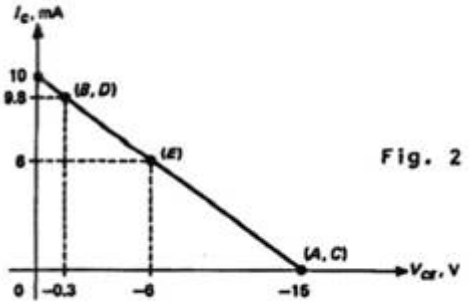

Fig. 2

B: V_{BE} is now – 0.8 V. This voltage is enough to drive the transistor into saturation producing a typical $V_{CE,\,sat} = -0.3$ V. Also note that $V_{CB} = V_{CE} - V_{BE} = 0.5$ V meaning that the collector base junction is forward biased which is a condition for saturation.

The collector current, I_C , is

$$I_C = [(V_{CC} - V_{CE}) / R_C] = [(15 - 0.3) / (1.5 \times 10^3)] = 9.8 \text{ mA}$$

C: Both the base and emitter are grounded, therefore $V_{BE} = 0$ and the transistor is again in cutoff as in A.

D: The base current can be calculated here by neglecting the V_{BE} drop which will be small compared with the 15 V source.

$$I_B \approx [15 / (42 \times 10^3)] = 0.357 \text{ mA}$$

Assume that the transistor is in the active region and calculate I_C.

$$I_C = h_{FE} I_B = 30(0.357 \times 10^{-3}) = 11.71 \text{ mA}$$

The maximum collector current = $(V_{CC} / R_L) = [15 / (1.5 \times 10^3)]$ = 10 mA. Therefore the results obtained were wrong and the assumption was incorrect; the transistor is instead in saturation, and the results btained in B are valid here.

E: Using the same procedure as in D:

$$I_B \approx [15 / (75 \times 10^3)] = 0.2 \text{ mA}$$

Assume the transistor is active again.

$$I_C = h_{FE} I_B = 30(0.2 \text{ mA}) = 6 \text{ mA}$$

I_C is below the maximum so our assumption is correct up to now.

SUBJECTS HOME

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PROBLEM 01 – 0053: (a) In Figure 1, if $h_{FE} = 100$, determine whether or not the silicon transistor is in saturation and find I_B. and I_C
(b) Repeat with the 2 kΩ emitter resistance added (Fig. 2).

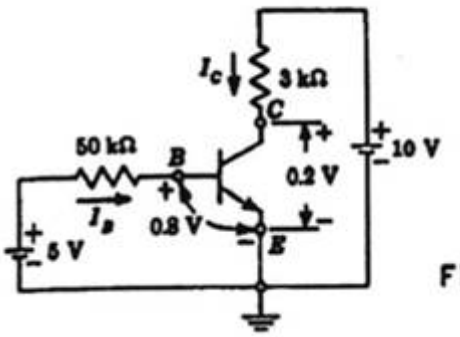

Fig. 1

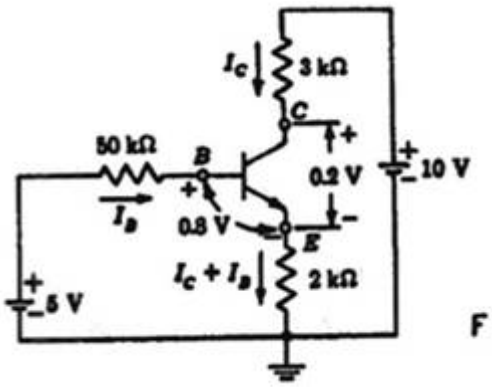

Fig. 2

Solution: (a) Assume that the transistor is in saturation. Applying KVL to the base circuit gives

$$-5 + 50I_B + 0.8 = 0$$

or

$$I_B = (4.2 / 50) = 0.0840 \text{ mA}$$

Applying KVL to the collector circuit yields

$$-10 + 3I_C + 0.2 = 0$$

or

$$I_C = (9.8 / 3) = 3.267 \text{ mA}$$

The minimum value of base current required for saturation is

$$I_B(\text{min}) = (I_C / h_{FE}) = [(3.267) / 100] = 0.0327 \text{ mA}$$

Since $I_B = 0.0840 > I_B(\text{min}) = 0.0327$ mA, we have verified that the transistor is in saturation.

(b) Assume that the transistor is in saturation. Applying KVL to the base and collector circuits, we obtain

$$-5 + 50I_B + 0.8 + 2(I_C + I_B) = 0$$

$$-10 + 3I_C + 0.2 + 2(I_C + I_B) = 0$$

If these simultaneous equations are solved for I_C and I_B, we obtain

$$I_C = 1.96 \text{ mA} \qquad I_B = 0.00550 \text{ mA}$$

Since $I_B(\text{min}) = I_C / h_{FE} = 0.0196$ mA $> I_B = 0.00550$, the transistor is not in saturation. Hence the device must be operating in the active region.
Applying KVL to the base circuit,

$$-5 + 50I_B + V_{BE},(\text{active}) + (I_B + I_C)(2) = 0$$

Since $I_C = h_{FE}I_B$ and V_{BE},active = .7 V,

$$-5 + 50I_B + .7 + I_B(100 + 1)(2) = 0$$

$$I_B = .0171 \text{ mA}$$

$$I_C = h_{FE}I_B = (100)(.0171) = 1.71 \text{ mA}$$

Using KVL around the outer loop,

$$V_{CB} - 50I_B + 5 - 10 + 3I_C = 0$$

$$V_{CB} = +7.25$$

The transistor is indeed in the active region.

SUBJECTS HOME

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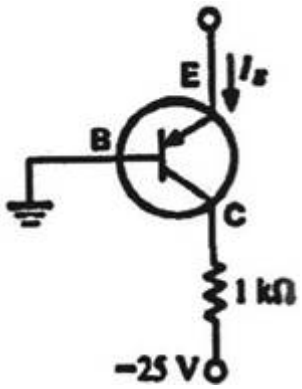
PROBLEM 01 – 0054: The transistor in the circuit shown has $\alpha_0 = 0.9$ and $I_{EO} = I_{CO} = 10\ \mu A$. Find the critical emitter current that just saturates the transistor.

Solution: With the E−B junction forward biased, the transistor will just enter saturation when the C−B junction (which was assumed to have been reverse biased)



just becomes forward biased, i.e. when $V_{CB} = 0$, which with
` $V_B = V_B = 0$ V requires $V_C = 0$ V. The collector current is given by $I_C = (V_C + 25)/1$. As I_E is increased, I_C increases. The I_C required to raise V_C to 0 is $I_C = [(V_C + 25) / 1] = 25$ mA. The corresponding input emitter current needed is $I_E = (I_C / \alpha_0) = 27.8$ mA.
Note that $\alpha = [\beta / (\beta + 1)]$.

SUBJECTS HOME

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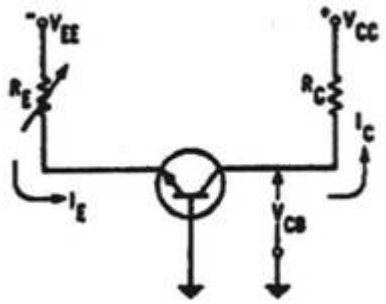
PROBLEM 01 – 0055: Suppose that in the circuit shown $V_{EE} = -21$ V, $V_{CC} = 24$ V, and $R_C = 8$ kΩ. What is the collector saturation current $I_{C(sat)}$, and what value of R_E will cause the collector to saturate?



common-base circuit

Solution: Saturation occurs when both junctions are forward biased. As a simplifying assumption, we may say that at saturation $V_{CB} = 0$, $V_{BE} = 0$, and $I_E = I_C$. Thus, the collector is saturated when the voltage across R_C is about equal to the source V_{CC}. Therefore

$$I_{C(sat)} \cong [(24 \text{ V}) / (8 \text{ k}\Omega)] = 3 \text{ mA}$$

The emitter current I_E that causes saturation is about 3 mA too. This $I_E \cong 3$ mA flows when $R_E \cong 21$ V/3 mA $\cong 7$ kΩ.

SUBJECTS HOME

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PROBLEM 01 – 0056: The behavior of the transistor in the saturation region becomes important in the design of switching circuits. To illustrate this, consider the circuit of Fig. 1, with V_{CC} = 10 V, R_b = 10 kΩ, and R_C = 1 kΩ. The transistor has β = 100, V_{BE} = + 0.7 V, and a saturation voltage $V_{CE,sat}$ = 0.1 V. Find the operating conditions when (a) V_{BB} = 1.5 V and (b) 10.7 V.

Solution: (a) For V_{BB} = 1.5 V application of KVL around the base-emitter loop yields

$$-V_{BB} + I_B R_b + V_{BE} = 0$$

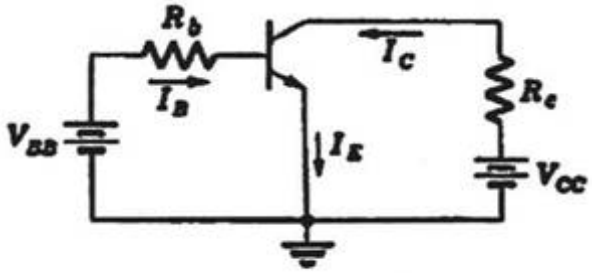

Fig. 1

or, solving for I_B

$$I_B = [(V_{BB} - V_{BE}) / R_b] = [(1.5 - 0.7) / 10^4] = 0.08 \text{ mA}$$

Since

$$I_C = \beta I_B = (100)(0.08) = 8 \text{ mA}$$

and

$$I_E \approx I_C = 8 \text{ mA}$$

We can find V_{CE} from KVL

$$V_{CE} = V_{CC} - I_C R_C = 10 - (8)(1) = 2 \text{ V}$$

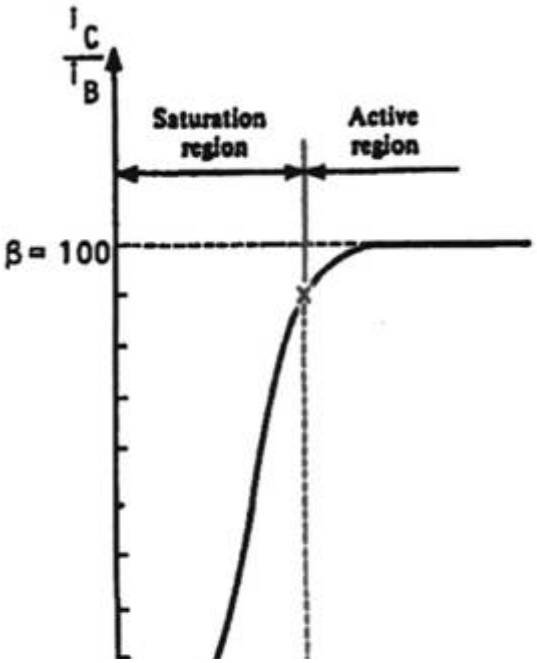

Fig. 2

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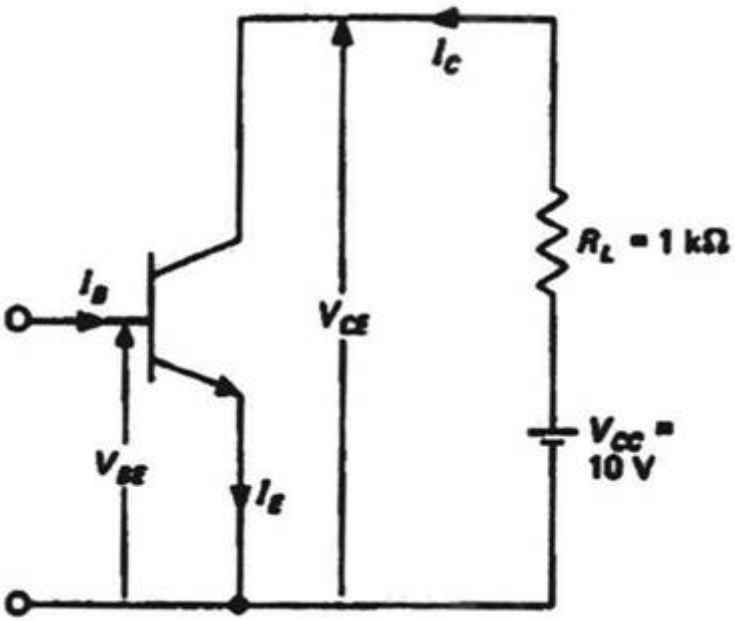
PROBLEM 01 – 0057: The transistor shown is to be driven between cutoff and active alternately by applying an appropriate voltage across the base emitter junction of the transistor.
(a) Determine the collector current, I_C, and V_{CE} for both states of the transistor assuming the transistor is ideal.
(b) Do (a) assuming that the transistor is a real Germanium transistor. What drive is needed at the base emitter junction to perform the desired task?
(c) Do (a) again, this time assuming the transistor is a real silicon transistor. What drive is needed at the base emitter junction in this case?



Solution: (a) OFF: $I_C = 0$

$V_{CE} = V_{CC} = 10$ V

ON: $I_C = (V_{CC} / R_L) = 10/1000 = 10$ mA

$V_{CE} = 0$

(b) OFF: With $V_{BE} = -0.1$ V, the transistor is turned off. The current is a certain value I_{CEX} and the voltage V_{CE} depends on I_{CEX}.$V_{CE} = V_{CC} - I_{CEX}R_L$.
ON: A voltage of about 0.3 V at the base-emitter junction is needed to turn on a germanium transistor. The collector-emitter junction will have a typical voltage of about 0.1 V ($V_{CE} \approx 0.1$ V). The collector current is $I_C = [(V_{CC} - V_{CE}) / R_C] = [(10 - 0.1) / (1{,}000)] = 9.9$ mA.
(c) OFF: For Si transistor, a V_{BE} of 0 V will turn it off. The current in the collector is some small number (for Si) I_{CES}. The voltage is then $V_{CE} = V_{CC} - I_{CEX}R_L$.
ON: A V_{BE} of about 0.7 volt is needed to turn on an Si transistor and the V_{CE} for an active Si transistor is typically 0.3 V. Therefore the collector current is

$I_C = [(10 - 0.3) / (1{,}000)] = 9.7$ mA.

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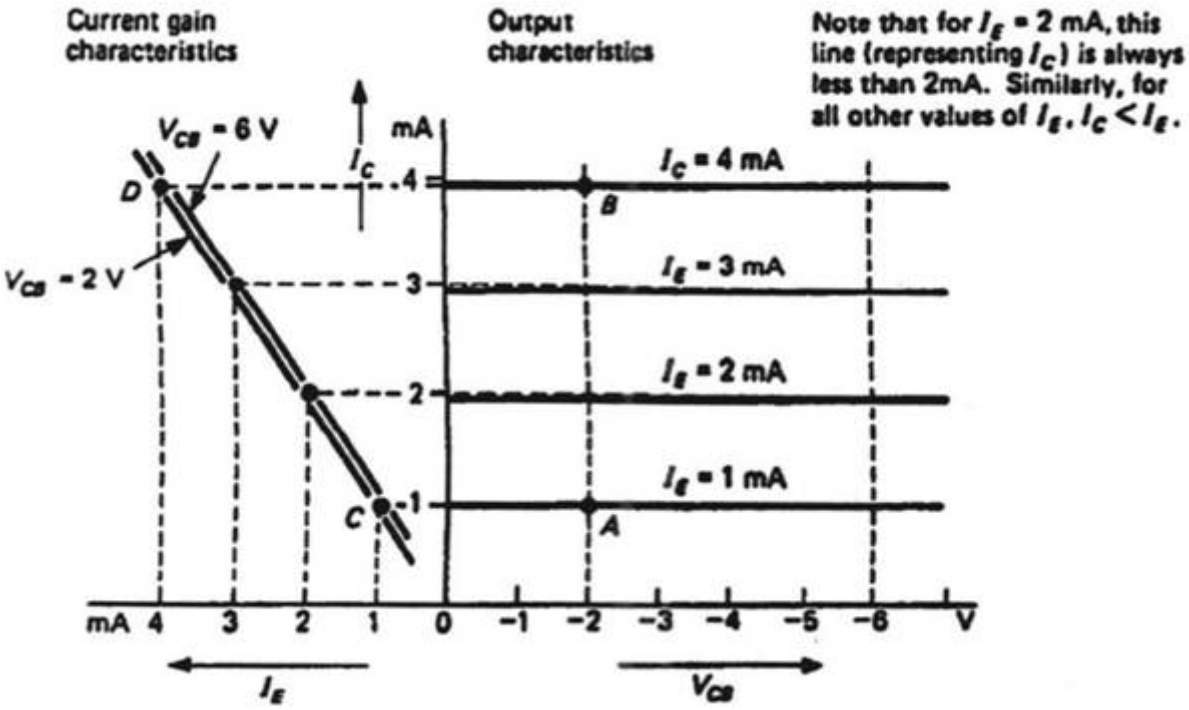
PROBLEM 01 – 0058: From the common base output characteristics shown derive the current gain characteristics for $V_{CB} = 2$ V and for $V_{CB} = 6$ V.



Solution: On the output characteristics draw a vertical line at $V_{CB} = 2$ V. Where the line intersects the output characteristics at point A, read $I_C = 0.95$ mA for $I_E = 1$ mA. Now plot point C at $I_C = 0.95$ mA on the vertical axis and $I_E = 1$ mA on the lefthand horizontal axis. Returning to the output characteristics, read $I_C = 3.95$ mA at $I_E = 4$ mA and $V_{CB} = 2$ V, point B. Now plot point D at $I_C = 3.95$ mA on the vertical axis and $I_E = 4$ mA on the horizontal axis. Draw a line through points C and D to give the current gain characteristic for $V_{CB} = 2$ V. Repeat the above procedure for $V_{CB} = 6$ V.

As can be seen, we have very nearly $I_C = I_E$. This is as expected since

$$I_C = \alpha_{dc} I_E + I_{CBO}$$

and

$$\alpha_{dc} \approx 1 \text{ and } I_{CBO} \approx 0\mu A.$$

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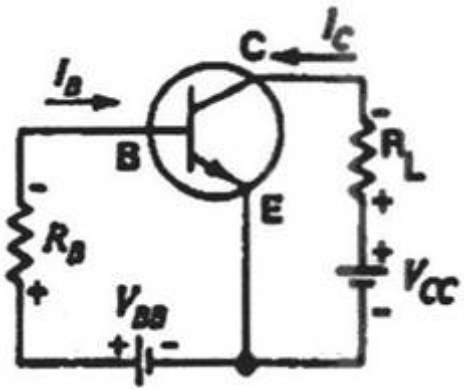
PROBLEM 01 – 0059: An n–p–n silicon transistor is chosen with V_{BB} = 6.0 volts and V_{CC} =12.0 volts. If the transistor has a β_{dc} of 50 and an I_B of 50 μA for an operating condition, determine (a) R_B, (b) I_C, (c) the dc voltage drop across R_L if R_L equals 1.0 kΩ, and (d) V_{CE}.



Solution: (a) By summing voltages around the base- emitter loop, we have

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(6.0 - 0.7) / \{50(10^{-6})\}] = 106 \text{ k}\Omega$$

(b) $$I_C = \beta I_B = 50\ (50)\ (10^{-6}) = 2.5 \text{ mA}$$

(c) knowing I_C,

$$V_{(R)L} = I_C R_L = 2.5\ (10^{-3})\ (1.0)\ (10^3) = 2.5 \text{ volts}$$

(d) this time considering the collector-emitter loop,

$$V_{CE} = V_{CC} - I_C R_L = 12 - 2.5 = 9.5 \text{ volts}$$

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PROBLEM 01 – 0060: (a) For the four circuits in Figs. 1−4, find the load line intercepts and slope. For simplicity, assume $\alpha = 1$.
(b) If the transistor used in each of the circuits has a breakdown voltage $BV_{CB} = 15$ V, which circuits will operate properly and why?

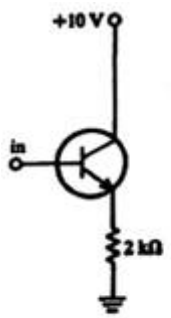

Fig. 1

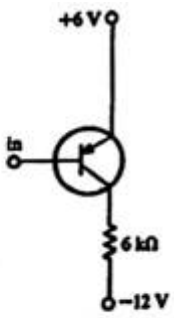

Fig. 2

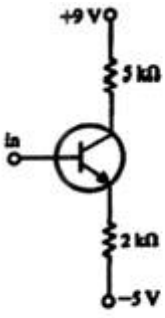

Fig. 3

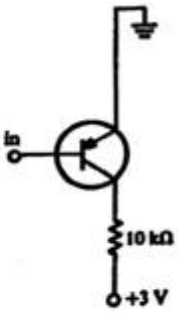

Fig. 4

Solution: (a) Figure 1: The output loop equation, obtained by summing the voltage drops from the 10 V supply to ground, is $2i_C + V_{CE} = 10$. At $i_C = 0$ we find $v_{CE} = 10$ V, while at $v_{CE} = 0$ we obtain $i_C = 5$ mA. Thus the load line intercepts are 10 V and 5 mA and the slope is $(i_C / v_{CE}) = -0.5$ mmho.
Figure 2: The output loop equation is $6i_C + v_{CE} = 18$. The intercepts are 18 V (at $i_C = 0$) and 3 mA (at $v_{CE} = 0$), and the slope is $-1/6\ (k\Omega)^{-1}$.
Figure 3: The output loop equation is $-9 + 5i_C + v_{CE} + 2i_E - 5 = 0$ or $7i_C + v_{CE} = 14$. The intercepts are thus 14 V (at $i_C = 0$) and 2 mA (at $v_{CE} = 0$) and the slope is $-1/7\ (k\Omega)^{-1}$.
Figure 4: This circuit will not work as shown since the power supply bias is wrong. There is no load line, rather the circuit sits at a single output point at $i_C = I_{CO} \approx 0$ and $v_{CE} \approx 3$ V.
(b) If we assume v_{EB} small, then $v_{CE} \approx v_{CB}$. To avoid damage to the transistor we must insure that the largest value of v_{CE} be less than the breakdown voltage of the junction or 15 V. All circuits except (2) have a v_{CE} intercept less than 15 V, so only these circuits will operate properly with a transistor having a $BV_{CB} = 15$ V.