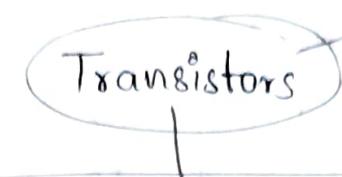


Prerequisites:

1) EDC (BJT, FET)

2) DSD (Mux, Demux, flipflops, adders)



It is a semiconductor device used to amplify or switch electronic signals.



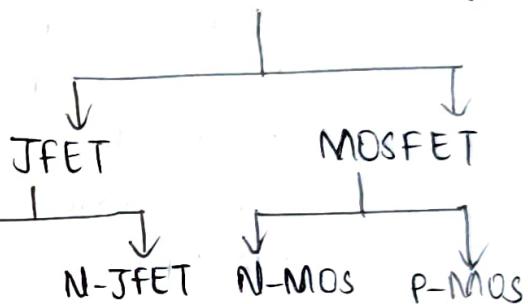
Bipolar Devices

(Both e⁻ and e⁺ takes part in conducting)

e.g.: BJT (Current controlled device)



Uni-polar devices
(Either e⁻ or e⁺ takes part in conducting)



→ Transistors

(multiple terminals)

→ Bipolar devices are current controlled whereas unipolar devices are voltage controlled.

→ BJT (Bipolar Junction Transistor)

JFET (Junction Field Effect Transistor)

MOSFET (Metal Oxide Semiconductor Field Effect Transistor)

→ MOSFET has another name called as IGFET
(Insulated Gate Field Effect Transistor)

→ 90% of syllabus is dealt with MOSFETs and 10% is dealt with Bipolar devices

→ Bipolar devices have the capability to drive the load excellently.

* MOSFET / IGFET

→ Insulated Gate Field effect Transistor (IGFET)

MOSFET

N-MOSFET

($1200 \text{ cm}^2\text{-V/sec}$)

P-MOSFET

($700 \text{ cm}^2\text{-V/sec}$) → mobility

1) Speed

2) Power utilization (low power)

3) Noise immunity (Good noise immunity)

{ 3 factors }

→ MOSFET is the building block of electronics.

→ mobility of e^-s is greater than mobility of e^+s

so, N-MOSFET is better compared to P-MOSFET

→ Whenever a device operates in saturation region,
current is maximum.

↓
that device can be
used as a switch.

→ Time taken to bring current from maximum to zero
is Reverse recovery time. reverse voltage is applied
after a negative recovery

→ In active region,

(i) Amplification is good (Used as amplifier).

→ In saturation region,

(i) Acts as switch.

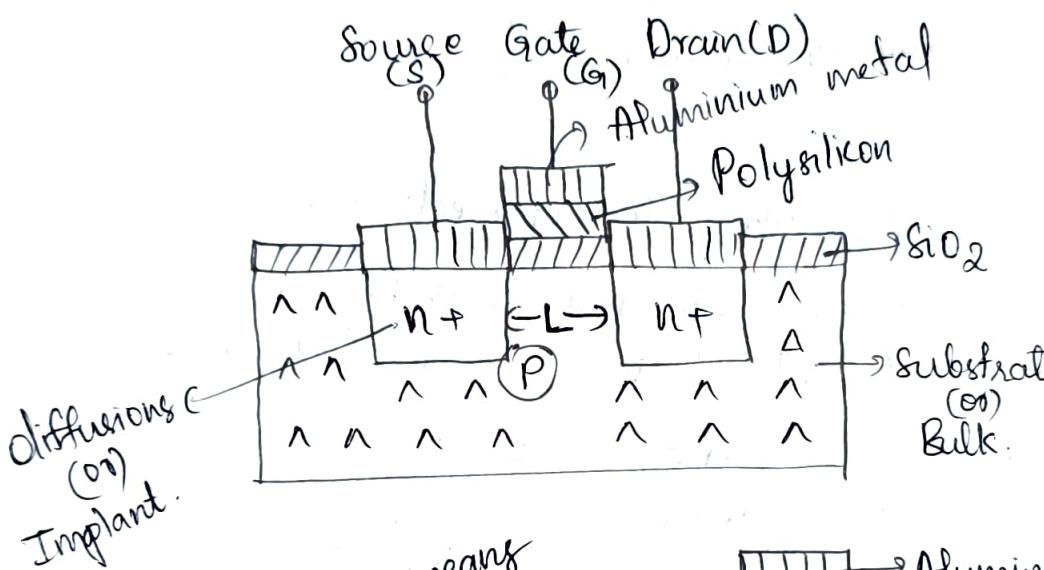
→ Switching speed is high in N-MOSFET compared
to P-MOSFET due to greater mobility of
N-MOSFET compared to P-MOSFET.

* N-MOSFET: (Enhancement mode)

- Conductivity is due to electrons (e^-)
- Substrate is doped with P-type impurities
(lightly doped)
- Implants are doped
with n-type impurities.
highly

B }
Al } (3rd group)
Ga }
In }
Tl }

- SiO_2 (silicon dioxide) acts as an insulator.



→ 5 nm technology means
length of channel = 5 nm
→ Smaller gate length
results in faster switching and low power consumption.

- Size of a MOSFET is known as Scale factor.
- The distance b/w source implant and drain implant is denoted by 'L' (length of channel)
- The width of Gate terminal is denoted by 'W'.

→ Aluminium

→ SiO_2

→ Polysilicon

→ Types of Integration

SSI (Small scale)

MSI (Medium scale)

LSI (Large scale)

VLSI (Very large scale)

ULSI (Ultra large scale)

GLSI (Giant large scale)

nano Technology

→ Length of channel (L) is varied according to the aspect ratio of (W/L) .

It determines device's performance including its switching speed, on-state resistance.

$$Z = \frac{W}{L}$$

↓
(Aspect ratio)

MOSFET (IGFET)

| (Based on structure)

↓
Enhancement
MOSFET

↓
Depletion
MOSFET

| (Based on conductivity).

↓
E-NMOSFET

↓
E-PMOSFET

↓
D-NMOSFET

↓
D-PMOSFET

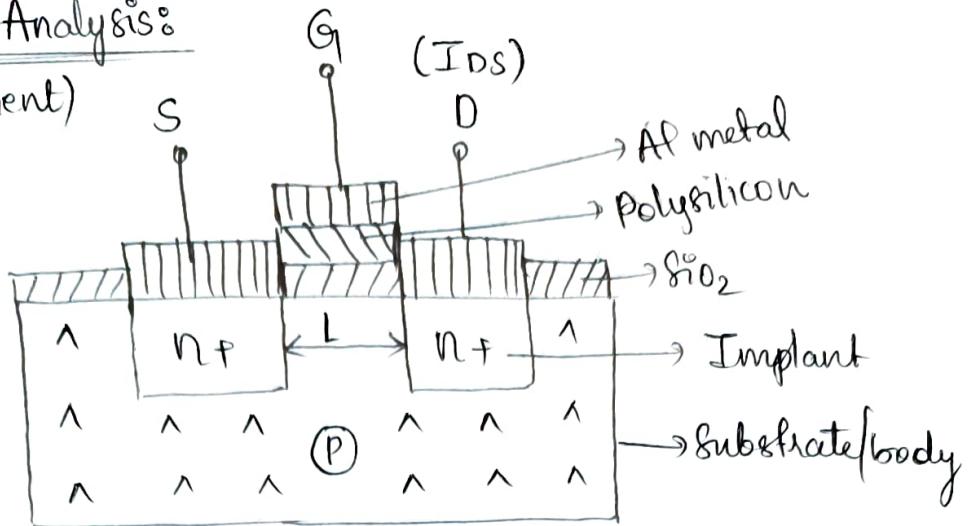
N-type: an intrinsic semiconductor doped with P, As, Sb. (e⁻s are majority charge carriers)

P-type: an intrinsic semiconductor doped with B, Al, Ga, In, Tl (holes are majority charge carriers)

Doping → CVD (Chemical Vapour Deposition)
→ PVD (Physical Vapour Deposition)

N-MOSFET Analysis:

(Enhancement)

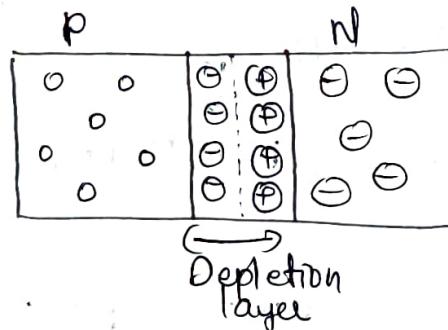


→ There are two types of current in a Semiconductor,

- ① Diffusion current (by virtue of potential difference)
- ② Drift current (n-type to p-type)

→ Diffusion current (p-type to n-type)

Holes from p-type diffuse into n-type and electrons from n-type diffuse into p-type due to concentration gradient to form a depletion region which results in the rise of diffusion current flowing from p to n side.



→ Due to the depletion region formation, there will be no movement of charge carriers.

→ In order to have the movement of charge carriers, we should apply external voltage and this process is called Biasing.

→ Biasing,

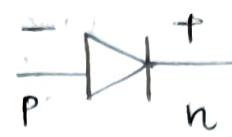
① Forward Biasing

{ +ve → p-type)
(-ve → n-type)



② Reverse Biasing

{ +ve → n-type)
(-ve → p-type)



→ Our main aim is to transfer \bar{e} 's from Source to Drain, due to this I_{DS} is developed at Drain terminal.

→ Source terminal should be forward Biased (FB)

(Source terminal → -ve)
(n-type)



repels extra \bar{e} 's in source implant
so that it reaches drain implant.

→ Drain terminal should be Reverse Biased (RB)

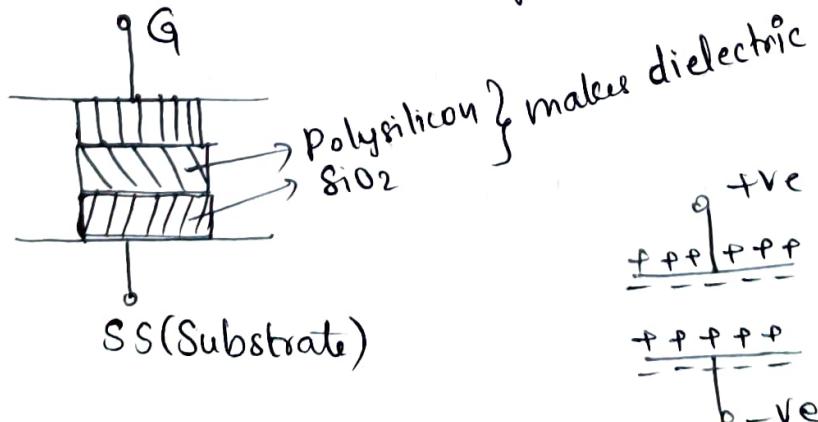
(Drain terminal → +ve)
(p-type)



attracts \bar{e} 's coming from source

→ MOSFET is a voltage controlled device and here Gate terminal acts as input terminal by controlling I_{DS} by a means of controlling gate voltage.

→ Gate to substrate acts as a capacitor



→ The input impedance of MOSFET is very high (∞)
(Due to this noise gets eliminated as
 SiO_2 acts as insulator)

- By controlling gate voltage we can control I_{DS} .
- Threshold voltage: The gate voltage at which small amount of current at drain appears is said to be threshold voltage.

→ Secondary behaviour of MOSFET,

Due to +ve gate voltage, -ve appears at channel and due to more -ve charge, the channel changes from p-type to n-type.

→ Increasing/decreasing the length of channel is called as channel length modulation

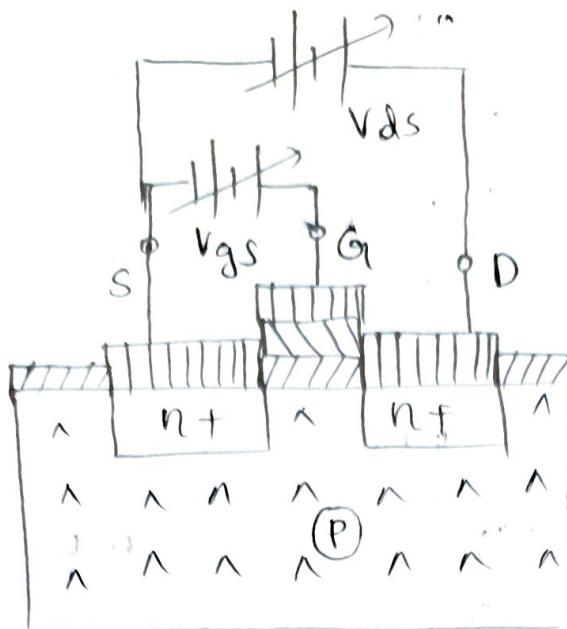
→ ~~V_{ds}~~ V_t - Threshold voltage }
 V_{GS} (V_{GG}) - Variable voltage } (voltages)
 V_{DS}
 I_{DS}

→ V_{GS} (gate \rightarrow +ve terminal; source \rightarrow -ve terminal)

→ V_{GS} (DC Analysis)
 V_{GS} (AC Analysis)

→ MOSFET consists of 4 terminals,

- Source terminal
- Gate terminal
- Drain terminal
- Substrate terminal.



- i/p voltage (V_{gs})
- o/p voltage (V_{ds})
- o/p current (I_{ds})

$$\rightarrow x = \frac{V_{ds}}{I_{ds}} \left| \begin{array}{l} \text{(Output resistance) / Drain resistance.} \\ V_{gs} - \text{constant} \end{array} \right.$$

→ Differentiation is done for two parameters
Partial differentiation is done if there are more than two parameters.

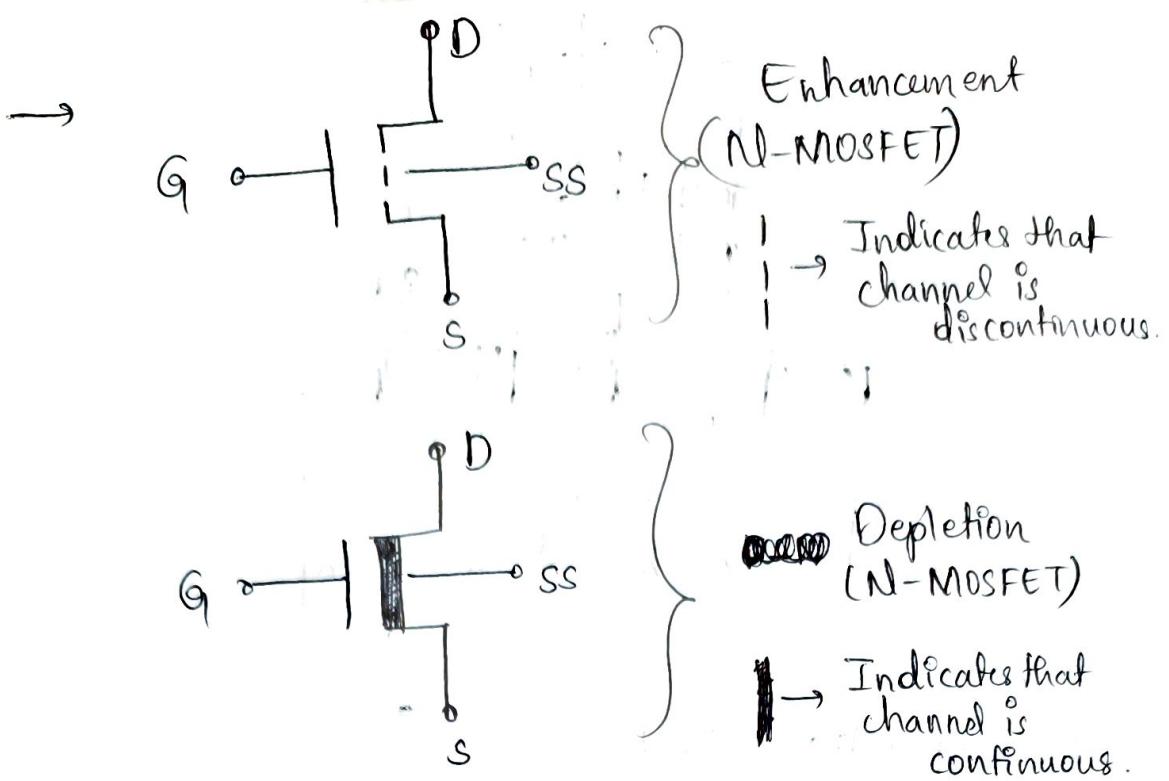
$$\frac{\partial V_{ds}}{\partial V_{ds}} \quad \frac{\partial V_{ds}}{\partial I_{ds}} \Big|_{V_{gs}-\text{const}}$$

$$\rightarrow \frac{\Delta V_{ds}}{\Delta I_{ds}} = \text{Dynamic resistance (Drain characteristics)}$$

$$\times R_{\text{mutual}} = \frac{V_{gs}}{I_{ds}} \text{ (Transfer characteristics)}$$

Transconductance

$$g_{\text{mutual}} = \frac{1}{R_{\text{mutual}}} = \frac{I_{ds}}{V_{gs}}$$



→ Keeping V_{ds} constant,

$$\text{I/p } V_{gs} = 0; \quad I_{ds} = 0$$

$$V_{gs} = 0.2V; \quad I_{ds} = 0$$

$$V_{gs} = 0.4V; \quad I_{ds} = 0$$

$V_{gs} = V_t / V_{g} / V_{\text{cut-in}}$; small amount of drain current is observed.

→ Source and Drain terminals are interchangeable and hence MOSFET is a bidirectional device.

if

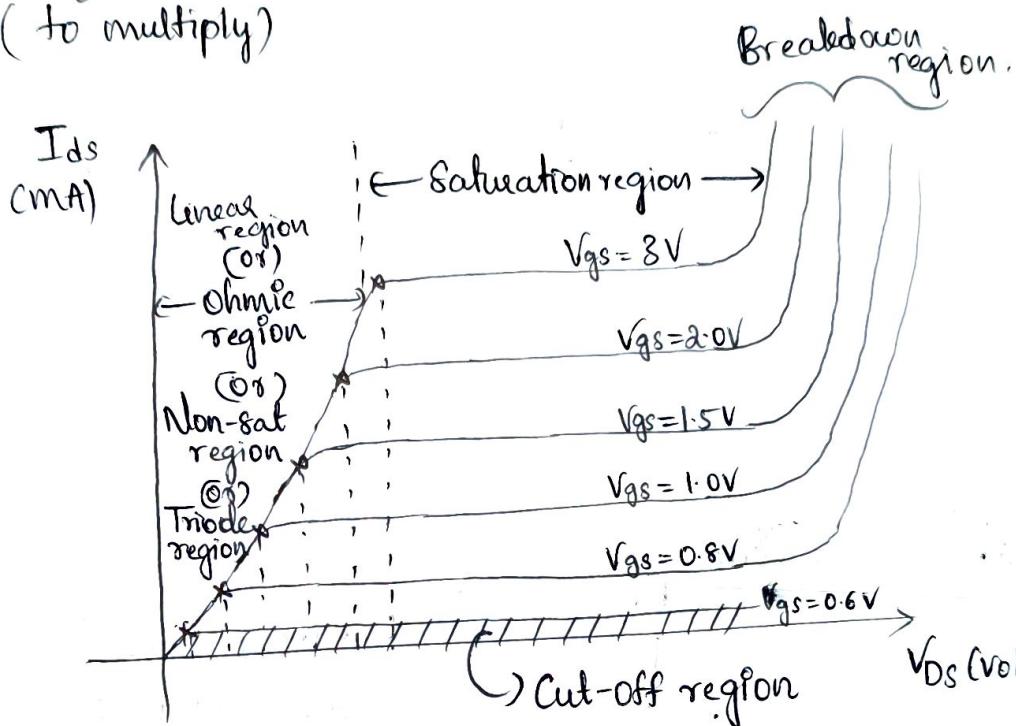
N-MOSFET characteristics:

1) Output characteristics: (Drain characteristics)

$$f(O/p) = f(V_{ds}, I_{ds}) \quad V_{gs} - \text{constant}$$

→ I_{ds} is independent of V_{ds} .

→ Avalanche breakdown is observed in MOSFET
 ↓ Latin word
 (to multiply)



coordinator $\rightarrow \left\{ \begin{array}{l} I_{ds}(\text{sat}) \\ V_{ds}(\text{sat}) \end{array} \right.$

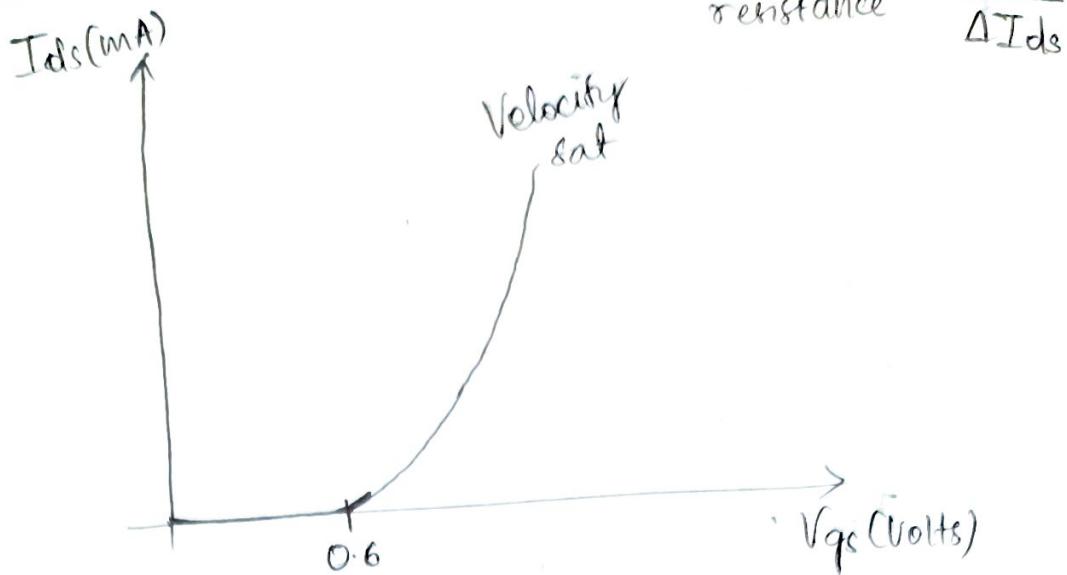
of '*' pt $\left\{ \begin{array}{l} V_{ds}(\text{sat}) - \text{the o/p voltage at which} \\ \text{max current appears.} \end{array} \right.$

→ As $V_{ds}(\text{sat})$ value increases, $I_{ds}(\text{sat})$ value also increases.

Avalanche breakdown

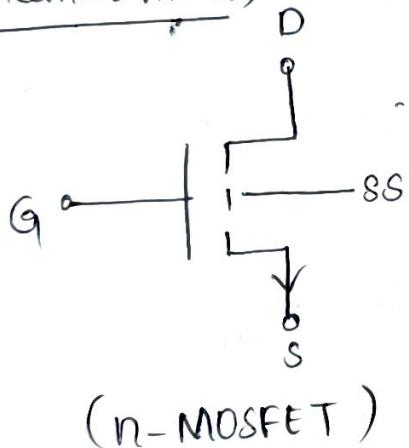
- Occurs when a high reverse voltage is applied
- As we increase reverse voltage, electric field across junction increases, this electric field exerts a force on the electrons and free them from covalent bonds. These free e⁻s start moving with high velocity across junction and collide with other atoms, thus creating more free electrons. This results in a rapid increase in net current.

2) Transfer characteristics:



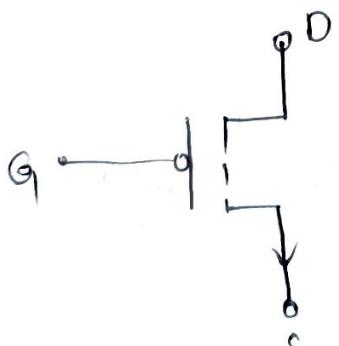
$$\text{static resistance} = \frac{\Delta V_{ds}}{\Delta I_{ds}}$$

Enhancement mode,



(n-MOSFET)

Electrons move from Source(s) to Drain(D) and current moves in opposite direction to the flow of e⁻s.



(p-MOSFET)

The dot near the gate terminal indicates that inversion of voltage

Technologies,

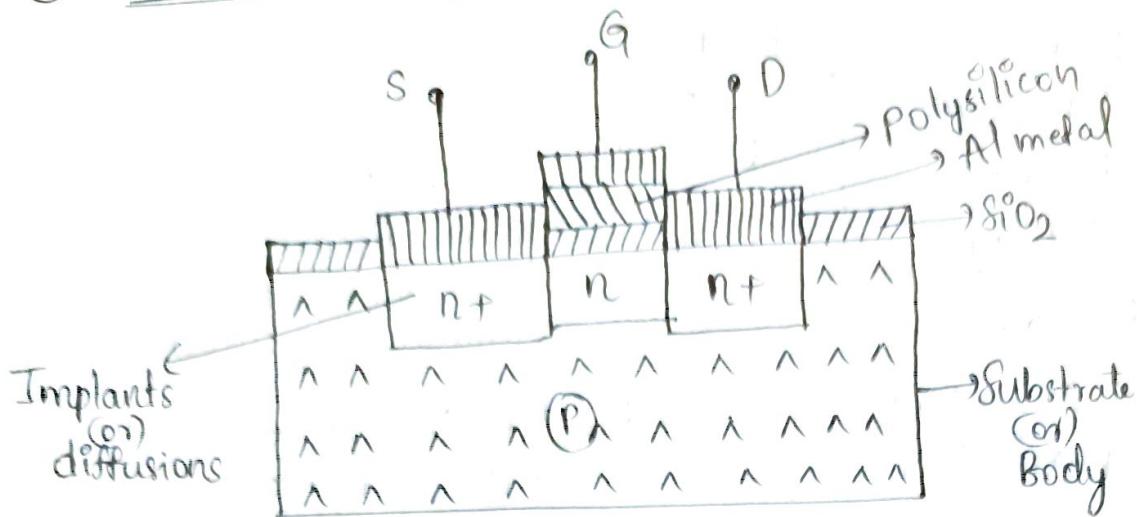
- ① R-R Logic
 - ② D-R logic
 - ③ DD Logic
 - ④ DT Logic
 - ⑤ TT logic
 - ⑥ EC Logic ✓
 - ⑦ NMOS Logic
 - ⑧ PMOS logic
 - ⑨ CMOS Logic ✓
 - ⑩ Pseudo-PMOS logic
 - ⑪ P-N MOS logic
 - ⑫ ~~CCMOS / C²MOS~~ logic
 - ⑬ ~~Domino~~ logic BICMOS ✓
- R - resistor
D - Diode
T - transistor
E - emitter
g - coupled
- Drawback / Reverse Recovery time
(Time taken to come from saturation to cutoff)
- (Emitter-Coupled logic
ie the fastest ones)
- (CMOS is low power consumed)
- BICMOS is high driving logic & less power consumed

→ DEPLETION MOSFET (Analysis)

→ MOORE's LAW

↓
prediction made by Gordon Moore in 1965 that
no. of transistors per silicon chip doubles every year.

(*) N-MOSFET Analysis (DEPLETION)

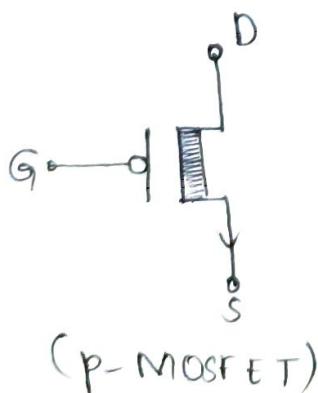
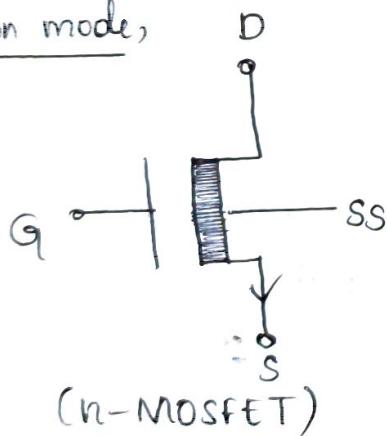


→ Our main aim is to transfer e⁻s from source to drain, due to this I_{DS} is developed at drain terminal.

→ In Depletion N-MOS, n-type channel is already deployed

→ Input impedance of Gate terminal is very high(∞) because of SiO₂ acting as an insulator.

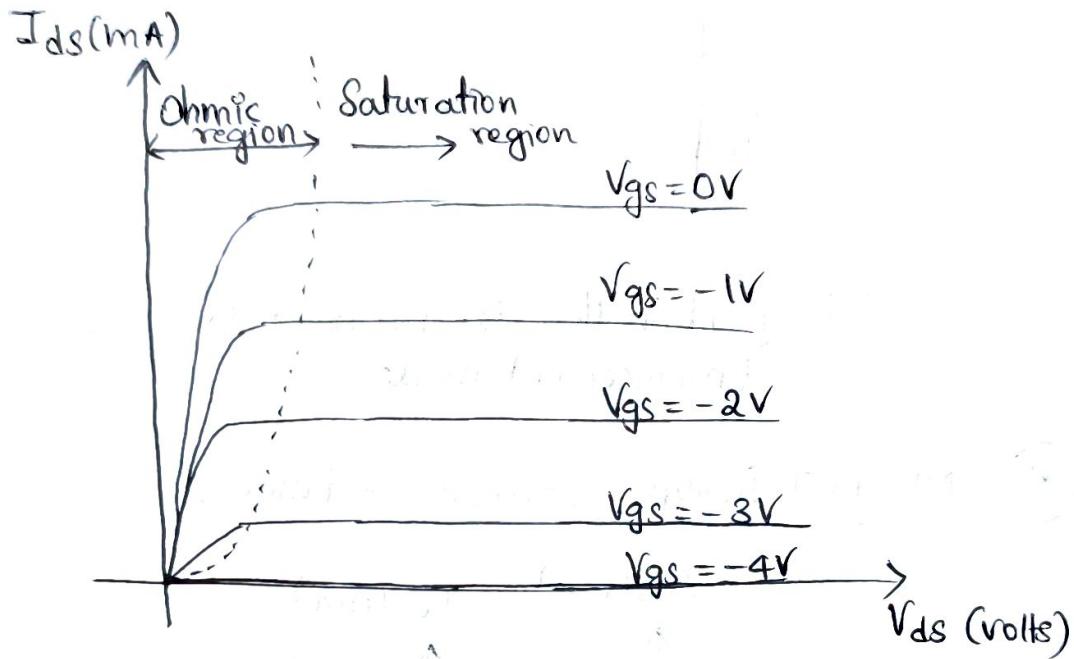
Depletion mode,



i) Output characteristics:

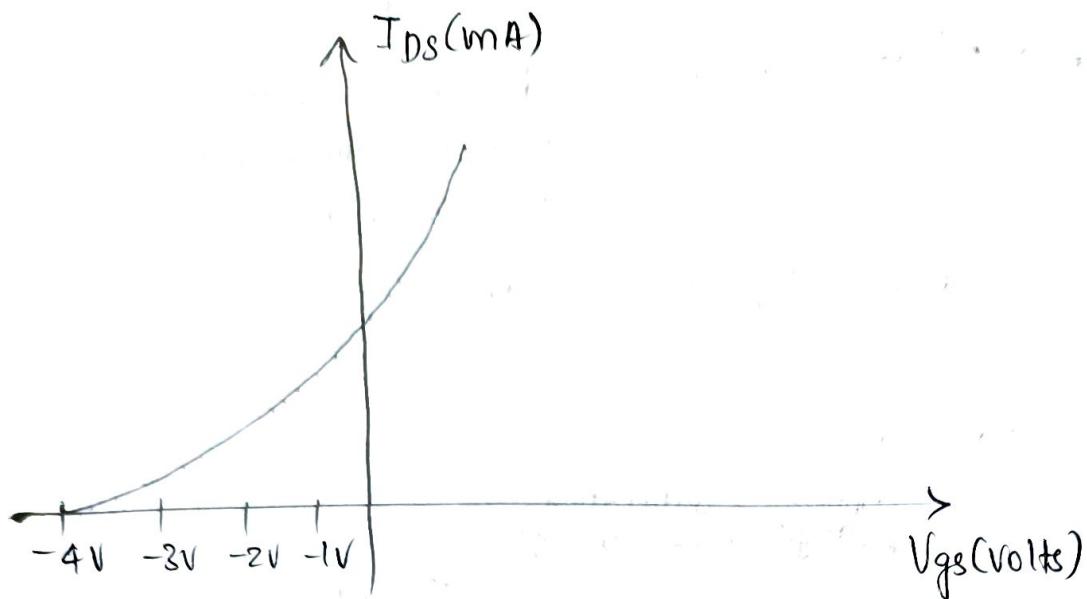
$$f(0/p) = f(V_{ds}, I_{ds}) \quad V_{gs} - \text{constant}$$

- At $V_{gs} = 0V$ (there will be movement of electrons from source to drain due to the presence of n-channel)
- I_{ds} is independent of V_{ds} .



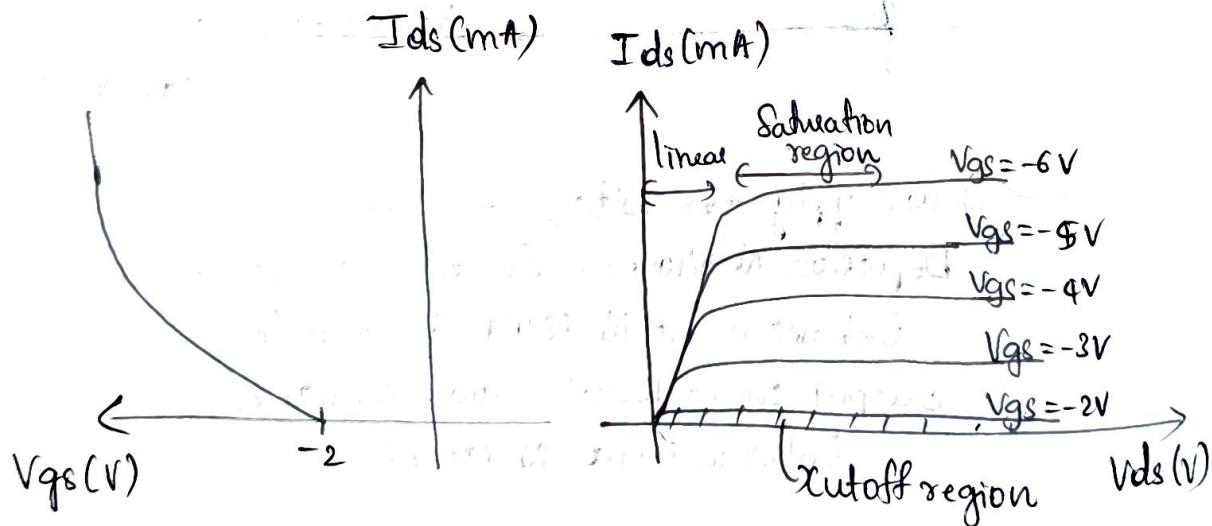
→ If we apply +ve voltages then the Depletion N-MOSFET functions similar to the Enhancement N-MOSFET and the output characteristics look similar to Enhancement N-MOSFET.

2) Transfer characteristics:



→ The graph in the 1st Quadrant looks similar to Enhancement mode.

(*) P-MOSFET Analysis: (Enhancement mode)



Topics discussed till 11/01/23,

→ Introduction class

→ MOSFET

↳ n-MOSFET } (V-I characteristics)
↳ p-MOSFET }

→ different types of Technologies

→ Logic design

(*) nMOS, pMOS, CMOS.

(*) Inverter / NOT Gate design

(*) Inverter / NOT Gate Analysis

→ Logic gates design using CMOS Logic

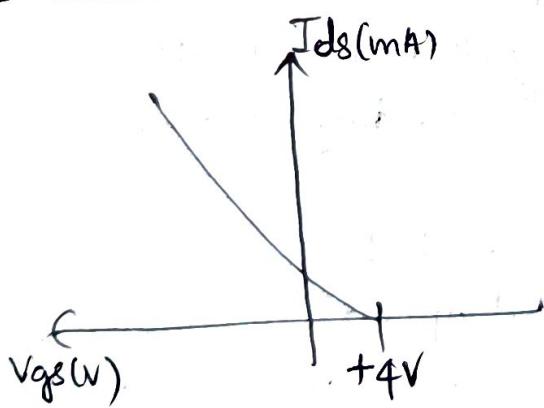
→ Fabrication process

nMOSFET pMOSFET CMOS

→ Stick diagram & Layout design

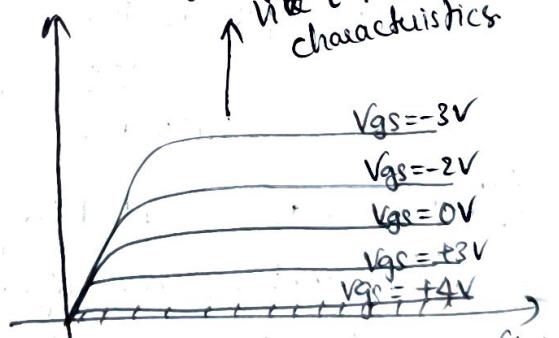
→ CMOS Analysis of

(*) P-MOSFET Analysis: (Depletion mode)



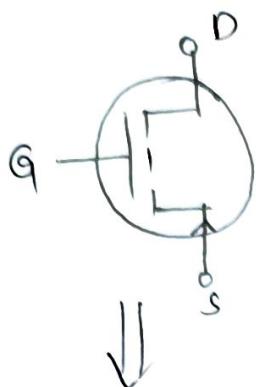
I_{ds} (mA)

above this it acts like n-MOSFET characteristics

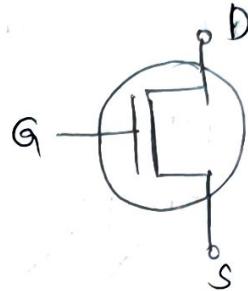
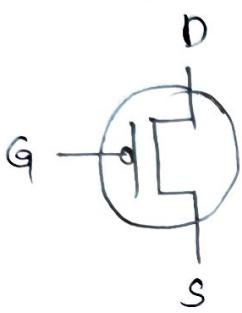


Symbols,

P-MOSFET



N-MOSFET



$$\text{CMOS} = \text{NMOS} + \text{PMOS}$$

↓
(Complementary Metal oxide Semiconductor)

→ Switching speed of N-MOS is high because electrons are majority charge carriers.

→ NOT gate is the building block of logic design whereas MOSFET is the building block of semiconductor.

Q] Why Emitter Coupled logic is fastest ?

Ans: • It achieves its high-speed operation by employing a relatively small voltage swing and preventing transistors from entering saturation region
(Reduce the storage delay time)

• ECL uses differential amplifier.

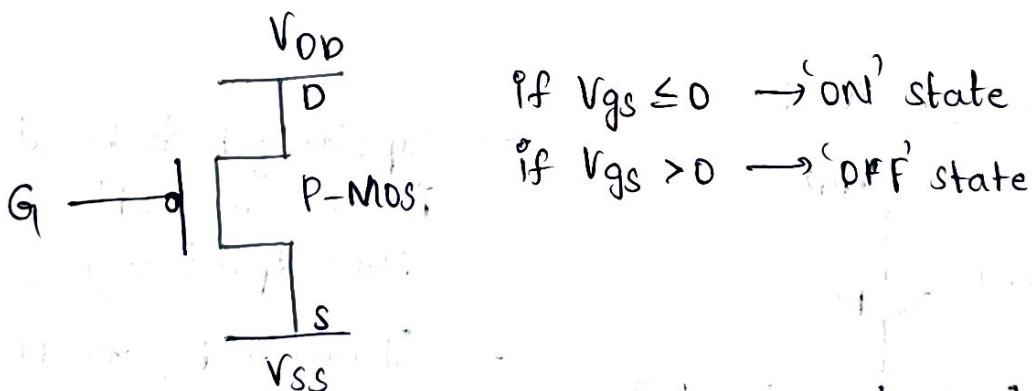
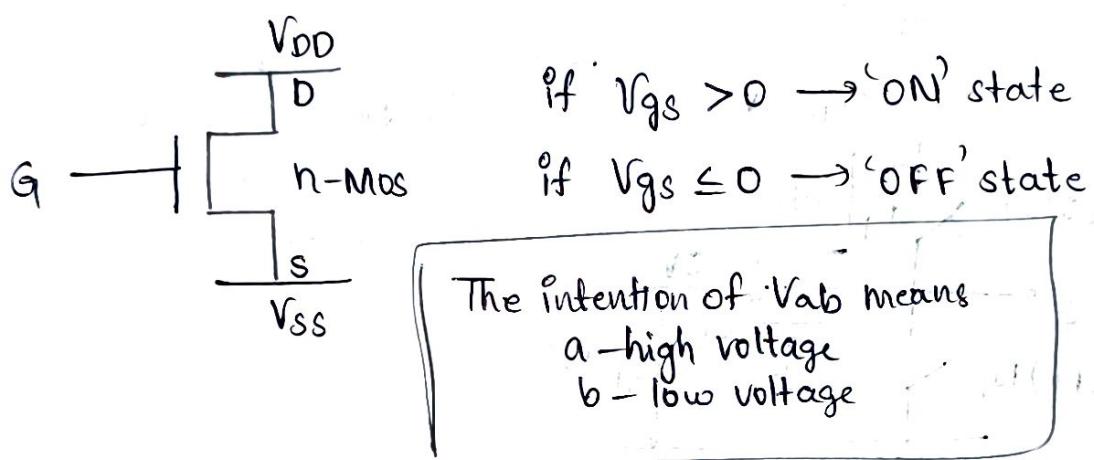
Logic Design

→ logic design is done between power rails (V_{DD} , V_{SS})

V_{DD} Pull up transistor/Region

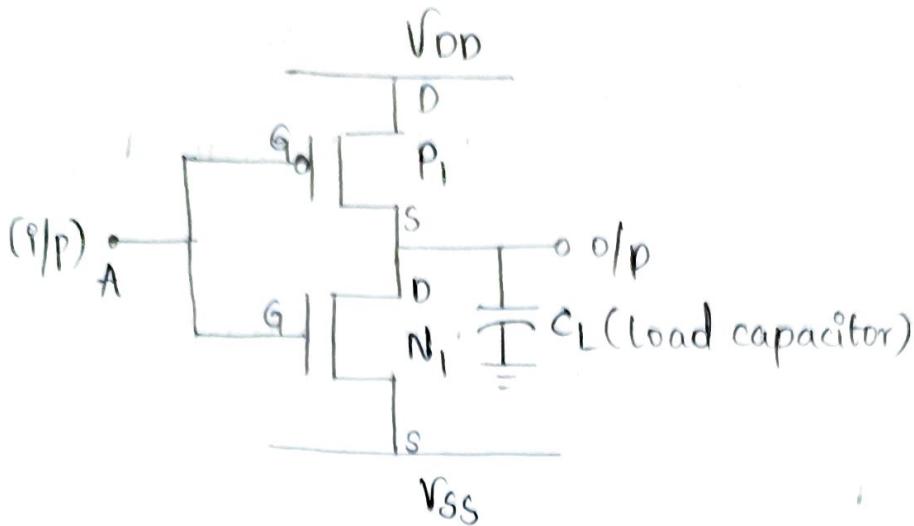
V_{SS} Pull down transistor/Region

$A \rightarrow \text{NOT gate} \rightarrow \bar{A}$ } (Inverter, Negation, Complementary)



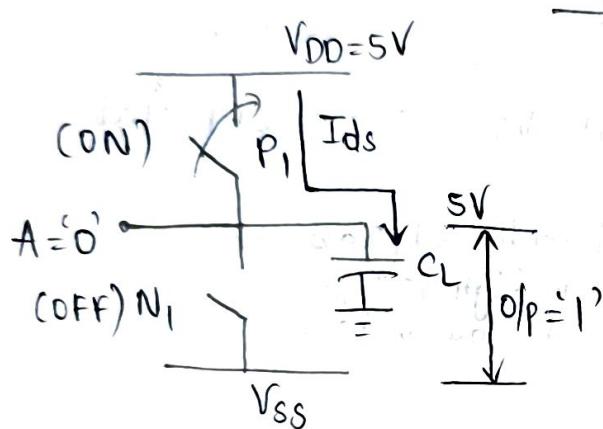
- Always PMOS is used as pull-up transistor
- Always nMOS is used as pull-down transistor.
- If they are connected reverse then it acts as a Buffer.

⑧ CMOS = NMOS + PMOS



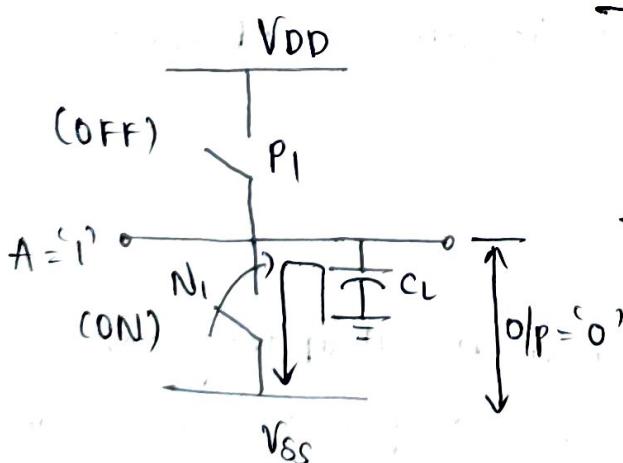
Switching diagrams,

Case-(i): $A = 0$



→ Capacitor gets charged in this case and hence the output is Logic '1'.

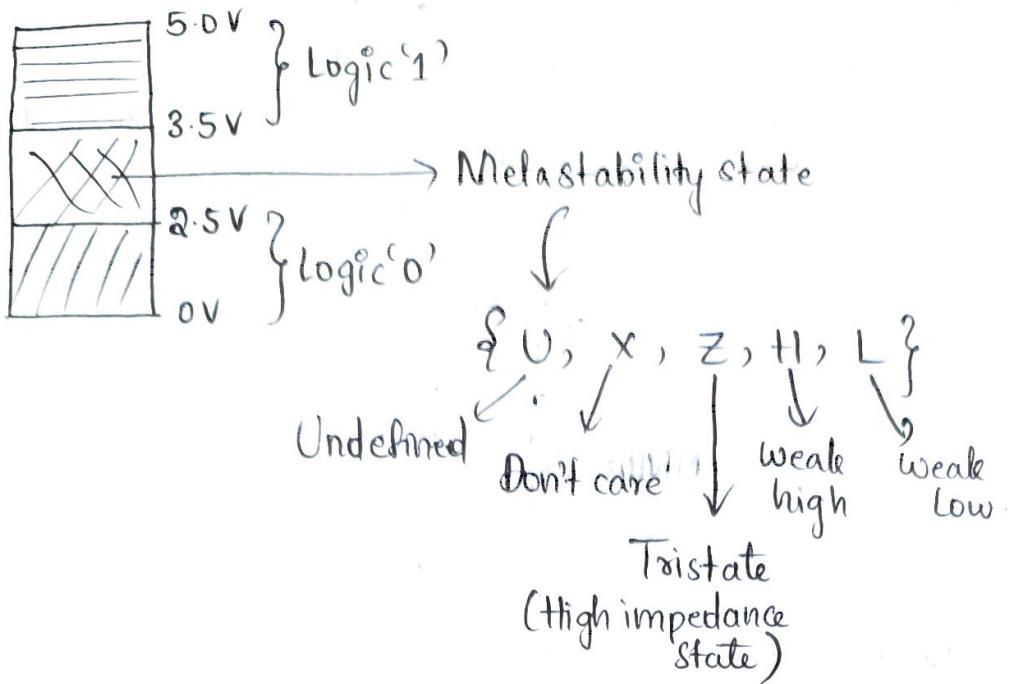
Case-(ii): $A = 1$



→ Capacitor gets discharged in this case and hence the output is logic '0'.

→ if we use Depletion PMOs then P1 is also 'ON' state and charging and discharging of capacitor is simultaneously observed.

→ So, we never use Depletion modes in MOSFETs.



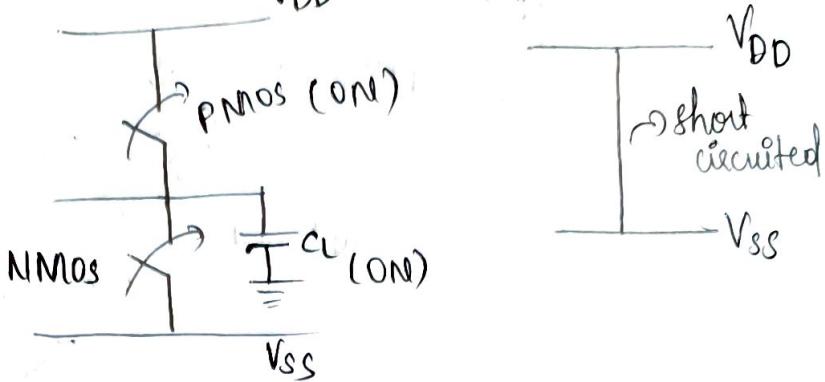
* CMOS Logic Implementation & Analysis:

- $P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}} + P_{\text{leakage}}$
 (power dissipation)
- leakage current doubles as the length of the channel decreases half.
 - static power (P_{static}) is observed when there is steady constant current supply (operates in one state)
 - In order to prevent leakage currents, substrate terminal is introduced.
 - Whenever there is transition from one state to another state continuously and the power observed in this case is dynamic power (P_{dynamic})

$A=0$ $A=1$
 PMOS ON \rightarrow OFF

NMOS OFF \rightarrow ON

→ Due to high switching speed of N-MOS there may be certain state in which both PMOS & NMOS will be 'ON' state while transitioning from $A=0$ to $A=1$ for a small period of time.

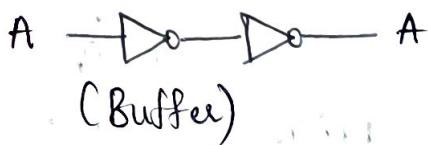
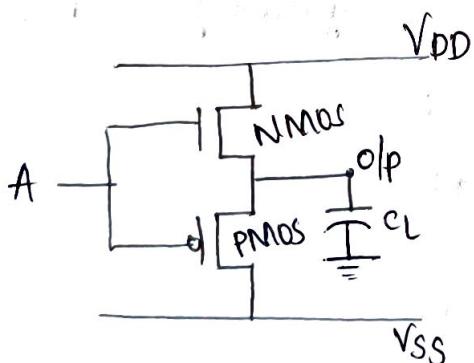


→ If we implement any logic using CMOS we get output in the complementary form.

→ Due to the difference in switching characteristics, capacitor charging and discharging doesn't happen desirably and hence inverter logic cannot be achieved.

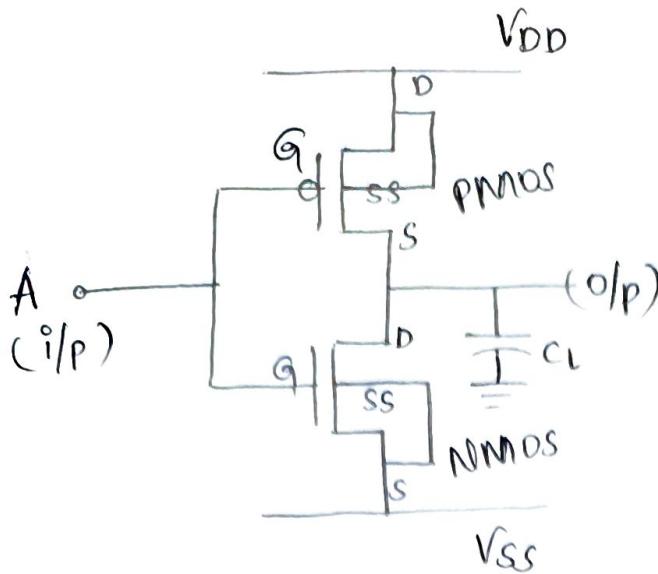
→ To avoid this we have to match the switching characteristics by changing the geometry of the transistor

$$\text{Aspect ratio (z)} = \frac{W}{L}$$



A	O/p
0	0
1	1

Whenever NMOS is connected in pull up region and PMOS is connected in pull down region, it acts as a buffer.



Body effects of substrate: As V_{GS} ↑ ↑ efficiency of substrate ↓ ↓.

- While fabrication, by proper doping concentration, we can avoid/control body effects
- By using substrate terminal, we can control body effects in the circuit and hence MOSFET is a 4-terminal device.
- In the above figure, PMOS substrate is connected to V_{DD} in pull up region and NMOS substrate is connected to V_{SS} in pull-down region and so overall ^{body} effect of the circuit is nullified.
- o/p of 1 circuit should be given to next circuit as the input, for this driver circuit is used.

CMOS + BJT \longrightarrow BiCMOS
 (Logic Design) (Driver circuit)

- In BJT high power dissipation happens

*) $f \rightarrow \text{CMOS} \rightarrow \bar{f}$

$a(b+c) \rightarrow \text{CMOS} \rightarrow \overline{\overline{a}(b+c)}$ \rightarrow ~~Do~~ $a(b+c)$

$f = a(b+c)$

(*) Not suggestible
 → because of delay
 → increasing no. of transistors
 → optimization is destroyed.

Demorgan's law,

$$\overline{a \cdot b} = \overline{a} + \overline{b}$$

$$\overline{a+b} = \overline{a} \cdot \overline{b}$$

→ Apply negation on both sides to regain originality

$$\begin{aligned} \bar{f} &= \overline{a(b+c)} \\ &= \overline{a} + \overline{(b+c)} \\ \boxed{\bar{f}} &= \overline{a} + \overline{b} \cdot \overline{c} \end{aligned}$$

*) Rule-1 :

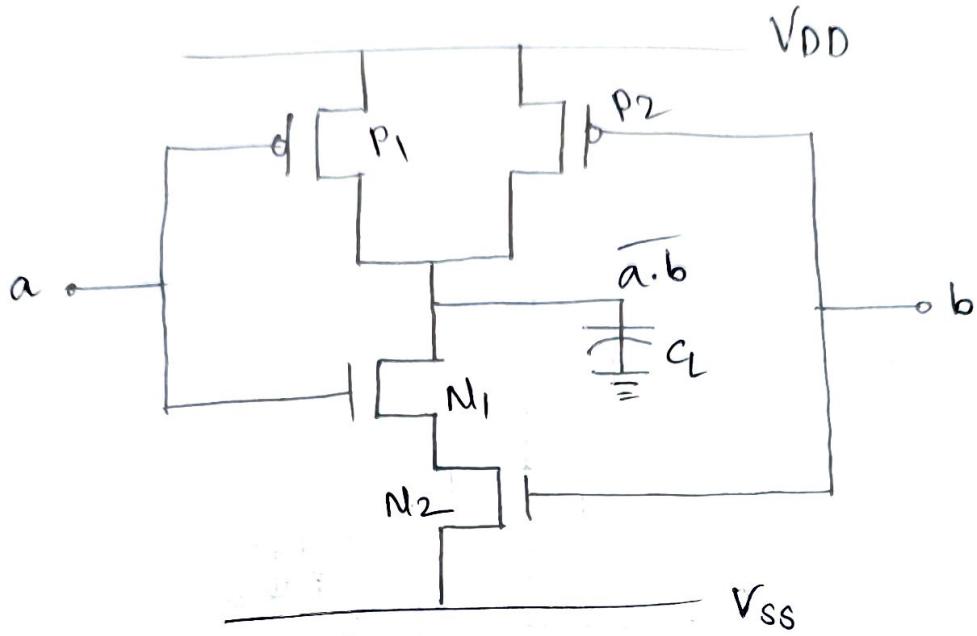
If in the given boolean function(expression), if variables are in product then PMOS transistors should be connected in parallel and NMOS transistors should be connected in series.

P - P - P

*) Rule-2 : (product - PMOS - parallel)

If in a given boolean expression, the variables are in summation then PMOS should be connected in series and NMOS should be connected in parallel.

→ Implement $f = \overline{a \cdot b}$ using CMOS logic.
 ↓
 complementary form
 $\bar{f} = a \cdot b$



a	b	$y = \overline{a \cdot b}$	i/p '0'	i/p '1'
0	0	1	PMOS	ON
0	1	1		OFF
1	0	1	NMOS	OFF
1	1	0		ON

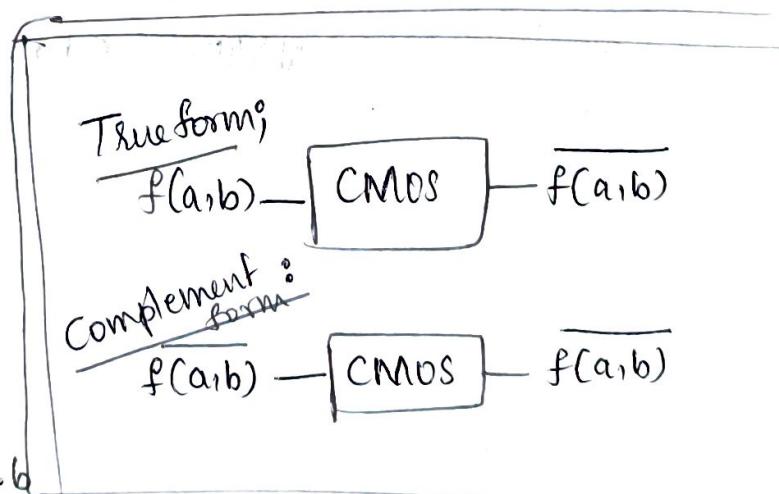
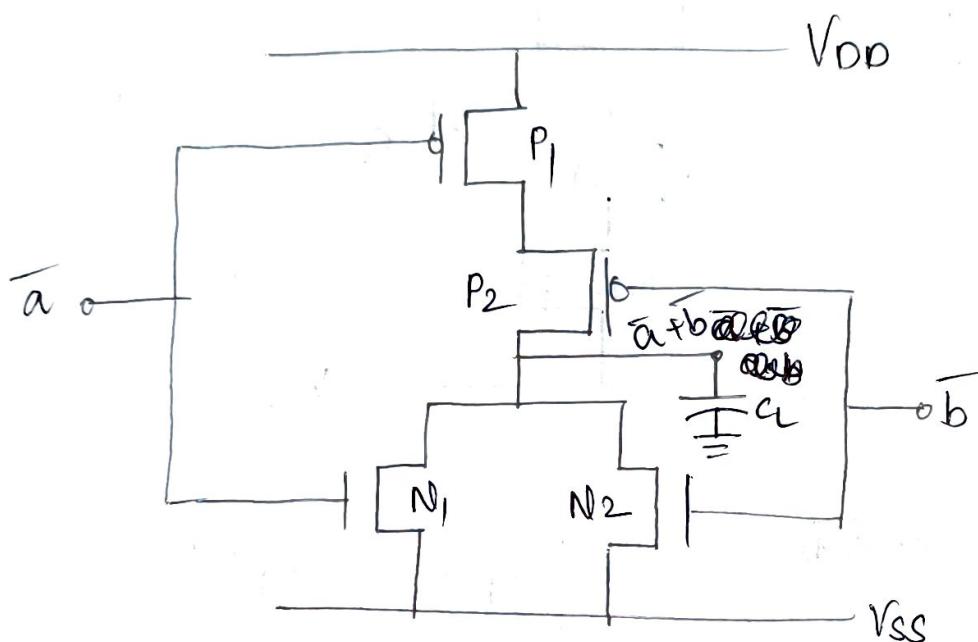
Q) Implement $f = a \cdot b$ using CMOS logic.

Sol:- $f = a \cdot b \rightarrow$ It is in true form,

Using De Morgan's law,

$$\overline{f} = \overline{a \cdot b}$$

$$\overline{f} = \overline{a} + \overline{b}$$



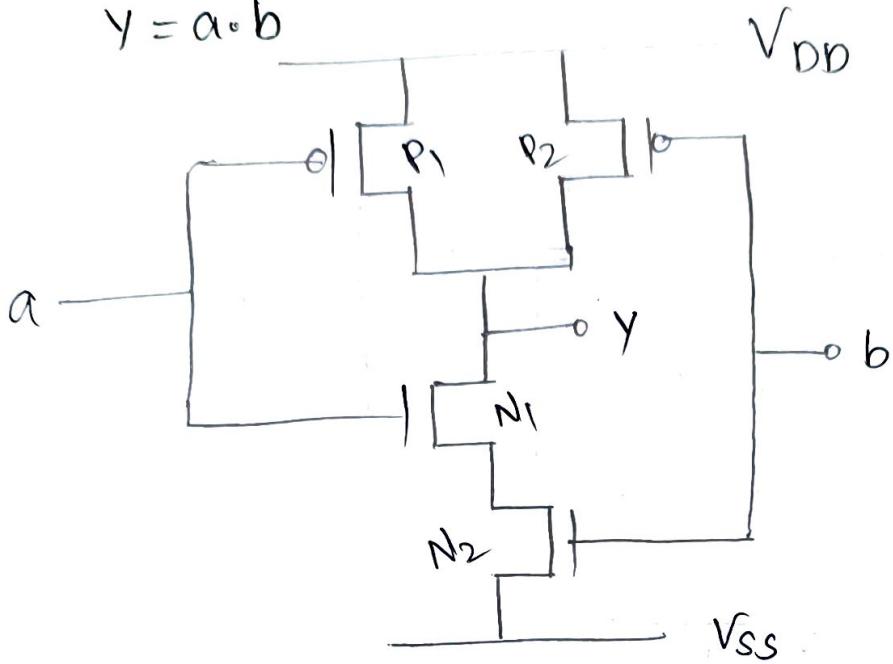
a	b	\bar{a}	\bar{b}	$y = a \cdot b$
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

* CMOS Logic Design :-

1) NAND gate

$y = \overline{a \cdot b} \rightarrow$ If it is in complemented form.

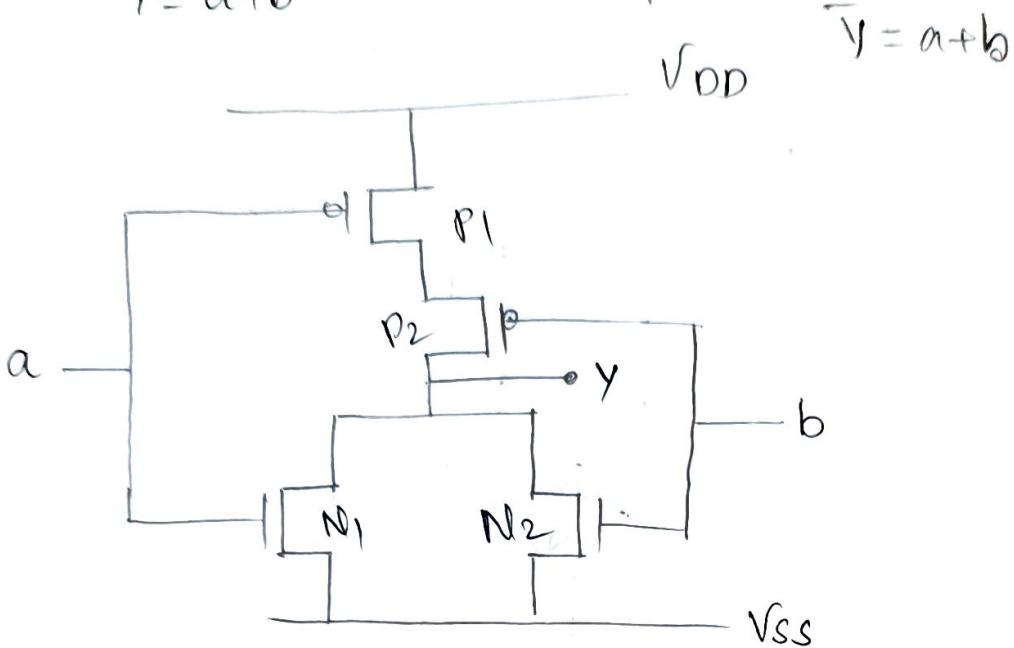
$$\overline{y} = a \cdot b$$



a	b	$y = \overline{a \cdot b}$
0	0	1
0	1	1
1	0	1
1	1	0

2) NOR gate:

$$Y = \overline{a+b} \rightarrow \text{It is in complemented form.}$$



a	b	$Y = \overline{a+b}$
0	0	1
0	1	0
1	0	0
1	1	0

OR gate:

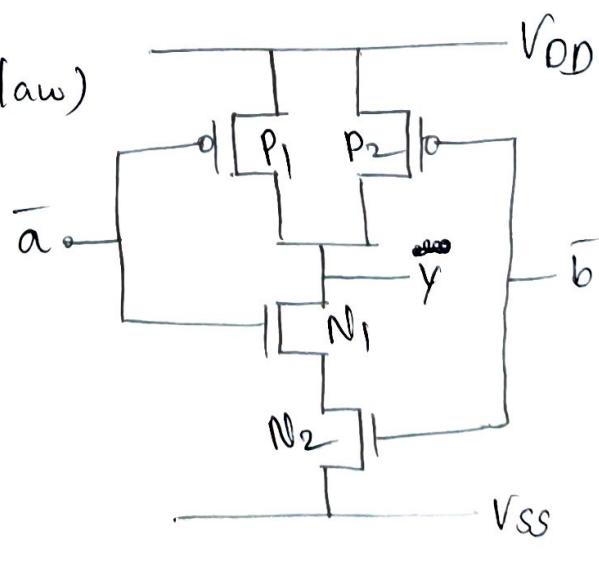
$$Y = a+b$$

Method-2: (DeMorgan's law)

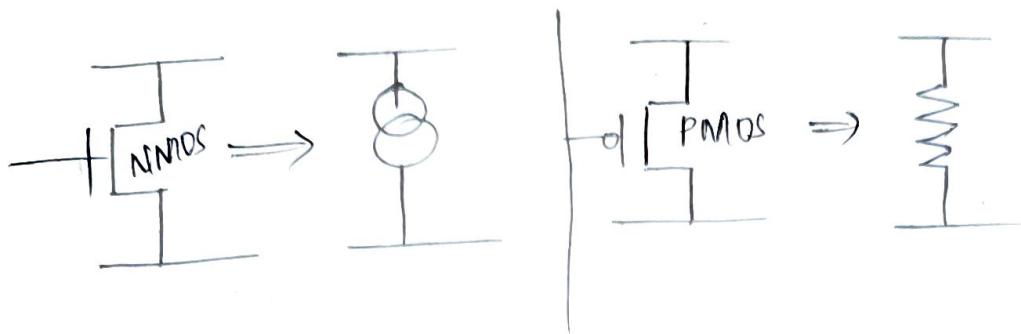
$$\bar{Y} = \overline{a+b}$$

$$\bar{Y} = \overline{a} \cdot \overline{b}$$

a	b	\bar{a}	\bar{b}	$Y = a+b$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	0



→ Mobility of NMOS is 2.5 times the mobility of PMOS
($\mu_n = 2.5 \mu_p$)



→ $T = RC$

In series Req \uparrow es \rightarrow so, $T \uparrow$ es.

In parallel Req \downarrow es \rightarrow so, $T \downarrow$ es.

(NAND technology is preferred over NOR technology because of high switching speed ($T \downarrow$ es))

→ NMOS has half the resistance of an equal sized PMOS.

$$\begin{pmatrix} \text{NMOS} - R \\ \text{PMOS} - 2R \end{pmatrix}$$

for NAND:

$$\begin{aligned} \text{Pullup resistance} &= 2R \parallel 2R = R \\ \text{Pulldown resistance} &= R + R = 2R \end{aligned} \quad \left. \right\} 3R$$

for NOR:

$$\begin{aligned} \text{Pullup resistance} &= 2R + 2R = 4R \\ \text{Pulldown resistance} &= R \parallel R = R/2 \end{aligned} \quad \left. \right\} \frac{9R}{2}$$

3) XOR gate

$$Y = a\bar{b} + \bar{a}b$$

$$Y = (\bar{a}b)(a\bar{b}) \rightarrow \text{It is in true form.}$$

Product terms should be connected in parallel.

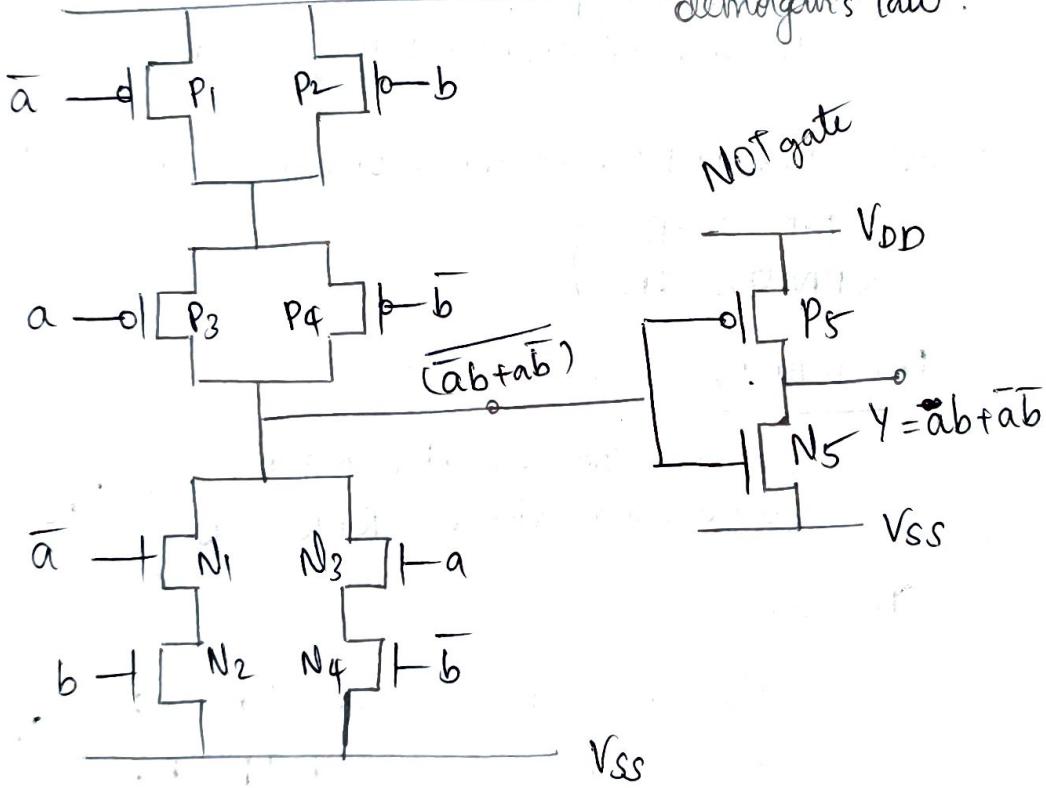
Pullup region

We have to connect the two product terms in series. (since it is in summation)

Pulldown region is quite opposite of pullup region.

Method-1: Applying NOT gate to the output

Method-2: Complement the function & then apply CMOS logic using DeMorgan's law.

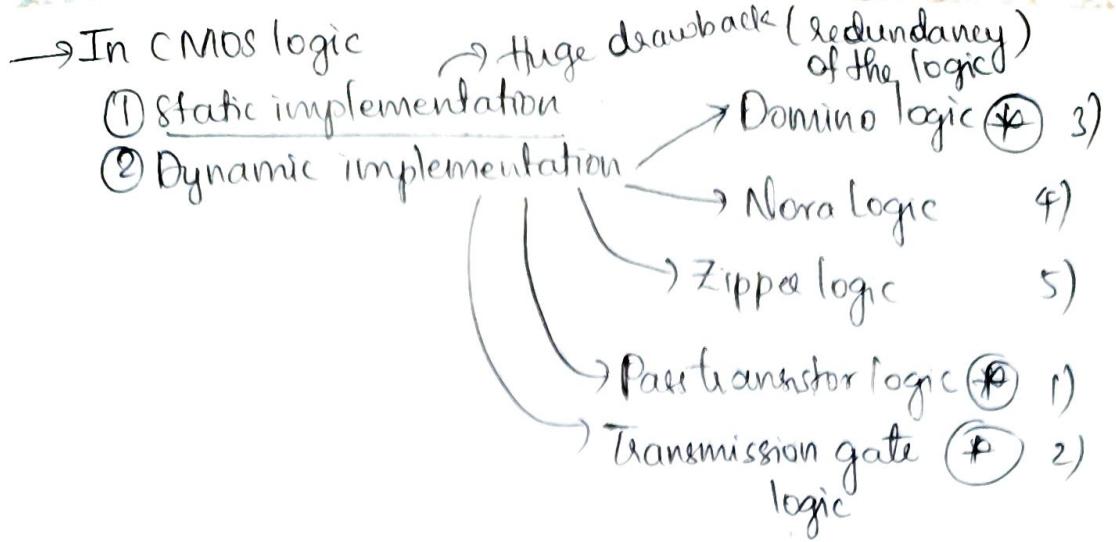


$$(\overline{\bar{a}b + a\bar{b}}) = \overline{\bar{a}\bar{b}} \cdot \overline{a\bar{b}}$$

$$= (\bar{a} + \bar{b}) \cdot (\bar{a} + b)$$

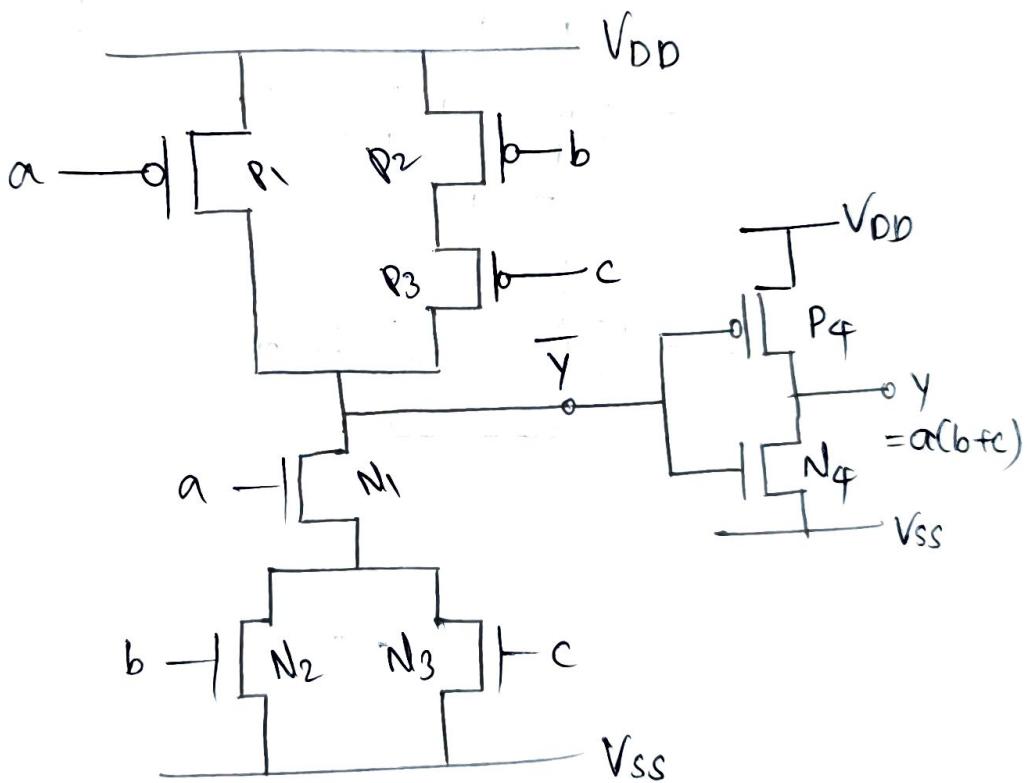
$$= \cancel{a}\cancel{a} + \cancel{a} \cdot b + \bar{a}\bar{b} + b\bar{b}$$

$$= a\bar{b} + \bar{a}b$$

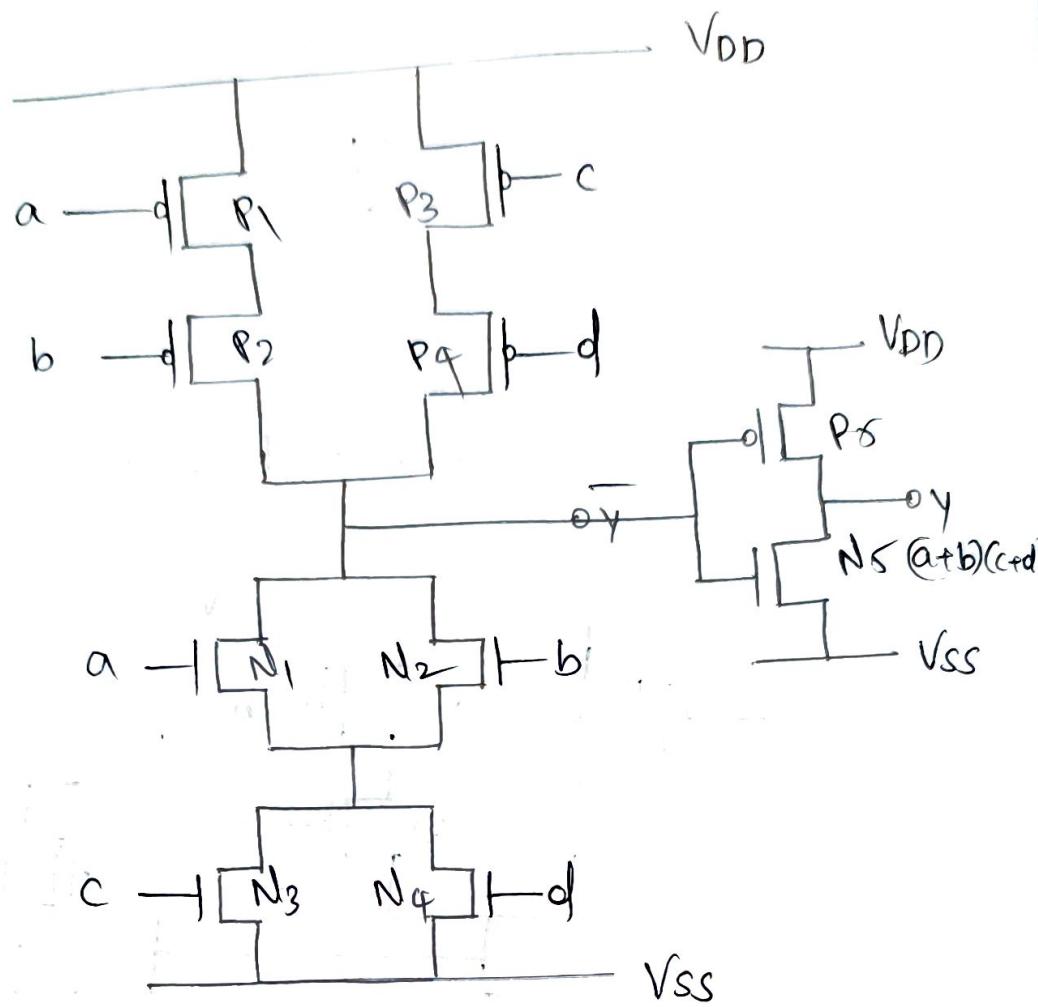


e.g: Implement the CMOS logic for

$$Y = a \cdot (b + c) \rightarrow \text{It is in true form}$$



e.g. Implement CMOS logic for
 $y = (a+b) \cdot (c+d)$ → It is in true form



$$\text{eg: } ① Y = a \cdot b \cdot c \cdot d$$

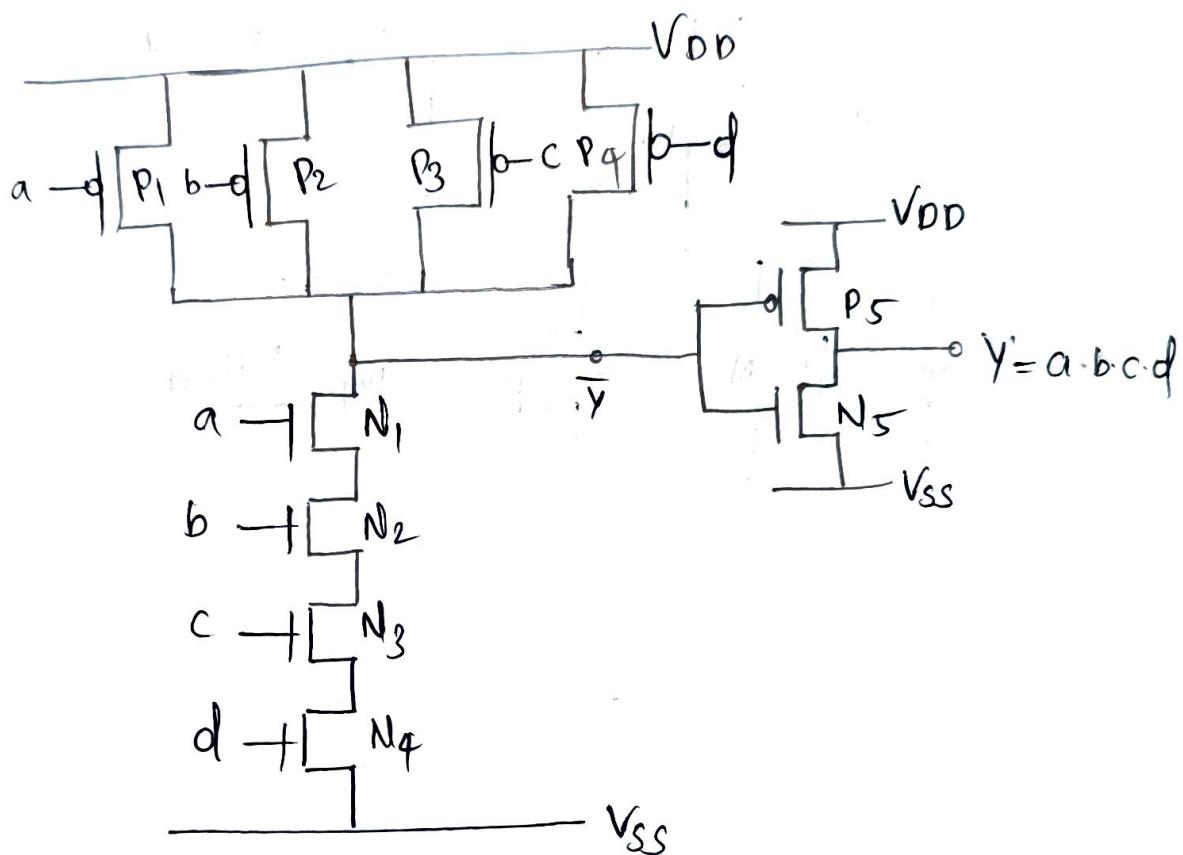
$$② Y = \overline{\overline{a} + b + c + d}$$

$$③ Y = \overline{a} \cdot b \cdot (c + \overline{d})$$

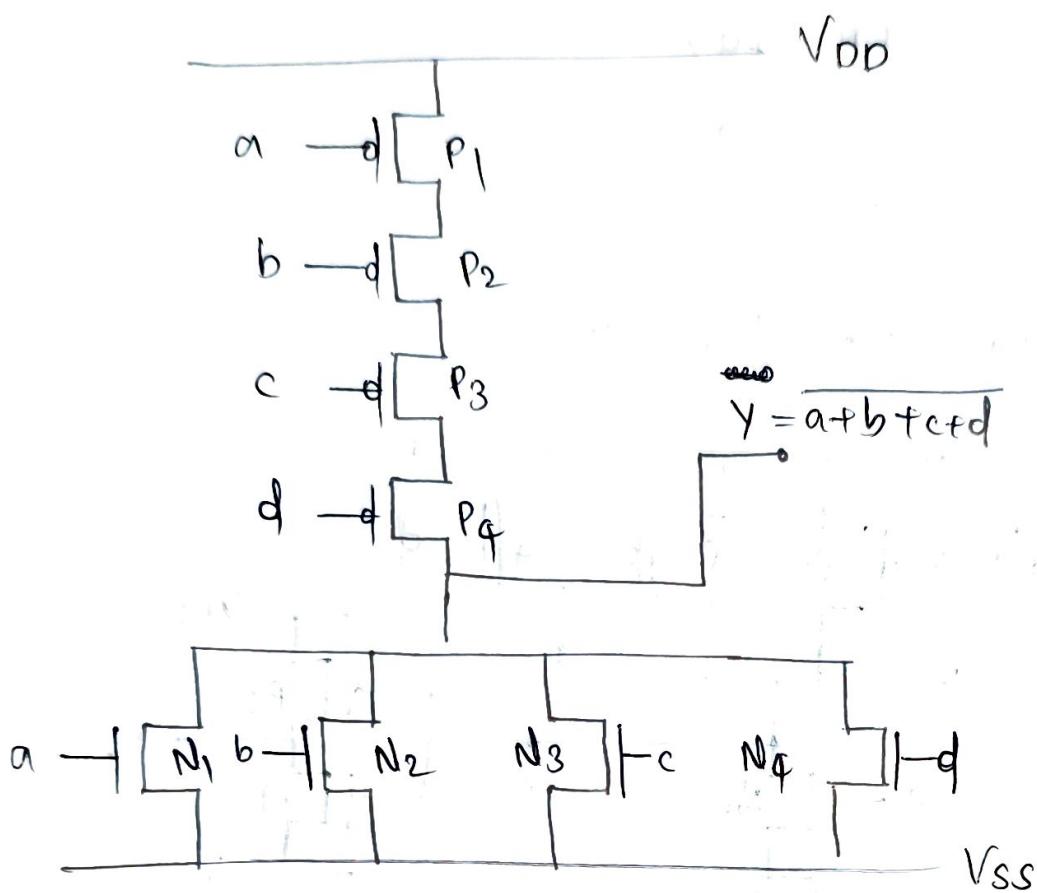
$$④ Y = \overline{\overline{a} \cdot \overline{b} \cdot \overline{c} \cdot \overline{d}}$$

$$⑤ Y = \overline{a} \overline{b} + ab$$

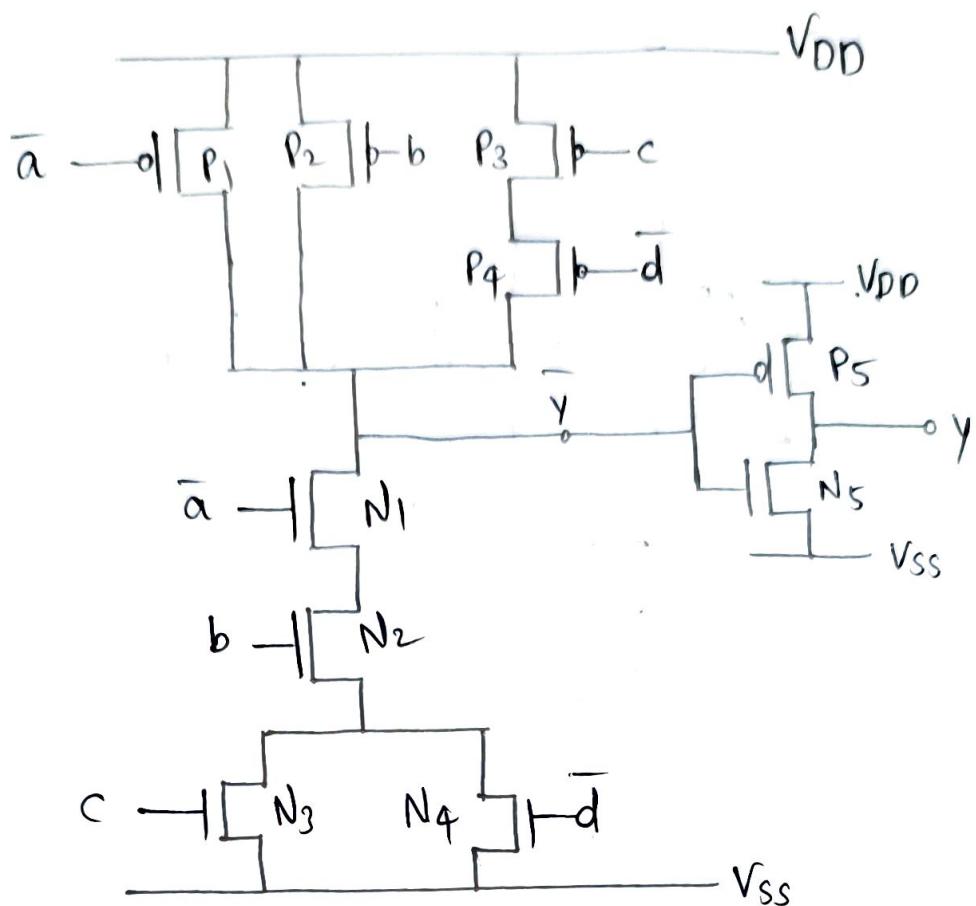
① $Y = a \cdot b \cdot c \cdot d \rightarrow$ It is in true form.



2) $y = \overline{a+b+c+d} \rightarrow$ It is in complement form.

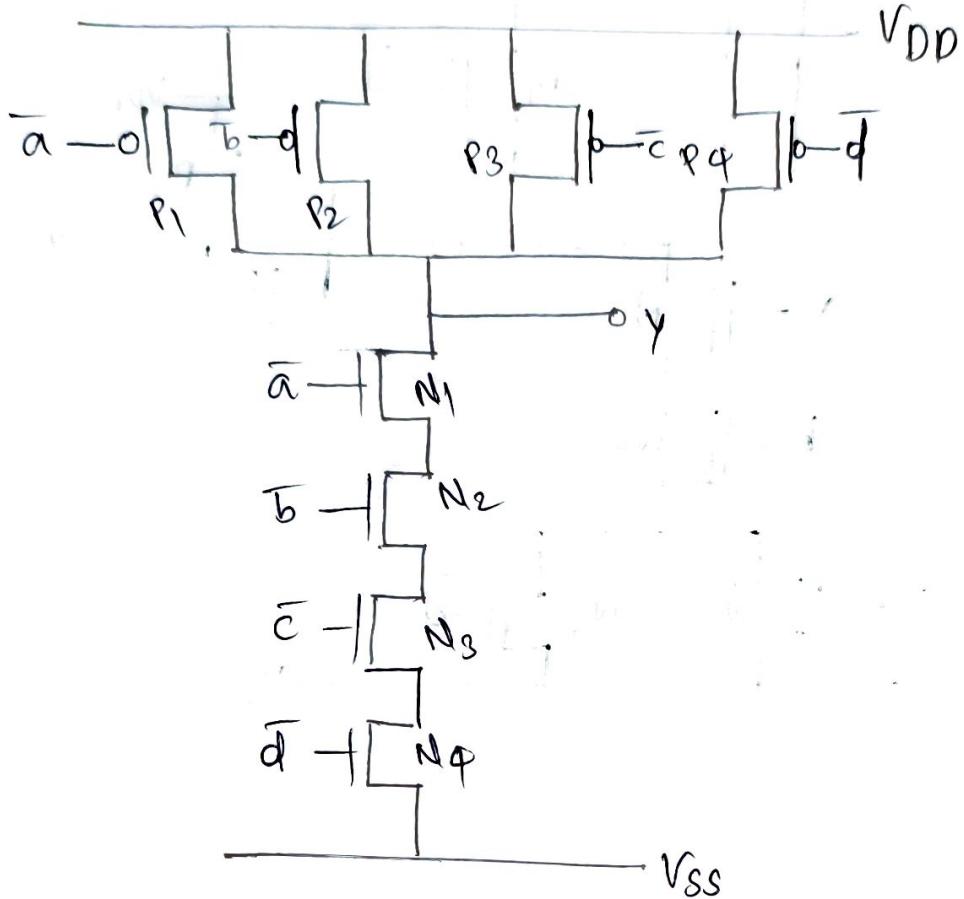


$$3) Y = \overline{ab}(c + \overline{d})$$

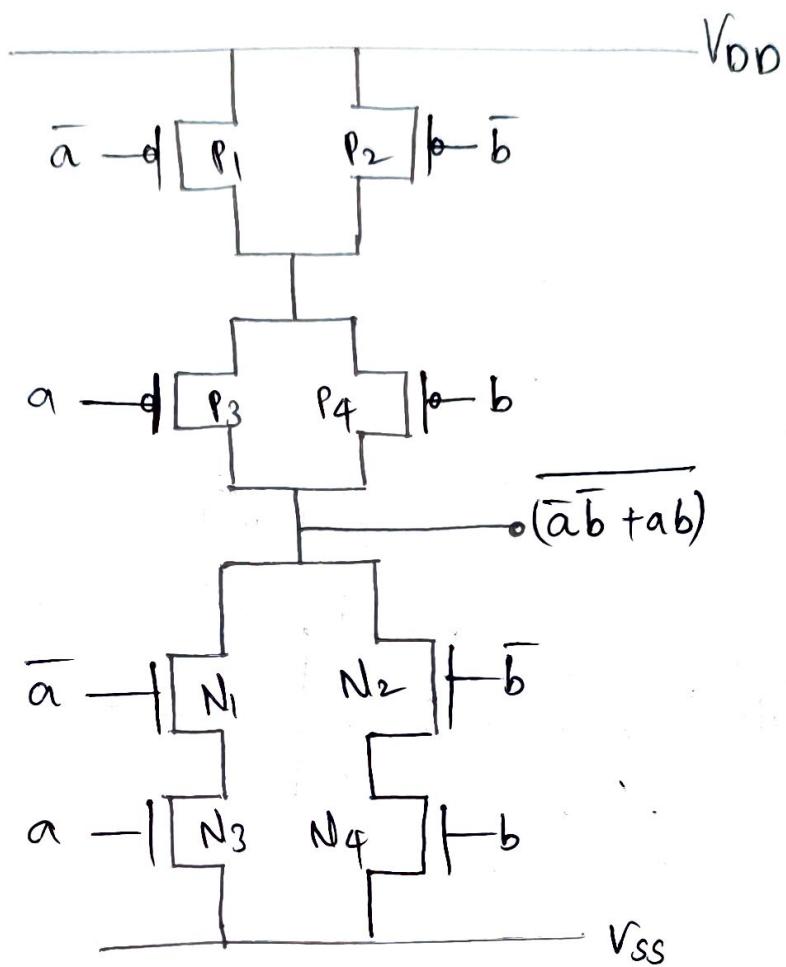


$$4) Y = \overline{\overline{a} \cdot \overline{b} \cdot \overline{c} \cdot \overline{d}} \rightarrow \text{It is in true form.}$$

$$\overline{Y} = \overline{\overline{a} \cdot \overline{b} \cdot \overline{c} \cdot \overline{d}}$$



5) $Y = \bar{a}\bar{b} + ab \rightarrow$ It is complemented form
of NOR gate



* MOS Transistor fabrication:

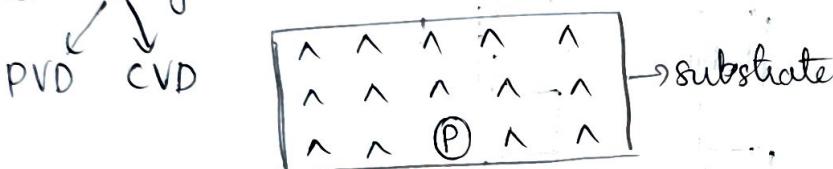
- ① nMOS fabrication
- ② pMOS fabrication
- ③ CMOS fabrication

→ n-well process
→ p-well process
→ Twin-tub process.

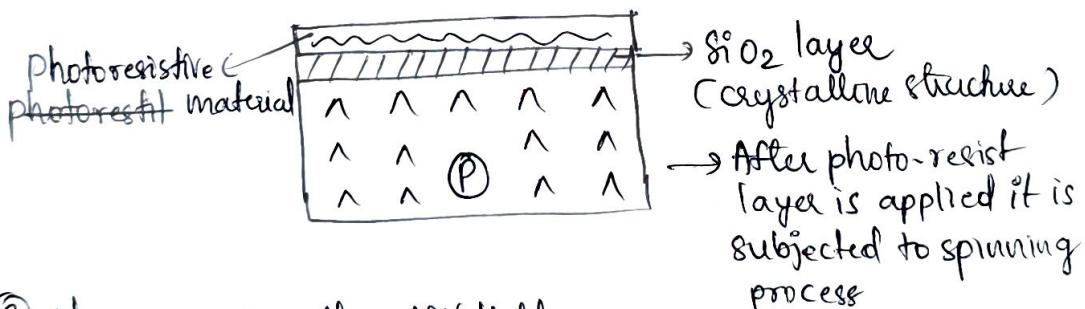
① NMOS fabrication process:

→ Silicon basic planar process (Refer)

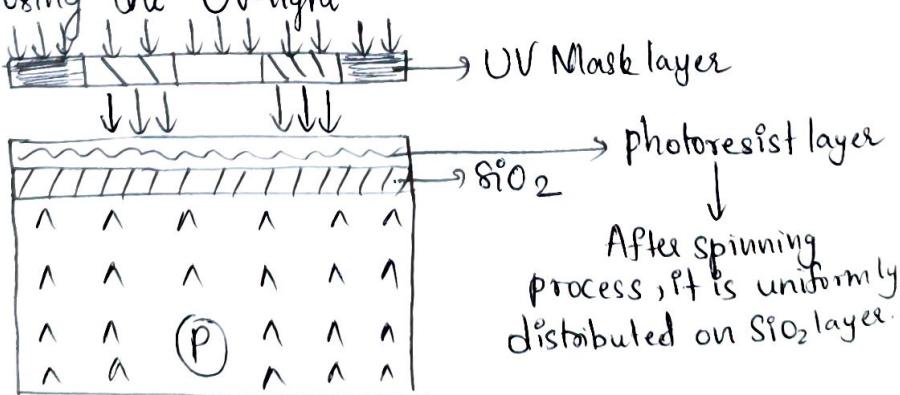
- ① Doping the substrate with p-type impurities.



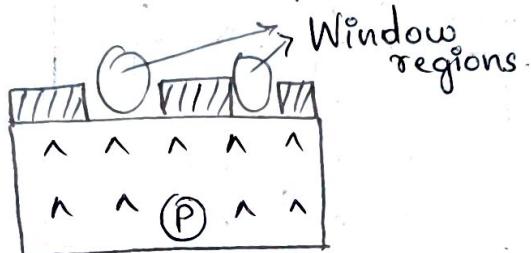
- ② SiO_2 layer is grown over the surface of the substrate.



- ③ Now exposing the UV-light

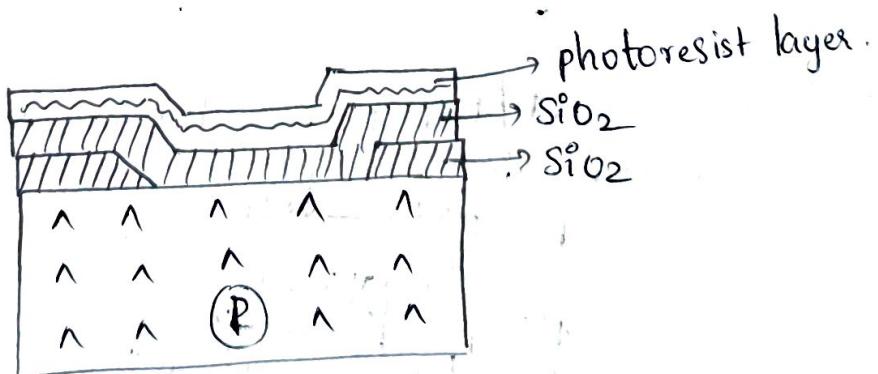


- UV rays are exposed through UV mask layer
- Inorder to create window regions for Source & Drain p-type substrate was exposed to the UV rays through UV mask layer
- Once UV rays was exposed at the defined window regions SiO_2 layer becomes very hard, then it has been etched off. This complete phenomenon is called photo lithography process.
- photoresist material is used as SiO_2 properties may change if direct exposure of UV-rays.

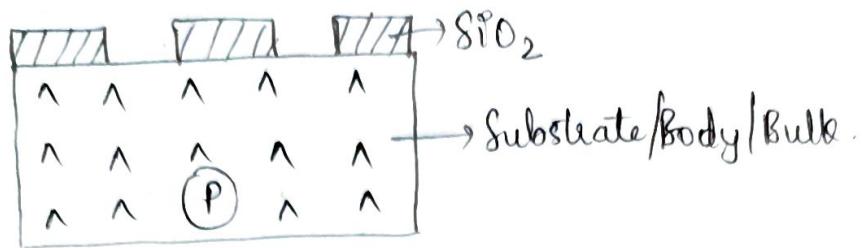


④ Again a SiO_2 layer is deposited, again photoresist layer is deposited and is exposed to UV rays via UV mask layer and gate terminal is achieved.

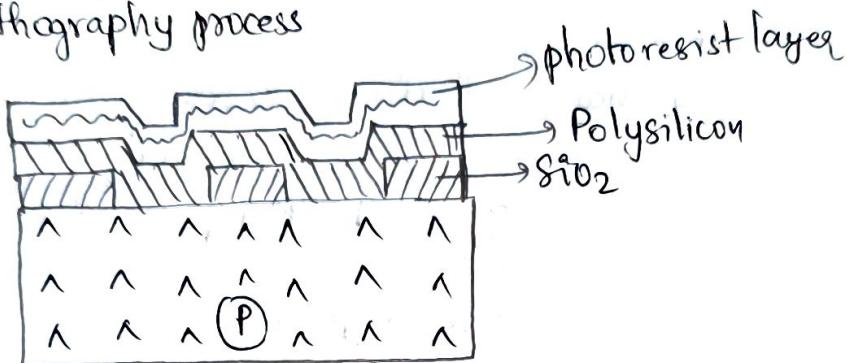
- Inorder to achieve/define gate terminal, it is again processed through photolithographic process.



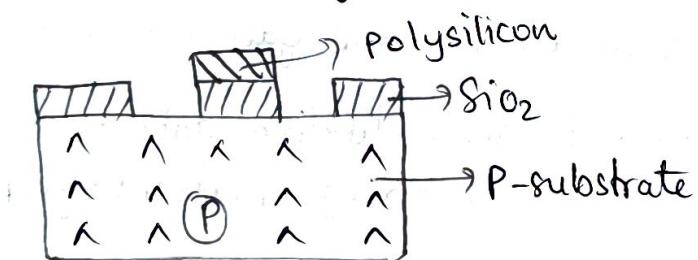
⑤



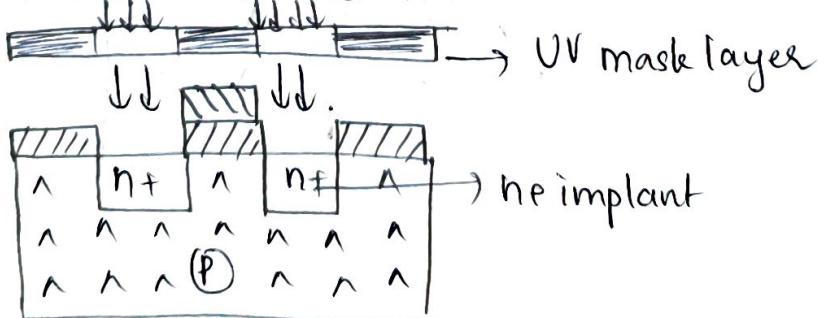
⑥ Polysilicon is deposited and is subjected to photolithography process



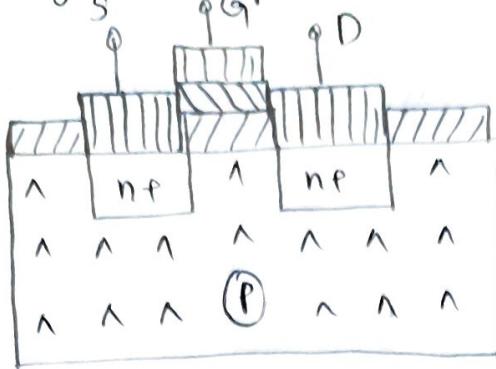
⑦ polysilicon is deposited only on gate terminal.



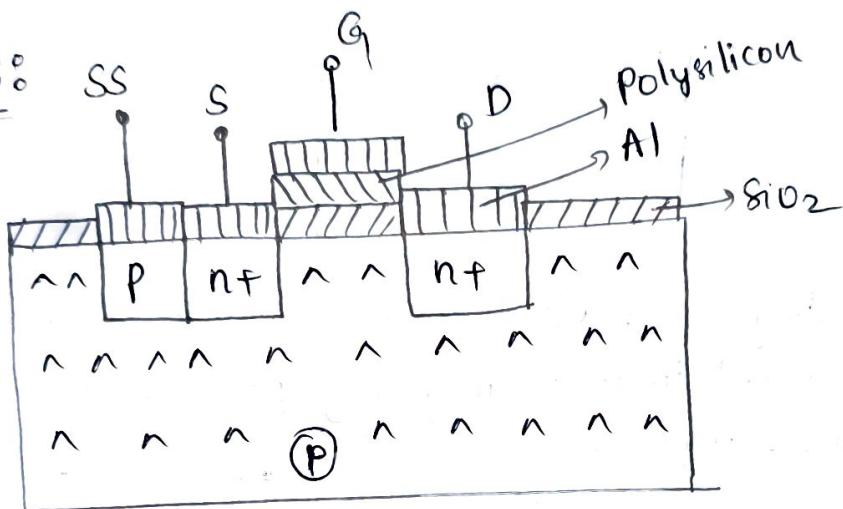
⑧ Through CVD/PVD process $n+$ implants are induced into the substrate



⑨ Aluminium layer is deposited over the layer.

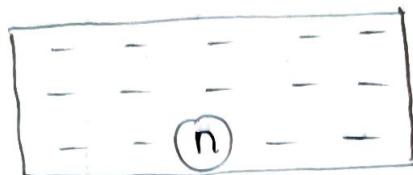


N-MOS

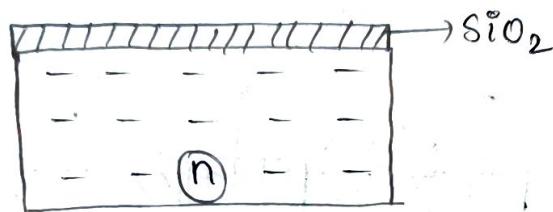


② PMOS fabrication:

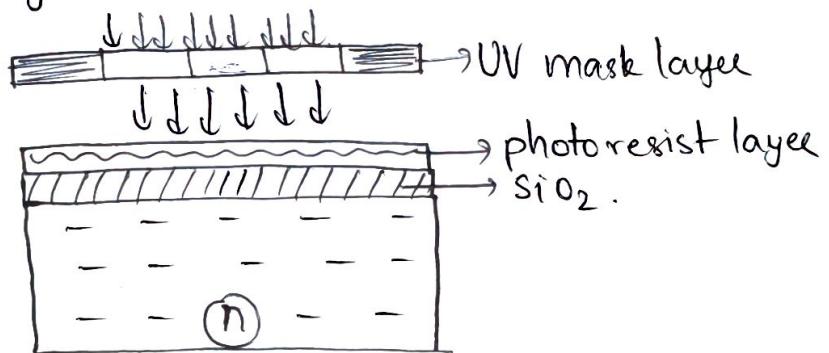
1) Doping the substrate with n-type impurities



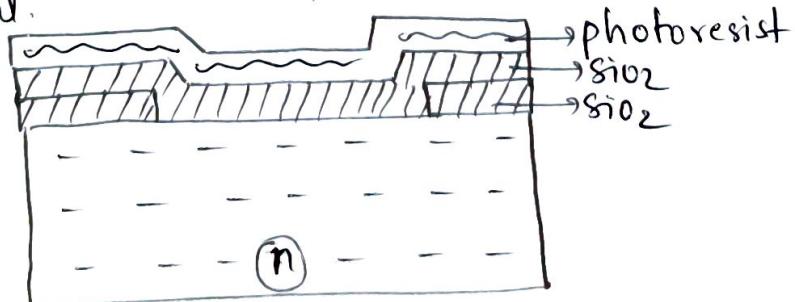
2) SiO_2 layer is grown over the surface of substrate



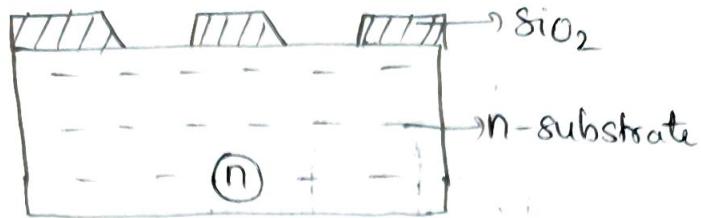
3) Depositing the photoresist layer on SiO_2 and is subjected to photolithography process to create window regions.



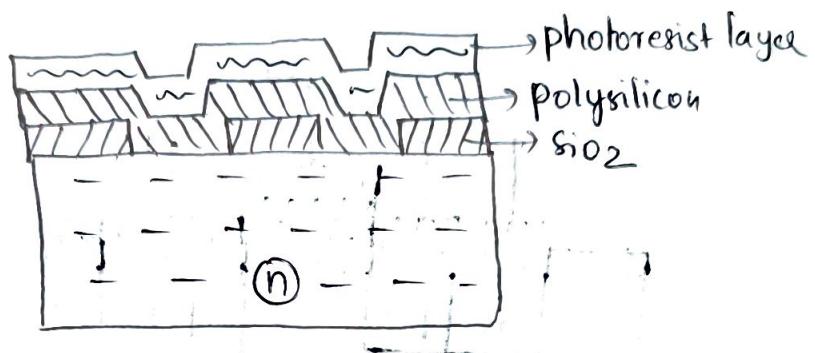
4) Again an SiO_2 layer is deposited and photoresist layer is deposited over it and is exposed to UV rays via UV masblayer so as to create gate terminal.



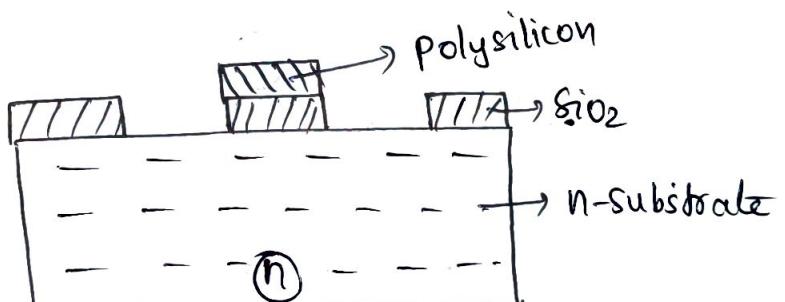
5)



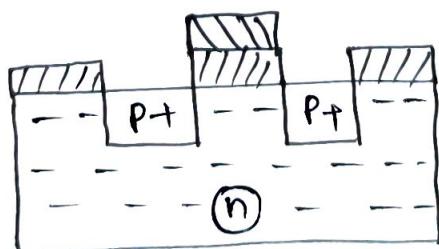
6) polysilicon is deposited and is subjected to photolithography process.



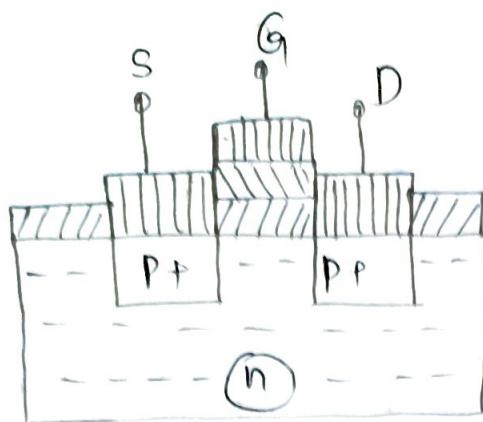
7) polysilicon is deposited only on gate terminal.



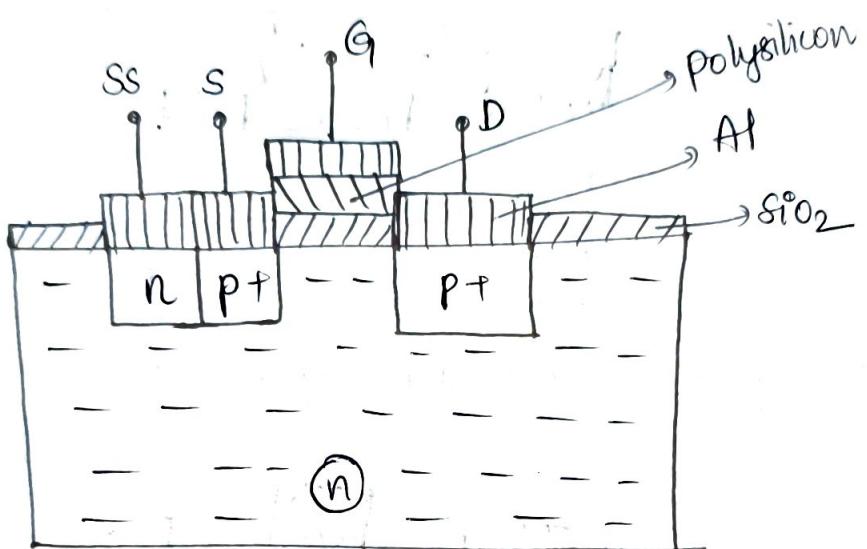
8) Through CVD/PVD process p+ implants are induced into the substrate



9) Aluminium layer is deposited over the layer



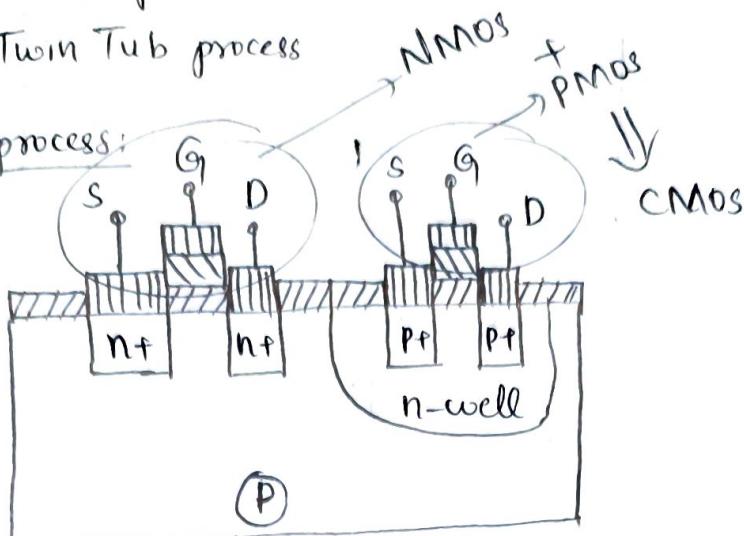
PMOS:



③ CMOS fabrication process:

- n-well process
- p-well process
- Twin-Tub process

(i) n-well process:



→ Latch-up problem occurs in n-well process because of virtual formation of BJTs (NPN & PNP).

→ Output of one transistor is connected to input of another transistor, due to this current is generated internally and may achieve saturation state, this current will escape if at all there are any cracks in the SiO_2 .

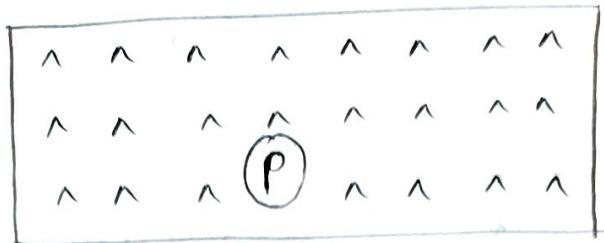
→ To correct Latch-up problem, Twin-Tub process is introduced in which 75% of substrate is covered with epitaxial layer which isolates the transistors (wells)

SiO_2 layers → thin layer (0.1 μm)
→ thick layer (10 μm)

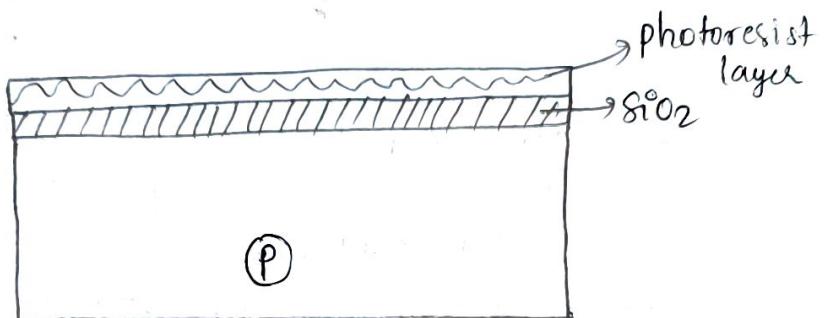
Polysilicon → polysilicon 1 (red colour)
→ polysilicon 2 (orange colour)

λ -rule
 μ -rule

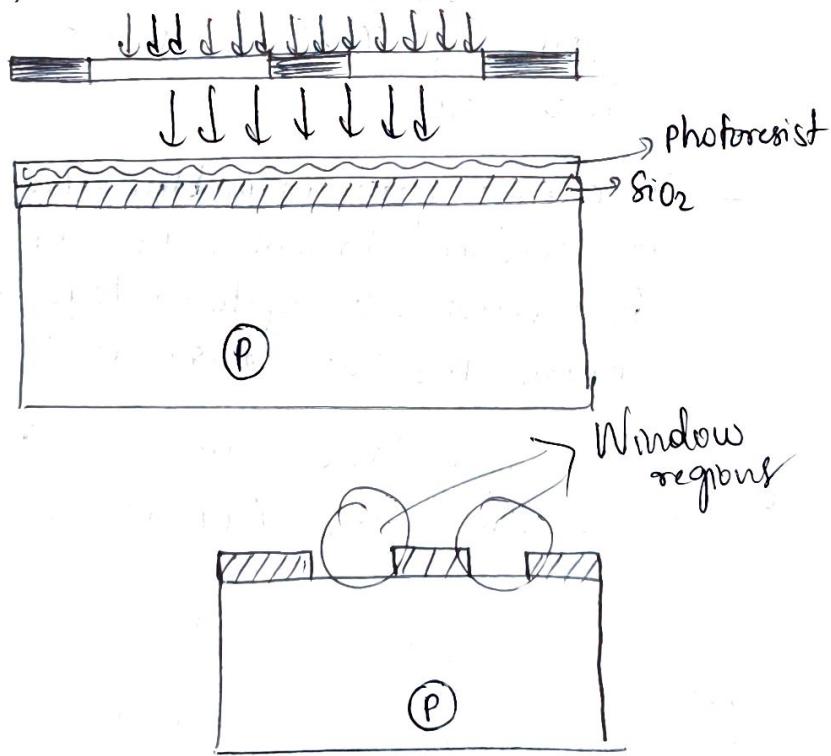
i) Doping the substrate with p-type impurities



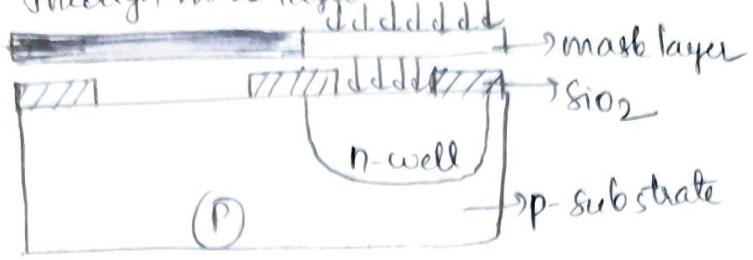
2) SiO_2 layer is grown over the substrate and photoresist layer is applied over it and is subjected to spinning process.



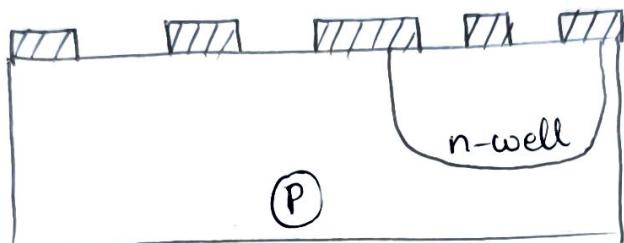
3) Through photolithography process window regions are created.



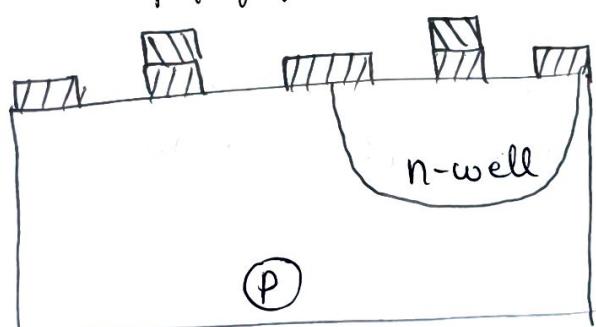
4) Using CVD/PVD process, n-well is deployed into the substrate through mask layer



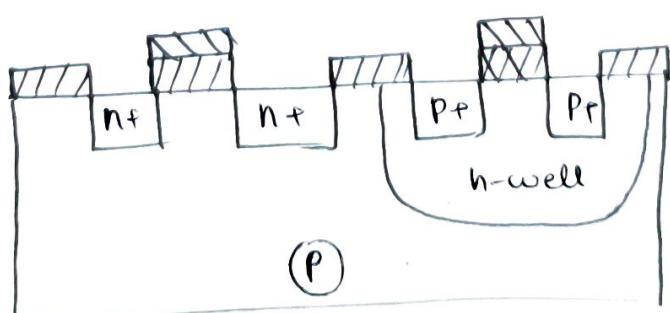
5) SiO₂ layer is grown over it and using photolithography process create gate terminal regions.



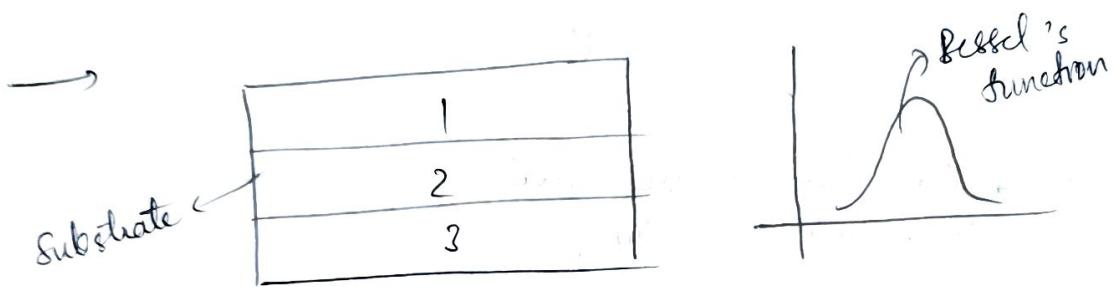
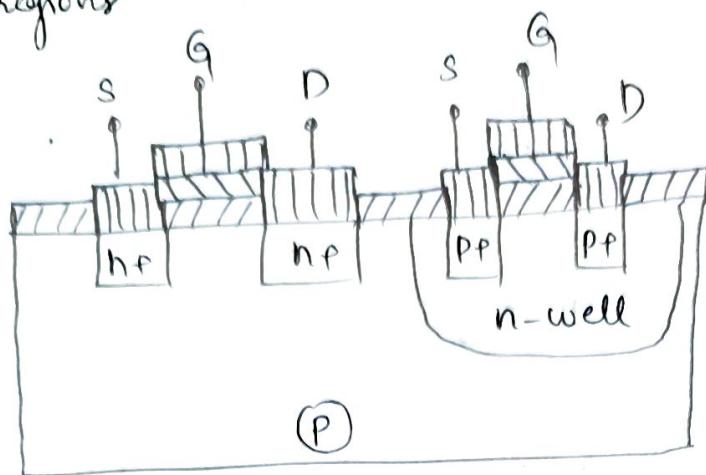
6) Polysilicon layer is deposited on gate terminals using photolithography process.



7) Using CVD/PVD process n+ implants and p+ implants are deployed into respective regions.



8) Aluminium layer is deposited at last and using photolithography process, Al layer is created over terminal regions



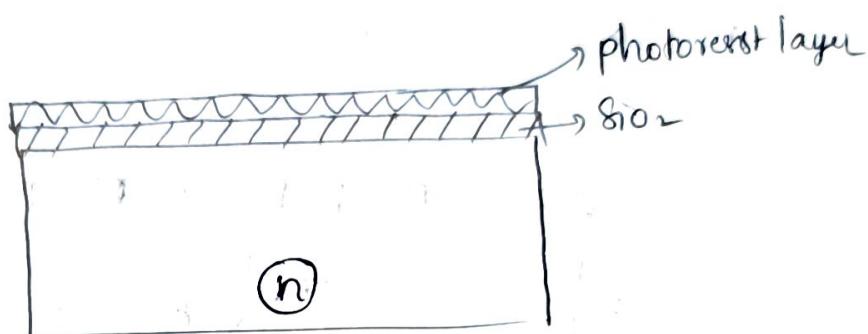
Doping of a substrate is done in such a way that graph of it looks like a bessel function

(ii) p-well process:

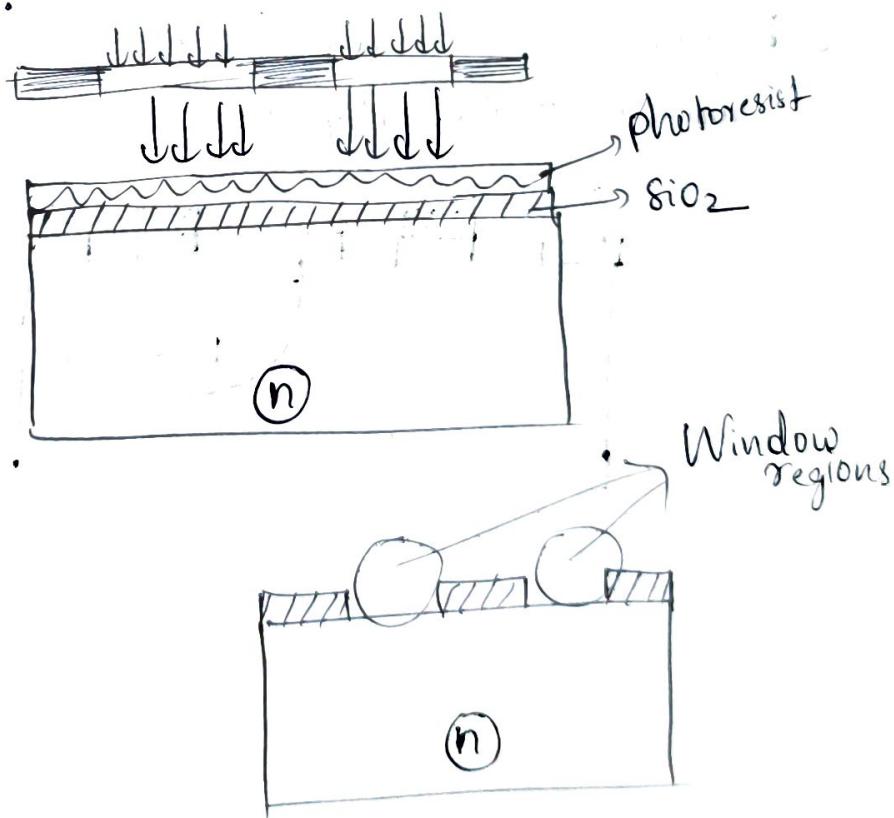
- Doping the substrate with n-type impurities.



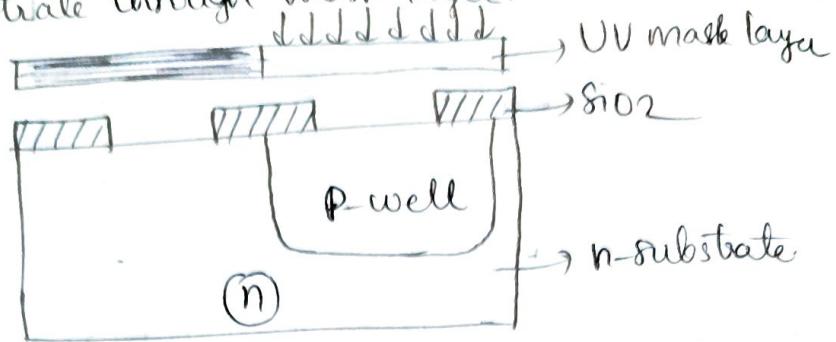
- SiO₂ layer is grown over the substrate and photoresist layer is applied over it and is subjected to spinning process.



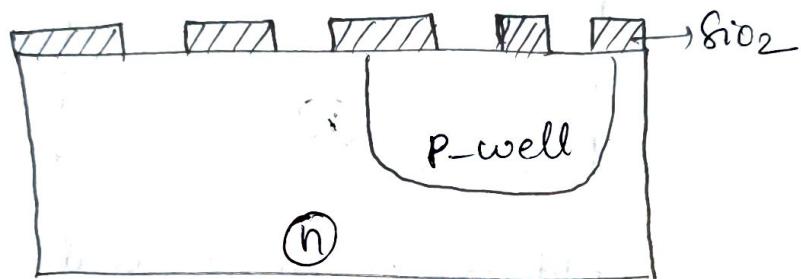
- Through photolithography process, window regions are created.



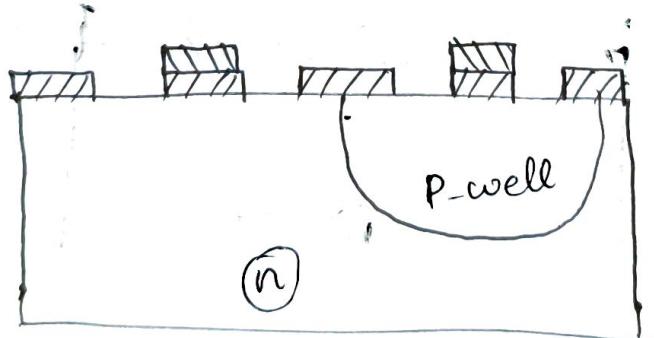
4) Using CVD/PVD process, p-well is deployed into the substrate through mask layer.



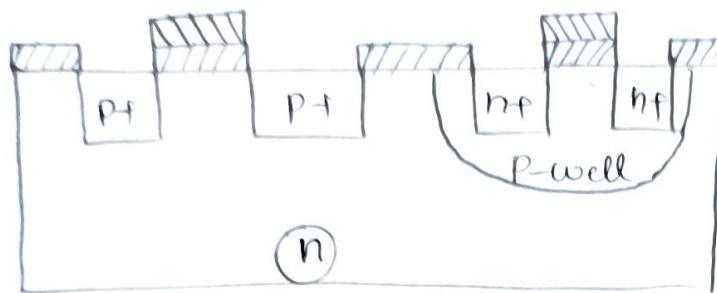
5) SiO₂ layer is grown over it and using photolithography process create gate terminals.



6) Polysilicon layer is deposited on gate terminals using photolithography process.



7) Using CVD/PVD process, p+ implants and n+ implants are deployed into respective regions.



8) Aluminium layer is deposited at last and using photolithography process, Al layer is created over terminal regions.

