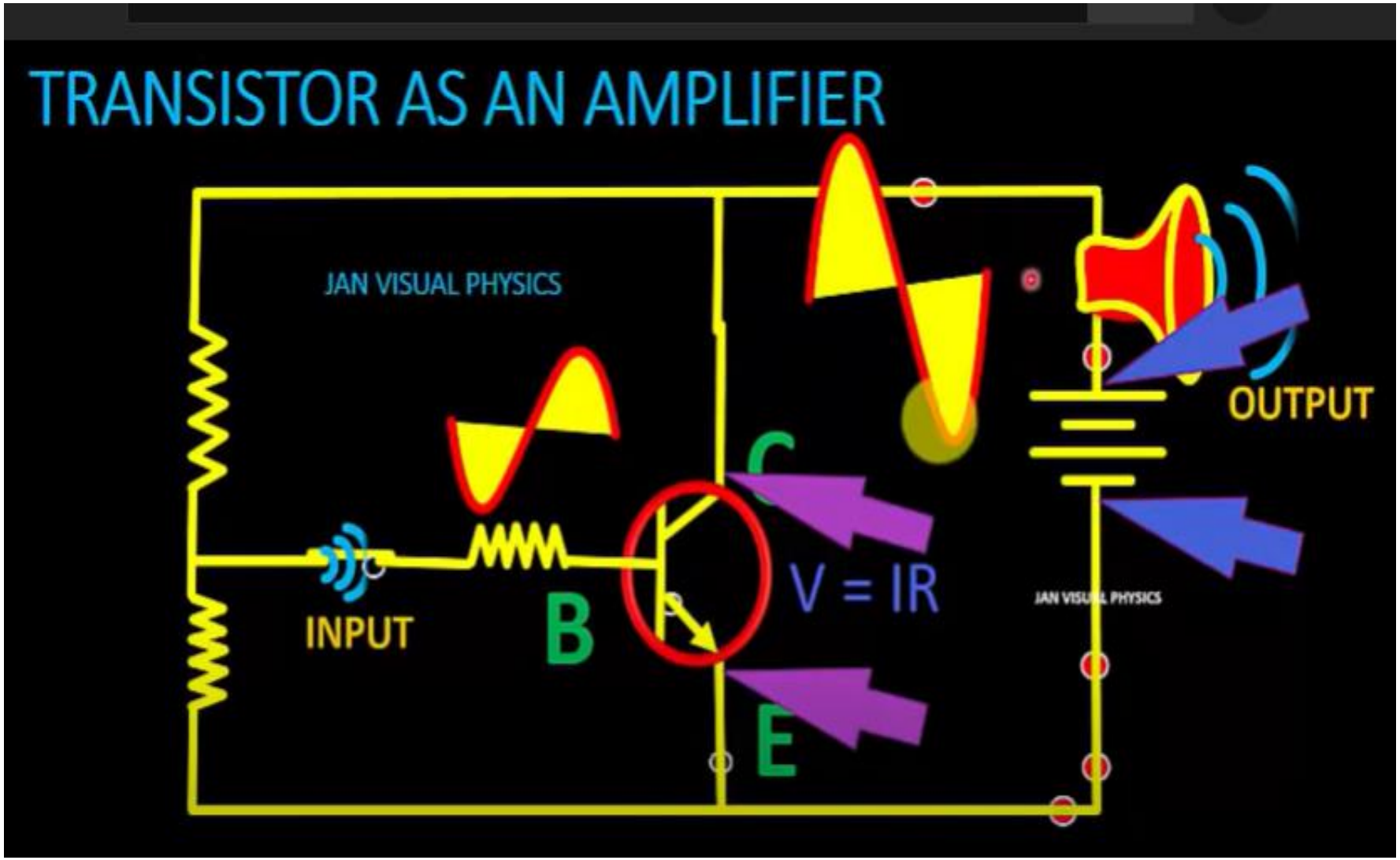
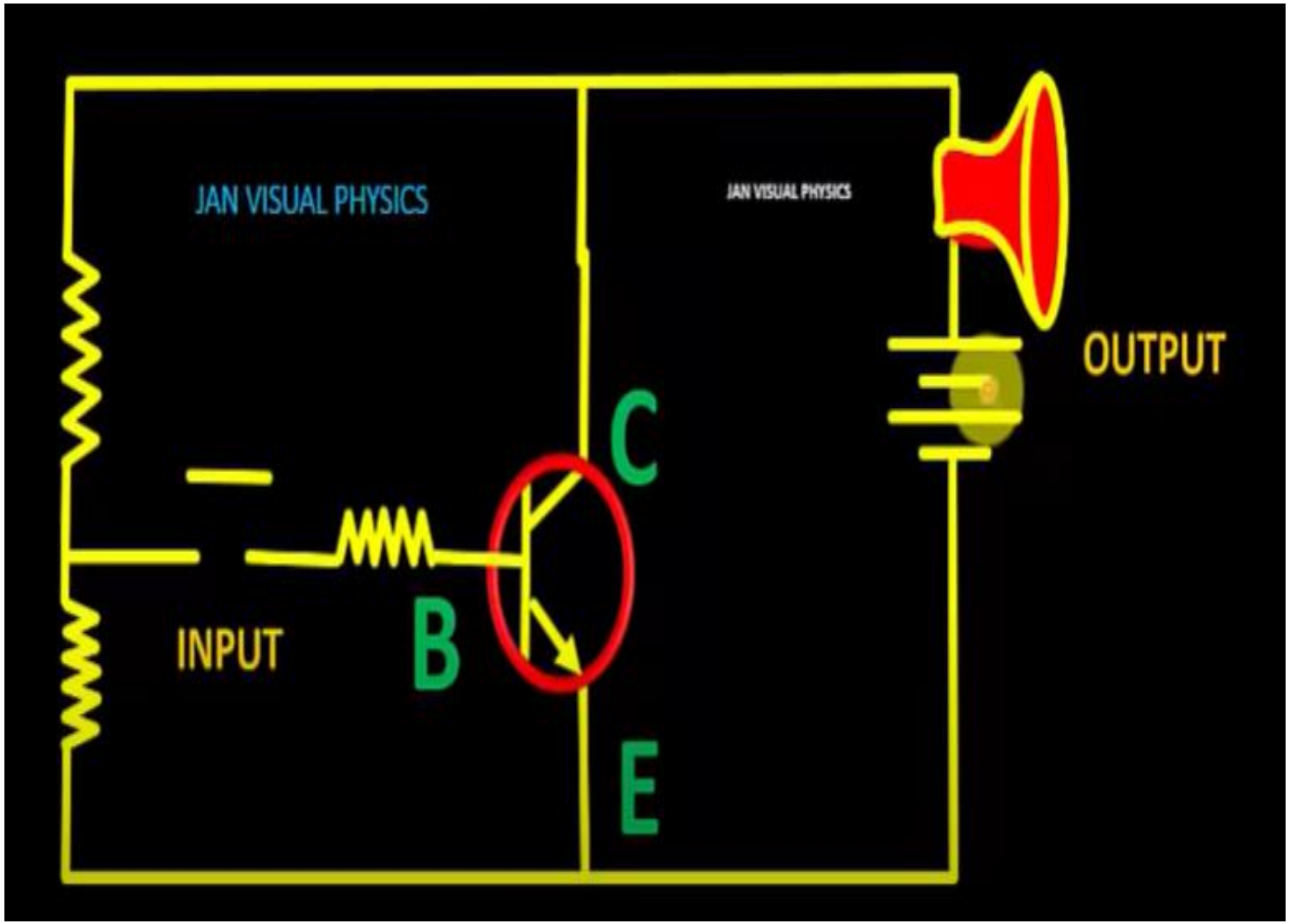
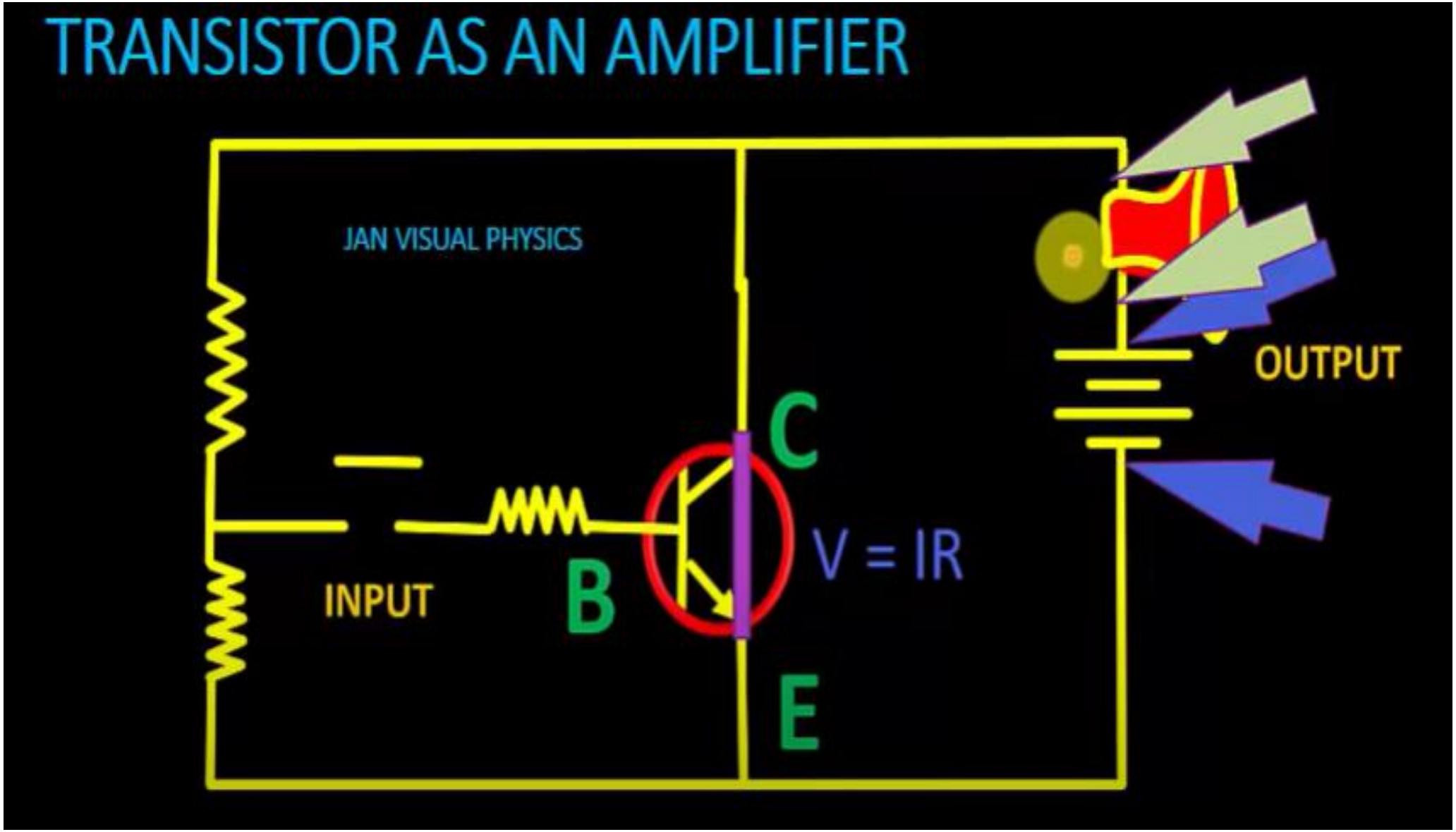
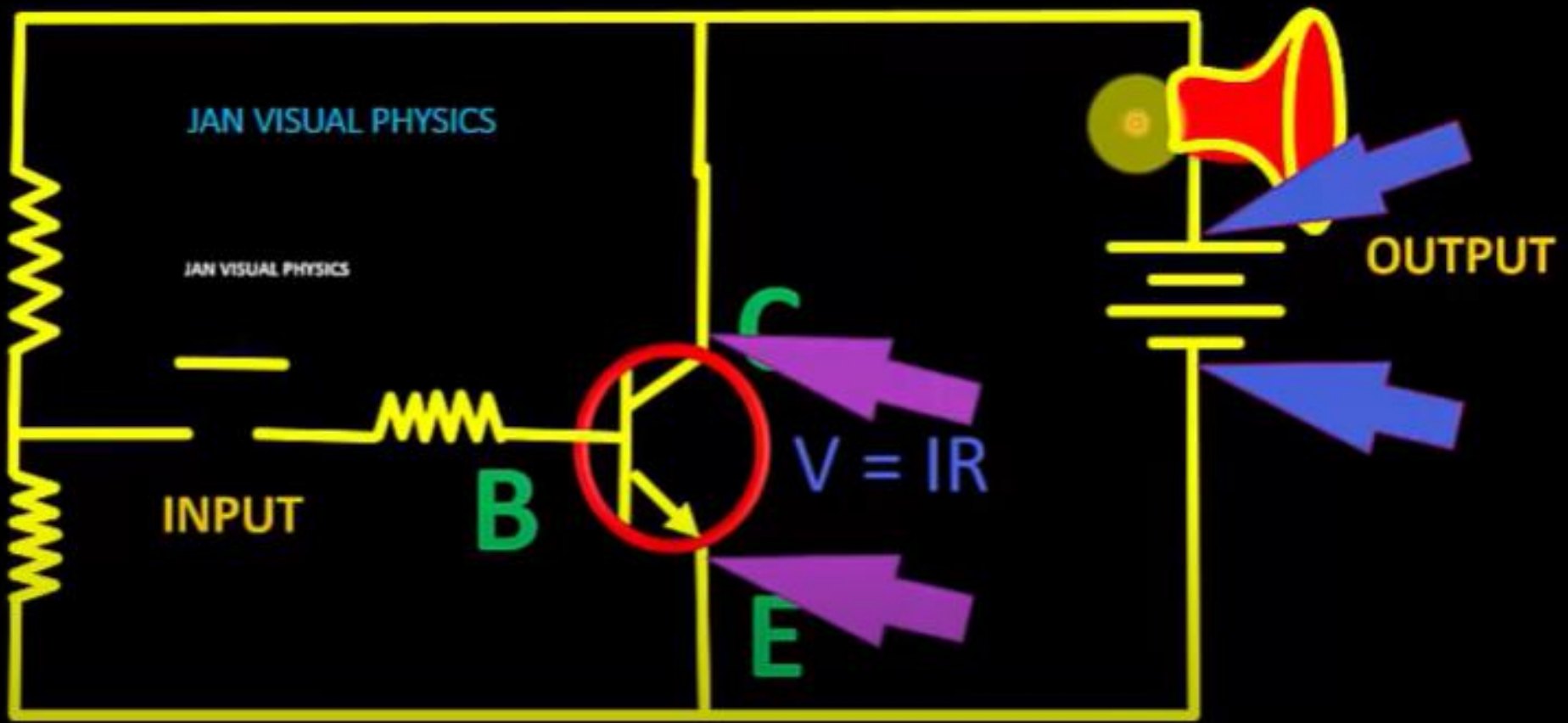
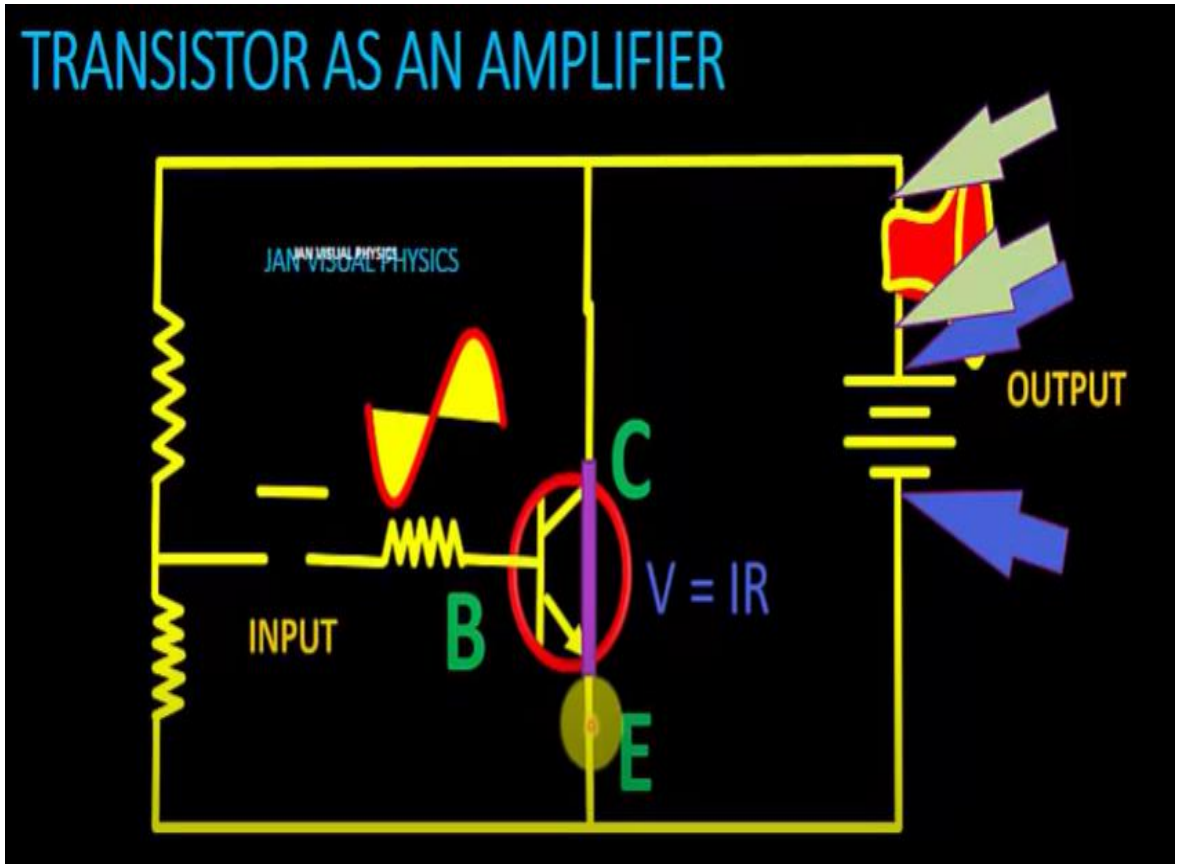

TRANSISTOR AS AN AMPLIFIER
JAN VISUAL PHYSICS
INPUT
B
C
E
V = IR
OUTPUT
JAN VISUAL PHYSICS

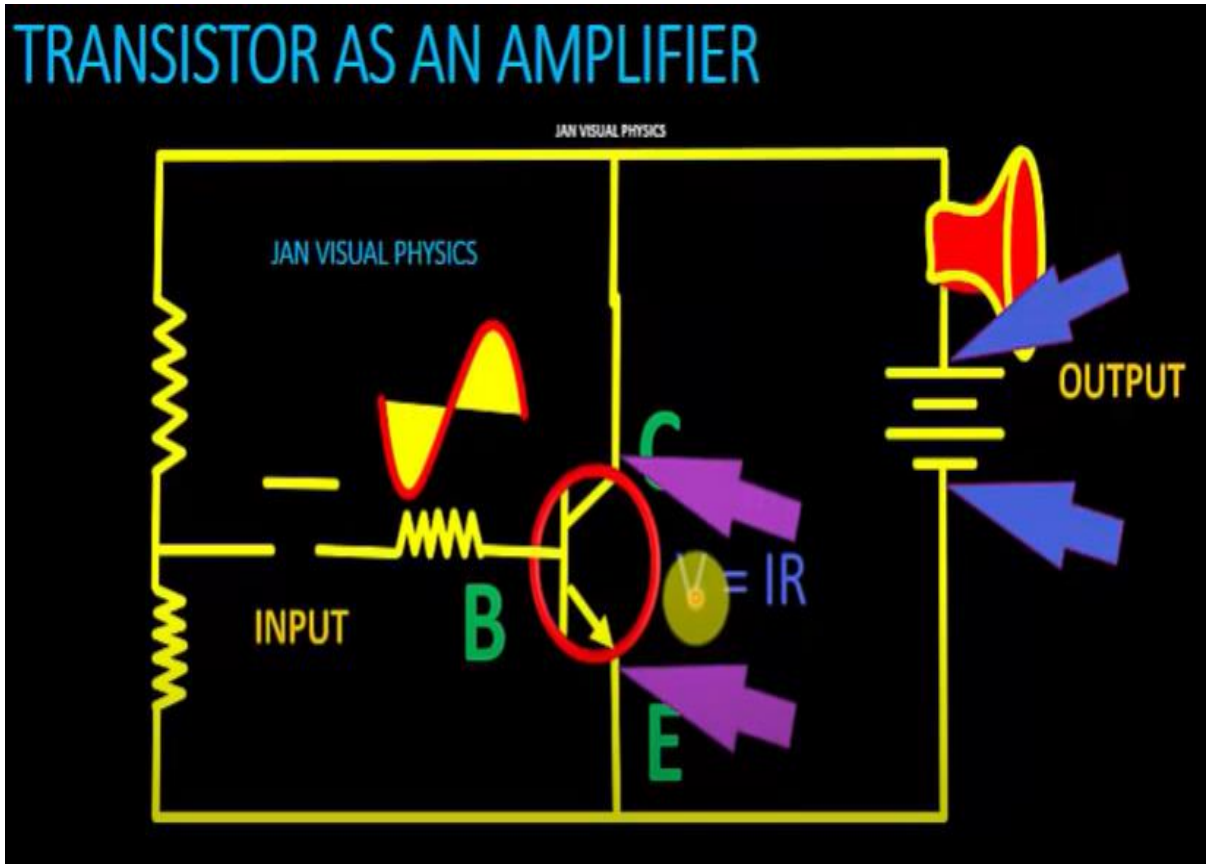

JAN VISUAL PHYSICS
JAN VISUAL PHYSICS
OUTPUT
C
INPUT
B
E

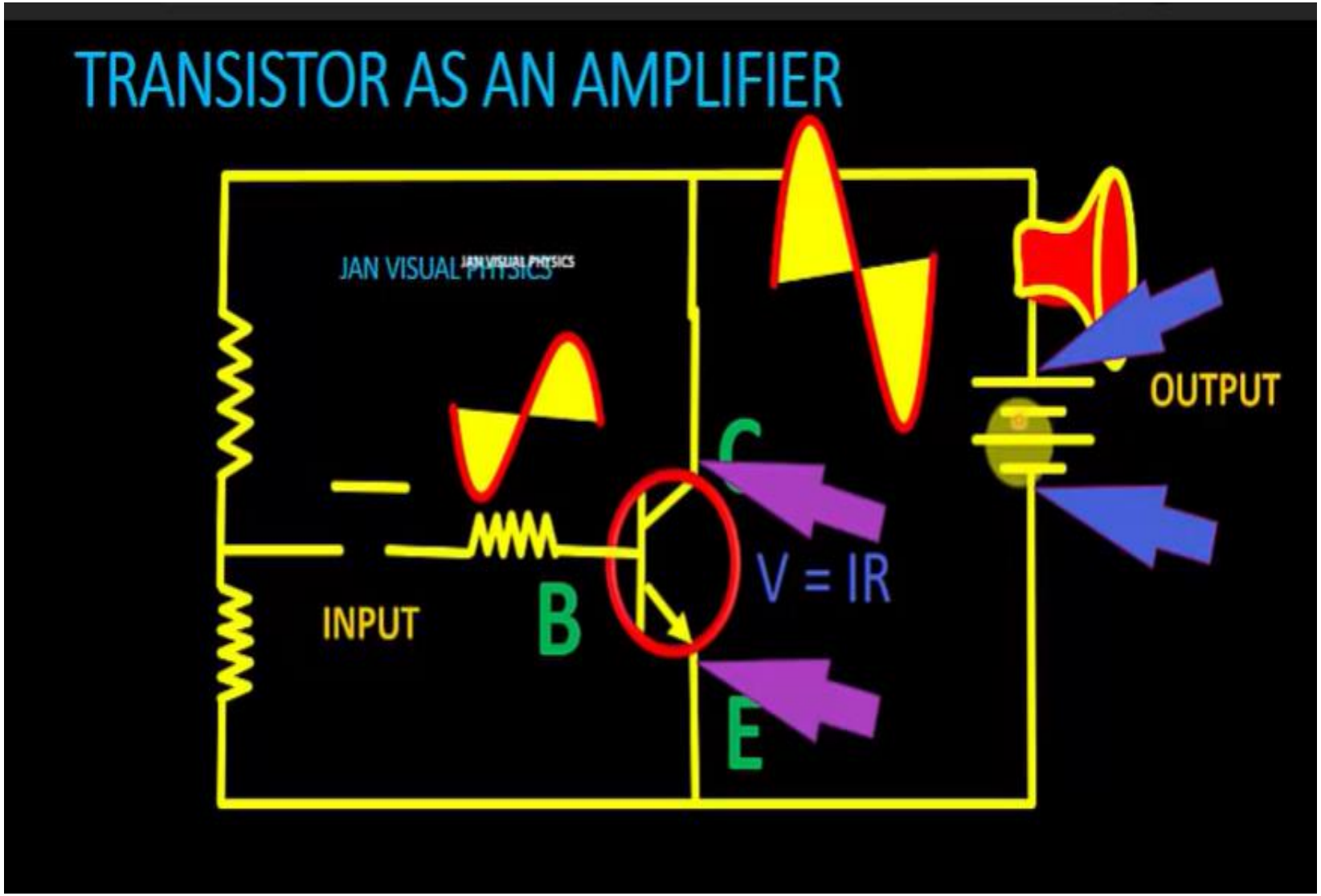

TRANSISTOR AS AN AMPLIFIER
JAN VISUAL PHYSICS
INPUT
B
C
E
V = IR
OUTPUT

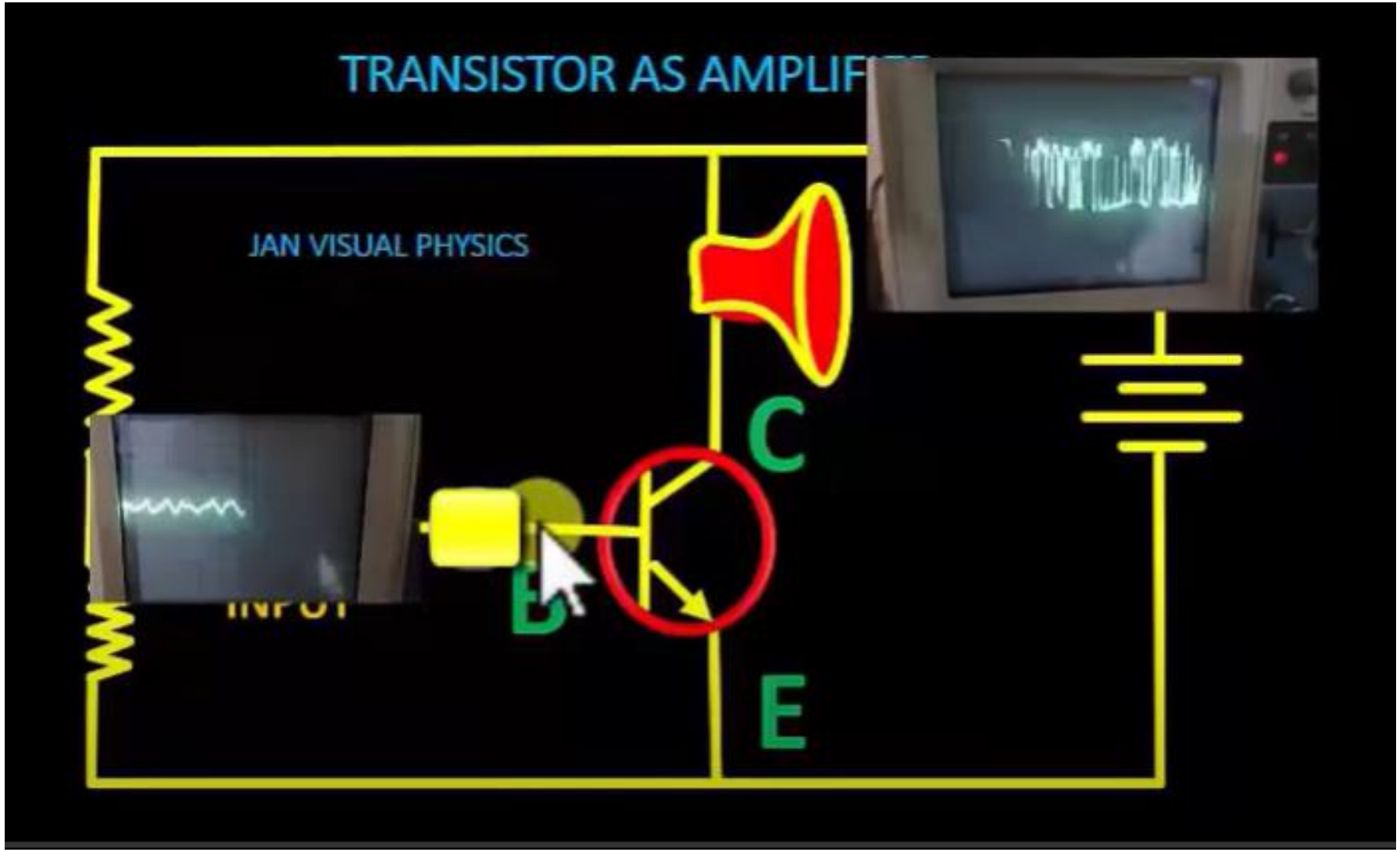
TRANSISTOR AS AN AMPLIFIER




TRANSISTOR AS AN AMPLIFIER
JAN VISUAL PHYSICS
OUTPUT
C
V = IR
INPUT
B
E


TRANSISTOR AS AN AMPLIFIER
JAN VISUAL PHYSICS
JAN VISUAL PHYSICS
OUTPUT
C
= IR
INPUT
B
E


TRANSISTOR AS AN AMPLIFIER
JAN VISUAL PHYSICS
JAN VISUAL PHYSICS
OUTPUT
C
V = IR
INPUT
B
E


TRANSISTOR AS AMPLIF
JAN VISUAL PHYSICS
C
B
E

Classification of Amplifiers

1)Based on Number of stage

I. Single stage amplifier- Single transistor
II. Multi stage amplifier-multi transistor

2)Based on its output

I. Voltage amplifier-increase voltage level input
II. Power amplifier –power level input

3)Based on its input signal

I. Small Signal –small fluctuations in collector current
II. Large signal-fluctuations in collector current is large

4) Based on the frequency

I. Audio-20 Hz to 20Khz
II. power- Very high frequency

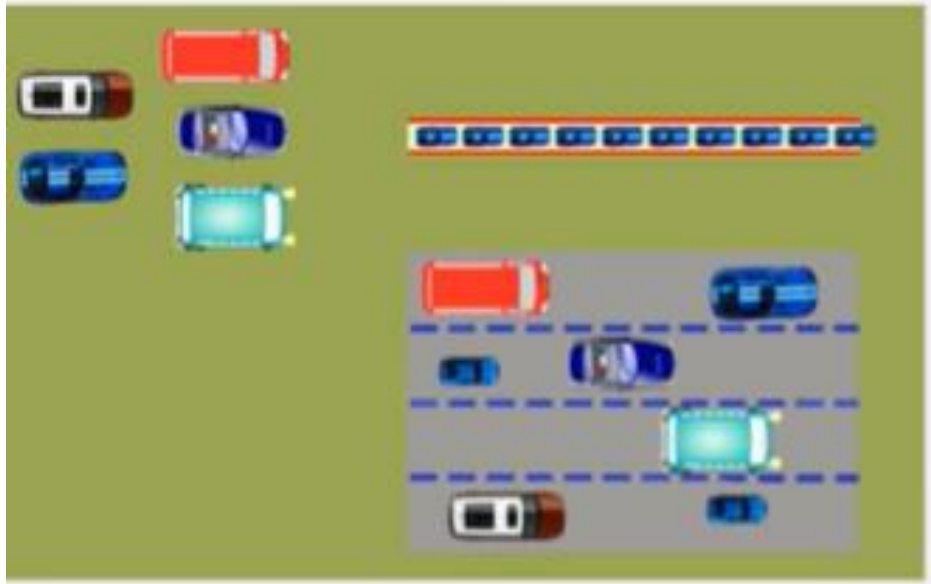
5) Based on biasing conditions

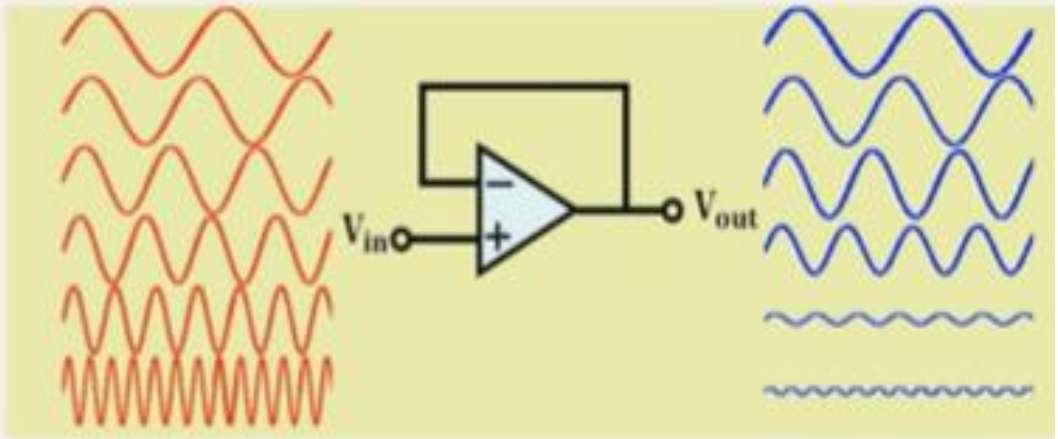
I. Class A
II. Class B
III. Class C
IV. Class AB

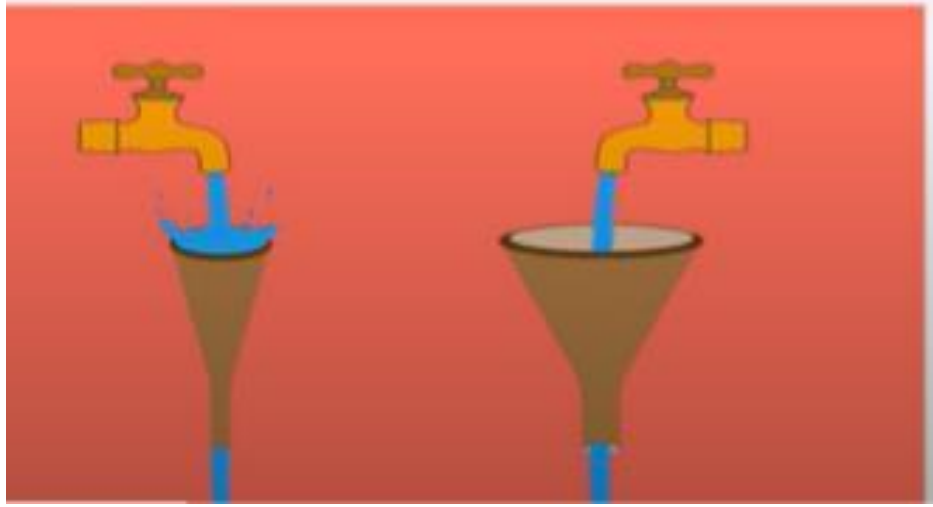
6) Based on coupling methods

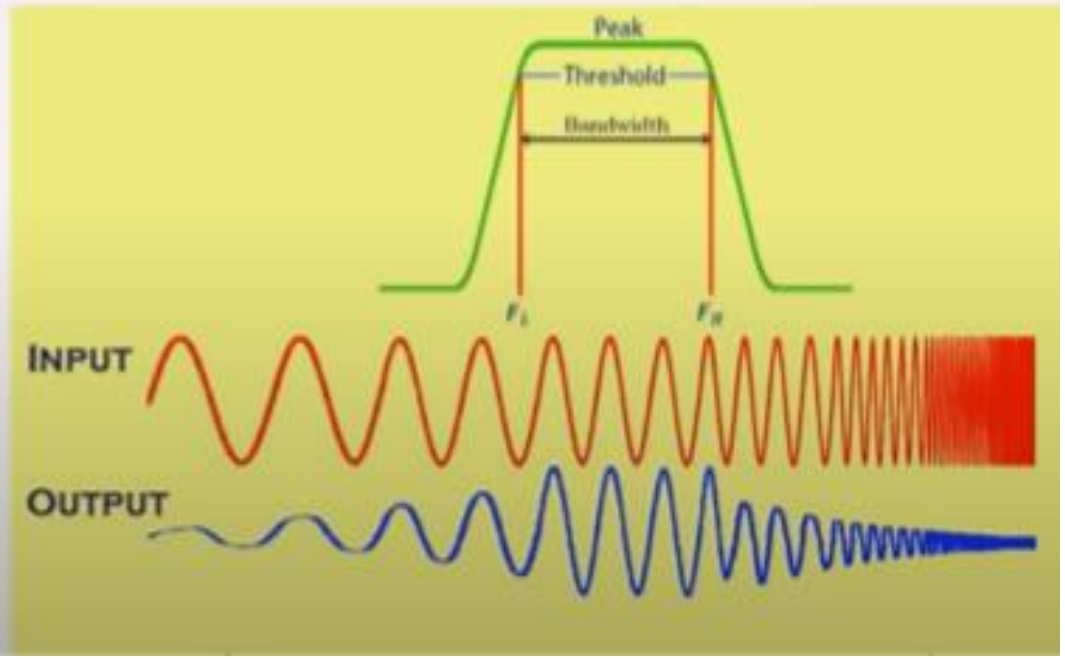
I. RC Coupling (R&C)
II. Transformer (Transformer)
III. Direct coupling (Transistor)

7) Based on its configurations CE,CB,CC




V_{in}
V_{out}




Peak
Threshold
Bandwidth
INPUT
OUTPUT

Search

Stratix 10 - Overview

Secure | https://www.altera.com/products/fpga/stratix-series/stratix-10/overview.html

intel FPGA PRODUCTS | SOLUTIONS | SUPPORT | ABOUT | BUY LOG IN Search

Download the Stratix 10 Device Family Table (PDF) to view the Stratix 10 FPGA and SoC family package plans with vertical migration support.

Stratix 10 FPGA and SoC Benefits

Achieve Performance Breakthroughs with Industry's Highest Performance FPGAs and SoCs

- Ground breaking HyperFlex FPGA Architecture delivering 2X the core performance gains†
- Up to 10 TFLOPS of single-precision floating-point DSP performance
- Quad-core 64 bit ARM Cortex-A53 hard processor subsystem operating up to 1.5 GHz

Break Through the Bandwidth Barrier

- Transceiver tiles (L-, H-, and E-tile) with data rates up to 56 Gbps that deliver 7X bandwidth vs. previous generation FPGAs†
  - Dual-mode transceiver (E-tile) supports up to 56 Gbps PAM-4 and 30 Gbps NRZ
  - Up to 144 full duplex transceivers in a single package
- Over 2.5 Tbps bandwidth for serial memory with support for Hybrid Memory Cube
- Over 2.3 Tbps bandwidth for parallel memory interfaces with support for DDR4 at 2,666 Mbps

Lower Operating Expense

- Leveraging Intel's leadership in process technology, Stratix 10 devices offer the most power-efficient technologies
  - Up to 70% lower power than prior-generation high-end FPGAs and SoCs†
  - Up to 80 giga floating point operations per second (GFLOPS)/Watt of single-precision floating point power efficiency
- Quad-core ARM Cortex-A53 processor optimized for performance per watt

Achieve the Highest Level of System Integration

- Largest monolithic FPGA device with 5.5 million LEs
- Heterogeneous 3D SiP solutions including transceivers and other advanced components
- 64 bit quad-core ARM Cortex-A53 to enable hardware virtualization, system management and monitoring capabilities, acceleration pre-processing, and more

Analog Arts
Innovation Beyond Imagination

Call Center : (781) 246-3800

Home | Products | Downloads | The Company | Store | Learning Center | Selection Table | Search...

OSCILLOSCOPE FUNCTION GENERATOR

PC-Based Oscilloscope | SG985

HOME / PRODUCTS / 5-IN-1 OSCILLOSCOPE / SG985: HIGH PERFORMANCE

Oscilloscope/ Spectrum Analyzer/ Data Recorder

- 2 channels
- 1 GHz analog input bandwidth
- 100 GS/s effective sampling rate, 250 MHz real sampling rate (125 MHz/ channel)
- Rise time: 500 pS
- 1 nS to 365 days/division (data logger)
- Vertical Division: 20 mV to 20 V (10x probe), 2 mV to 2 V (1x probe)
- Input Range: ±80 mV to ±80 V (10x probe), ±8 mV to ±8 V (1x probe)
- 10-bit ADC
- 1 Megabyte data record length

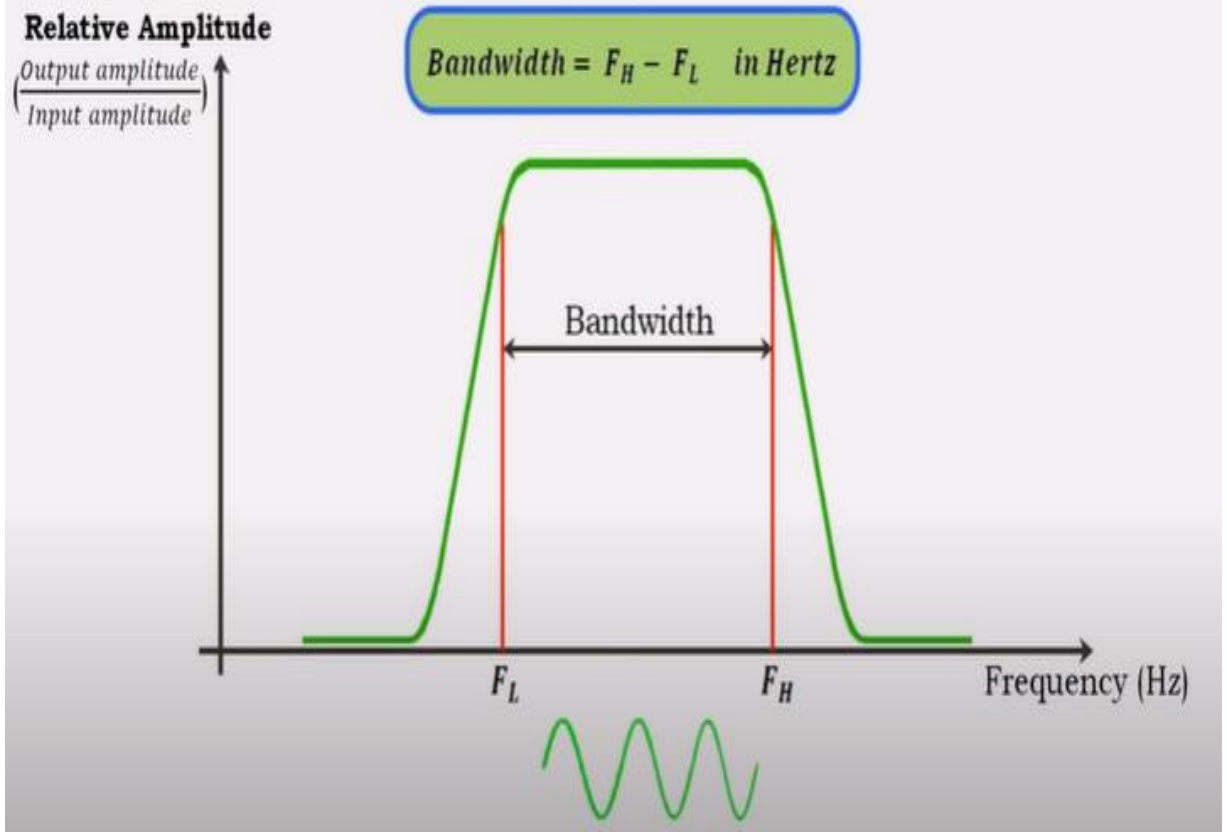
Arbitrary Waveform Generator

- 10 mHz to 150 MHz output frequency

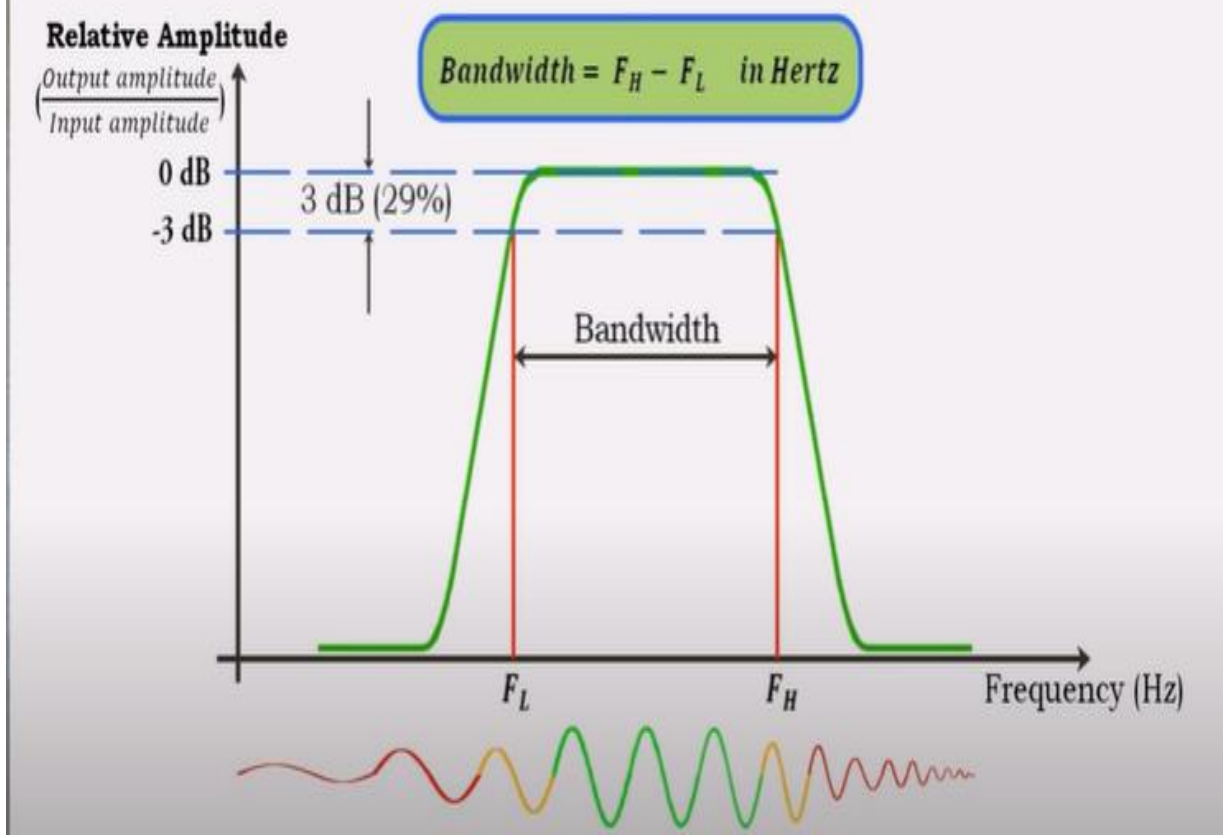
ERVIEW >

SG985 Video Description

BANDWIDTH

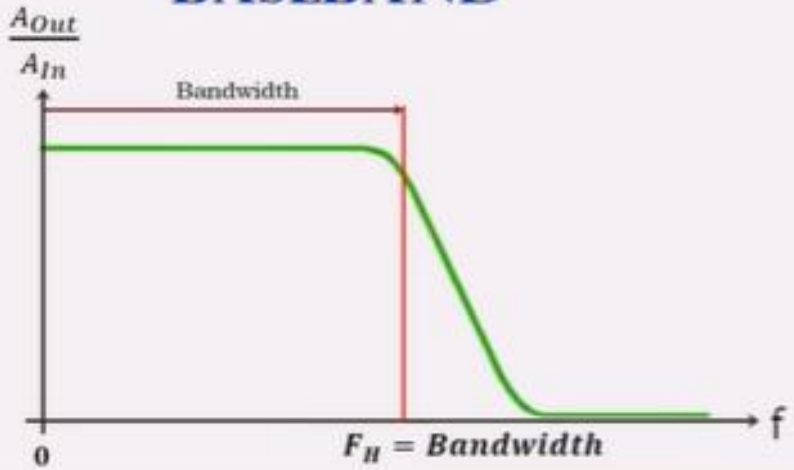


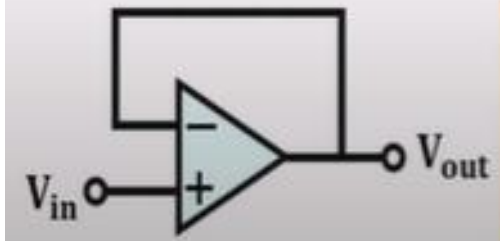
BANDWIDTH



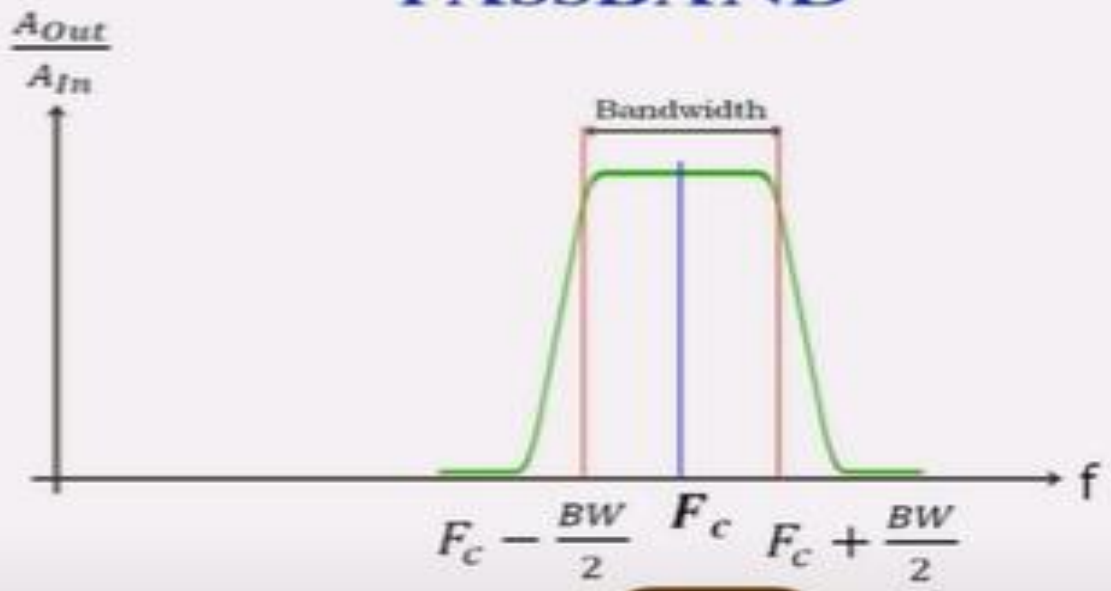
BASEBAND VS. PASSBAND

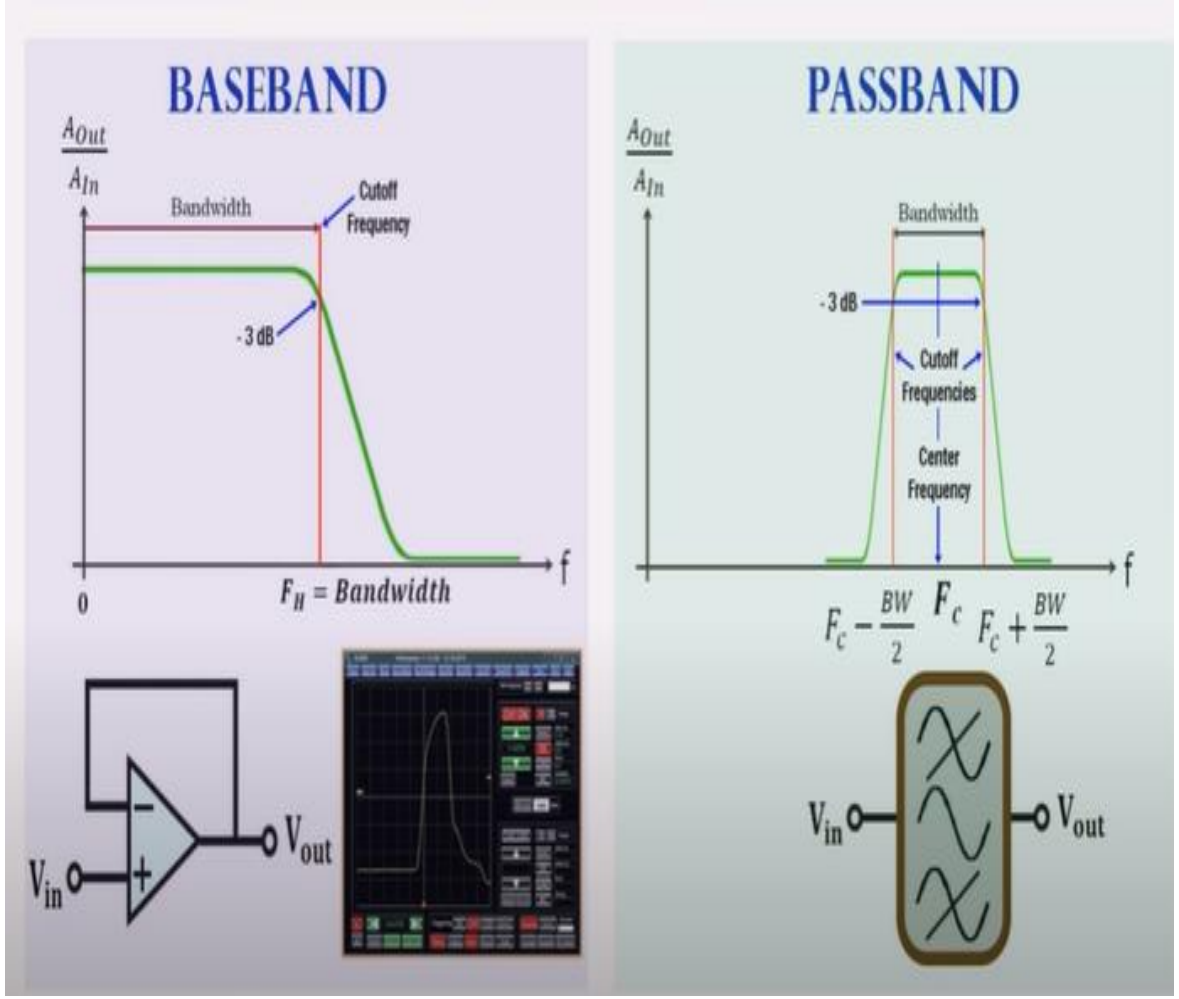
BASEBAND

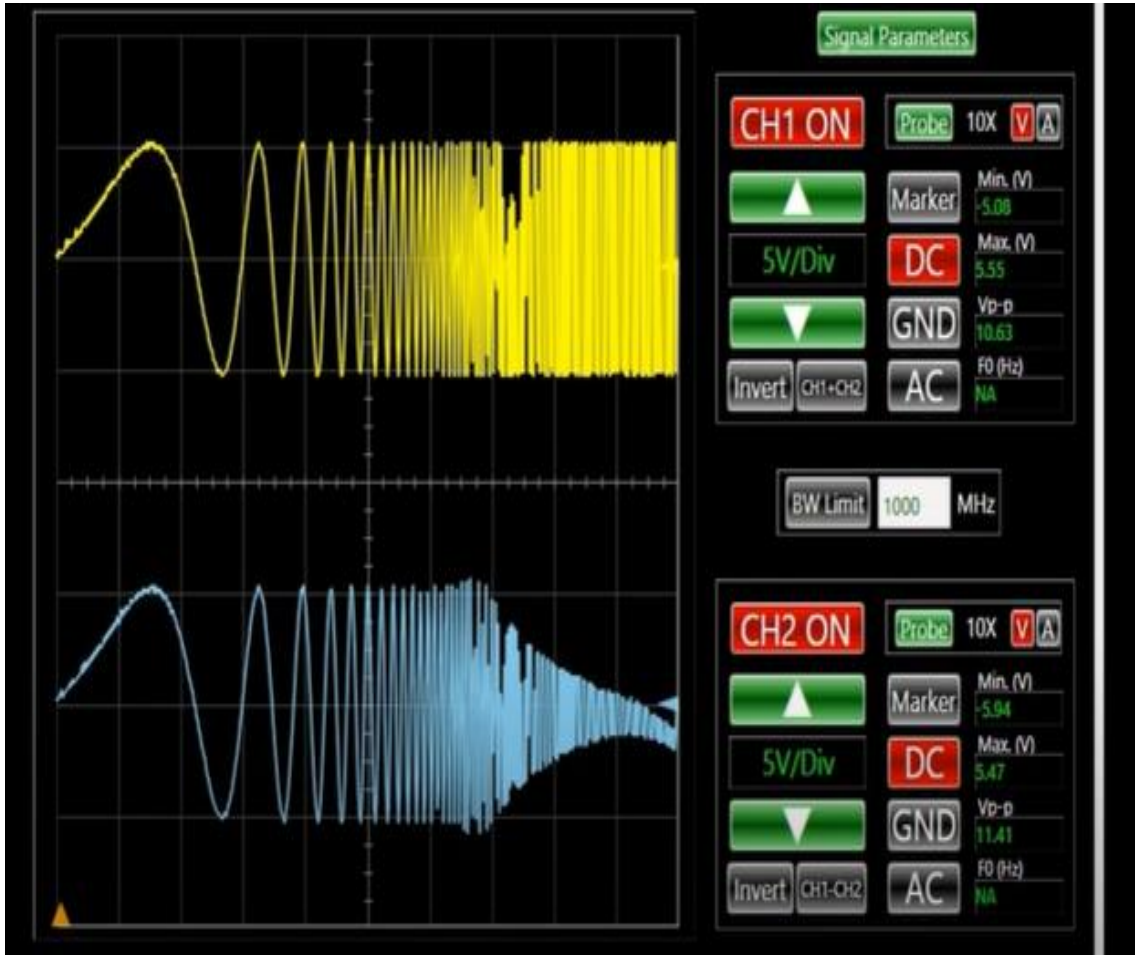




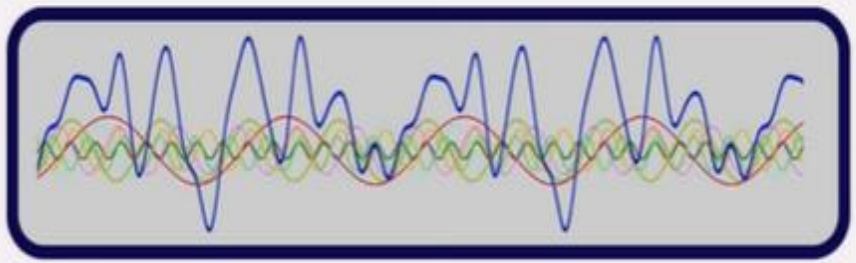
PASSBAND

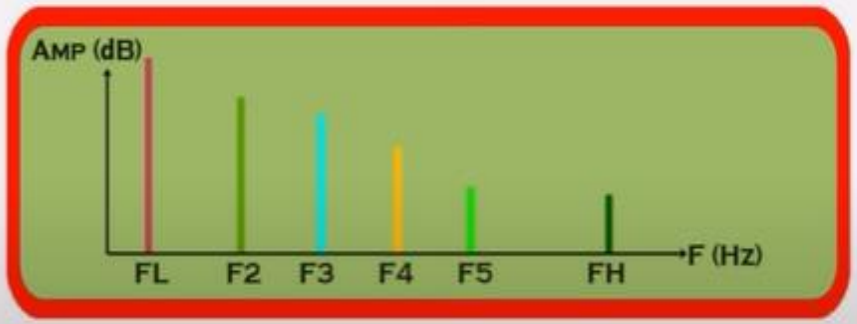



BASEBAND
A_{Out}
A_{In}
Bandwidth
Cutoff Frequency
-3 dB
0
F_H = Bandwidth
f
V_{in}
V_{out}
PASSBAND
A_{Out}
A_{In}
Bandwidth
-3 dB
Cutoff Frequencies
Center Frequency
$F_c - \frac{BW}{2}$
F_c
$F_c + \frac{BW}{2}$
f
V_{in}
V_{out}

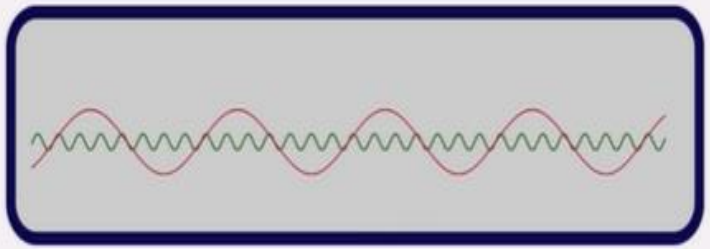

Signal Parameters
CH1 ON
Probe
10X
V
A
Marker
Min. (V)
-5.08
5V/Div
DC
Max. (V)
5.55
GND
Vp-p
10.63
Invert
CH1+CH2
AC
F0 (Hz)
NA
BW Limit
1000
MHz
CH2 ON
Probe
10X
V
A
Marker
Min. (V)
-5.94
5V/Div
DC
Max. (V)
5.47
GND
Vp-p
11.41
Invert
CH1-CH2
AC
F0 (Hz)
NA

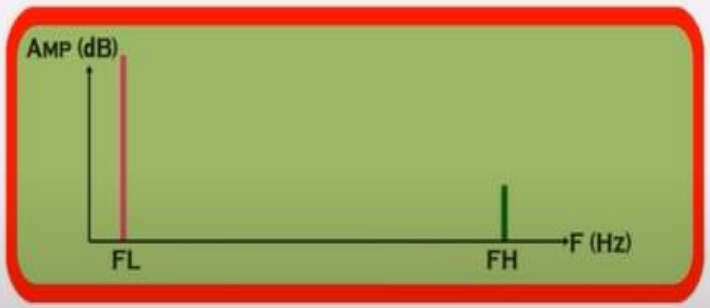
BUILDING BLOCKS OF SIGNALS



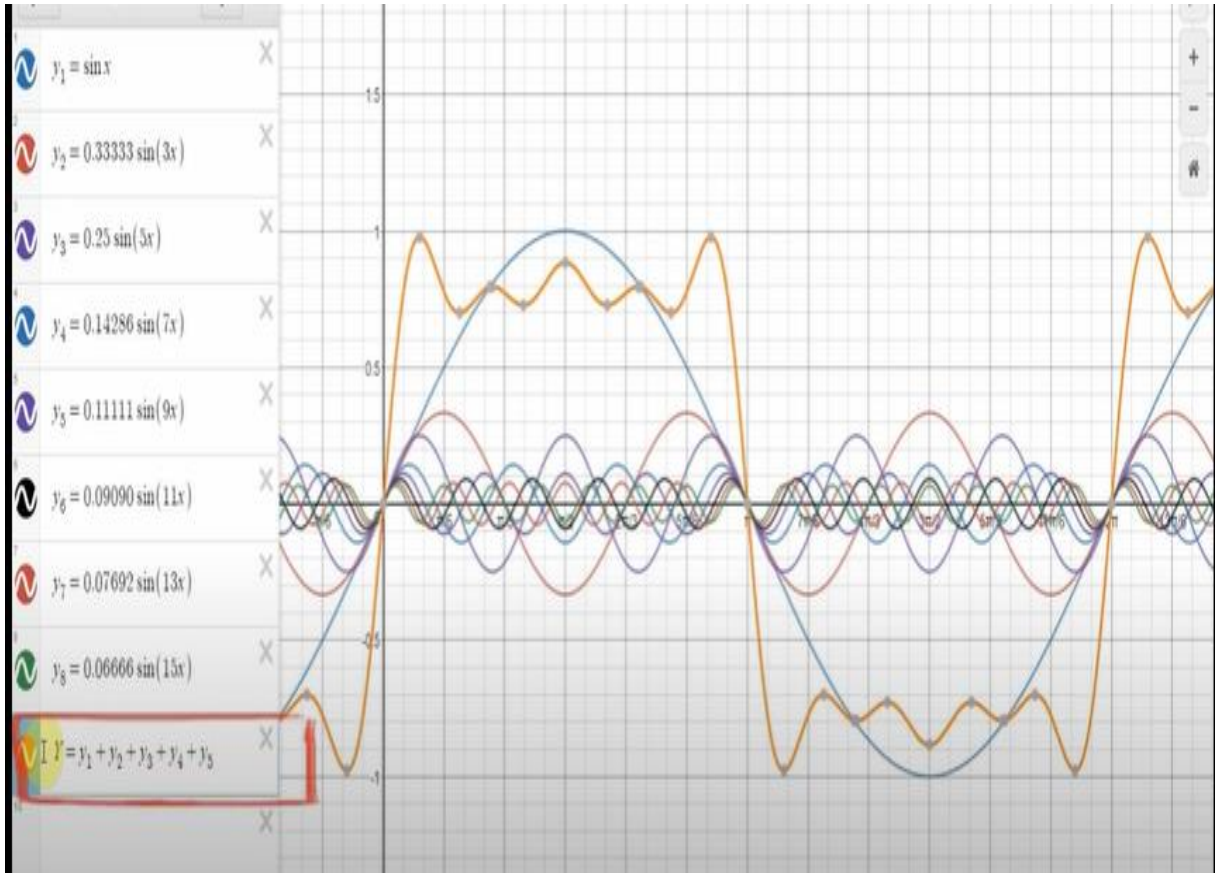


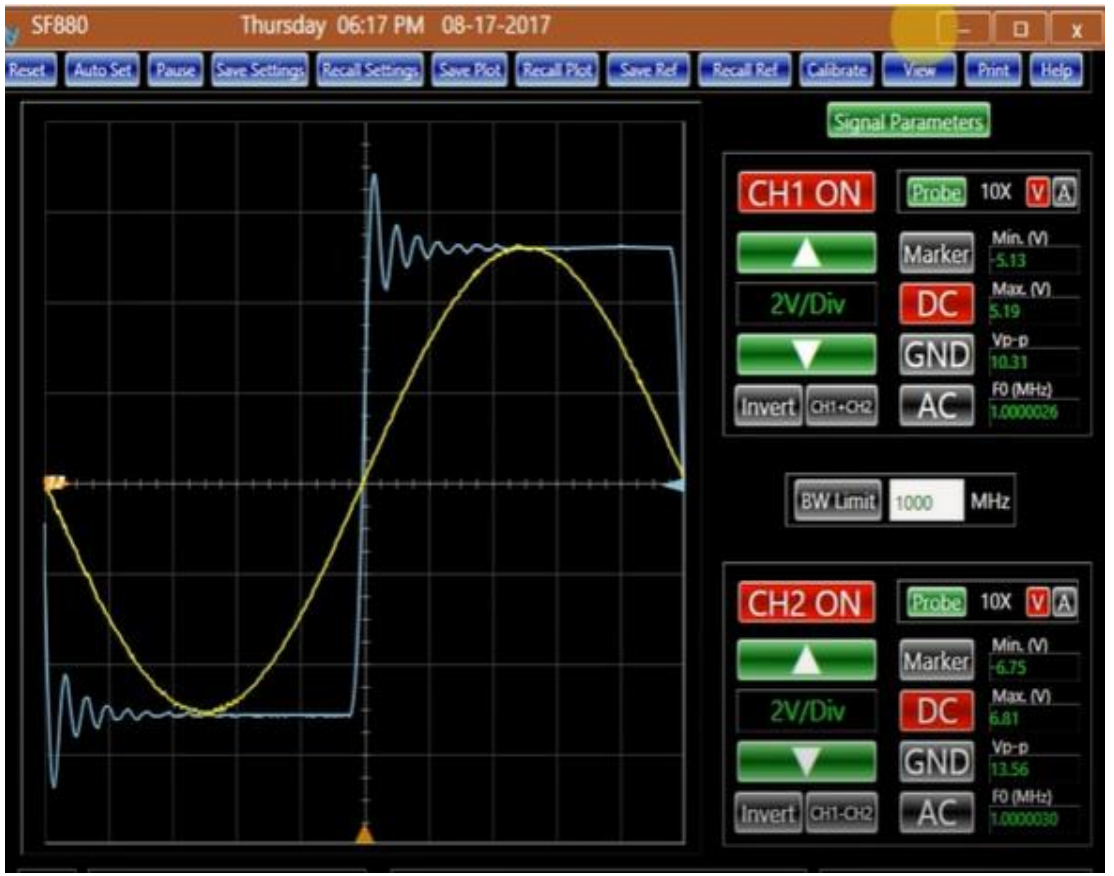
BUILDING BLOCKS OF SIGNALS

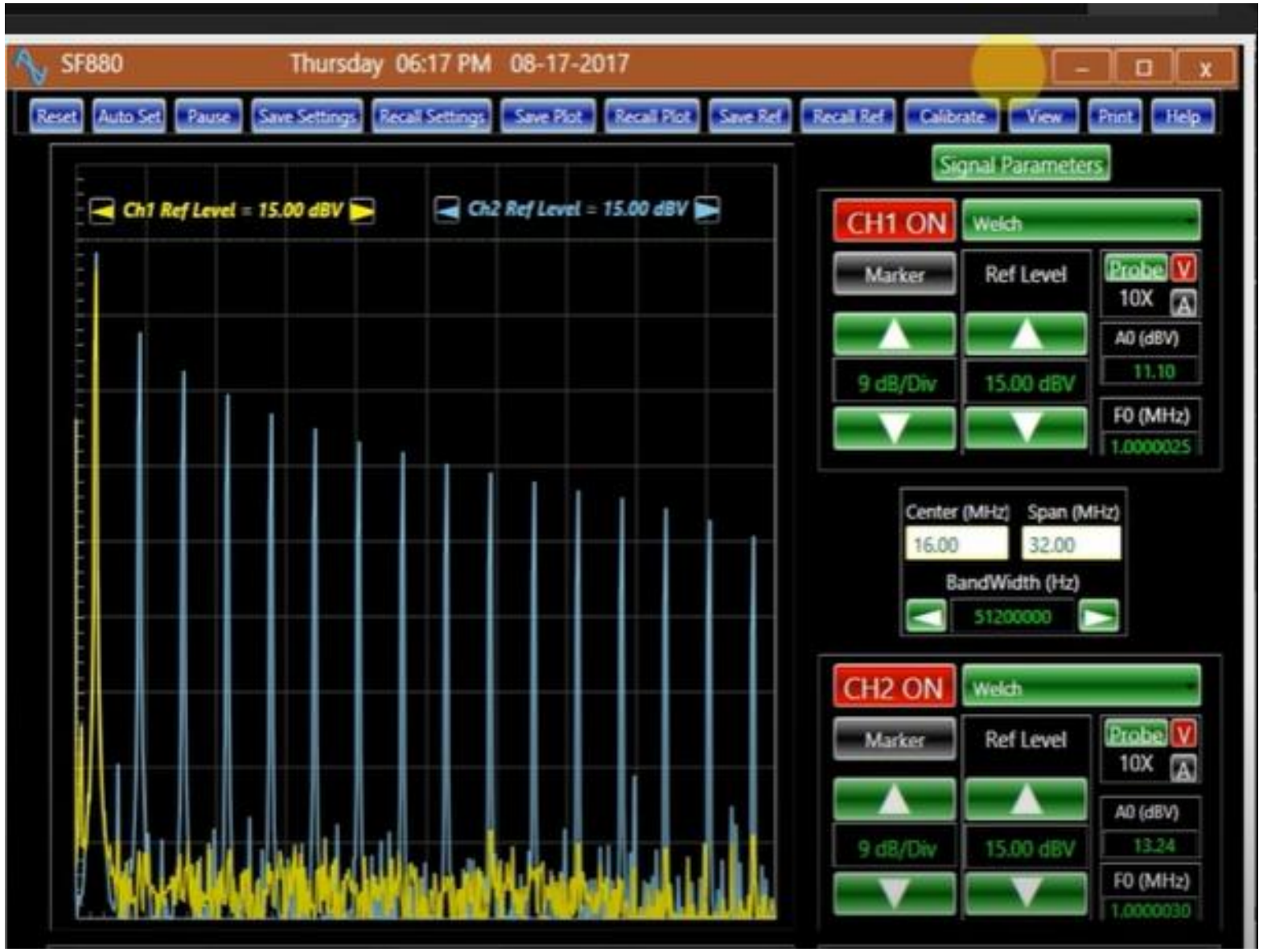




$$Signal\ Bandwidth = F_{Highest\ Component} - F_{Lowest\ Component} \quad in\ Hertz$$


$y_1 = \sin x$
$y_2 = 0.33333 \sin(3x)$
$y_3 = 0.25 \sin(5x)$
$y_4 = 0.14286 \sin(7x)$
$y_5 = 0.11111 \sin(9x)$
$y_6 = 0.09090 \sin(11x)$
$y_7 = 0.07692 \sin(13x)$
$y_8 = 0.06666 \sin(15x)$
$Y = y_1 + y_2 + y_3 + y_4 + y_5$


SF880
Thursday 06:17 PM 08-17-2017
Reset
Auto Set
Pause
Save Settings
Recall Settings
Save Plot
Recall Plot
Save Ref
Recall Ref
Calibrate
View
Print
Help
Signal Parameters
CH1 ON
Probe
10X
V
A
Marker
Min. (V)
-5.13
2V/Div
DC
Max. (V)
5.19
GND
Vp-p
10.31
Invert
CH1+CH2
AC
F0 (MHz)
1.0000026
BW Limit
1000
MHz
CH2 ON
Probe
10X
V
A
Marker
Min. (V)
-6.75
2V/Div
DC
Max. (V)
6.81
GND
Vp-p
13.56
Invert
CH1-CH2
AC
F0 (MHz)
1.0000030


SF880
Thursday 06:17 PM 08-17-2017
Reset
Auto Set
Pause
Save Settings
Recall Settings
Save Plot
Recall Plot
Save Ref
Recall Ref
Calibrate
View
Print
Help
Ch1 Ref Level = 15.00 dBV
Ch2 Ref Level = 15.00 dBV
Signal Parameters
CH1 ON
Welch
Marker
Ref Level
Probe V
10X A
A0 (dBV)
11.10
9 dB/Div
15.00 dBV
F0 (MHz)
1.0000025
Center (MHz)
Span (MHz)
16.00
32.00
BandWidth (Hz)
51200000
CH2 ON
Welch
Marker
Ref Level
Probe V
10X A
A0 (dBV)
13.24
9 dB/Div
15.00 dBV
F0 (MHz)
1.0000030

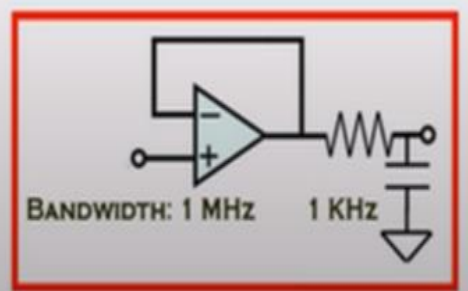
BANDWIDTH REQUIREMENT

System Bandwidth >> Signal's Highest Frequency Component

Signal Bandwidth = 2 MHz,

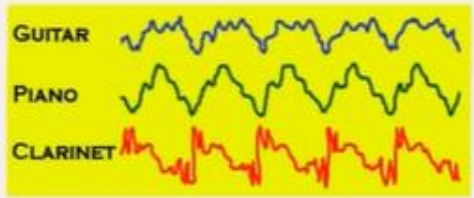
Center Frequency = 10 MHz

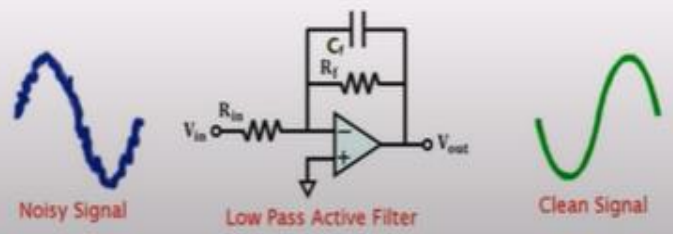
System Bandwidth $\gg$ 11 MHz $(10\ MHz + \frac{2\ MHz}{2})$



Circuit Bandwidth $\simeq$ 1 KHz

Bandwidth and Performance





Data Transfer