

ASSIGNMENT-2 HINTS & SOLUTIONS

- 1 Show that the Fermi level is at the center of forbidden gap in an intrinsic semiconductor. State what happens to the Fermi level of N-type and P-type semiconductors by referring to expressions concerned.

(First define Fermi level)

- Fermi level is the measure of the energy of least tightly held electrons
- Fermi level also indicates the probability of occupancy of a given energy level by an electron
- The probability that the charged particle will have an energy E is given by Fermi-Dirac distribution or Fermi function $f(E) = \frac{1}{1 + e^{\left(\frac{E - E_F}{kT}\right)}}$

Where E_F = Fermi energy or Fermi level (eV)

k = Boltzman's constant (1.38×10^{-24} J/K or 8.62×10^{-5} eV/K), T = temperature (K)

$kT = 0.026$ eV at room temp (300 K)

- If $E = E_F$, then $f(E) = 0.5$
- So, Fermi level is defined as the energy point where the probability of occupancy by an electron is exactly 50%, or 0.5

Expression for Fermi level in an intrinsic semiconductor:

- Derivation of Fermi level in an intrinsic semiconductor (E_F'):

Refer to your class notes for derivation of E_F'

- The Fermi level of intrinsic semiconductor is given by

$$E_F' = \left(\frac{E_C + E_V}{2} \right) + \frac{kT}{2} \ln \left(\frac{N_V}{N_C} \right)$$

E_C = Conduction band bottom edge energy level (eV)

E_V = Valence band top edge energy level (eV)

N_C = Effective density of energy states in conduction band

N_V = Effective density of energy states in valence band

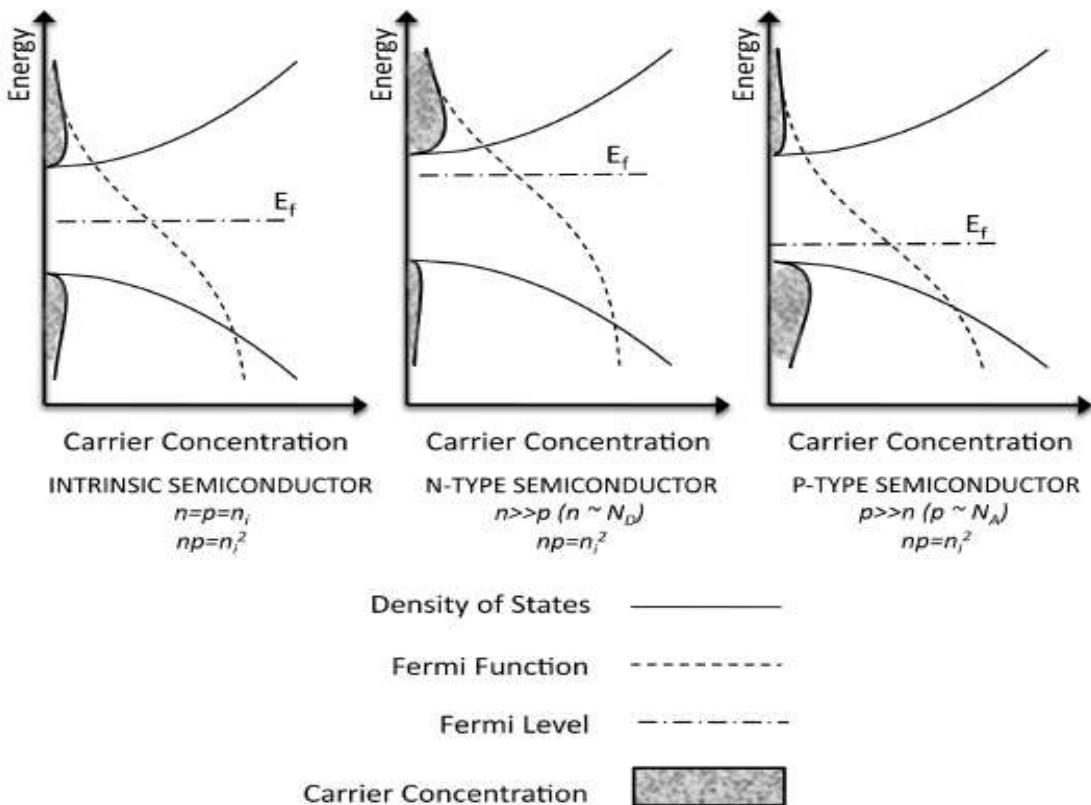
k = Boltzman's constant (1.38×10^{-24} J/K or 8.62×10^{-5} eV/K), T = temperature (K)

$kT = 0.026$ eV at room temp (300 K)

- The second term contributes very little, hence the intrinsic Fermi level is

$$E_F' = \left(\frac{E_C + E_V}{2} \right)$$

The Fermi level in case of intrinsic semiconductor (E_F') lies in the middle of bandgap



Extrinsic semiconductor:

- N-type semiconductor: The Fermi level of N-type semiconductor (E_F^N) is given by

$$E_F^N = E_C - kT \ln\left(\frac{N_c}{N_d}\right)$$

Where, E_C = Conduction band bottom edge energy level (eV)

N_c = Effective density of energy states in conduction band

N_d = Donor impurity concentration (atoms/cm³)

k = Boltzmann's constant (1.38×10^{-24} J/K or 8.62×10^{-5} eV/K), T = temperature (K)

$kT = 0.026$ eV at room temp (300 K)

- In N-type SC, the Fermi level (E_F^N) is higher than intrinsic Fermi level (E_F^i) and close to the conduction band (just below the CB).

- P-type semiconductor: The Fermi level of N-type semiconductor (E_F^P) is given by

$$E_F^P = E_V + kT \ln\left(\frac{N_v}{N_A}\right)$$

Where, E_V = Valence band top edge energy level (eV)

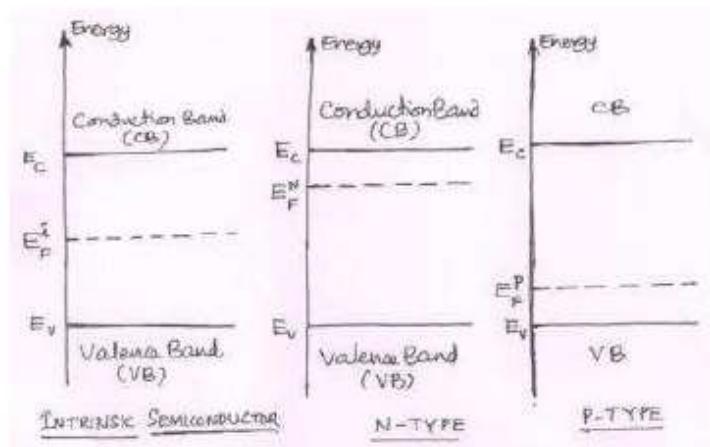
N_v = Effective density of energy states in valence band

N_A = Acceptor impurity concentration (atoms/cm³)

k = Boltzmann's constant (1.38×10^{-24} J/K or 8.62×10^{-5} eV/K), T = temperature (K)

$kT = 0.026$ eV at room temp (300 K)

- In P-type SC, the Fermi level (E_F^P) is lower than intrinsic Fermi level (E_F^i) and close to the valence band (just above the VB).



2 Explain Drift and diffusion currents with reference to a semiconductor.

- The two mechanisms of flow of current in a semiconductor are:
 - (i) Drift Current (J_{drift}),
 - (ii) Diffusion current (J_{diff})
- Net current in a semiconductor (J) is sum of drift current and diffusion current

$$J = J_{drift} + J_{diff} \quad \dots \dots \dots (1)$$

Here J is current density given by $J = \sigma E$

Where, σ = conductivity $(\Omega-m)^{-1}$ of the material,

E = electric field (V/m) applied across the semiconductor

Drift current (J_{drift})

- The charged particles move or drift under the influence of the applied electric field E
- The ordered movement of charge carriers due to applied electric field is called drift and the resulting current is called drift current
- The drift current due to applied electric field E (V/m) is

$$J = \sigma E \quad \dots \dots \dots (2)$$

Where, σ is conductivity $(\Omega-m)^{-1}$ of the material, given by

$$\sigma = n\mu q,$$

Where, μ is mobility ($m^2/V-s$) $\leftarrow ((m/s)/(V/m))$

n = electron concentration (number of electrons/unit volume)

q = charge on electron ($-1.6 \times 10^{-19} C$)

- As current in a semiconductor is due to both electrons (n) and holes (p)

$$J_{drift} = J_{n-drift} + J_{p-drift}$$

$$J_{drift} = (n\mu_n q)E + (p\mu_p q)E$$

$$J_{drift} = (n\mu_n + p\mu_p)qE \quad \dots \dots \dots (3)$$

Where, μ_n = mobility of electrons ($cm^2/V-s$), n = concentration of electrons ($atoms/cm^3$)

μ_p = mobility of holes ($cm^2/V-s$); p = concentration of electrons ($atoms/cm^3$)

Diffusion current (J_{diff})

(It is possible for electric current to flow in a semiconductor, even in the absence of applied voltage.
Diffusion current)

- Carrier concentration gradient: The charge carriers have a natural tendency to diffuse (move) from a region of higher concentration to the region of lower concentration
- The uncoordinated random movement of charge carriers due to charge gradient is called diffusion and the current associated with diffusion process is called Diffusion current.
- Diffusion current density is directly proportional to concentration gradient
- Diffusion current density \propto The rate of change of concentration per unit length of SC

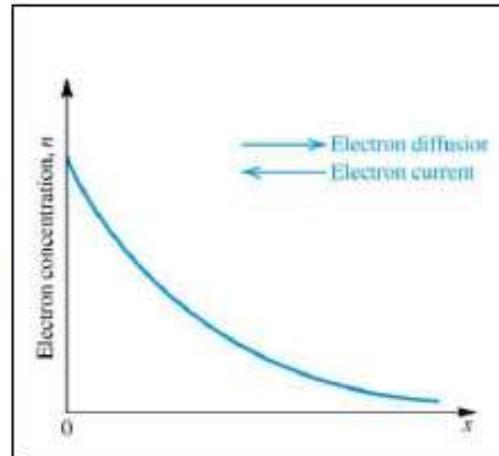
Diffusion current for electrons:

- Carriers move toward regions of lower concentration, so diffusion current densities are proportional to the negative of the carrier gradient.
- As shown in figure, the electrons diffusing in the x direction, giving rise to an electron-diffusion current in the negative $-x$ direction

$$J_{n-diff} \propto (-q)(-\frac{\partial n}{\partial x})$$

$$J_{n-diff} = D_n q \frac{\partial n}{\partial x} \quad \dots \dots (4)$$

Where, D_n is electron diffusion coefficient (cm^2/s)



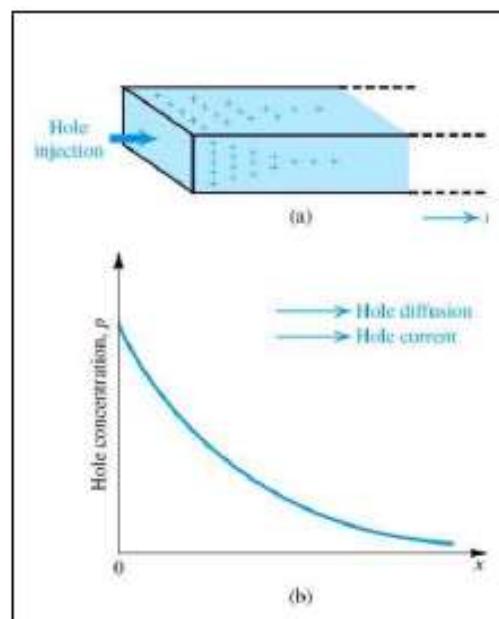
Diffusion current for holes:

- The holes diffuse in the positive direction of x and give rise to a hole-diffusion current in the same direction

$$J_{p-diff} \propto (q)(-\frac{\partial p}{\partial x})$$

$$J_{p-diff} = -D_p q \frac{\partial p}{\partial x} \quad \dots \dots (4)$$

Where, D_p is called hole diffusion coefficient (cm^2/s)



Total current:

Total current is the sum of drift and diffusion current

$$J = J_{drift} + J_{diff}$$

$$J = (J_{n-drift} + J_{p-drift}) + (J_{n-diff} + J_{p-diff})$$

$$J = (J_{n-drift} + J_{n-diff}) + (J_{p-drift} + J_{p-diff})$$

$$J = (q\mu_n n E + qD_n \frac{\partial n}{\partial x}) + (q\mu_p p E - qD_p \frac{\partial p}{\partial x})$$

$$J = J_n + J_p$$

3. Explain how the depletion region is formed at a P-N junction.

P-type semiconductor has :

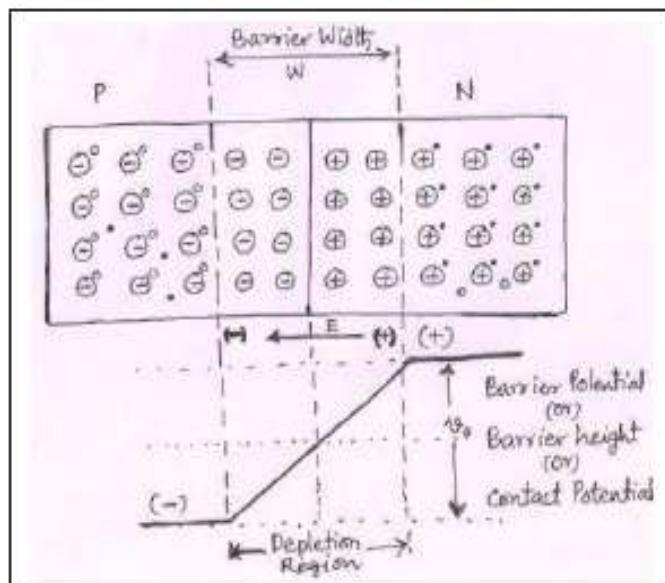
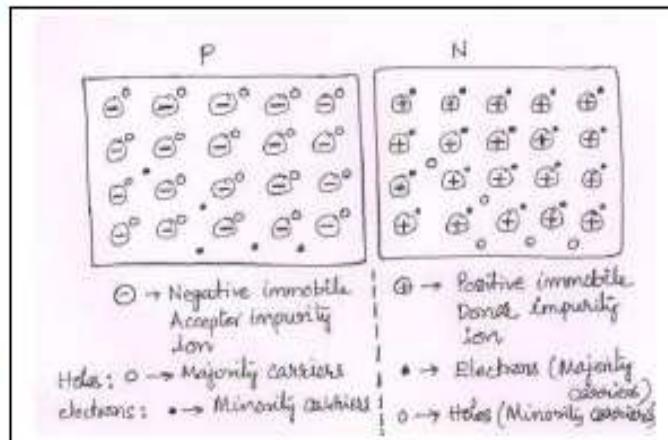
- Mobile charge carriers:
 - (i) Holes as majority carriers,
 - (ii) Electrons as minority carriers
- Immobile ions: Negatively charged impurity ions

N-type semiconductor has :

- Mobile charge carriers: (i) Electrons as majority carriers, (ii) Holes as minority carriers
- Immobile ions: Positively charged impurity ions
- By themselves, P-type and N-type semiconductors are of very limited use
- If a junction is made by joining P-type material to N-type material, a useful device is produced called P-N junction diode

As soon as the P-N junction is formed, the following processes are initiated:

- Charge gradient across the junction:
Excess of holes in P-type and excess of electrons in N-type materials.
- Diffusion of charge carriers: Due to charge gradient,
 - majority holes from P region diffuse into the N region ; and
 - majority electrons from N region diffuse into P region



This diffusion of majority carriers establishes diffusion current (I_{diff}) in the diode

- Electron-hole recombination: As the charge carriers diffuse across the junction, holes will recombine with free electrons and (vice-versa) electrons will recombine with holes.
- Depletion region or space-charge region:
 - The process of electron-hole recombination will uncover the bound charges and leave behind a region of immobile ions at the immediate vicinity of the junction.
 - This region where there will be no mobile charges is called a depletion region or it is also called space charge region. This region is devoid of the free carriers.
 - Depletion region acts like a barrier that opposes the flow of electrons from n-side and holes from p-side.
 - The physical width of depletion region is called barrier width (W). It is of order of Angstrom (10^{-10} m)

$$\text{The barrier width is given by } w = \sqrt{\frac{2\epsilon_0 \epsilon_r V_0}{q} \left(\frac{N_D + N_A}{N_D N_A} \right)}$$

N_D = Donor impurity concentration, N_A = Acceptor impurity concentration,
 n_i = intrinsic concentration, ϵ_r = relative permittivity, V_0 = barrier potential (V),
 q = charge on electron (C)

Barrier potential (V_0)

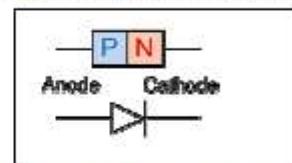
- The depletion region consists of uncovered negative charge on the P side and uncovered positive charge on the N side.
- That means a potential is developed across the junction and that potential is positive on the N side and negative on the P side.
- This potential will be now preventing further diffusion of charge (majority) carriers across the junction.
- This is called barrier potential (V_0) because of the fact that it is a barrier to further movement of carriers.
- Barrier potential is also referred to as height of the barrier or built-in potential or contact potential
- The expression for barrier potential (V_0) is given by

$$V_0 = \frac{kT}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right)$$

Where, N_D = Donor impurity concentration N_A = Acceptor impurity concentration,

k = Boltzman's constant (eV/K), T = temp (K); $kT = 0.026 \text{ eV}$ at room temp (300 K),
 n_i = intrinsic concentration, q = charge on electron (C)

- The Barrier potential or built-in potential (V_o) = $\begin{cases} 0.3 \text{ V, for Ge diodes} \\ 0.7 \text{ V, for Si diodes} \end{cases}$
- Due to barrier potential, an electric field (E) will be set up, which is directed from N side to P side
- On one side the barrier potential discourages the diffusion of majority carriers across the junction. At the same time the barrier potential helps the minority carriers to drift across the junction resulting in drift current (I_{drift})
- Under steady state or at equilibrium, $I_{diff} = I_{drift}$
So net current in the diode under open circuit is zero.
- The circuit symbol of P-N junction diode is shown. This diode has immense applications in electronics starting from rectification



4. Explain the operation of the p-n diode in forward and reverse bias modes. Also plot the V-I characteristic curve for Si and Ge diodes.

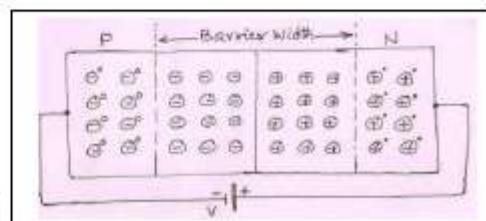
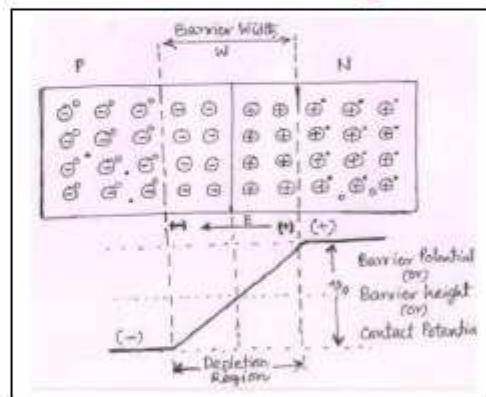
Open circuited diode

- When no external voltage is applied across the P-N junction diode, it is said to be open circuited.
- The figure shows the P-N junction under open circuit. It depicts a space-charge region or depletion region in the vicinity of the junction

Biased diode: When some external voltage is applied across the diode, it is said to be biased.

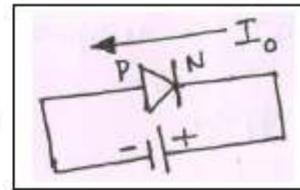
Reverse bias: Figure shows a reverse biased P-N junction.

- Positive terminal of the external battery is connected to the N side
- Negative terminal of the battery is connected to the P side
- The majority carriers are drawn away from the junction due to external battery polarity.
- This act widens the depletion region and increases the barrier potential.
- However, the barrier potential drives the minority carriers to cross the junction.
- As the minority carriers are small in number in number, the diode current in reverse bias is very small. It is also called *reverse leakage current*.



- Reverse saturation current (I_o): At a given temperature, the minority carriers are fixed in number. Hence the diode reverse current will remain constant, even if the applied reverse bias voltage is increased. For this reason, the diode reverse current is also called reverse saturation current (I_o)

$$I_o = \begin{cases} \text{few } \mu A, & \text{for Ge diodes} \\ \text{few } nA, & \text{for Si diodes} \end{cases}$$



- Breakdown voltage (V_{BD}): If the reverse voltage is increased beyond a particular value, called breakdown voltage (V_{BD}), there will be a sudden rise in the I_o .
- V_{BD} is normally very high and practical rectifier diodes are not operated in breakdown condition.
- Breakdown voltage in conventional diodes: $V_{BD} = \begin{cases} 50-70V & , \text{ for Ge diodes} \\ \text{around } 100V. & \text{for Si diodes} \end{cases}$

(Note: Breakdown region of operation is useful in "Voltage Regulator" applications. Those diodes are called Zener diodes, which are deliberately operated in breakdown region)

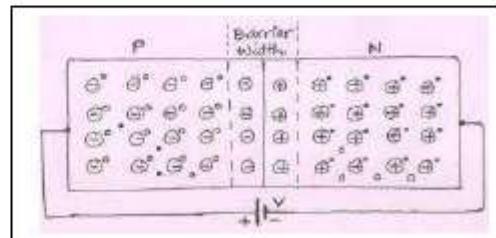
- The I_o is a temperature dependent parameter
- When temperature increases, more covalent bonds will be broken. Majority carriers will be drawn away from junction by applied reverse bias, whereas the barrier potential will help the minority carriers drift across the junction. This increases the reverse saturation current.
- Reverse saturation current doubles for every 10°C rise in temperature

$$I_{02} = I_{01} \left(2^{\left(\frac{\Delta T}{10} \right)} \right); \quad \text{Where, } I_{01} = \text{Reverse saturation current at temp } T_1 {}^{\circ}\text{C}$$

$$I_{02} = \text{Reverse saturation current at temp } T_2 {}^{\circ}\text{C}, \quad \Delta T = (T_2 - T_1) {}^{\circ}\text{C}$$

Forward bias: Figure shows a forward biased P-N junction

- Positive terminal of the external battery is connected to the P side
- Negative terminal of the battery is connected to the N side



- Majority holes in P side are repelled from positive terminal of the battery and are forced to cross the junction, by penetrating the depletion region.
- Majority electrons in N side are repelled from negative terminal of the battery and are forced to cross the junction, by penetrating the depletion region.
- This act reduces the depletion region and the barrier potential.
- The diode does not conduct well until the applied voltage (V) overcomes the barrier potential (v_o)

- The Barrier potential or built-in potential (v_o) = $\begin{cases} 0.3 \text{ V, for Ge diodes} \\ 0.7 \text{ V, for Si diodes} \end{cases}$
- When applied voltage (v) approaches 0.7 V for Si, large number of electrons and hole are drifted to cross the junction
- When $v > v_o$, even a small increase in the v produces a sharp increase in the current
- Cut-in voltage or knee voltage (v_o): The voltage at which the diode current starts to increase rapidly is called *cut-in voltage or knee voltage*
- Diode current equation: For the applied external voltage (v), the forward current through diode (I) is given by

$$I = I_0 e^{\left(\frac{v}{\eta V_T}\right)}$$

Where, I = forward current through the diode (Amp)

I_0 = Reverse saturation current through the diode (A)

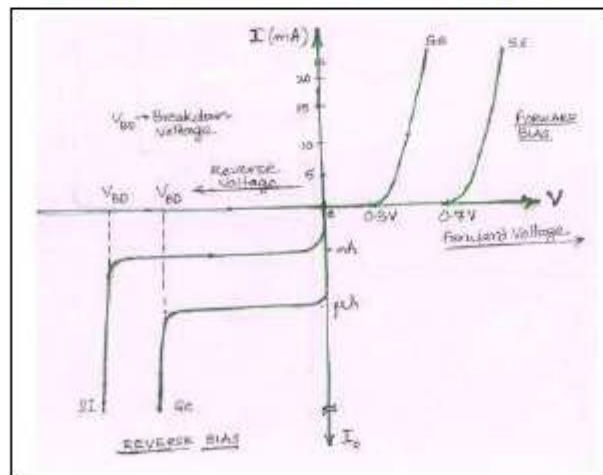
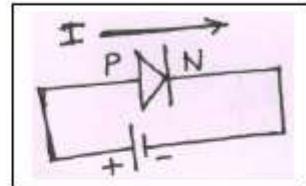
v = forward voltage applied across the diode (V)

$$\eta = \begin{cases} 1; \text{ for Ge} \\ 2; \text{ for Si} \end{cases}$$

$$V_T = \text{Volt equivalent of temperature (Volts)} = \frac{T}{11,600} \text{ Volts, T in Kelvin}$$

At room temperature ($27^\circ C = 300 \text{ K}$), $V_T = 300/11,600 = 0.025862 \text{ V} = 26 \text{ mV}$

- The diode forward current increases exponentially with the applied voltage across the diode
- The following figure shows the V-I characteristics of Ge and Si P-N junction diodes

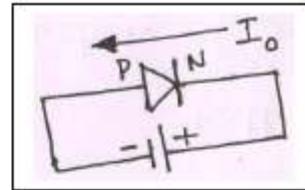


(Though figures are very essential in presentation, You should not take much time in drawing figures.

You should be able to draw each figure within a minute or two. It requires prior practice. Otherwise you will end up finding no time to attempt all questions. Do practice, drawing all figures!)

5. What is reverse saturation current (I_o)? Mention approximate order of I_o for Ge and Si diodes. Discuss the effect of temperature on I_o by writing necessary expression.

- When a diode is reversed biased, the current in the diode is due to minority carriers
- As the minority carriers are small in number in number, the diode current in reverse bias is very small. It is also called *reverse leakage current*.
- Reverse saturation current (I_o): At a given temperature, the minority carriers are fixed in number. Hence the diode reverse current will remain constant, even if the applied reverse bias voltage is increased. For this reason, the diode reverse current is also called reverse saturation current (I_o)



$$I_o = \begin{cases} \text{few } \mu\text{A, for Ge diodes} \\ \text{few nA, for Si diodes} \end{cases}$$

- The I_o is a temperature dependent parameter
- When temperature increases, more covalent bonds will be broken. Majority carriers will be drawn away from junction by applied reverse bias, whereas the barrier potential will help the minority carriers drift across the junction. This increases the reverse saturation current.
- Reverse saturation current doubles for every 10 °C rise in temperature

$$I_{o2} = I_{o1} \left(2^{\left(\frac{\Delta T}{10} \right)} \right); \quad \text{Where, } I_{o1} = \text{Reverse saturation current at temp } T_1 {}^\circ\text{C}$$

$$I_{o2} = \text{Reverse saturation current at temp } T_2 {}^\circ\text{C}, \quad \Delta T = (T_2 - T_1) {}^\circ\text{C}$$

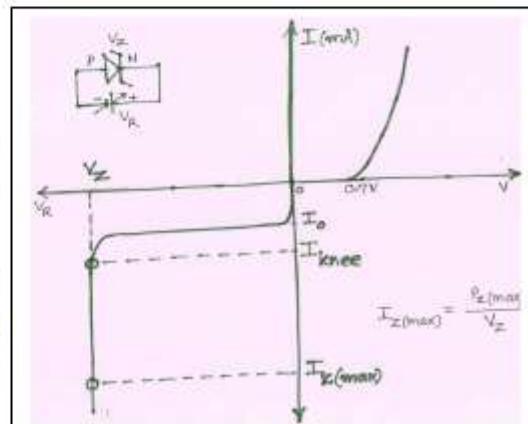
6. Explain breakdown mechanisms that occur in a p-n junction diode.

Refer to class notes ...

Points to be covered:

Breakdown:

- Some diodes are specially manufactured to breakdown when they are operated in reverse bias.
- When the applied reverse bias voltage exceeds the specified voltage, called breakdown voltage, the diode enters into breakdown mode.
- The figure shows typical V-I characteristic curves of a breakdown diode.



- In the breakdown mode, the voltage across the diode remains constant even if, the reverse current in the diode varies over fairly wide range.
- The manufacturer specifies the following details:
 - (i) Breakdown voltage of the diode (V_z)
 - (ii) Maximum power that the diode can dissipate ($P_{z(\max)}$), and
 - (iii) The minimum current to be maintained through the diode (I_{knee})

Breakdown mechanisms: (i) Zener mechanism, (ii) Avalanche mechanism

- Elaborate on Zener mechanism
- Elaborate on avalanche mechanism
- Draw neat diagrams showing the Zener and avalanche breakdown voltages
- Mention application:
 - Used in voltage regulators.
 - Draw the circuit schematic of Zener voltage regulator

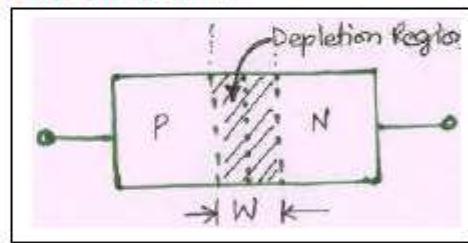
7. How many types of capacitances are associated with pn-junction? Explain which type of capacitance is important for forward and reverse bias modes of operation.

Refer to class notes...

Important Points...

Capacitance in P-N junction diode:

- The P and N regions are essentially low resistance areas due to high concentration of majority carriers.
- The depletion region, which is depleted of charge carriers, serves as an effective insulation.
- Hence, a diode has a very high resistance depletion region (Insulator) sandwiched between low resistive P and N regions
- The P and N regions act as plates of capacitor, while the depletion region acts as the insulating dielectric
- Thus a P-N junction diode can be compared to a charged capacitor and the capacitances associated with the P-N junction are : (i) Transition capacitance, (ii) Diffusion capacitance



Transition Capacitance (C_T):

- This is the capacitance of a reverse biased diode.
- It is also known as Space-charge capacitance or junction capacitance

- C_T is given by $C_T = \frac{\epsilon A}{W}$

Where ϵ = the permittivity of semiconductor material

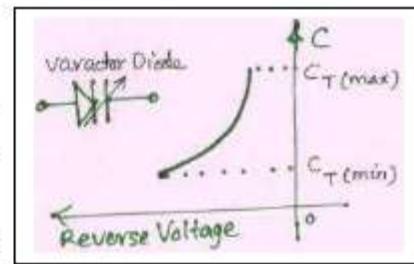
A = Cross-sectional area of junction

W = width of depletion region

- The C_T can be controlled by varying the width of depletion region (W). The W can be varied with the applied reverse bias voltage.
- As the reverse bias voltage increases, the W increases and hence C_T decreases and vice-versa.

Varactor Diodes or Vari-caps:

- The Si diodes designed for getting variable capacitance effects under reverse bias are called Varactor diodes. They are also called voltage variable capacitance diodes.
- The typical variation in capacitance that can be obtained is $2\text{-}12 \mu\text{F}$ and $20\text{-}28 \mu\text{F}$.



Diffusion Capacitance (C_D):

- This is the capacitance of a forward biased diode.
- During forward bias, the barrier width of the diode decreases.
- C_D is given by $C_D = \frac{\tau I}{\eta V_T}$

Where τ = mean life time the charge carrier

I = forward current through the diode (Amp)

$$\eta = \begin{cases} 1; & \text{for Ge} \\ 2; & \text{for Si} \end{cases}$$

$$V_T = \text{Volt equivalent of temperature (Volts)} = \frac{T}{11,600} \text{ Volts, T in Kelvin}$$

At room temperature ($27^{\circ}\text{C} = 300 \text{ K}$), $V_T = 300/11,600 = 0.025862 \text{ V} = 26 \text{ mV}$

- C_D of a forward biased diode \propto Diode forward current (I)
- C_D ranges from 10 to 1000 pF
- C_D of a forward biased diode $>>$ C_T of a reverse biased diode

8. Explain the phenomenon of Hall Effect. Mention its applications.

Refer to class notes

Hints:

Hall effect: statement

When a current carrying conductor is placed in a transverse magnetic field (\vec{B}), an electric field (\vec{E}) is induced perpendicular to \vec{I} and \vec{B}

Derivation for Hall coefficient: Refer to class notes....

$$R_H = \frac{V_H W}{B I}$$

Applications of Hall effect: Hall effect finds very useful applications in electronics

- Identification semiconductor as P-type or N-type
- Measurement of carrier concentrations in a semiconductor
- Measurement of mobility of electrons and holes in a semiconductor
- Magnetic field meter
- Hall effect Multiplier

Refer to class notes for details on above listed applications

9. For what value of voltage will the reverse current (I_o) in a p-n junction Ge diode reach 90% of its saturation value at room temperature?

The value of Voltage at which the reverse current in Ge reaches 90% of its saturation value at room temperature.

$$-0.9 I_o = I_o (e^{\frac{V}{nV_T}} - 1)$$

$$0.9 = e^{\frac{V}{nV_T}} \quad n=1 \Rightarrow V_T = 0.026$$

$$0.9 = e^{\frac{V}{0.026}}$$

Taking \ln on both sides

$$\ln(0.9) = \frac{V}{0.026}$$

$$\therefore V = 0.026 (\ln(0.9))$$

$$= -0.30 (0.026)$$

$$\therefore \underline{-0.0698} \underline{3-0.06V}$$

10. A Si diode operates at a forward voltage of 0.6V. Calculate the factor by which the current will be multiplied when the temperature changes from $25^{\circ}C$ to $150^{\circ}C$.

Factor by which the current gets multiplied
in a diode when temp. changes from
 $(298^{\circ}K)$ to $(423^{\circ}K)$. $\left[\frac{I_{25}}{I_{150}} \right]$
 $V_f = 0.4V \quad I = I_0 e^{v/kT}$

when temperature changes, I₀ changes &
 v/k changes.

$$I_{150} = I_{0(25)} \left(e^{\frac{(T_2 - T_1)}{298}} \right)$$

$$= I_{0(25)} (2^{12.5})$$

$$\approx 5792.6 (I_{0(25)})$$

$$V_T \text{ at } 423^{\circ}K = \frac{T}{11,600} = \frac{423}{11,600} = 0.0365V$$

$$V_T \text{ at } 298^{\circ}K = \frac{T}{11,600} = \frac{298}{11,600} = 0.0259V$$

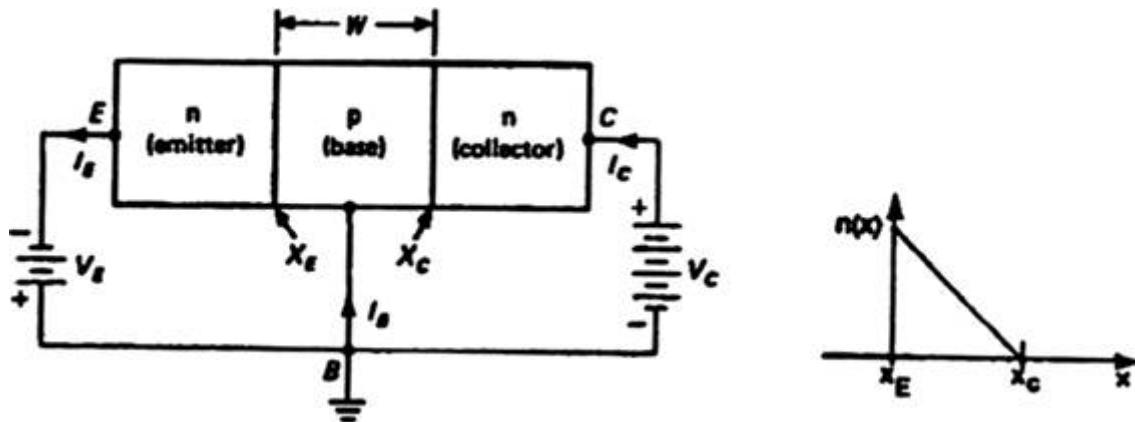
$$\frac{I_{25}}{I_{150}} = \frac{I_{0(25)} (e^{v/kT} - 1)}{I_{0(150)} (e^{v/kT} - 1)}$$

$$= \frac{I_{0(25)} (e^{0.4/2(0.0259)} - 1)}{5792.6 (I_{0(25)}) (e^{0.4/2(0.0365)} - 1)}$$

$$= \frac{2396.3}{(5792.6)(229.7)} = 1.73 \times 10^{-3}$$

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PROBLEM 01 – 0032: The p-type base region of an n–p–n bipolar silicon transistor of the type shown below has a width of 2.0×10^{-6} m and is doped with 1.0×10^{21} acceptors/m³. Electrons are injected into this region from the emitter at x_E , producing a uniform gradient of electrons there. The electron concentration drops to zero at the collector at x_c . If 2.0×10^{20} electrons/m³ are present at the emitter edge of the base region (x_E), calculate the diffusion current density of electrons through this base region under steady-state conditions. What electric field must be present in this base region to yield an electron drift current density just equal to the diffusion current density just calculated? Determine the voltage drop across the base width corresponding to this field.



Solution:

From Einstein relation for electrons,

$$\begin{aligned} D_n &= (kT / q) \mu_n \\ &= 0.026 \text{ V}^{-1} (0.14 \text{ m}^2 / \text{V-sec}) \\ &= 0.0036 \text{ m}^2 / \text{sec}, \end{aligned}$$

Here k is the gas constant, q the electronic charge, and T the absolute temperature. μ_n is the electron mobility and $\mu_n = 0.14 \text{ m}^2 / \text{V-sec}$ for the element silicon.

$$\begin{aligned} (J_n)_{\text{diffusion}} &= qD_n (dn / dx) \\ &= 1.6 \times 10^{-19} \text{ C}(0.0036 \text{ m}^2/\text{sec})[\{2.0 \times 10^{20}\} / \{2.0 \times 10^{-6}\}] \text{ m}^{-4} \\ &= 5.8 \times 10^4 \text{ A/m}^2. \end{aligned}$$

$$(J_n)_{\text{drift}} = qn\mu_n\varepsilon = (J_n)_{\text{diffusion}}$$

Hence,

$$\varepsilon = [(J_n)_{\text{diffusion}}] / [qn\mu_n]$$

$$5.8 \times 10^4 \text{ A/m}^2 = 1.6 \times 10^{-19} \text{ C}(1.0 \times 10^{21} \text{ m}^{-3})(0.14 \text{ m}^2 / \text{V-sec})(\varepsilon) \text{ V/m}$$

$$\varepsilon = 2.6 \times 10^3 \text{ V/m.}$$

$$\begin{aligned} \text{The voltage drop is } V &= \varepsilon W = 2.6 \times 10^3 (2.0 \times 10^{-6}) \\ &= 5.2 \times 10^{-3} \text{ V.} \end{aligned}$$

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- PROBLEM 01 – 0033: A silicon p⁺-n-p transistor has a base width of 2.0×10^{-6} m and base resistivity of $0.0010 \Omega\text{-m}$. The hole lifetime in the base region is $0.10 \mu\text{sec}$. The emitter region has thickness 1.0×10^{-6} m and resistivity $0.000010 \Omega\text{-m}$. The emitter and collector areas are both $2.5 \times 10^{-9} \text{ m}^2$.
- a) Show that the component of the base current necessary for supplying electrons for recombining holes in the base region is small compared to the collector current.
- b) Calculate the injection efficiency of holes for the emitter of this transistor.

Solution:

a) It seems reasonable to assume that if small base current is needed for recombining holes in the base, then the diffusion length L_p ought to be much larger than the base width. It can be shown that if the electron current for recombining holes is negligible, it is necessary that $(W^2 / 2L_p^2) \ll 1$, where $L_p^2 = D_p \tau_p$. Now

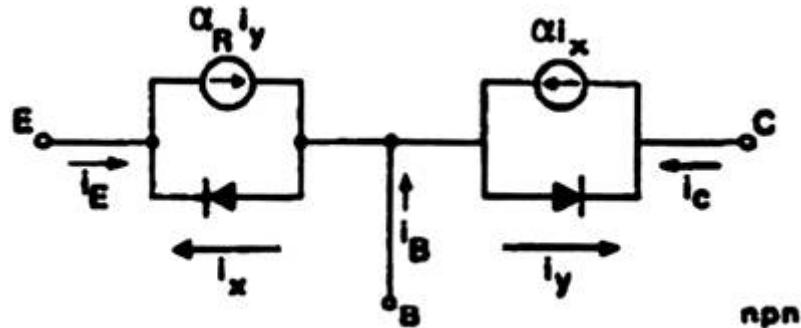
$$(W^2 / 2L_p^2) = [\{(2.0 \times 10^{-6})^2 \text{ m}^2\} / \{2(1.25 \times 10^{-3} \text{ m}^2/\text{sec})(1.0 \times 10^{-7} \text{ sec})\}] \\ = 1.6 \times 10^{-2} \ll 1.$$

b) The injection efficiency is given by

$$\gamma = [1 / \{1 + \sigma_n W / \sigma_p W_E\}] \\ = [1 / \{1 + [1 / (0.0010)](\Omega\text{-m})^{-1} (2.0 \times 10^{-6} \text{ m}) \\ / [1 / (0.000010)](\Omega\text{-m})^{-1}(1.0 \times 10^{-6} \text{ m})\}] \\ = [1 / \{1 + 2.0 \times 10^{-2}\}] = 0.98 \quad \text{or} \quad 98 \text{ percent.}$$

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PROBLEM 01 – 0034: For an npn transistor, find i_B in terms of v_{BC} and i_C using the Ebers–Moll model.



Solution:

The Ebers–Moll model is shown. The currents through the diodes are given conventionally by

$$i_x = I_{ES}[\exp\{qv_{BE}/(kT)\} - 1] \quad (1)$$

$$i_y = I_{CS}[\exp\{qv_{BC}/(kT)\} - 1] \quad (2)$$

and the other currents are

$$i_E = \alpha_R i_y - i_x \quad (3)$$

$$i_C = \alpha i_x - i_y \quad (4)$$

$$i_B = -i_E - i_C \quad (5)$$

It is desired to find an expression for i_B that contains only v_{BC} and i_C as terminal variables. From Eq. (4),

$$i_x = [i_C + i_y] / \{\alpha\} \quad (6)$$

and substitution in Eq. (3) gives

$$i_E = \alpha_R i_y - [i_C + i_y] / \{\alpha\} \quad (7)$$

or

$$i_E = \alpha_R I_{CS}[\exp(qv_{BC}/kT) - 1] - [i_C + I_{CS}[\exp(qv_{BC}/kT) - 1]] / \alpha \quad (8)$$

We substitute this value for i_E into Eq. (5) and gather terms to obtain

$$\begin{aligned} i_B &= -i_E - i_C \\ &= [(1 - \alpha) / \alpha] i_C + [1 - \alpha \alpha_R] / \alpha I_{CS} [\exp(qv_{BC}/kT) - 1] \end{aligned} \quad (9)$$

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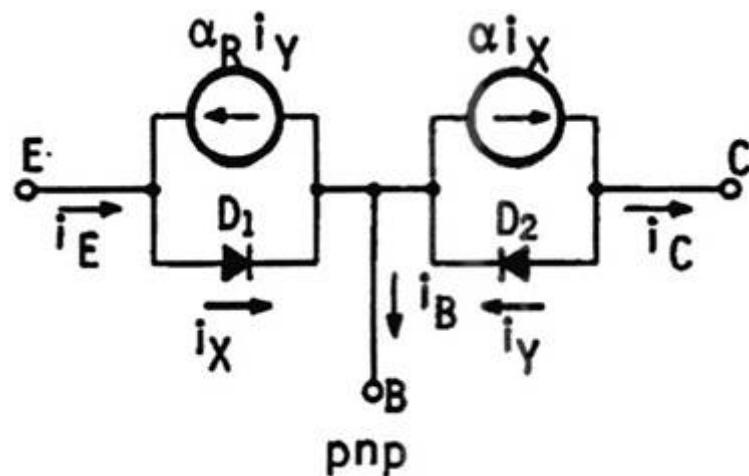
PROBLEM 01 – 0035: A pnp transistor has $\alpha = \alpha_R = 0.9$ and $I_{CO} = I_{EO} = 10 \mu\text{A}$ at room temperature.

a) Find the collector current when the transistor is off.

Assume that for an off transistor, v_{EB} and v_{CB} are large and negative with respect to kT/q . (At $T = 25^\circ\text{C}$, $kT/q \approx 0.025 \text{ V}$.)

b) Find the collector current when the transistor is on.

Assume that for an on transistor $v_{EB} = 0.25 \text{ V}$ and v_{CB} is large and negative.



Solution:

The Ebers–Moll model for a pnp transistor is shown. When C is open and EB is reverse-biased, the currents are defined as $i_E = I_{EO}$ and $i_x = I_{ES}$. When E is open and CB is reverse-biased, the currents are $i_C = I_{CO}$ and $i_y = I_{CS}$. When C is open, we have the equations

$$i_y = \alpha i_x = \alpha I_{ES}$$

$$i_E = I_{EO} = i_x - \alpha R i_y$$

$$\text{Thus } I_{EO} = I_{ES}(1 - \alpha \alpha_R) \quad (1)$$

Similarly, from the case where E is open,

$$I_{CO} = I_{CS}(1 - \alpha \alpha_R) \quad (2)$$

The current through any diode is given by

$$i_D = I_{DO} (e^{qv/kT} - 1)$$

where I_{DO} is the reverse-bias current, v is the voltage across the diode, and q/kT is a temperature-dependent constant. Therefore, from the figure and the definitions of I_{ES} and I_{CS} , we have

$$i_x = I_{ES} (e^{[q(v)EB] / kT} - 1)$$

$$i_y = I_{CS} (e^{[q(v)CB] / kT} - 1)$$

and so

$$i_E = I_{ES} (e^{[q(v)EB] / kT} - 1) - \alpha R I_{CS} (e^{[q(v)CB] / kT} - 1) \quad (3)$$

$$i_C = \alpha I_{ES} (e^{[q(v)EB] / kT} - 1) - I_{CS} (e^{[q(v)CB] / kT} - 1) \quad (4)$$

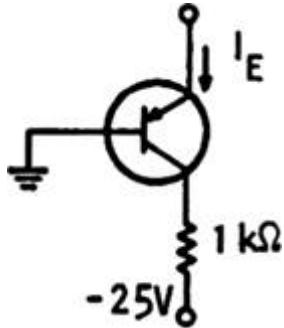
a) The solution is obtained directly from the second Ebers–Moll equation, eq. 4.

$$i_C = \alpha I_{ES} (e^{[q(v)EB] / kT} - 1) - I_{CS} (e^{[q(v)CB] / kT} - 1)$$

Since both v_{EB} and $v_{CB} \ll kT/q$, each expression in parentheses reduces to -1 , and so

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- PROBLEM 01 – 0036: The transistor in the circuit shown has $\alpha_0 = 0.9$ and $I_{EO} = I_{CO} = 10 \mu\text{A}$.
- Find the critical emitter current that just saturates the transistor.
 - Determine the saturation voltage and its polarity.



Solution:

a) With the E–B junction forward biased, the transistor will just enter saturation when the C–B junction (which was assumed to have been reverse biased) just becomes forward biased, i.e. when $V_{CB} = 0$, which with $v_B = V_B = 0 \text{ V}$ requires $V_C = 0 \text{ V}$. The collector current is given by $I_C = [(V_C + 25) / 1]$. As I_E is increased, I_C increases. The I_C required to raise V_C to 0 is $I_C = [(V_C + 25) / 1] = 25 \text{ mA}$. The corresponding input emitter current needed is $I_E = [I_C / \alpha_0] = 27.8 \text{ mA}$.

b) The Ebers–Moll equations for a pnp transistor are

$$i_E = [1 / (1 - \alpha\alpha_R)] [i_{EO} (e^{[q(v)EB] / kT} - 1) - \alpha_R I_{CO} (e^{[q(v)CB] / kT} - 1)] \quad (1)$$

$$i_C = [1 / (1 - \alpha\alpha_R)] [\alpha i_{EO} (e^{[q(v)EB] / kT} - 1) - I_{CO} (e^{[q(v)CB] / kT} - 1)] \quad (2)$$

Equations 1 and 2 may be solved simultaneously for v_{EB} and v_{CB} . If i_E and i_C are both considered in absolute value, the junction voltages are given by

$$v_{EB} = (kT / q) \ln [1 + \{(i_E \alpha_R i_C) / (I_{EO})\}] \quad (3)$$

$$v_{CB} = (kT / q) \ln [1 + \{(-i_C + \alpha i_E) / (I_{CO})\}] \quad (4)$$

The saturation voltage is $v_{CE} = v_{CB} = v_C - v_E$. By definition of the edge of saturation $v_{CB} = 0$ which, with $v_B = 0$ reduces to $v_C = 0$. In this case the saturation voltage $v_{CE} = -v_E$. Substitution into eq. 3 yields

$$V_{EB} = V_E = 40 \ln (1 + 528) = 163 \text{ mV}$$

from which the saturation voltage is $v_{CE} = -0.163 \text{ V}$ or $v_E > v_C$ for a pnp transistor at the edge of saturation.

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PROBLEM 01 – 0037: Establish that the transistor in the circuit in Fig. 1 is operating in the active mode. Assume that β equals 99 for this transistor. Find i_B and i_C .

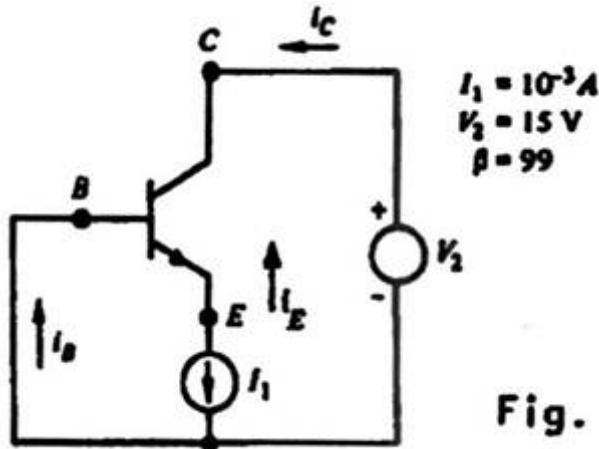


Fig. 1

Solution:

In the active mode the emitter-base junction is forward biased and the collector-base junction reverse biased. The current source I_1 causes a negative emitter current to flow. The base-emitter junction resembles a diode, so that

$$i_E \approx -I_{ES}[\exp\{(qV_{BE}) / (kT)\} - 1]$$

where I_E is considered as flowing into the emitter. Since, as we said, I_E is negative, then the exponential term must be greater than 1, and therefore V_{BE} must be positive, and so forward-biased. The collector-base voltage is simply V_2 . Hence the collector junction is reverse biased by 15 volts.

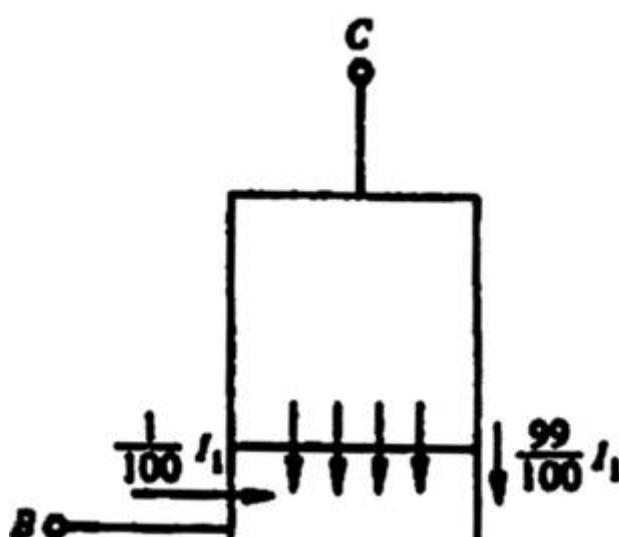
With the emitter-base junction forward biased, and the collector-base junction reverse biased, the transistor is indeed operating in the active region. We may solve for i_B

$$i_B = -[\{i_E\} / \{\beta + 1\}] = -[\{-I_1\} / \{\beta + 1\}]$$

$$i_B = -[-10^{-3}] / \{100\} = 10^{-5} \text{ A}$$

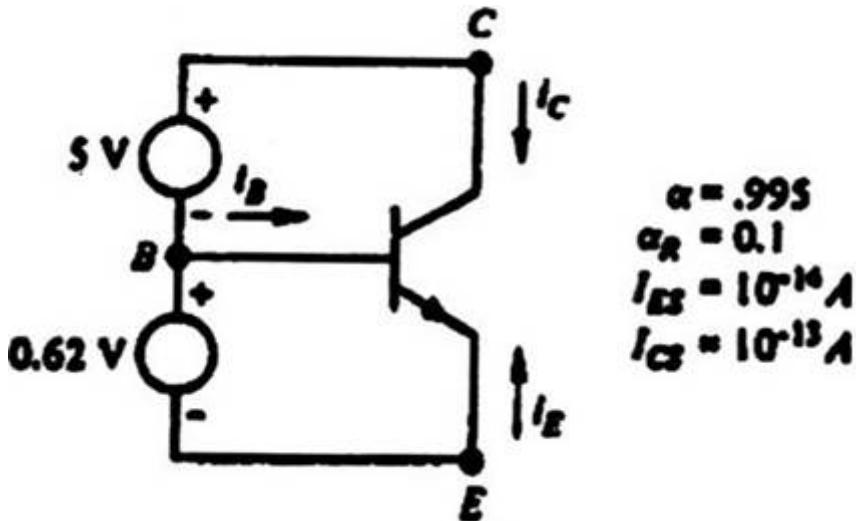
We may also find i_C

$$i_C = \beta i_B$$



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PROBLEM 01 – 0038: The transistor below has voltage sources applied between emitter and base and between base and collector; thus v_{BE} and v_{BC} are specified. Determine v_{CE} , i_E , i_B and i_C .



Solution:

First, by a direct addition of voltages, $v_{CE} = 5.62$ V. To solve for i_C and i_E , we simply evaluate the following two equations governing i_C and i_E of a n-p-n transistor in the active region:

$$i_C = \alpha I_{ES} [\exp \{(qv_{BE}) / kT\} - 1] - I_{CS} [\exp \{(qv_{BC}) / kT\} - 1] \quad (1)$$

$$i_E = - I_{ES} [\exp \{(qv_{BE}) / kT\} - 1] + \alpha_R I_{CS} [\exp \{(qv_{BC}) / kT\} - 1] \quad (2)$$

At room temperature $kT/q = 0.026$ V. From equation (1)

$$i_C = 0.995 \times 10^{-14} \times [\exp(0.62 / 0.026) - 1] - 10^{-13} [\exp(-5.0) / 0.026 - 1]$$

$$= 0.995 \times 10^{-14} \times 2.3 \times 10^{-10} + 10^{-13}$$

$$i_C = 2.3 \times 10^{-4} A$$

From Equation (2)

$$i_E = - 10^{-14} (2.3 \times 10^{10}) - 10^{-14}$$

$$i_E = - 2.3 \times 10^{-4} A$$

We obtain i_B by subtraction, that is

$$i_B = - i_C - i_E \cong 0$$

Now in reality i_B is not zero; the error stems from the approximation that

$0.995 \times 2.3 \times 10^{-14} \times 10^{10}$ equals 2.3×10^{-4} in calculating i_C . Thus

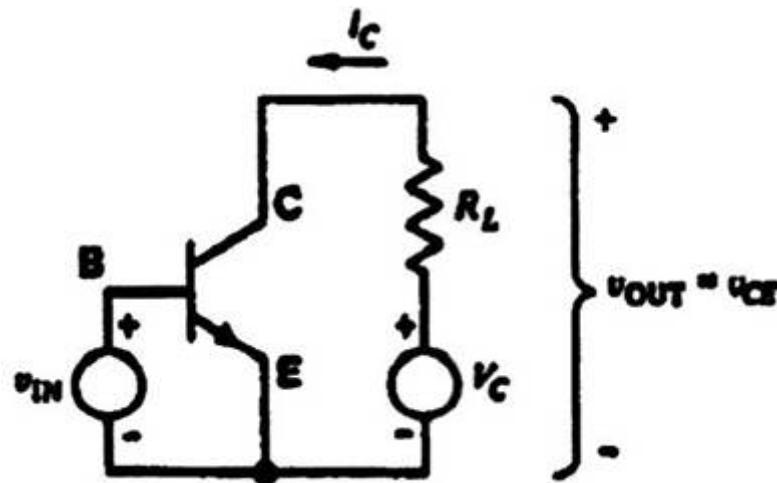
$$i_B = - 0.995 \times 2.3 \times 10^{-4} + 2.3 \times 10^{-4}$$

$$i_B = 1.15 \times 10^{-6} A$$

For the values $v_{BC} = -5$ V, $v_{BE} = 0.62$ V.

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PROBLEM 01 – 0039: The transistor in the following circuit is operating in the active mode. Find the base current, collector current, and collector-to-emitter voltage, assuming that $I_{ES} = 10^{-14}$ A. Find the change in collector-to-emitter voltage assuming that the input voltage increases by 0.018 V. $v_{IN} = 0.7$ V; $R_L = 1000 \Omega$; $V_C = 15$ V; $\beta = 200$; $kT/q = 0.026$ V. (This value corresponds to $T = 300^\circ\text{K}$, that is, room temperature.)



Solution:

The emitter-base junction is forward biased by 0.7 V. Furthermore the emitter current is related to the emitter-base voltage by the relationship

$$i_E = -I_{ES}[\exp\{(qv_{BE}) / (kT)\} - 1] \quad (\text{npn}) \quad (1)$$

Hence,

$$i_E = -10^{-14} \exp\{(0.7) / (0.026)\} = -5 \times 10^{-3} \text{ A}$$

Since $\beta = 200$, alpha is close to one, in fact, $\alpha = [\beta / (1 + \beta)] = 0.995$. Thus i_C is nearly equal in magnitude to i_E , that is, $i_C \approx 5 \times 10^{-3}$ A. We can solve for v_{CE} by a single loop equation:

$$v_{CE} - V_C + i_C R_L = 0$$

Thus

$$v_{CE} = 15 - 5 \times 10^{-3} \times 1000 = 10 \text{ V}$$

This voltage is sufficient to assure that the transistor is indeed biased in the active region because $v_{CB} = v_{CE} - v_{BE} = 9.3$ V, and the collector-base junction is therefore reverse biased. The base current is given by

$$(i_C / \beta) = 2.5 \times 10^{-5} \text{ A}$$

We now recompute the output voltage with an 18-mV increase in the input voltage. Such an increase approximately doubles the emitter current.

$$i_E = -10^{-14} \exp\{(0.718) / (0.026)\} = -10^{-2} \text{ A}$$

Therefore the base current and collector current double. From the loop equation given above $v_{CE} = 15 - 10^{-2} \times 10^3 = 5$ V. (Note that the transistor remains in the active mode.) It is interesting that for a change in v_{BE} of 0.018 V, there is a change in v_{CE} of -5 V. That is, input voltages are multiplied by a factor of $[(-5) / (0.018)] = -280$.

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PROBLEM 01 – 0040: The measured collector and base currents of a certain transistor are

$$I_C = 5.202 \text{ mA}, I_B = 50 \mu\text{A}, I_{CBO} = 2 \mu\text{A}$$

(a) Calculate α_{dc} , β_{dc} , and I_E .

(b) Find the new level of I_B required to make $I_C = 10 \text{ mA}$.

Solution:

(a) In a transistor,

$$I_C = \alpha_{dc} I_E + I_{CBO} \quad (I_{CBO} \text{ is the collector leakage current})$$

and

$$I_E = I_B + I_C$$

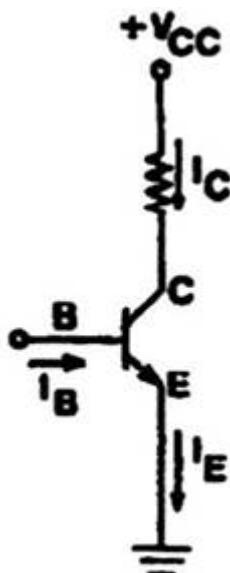
Substituting and solving for I_C , we have

$$I_C = [\{\alpha_{dc}\} / \{1 - \alpha_{dc}\}] I_B + [1 / \{1 - \alpha_{dc}\}] I_{CBO}$$

or since

$$\beta_{dc} = [\{\alpha_{dc}\} / \{1 - \alpha_{dc}\}],$$

$$I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO}.$$



$$\begin{aligned} \text{Thus, } 5.202 \text{ mA} &= (\beta_{dc} \times 50 \mu\text{A}) + (\beta_{dc} + 1)2 \mu\text{A} \\ &= \beta_{dc} (50 \mu\text{A} + 2 \mu\text{A}) + 2 \mu\text{A} \end{aligned}$$

and

$$\beta_{dc} = [\{5.202 \text{ mA} - 2 \mu\text{A}\} / \{52 \mu\text{A}\}] = 100$$

$$I_E = I_C + I_B.$$

$$\text{Therefore, } I_E = 5.202 \text{ mA} + 50 \mu\text{A} = 5.252 \text{ mA}$$

$$I_C = \alpha_{dc} I_E + I_{CBO}.$$

$$\text{Thus, } 5.202 \text{ mA} = (\alpha_{dc} \times 5.252 \text{ mA}) + 2 \mu\text{A}$$

$$\alpha_{dc} = [\{5.202 \text{ mA} - 2 \mu\text{A}\} / \{5.252 \text{ mA}\}] = 0.99$$

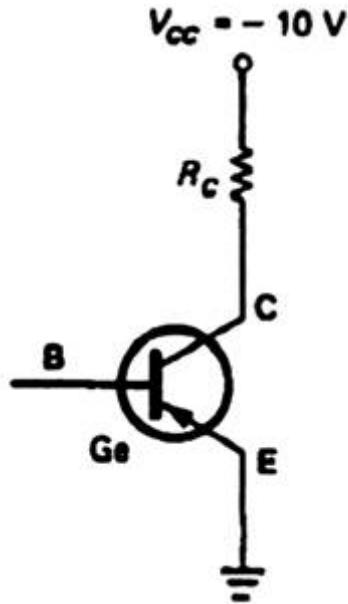
$$(b) \quad I_C = \beta_{dc} I_B + (\beta_{dc} + 1) I_{CBO}.$$

$$\text{Therefore, } 10 \text{ mA} = (100 \times I_B) + (101 \times 2 \mu\text{A})$$

$$I_B = [\{10 \text{ mA} - 202 \mu\text{A}\} / \{100\}] = 97.98 \mu\text{A}$$

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PROBLEM 01 – 0041: The transistor in the circuit shown has a maximum I_{CBO} specified at $5 \mu\text{A}$ and a beta of $25 \text{ min}, 180 \text{ max}$. Find a value of collector resistor which will ensure that the collector voltage does not drop below 9 V with the base open-circuited.



Solution: The maximum I_{CEO} leakage current is

$$I_{CEO} = \beta I_{CBO} = 180 \times 5 \mu\text{A} = 900 \mu\text{A} = 0.9 \text{ mA}$$

The maximum allowable voltage drop across R_C is $10 - 9 = 1 \text{ V}$:

$$R_C = (V/I) = [1 \text{ V} / 0.9 \text{ mA}] = 1.1. \text{ K}$$

A 1-K resistor would be used at R_C .

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- PROBLEM 01 – 0042: A transistor has the CE output characteristics drawn in Figure 2.
- Find I_C and V_{CE} for $I_B = 50 \mu\text{A}$, with $V_{CC} = 12 \text{ V}$ and $R_C = 1 \text{ k}\Omega$.
 - Repeat using $I_B = 0$.
 - Repeat using $I_B = 125 \mu\text{A}$ and $I_B = 150 \mu\text{A}$.
- For each case, in which mode is the transistor operating?

Solution:

a) The load-line equation is

$$12 \text{ V} = I_C \times 1 \text{ k}\Omega + V_{CE}$$

and is plotted as shown in Figure 2. The intersection of this load line and the $I_B = 50 \mu\text{A}$ curve is thus $I_C = 5 \text{ mA}$ and $V_{CE} = 7 \text{ V}$. The voltage across the $1\text{-k}\Omega$ resistor is $5 \text{ mA} \times 1 \text{ k}\Omega = 5 \text{ V}$. These values can be checked by substituting into the load-line equation. In this case, the operating point lies in the active region of the transistor characteristics.

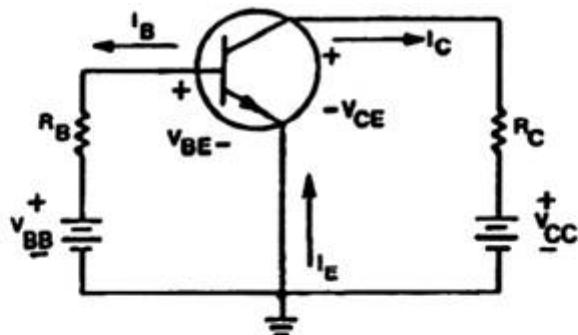


Fig. 1

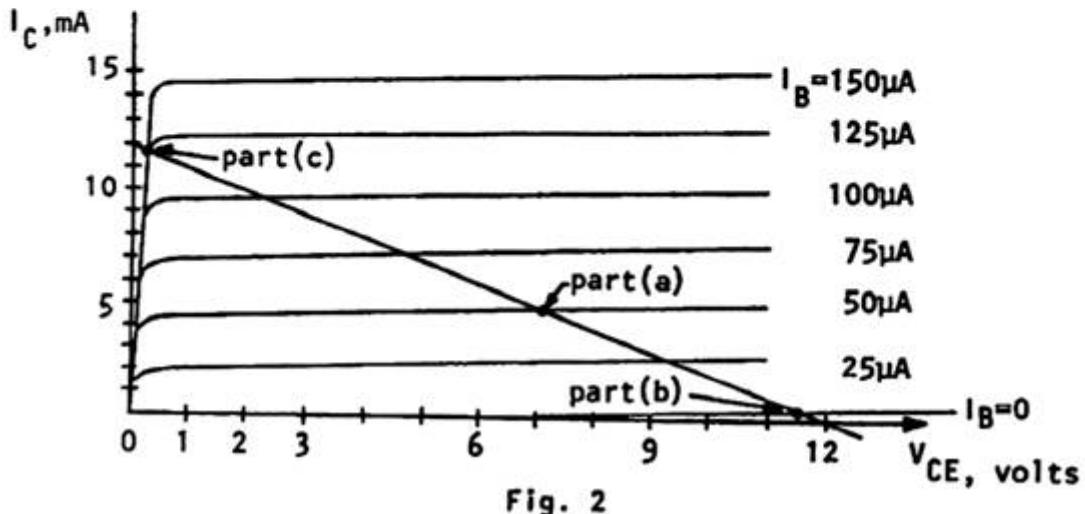


Fig. 2

- The intersection of the load line and the $I_B = 0$ curve gives the new operating point as $I_C \approx 0$ and $V_{CE} = 12 \text{ V}$. Since the transistor is in cutoff, only a small leakage current (I_{CEO}) flows and the voltage dropped across the series resistor is essentially zero. Thus $V_{CE} = V_{CC}$.
- The intersection of the load line and the $I_B = 125 \mu\text{A}$ curve gives the operating point as $I_C = 11.8 \text{ mA}$ and $V_{CE} = 0.2 \text{ V}$. This operating point lies

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PROBLEM 01 – 0043: The silicon transistor of Figure 1 has the output characteristic curves drawn in Figure 2.

- Find I_C and V_{CB} for $I_E = 20 \text{ mA}$ if $V_{CC} = 40 \text{ volts}$ and $R_C = 1.6 \text{ k}\Omega$.
- Repeat using $I_E = 0$.
- Repeat for $I_E = 30 \text{ mA}$ and $I_E = 40 \text{ mA}$.

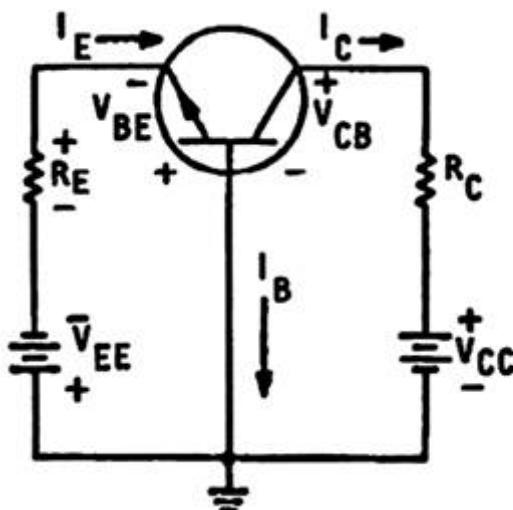


Fig. 1

Solution:

- a) The load-line equation is $40 \text{ V} = I_C \times 1.6 \text{ k}\Omega + V_{CB}$. The plot of this line on the characteristic curves is shown in Figure 2. Note that the two points used to plot the load line are $(I_C = 0, V_{CB} = 40 \text{ V})$ and $(I_C = 40 \text{ V}/1.6 \text{ k}\Omega = 25 \text{ mA}, V_{CB} = 0)$.

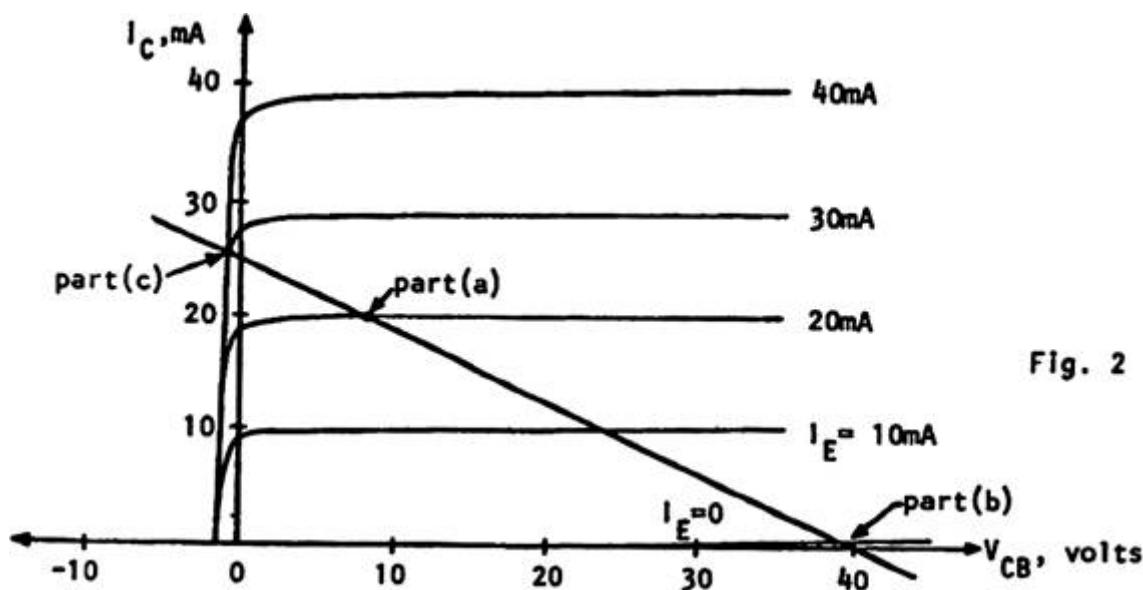
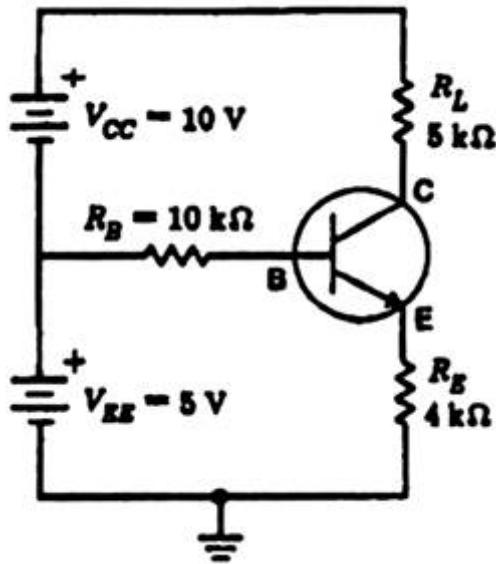


Fig. 2

The intersection of this load line and the output curve for $I_E = 20 \text{ mA}$ is the operating point. It is seen to be $I_C = 19.5 \text{ mA}$ and $V_{CB} = 8.8 \text{ volts}$. The voltage across the $1.6\text{-k}\Omega$ resistor is $19.5 \text{ mA} \times 1.6 \text{ k}\Omega = 31.2 \text{ V}$. This can be checked by substituting these values into the load-line equation. In this case, the operating point lies in the active region of the transistor.

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PROBLEM 01 – 0044: Find the V_{CE} for the circuit shown. Neglect V_{BE} .



Solution:

1. Find I_E

$$I_E = [(V_{EE}) / (R_E)] = [(5 \text{ V}) / (4 \text{ k}\Omega)] = 1.25 \text{ mA}$$

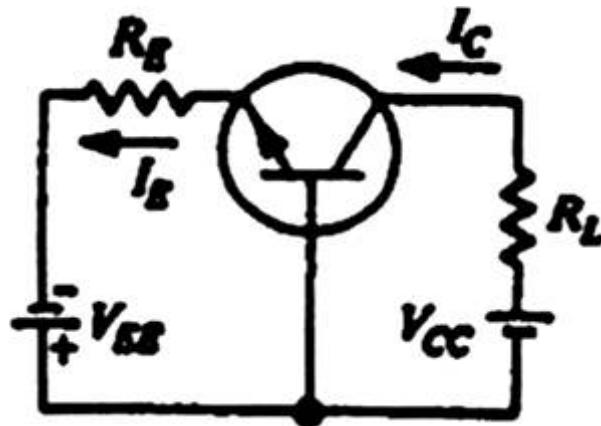
2. Find V_{CE}

$$V_{CE} = V_{CC} - I_E R_L = 10 \text{ V} - (1.25 \text{ mA}) 5 \text{ k}\Omega$$

$$V_{CE} = 10 \text{ V} - 6.25 \text{ V} = 3.75 \text{ V}$$

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PROBLEM 01 – 0045: In the circuit shown, I_E is chosen to be 2.0 mA. If $V_{EE} = 12.0$ volts, $V_{CC} = 12.0$ volts, and $R_L = 5.0 \text{ k}\Omega$, determine (a) R_E , (b) I_C , (c) $I_C R_L$, and (d) V_{CB} .



Solution:

- (a) $R_E \approx [V_{EE} / I_E] = [12 / 2(10^{-3})] = 6 \text{ k}\Omega$
- (b) $I_C \approx I_E \approx 2 \text{ mA}$
- (c) $I_C R_L = 2.0(10^{-3})(5.0)(10^3) = 10 \text{ volts}$
- (d) $V_{CB} = V_{CC} - I_C R_L = 12 - 10 = 2.0 \text{ volts}$

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- PROBLEM 01 – 0046: (a) Find the transistor currents in the circuit of Fig. 1. A silicon transistor with $\beta = 100$ and $I_{CO} = 20 \text{ nA} = 2 \times 10^{-5} \text{ mA}$ is used.
 (b) Repeat part (a) if a $2\text{-k}\Omega$ emitter resistor is added to the circuit, as in Fig. 2.

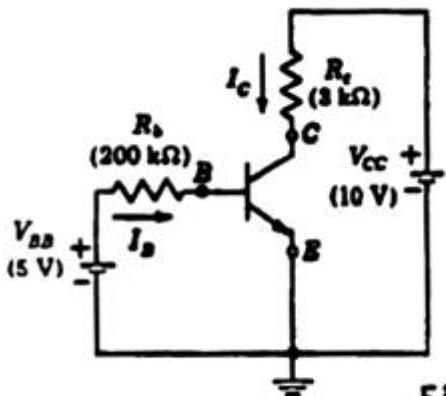


Fig. 1

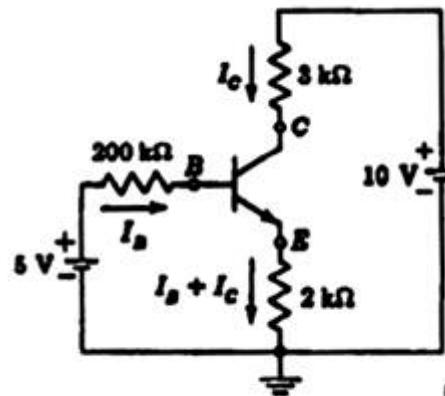


Fig. 2

Solution:

(a) Since the base is forward-biased, the transistor is not cut off. Hence it must be either in its active region or in saturation. Assume that the transistor operates in the active region. From KVL applied to the base circuit of Fig. 1 (with I_B expressed in milli-amperes), we have

$$-5 + 200 I_B + V_{BE} = 0$$

A reasonable value for V_{BE} is 0.7 V in the active region, and hence

$$I_B = [5 - 0.7] / 200 = 0.0215 \text{ mA}$$

Since $I_{CO} \ll I_B$, then $I_C \approx \beta I_B = 2.15 \text{ mA}$.

We must now justify our assumption that the transistor is in the active region, by verifying that the collector junction is reverse-biased. From KVL applied to the collector circuit we obtain

$$-10 + 3 I_C + V_{CB} + V_{BE} = 0$$

or

$$V_{CB} = 10 - (3)(2.15) - 0.7 = +2.85 \text{ V}$$

For an n-p-n device a positive value of V_{CB} represents a reverse-biased collector junction, and hence the transistor is indeed in its active region. Note that I_B and I_C in the active region are independent of the collector circuit resistance R_C . Hence, if R_C is increased sufficiently above 3 kΩ, then V_{CB} changes from a positive to a negative value, indicating that the transistor is no longer in its active region.

(b) The current in the emitter resistor of Fig. 2 is

$$I_B + I_C \approx I_B + \beta I_B = 101 I_B$$

assuming $I_{CO} \ll I_B$. Applying KVL to the base circuit yields

$$-5 + 200 I_B + 0.7 + (2)(101 I_B) = 0$$

or

$$I_B = 0.0107 \text{ mA} \quad I_C = 100 I_B = 1.07 \text{ mA}$$

Note that $I_{CO} = 2 \times 10^{-5} \text{ mA} \ll I_B$, as assumed.

To check for active circuit operation, we calculate V_{CB} . Thus

$$V_{CB} = -3 I_C + 10 - (2)(101 I_B) - 0.7$$

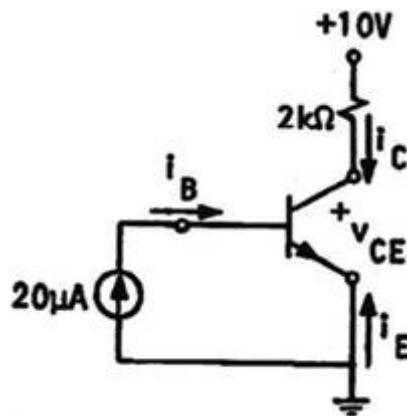
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PROBLEM 01 – 0047: A silicon npn transistor with $\alpha = 0.99$ and $I_{CBO} = 10^{-11}$ A is connected as shown. Predict i_C , i_E , and v_{CE} , (Note: It is convenient and customary in drawing electronic circuits to omit the battery, which is assumed to be connected between the +10-V terminal and ground.)

Solution:

For this transistor,

$$\beta = [\alpha / (1 - \alpha)] = [(0.99) / (1 - 0.99)] = [(0.99) / (0.01)] = 99$$



and the collector cutoff current is

$$I_{CEO} = (1 + \beta)I_{CBO} = (1 + 99) 10^{-11} = 10^{-9} \text{ A}$$

The collector current is

$$i_C = \beta i_B + I_{CEO} = 99 \times 2 \times 10^{-5} + 10^{-9} \cong 1.98 \text{ mA}$$

As expected for a silicon transistor, I_{CEO} is a very small part of i_C .

The emitter current is

$$i_E = -(i_B + i_C) = -(0.02 + 1.98)10^{-3} = -2 \text{ mA}$$

The collector-emitter voltage is

$$v_{CE} = 10 - i_C R_C \cong 10 - 2 \text{ (mA)} \times 2 \text{ (k}\Omega\text{)} = 6 \text{ V}$$

Since $v_{CB} = v_{CE} - v_{BE} \cong 6 - 0.7 = +5.3$ V, the collector-base junction is reverse biased.

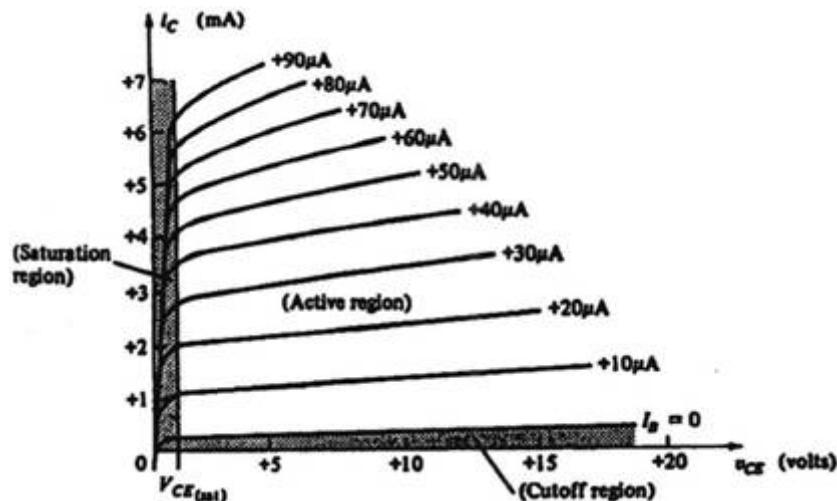
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- PROBLEM 01 – 0048: (a) Find the dc beta at an operating point of $V_{CE} = +10$ V and $I_C = +3$ mA on the characteristics given.
 (b) Find the value of α corresponding with this operating point.
 (c) At $V_{CE} = +10$ V find the corresponding value of I_{CEO} .
 (d) Calculate the approximate value of I_{CBO} using the β_{dc} obtained in part (a).

Solution: (a) At the intersection of $V_{CE} = +10$ V and $I_C = +3$ mA, $I_B = +25 \mu A$, so that

$$\beta_{dc} = (I_C / I_B) = [(3 \times 10^{-3}) / (25 \times 10^{-6})] = 120$$

$$(b) \alpha = [\beta / (\beta + 1)] = (120 / 121) \cong 0.992$$



- (c) I_{CEO} is the emitter current (equal to the collector current) that flows when $I_B = 0$. From the characteristics, we find

$$I_{CEO} = 300 \mu A$$

$$(d) I_{CBO} \cong (I_{CEO} / \beta) = [(300 \mu A) / 120] = 2.5 \mu A$$

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PROBLEM 01 – 0049: A silicon transistor is used in the circuit shown. If V_{BB} is 4 volts, and $I_B = 50 \mu\text{A}$,

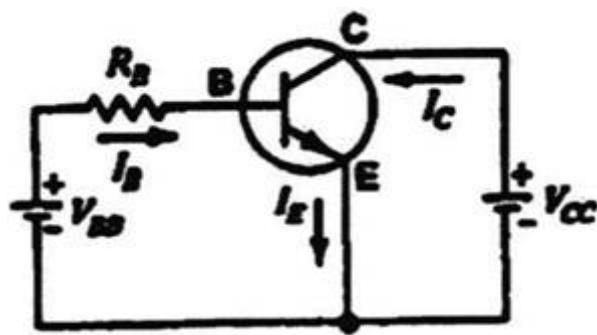
- (a) determine with $V_{BE} = 0.7$ and $V_{BE} = 0$.
- (b) Repeat (a) for $V_{BB} = 12$ V.

Solution: (a) With $V_{BE} = 0.7$ V,

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(4.0 - 0.7) / \{50(10^{-6})\}] = 66 \text{ k}\Omega$$

With $V_{BE} = 0$ V,

$$R_B = [V_{BB} / I_B] = [(4.0) / \{50(10^{-6})\}] = 80 \text{ k}\Omega$$



From the above, we can conclude that the second solution might be too approximate. Actually, it contains a 21 percent error.

(b) With $V_{BE} = 0.7$ V,

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(12 - 0.7) / \{50(10^{-6})\}] = 226 \text{ k}\Omega$$

With $V_{BE} = 0$ V,

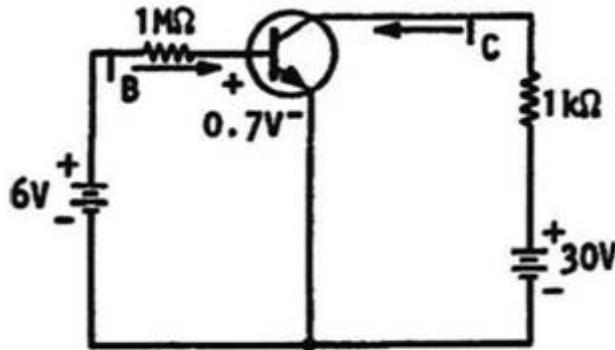
$$R_B = [V_{BB} / I_B] = [12 / \{50(10^{-6})\}] = 240 \text{ k}\Omega$$

Here we have only a 6.2 percent discrepancy, so when the battery voltage is much greater than the base-emitter voltage drop then the approximation of $V_{BE} = 0$ is appropriate.

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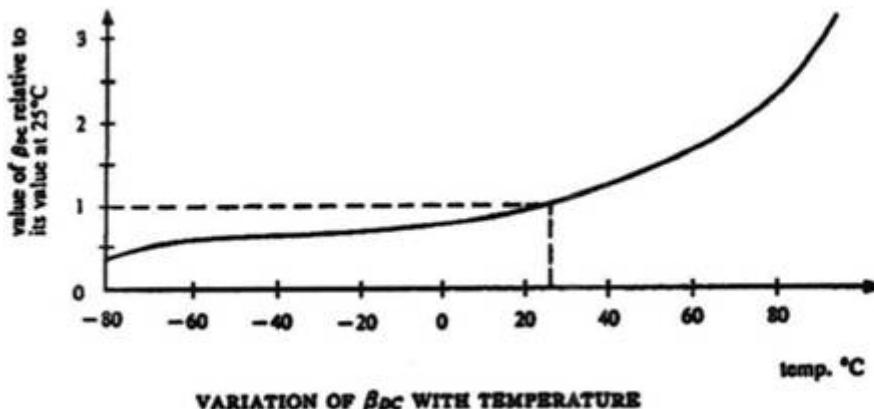
PROBLEM 01 – 0050: Calculate I_B and I_C in the circuit of Figure 1 at 25°C and at 55°C if the transistor is silicon and has $\beta_{DC} = 100$ and $I_{CBO} = 0.1 \mu\text{A}$ at 25°C .

Solution: (a) At 25°C :

**Fig. 1**

$$I_B = [(6 \text{ V} - 0.7 \text{ V}) / (1 \text{ M}\Omega)] = 5.3 \mu\text{A}$$

$$\begin{aligned} I_C &= \beta_{DC} \times I_B + I_{CEO} \\ &= 100 \times 5.3 \mu\text{A} + 101 \times 0.1 \mu\text{A} \\ &= 530 \mu\text{A} + 10.1 \mu\text{A} = 540.1 \mu\text{A} \end{aligned}$$

**Fig. 2****VARIATION OF β_{DC} WITH TEMPERATURE**

(b) At 55°C :

$$V_{BE} = 0.7 \text{ V} - (30) \times (2 \text{ mV}) = 0.64 \text{ V}$$

$$I_{CBO} = 0.1 \mu\text{A} \text{ doubled 3 times} = 0.8 \mu\text{A}$$

$$\beta_{DC} = 1.45 \times 100 = 145 \text{ (from Figure 2)}$$

Thus

$$I_B = [(6 \text{ V} - 0.64 \text{ V}) / (1 \text{ M}\Omega)] = 5.36 \mu\text{A}$$

$$I_C = 145 \times 5.36 \mu\text{A} + 146 \times 0.8 \mu\text{A}$$

$$= 777 \mu\text{A} + 116.8 \mu\text{A} = 893.8 \mu\text{A}$$

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PROBLEM 01 – 0051: A certain transistor has $h_{FE} = 50$. If the base current is 0.1 mA, and we ignore the small leakage current, what is the collector current? What happens if the base current is changed to 0.2 mA?

Solution:

$$h_{FE} = (I_C / I_B)$$

so that

$$I_C = h_{FE} I_B$$

$$I_C = (50) (0.1) (10^{-3}) = 5.0 \text{ mA}$$

If the base current is changed to 0.2 mA, the collector current becomes

$$I_C = (50) (0.2) (10^{-3})$$

$$I_C = 10.0 \text{ mA}$$

The parameter h_{FE} is the low-mid frequency short-circuit CE current gain, which will be discussed extensively in Chapter 4.

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PROBLEM 01 – 0052:

Fig. 1 shows an Si transistor in the grounded emitter configuration. The transistor has $h_{FE} = 30$ and the reverse cutoff current is negligible. The base can be shifted to five different positions. Estimate for these positions, the values of I_C and V_{CE} .

Solution:

First note that the transistor is PNP (emitter arrow points inwards). This is important in determining the state of the transistor.

A: $V_{BE} = +1\text{ V}$ which is reverse biased for a PNP transistor. The transistor is in cutoff and the collector current, I_C is 0. Using KVL, $V_{CE} = V_{CC} = -15\text{ V}$. Fig. 2 shows the location of point A and the other point.

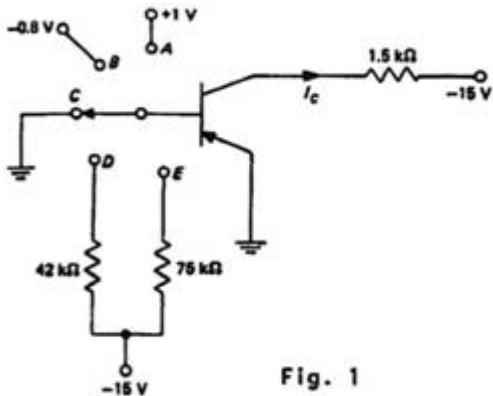


Fig. 1

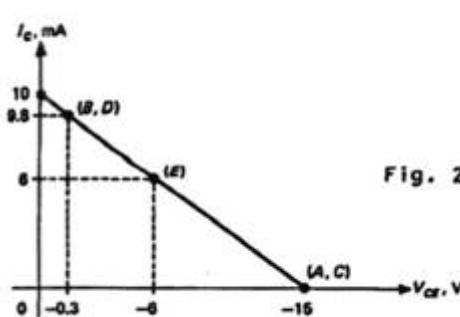


Fig. 2

B: V_{BE} is now -0.8 V . This voltage is enough to drive the transistor into saturation producing a typical $V_{CE, \text{sat}} = -0.3\text{ V}$. Also note that $V_{CB} = V_{CE} - V_{BE} = 0.5\text{ V}$ meaning that the collector base junction is forward biased which is a condition for saturation.

The collector current, I_C , is

$$I_C = [(V_{CC} - V_{CE}) / R_C] = [(15 - 0.3) / (1.5 \times 10^3)] = 9.8\text{ mA}$$

C: Both the base and emitter are grounded, therefore $V_{BE} = 0$ and the transistor is again in cutoff as in A.

D: The base current can be calculated here by neglecting the V_{BE} drop which will be small compared with the 15 V source.

$$I_B \approx [15 / (42 \times 10^3)] = 0.357\text{ mA}$$

Assume that the transistor is in the active region and calculate I_C .

$$I_C = h_{FE}I_B = 30(0.357 \times 10^{-3}) = 11.71\text{ mA}$$

The maximum collector current = $(V_{CC} / R_L) = [15 / (1.5 \times 10^3)] = 10\text{ mA}$. Therefore the results obtained were wrong and the assumption was incorrect; the transistor is instead in saturation, and the results obtained in B are valid here.

E: Using the same procedure as in D:

$$I_B \approx [15 / (75 \times 10^3)] = 0.2\text{ mA}$$

Assume the transistor is active again.

$$I_C = h_{FE}I_B = 30(0.2\text{ mA}) = 6\text{ mA}$$

I_C is below the maximum so our assumption is correct up to now.

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- PROBLEM 01 – 0053: (a) In Figure 1, if $h_{FE} = 100$, determine whether or not the silicon transistor is in saturation and find I_B and I_C
 (b) Repeat with the $2\text{ k}\Omega$ emitter resistance added (Fig. 2).

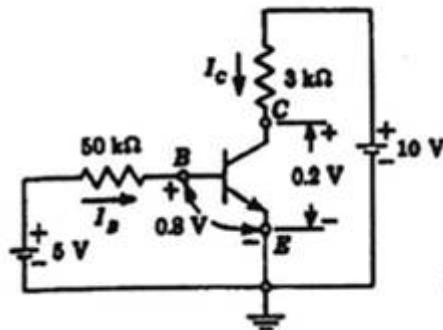


Fig. 1

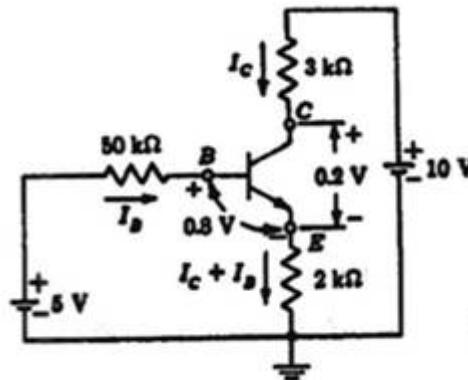


Fig. 2

Solution:

(a) Assume that the transistor is in saturation. Applying KVL to the base circuit gives

$$-5 + 50I_B + 0.8 = 0$$

or

$$I_B = (4.2 / 50) = 0.0840 \text{ mA}$$

Applying KVL to the collector circuit yields

$$-10 + 3I_C + 0.2 = 0$$

or

$$I_C = (9.8 / 3) = 3.267 \text{ mA}$$

The minimum value of base current required for saturation is

$$I_B(\min) = (I_C / h_{FE}) = [(3.267) / 100] = 0.0327 \text{ mA}$$

Since $I_B = 0.0840 > I_B(\min) = 0.0327 \text{ mA}$, we have verified that the transistor is in saturation.

(b) Assume that the transistor is in saturation. Applying KVL to the base and collector circuits, we obtain

$$-5 + 50I_B + 0.8 + 2(I_C + I_B) = 0$$

$$-10 + 3I_C + 0.2 + 2(I_C + I_B) = 0$$

If these simultaneous equations are solved for I_C and I_B , we obtain

$$I_C = 1.96 \text{ mA} \quad I_B = 0.00550 \text{ mA}$$

Since $I_B(\min) = I_C / h_{FE} = 0.0196 \text{ mA} > I_B = 0.00550$, the transistor is not in saturation. Hence the device must be operating in the active region.

Applying KVL to the base circuit,

$$-5 + 50I_B + V_{BE,(\text{active})} + (I_B + I_C)(2) = 0$$

Since $I_C = h_{FE}I_B$ and $V_{BE,(\text{active})} = .7 \text{ V}$,

$$-5 + 50I_B + .7 + I_B(100 + 1)(2) = 0$$

$$I_B = .0171 \text{ mA}$$

$$I_C = h_{FE}I_B = (100)(.0171) = 1.71 \text{ mA}$$

Using KVL around the outer loop,

$$V_{CB} - 50I_B + 5 - 10 + 3I_C = 0$$

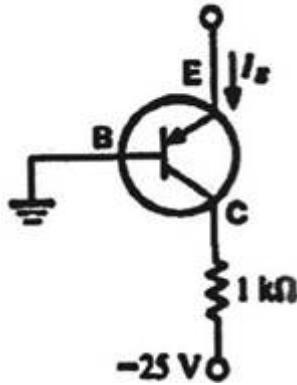
$$V_{CB} = +7.25$$

The transistor is indeed in the active region.

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PROBLEM 01 – 0054: The transistor in the circuit shown has $\alpha_0 = 0.9$ and $I_{EO} = I_{CO} = 10 \mu\text{A}$. Find the critical emitter current that just saturates the transistor.

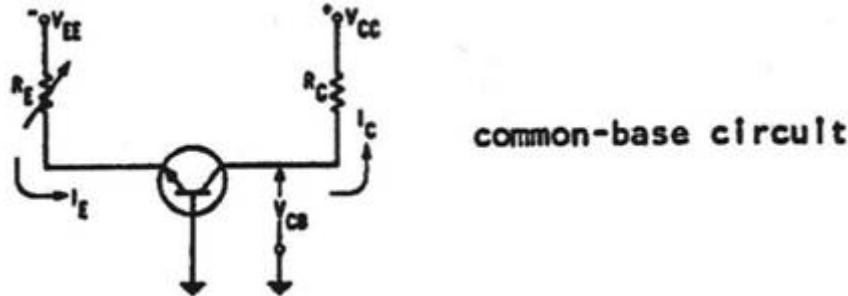
Solution: With the E–B junction forward biased, the transistor will just enter saturation when the C–B junction (which was assumed to have been reverse biased)



just becomes forward biased, i.e. when $V_{CB} = 0$, which with $V_B = V_B = 0 \text{ V}$ requires $V_C = 0 \text{ V}$. The collector current is given by $I_C = (V_C + 25)/1$. As I_E is increased, I_C increases. The I_C required to raise V_C to 0 is $I_C = [(V_C + 25) / 1] = 25 \text{ mA}$. The corresponding input emitter current needed is $I_E = (I_C / \alpha_0) = 27.8 \text{ mA}$.
Note that $\alpha = [\beta / (\beta + 1)]$.

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PROBLEM 01 – 0055: Suppose that in the circuit shown $V_{EE} = -21$ V, $V_{CC} = 24$ V, and $R_C = 8 \text{ k}\Omega$. What is the collector saturation current $I_{C(\text{sat})}$, and what value of R_E will cause the collector to saturate?



Solution:

Saturation occurs when both junctions are forward biased. As a simplifying assumption, we may say that at saturation $V_{CB} = 0$, $V_{BE} = 0$, and $I_E = I_C$. Thus, the collector is saturated when the voltage across R_C is about equal to the source V_{CC} . Therefore

$$I_{C(\text{sat})} \cong [(24 \text{ V}) / (8 \text{ k}\Omega)] = 3 \text{ mA}$$

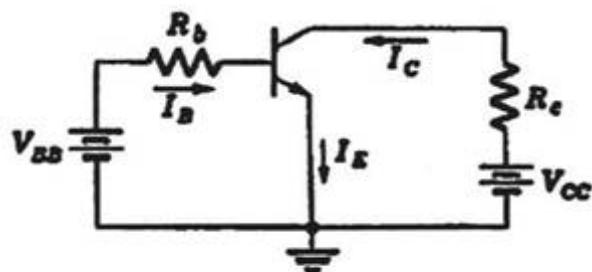
The emitter current I_E that causes saturation is about 3 mA too. This $I_E \cong 3 \text{ mA}$ flows when $R_E \cong 21 \text{ V}/3 \text{ mA} \cong 7 \text{ k}\Omega$.

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PROBLEM 01 – 0056: The behavior of the transistor in the saturation region becomes important in the design of switching circuits. To illustrate this, consider the circuit of Fig. 1, with $V_{CC} = 10$ V, $R_b = 10 \text{ k}\Omega$, and $R_C = 1 \text{ k}\Omega$. The transistor has $\beta = 100$, $V_{BE} = +0.7$ V, and a saturation voltage $V_{CE,sat} = 0.1$ V. Find the operating conditions when (a) $V_{BB} = 1.5$ V and (b) 10.7 V.

Solution: (a) For $V_{BB} = 1.5$ V application of KVL around the base-emitter loop yields

$$-V_{BB} + I_B R_b + V_{BE} = 0$$

**Fig. 1**

or, solving for I_B

$$I_B = [(V_{BB} - V_{BE}) / R_b] = [(1.5 - 0.7) / 10^4] = 0.08 \text{ mA}$$

Since

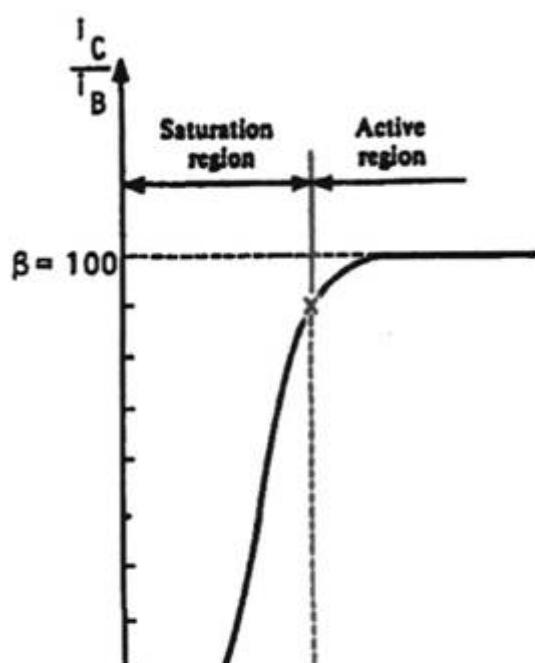
$$I_C = \beta I_B = (100)(0.08) = 8 \text{ mA}$$

and

$$I_E \approx I_C = 8 \text{ mA}$$

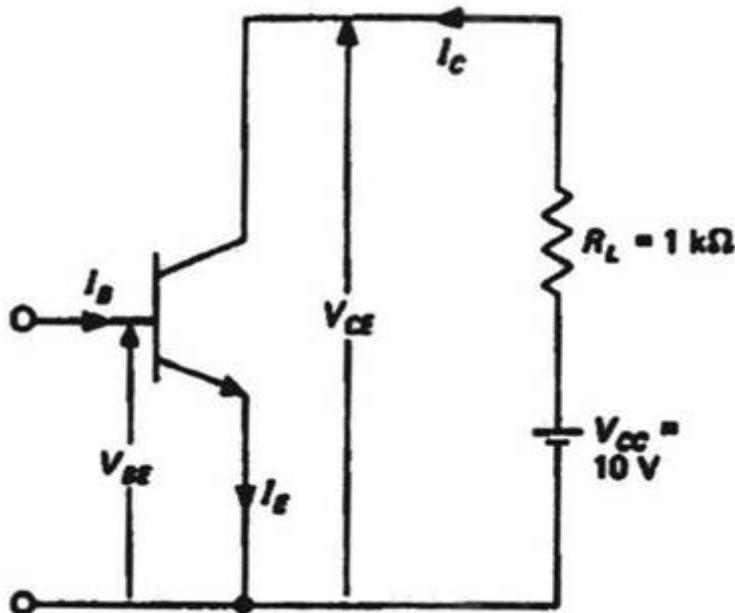
We can find V_{CE} from KVL

$$V_{CE} = V_{CC} - I_C R_C = 10 - (8)(1) = 2 \text{ V}$$

**Fig. 2**

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- PROBLEM 01 – 0057:** The transistor shown is to be driven between cutoff and active alternately by applying an appropriate voltage across the base emitter junction of the transistor.
- Determine the collector current, I_C , and V_{CE} for both states of the transistor assuming the transistor is ideal.
 - Do (a) assuming that the transistor is a real Germanium transistor. What drive is needed at the base emitter junction to perform the desired task?
 - Do (a) again, this time assuming the transistor is a real silicon transistor. What drive is needed at the base emitter junction in this case?



Solution:

(a) OFF: $I_C = 0$

$$V_{CE} = V_{CC} = 10 \text{ V}$$

$$\text{ON: } I_C = (V_{CC} / R_L) = 10/1000 = 10 \text{ mA}$$

$$V_{CE} = 0$$

(b) OFF: With $V_{BE} = -0.1 \text{ V}$, the transistor is turned off. The current is a certain value I_{CEX} and the voltage V_{CE} depends on I_{CEX} . $V_{CE} = V_{CC} - I_{CEX}R_L$.

ON: A voltage of about 0.3 V at the base-emitter junction is needed to turn on a germanium transistor. The collector-emitter junction will have a typical voltage of about 0.1 V ($V_{CE} \approx 0.1 \text{ V}$). The collector current is

$$I_C = [(V_{CC} - V_{CE}) / R_L] = [(10 - 0.1) / (1,000)] = 9.9 \text{ mA}$$

(c) OFF: For Si transistor, a V_{BE} of 0 V will turn it off. The current in the collector is some small number (for Si) I_{CES} . The voltage is then

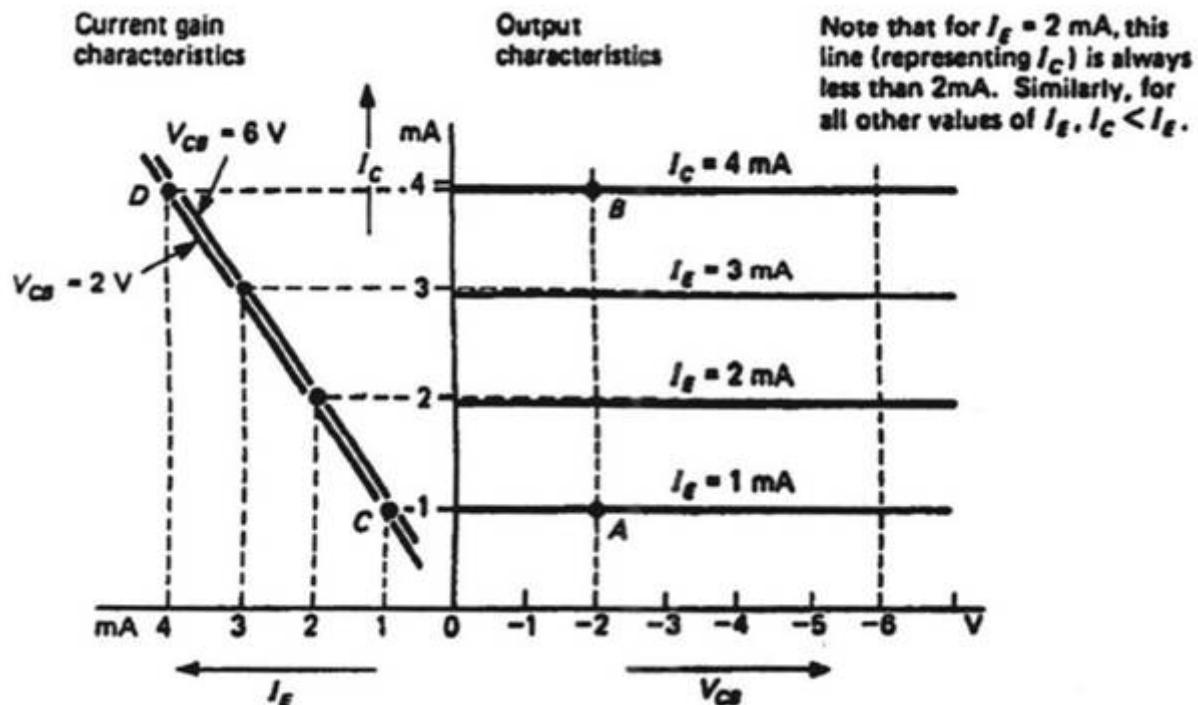
$$V_{CE} = V_{CC} - I_{CES}R_L$$

ON: A V_{BE} of about 0.7 volt is needed to turn on an Si transistor and the V_{CE} for an active Si transistor is typically 0.3 V. Therefore the collector current is

$$I_C = [(10 - 0.3) / (1,000)] = 9.7 \text{ mA}$$

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PROBLEM 01 – 0058: From the common base output characteristics shown derive the current gain characteristics for $V_{CB} = 2$ V and for $V_{CB} = 6$ V.



Solution: On the output characteristics draw a vertical line at $V_{CB} = 2$ V.

Where the line intersects the output characteristics at point A, read $I_C = 0.95$ mA for $I_E = 1$ mA. Now plot point C at $I_C = 0.95$ mA on the vertical axis and $I_E = 1$ mA on the lefthand horizontal axis. Returning to the output characteristics, read $I_C = 3.95$ mA at $I_E = 4$ mA and $V_{CB} = 2$ V, point B. Now plot point D at $I_C = 3.95$ mA on the vertical axis and $I_E = 4$ mA on the horizontal axis. Draw a line through points C and D to give the current gain characteristic for $V_{CB} = 2$ V. Repeat the above procedure for $V_{CB} = 6$ V.

As can be seen, we have very nearly $I_C = I_E$. This is as expected since

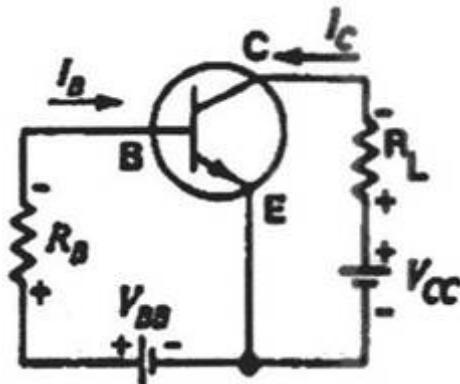
$$I_C = \alpha_{dc} I_E + I_{CBO}$$

and

$$\alpha_{dc} \approx 1 \text{ and } I_{CBO} \approx 0 \mu\text{A}.$$

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PROBLEM 01 – 0059: An n-p-n silicon transistor is chosen with $V_{BB} = 6.0$ volts and $V_{CC} = 12.0$ volts. If the transistor has a β_{dc} of 50 and an I_B of $50 \mu\text{A}$ for an operating condition, determine
 (a) R_B , (b) I_C , (c) the dc voltage drop across R_L if R_L equals $1.0 \text{ k}\Omega$, and (d) V_{CE} .



Solution:

(a) By summing voltages around the base- emitter loop, we have

$$R_B = [(V_{BB} - V_{BE}) / I_B] = [(6.0 - 0.7) / \{50(10^{-6})\}] = 106 \text{ k}\Omega$$

$$(b) I_C = \beta I_B = 50 (50) (10^{-6}) = 2.5 \text{ mA}$$

(c) knowing I_C ,

$$V_{(R)L} = I_C R_L = 2.5 (10^{-3}) (1.0) (10^3) = 2.5 \text{ volts}$$

(d) this time considering the collector-emitter loop,

$$V_{CE} = V_{CC} - I_C R_L = 12 - 2.5 = 9.5 \text{ volts}$$

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PROBLEM 01 – 0060:

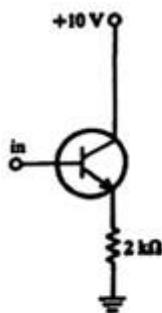
(a) For the four circuits in Figs. 1–4, find the load line intercepts and slope. For simplicity, assume $\alpha = 1$.(b) If the transistor used in each of the circuits has a breakdown voltage $BV_{CB} = 15$ V, which circuits will operate properly and why?

Fig. 1

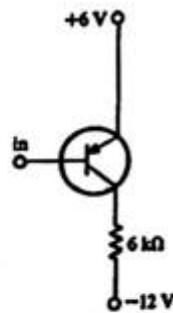


Fig. 2

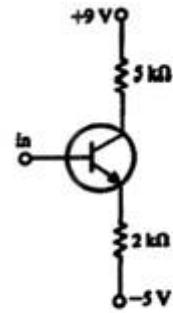


Fig. 3

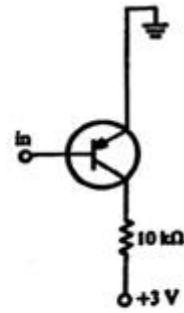


Fig. 4

Solution:

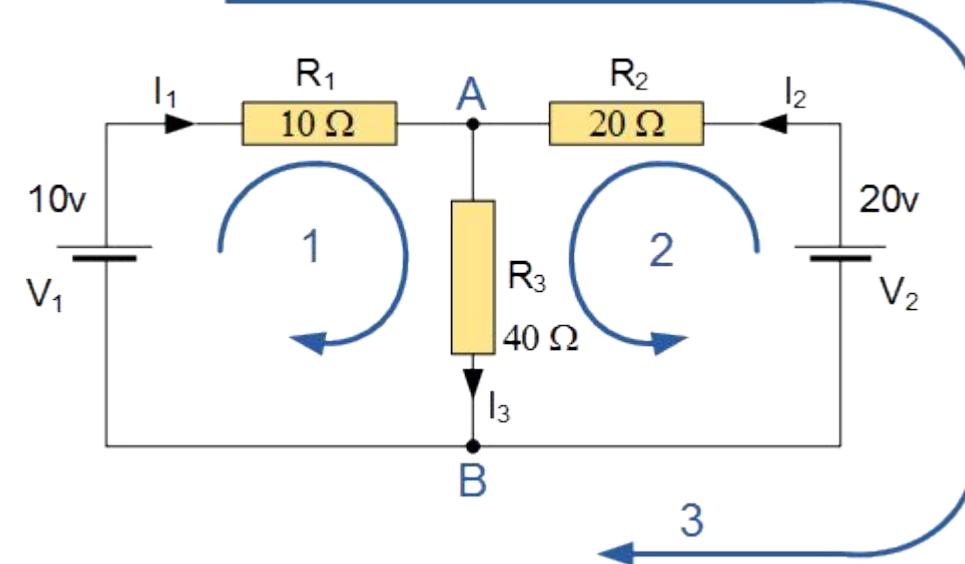
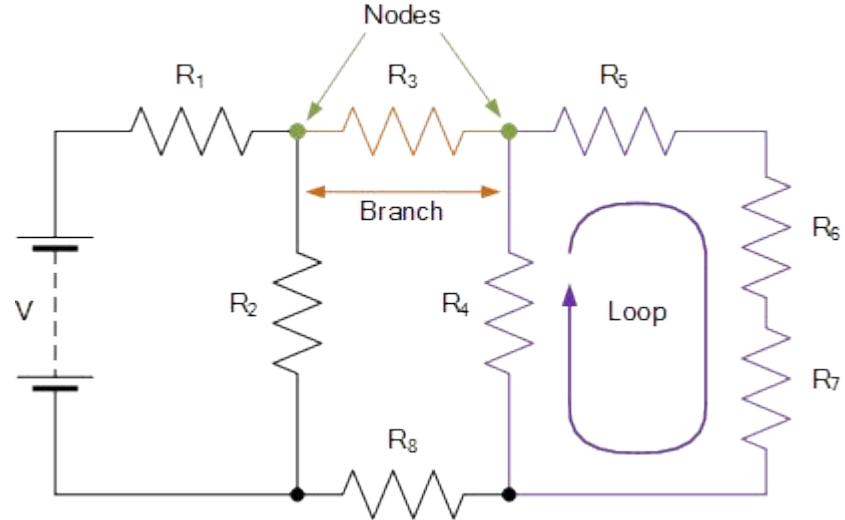
(a) Figure 1: The output loop equation, obtained by summing the voltage drops from the 10 V supply to ground, is $2i_C + v_{CE} = 10$. At $i_C = 0$ we find $v_{CE} = 10$ V, while at $v_{CE} = 0$ we obtain $i_C = 5$ mA. Thus the load line intercepts are 10 V and 5 mA and the slope is $(i_C / v_{CE}) = -0.5$ mmho.

Figure 2: The output loop equation is $6i_C + v_{CE} = 18$. The intercepts are 18 V (at $i_C = 0$) and 3 mA (at $v_{CE} = 0$), and the slope is $-1/6$ ($k\Omega$) $^{-1}$.

Figure 3: The output loop equation is $-9 + 5i_C + v_{CE} + 2i_E - 5 = 0$ or $7i_C + v_{CE} = 14$. The intercepts are thus 14 V (at $i_C = 0$) and 2 mA (at $v_{CE} = 0$) and the slope is $-1/7$ ($k\Omega$) $^{-1}$.

Figure 4: This circuit will not work as shown since the power supply bias is wrong. There is no load line, rather the circuit sits at a single output point at $i_C = I_{CO} \approx 0$ and $v_{CE} \approx 3$ V.

(b) If we assume v_{EB} small, then $v_{CE} \approx v_{CB}$. To avoid damage to the transistor we must insure that the largest value of v_{CE} be less than the breakdown voltage of the junction or 15 V. All circuits except (2) have a v_{CE} intercept less than 15 V, so only these circuits will operate properly with a transistor having a $BV_{CB} = 15$ V.



Using **Kirchhoffs Current Law, KCL** the equations are given as:

$$\text{At node A : } I_1 + I_2 = I_3$$

$$\text{At node B : } I_3 = I_1 + I_2$$

Using **Kirchhoffs Voltage Law, KVL** the equations are given as:

$$\text{Loop 1 is given as : } 10 = R_1 I_1 + R_3 I_3 = 10I_1 + 40I_3$$

$$\text{Loop 2 is given as : } 20 = R_2 I_2 + R_3 I_3 = 20I_2 + 40I_3$$

NPN

$$I_E = I_S [e^{VBE / VT}]$$

PNP

$$I_E = I_S [e^{VEB / VT}]$$

$$I_C = \beta I_B$$

$$I_C = \alpha I_E$$

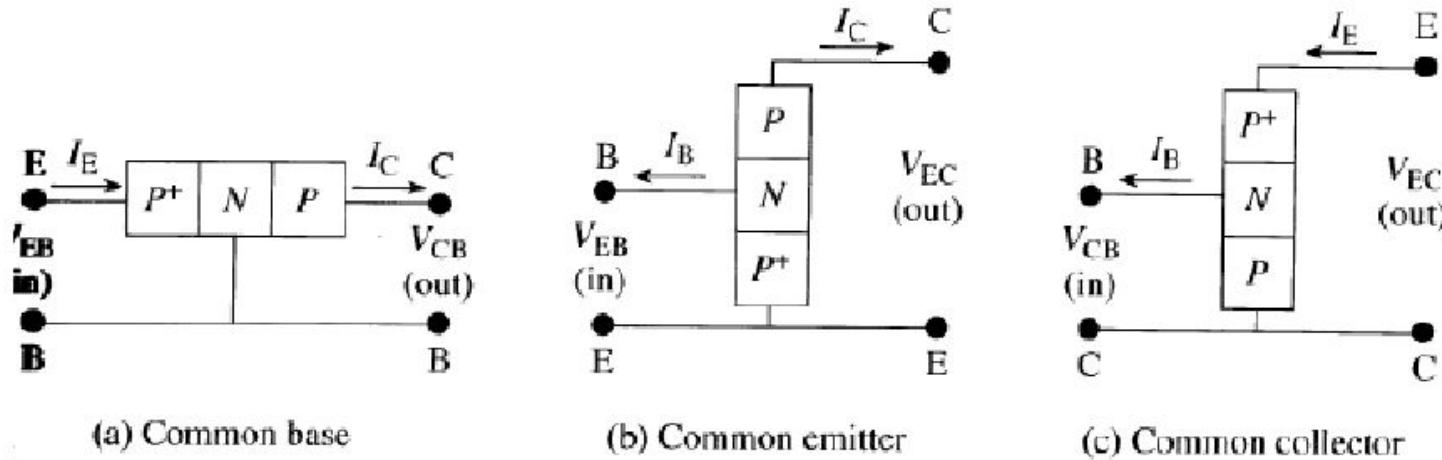
$$I_E = I_B(\beta + 1)$$

$$\alpha = \frac{\beta}{1 + \beta}$$

$$\beta = \frac{\alpha}{1 - \alpha}$$

Based on KCL: $I_E = I_C + I_B$

BJT configurations



Common Base Configuration – has **Voltage Gain** but **no Current Gain**.

Common Emitter Configuration – has **both Current and Voltage Gain**.

Common Collector Configuration – has **Current Gain** but **no Voltage Gain**.

Alpha (α):

- It is a large signal current gain in common base configuration.
- It is the ratio of collector current (output current) to the emitter current (input current).

$$\alpha = \frac{I_C}{I_E}$$

- It indicates that the amount of emitter current reaching to collector.
- Its value is unity ideally and practically less than unity.

Gama (γ):

- It is a current gain in common collector configuration and it is the ration of emitter current (output current) to base current (input current).

$$\gamma = \frac{I_E}{I_B}$$

- It is also called emitter efficiency that how much current is injected from the emitter to base after recombination of minority charge carriers in base.
- It's value is high compared to α, β
- Relation between α, β and γ

$$\gamma = \beta + 1 = \frac{1}{1 - \alpha}$$

Beta (β):

- It is a current gain factor in the common emitter configuration. It is the ration of collector current (output current) to base current (output current).

$$\beta = \frac{I_C}{I_B}$$

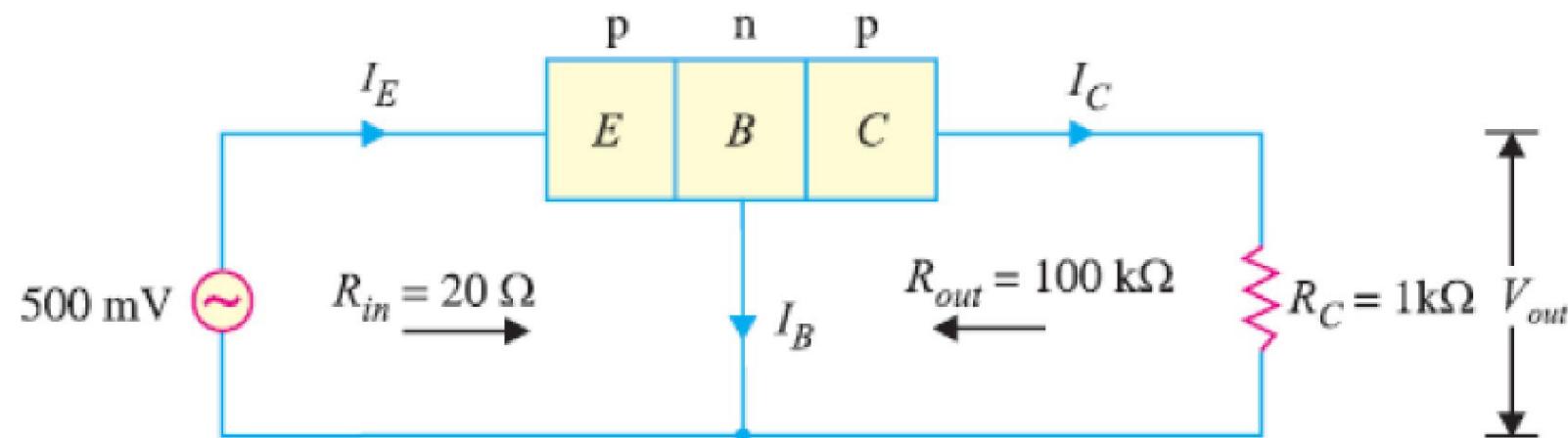
- Normally Its value is greater than 100.

$$\alpha \gamma = \beta$$

1) A common base transistor amplifier has an input resistance of 20Ω and output resistance of $100\text{ k}\Omega$. The collector load is $1\text{ k}\Omega$. If a signal of 500 mV is applied between emitter and base, find the voltage amplification. Assume α_{ac} to be nearly one

Solution

Here the output resistance is very high as compared to input resistance, since the input junction (base to emitter) of the transistor is forward biased while the output junction (base to collector) is reverse biased.



Input current, $I_E = \frac{\text{Signal}}{R_{in}} = \frac{500 \text{ mV}}{20 \Omega} = 25 \text{ mA}$. Since α_{ac} is nearly 1, output current, $I_C = I_E = 25 \text{ mA}$.

$$\text{Output voltage, } V_{out} = I_C R_C = 25 \text{ mA} \times 1 \text{ k}\Omega = 25 \text{ V}$$

$$\therefore \text{Voltage amplification, } A_v = \frac{V_{out}}{\text{signal}} = \frac{25 \text{ V}}{500 \text{ mV}} = 50$$

2) In a common base connection , IE = 1mA, IC = 0.95mA. Calculate the value of IB

Solution :

Using the relation, $I_E = I_B + I_C$

$$1 = I_B + 0.95$$

$$I_B = 1 - 0.95 = \mathbf{0.05 \text{ mA}}$$

3) In a common base connection, current amplification factor is 0.9. If the emitter current is 1mA, determine the value of base current.

Solution :

Here, $\alpha = 0.9$, $I_E = 1 \text{ mA}$

Now

$$\alpha = \frac{I_C}{I_E}$$

or

$$I_C = \alpha I_E = 0.9 \times 1 = 0.9 \text{ mA}$$

Also

$$I_E = I_B + I_C$$

∴

$$\text{Base current, } I_B = I_E - I_C = 1 - 0.9 = \mathbf{0.1 \text{ mA}}$$

4) In a common base connection, $I_C = 0.95$ mA and $I_B = 0.05$ mA. Find the value of α .

Solution :

$$\text{We know } I_E = I_B + I_C = 0.05 + 0.95 = 1 \text{ mA}$$

$$\therefore \text{Current amplification factor, } \alpha = \frac{I_C}{I_E} = \frac{0.95}{1} = 0.95$$

5) In a common base connection, the emitter current is 1mA. If the emitter circuit is open, the collector current is 50 μ A. Find the total collector current. Given that $\alpha = 0.92$.

Solution :

$$\text{Here, } I_E = 1 \text{ mA, } \alpha = 0.92, \quad I_{CBO} = 50 \mu\text{A}$$

$$\begin{aligned}\text{Total collector current, } I_C &= \alpha I_E + I_{CBO} = 0.92 \times 1 + 50 \times 10^{-3} \\ &= 0.92 + 0.05 = 0.97 \text{ mA}\end{aligned}$$

Q6. In a common base connection, $\alpha = 0.95$. The voltage drop across $2\text{ k}\Omega$ resistance which is connected in the collector is 2V. Find the base current.

Solution :

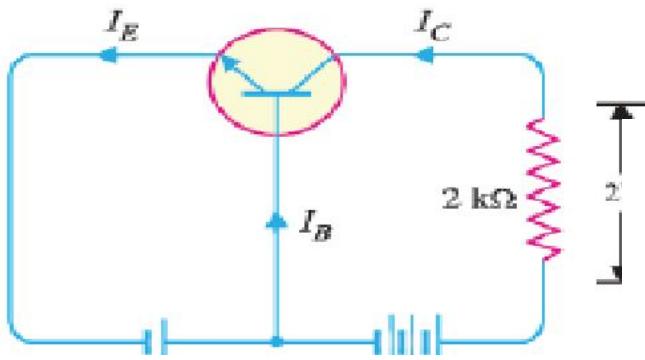


Fig. 2 shows the required common base connection

The voltage drop across RC ($= 2\text{ k}\Omega$) is ...

$$I_E = \frac{I_C}{\alpha} = \frac{1}{0.95} = 1.05 \text{ mA}$$

Using the relation, $I_E = I_B + I_C$

$$\therefore I_B = I_E - I_C = 1.05 - 1 \\ = 0.05 \text{ mA}$$

$$I_C = 2 \text{ V}/2 \text{ k}\Omega = 1 \text{ mA}$$

$$\alpha = I_C/I_E$$

Q7. For the common base circuit shown in Fig. 3, determine IC and VCB . Assume the transistor to be of silicon.

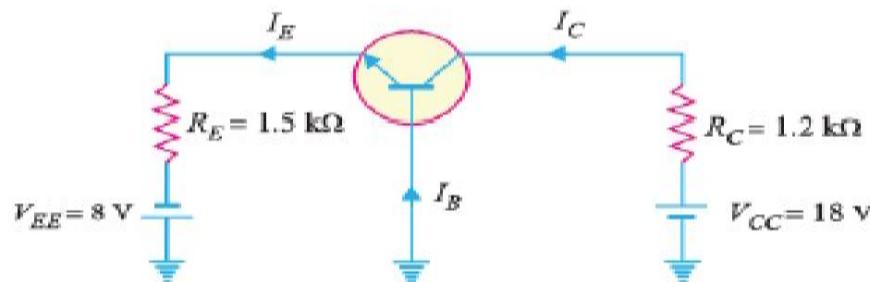


Fig. 3

Solution :

Since the transistor is of silicon, $V_{BE} = 0.7V$.

Applying Kirchhoff's voltage law to the emitter-side loop, we get,

$$V_{EE} = I_E R_E + V_{BE}$$

$$\text{or } I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{8V - 0.7V}{1.5 \text{ k}\Omega} = 4.87 \text{ mA}$$

$$\therefore I_C \approx I_E = 4.87 \text{ mA}$$

Applying Kirchhoff's voltage law to the collector-side loop, we have,

$$V_{CC} = I_C R_C + V_{CB}$$

$$\therefore V_{CB} = V_{CC} - I_C R_C$$

$$= 18 \text{ V} - 4.87 \text{ mA} \times 1.2 \text{ k}\Omega = 12.16 \text{ V}$$

**Q8. Find the value of β if (i) $\alpha = 0.9$ (ii)
 $\alpha = 0.98$ (iii) $\alpha = 0.99$.**

Solution :

(i) $\alpha = 0.9$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.9}{1 - 0.9} = 9$$

(ii) $\alpha = 0.98$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.98}{1 - 0.98} = 49$$

(iii) $\alpha = 0.99$

$$\beta = \frac{\alpha}{1 - \alpha} = \frac{0.99}{1 - 0.99} = 99$$

Q9. Calculate IE in a transistor for which $\beta = 50$ and $I_B = 20 \mu A$.

Solution :

Here $\beta = 50$, $I_B = 20 \mu A = 0.02 \text{ mA}$

Now

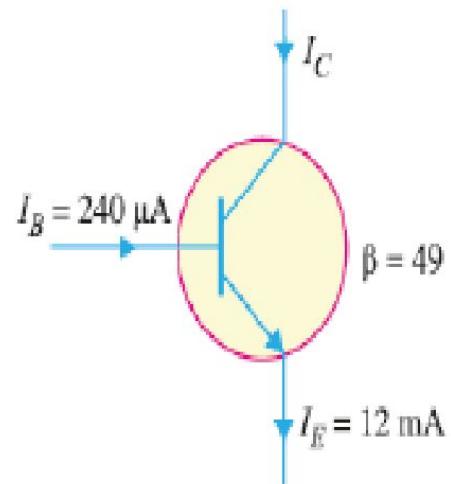
$$\beta = \frac{I_C}{I_B}$$

\therefore

$$I_C = \beta I_B = 50 \times 0.02 = 1 \text{ mA}$$

Using the relation, $I_E = I_B + I_C = 0.02 + 1 = 1.02 \text{ mA}$

Q10. Find the α rating of the transistor shown in Fig. 4. Hence determine the value of I_C using both α and β rating of the transistor.



Solution :

$$\alpha = \frac{\beta}{1 + \beta} = \frac{49}{1 + 49} = 0.98$$

The value of I_C can be found by using either α or β rating as under :

$$I_C = \alpha I_E = 0.98 (12 \text{ mA}) = 11.76 \text{ mA}$$

$$\text{Also } I_C = \beta I_B = 49 (240 \mu\text{A}) = 11.76 \text{ mA}$$

Solution :

Q11. For a transistor, $\beta = 45$ and voltage drop across $1\text{k}\Omega$ which is connected in the collector circuit is 1 volt. Find the base current for common emitter connection.

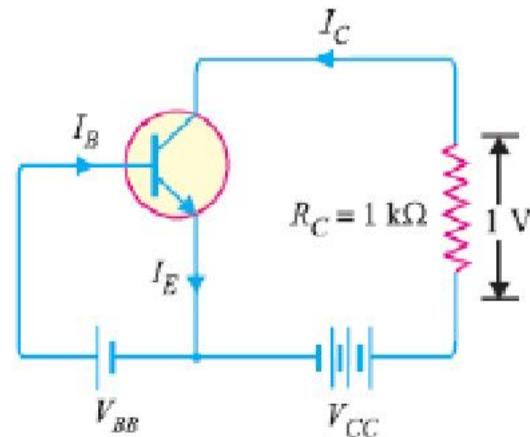


Fig. 5

Fig. 5 shows the required common emitter connection. The voltage drop across $RC (= 1\text{k}\Omega)$ is 1 volt.

$$\therefore I_C = \frac{1V}{1\text{k}\Omega} = 1\text{ mA}$$

$$\text{Now } \beta = \frac{I_C}{I_B}$$

$$\therefore I_B = \frac{I_C}{\beta} = \frac{1}{45} = 0.022\text{ mA}$$

Solution:

Q12. A transistor is connected in common emitter (CE) configuration in which collector supply is 8 V and the voltage drop across resistance R_C connected in the collector circuit is 0.5 V. The value of $R_C = 800 \Omega$. If $\alpha = 0.96$, determine : (i) collector-emitter voltage (ii) base current.

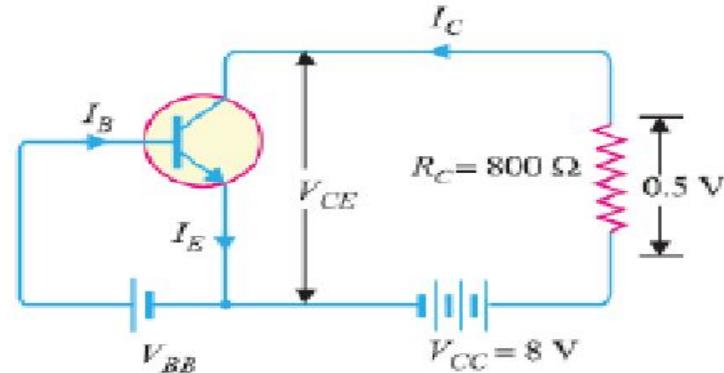


Fig.6

Fig. 6 shows the required common emitter connection with various values.

Collector-emitter voltage,

$$V_{CE} = V_{CC} - 0.5 = 8 - 0.5 = 7.5 \text{ V}$$

(i)

(ii)

The voltage drop across $R_C (= 800 \Omega)$ is 0.5 V.

$$I_C = \frac{0.5 \text{ V}}{800 \Omega} = \frac{5}{8} \text{ mA} = 0.625 \text{ mA}$$

$$\text{Now } \beta = \frac{\alpha}{1 - \alpha} = \frac{0.96}{1 - 0.96} = 24$$

$$\therefore \text{Base current, } I_B = \frac{I_C}{\beta} = \frac{0.625}{24} = 0.026 \text{ mA}$$

Solution :

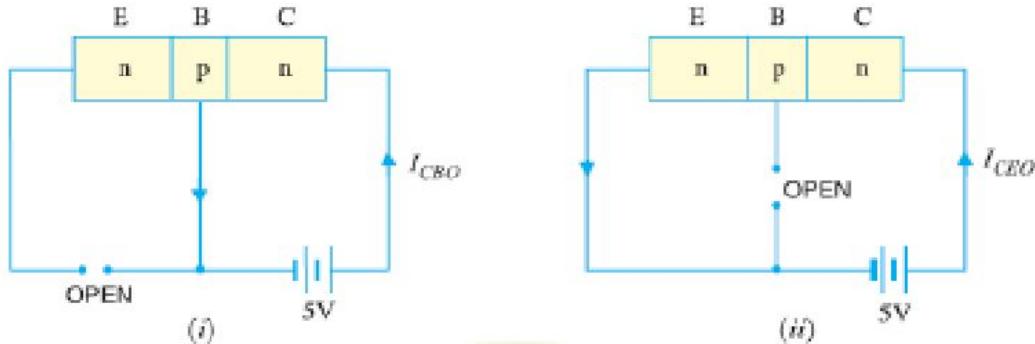


Fig. 7

Q13 An n-p-n transistor at room temperature has its emitter disconnected. A voltage of 5 V is applied between collector and base. With collector positive, a current of 0.2 μ A flows. When the base is disconnected and the same voltage is applied between collector and emitter, the current is found to be 20 μ A. Find α , I_E and I_B when collector current is 1 mA.

When the emitter circuit is open as shown in Fig.7 (i) , the collector-base junction is reverse biased. A small leakage current I_{CBO} flows due to minority carriers.

$$\therefore I_{CBO} = 0.2 \mu\text{A} \quad \dots \text{given}$$

When base is open [See Fig. 8.23 (ii)], a small leakage current I_{CBO} flows due to minority carriers.

$$\therefore I_{CBO} = 20 \mu\text{A} \quad \dots \text{given}$$

$$\text{We know} \quad I_{CBO} = \frac{I_{CBO}}{1 - \alpha}$$

$$\text{or} \quad 20 = \frac{0.2}{1 - \alpha}$$

$$\therefore \alpha = 0.99$$

$$\text{Now} \quad I_C = \alpha I_E + I_{CBO}$$

$$\text{Here} \quad I_C = 1\text{mA} = 1000 \mu\text{A}; \alpha = 0.99; I_{CBO} = 0.2 \mu\text{A}$$

$$\therefore 1000 = 0.99 \times I_E + 0.2$$

$$\text{or} \quad I_E = \frac{1000 - 0.2}{0.99} = 1010 \mu\text{A}$$

$$\text{and} \quad I_B = I_E - I_C = 1010 - 1000 = 10 \mu\text{A}$$

Q14) The collector leakage current in a transistor is 300 μA in CE arrangement. If now the transistor is connected in CB arrangement, what will be the leakage current?

Given that $\beta = 120$.

Solution

$$I_{CEO} = 300 \mu\text{A}$$

$$\beta = 120 ; \alpha = \frac{\beta}{\beta+1} = \frac{120}{120+1} = 0.992$$

Now, $I_{CEO} = \frac{I_{CBO}}{1-\alpha}$

$$\therefore I_{CBO} = (1-\alpha) I_{CEO} = (1-0.992) \times 300 = 2.4 \mu\text{A}$$

Note that leakage current in *CE* arrangement (*i.e.* I_{CEO}) is much more than in *CB* arrangement (*i.e.* I_{CBO}).

Q15. For a certain transistor, $I_B = 20 \mu A$; $I_C = 2 \text{ mA}$ and $\beta = 80$. Calculate I_{CBO} .

Solution :

$$I_C = \beta I_B + I_{CEO}$$

or

$$2 = 80 \times 0.02 + I_{CEO}$$

∴

$$I_{CEO} = 2 - 80 \times 0.02 = 0.4 \text{ mA}$$

Now

$$\alpha = \frac{\beta}{\beta+1} = \frac{80}{80+1} = 0.988$$

∴

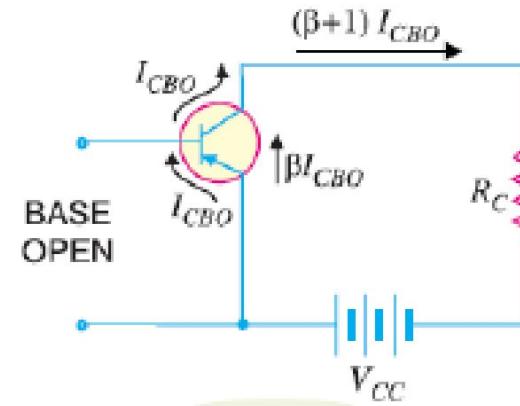
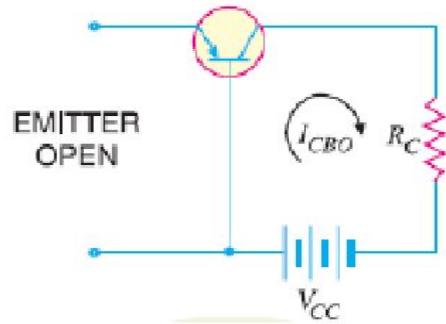
$$I_{CBO} = (1 - \alpha) I_{CEO} = (1 - 0.988) \times 0.4 = 0.0048 \text{ mA}$$

I_{CBO} is the collector current with collector junction reverse biased and base open-circuited. I_{CEO} is the collector current with collector junction reverse biased and emitter open-circuited. I_{CBO} is reverse leakage current going from the Collector to the Base. This current is then amplified by β to produce additional Collector current, thus the " $1+\beta$ " term.

Q16. Using diagrams, explain the correctness of the relation $I_{CEO} = (\beta + 1)I_{CBO}$.

Solution :

The leakage current I_{CBO} is the current that flows through the base-collector junction when emitter is open as shown in Fig. 8.



When the transistor is in CE arrangement, the base current (i.e. I_{CBO}) is multiplied by β in the collector as shown in Fig. 9.

∴

$$I_{CEO} = I_{CBO} + \beta I_{CBO} = (\beta + 1) I_{CBO}$$

Q17. Determine V_{CB} in the transistor circuit shown in Fig. 10 (i). The transistor is of silicon and has $\beta = 150$.

Solution :

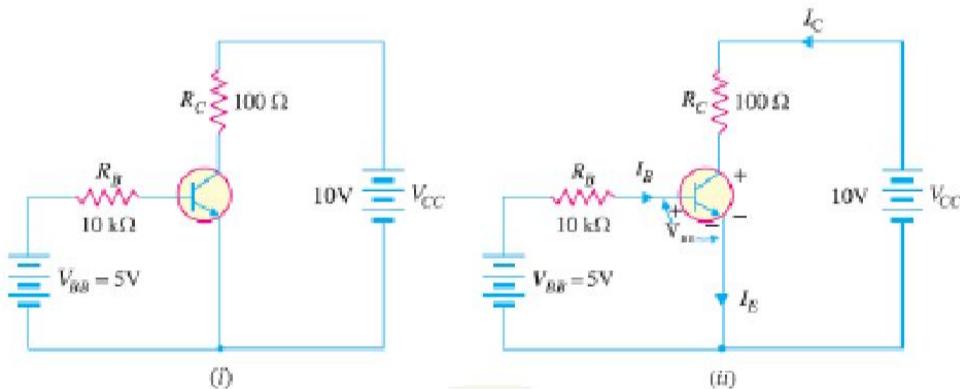


Fig.10

Solution :

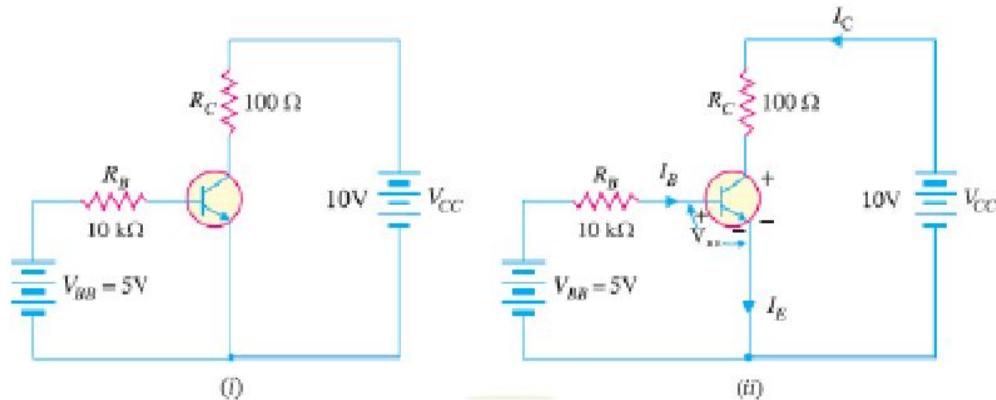


Fig.10

Fig. 10 (i) shows the transistor circuit while Fig. 10 (ii) shows the various currents and voltages along with polarities.

Applying Kirchhoff's voltage law to base-emitter loop, we have,

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$\text{or } I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{10\text{ k}\Omega} = 430 \mu\text{A}$$

$$\therefore I_C = \beta I_B = (150)(430 \mu\text{A}) = 64.5 \text{ mA}$$

$$\begin{aligned} \text{Now } V_{CE} &= V_{CC} - I_C R_C \\ &= 10\text{V} - (64.5 \text{ mA})(100\Omega) = 10\text{V} - 6.45\text{V} = 3.55\text{V} \end{aligned}$$

$$\text{We know that : } V_{CE} = V_{CB} + V_{BE}$$

$$\therefore V_{CB} = V_{CE} - V_{BE} = 3.55 - 0.7 = \text{2.85V}$$

Q18. In a transistor, $I_B = 68 \mu A$, $I_E = 30 mA$ and $\beta = 440$. Determine the α rating of the transistor. Then determine the value of I_C using both the α rating and β rating of the transistor.

Solution :

$$\alpha = \frac{\beta}{\beta+1} = \frac{440}{440+1} = 0.9977$$

$$I_C = \alpha I_E = (0.9977) (30 \text{ mA}) = 29.93 \text{ mA}$$

Also

$$I_C = \beta I_B = (440) (68 \mu A) = 29.93 \text{ mA}$$

Q19. A transistor has the following ratings : $I_C \text{ (max)} = 500 \text{ mA}$ and $\beta_{\text{max}} = 300$.

Determine the maximum allowable value of I_B for the device.

Solution :

$$I_{B \text{ (max)}} = \frac{I_{C \text{ (max)}}}{\beta_{\text{max}}} = \frac{500 \text{ mA}}{300} = 1.67 \text{ mA}$$

For this transistor, if the base current is allowed to exceed 1.67 mA, the collector current will exceed its maximum rating of 500 mA and the transistor will probably be destroyed.

Q20. Fig. 11 shows the open circuit failures in a transistor. What will be the circuit behaviour in each case ?

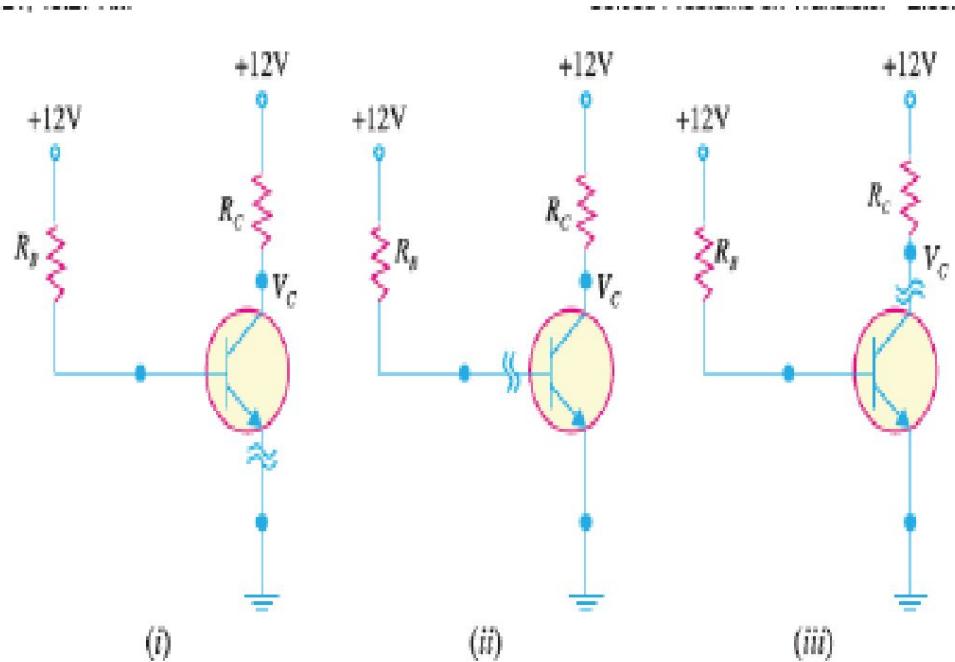


Fig. 11

(i) Open emitter :

Fig. 11 (i) shows an open emitter failure in a transistor. Since the collector diode is not forward biased, it is OFF and there can be neither collector current nor base current.

Therefore, there will be no voltage drops across either resistor and the voltage at the base and at the collector leads of the transistor will be 12V.

(ii) Open-base :

Fig. 11 (ii) shows an open base failure in a transistor. Since the base is open, there can be no base current so that the transistor is in cut-off. Therefore, all the transistor currents are 0A. In this case, the base and collector voltages will both be at 12V.

(iii) Open collector :

Fig. 11 (iii) shows an open collector failure in a transistor. In this case, the emitter diode is still ON, so we expect to see 0.7V at the base. However, we will see 12V at the collector because there is no collector current.

Emitter-Bias Configuration (Solved Problem)

For the emitter-bias circuit, determine:

(a) R_C

(b) R_E

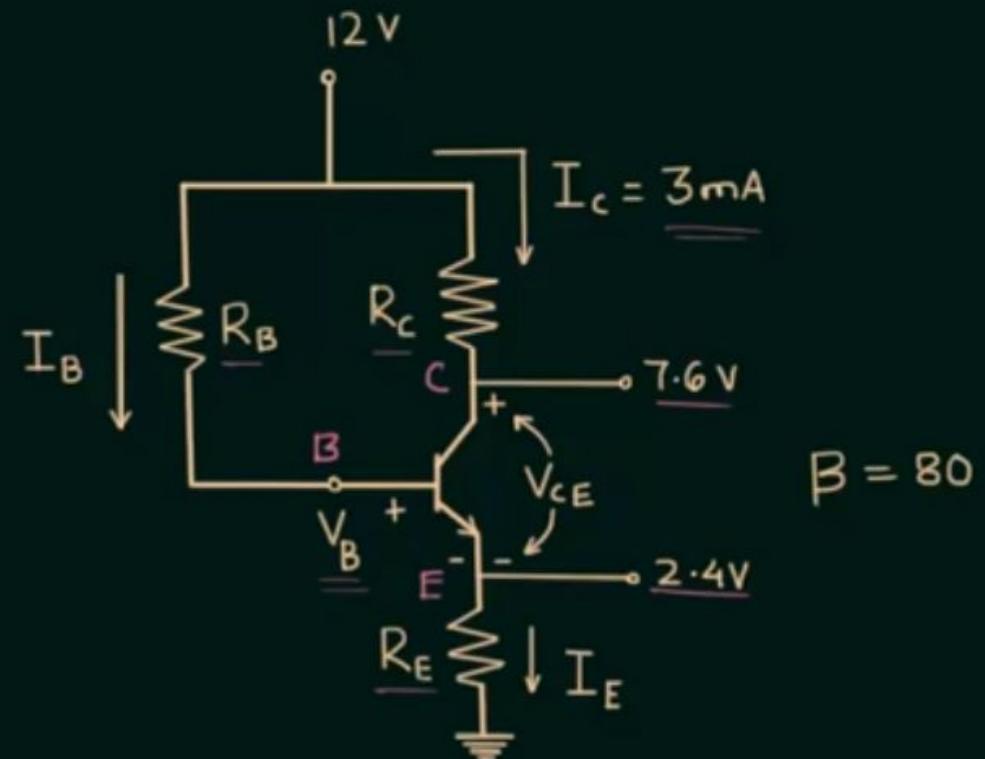
(c) R_B

(d) V_{CE} ($\underline{0} \text{ } \underline{p}$)

(e) V_B

$$I_C = 3 \text{ mA} \quad V_C = 7.6 \text{ V} \quad V_{CC} = 12 \text{ V}$$

$$\beta = 80 \quad V_E = 2.4 \text{ V}$$



Sel: c) $V_{BE} = 0.7V$ (si) d) $V_{CE} = V_C - V_E$

$$V_B - V_E = 0.7V$$

$$V_B = 2.4V + 0.7V$$

$$V_B = 3.1V \quad \underline{Ans}$$

$$V_{CE} = 5.2V \quad \underline{Ans}$$

c) $+12V - I_B R_B = 3.1V$ $I_B = I_C / \beta = \frac{3mA}{80} = 37.5\mu A$ $R_B = \frac{12V - 3.1V}{37.5\mu A} = 231.4k\Omega$ \underline{Ans}

FOR THE Emitter-Bias CIRCUIT, DETERMINE:

(a) R_C

(b) R_E

(c) R_B

(d) V_{CE} (O/P)

(e) V_B

a) $12V - I_C R_C = 7.6V$

$$R_C = \frac{12V - 7.6V}{I_C}$$

$$R_C = 1.47k\Omega \quad I_C = 3mA$$

b) $2.4V - I_E R_E = 0V$

$$R_E = \frac{2.4V}{I_E} = 0.8k\Omega$$

