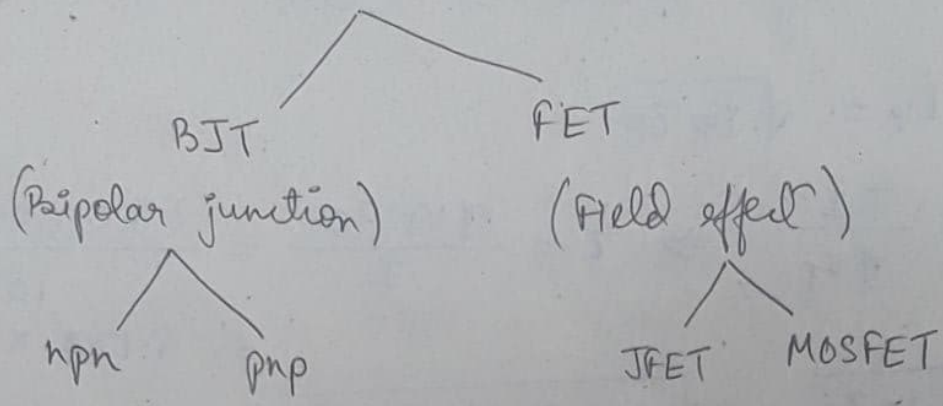
UNIT 2 : TRANSISTOR

↓

electronic device made of semiconductor used to amplify or switch electronic signals.

* It is atleast 3 terminal device.



BJT

3 terminal SC device which depends on both majority and minority carriers.

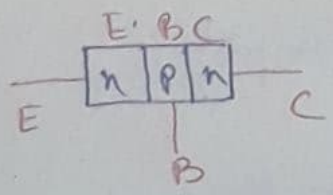
Uses

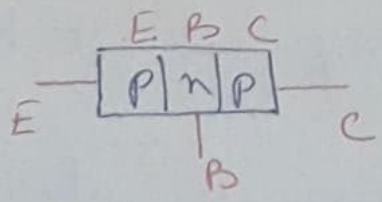
Amplifier, switch, oscillator, computer, satellite

Construction

It consist of a Si or Ge crystal in which thin layer of n type material is sandwiched b/w 2 p type layer. This is pnp transistor.

When p type material is sandwiched b/w. 2 layers of n type material, it is called npn transistor.





Transistor = transfer + Resistor

we are transfering current from 1 resistance path to another resistance path.

3 regions → Emitter, Base, collector

3 terminal → emitter, Base, collector

2 junctions → emitter to base junc. / emitter junction

collector to base junc. / collector junc.

Emitter

* left hand side region of transistor
* Heavily doped than other 2 regions
* Supply majority carrier to base.
* Medium in size.
* Always FB wrt base so that it can supply large no. of majority carriers.

Base

* Narrow, middle region
* very thin and lightly doped.
  ↳ to reduce recombination.
* As base emitter region is FB, it offers low resistance for emitter current. It allows most of the majority carriers to collector.

Collector

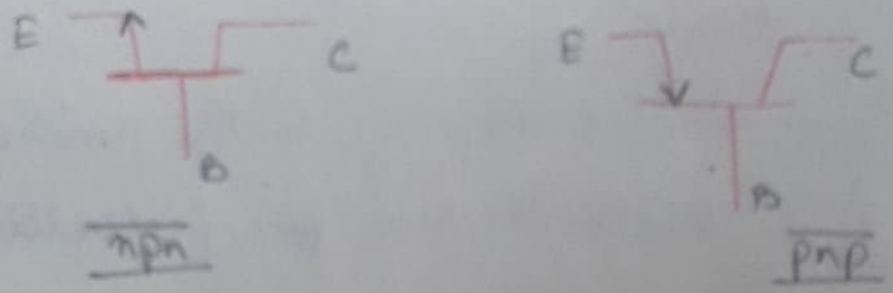
* Right hand region
* Moderately doped.

* Large in size as it has to dissipate power.

* collector region is always RB wrt base.

$$W \propto \sqrt{\frac{1}{N_A} + \frac{1}{N_D}}$$

$W_C > W_E \quad \therefore N_C < N_E$



npn pnp

Arrow gives dir^n of emitter current.

Modes of operation

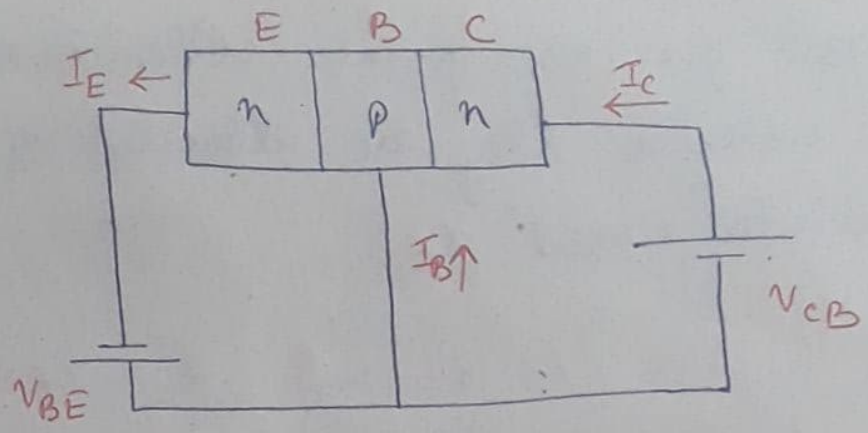
Forward Active : J_E – FB J_C – RB
used as amplifier

Saturation mode : J_E – FB J_C – FB
used as closed switch

cut off mode : J_E – RB , J_C – RB
used as open switch

Inverse active : J_E RB J_C FB
used as attenuator

operation of npn transistor



Case 1: When V_{BE} ON and collector unbiased.

* I_E. FB ⇒ depletion region width reduces.
* Majority carriers ie. e^- from emitter diffuse to base and majority carrier from base diffuse to emitter. This constitutes I_E.

Case 2 : When V_{CB} is ON and emitter is unbiased.

* width of depletion layer ↑.
* No flow of majority carriers
* Minority carriers flows.

Case 3 : When both are switched on.

* . Base emitter junction is FB and collector base is RB.

* FB causes e^-s to flow from n type emitter to p type base. Holes flow from p type base n type emitter.

* Majority carrier e^- after reaching base tend to combine with holes.
But base is lightly doped and thin so less

recombination happens

* Almost 98% free e^-s go into collector. once they reach collector they are attracted by V_{cc} This is collector current I_C.

* collector junction is RB and RB appears majority carrier flow and actual flow of minority carrier

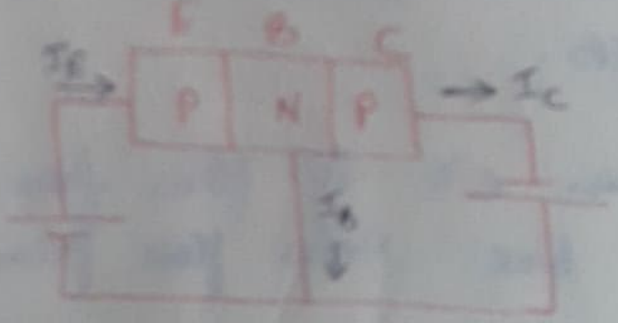
* Majority carrier is e^- from n side and hole from p side.

In p type, the majority carrier of n type i.e e^- are minority carrier in p type

∴ To collector junction, e^- appear as minority carrier and helps to cross the junction.

$$I_E = I_B + I_C$$

PNP operation



Majority carriers are holes

Mobility of e^- is greater than mobility of holes and fabrication of npn is easier ∴ - NPN is preferred

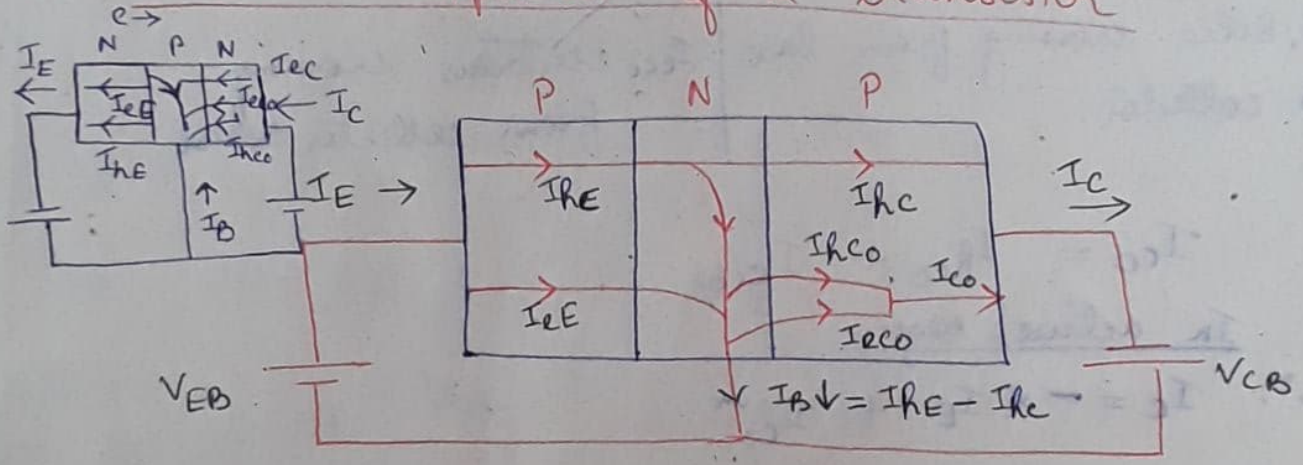
Q| In a certain transistor, emitter current is 1.02 times as large as that of collector current. If emitter current is 12mA. Find base current.

$$I_E = 1.02\, I_C$$

$$I_C = \frac{12\,m}{1.02} = 11.76\,mA$$

$$I_E = I_B + I_C = 12 - 11.76 = 0.235m$$

Current components of a transistor



* EB junc. FB and CB junct. is RB

* $I_E = I_{hE} + I_{eE}$

  I_{hE} ↓ hole current due to crossing of holes from E to B

  I_{eE} → electron current due to crossing of e⁻s from B to E.

* Emitter heavily doped as compared to base. Thus electron current I_{eE} is negligible compared to hole current.

* All the holes crossing E junc. donot reach C junc as some of them recombine with e⁻s in base.

~~* Hole current at collector region,~~

I_{hc} - hole current at collector region.

$\therefore I_B = I_{hE} - I_{hc}$

→ Since collector junction is RB, a reverse saturation current I_{co} flows.

Total collector current, $I_c = I_{hc} + I_{co}$

Now, I_{co} consist of 2 currents ie.

I_{hco}, holes crossing from base to collector | I_{eco} electrons crossing from collector to base

$$I_{co} = I_{hco} + I_{eco}$$

Types of configuration

When a transistor is to be connected in a circuit, one terminal is used as i/p terminal, one as o/p terminal and third one as common terminal.

1. Common Base (CB)
2. Common Emitter (CE)
3. Common collector (CC)

Current Amplification Factor

Ratio of change in o/p current to change in input current is called current amplification factor.

In CB configuration, current amplification factor, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

In CE conf, current amplification factor, $\beta = \frac{\Delta I_C}{\Delta I_B}$

In CC conf, " " " , $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Relation b/w α and β

We know, $\Delta I_E = \Delta I_C + \Delta I_B$

$\Delta I_C = \alpha \Delta I_E \quad \left[\because \alpha = \frac{\Delta I_C}{\Delta I_E}\right]$

$\Delta I_E = \alpha \Delta I_E + \Delta I_B$

$\Delta I_B = (1-\alpha) \Delta I_E$

÷ both sides by ΔI_C,

$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C} (1-\alpha)$

$$\Rightarrow \frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha)$$

$$\Rightarrow \boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Rearranging, we get $\boxed{\alpha = \frac{\beta}{1+\beta}}$ or $\boxed{\frac{1}{\alpha} - \frac{1}{\beta} = 1}$

→ Relation b/w α, β, γ

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Rightarrow \Delta I_B = \Delta I_E - \Delta I_C$$

$$\therefore \gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

÷ numerator and denominator on RHS by ΔI_E,

$$\gamma = \frac{\Delta I_E / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

$$\therefore \boxed{\gamma = \frac{1}{1-\alpha} = \beta + 1}$$

8| common base dc current gain of a transistor is 0.967. If emitter current is 10mA, what is the value of base current?

Given, $\alpha = 0.967 \quad I_E = 10mA$

$$\alpha = \frac{I_C}{I_E} = \frac{I_C}{10} \Rightarrow I_C = 0.967 \times 10 = 9.67mA$$

$$I_E = I_B + I_C$$

$$\Rightarrow 10 = I_B + 9.67$$

$$\Rightarrow \boxed{I_B = 0.33mA}$$

Q| If a transistor has α of 0.97, find value of β. If $\beta = 200$, find α.

$$\alpha = 0.97 \quad , \beta = \frac{\alpha}{1-\alpha} = \frac{0.97}{1-0.97} = 32.33$$

$$\beta = 200 \quad , \alpha = \frac{\beta}{1+\beta} = \frac{200}{1+200} = 0.995$$

Q| A transistor has $\beta = 150$. Find collector and base current if $I_E = 10\,mA$.

Given, $\beta = 150$, $I_E = 10\,mA$

$$\alpha = \frac{\beta}{\beta+1} = \frac{150}{150+1} = 0.993$$

Also, $\alpha = \frac{I_C}{I_E} \Rightarrow 0.993 = \frac{I_C}{10} \Rightarrow I_C = 9.93\,mA$

$$I_E = I_B + I_C$$

$$\Rightarrow I_B = 0.07\,mA$$

Q| When emitter current of a transistor is changed by 1 mA, there is change in collector current by 0.99 mA. Find current gain of transistor.

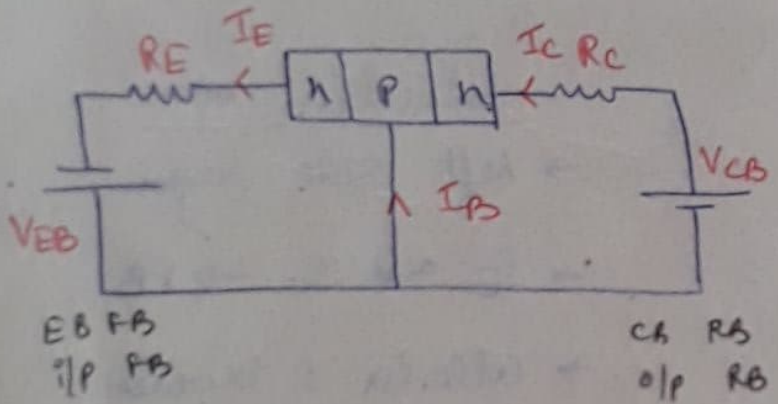
Sol^n $$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{0.99 \times 10^{-3}}{1 \times 10^{-3}} = 0.99$$

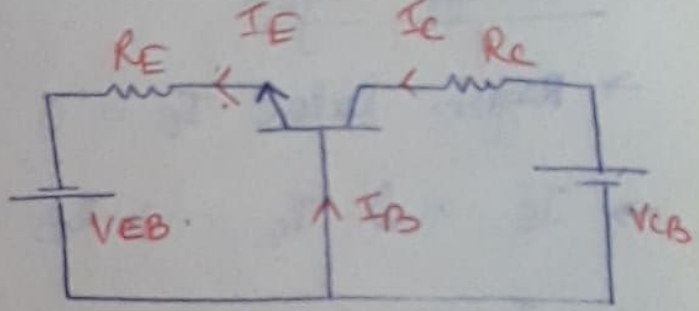
CB Configuration

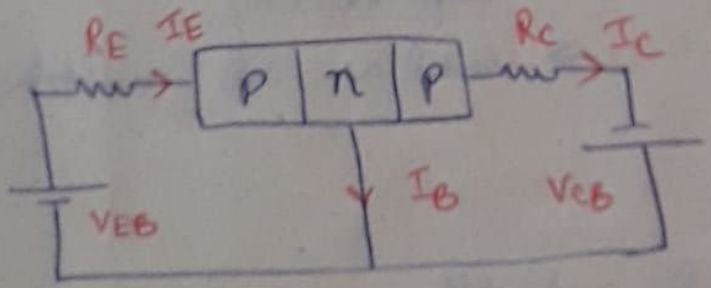
Emitter – i/p terminal

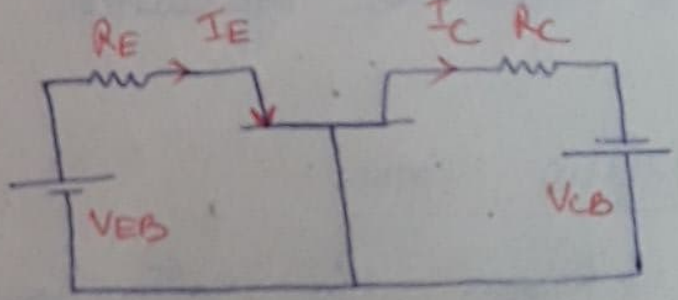
collector – o/p

Base – common



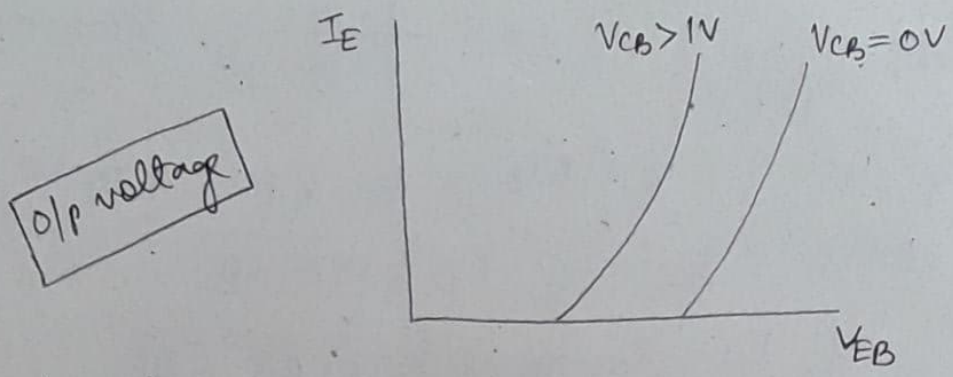






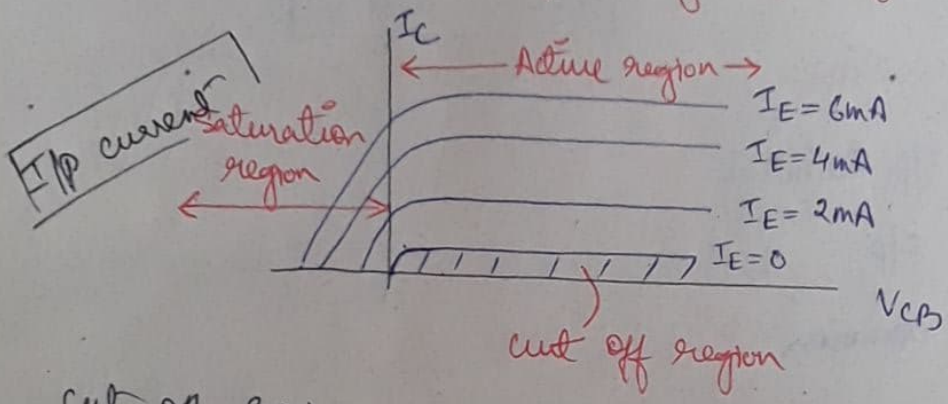
I/p characteristics of CB

Relates i/p current with i/p voltage for given o/p voltage



o/p characteristics of CB

Relates o/p current with o/p voltage for given i/p current



cut off region

→ Region below $I_E = 0$

→ J_E and J_C → RB

→ $I_C = I_{CBO}$

→ used as off switch

Saturation region

→ left side region

→ J_E and J_C → FB

→ collector I increases exponentially.

→ used as on switch

Active region

→ Region b/w saturation and cut off.

→ J_E FB, J_C RB

→ $\boxed{I_C = \alpha I_E + I_{CBO}}$ ← only for active region

→ used as amplifier.

I/p Resistance

$$R_i = \frac{\Delta V_{EB}}{\Delta I_E}$$

Low

O/p resistance

$$R_o = \frac{\Delta V_{CB}}{\Delta I_c}$$

High

	R_i	R_o	A_I	A_V	A_p
CB	Low	High	≈ 1	High	Low (compared to CE)

Application of CB

RF amplifier, wide band amplifier.

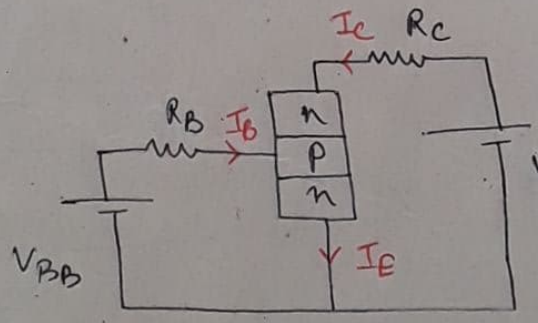
~~Q) A transistor in CB has~~

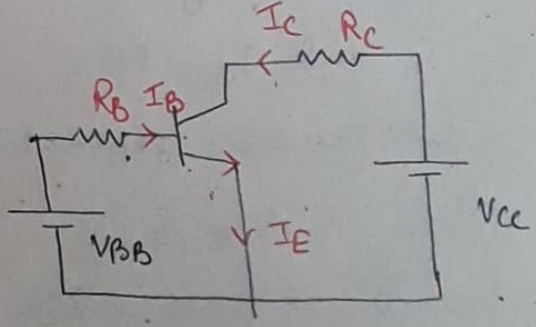
CE configuration

Base — i/p terminal

Emitter — common

Collector — o/p terminal



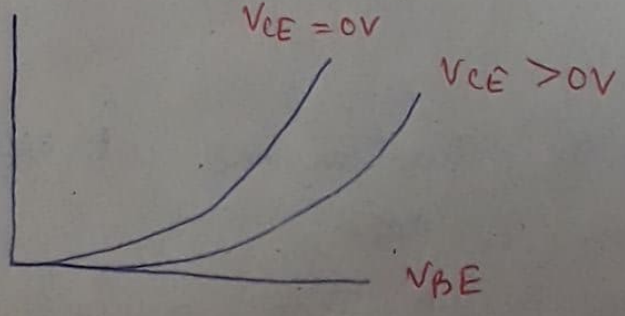


EB FB
i/p FB

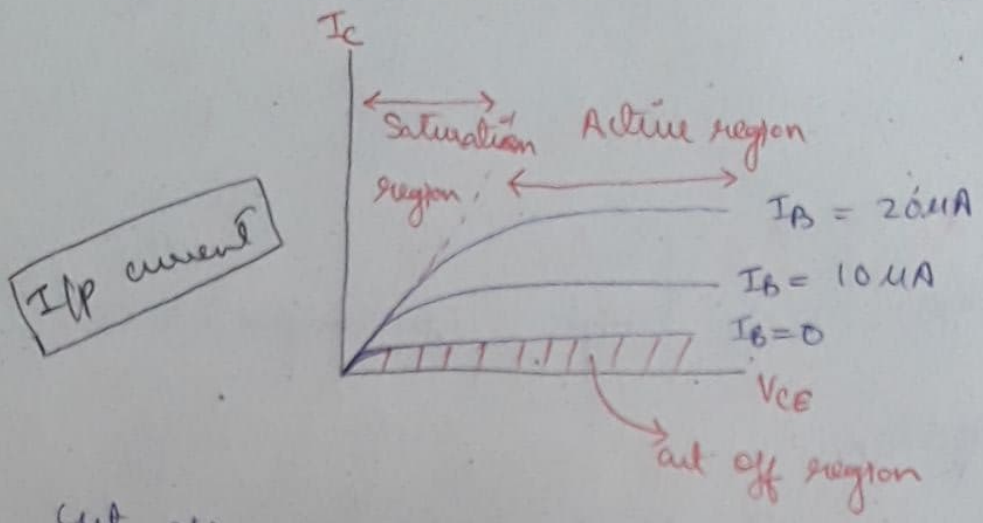
C RB
o/p RB

I/p characteristics of CE

o/p voltage



o/p characteristics of CE



cut off region

Below $I_B = 0$

J_E and J_C → RB

$I_C = (1+\beta)\ I_{CBO}$ where $I_B = 0$

$V_{CE} = V_{CC}$

used as OFF switch

Saturation region

J_E and J_C FB

I_C increases exponentially

$V_{CE} \leq V_{CE(sat)}$

used as ON switch

$V_{CE} = 0.2/0.3\ V$ for Si transistor

$V_{CE} = 0.1\ V$ for Ge transistor

Active

Region b/w saturation and cut off

J_E FB, J_C RB

$I_C = \beta I_B + (1+\beta)\ I_{CBO}$ → used as amplifier

Input resistance

$$R_i = \frac{\Delta V_{BE}}{\Delta I_B}$$

o/p resistance

$$R_o = \frac{\Delta V_{CE}}{\Delta I_C}$$

$A_I \rightarrow \frac{o/p}{i/p}$

CE

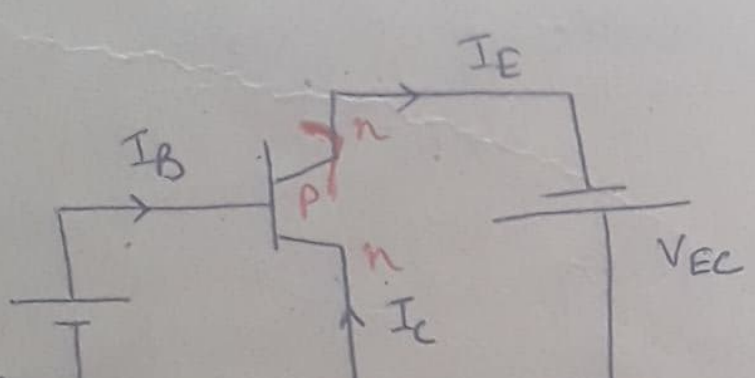
R_i	R_o	A_I	A_V	A_P
Medium	Medium	High	High	High

Applications

1. Audio frequency circuits
2. wide band amplifier.

CC configuration

Base – i/p terminal collector – common emitter – o/p.



XB FB
E FB
i/p FB

For CC

$V_{CE} = V_{CB} + V_{BE}$
+ve +ve +ve

NPN
E B C

$V_E < V_B$ FB

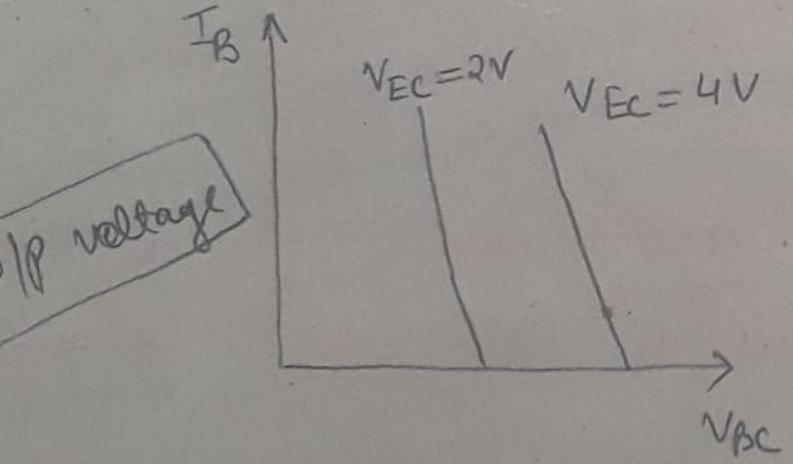
$V_{BE} \rightarrow +ve$
$\Rightarrow V_B - V_E$ +ve

V_{CB} RB

$V_C > V_B$
$\Rightarrow V_C - V_B$ +ve

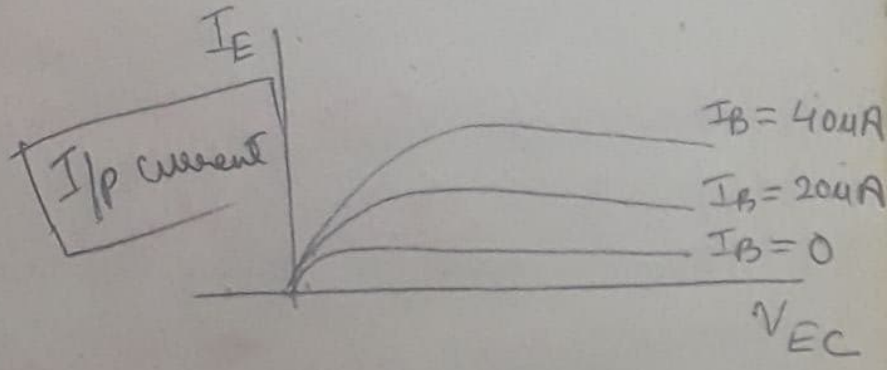
$V_C > V_E$
(+) (−)
$V_C - V_E > 0$

I/p characteristics



o/p characteristics

Same as CE configuration



I/p resistance

$$R_i = \frac{\Delta V_{BC}}{\Delta I_B}$$

O/p resistance

$$R_o = \frac{\Delta V_{EC}}{\Delta I_E}$$

Application $\leftarrow$ Buffer
Impedance matching

R_i	R_o	A_I	A_V	A_P
High	Low	High	Less than 1	Low

Q) A transistor in CB has $I_C = 2.98\ mA$, $I_E = 3mA$ and $I_{CO} = 0.01mA$. What current will flow in collector when connected in CE configuration with base current $30\mu A$.

Given,

$$I_C = 2.98\ mA,\ I_E = 3mA,\ I_{CO} = 0.01\ mA$$

For CB :

$$I_C = \alpha I_E + I_{CO}$$

$$\alpha = \frac{I_C - I_{CO}}{I_E} = \frac{(2.98 - 0.01) \times 10^{-3}}{3 \times 10^{-3}} = 0.99$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1 - 0.99} = 99$$

For CE :

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$= 99 \times 30 \times 10^{-6} + (1+99) \times 0.01 \times 10^{-3}$$

$$= 3.97\ mA$$

Transistor Biasing

The basic function of a transistor is to amplify weak signal (amplifier) or ON / OFF switch.

Biasing

In order to produce distortion free O/P, supply voltage and resistance in the circuit must be choosen suitably.

~~These~~

current I_C and I_B and voltage V_{BE} and V_{CE} are reqd. to set by biasing circuit.

Proper values of current and voltage allow transistor to amplify weak signal.

Process of providing a fixed value of current which should flow through transistor with fixed voltage drop across transistor junction.

If amplifier is not biased with correct dc voltage it can go into saturation or cut off.

The values of current and voltage defines a point at which transistor operates. This pt. is called operating pt or quiescent pt or Q pt.

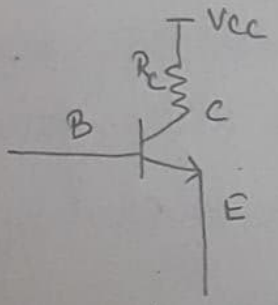
Method of establishing Q pt is called biasing.

Ckts used for getting proper operating pt is biasing ckt.

operating pt should be always in active region.

DC Load Line

For CE ckt

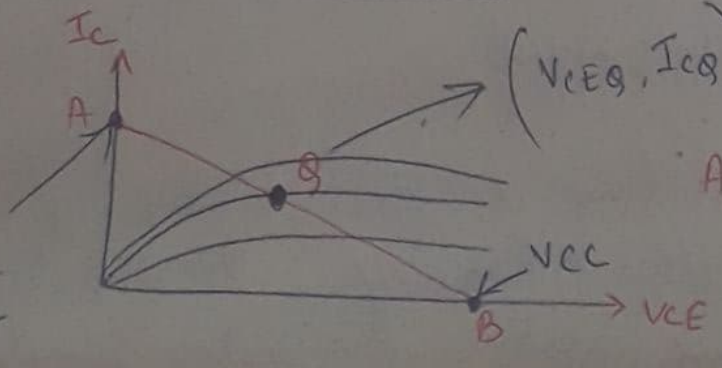


Applying KVL,

$$V_{CC} = I_C R_C + V_{CE}$$

Put $V_{CE} = 0 \Rightarrow \boxed{I_C = \frac{V_{CC}}{R_C}}$ ← coordinates of A

Put $I_C = 0 \Rightarrow \boxed{V_{CE} = V_{CC}}$ ← coordinates of B



AB is DC load line

$V_{CEQ} = \frac{V_{CC}}{2} = \frac{V_{CE}}{2}$

$I_{CQ} = \frac{I_C}{2}$

→ ~~Q pt~~ DC load can be drawn if R_c and V_{cc} are known.

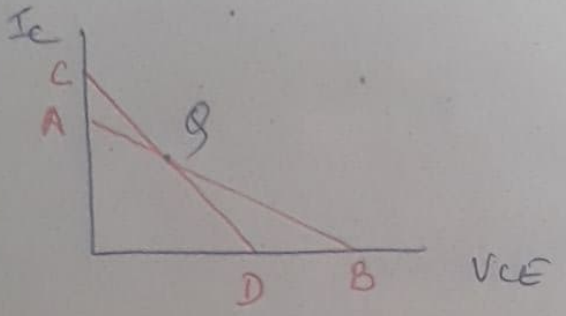
→ Q pt is mid pt. of dc load line AB.

→ Q pt must be in active region.

AC load line

AC load line should pass through Q pt.

Intersection of DC and AC load line gives Q pt.



AB – DC load line

CD – AC load line

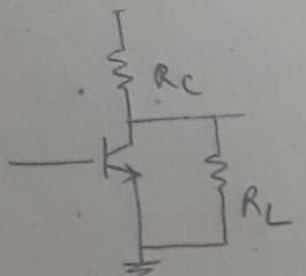
DC load line is less steep than AC load line.

To find AC load line

$$V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$$

$$I_c = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

$$\boxed{R_{ac} = R_c \parallel R_L}$$



Q| Given. $R_c = 8k\Omega$, $R_L = 24k\Omega$ and $V_{cc} = 24V$. Draw DC load line and determine operating pt. Also draw ac load line.

Soln

DC load line

$$V_{CC} = V_{CE} + I_C R_C$$

coordinate of A

Put $V_{CE} = 0$

$\Rightarrow V_{CC} = I_C R_C$

$\Rightarrow I_C = \frac{V_{CC}}{R_C} = \frac{24}{8k} = 3mA$

coordinate of B

Put $I_C = 0$

$\Rightarrow V_{CC} = V_{CE} = 24V$

Q point

Middle pt. of AB

$$V_{CEQ} = \frac{V_{CE}}{2} = 12V$$

$$I_{CQ} = \frac{I_C}{2} = \frac{3}{2} = 1.5\ mA$$

Ac load line

$$R_{ac} = R_C \| R_L = \frac{8 \times 24}{8+24} = 6k\Omega$$

$$V_{CE} = V_{CEQ} + I_{CQ} R_{ac}$$

$$= 21V$$

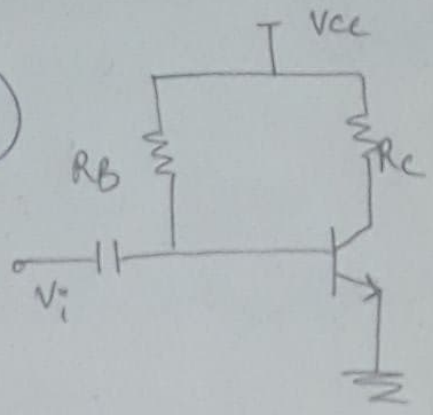
$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 3.5\ mA.$$

Q) Design the ckt shown, given Q pt values are $I_{CQ} = 1mA$, $V_{CEQ} = 6V$. Assume $V_{CC} = 10V$, $\beta = 100$ and $V_{BE(on)} = 0.7V$

Sol^{n}

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} \quad (\text{using KVL})$$

$$= \frac{10-6}{1\times10^{-3}} = 4\,k\Omega$$



$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\times10^{-3}}{100} = 10\,\mu A$$

$$R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}} = \frac{10-0.7}{10\times10^{-6}} = 0.93\,M\Omega$$

Hint

For DC load line

Put $I_C = 0$, $\boxed{V_{CE} = V_{CC}}$

$$V_{CEQ} = \frac{V_{CE}}{2} = \frac{V_{CC}}{2} = 5\,V$$

$V_{CC} = 12V$

$V_{CEQ} = 7V$

$V_{CEQ} = V_{CE}$

$I_{CQ} = I_C$

Thermal Runaway

For CE amplifier

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

→ β, I_B and I_{CO} increase with temperature

→ I_{CO} doubles for every 10°C rise in temperature

→ When I_{CO} increases, I_C increases

$$I_C = I_{CH} + I_{CO}$$

→ This causes power dissipation to increase as collector dissipates power

⇒ I_{CO} ↑, I_C ↑ and the process is cumulative leads to thermal Runaway and destroys the

transistor

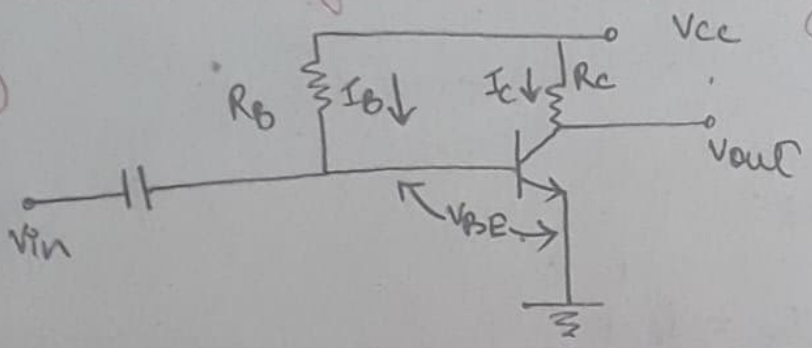
→ Q pt shifts due to change in temperature and transistor can be driven to saturation.

If ckt is designed such that base current I_B decrease with rise in temperature, then decrease in βI_B will compensate for increase in $(1+\beta) I_{CO}$ and keeps I_C almost constant.

In power transistors, the heat developed at collector junction may be removed by use of heat sink, metal sheet fitted to collector which radiates heat quickly.

Methods of transistor biasing

① Fixed bias or base resistor method



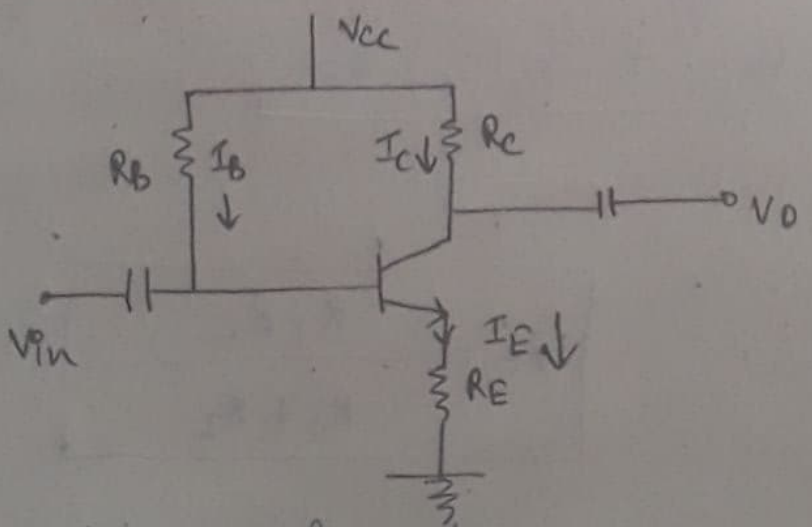
* $V_{CC} = I_B R_B + V_{BE}$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\frac{dI_B}{dI_C} = 0 \Rightarrow * \quad S = 1 + \beta$$

β is large
⇒ stability poor

② Emitter Feedback bias



For base emitter loop

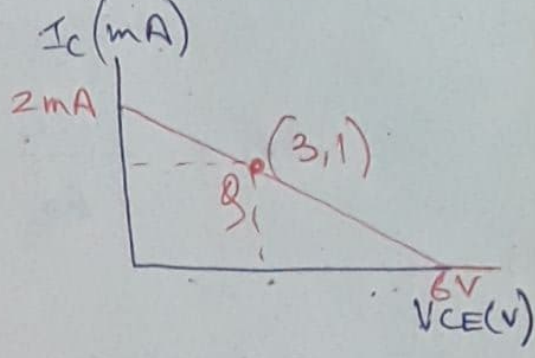
$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

For collector emitter loop

KVL $\Rightarrow$ $V_{CC} = I_C R_C + V_{CE} + I_E R_E$

$$S = \frac{1 + \beta}{1 + \beta \dfrac{R_E}{R_E + R_B}}$$

8| In fixed bias compensation for a silicon transistor with $\beta = 100$ is used. $V_{cc} = 6V$, $R_c = 3k\Omega$, & $R_B = 530\,k\Omega$. Draw dc load line and determine operating pt. what is stability factor.



Soln

DC load line

$$V_{cc} = V_{CE} - I_C R_C$$

Put $I_C = 0 \Rightarrow V_{CE} = V_{cc} = 6V$.

Put $V_{CE} = 0 \Rightarrow I_C = \frac{V_{cc}}{R_c} = \frac{6}{3\times10^3} = 2mA$

Q pt

$$V_{CEQ} = \frac{V_{CE}}{2} = 3V$$

$$I_{CQ} = \frac{I_{CQ}}{2} = 1mA$$

$$S = 1+\beta = 1+100 = 101$$

9| For emitter FB bias circuit, $V_{cc} = 10V$, $R_c = 1.5k\Omega$, $R_B = 270\,k\Omega$ and $R_E = 1\,k\Omega$. Assuming $\beta = 50$, $V_{BE} = 0$. Determine (a) stability factor (b) I_B (c) I_C.

Soln

(a) $$S = \frac{1+\beta}{1+\beta\frac{R_E}{R_E+R_B}} = \frac{1+50}{1+\frac{50\times1\times10^3}{1\times10^3+270\times10^3}}$$

$$= 43.04$$

(B)

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0 \qquad \left(\beta = \frac{I_C}{I_B}\right)$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0$$

$$\Rightarrow V_{CC} - V_{BE} = I_B R_B + I_B R_E + R_E I_C = 0$$

~~$\Rightarrow V_{CC} - V_{BE} = I_B [R_B \{ R_E (1 +$~~

$$\Rightarrow V_{CC} - V_{BE} = I_B R_B + I_B R_E + \beta I_B R_E$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E(H_B)} = \frac{10 - 0.7}{27 \times 10^3 + 51 (1 \times 10^3)}$$

$$= 28.97\ \mu A$$

(c) $I_C = \beta I_B = 50)$ ~~(1.45m~~ (28.97×10^{-6})

$$= 1.45\ mA$$

8/Given, supply of 24V, $\beta = 110$, $I_{CQ} = 4mA$, $V_{CEQ} = 8V$ and $V_E = \frac{V_{CC}}{8}$. Find I_B, I_E and R_E

Soln

$\because \frac{V_{CC}}{2} \neq V_{CEQ}$ $\therefore V_{CE} = V_{CEQ}$

$I_C = I_{CQ}$

$\rightarrow I_B = \frac{I_{CQ}}{\beta} = \frac{4 \times 10^3}{110} = 36.36\mu A$

$\rightarrow I_E = I_B + I_C = 36.36 \times 10^{-6} + 4 \times 10^{-3}$

$= 4.03636mA$

$\rightarrow$ ~~$R_E = \frac{V_E}{I_E} = \frac{0.3}{\quad}$~~ $V_E = \frac{V_{CC}}{8} = \frac{24}{8} = 3V$

$R_E = \frac{V_E}{I_E}$

$= 743.244$

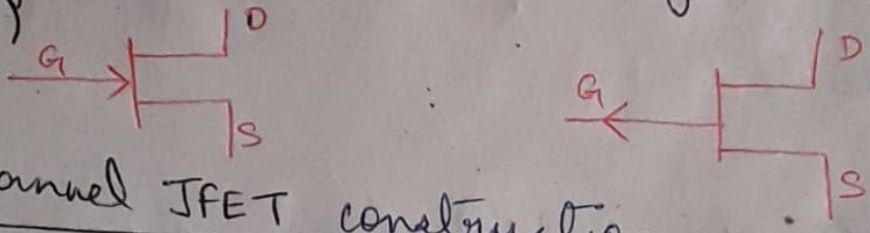
Field Effect Transistor

- JFET
- MOSFET

* FET is a unipolar 3 terminal device.
* In FET, flow of current is controlled by electric field.
  - current conduction only by majority carriers

⇒ Depending upon majority carriers, JFET classified

- n channel JFET (majority carriers are e⁻s)
- p channel JFET (majority carriers holes)



⇒ N channel JFET construction

It consist of a n type si material with two diffused p regions.

Source - Electrons which are majority carriers enter to the n type material through source

Drain - majority carriers leave the material through drain.

Gate – Heavily doped P type silicon diffused both sides of n type Si.

Channel – Region between the depletion region is channel. Majority carrier moves through channel.

→ Operation

① When $V_{GS} = 0$ and $V_{DS} = 0$

Thickness of depletion region is uniform

② When $V_{DS} = 0$ and V_{GS} decreased from zero or V_{GS} negative

PN junction is RB and thickness of depletion region increases

As more RB is applied means more –ve V_{GS} is applied thickness of depletion region again increases until two regions make contact with each other.

The channel is said to be cut off.

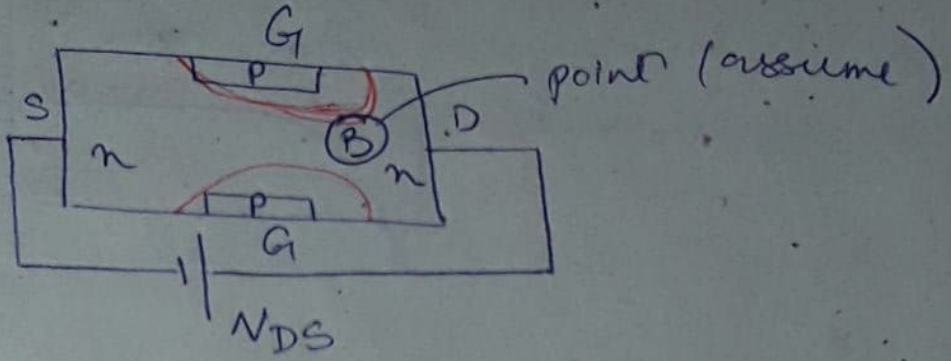
② When $V_{GS} = 0$ and V_{DS} is increased or +ve V_{DS}

→ Drain is +ve wrt source
→ Majority carrier flow from S to D.

As drain is more +ve, so RBB more RB

∴ Thickness of depletion region increases

∴ The channel is wedge shaped.



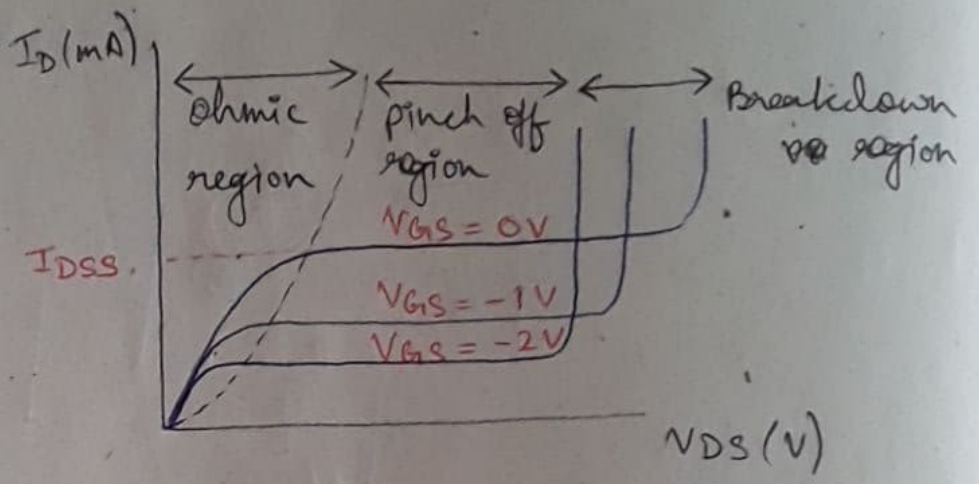
As V_{DS} ↑, cross section of channel decreases

The value of V_{DS} at which cross section ~~at B~~ area of channel at B is minimum is called Pinch off voltage, V_p and channel is said to be pinched off.

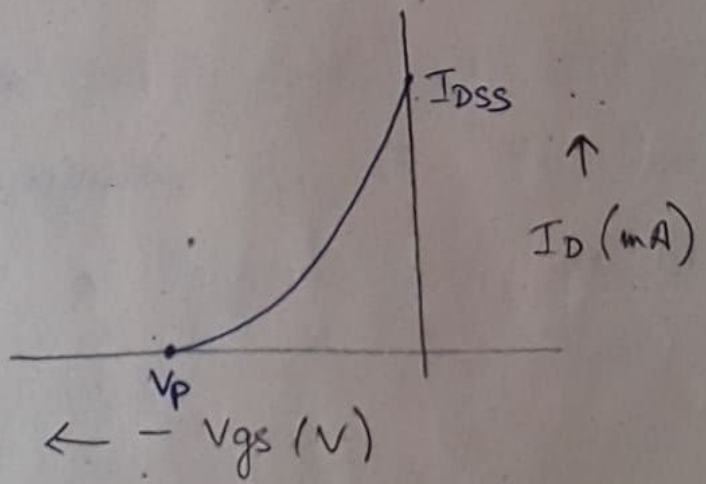
Channel acts as a resistor and JFET can be used as voltage variable resistor (or) voltage dependent resistor

IV characteristics of JFET

① Drain characteristics



② Transfer characteristics



JFET current equation

$$I_D = I_{DSS}\left(1 - \frac{V_{gs}}{V_{gs(off)}}\right)^2$$

Also, $V_P = |V_{gs(off)}| \Rightarrow I_D = I_{DSS}\left(1 - \frac{V_{gs}}{V_P}\right)^2$

↓

value of I_D when $V_{gs} = 0$

Application of FET

1. Used as buffer in measuring instruments
2. used as RF amplifier in FM tuner.
3. used as voltage variable resistor in operational amplifier.
4. used in low frequency amplifier in hearing aid
5. used in computers
6. Used in oscillators

Comparison of BJT and FET

FET	BJT
1. unipolar device ie depends only on majority carriers	1. Bipolar device ie depends on majority and minority carriers
2. No junction	2. Junction present
3. less noisy	3. More noisy

FET

(4) High input impedance

(5) voltage controlled device ie voltage at i/p controls o/p current

(6) Easy to fabricate

(7) -ve temp^{n}. coeff. at high current level

(8) Speed more

BJT

(4) Low input impedance.

(5) current controlled device as i/p current controls o/p current

(6) Fabrication complex than FET

(7) +ve temp^{n}. coff. at high current level.

(8) Speed less.