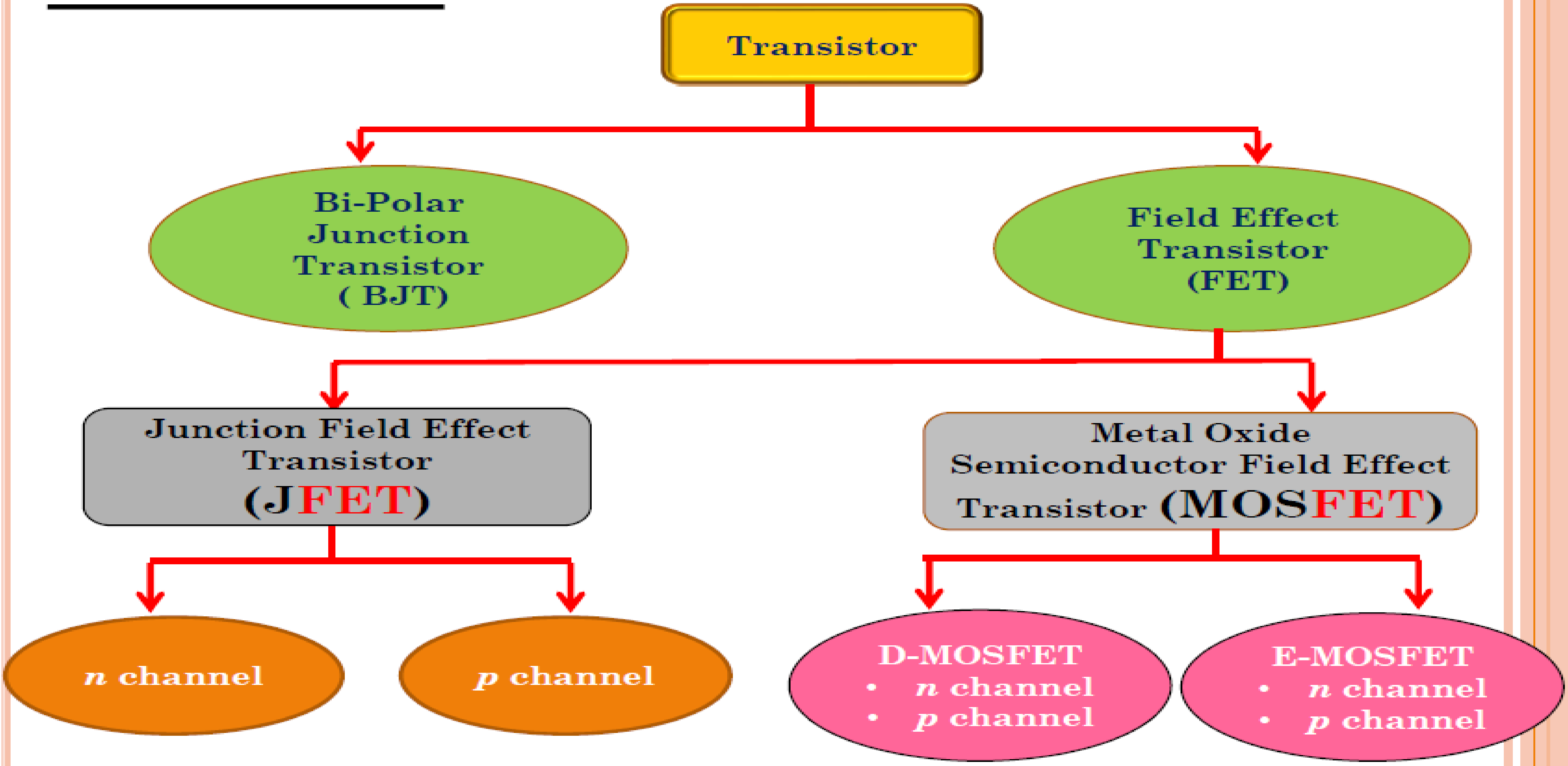
OVERVIEW


Transistor
Bi-Polar Junction Transistor (BJT)
Field Effect Transistor (FET)
Junction Field Effect Transistor (JFET)
Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
n channel
p channel
D-MOSFET
• n channel
• p channel
E-MOSFET
• n channel
• p channel

THE FIELD-EFFECT TRANSISTOR

- The FET is a single carrier device and is often called the **unipolar transistor** because the carriers involved in the operation are **either electrons or holes**.

- The FET is also a semiconductor device in which the output quantity is **controlled by an electric field**, which is often the input quantity.

- The phenomenon where the conductivity of the semiconductor is modulated by an electric field applied normally to the surface of the semiconductor is called ***field effect***,

- This principle is brought into operation by **extending the depletion region** deep into the bulk of the semiconductor.

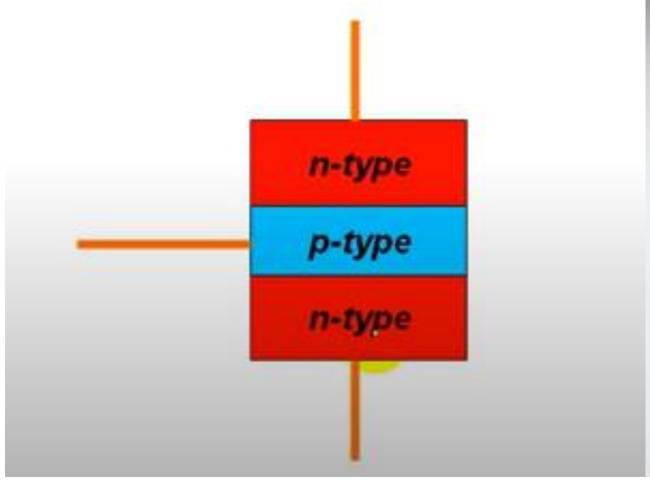
THE FIELD-EFFECT TRANSISTOR

- **Junction Field-effect Transistor (JFET):-** In a junction FET, the **control voltage modulates** the depletion width of a reverse-biased *p-n junction which, in* turn, varies with the various parameters of the device.

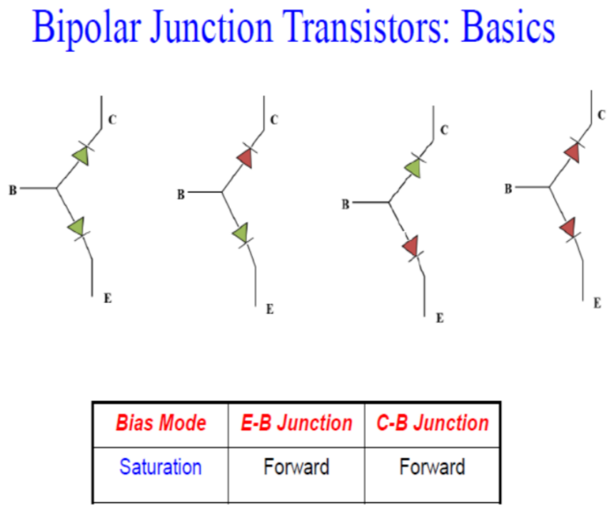
- **Insulated Gate Field-effect Transistor (IGFET):-** The IGFET is also called the metal-oxide-semiconductor field-effect transistor (MOSFET). In this, the metal gate electrode is separated from the semiconductor by an insulator.

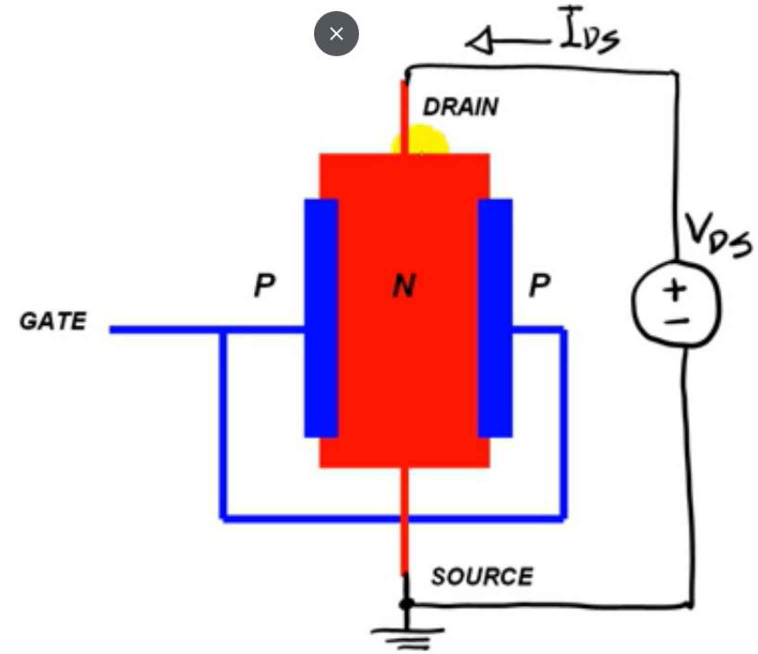
- **Metal-semiconductor Field-effect Transistor (MESFET):-** If the MOS junction is replaced by a direct metal-semiconductor contact, i.e., a Schottky barrier, it is called metal-semiconductor FET (MESFET). A MESFET is similar to a JFET except for the following differences:

(i) It has a single gate (ii) The gate is formed by a metal-semiconductor junction

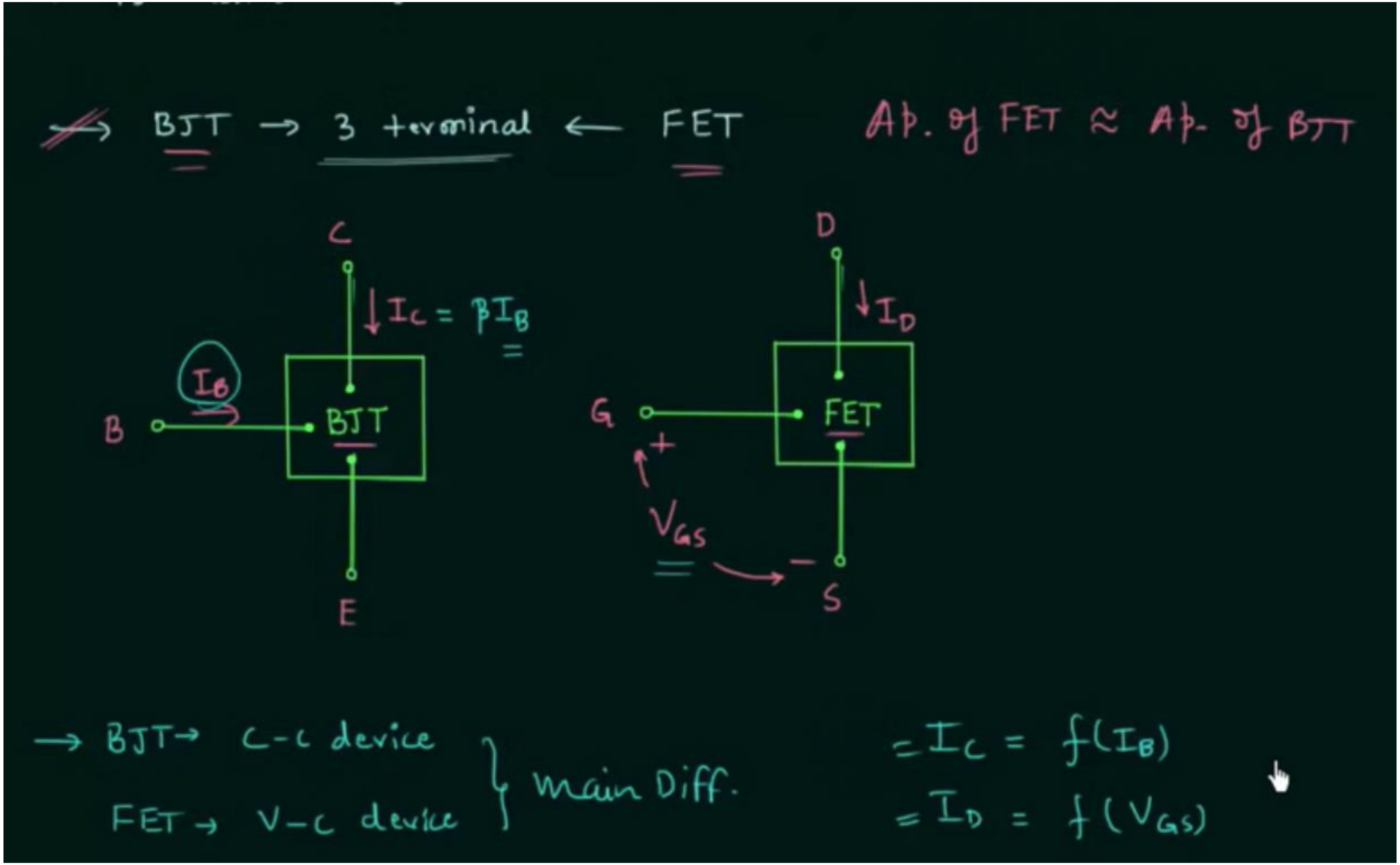

n-type
p-type
n-type


Different Regions of Operation
Active Region
Amplification
Cut-off Region
Switching
Saturation Region

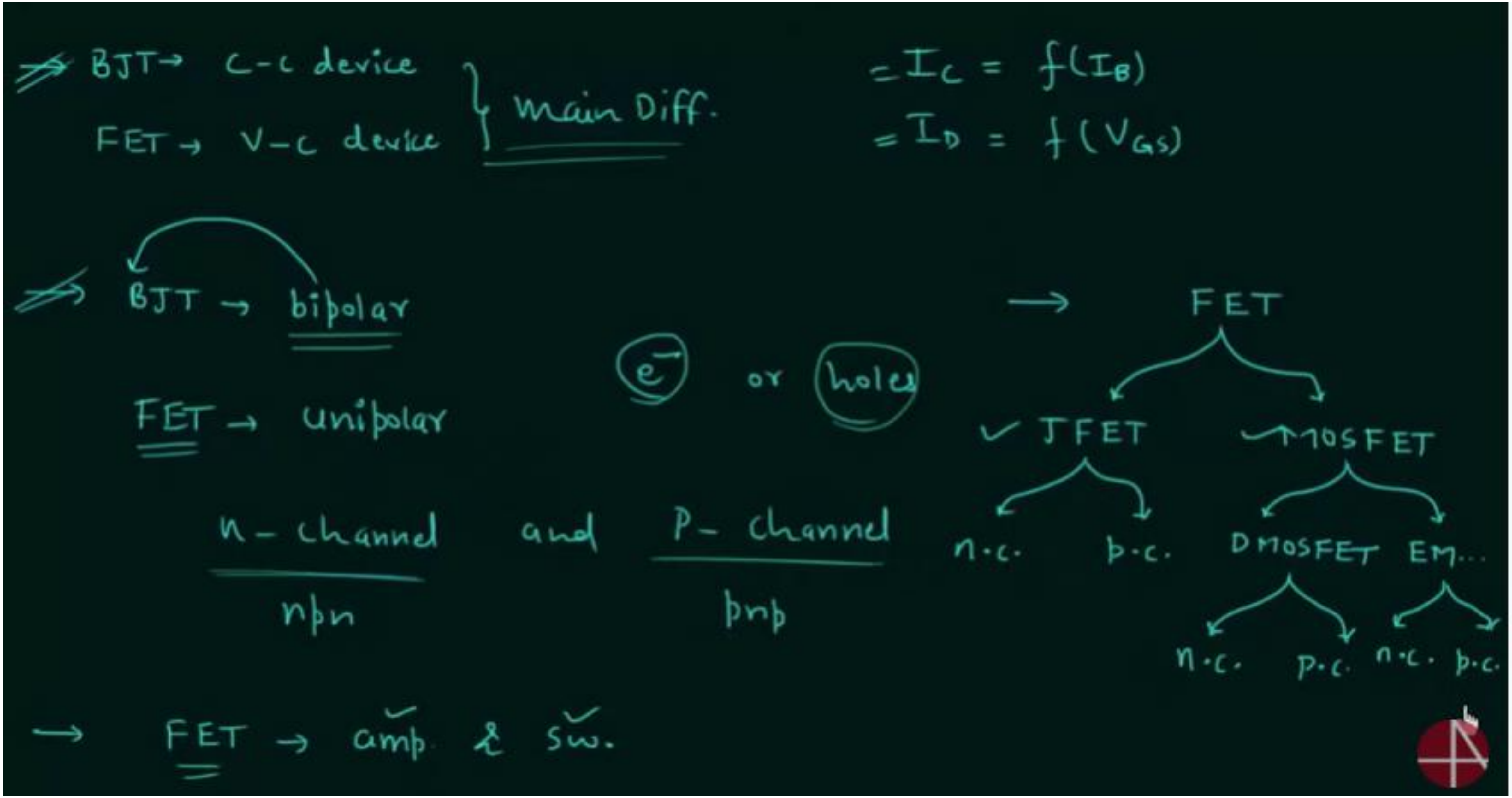

Bipolar Junction Transistors: Basics
Bias Mode
E-B Junction
C-B Junction
Saturation
Forward
Forward


I_{DS}
DRAIN
V_{DS}
GATE
P
N
P
SOURCE

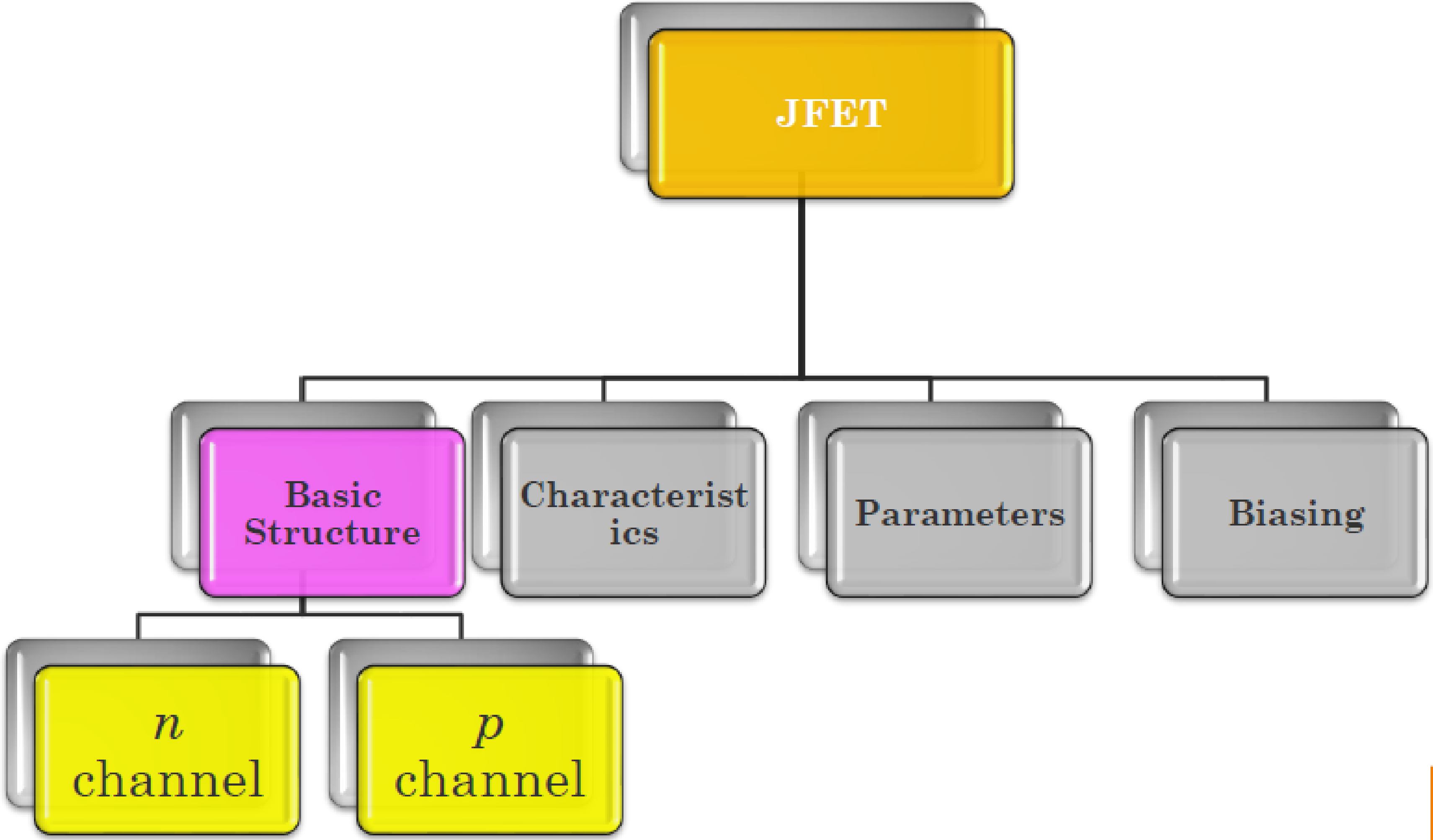
Field effect Transistors



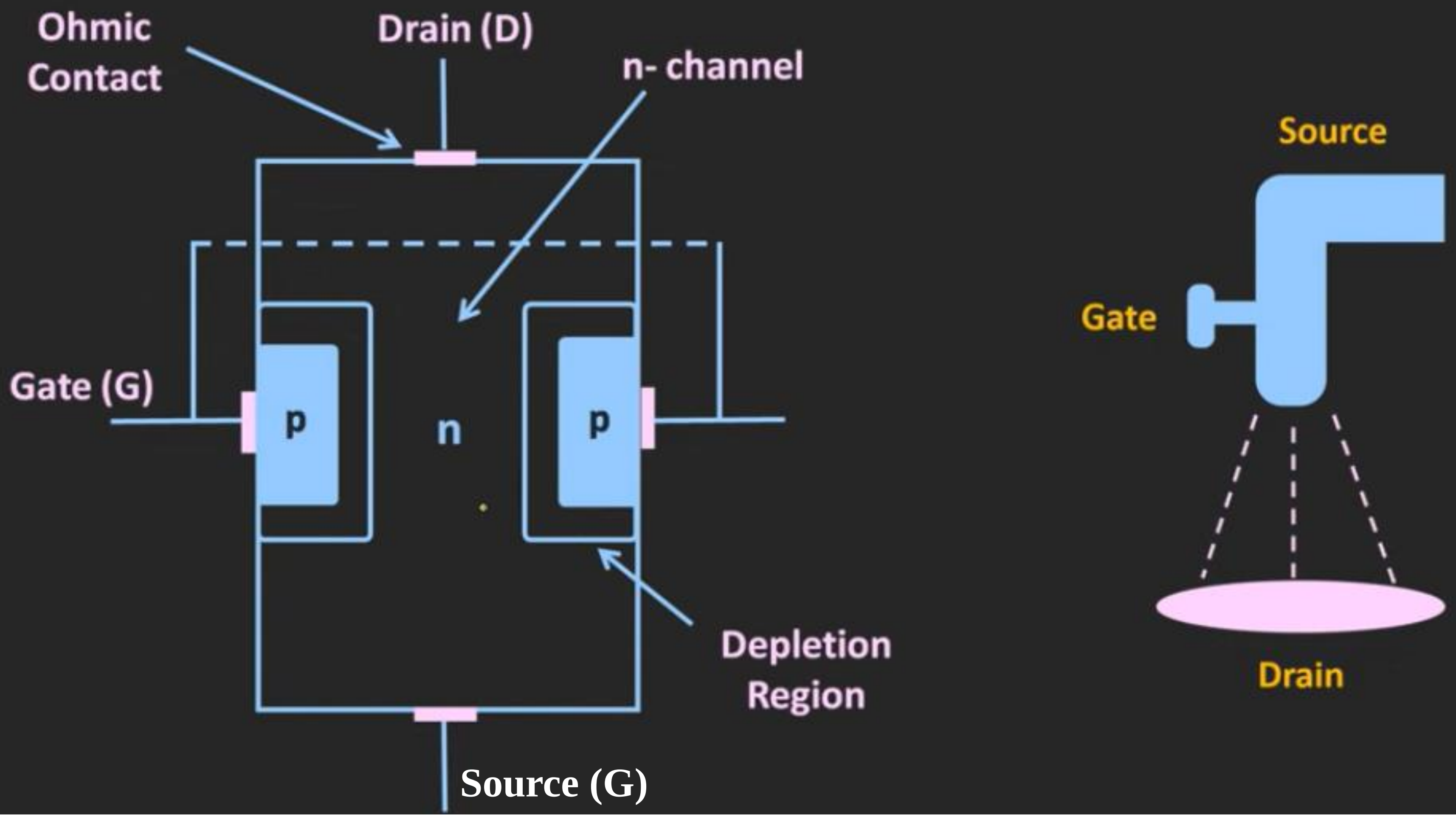
Field effect Transistors

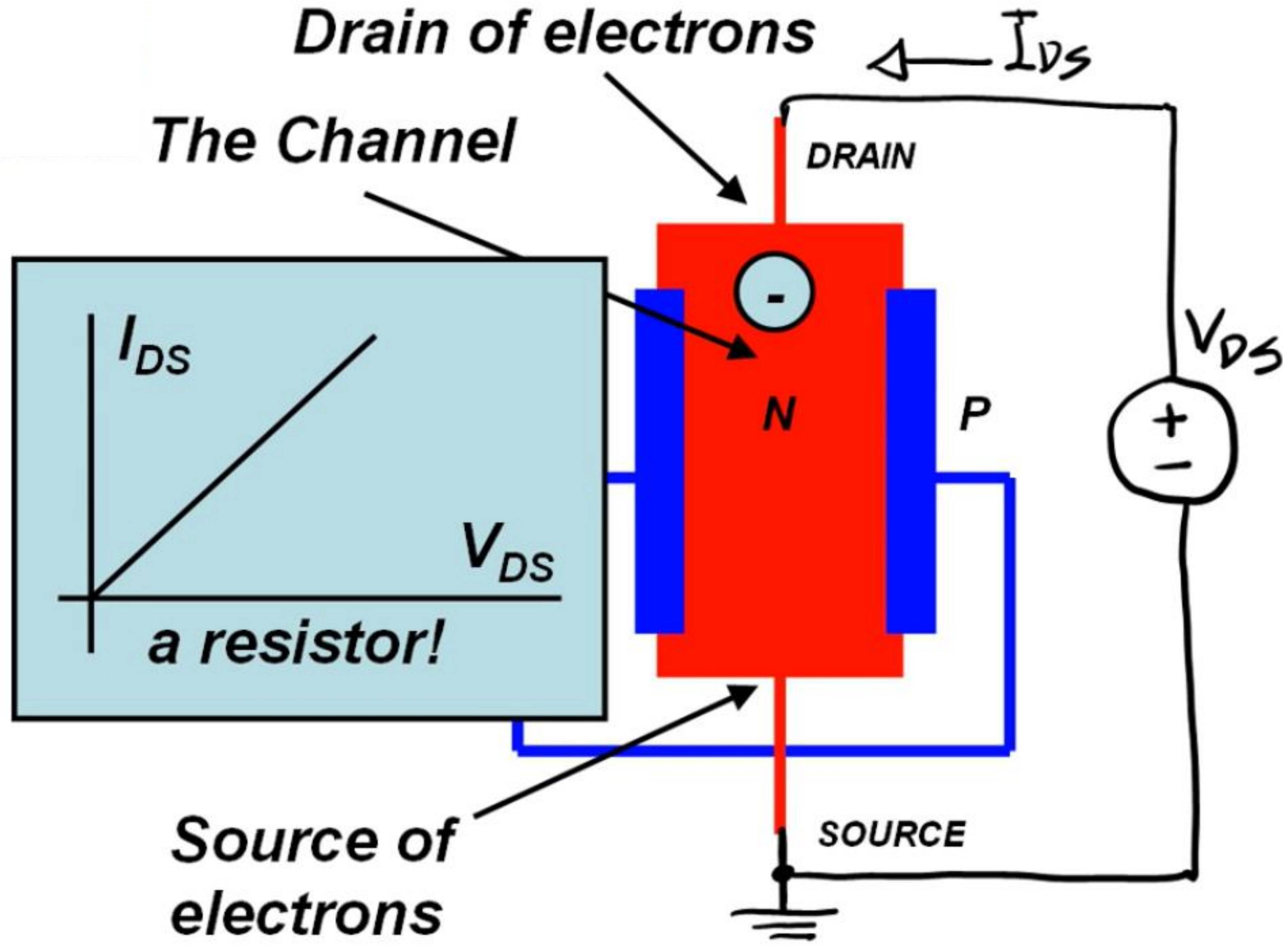


JFET

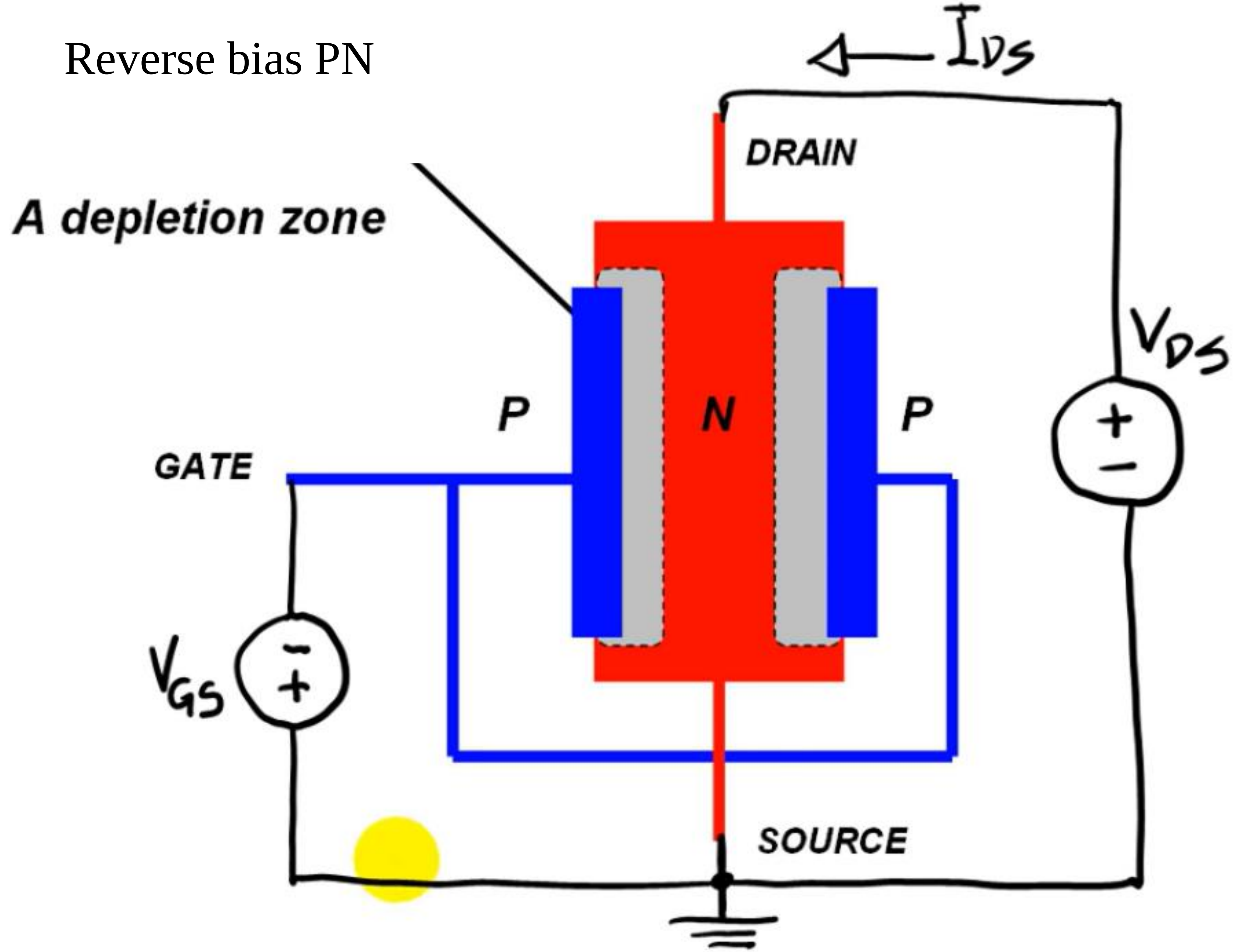

JFET
Basic Structure
Characteristics
Parameters
Biasing
n channel
p channel

Junction Field Effect Transistor (JFET)

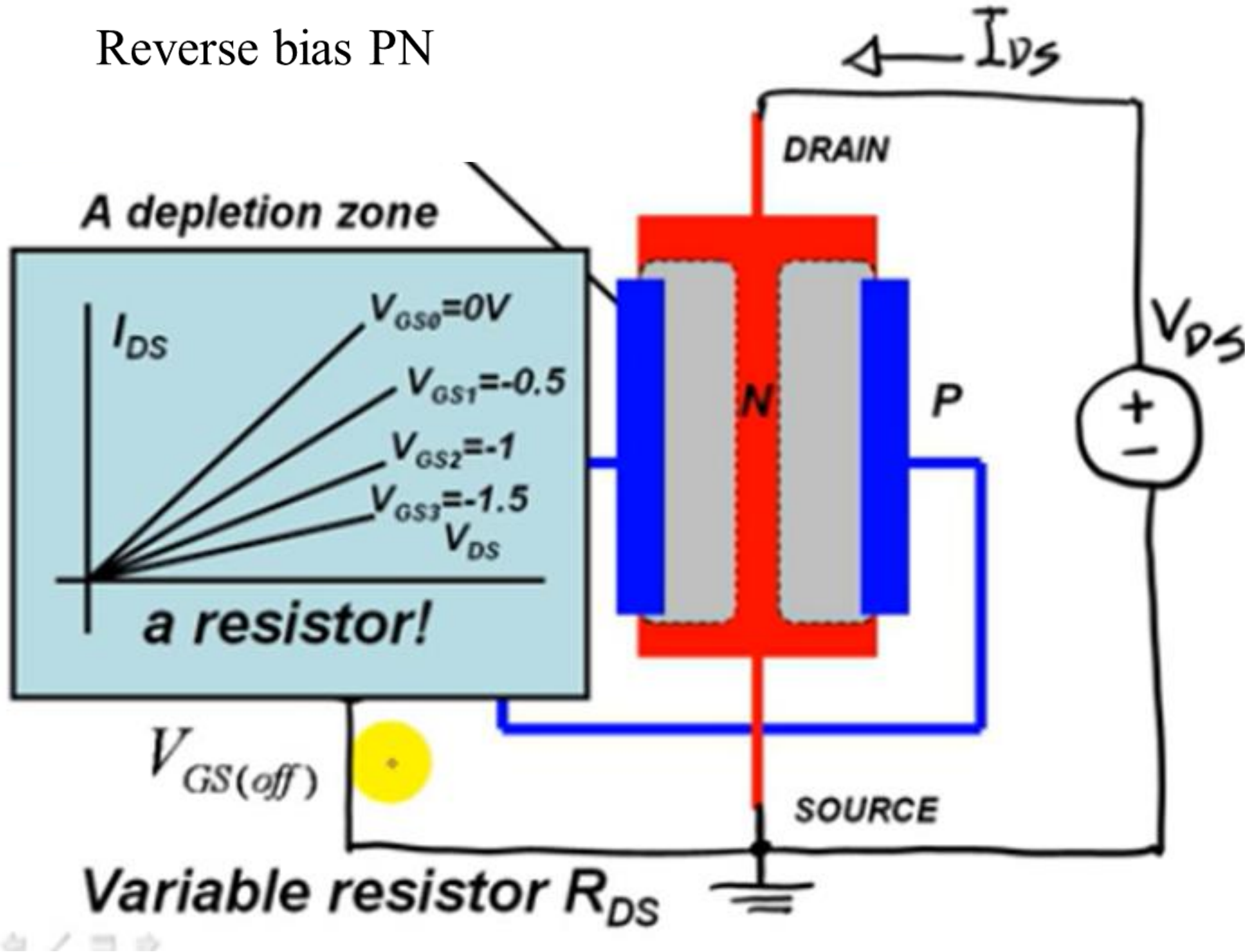



Drain of electrons
IDS
The Channel
DRAIN
-
IDS
VDS
N
P
VDS
+
−
a resistor!
Source of electrons
SOURCE

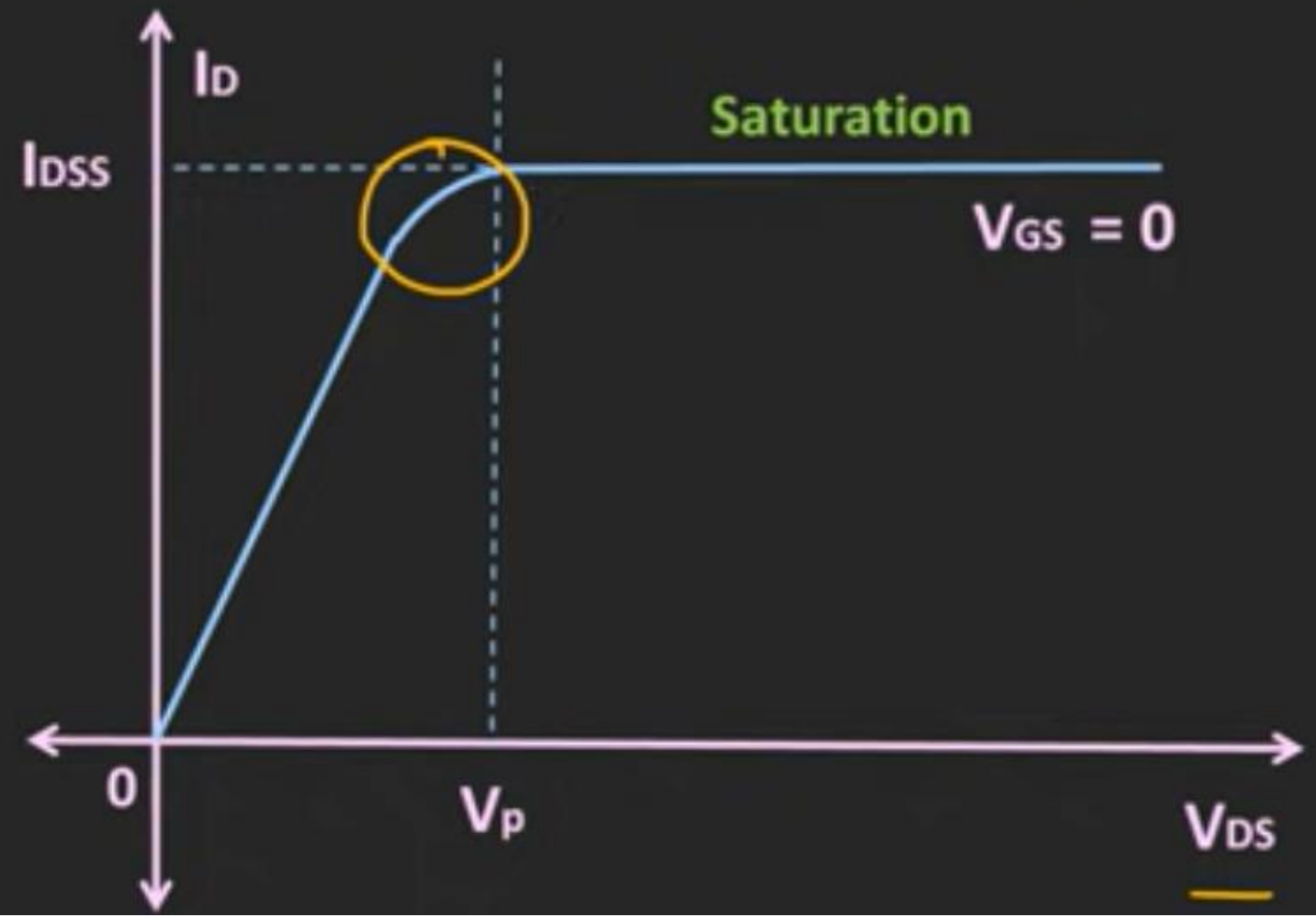
Reverse bias PN



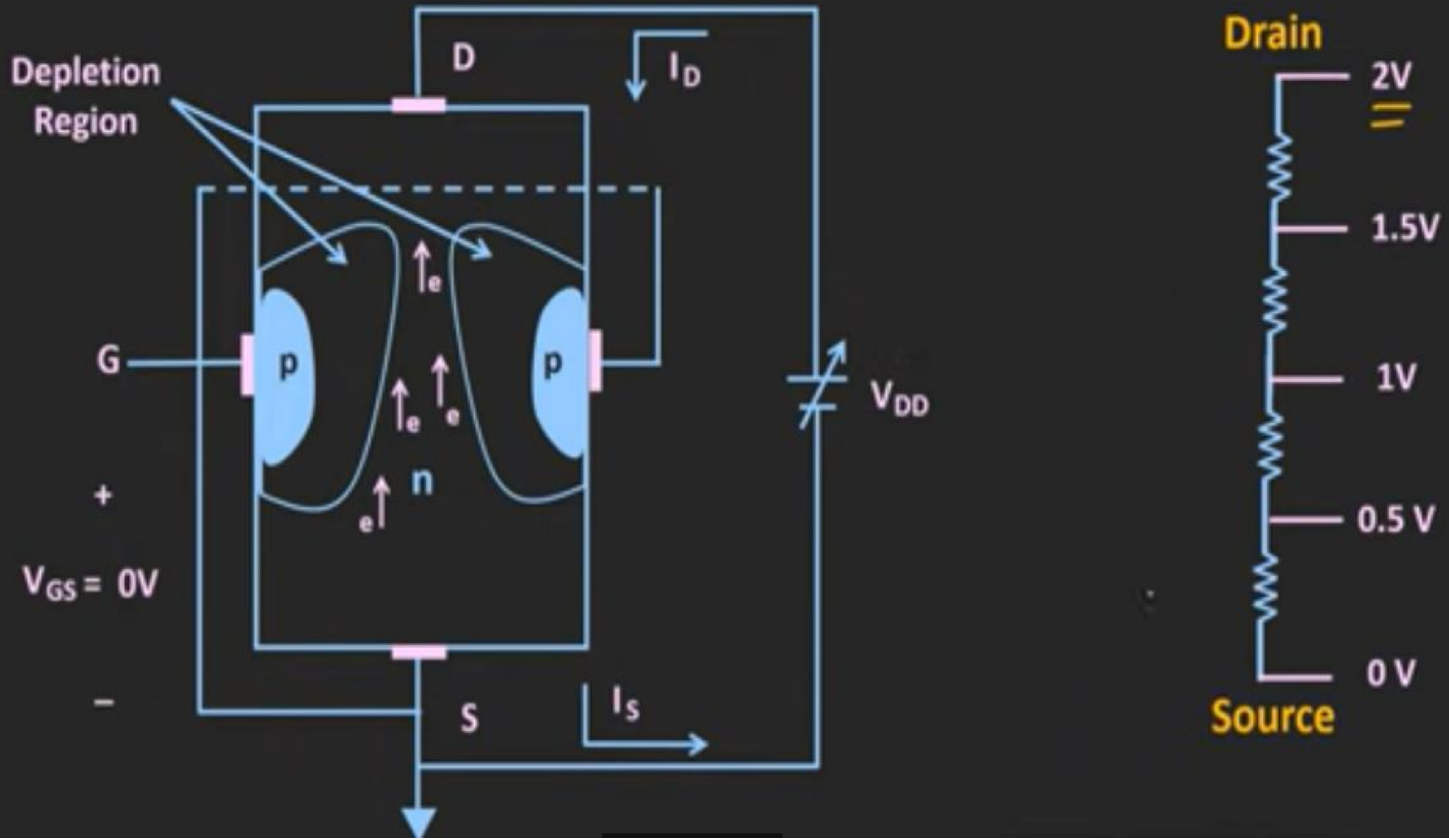
Reverse bias PN



n-channel JFET Output Characteristics



n-channel JFET

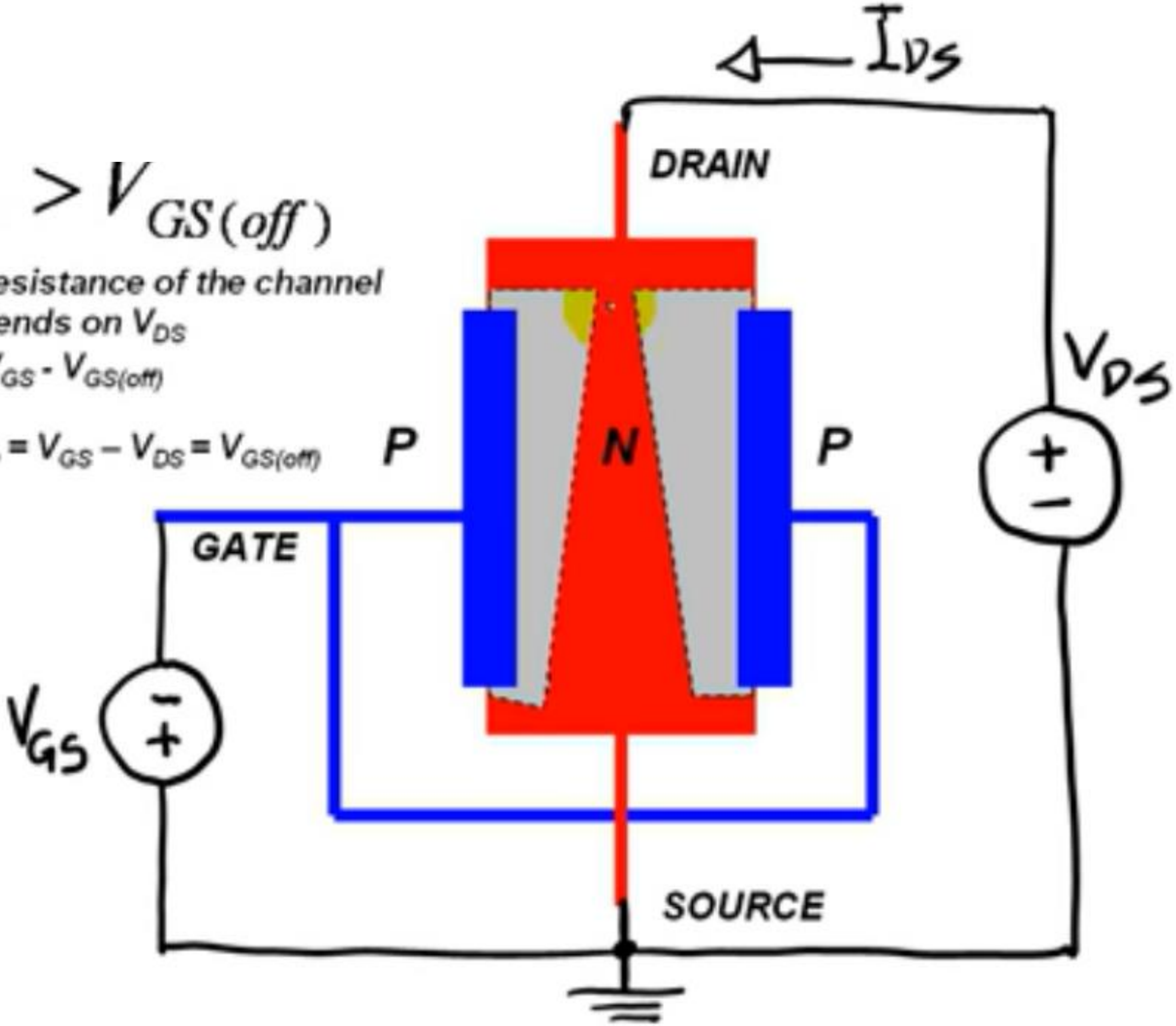


$$V_{GS} > V_{GS(off)}$$

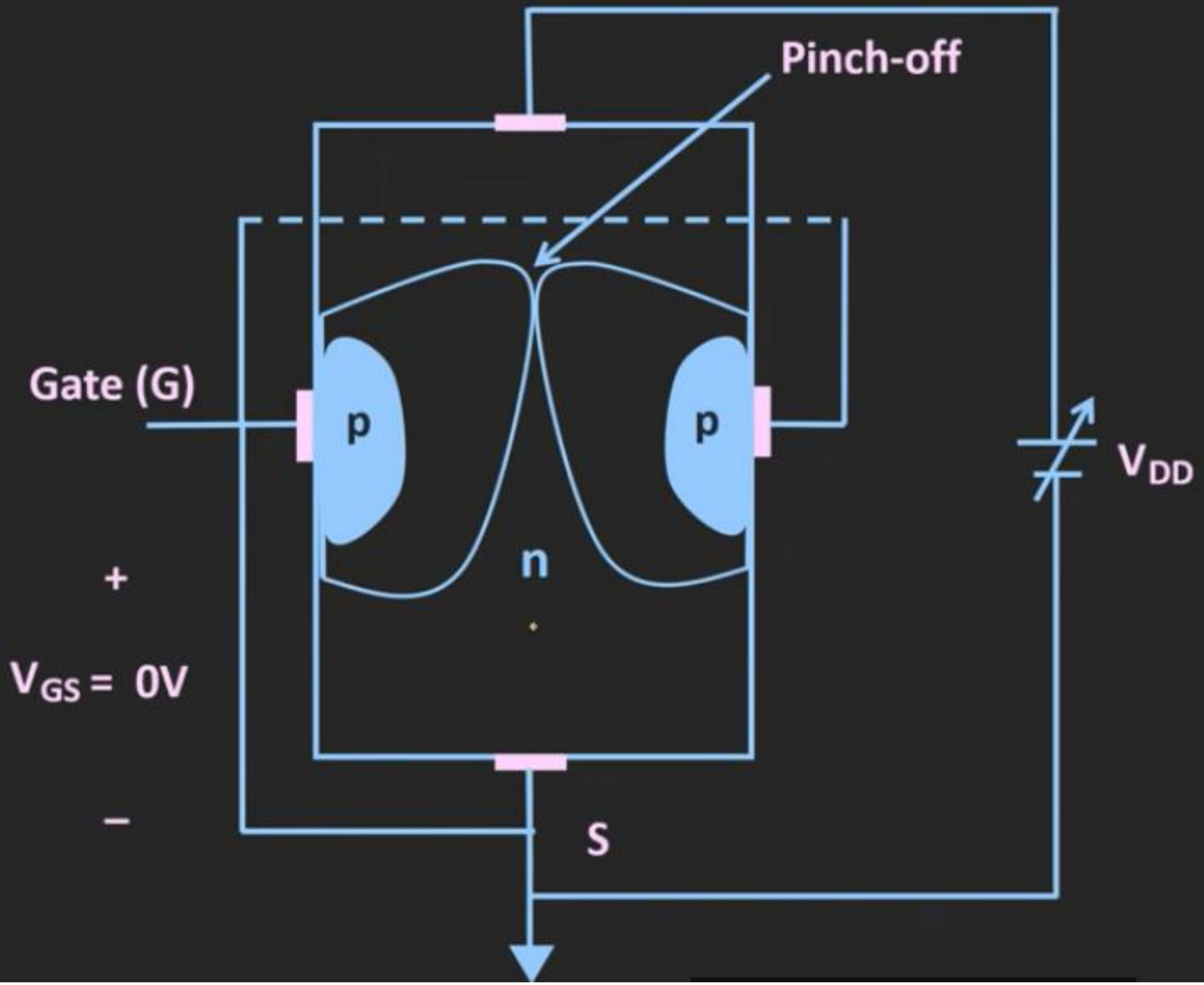
So, the resistance of the channel also depends on V_{DS}

If $V_{DS} = V_{GS} - V_{GS(off)}$

then $V_{GD} = V_{GS} - V_{DS} = V_{GS(off)}$



Pinch-off Condition in JFET

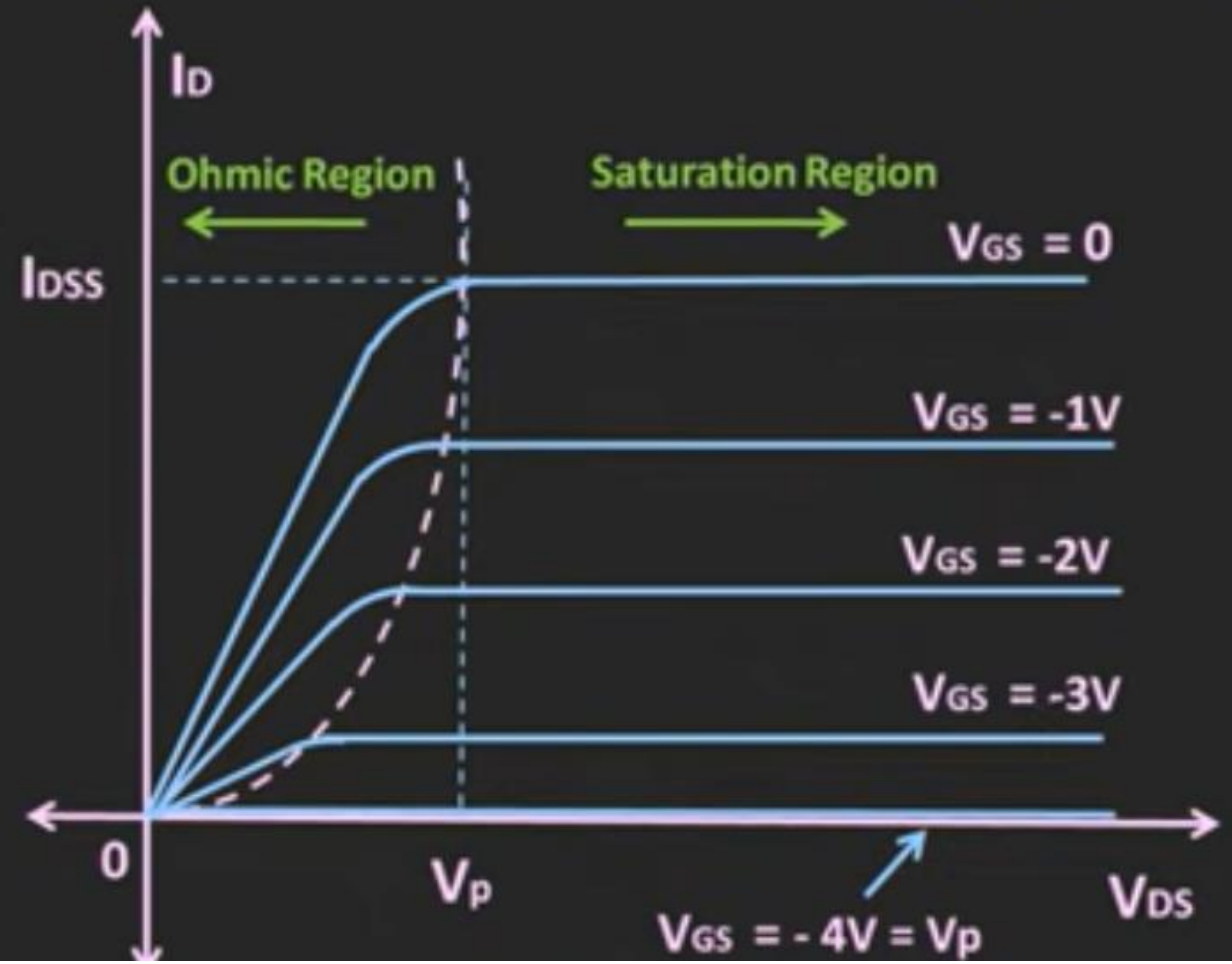


$V_{GS} = 0$ and $V_{DS} > 0$

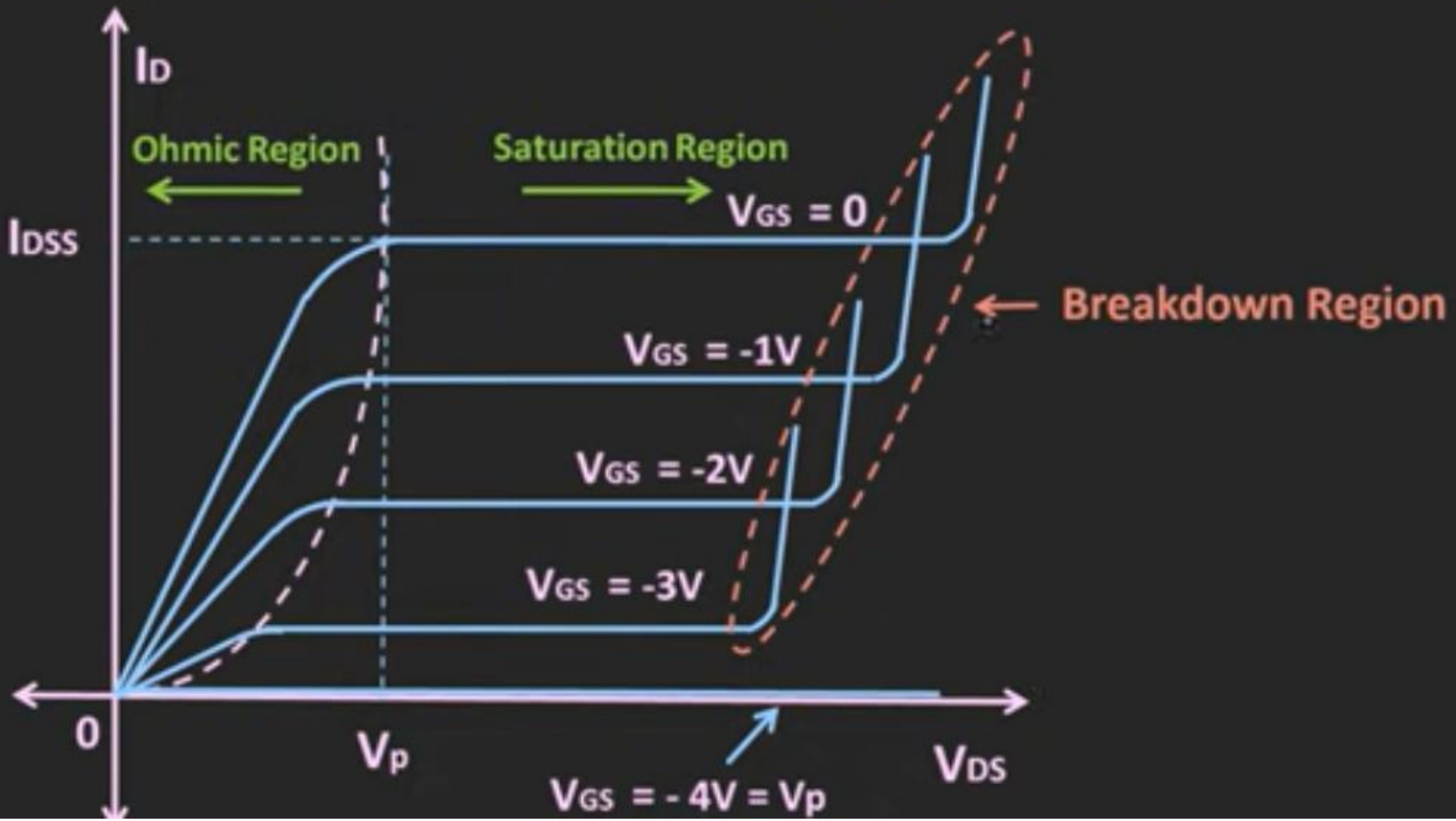
V_P

$V_{DS} \geq V_P$

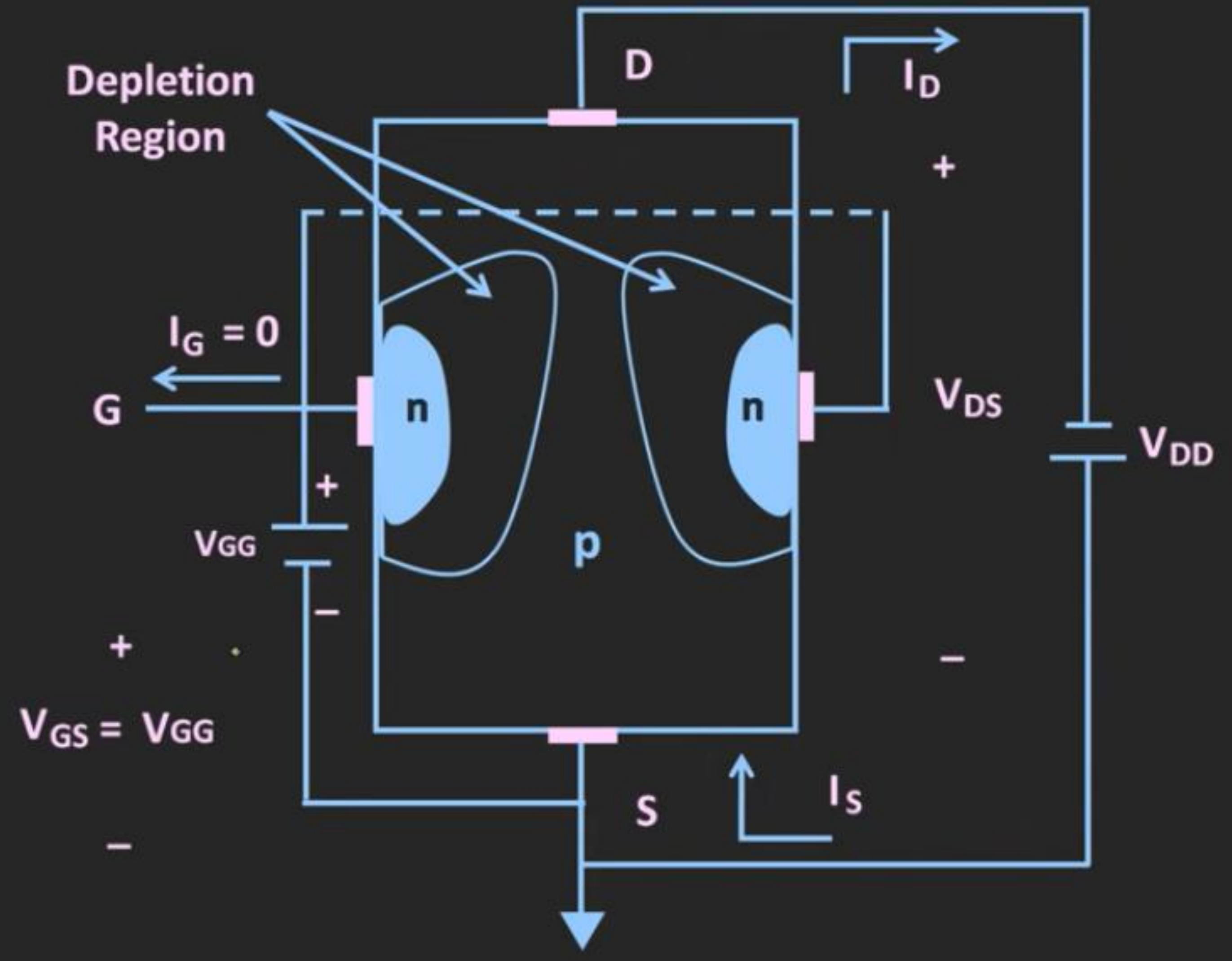
n-channel JFET Output Characteristics



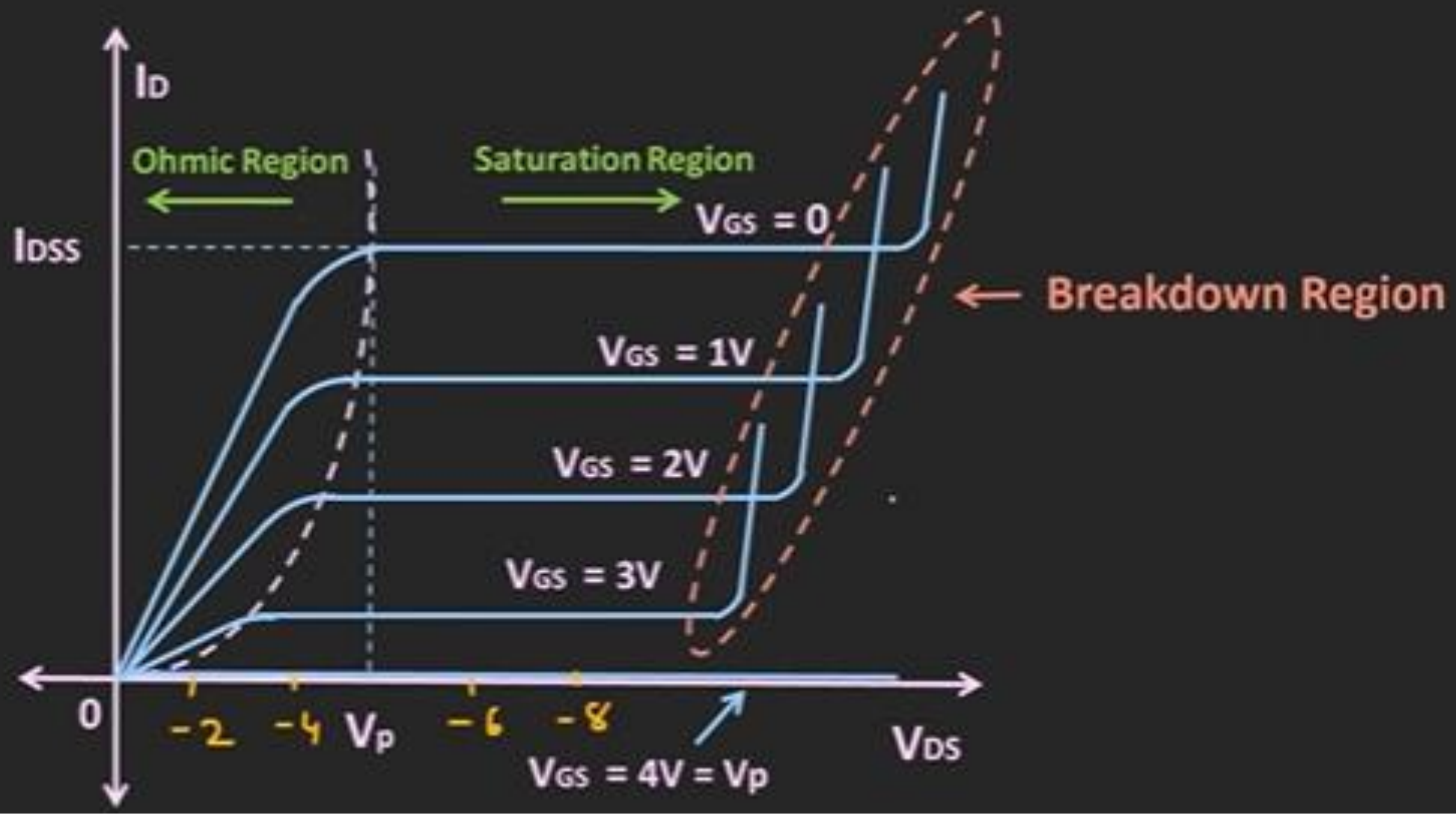
n-channel JFET Output Characteristics



p-channel JFET



p-channel JFET Output Characteristics

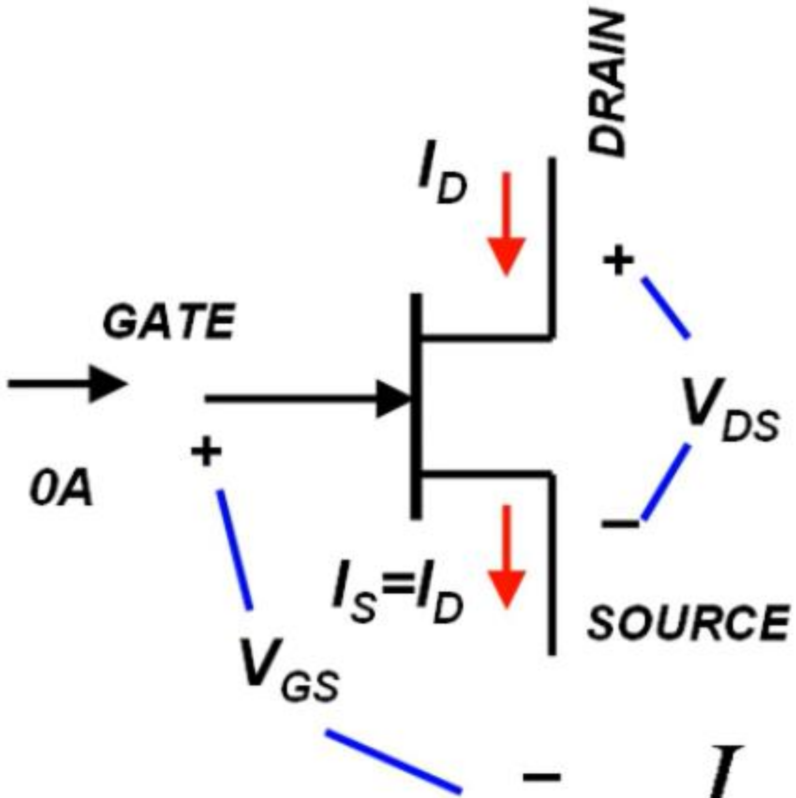


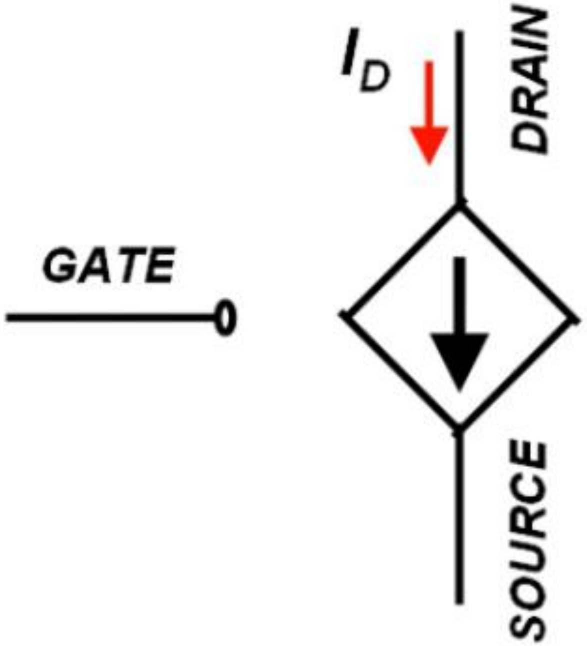
Graphical Symbol

n- channel JFET

p- channel JFET

Symbol and Model





$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

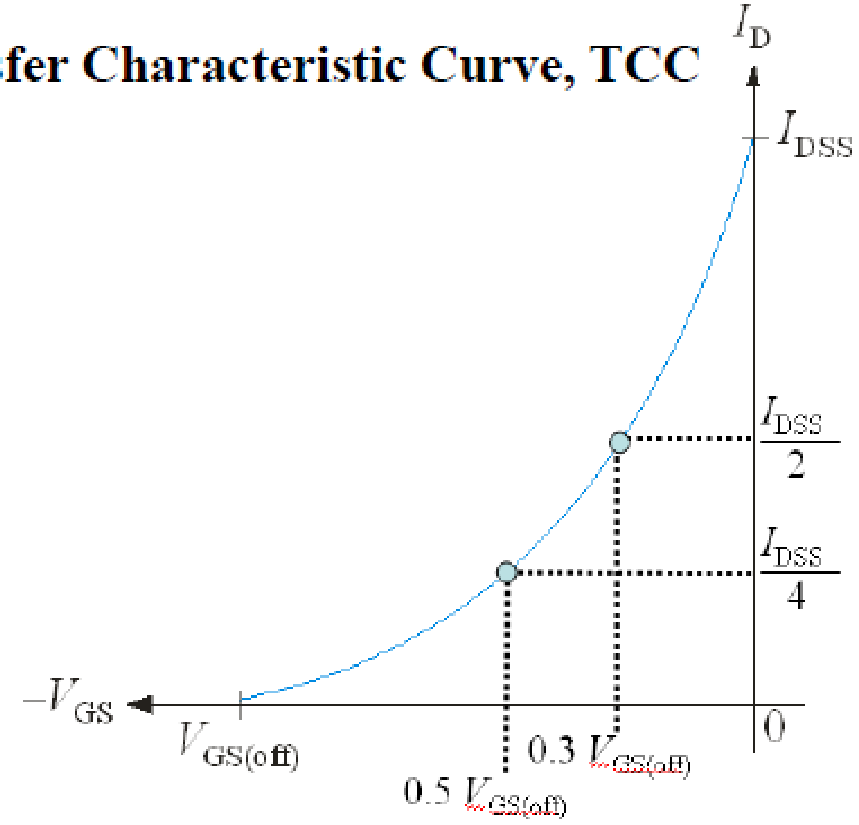
Amplification is not LINEAR but QUADRATIC!
Soooo …. The FET introduces distortion!

JFET Characteristics :Transfer Characteristics Curve,TCC

- TCC will show the value of ID at certain value of V_{GS} .
- A JFET transfer characteristic curve is expressed approximately as: **(Square Law)**

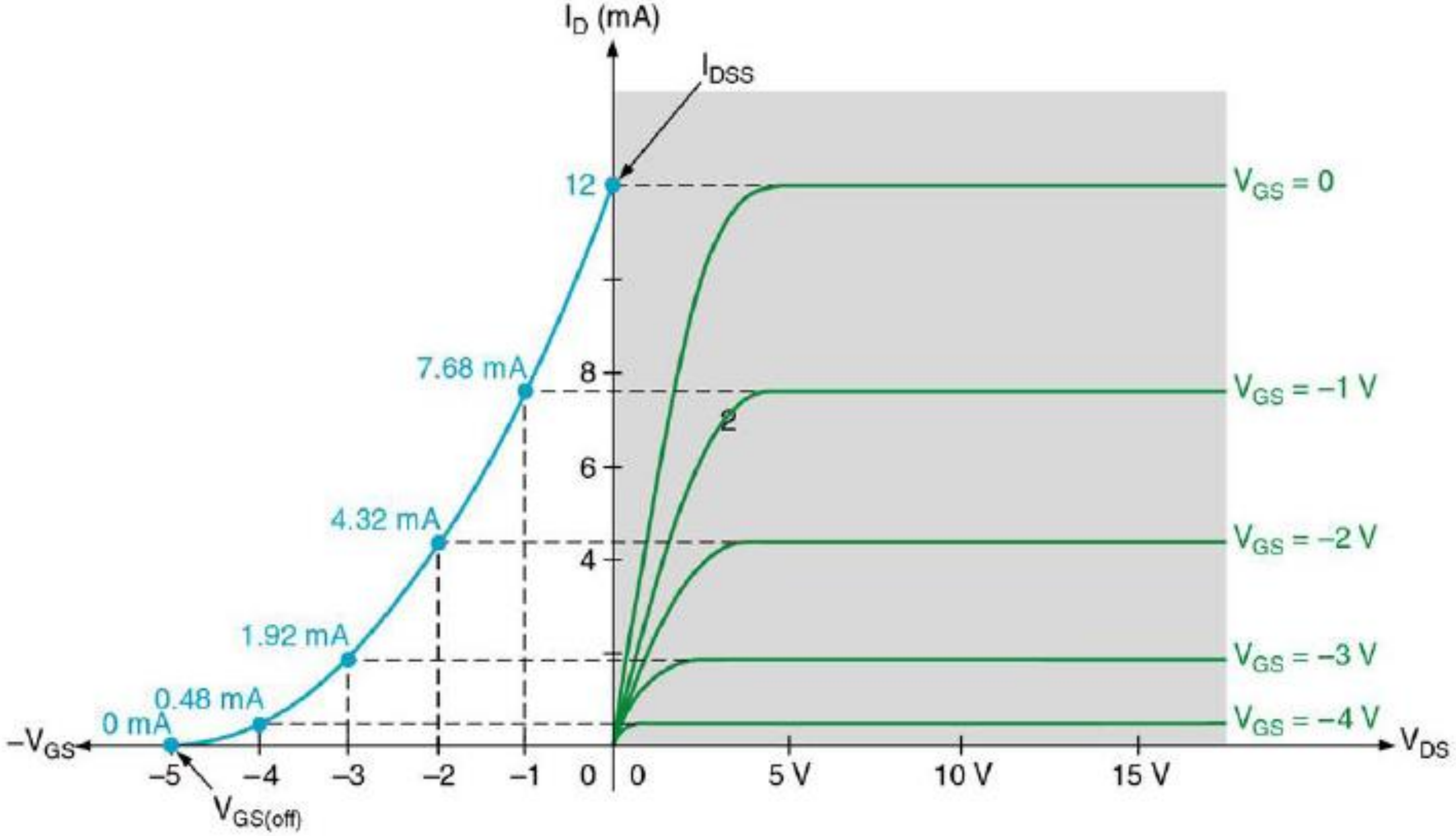
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Transfer Characteristic Curve, TCC



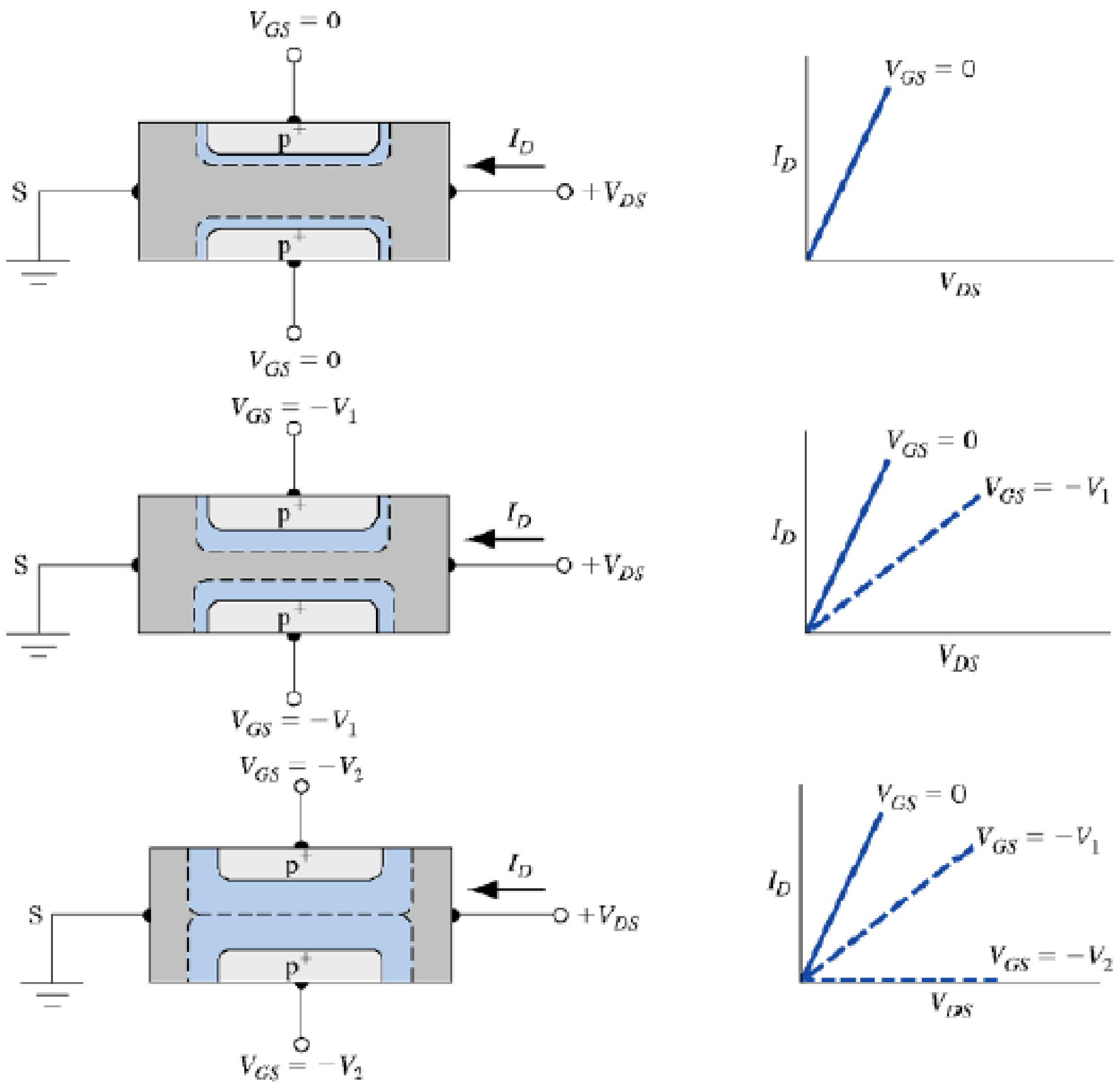
- I_D can be determined for any V_{GS} **if $V_{GS(off)}$ and I_{DSS} are known**.
- **$V_{GS(off)}$ and I_{DSS}** are usually available from the JFET **datasheet.**

- **Transfer characteristic curve (blue)** can be developed from **Drain characteristic curves (green)** by plotting values of I_D for the values of V_{GS} taken from drain curves at pinch-off, Vp.



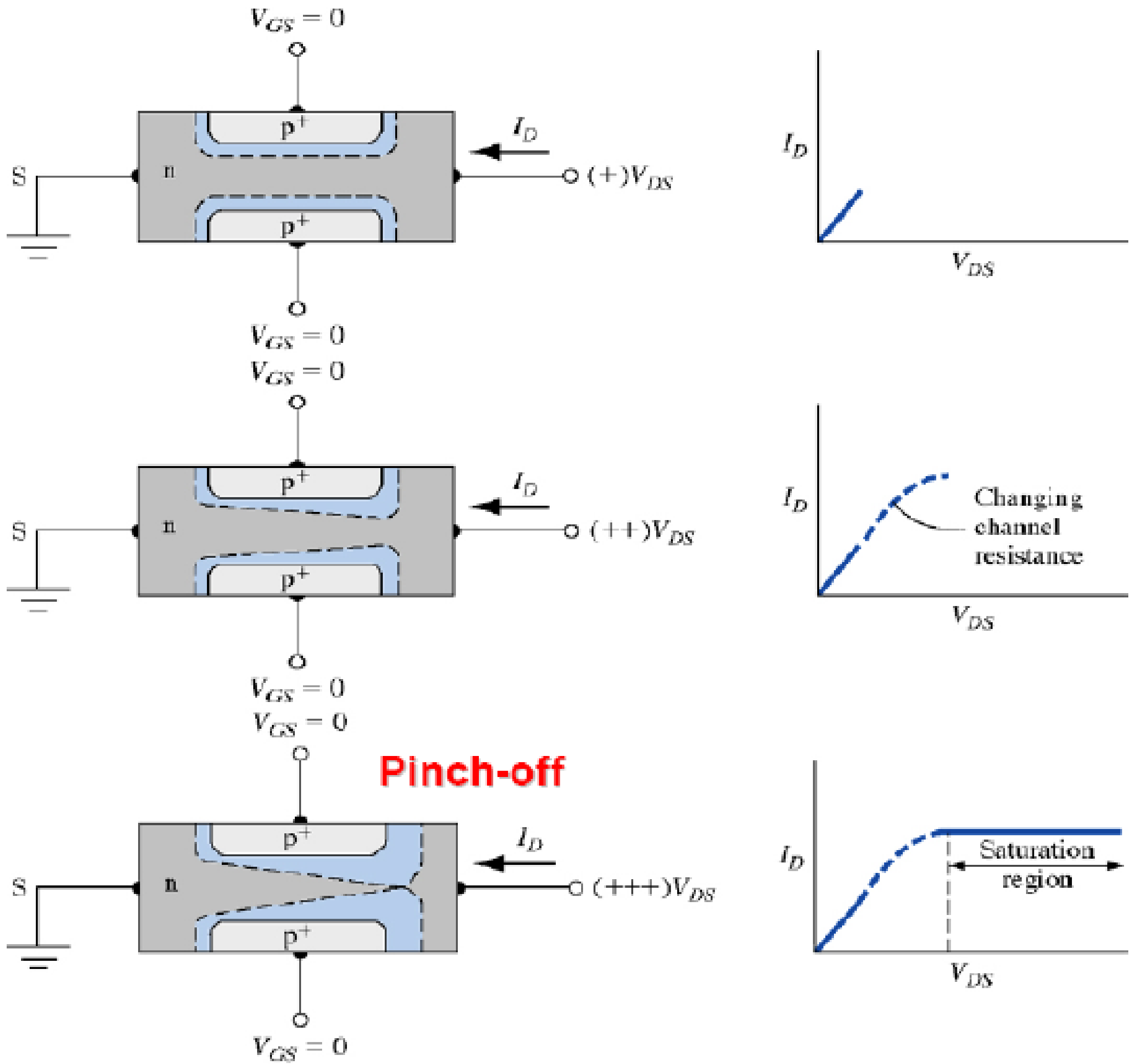
- When V_{GS} = - 2V, I_D = 4.32mA.
- When V_{GS} = 0V, $I_D = I_{DSS}$ = 12mA.

I-V CHARACTERISTICS



V_G controls the channel width → V_G control I_d

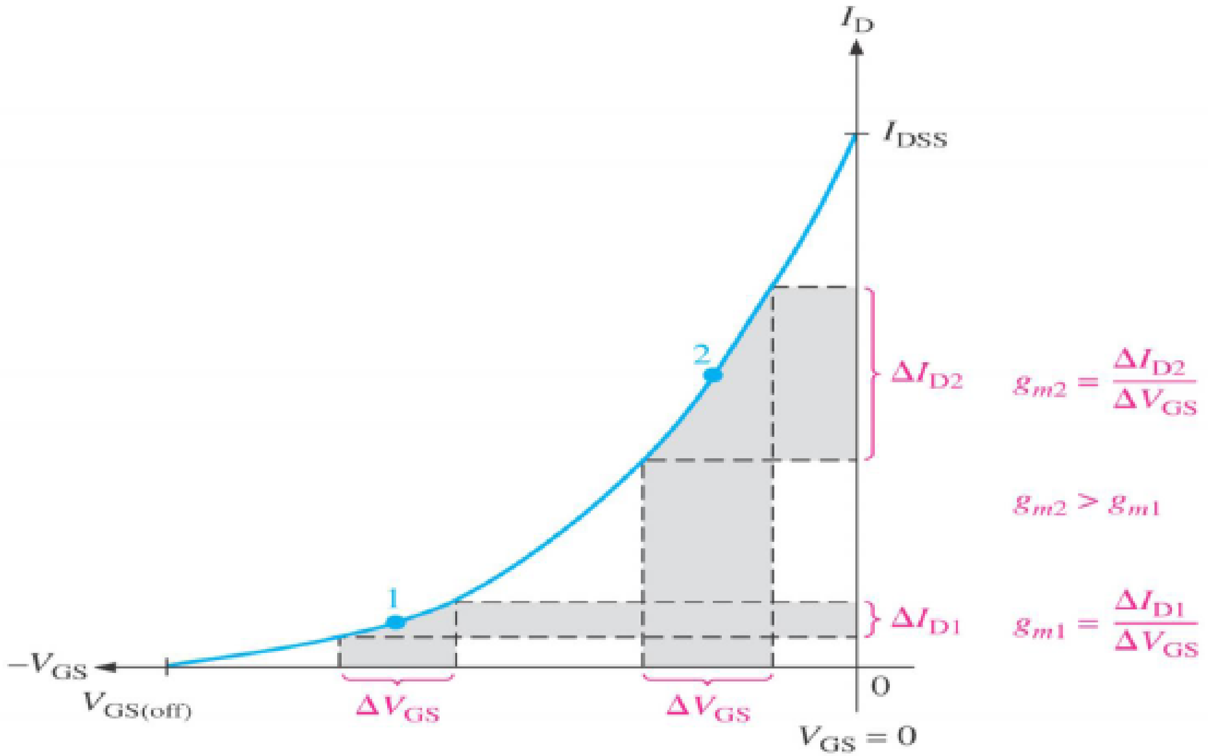
I-V CHARACTERISTICS



After pinch-off: $I_D \neq f(V_D)$; $I_D = f(V_G)$ - current source

JFET Parameters: Forward Transconductance

- **Forward Transfer Conductance, g_m** is the changes in drain current (ΔI_D) based on changes in gate-to-source voltage (ΔV_{GS}) with V_{DS} is constant.
- The value is larger at the top of the curve (near $V_{GS}=0$) but become smaller as you increase V_{GS} (near $V_{GS(off)}$).



$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}}$$

JFET Parameters : Input Resistance, R_{in}

- Since JFET operates with GS-junction reverse-biased for operation , which makes the **input resistance (R_{in})** becomes so **large at the gate**.
- This high input resistance is one advantage of using JFET over BJT.
- This input resistance R_{in} can be calculated at different V_{GS} using :

$$\boxed{R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|}$$

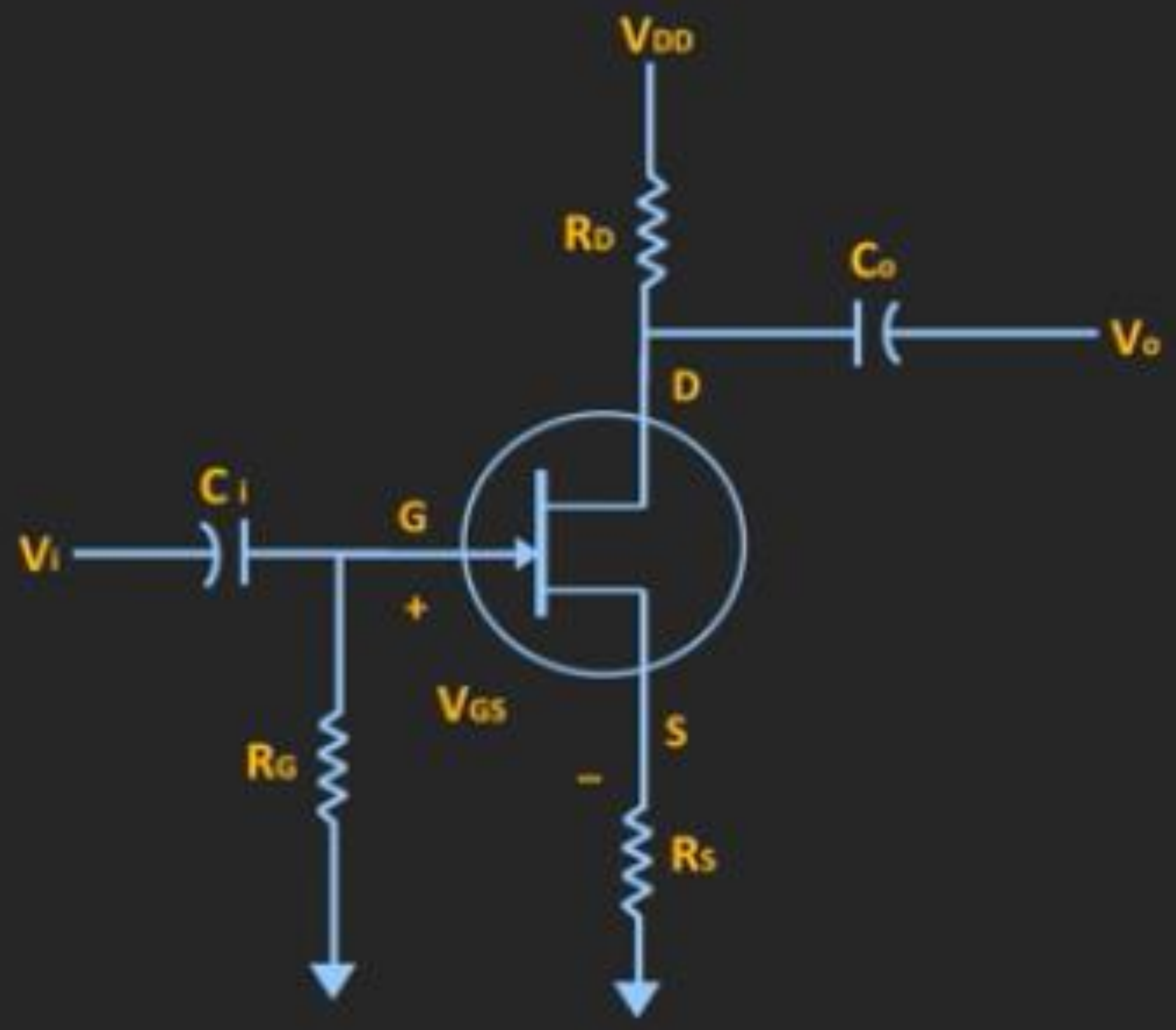
Where:
I_{GSS} = Gate Reverse Current (if not given refer data sheet)

- The value of input resistance is absolute value (no sign).

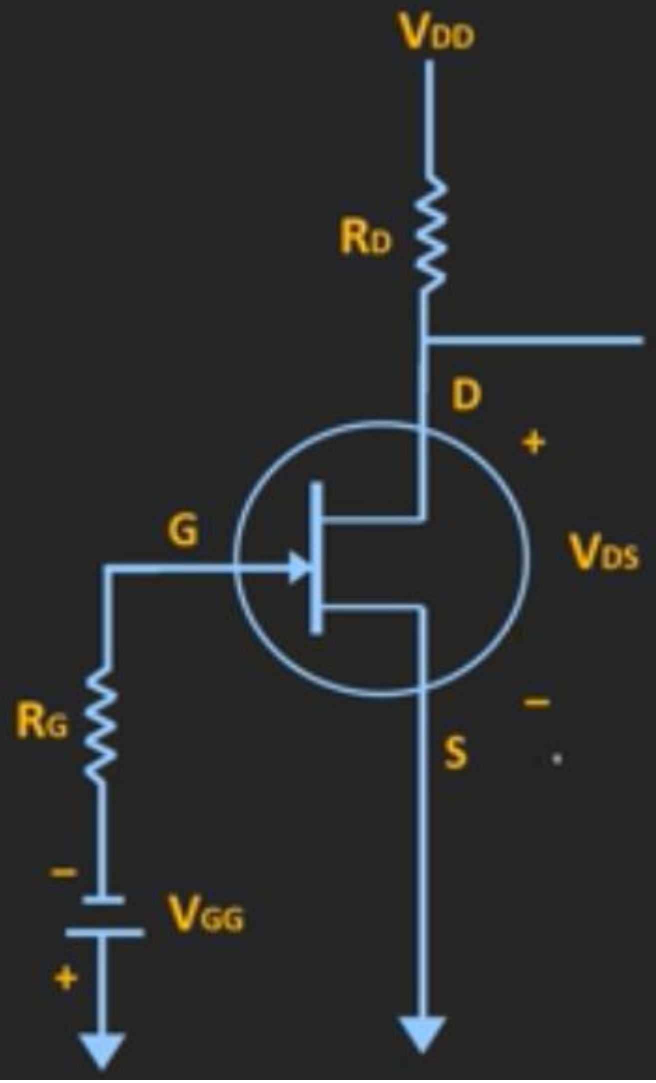
Biasing Circuits used for JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

JFET Self bias Configuration



JFET Fixed bias Configuration



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

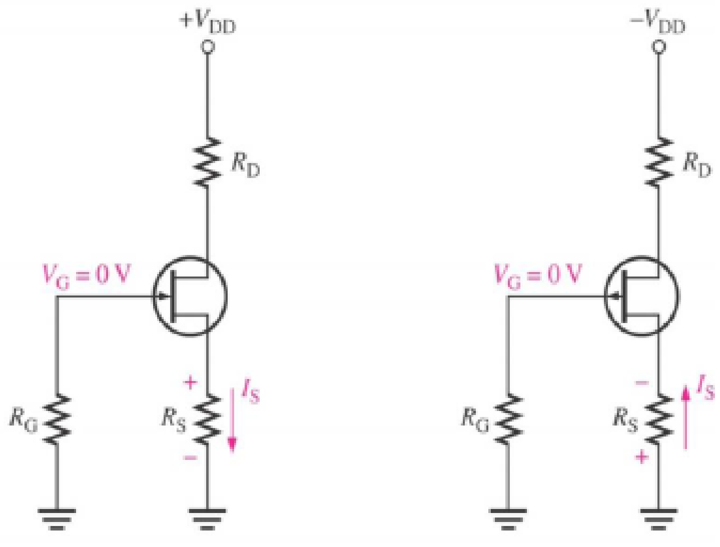
JFET Biasing- 1) Self bias

- **Self-bias** is the most common type of biasing method for JFETs.
- JFET must be operated such that the gate-source junction is always reverse biased.
- To keep the GS-junction reverse biased:

(a). V_{GS} will be -ve for *n*-channel JFET (b). V_{GS} will be +ve for *p*-channel JFET.

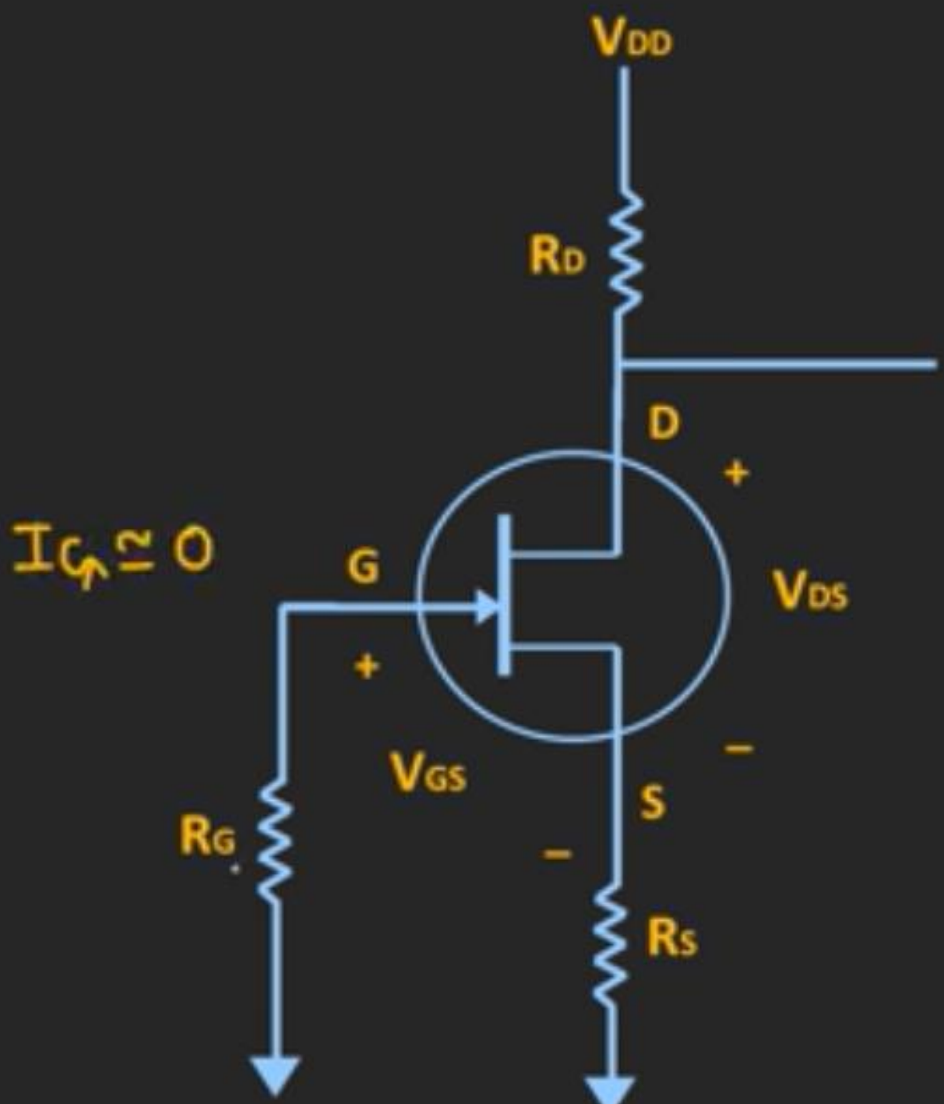
- It can be achieved using self-bias arrangement as shown in figure below.
- The gate resistor,RG : not affect the bias because it has essentially no volt drop across it.
- Therefore, the gate remains 0V.
- RG only to force the gate to be 0V and isolate an ac signal from ground in amplifier applications.
- Self-biased JFETs:

$$I_D = I_S \text{ for all JFET circuits}$$



(a) *n* channel (b) *p* channel

JFET Self bias Configuration



THE FIELD-EFFECT TRANSISTOR

Comparison between the BJT and the FET

BJT	*FET*
1. Two types of carriers (electrons and holes) are required.	1. Only one type of carrier (electron or hole) is required.
2. Carriers move through the base by diffusion process.	2. Carriers move through the channel by drift process.
3. The BJT has a comparatively lower switching speed due to the diffusion process.	3. The FET has a higher switching speed due to the drift process; the drift of the carrier is faster than diffusion.
4. The BJT is not a thermally stable device.	4. The FET has a negative temperature coefficient at high-current operations, i.e., the current decreases as temperature increases Due to this particular feature, a uniform temperature distribution and protection against breakdown can be achieved.
5. In case of IC fabrication, the BJT requires more space than the FET.	5. In case of IC fabrication the FET requires lesser space than the BJT.
6. At audio frequencies the BJT offers less power gain.	6. At audio frequencies the FET offers greater power gain.
7. The BJT is a current-controlled device.	7. The FET is a voltage-controlled device.
8. The BJT offers low input impedance.	8. The FET offers high input impedance, therefore, it can be used as a buffer.
9. BJT is much noisier than FET.	9. FET is less noisy.
10. The BJT has offset voltage.	10. The FET has no offset voltage.
11. The BJT can also be used as a switch; it is taken to be in the OFF state when operating in the cut off region, and in the ON state when it is operating in the saturation region.	11. The FET is particularly useful for its operation as a controlled switch, operating in both the conducting and the non-conducting zones.