- Must be properly biased s.t. operating voltage and current are within the linear portion of the active region of the JFET.

- **Introduction to JFET Biasing :→**

In BJT

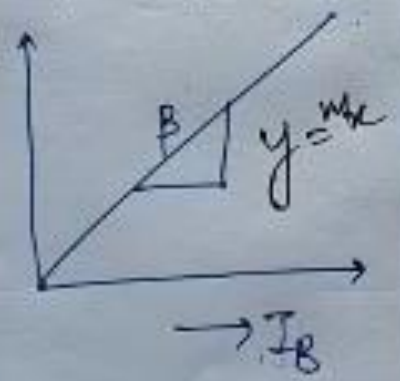
$I_c = \beta I_B$

I_c → O/P, β → Const: Amplification factor, I_B → I/P

$I_c + I_B = I_E$

$I_B \ll I_c$

$\Rightarrow I_c \cong I_E$



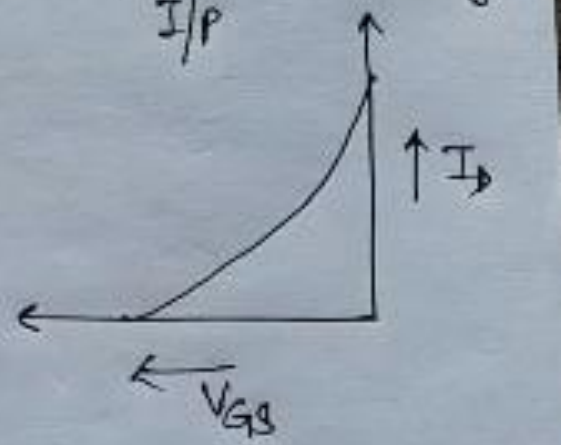
∴ In case of BJT, the variation of I_c with I_B is LINEAR.

But in case of FET

$I_D = f(V_{GS})$

I_D → O/P, V_{GS} → I/P

$y = x^2$ or $x = y^2$



To find Q-point ⟶ There are 2 approaches

1) Mathematical
2) Graphical

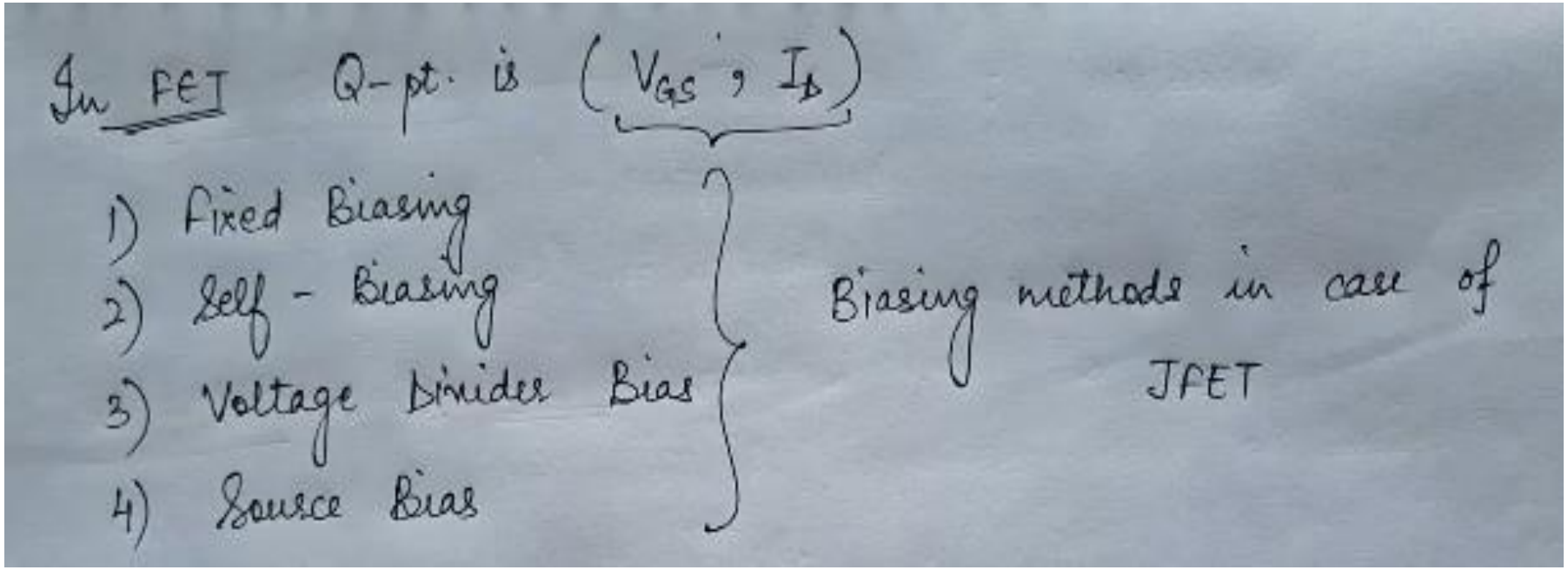
In BJT I_C linear variation with I_B

∴ Mathematical approach will be easy to find Q-pt.

In FET the variation of I_D is non-linear with V_{GS}

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{(V_{GS})_{off}}\right]^2 \longrightarrow \text{Shockley's eqn.}$$

⟶ Graphical approach is easy to use.



BIASING CIRCUITS USED FOR JFET

- Fixed bias circuit
- Self bias circuit
- Potential Divider bias circuit

INTRODUCTION

The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \cong 0\ \text{A} \quad \text{and} \quad I_D = I_S$$

For JFETs and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = k(V_{GS} - V_T)^2$$

It is particularly important to realize that all of the equations above are for the device only!. They do not change with each network configuration so long as the device is in active region.

(A) FIXED-BIAS CONFIGURATION

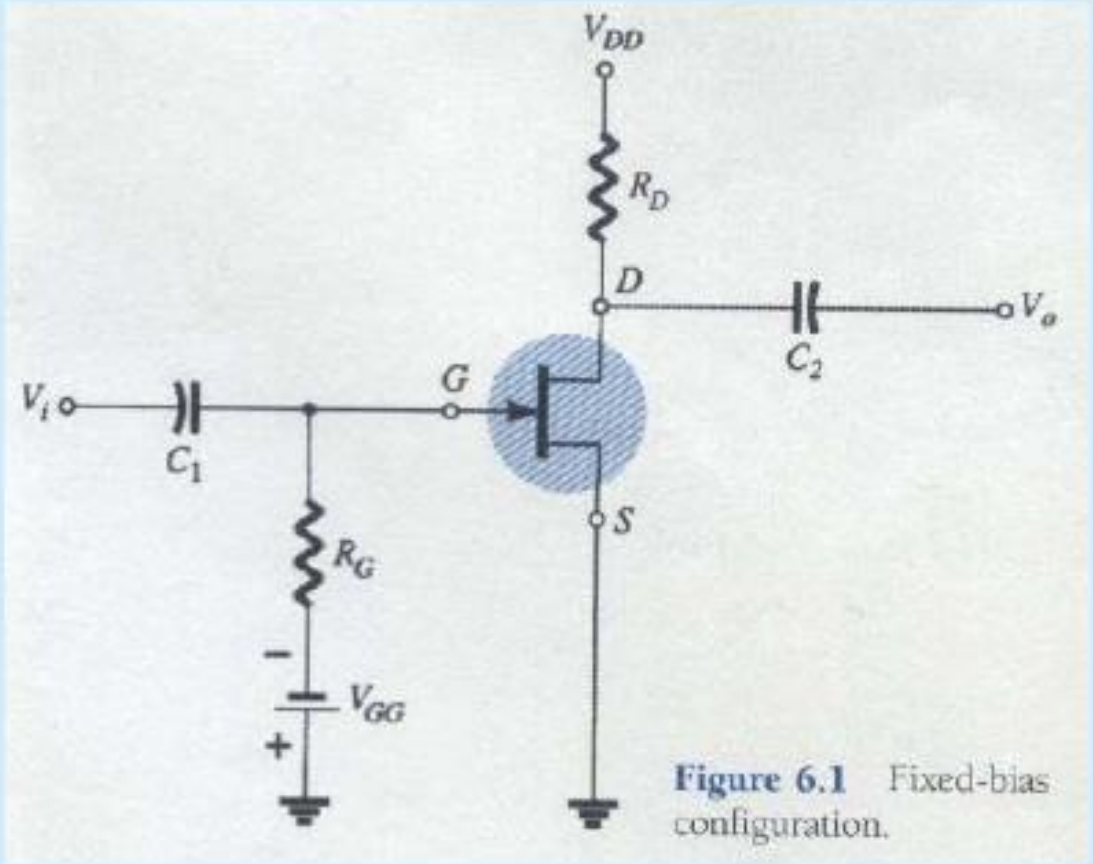
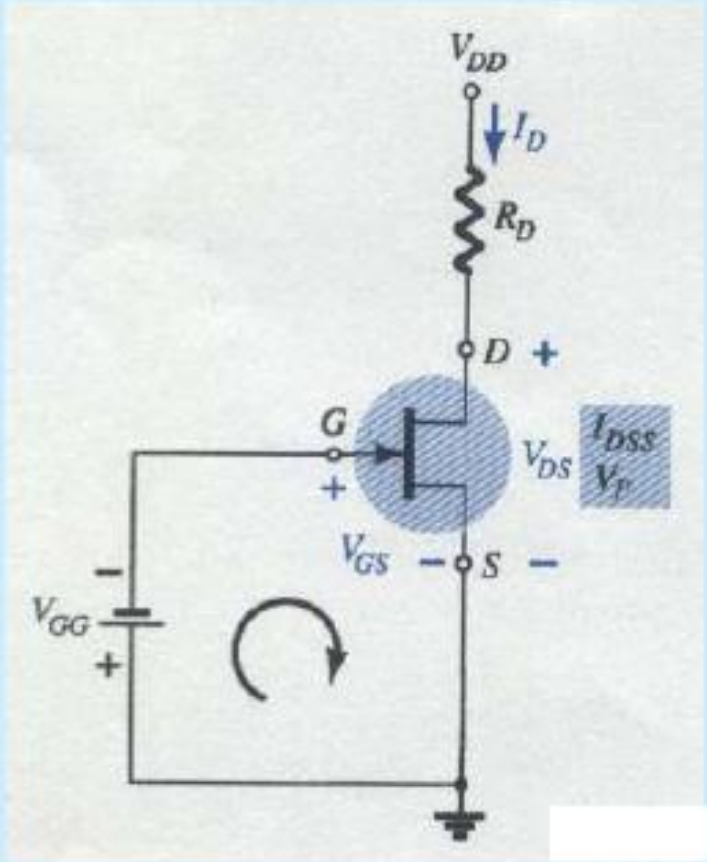


Figure 6.1 Fixed-bias configuration.



V_i&V_o:input & output ac levels
C_1&C_2: the coupling capacitors (open for dc analysis & low impedance (essentially short circuit) for ac analysis.

For dc analysis;

$$I_G \cong 0 \text{ A}$$

$$V_{R_G} = I_G R_G = (0 \text{ A}) R_G = 0 \text{ V}$$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network redrawn for the dc analysis.

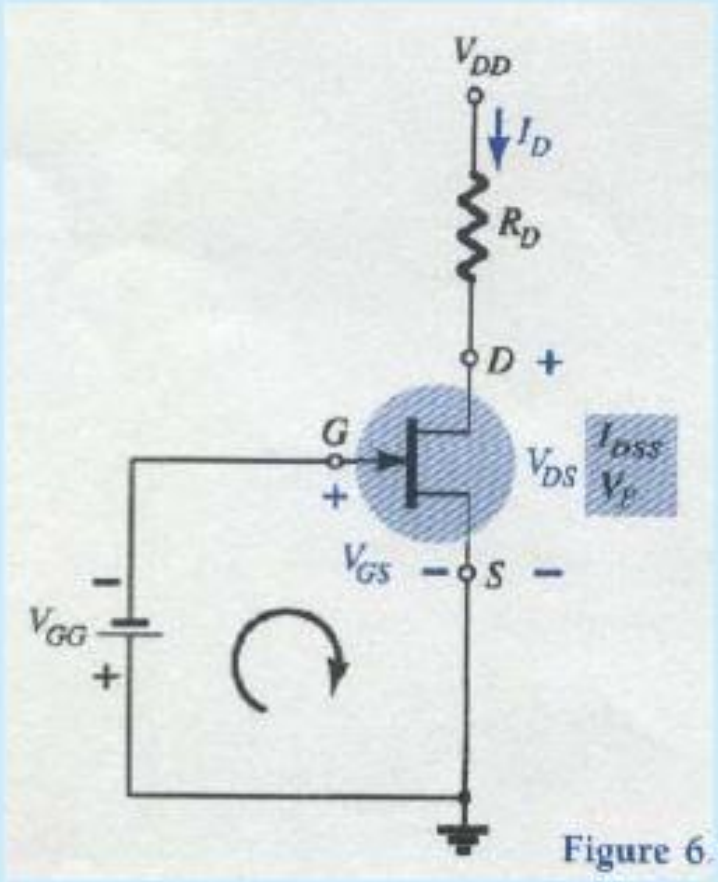


Figure 6

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}.
KVL in the clockwise direction will result in

$$-V_{GG} - V_{GS} = 0$$

$$V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration".
The resulting level of drain current I_D is now controlled by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Since V_{GS} is fixed quantity, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated. Here, a mathematical solution to a FET configuration is quite direct.

Case I: $V_{GS} = 0V$

$I_D = I_{DSS}$

$P1 \equiv (0, I_{DSS})$

0V, 8mA

I_D Vs V_{GS}

Case II: $I_D = 0A$

$V_{GS} = V_P$

$P2 \equiv (V_P, 0)$

-6V, 0A

8mA

I_{DSS} (Max.)

$V_P = -6V$

Case III: $V_{GS} = V_P/2$

$I_D = I_{DSS}\left(1 - \frac{V_P/2}{V_P}\right)^2$

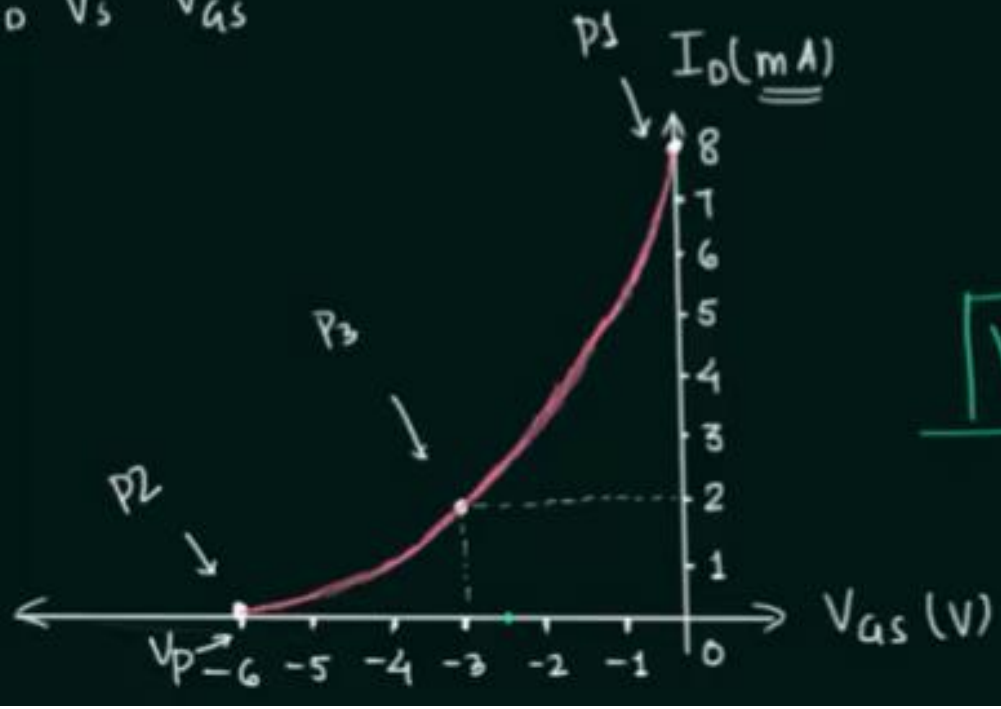
$= I_{DSS}(1 - 1/2)^2$

$I_D = I_{DSS}/4$

$P3 \equiv \left(\frac{V_P}{2}, \frac{I_{DSS}}{4}\right)$

$\frac{-6}{2}V$ $\quad \frac{8mA}{4}$

$(-3V, 2mA)$



$V_{GS} = -V_{GG}$

$P1 \equiv (0, I_{DSS})$ ✓ 0V, 8mA

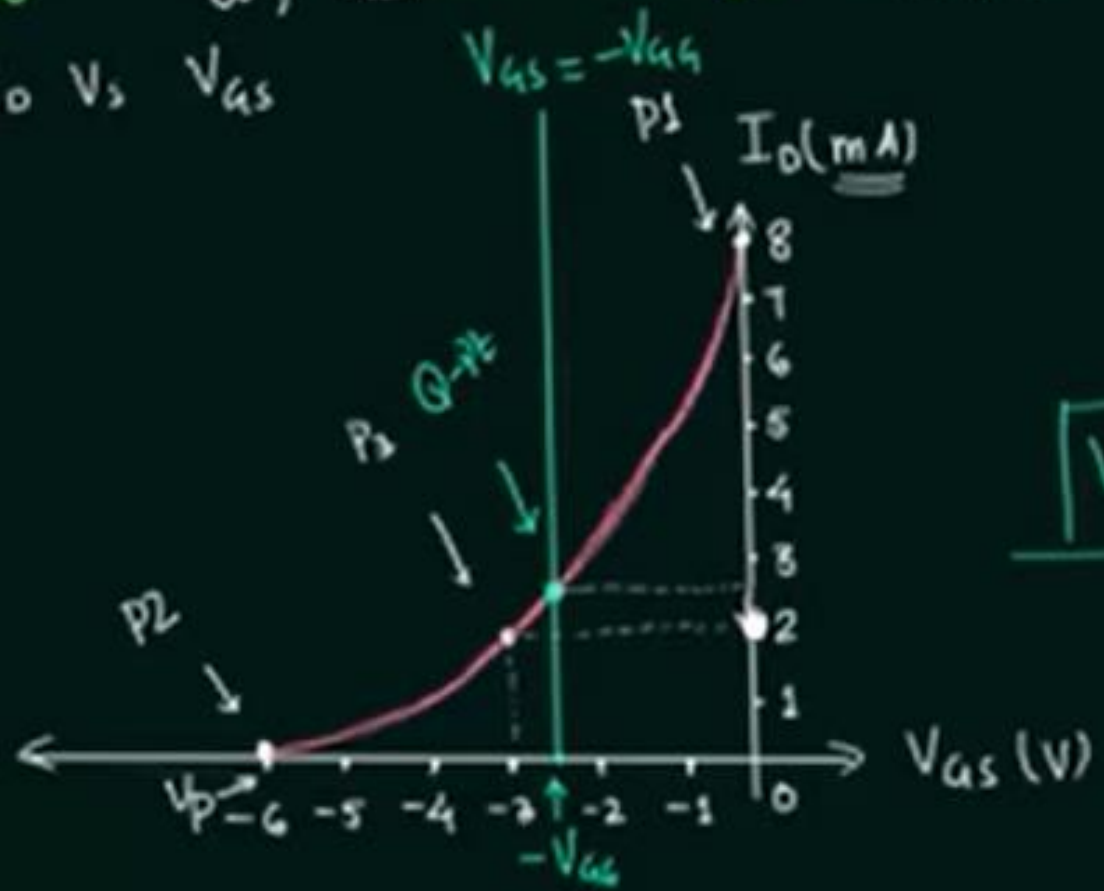
$P2 \equiv (V_P, 0)$ ✓ −6V, 0A

8mA

$I_{DSS}(Max.)$

$V_P = -6V$

I_D Vs V_{GS}



$V_{GS} = -V_{GG}$

$= I_{DSS}(1 - 1/2)^2$

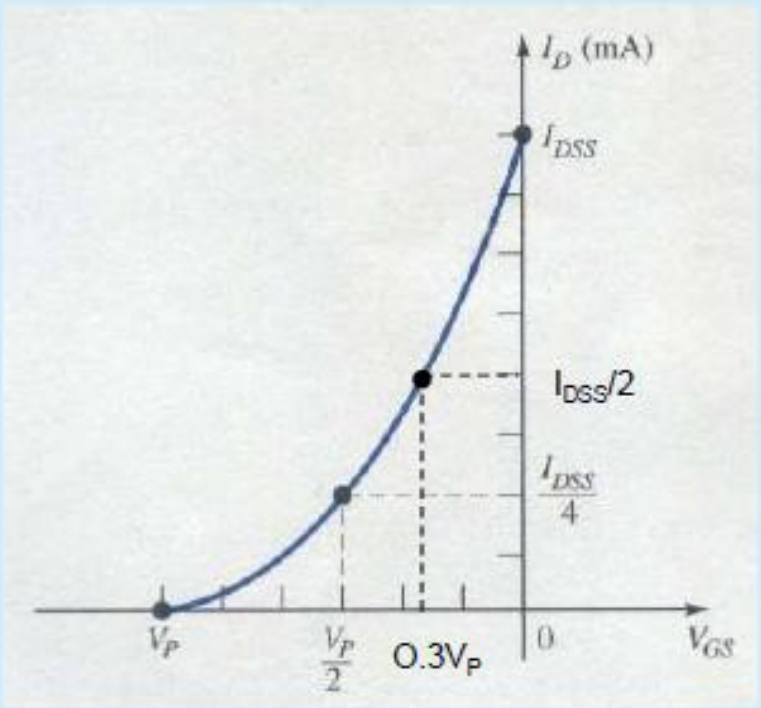
$I_D = I_{DSS}/4$

$P3 \equiv \left(\frac{V_P}{2}, \frac{I_{DSS}}{4}\right)$

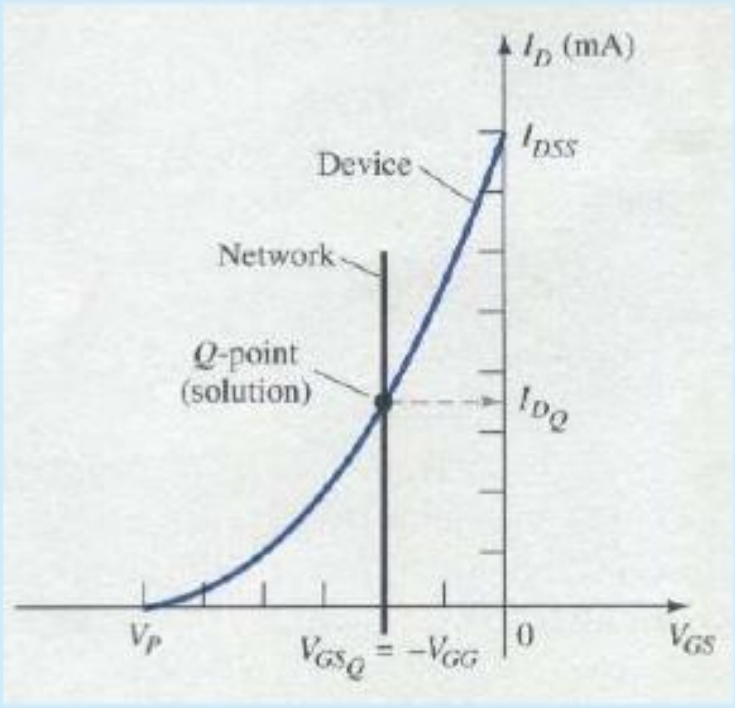
$\frac{-6}{2}V$ $\quad \frac{8mA}{4}$

$(-3V, 2mA)$

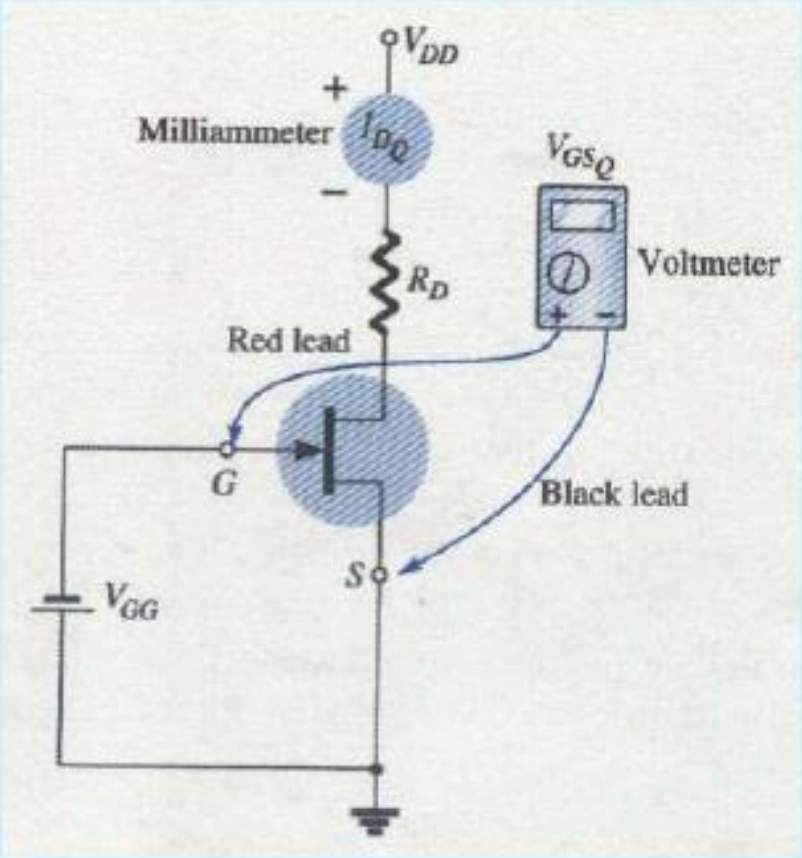
On the other hand, graphical analysis would require a plot of Shockley's equation. Recall that choosing $V_{GS}=V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation.



In this analysis, four points defined by I_{DSS}, V_P and intersection will be sufficient for plotting the curve.



The fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$.
The quiescent level of I_D is determined by drawing a horizontal line from the Q-point to the vertical I_D axis.



Once the network is constructed and operating, the dc levels of I_D and V_{GS} that will be measured by the meters are the quiescent values.

The drain-to-source voltage, V_{DS} of the output section can be determined by applying KVL;

$$+V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

Recall that single-subscript voltages refer to the voltage at a point with respect to ground.

$$V_S = 0\,\text{V}$$

Using double-subscript notation:

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S = V_{DS} + 0\,\text{V}$$

$$V_D = V_{DS}$$

$$V_{GS} = V_G - V_S$$

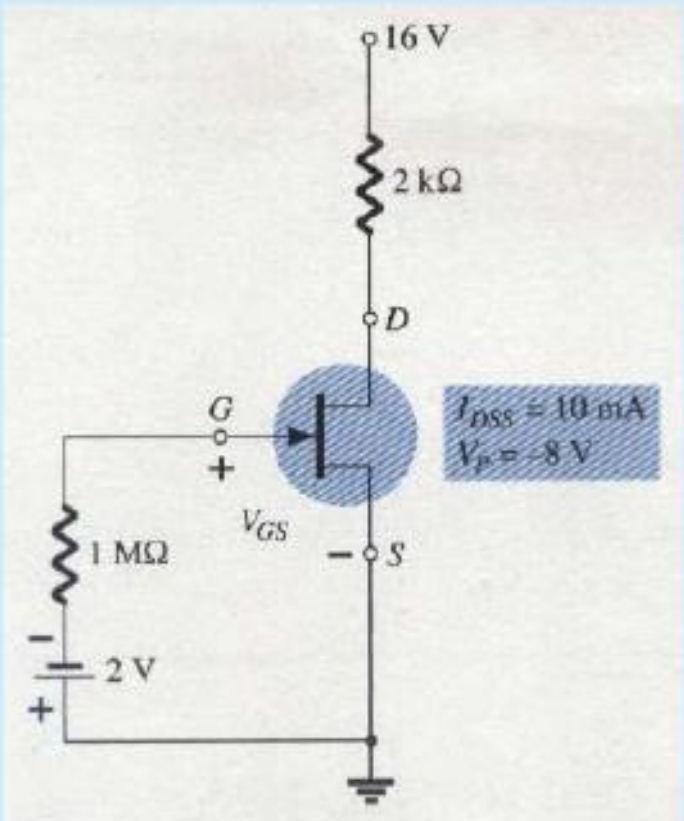
$$V_G = V_{GS} + V_S = V_{GS} + 0\,\text{V}$$

$$V_G = V_{GS}$$

Example (1): Determine the following.

(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_D.
(e) V_G.
(f) V_S.

Solution:
Mathematical Approach



(a) $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

(b) $I_{D_Q} = I_{DSS}\left(1 - \dfrac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \dfrac{-2\text{ V}}{-8\text{ V}}\right)^2$

$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$

$= \mathbf{5.625\ mA}$

(c) $V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$

$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$

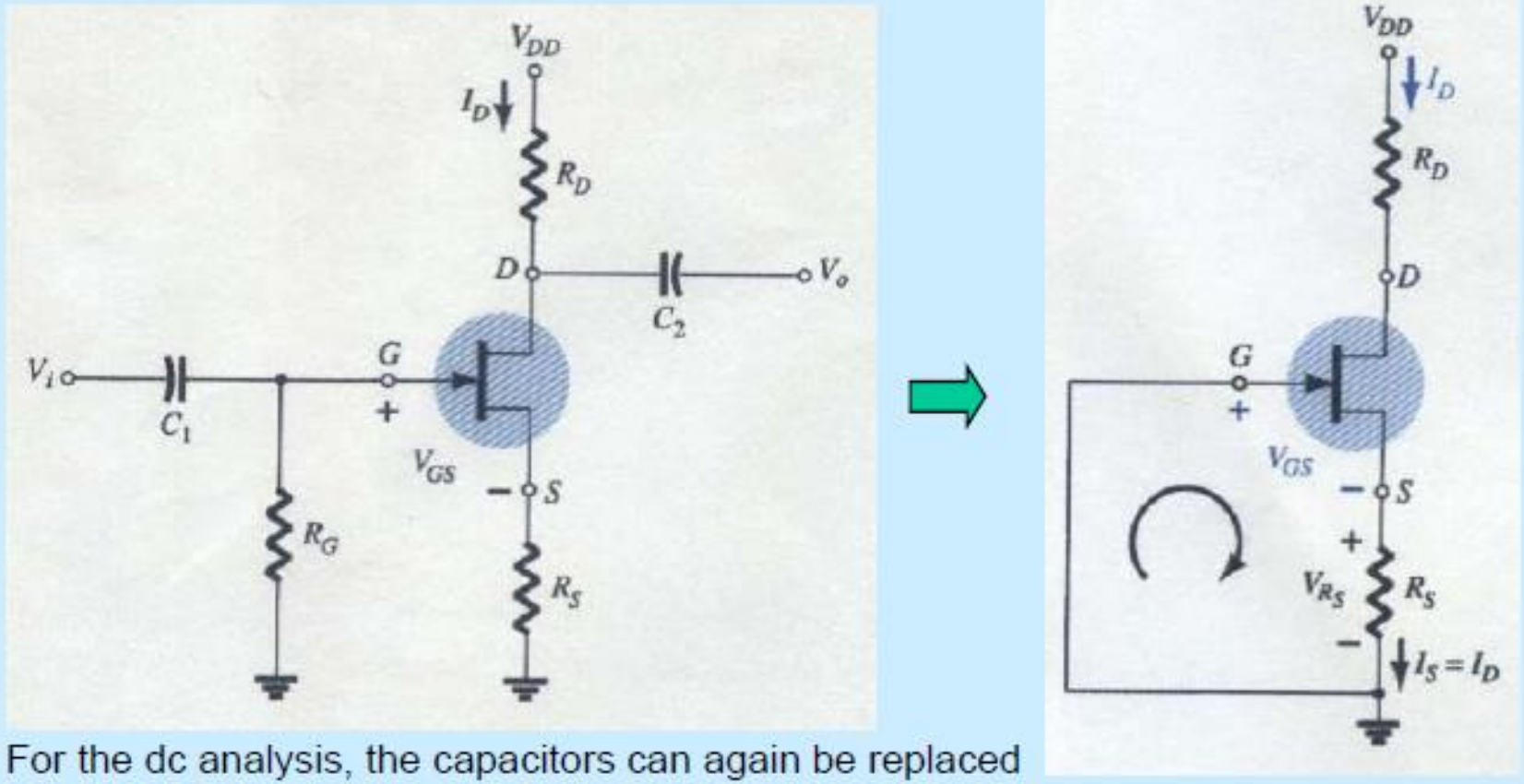
(d) $V_D = V_{DS} = \mathbf{4.75\ V}$

(e) $V_G = V_{GS} = \mathbf{-2\ V}$

(f) $V_S = \mathbf{0\ V}$

(B) SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies as required for fixed-bias configuration. The controlling gate-to-source voltage, V_{GS} is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration.



For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since I_G = 0A.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated loop, we find that

$$-V_{GS} - V_{R_S} = 0$$

$$V_{GS} = -V_{R_S}$$

$$\boxed{V_{GS} = -I_D R_S}$$

Note that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

The mathematical solution could be obtained simply by substituting the above equation into Shockley's equation as shown below;

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2$$

$$I_D = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$$

Self-Bias Configuration of JFET (Graphical Approach)

$I_{DSS} = 8\,mA$

$V_P = -6\,V$

$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$

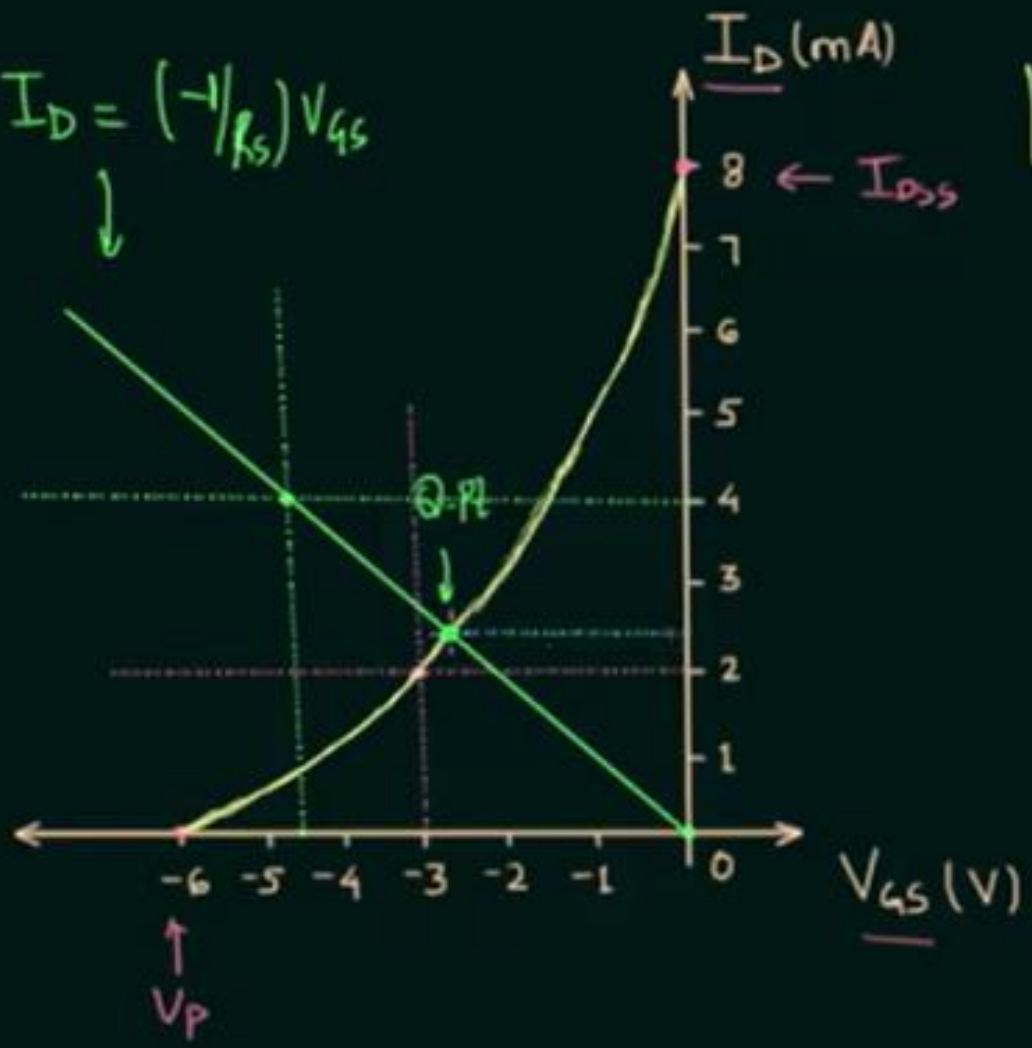
$I_D = 0A \quad V_{GS} = 0V$

$V_{GS} = V_P \quad I_D = I_{DSS}$

$V_{GS} = V_P/2 = -3V$

$I_D = \frac{I_{DSS}}{4} = \frac{8mA}{4} = 2mA$

$I_D = (-1/R_S)V_{GS}$



$y = mx + c$

$V_{GS} = -I_D R_S$

$x \quad y$

$I_D = \left(\frac{-1}{R_S}\right)V_{GS}$

$y = mx$

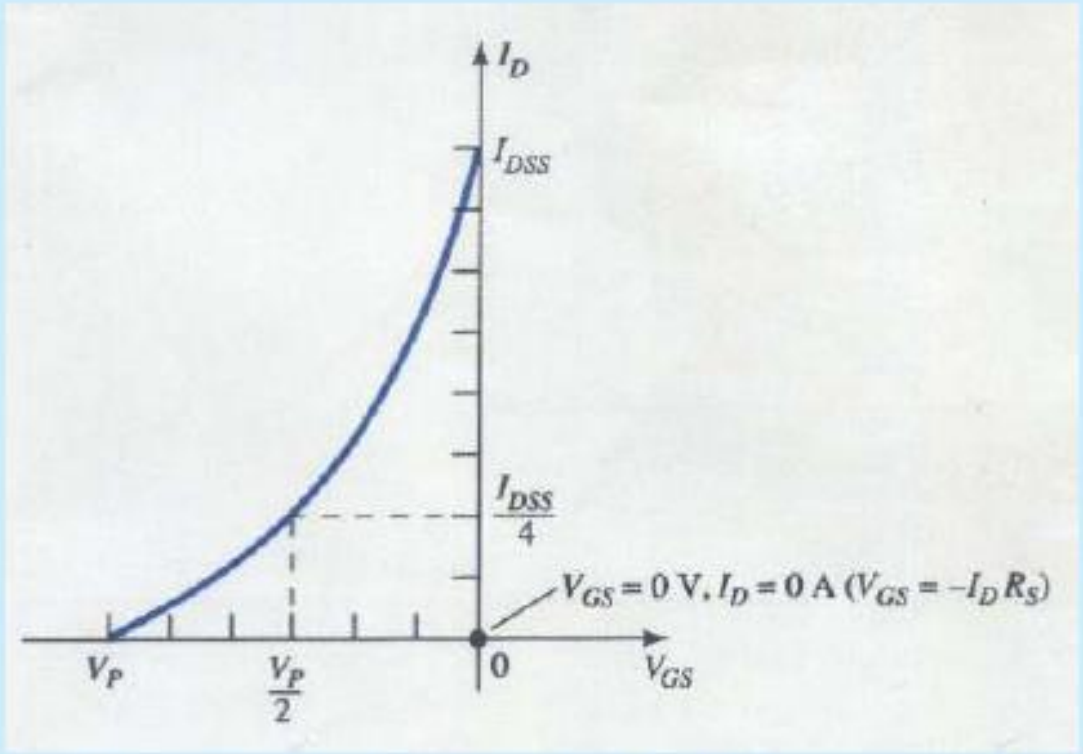
$V_{GS} = 0V$

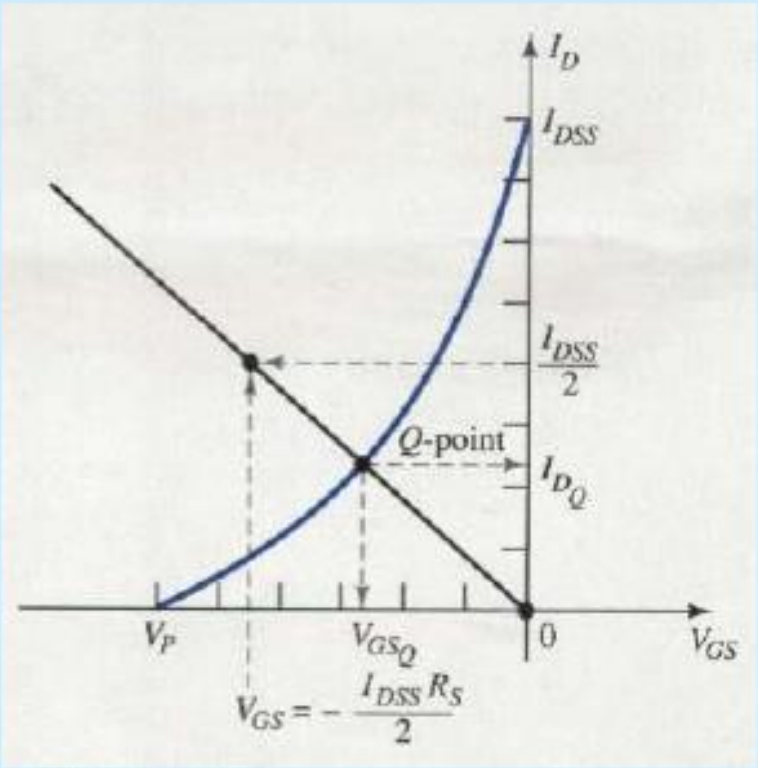
$I_D = 0A$

$I_D = I_{DSS}/2$

$V_{GS} = \frac{-I_{DSS}R_S}{2}$

Graphical Approach:





First, the transfer characteristics are defined using 4 points technique.

Then, a straight line has to be defined on the same graph by identifying two points.

Point (1); The most obvious condition to apply is $I_D = 0$ A since it results in $V_{GS} = -I_D R_S = (0\ A)\ R_S = 0$ V. Therefore, the first point is $I_D = 0$A and $V_{GS} = 0$V.

Point (2): For example, we choose a level of I_D equal to one-half the saturation level.

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

The straight line is drawn using the above two points and the quescient point obtained at the intersection of the straight line plot and the device characteristic curve.
The quescient values of I_D and V_{GS} can then be determined and used to find the other quantities of interest.
The level of V_{DS} can be determined by applying KVL to the output circuit.

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

$$I_D = I_S$$

$$\boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$$

In addition;

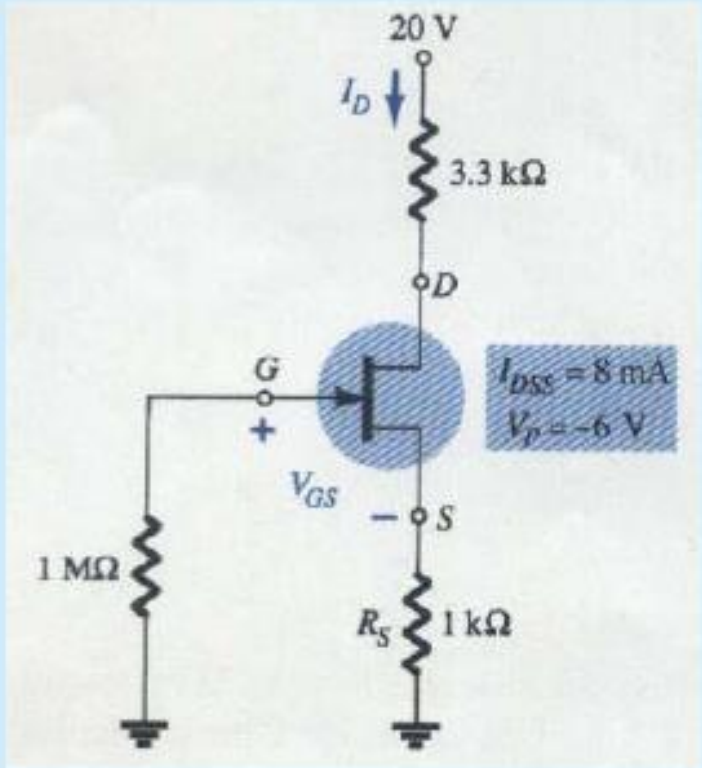
$$\boxed{V_S = I_D R_S}$$

$$\boxed{V_G = 0\,\text{V}}$$

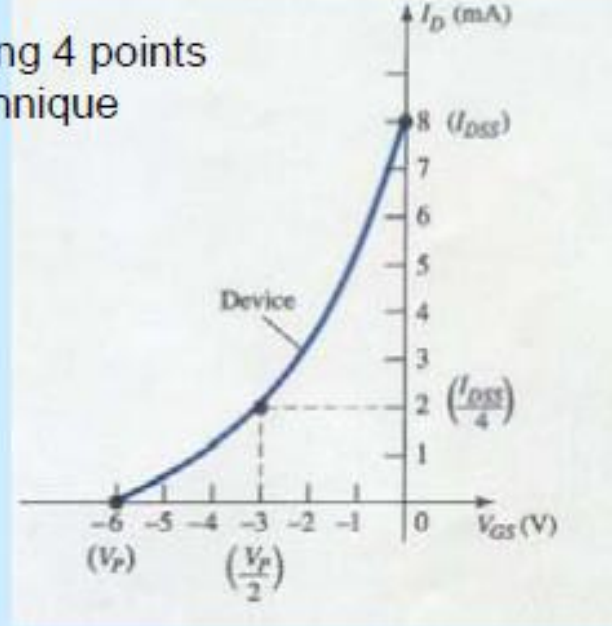
$$\boxed{V_D = V_{DS} + V_S = V_{DD} - V_{R_D}}$$

Example (2): Determine the following.

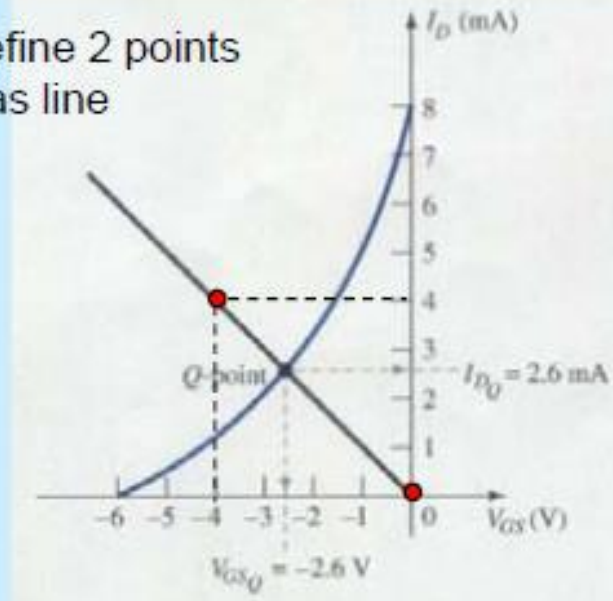
(a) V_{GS_Q}.
(b) I_{D_Q}.
(c) V_{DS}.
(d) V_S.
(e) V_G.
(f) V_D.



Using 4 points technique



Define 2 points bias line



Basic equation;

$$V_{GS} = -I_D R_S$$

Example: $I_D = 4\text{ mA}, \quad V_{GS} = -(4\text{ mA})(1\text{ k}\Omega) = -4\text{ V}$

(a) $V_{GS_Q} = \mathbf{-2.6\ V}$

(b) At the quiescent point:

$$I_{D_Q} = \mathbf{2.6\ mA}$$

(c) Eq. (6.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$

$$= 20\ \text{V} - (2.6\ \text{mA})(1\ \text{k}\Omega + 3.3\ \text{k}\Omega)$$

$$= 20\ \text{V} - 11.18\ \text{V}$$

$$= \mathbf{8.82\ V}$$

(d) Eq. (6.12): $V_S = I_D R_S$

$$= (2.6\ \text{mA})(1\ \text{k}\Omega)$$

$$= \mathbf{2.6\ V}$$

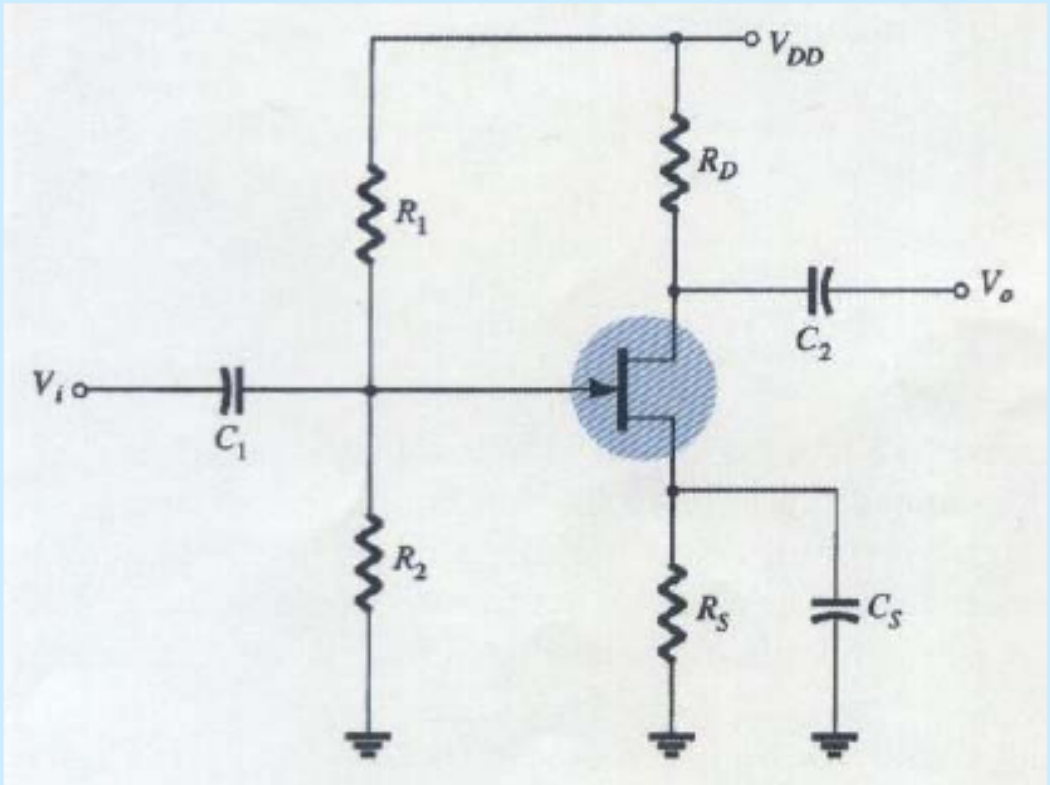
(e) Eq. (6.13): $V_G = \mathbf{0\ V}$

(f) Eq. (6.14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

(C) VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied To FET amplifiers.

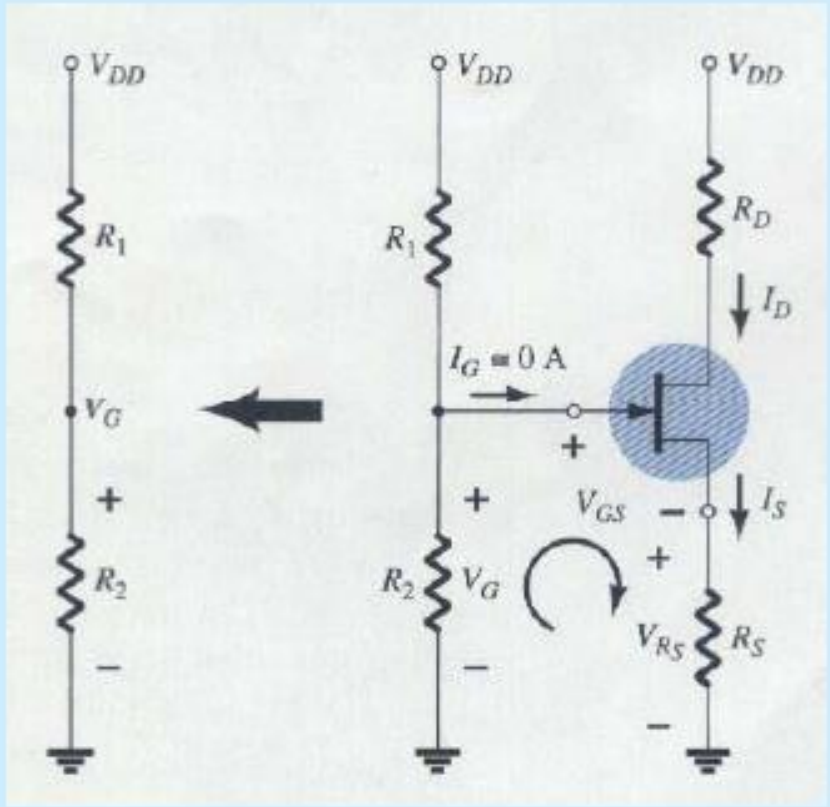


The basic construction is exactly the same but the dc analysis of each is quite difference.

I_G = 0A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits.

Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network can be redrawn as shown in the next slide for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.



KCL requires that $I_{R1} = I_{R2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G.

The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

KVL in the clockwise direction to the indicated loop will result in

$$V_G - V_{GS} - V_{R_s} = 0$$

$$V_{GS} = V_G - V_{R_s}$$

and substituting $V_{R_s} = I_S R_S = I_D R_S$, we have

$$V_{GS} = V_G - I_D R_S$$

The procedure for plotting the above equation is not a difficult one and will proceed in the next slide.

Since any straight line requires two points to be defined, first we can use the fact that anywhere on the horizontal axis, the current $I_D = 0$ mA. Therefore, select I_D to be 0 mA, we are stating that we are somewhere on the horizontal axis.
The exact location can be determined by substituting $I_D = 0$ mA into the previous equation and finding the resulting value of V_{GS} as follows:

$$V_{GS} = V_G - I_D R_S$$
$$= V_G - (0\text{ mA})R_S$$

Point No.1

$$V_{GS} = V_G|_{I_D = 0\text{ mA}}$$

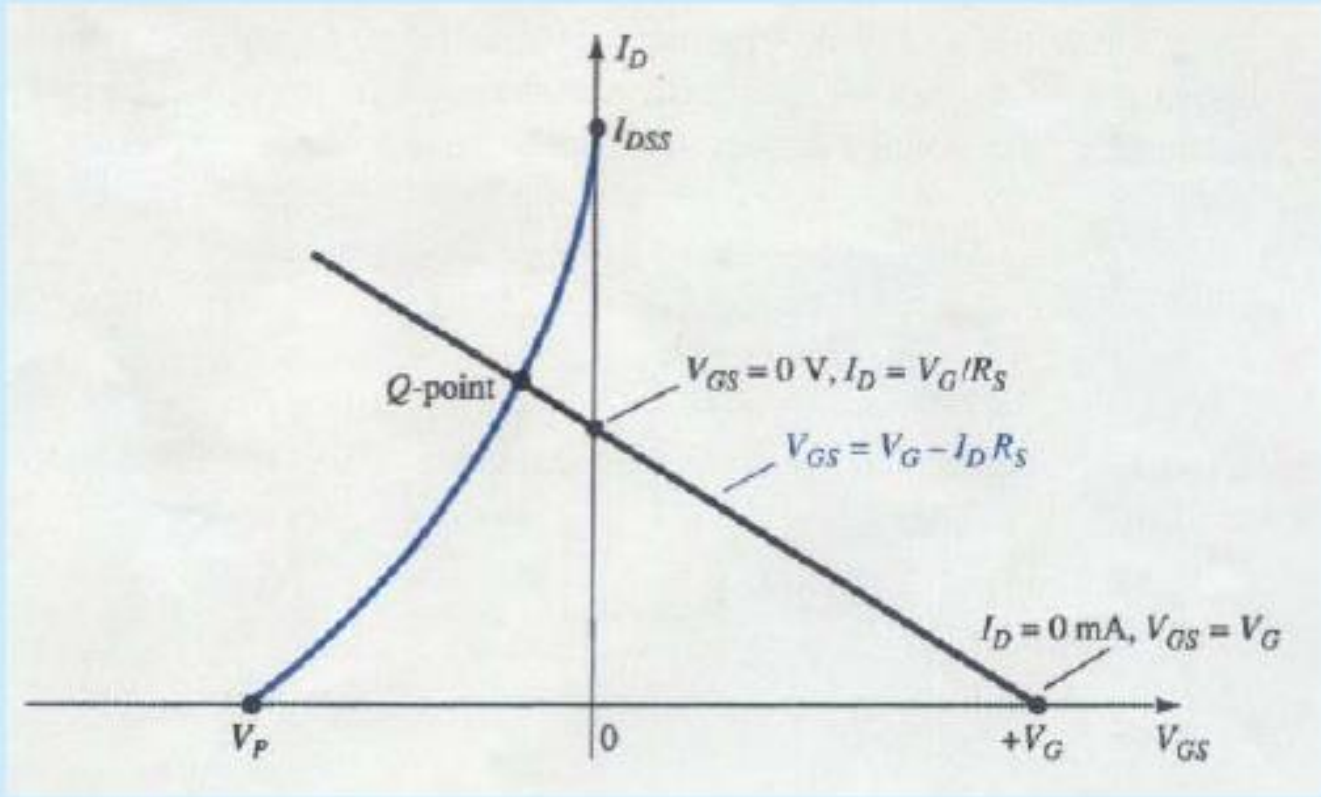
The result specifies that whenever we plot the above equation, if we choose $I_D = 0$ mA, the value of V_{GS} for the plot will be V_G volts.

For the other point, let us employ the fact that at any point on the vertical axis $V_{GS} = 0$ V and solve for the resulting value of I_D:

$$V_{GS} = V_G - I_D R_S$$
$$0\text{ V} = V_G - I_D R_S$$

Point No.2

$$I_D = \frac{V_G}{R_S}\bigg|_{V_{GS} = 0\text{ V}}$$



The two points defined in the previous slide permit the drawing of a straight line. The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

$$V_{GS} = V_G - I_D R_S$$

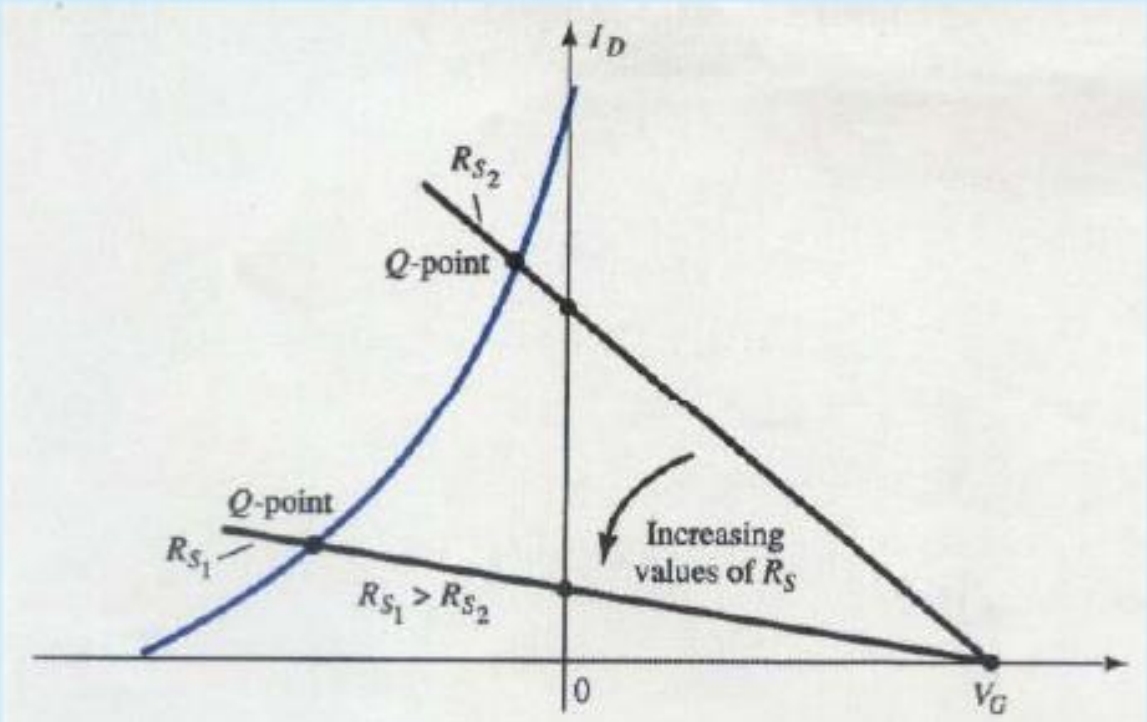
$$0\,\text{V} = V_G - I_D R_S$$

$$I_D = \left.\frac{V_G}{R_S}\right|_{V_{GS} = 0\,\text{V}}$$

Since the intersection on the vertical axis is determined by $I_D = V_G/R_S$ and V_G is fixed by the input network, increasing values of R_S will reduce the level of the I_D intersection as shown in the figure.

It is fairly obvious that:

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.



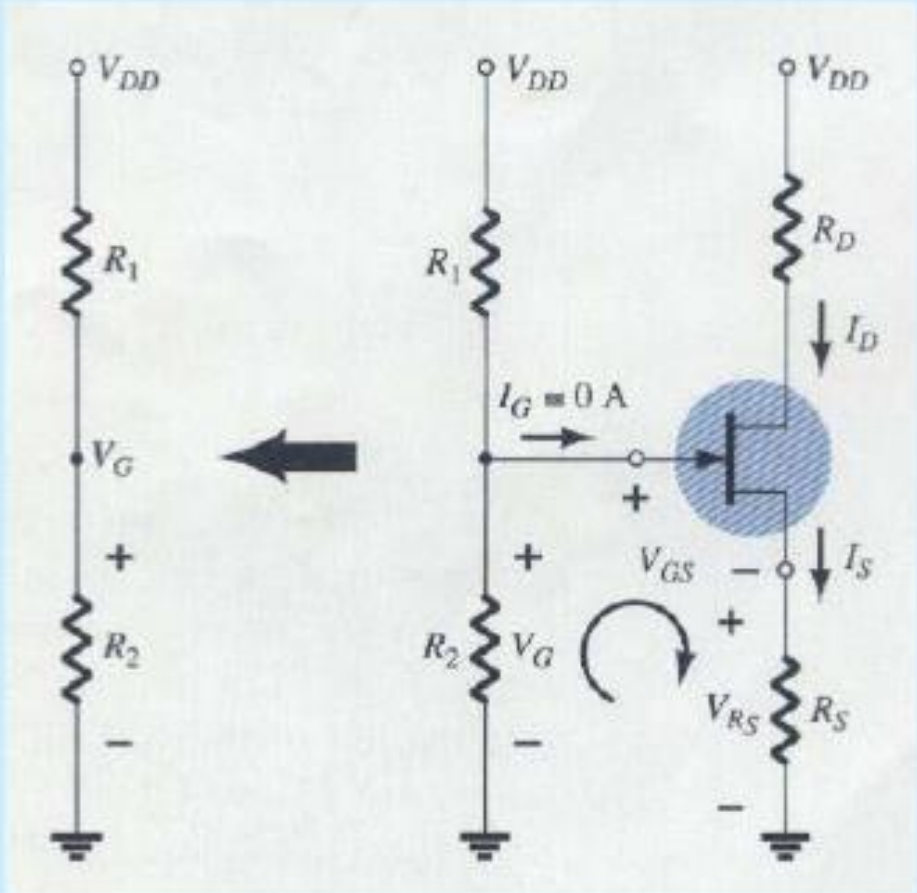
Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner.
That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

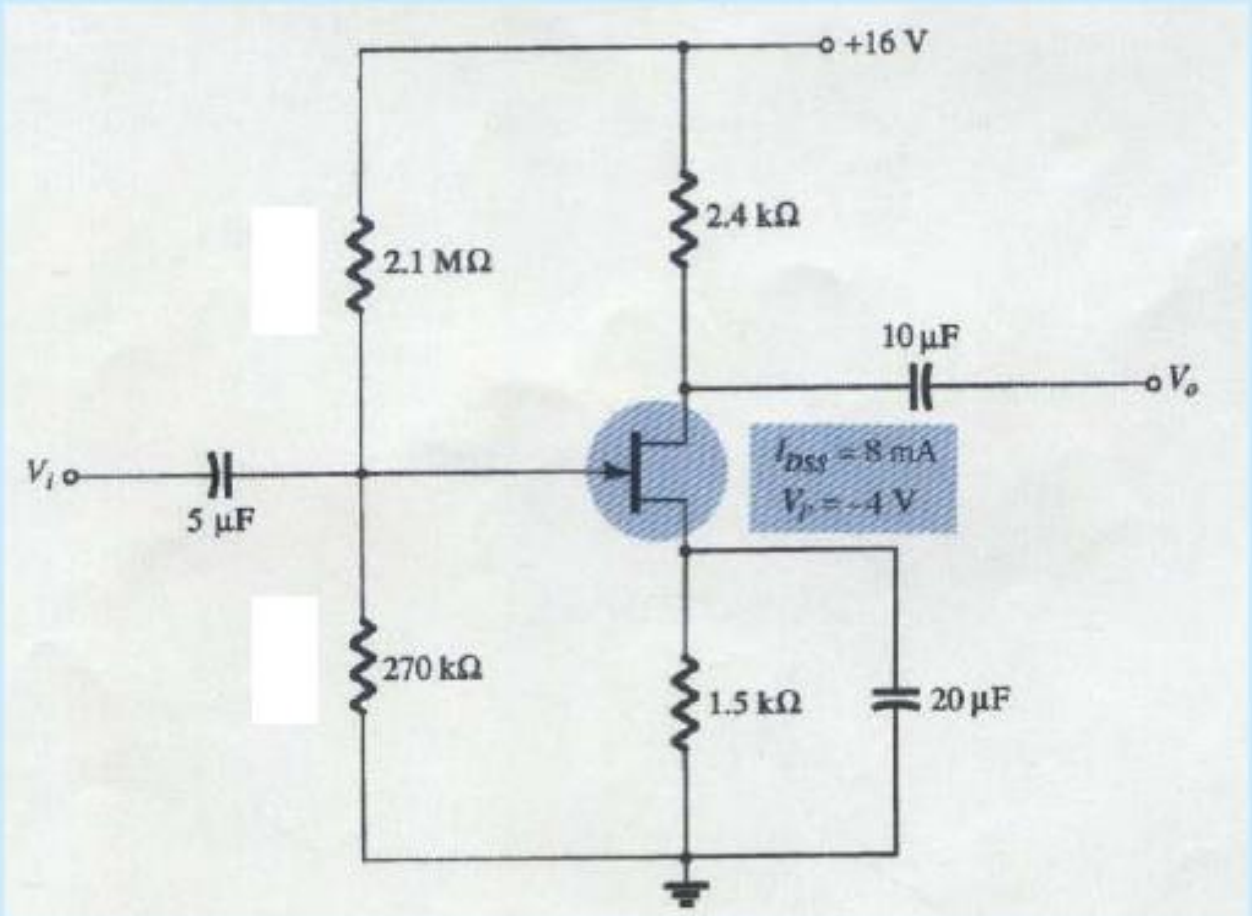
$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$



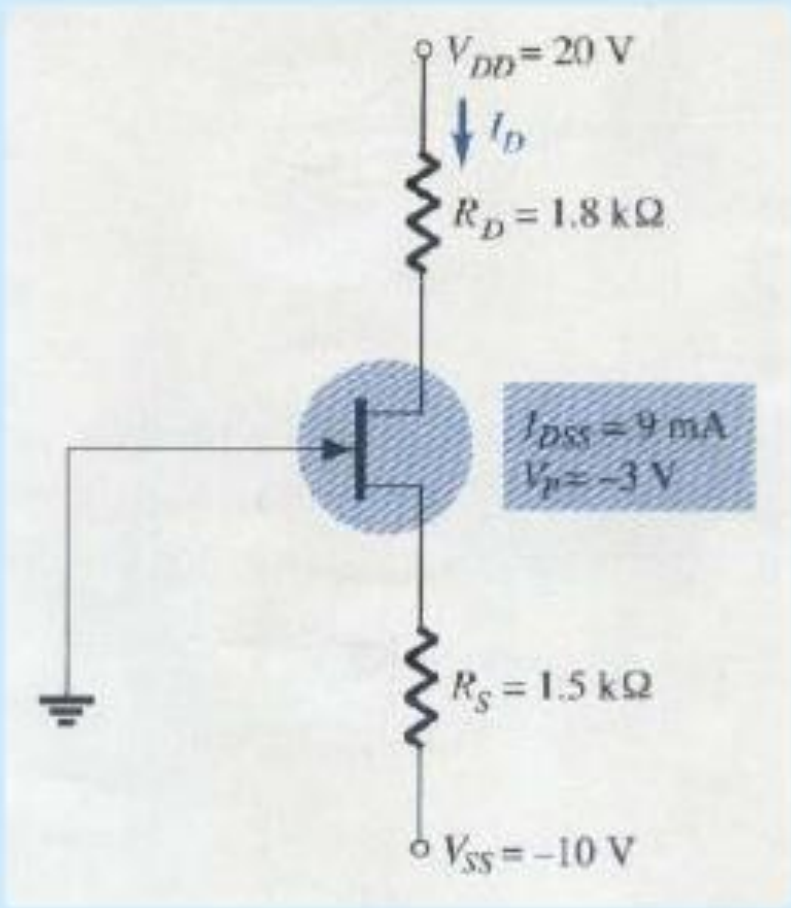
Example (3): Determine the following.

(a) I_{D_Q} and V_{GS_Q}.
(b) V_D.
(c) V_S.
(d) V_{DS}.
(e) V_{DG}.



Example (4): Determine the following.

(a) I_{D_Q} and V_{GS_Q}.
(b) V_{DS}.
(c) V_D.
(d) V_S.



THE FIELD-EFFECT TRANSISTOR

Comparison between the BJT and the FET

BJT	*FET*
1. Two types of carriers (electrons and holes) are required.	1. Only one type of carrier (electron or hole) is required.
2. Carriers move through the base by diffusion process.	2. Carriers move through the channel by drift process.
3. The BJT has a comparatively lower switching speed due to the diffusion process.	3. The FET has a higher switching speed due to the drift process; the drift of the carrier is faster than diffusion.
4. The BJT is not a thermally stable device.	4. The FET has a negative temperature coefficient at high-current operations, i.e., the current decreases as temperature increases Due to this particular feature, a uniform temperature distribution and protection against breakdown can be achieved.
5. In case of IC fabrication, the BJT requires more space than the FET.	5. In case of IC fabrication the FET requires lesser space than the BJT.
6. At audio frequencies the BJT offers less power gain.	6. At audio frequencies the FET offers greater power gain.
7. The BJT is a current-controlled device.	7. The FET is a voltage-controlled device.
8. The BJT offers low input impedance.	8. The FET offers high input impedance, therefore, it can be used as a buffer.
9. BJT is much noisier than FET.	9. FET is less noisy.
10. The BJT has offset voltage.	10. The FET has no offset voltage.
11. The BJT can also be used as a switch; it is taken to be in the OFF state when operating in the cut off region, and in the ON state when it is operating in the saturation region.	11. The FET is particularly useful for its operation as a controlled switch, operating in both the conducting and the non-conducting zones.