

- IC fabrication } Backend
- HDL - Hardware Description Language }
- VHDL }
- Verilog - Verification Language } Frontend
 - supports testing
- System verilog (OOPS)
- UVM - Universal Verification Methodology
 - for verifying integrated circuit Designs
- (+Python
+matlab)
- FPGA - Field Programmable Gate Array
 - It is an IC that consists of internal hardware blocks with user programmable interconnects to customize operation for a specific application.
 - FPGA's are used in place of microprocessors.
- Verilog ... Drawback : Precision

Units: ① Fabrication

② Parametric Analysis - V, I, Figure of merits, ID, IO, RC(C), delay, frequency

③ Logic

④ Latest Trends

Basics:

→ EDC : BJT - Working, VI characteristics

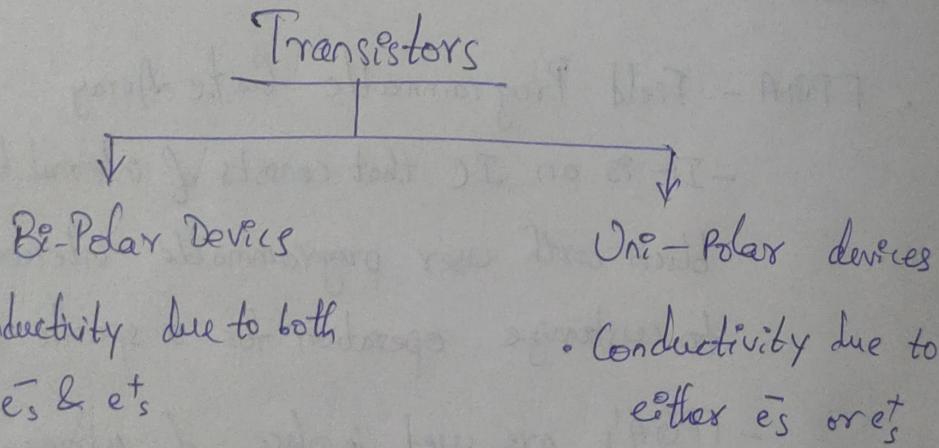
FET (MOSFET) - Working, Symbol,

VI characteristics

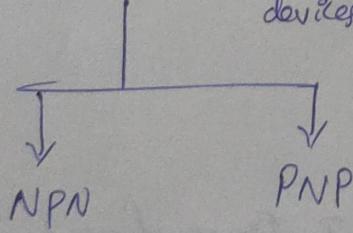
→ DSD :- MUX, De-mux, flip-flops, Adders, Encoders,
Decoders

- Variable devices

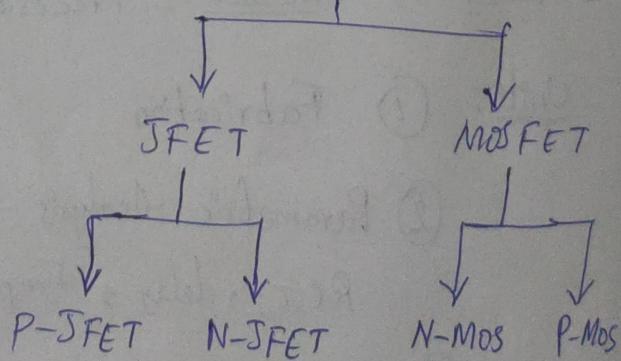
- Transistors : Trans - multiple & estors - terminals
(electronics) → from Greek



BJT (current controlled devices)



Unipolar (voltage controlled devices)



. In core-semiconductor industries : MOSFET's (77%)
BJT's (11%)

- JFET used as Driver cards
 - BJT as integrator circuit for integration
 - MOSFET - Building blocks of semi-conductors.
 - IC - integration of circuits
 - BJT - drives the load (Bi-polar Junction Transistor)
 - MOSFET - Evaluates the Logic
 - Metal Oxide Semiconductor Field Effect Transistor
- IGFET - Insulated Gate FET

→ Logical evaluation by MOSFET, this output should be driven properly and it is taken care by BJT.

03/01/2023

MOSFET / IGFET :

- Metal Oxide Semiconductor Field Effect Transistor
- Insulated Gate Field Effect Transistor
- Based on type of substrates : (mobility)
 - MOSFET
 - N-MOSFET ($1200 \text{ cm}^2 \cdot \text{V/sec}$)
 - P-MOSFET ($700 \text{ cm}^2 \cdot \text{V/sec}$)
- Spec, Effect/Efficiency, Power Utilization, Noise immunity,
• 100% nullification of noise is not possible.
- Speed, Low power consumption, Noise immunity
(Expectations / Required ones of an electronic circuit)]
- Building Blocks of Electronics - MOSFET's
- Substrate : Pure Si wafer
- $\mu_e > \mu_h \Rightarrow$ Switching speed is high
(mobility) Max. current can be drawn \Rightarrow Saturated state
- So N-MOSFET preferable over P-MOSFET, as majority carriers are e^- & minority carriers are holes in N-MOSFET.
- $I_{CE(\text{sat})}$ - In saturation state, max. current can be drawn and it can be used as a switch (in active region)
 $I_{C(\text{max})}$ (ON)

• Reverse Recovery time : from $I_{C(sat)}$ to 0

• Active region : The region from 0 to $I_{C(sat)}$
~~Cut~~ (for an amplifier)

→ In Active region, no clipping of signal occurs.

• High mobility - switching speed increases.

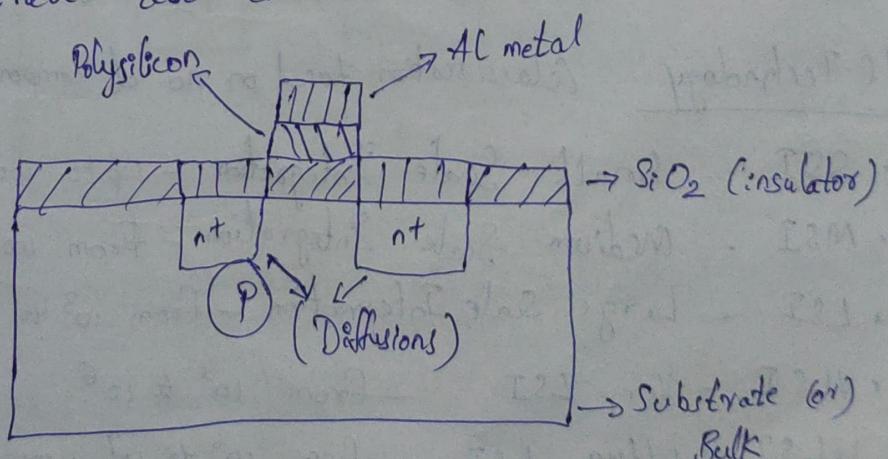
N-MOSFET : (Drain current is due to e^-) (Uni-polar device) (I_D)

• B, Al, In, Ga - Trivalent elements (P-type elements)

• P, As, Sb (Antimony) - Pentavalent element (N-type elements)

• Dope substrate with P-type impurity.

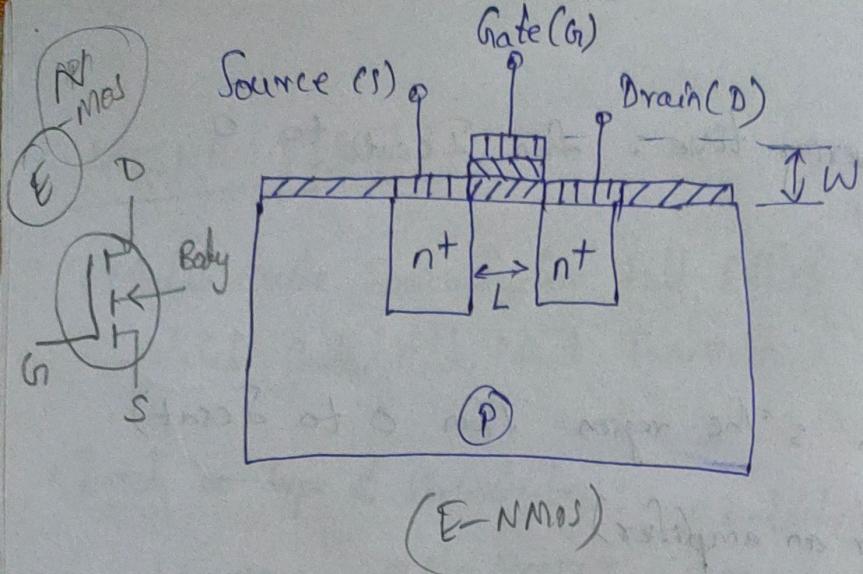
• Substrate also called as Bulk.



• n⁺ → means highly doped

• Diffusions or Implant

• n++ → very highly doped



→ Al metal
 → Poly silicon
 → SiO₂

- Length of Channel 'L' → Distance b/w Source implant & Drain implant.

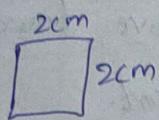
H.W

- SSI, VLSI, Scaling Integrations, Mealy, Massey Laws
- Moore's Law : states that every 2 years the no. of transistors in a chip should double.
- Size of Transistor : Parameters
 - Length of channel (L) Ex: 5 nm
5 × 10⁻⁹ m
 - Width of Gate ~~Resistor~~ (W)
 - Scaling - changing . Scale means to change

IC Technology Classification based on no. of components integrated

- SSI - Small Scale Integration - up to 100 components
- MSI - Medium Scale Integration - from 100 to 10³ "
- LSI - Large Scale Integration - from 10³ to 10⁵
- VLSI - Very LSI - from 10⁵ to 10⁶
- ULSI - Ultra LSI - from 10⁶ to 10⁹ components
- GLSI - Giant LSI
- Nano Technology

- No. of transistors accommodation in the given chip of area 'A' has been increased over the years



In 1960 - 10 Transistors accommodated

1970 - 40

1980 - 50

1990 - 100

2000 - 1000

2010 - > 2000

2020 - > 1 lakh

- Over the years, size of transistor made smaller & smaller.

- Increase or Decrease 'Z' w.r.t the aspect ratio of W.

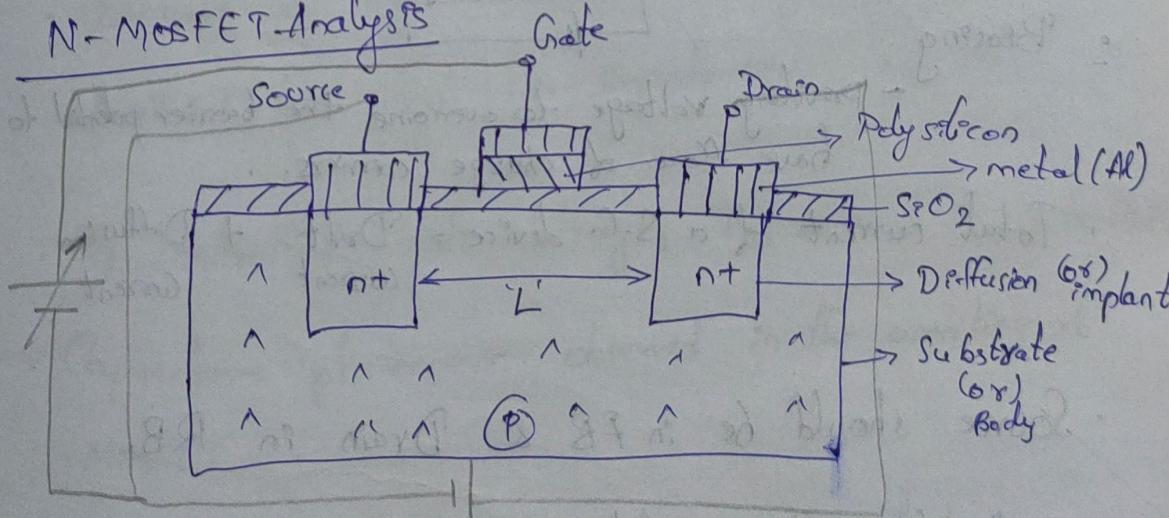
W.

- $Z = \frac{W}{L}$ • Z' - Aspect ratio

- Scaling: \sqrt{L} - to increase speed of operation

04/01/2023

N-MOSFET Analysis



(E-NMOS) MOSFET (Based on structure)

Enhancement MOSFET

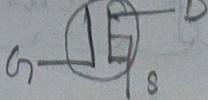
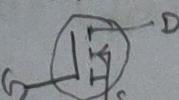
E-NMOSFET

E-PMOSFET

Depletion MOSFET

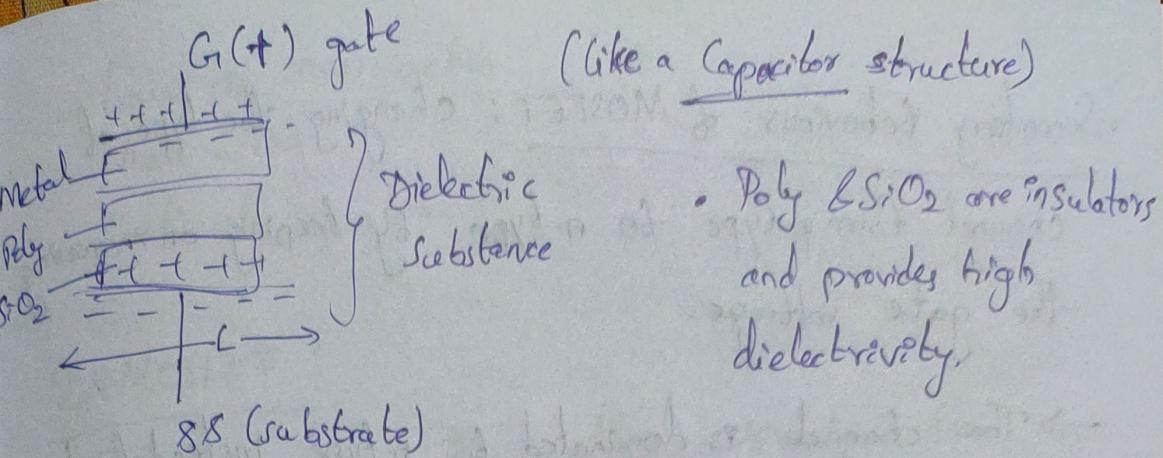
D-NMOSFET

D-PMOSFET



04/01/2023

- Source : Pumps out the carriers.
 → Where charge carriers take birth.
 → These charge carriers tries to move towards the drain and this causes current.
- Drain : I_D (or) I_{DS} → Drain Current
- Charge carriers move from source to drain via channel.
- Distance b/w source & drain - Length of channel.
- Diffusion current : (happens by nature, by attraction.)
 (by virtue of potential difference) \Rightarrow recombination of e^- & h^+ takes place.
- Barrier Potential
- Biasing - Providing voltage to overcome the barrier potential to have flow of charge carriers.
- Total current of a S.C. device = Drift current + Diffusion current
- Source should be in FB & Drain in RB.
- Gate terminal is like a tap of water
- By controlling Gate voltage, we can control flow of charge carriers & so called the device is called as Voltage controlled device

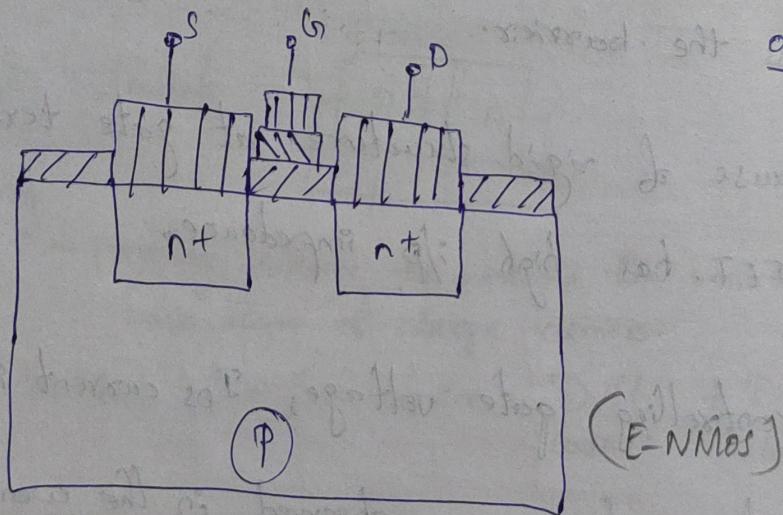


- Poly & SiO_2 are insulators and provides high dielectrivity.

- Input Impedance of MOSFET is very high ($\approx \infty$)
- Input i.e. Analog or Digital information comes through Gate terminal.
- The input has a hurdle / barrier, input need to cross the barrier.
- Because of rigid structure at gate terminal, MOSFET has high i/p impedance.
- By controlling gate voltage, I_{DS} current is controlled.
- Capacitance phenomenon observed in the working of MOSFET.
- The voltage (at gate terminal) at which drain current observed is called threshold voltage.
- Gate voltage $< V_{TH}$; electrons get recombined by the holes (in substrate) in channel.

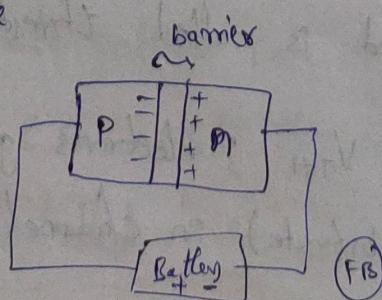
- Secondary behaviour of MOSFET: changing the type of channel from p-type to n-type by keeping on increasing the gate voltage.
- The channel is dominated by n-type instead of p-type
- Mobility of ϵ_s i.e. speed of charge carriers by Forward biasing Source and Reverse biasing Drain.

★ Increasing or Decreasing i.e. Modulating the length of channel is called as Channel Length Modulation



In P-N junction

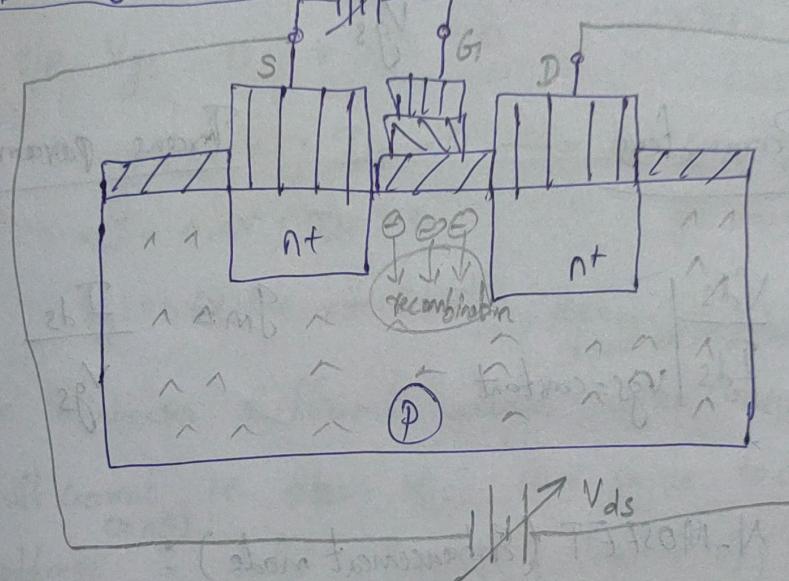
- As immobile ions get accumulated, free e^- & h^+ cannot pass through this barrier & so some biasing need to be given i.e. some supply voltage



- Laws of mass action
- Hall action
- Continuity equation

P-N-MOSFET :

- N_t , V_{gs} , V_{ds} , I_{ds} $\rightarrow V_{gs} \rightarrow$ AC analysis - (use low caps)



(E-NMOS)

- $V_{gs} \rightarrow$ Variable voltage \rightarrow gate-source voltage
 - Diffusion Current : it is by virtue of potential difference and recombination of e^- & e^+ takes place.
 - Initially, I_{ds} must maintain zero, if it is non-zero then it is dangerous. (i.e. diffusion current must be maintained zero, as drift current will be zero without supply)
 - I/P voltage : V_{gs}
 - O/P voltage : V_{ds}
 - O/P Current : I_{ds}
- } 3 parameters For Analysis

$$\rightarrow O/P \text{ Resistance} = \frac{V_{ds}}{I_{ds}} \quad | \quad V_{gs} = \text{constant}$$

Do partial differentiation
if more than 2 parameters

Do differentiation
- if 2 parameters

$$\cdot \text{Dynamic Resistance} = \frac{\Delta V_{ds}}{\Delta I_{ds}} \quad \left| \begin{array}{l} \\ \\ V_{gs} = \text{constant} \end{array} \right.$$

Transfer characteristics

$$\text{Static resistance} = \frac{\Delta V_{ds}}{\Delta I_{ds}}$$

$$\cdot \text{Trans Conductance: } g_m = \frac{I_{ds}}{V_{gs}}$$

Output Parameters

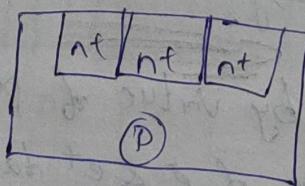
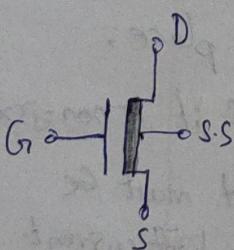
$$\text{O/P Resistance} = \frac{V_{ds}}{I_{ds}} \quad \left| \begin{array}{l} \\ \\ V_{gs} = \text{constant} \end{array} \right.$$

$$g_m = \frac{I_{ds}}{V_{gs}}$$

Trans parameters

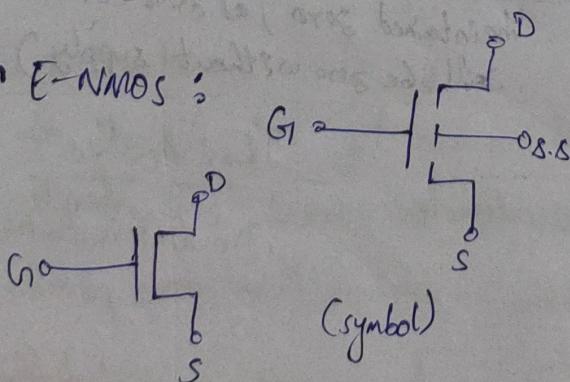
Working of N-MOSFET (Enhancement mode):

D-NMOS:



- Continuous channel
- Even without supply, there is a flow of drain-current (due to diffusion current)
- And so not preferred for industrial purpose.

E-NMOS:



• Discontinuous channel

• Hence, preferred

In D-NMOSFET, there is a continuous channel and even without V_{gs} , I_{ds} is observed.

I_{ds} is observed even ^{when} input voltage V_{gs} is not supplied
i.e. $V_{gs} = 0$ in D-MOSFET

Hence, E-MOSFET preferred over D-MOSFET

Working of E-NMOS:

O/P $V_{gs} = 0 \Rightarrow I_{ds} = 0 \rightarrow V_{ds}$ is maintained constant.

$V_{gs} = 0.2V ; I_{ds} = 0 \rightarrow$ As holes of p-substrate
 $V_{gs} = 0.4V ; I_{ds} = 0$ get recombined with $\bar{e}s$

$V_{gs} = 0.6V = V_t ; I_{ds} = i_0(nA)$ (that should be supplied)

The minimum sufficient voltage which causes a small drift current i.e. efflux of $\bar{e}s$ from source to drain, such voltage is called threshold voltage ($V_t / V_s / V_{cat-en}$)

$V_{gs} = 0.8V ; I_{ds} \uparrow$

MOSFET
Source-Drain

$V_{gs} \uparrow$ then $I_{ds} \uparrow$

$$(2\mu C_s V_F)^2 = C_0(V) + \text{constant}$$

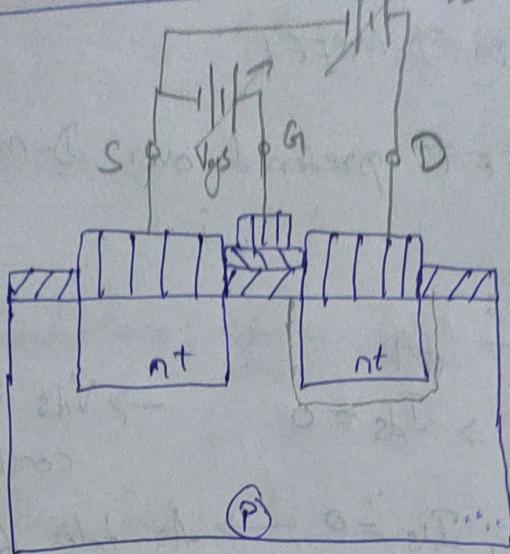
At particular point I_{ds} remains constant, as the channel completely filled with $\bar{e}s$

channel: Ptype to ntype

Secondary behaviour of MOSFET

N-MOSFET characteristics

10/01/2023



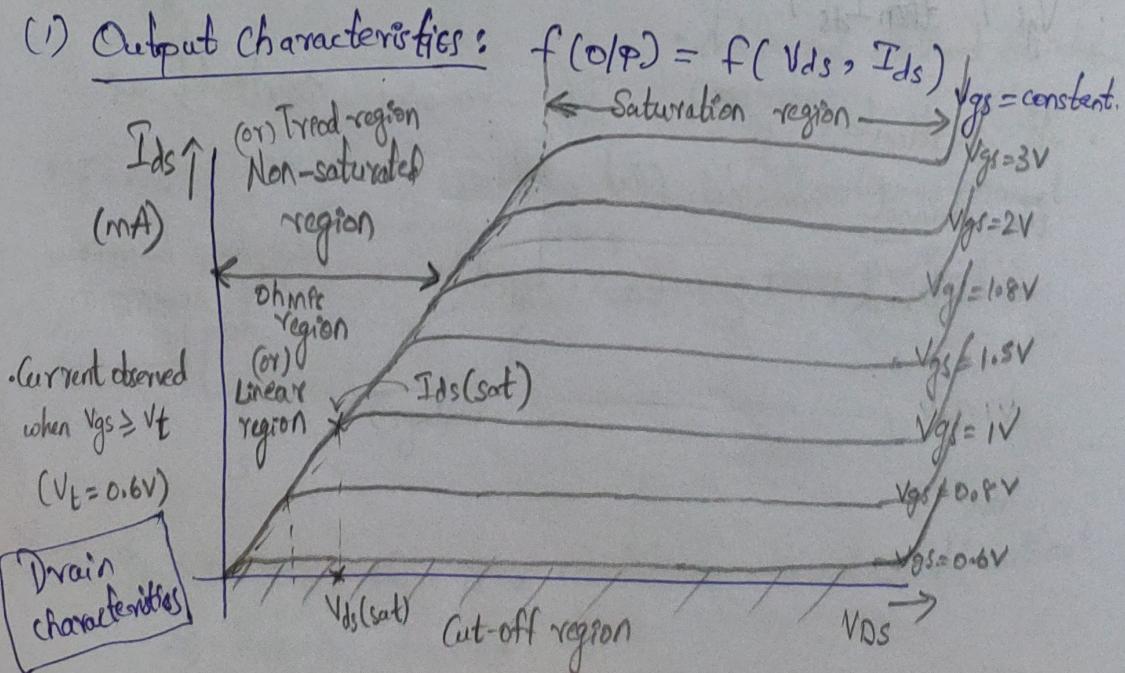
1. Capacitance phenomenon at Gate terminal.

2. Input given at Gate terminal, power supply or ground connected to Drain terminal.

MOSFET is a Bi-directional device i.e. source and drain terminals are interchangeable.

→ No deviation: in structure, in working phenomena & in I-V characteristics.

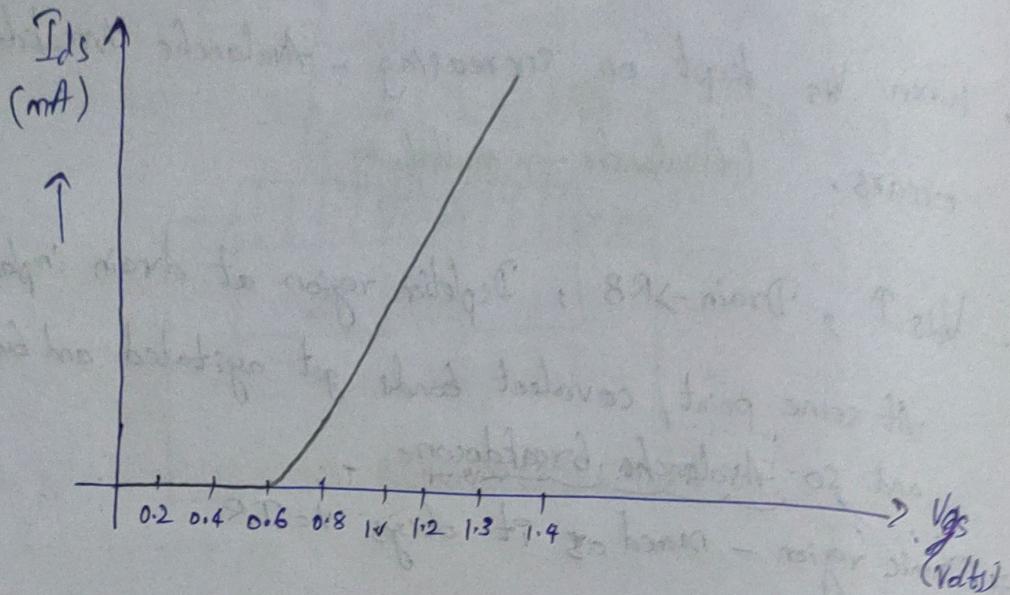
(1) Output characteristics:



- I_{ds} is independent of V_{ds} . (approximately) (when $V_{gs} = 0V$)
- When V_{ds} kept on increasing - Avalanche breakdown occurs. (Avalanche \rightarrow multiplying)
- $V_{ds} \uparrow$, Drain \rightarrow RB, Depletion region at drain implant \uparrow , At some point, covalent bonds get agitated and burst out and so Avalanche breakdown.
 → Ohmic region - named as it obeys $V = IR$
- MOSFET used in applications like in amplifying to avoid high noise effects.
- For designing amplifier, we operate MOSFET in Ohmic region.
- For switch purposes, operated in Saturation region (ON) and Cut-off region (OFF).
- Output characteristics other name Drain Characteristics.

- $V_{ds(\text{sat})}$ - point at which $I_{ds(\text{sat})}$ obtained i.e. $I_{ds(\text{maximum})}$ or saturated.
- $I_{ds(\text{sat})}$ - maximum I_{ds} at fixed V_{gs}
- $V_{ds(\text{sat})}$ is dependent on V_{gs}
 $V_{gs} \uparrow$ then $V_{ds(\text{sat})} \uparrow$
- $V_{ds(\text{sat})}$ - value of Drain-source voltage at which I_{ds} saturates
- $V_{ds(\text{sat})}$ always calculated at fixed V_{gs} and by $I_{ds(\text{sat})}$

(2) Transfer characteristics : I_{ds} vs V_{gs}

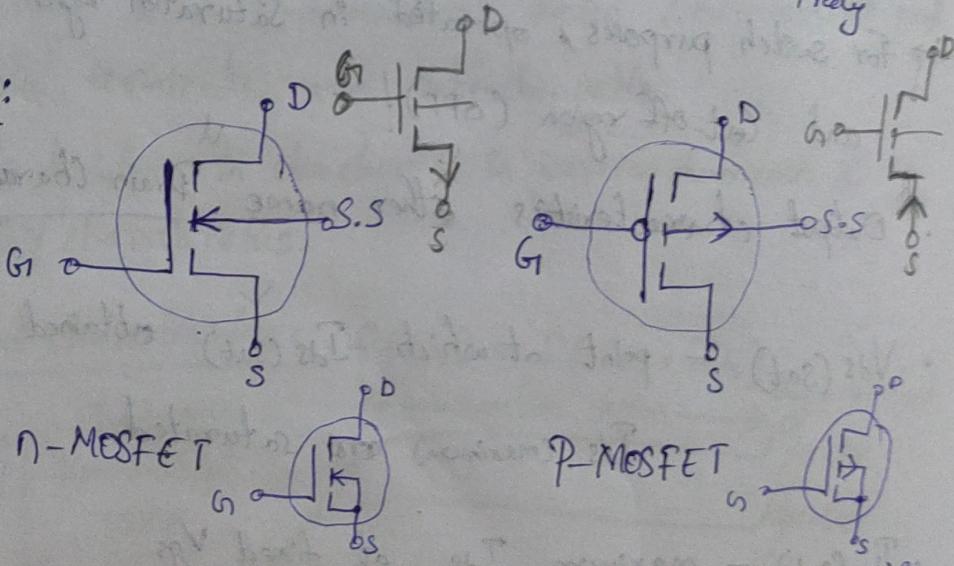


- $V_{gs} \uparrow \rightarrow$ mobility of charge carriers $\uparrow \rightarrow$ Velocity saturation state?

- Drain barrier induced i.e. no barrier $\Rightarrow e^-$ moves freely

Symbol:

Enhancement mode



- Bubble is given in P-MOS symbol, bubble means NOT (-ve), as in P-MOS we give -ve V_{gs} .

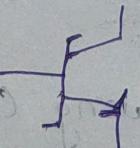
① D - MOSFET

Assignment

② Moore's Law

③ N - MOSFET
(Refresher)

Technologies (Logics)

- 1) R-R Logic
 - 2) D-R Logic
 - 3) DDL - ^{more} power dissipations
 - 4) DTL
 - 5) TTL ^{got an idea} \rightarrow ^{Reverse Recovery time is high (dead time of TTL)} I_G
- Shaky transistor :  (+) good reverse recovery time
- ✓ 6) ECL - Emitter Coupled Logic (fastest logic)
 - 7) NMOS Logic
 - 8) PMOS Logic
 - ✓ 9) CMOS Logic (Low Power consumption)
 - 10) P-PMOS Logic (Pseudo-PMOS)
 - 11) P-NMOS Logic
 - 12) CCMOS / C²MOS Logic (clocked CMOS)
 - 13) Domino Logic
 - ✓ 13) BiCMOS (High Driving capability & Low Power consumption)

12/01/2023

Introduction

① MOSFET

↳ n-MOSFET }
↳ p-MOSFET } V-I characteristics

② Technologies

* ③ Logic Design - (*) ~~and~~ nMOS, PMOS, CMOS

(*) Inverter / NOT gate Design.

(*) " " " Analysis

④ Logic Gates Design using CMOS Logic

⑤ Fabrication process

(i) nMOSFET (ii) p-MOSFET (iii) CMOS

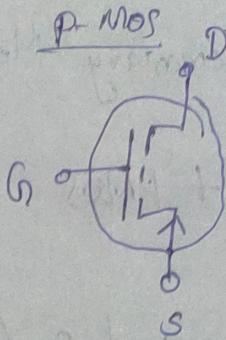
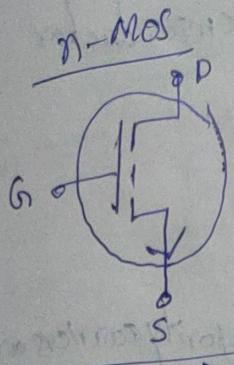
⑥ Stick Diagrams and Layout Design

⑦ CMOS Analysis & Driving Circuits

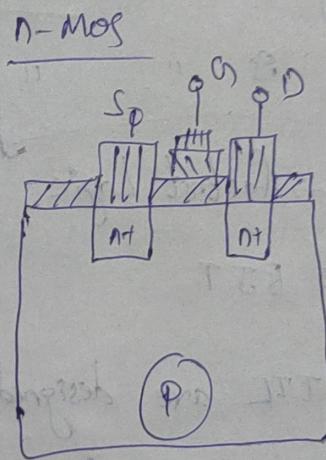
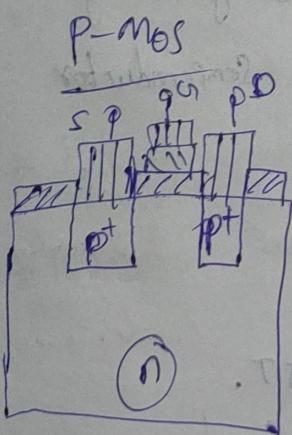
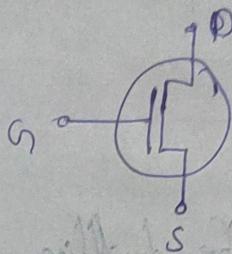
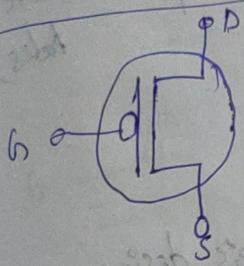
Brings

Crayons

Sketch
Pens



Enhancement Mode



$V_{GS} \rightarrow$ (-ve)

$V_S \rightarrow$ +ve terminal

$V_D \rightarrow$ -ve terminal

Si on chip 1cm x 1cm



• Around 200 ICs need to be fabricated on the Si chip

• For every IC, equal powersupply, and same clockpulse need to be given.

• All IC's should be in equilibrium

• Sometimes due to long wiring, IC's at distant may not receive same powersupply \rightarrow This is dangerous

$$V_{PP} = 12V \rightarrow 11.9V$$

$$f = 10 \text{ MHz} \rightarrow 9.99 \text{ MHz}$$

- CMOS : Complementary Metal-Oxide Semiconductor

- CMOS = NMOS + PMOS

Drawbacks

- PMOS : Switching speed is low (as majority carriers are holes)
- NMOS : Continuous ON

→ 'NOT' gate is the building block of logic design.

→ MOSFET is a Semiconductor

→ ECL → fastest Logic BJT

→ TTL → BJT

→ ECL & TTL are designed using BJT.

Q. Why ECL is the fastest logic : due to avoidance of saturation region for application.

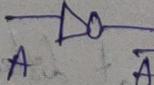
★ LOGIC DESIGN ★

- Power rails

(Power supply) ————— V_{DD} (Pull-up Transistor/Region)

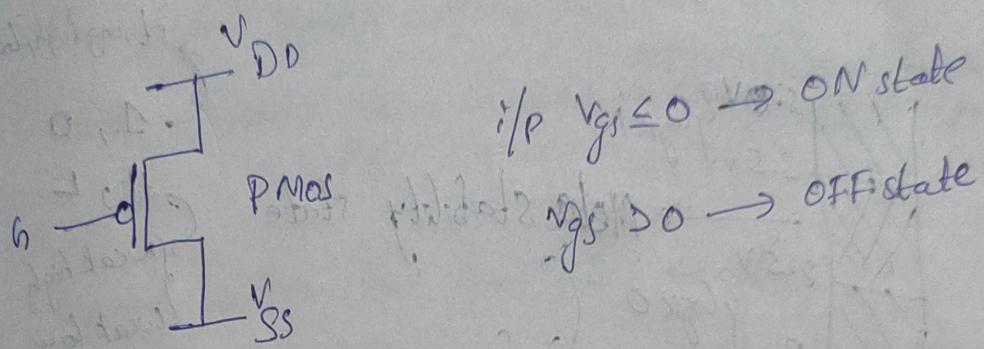
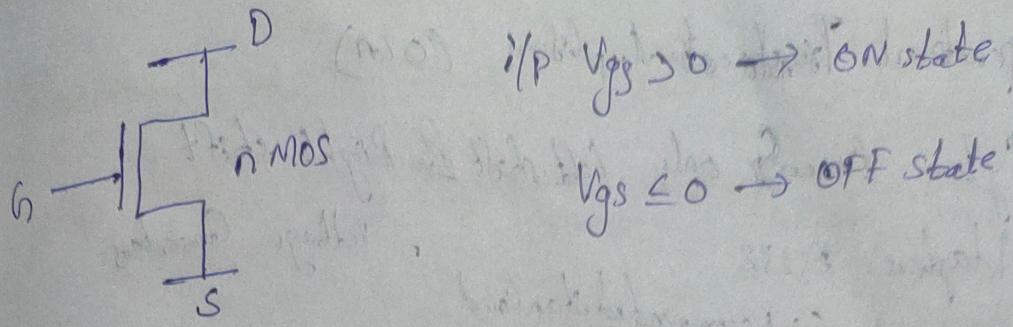
(Substrate) ————— V_{SS} (Pull-down Transistor/Region)

- NOT gate



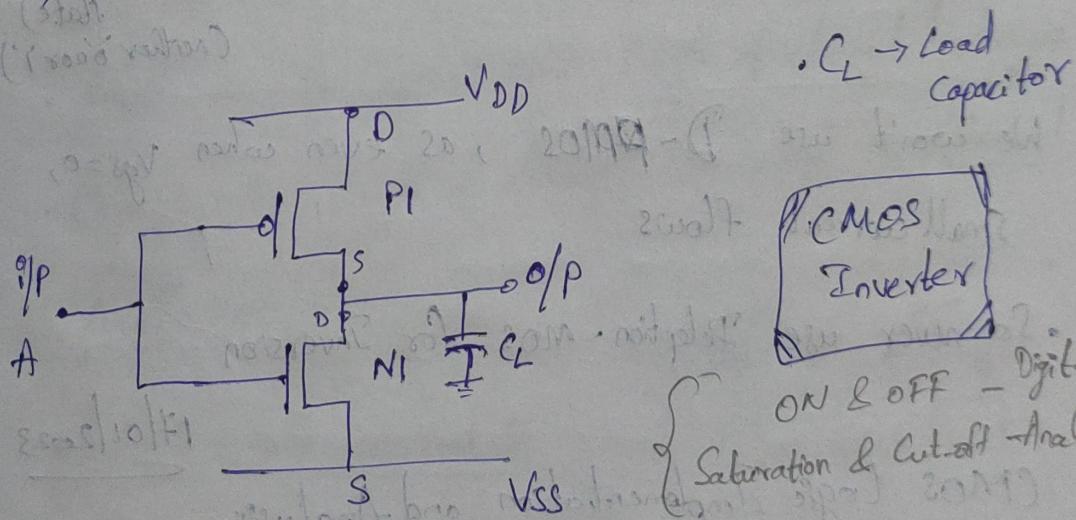
A	Y = \bar{A}
0	1
1	0

Inverter, Negation, Complementary



→ Pull-up Transistor : → Always PMOS used

→ Pull-down Transistor : → Always nMOS used



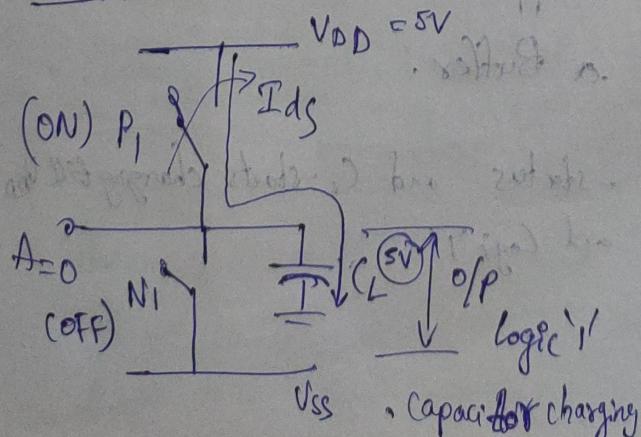
CMOS Inverter

ON & OFF - Digital

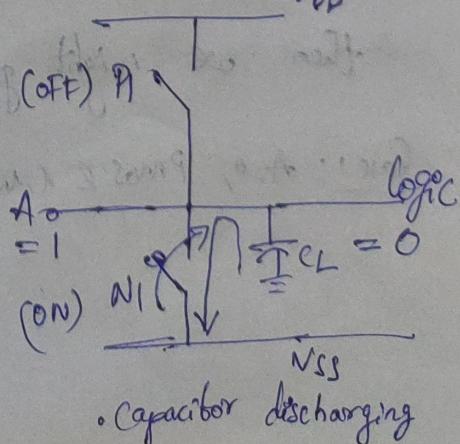
Saturation & Cut-off - Analog

Switching Diagrams / Circuit / network

Case(i) $A=0$:

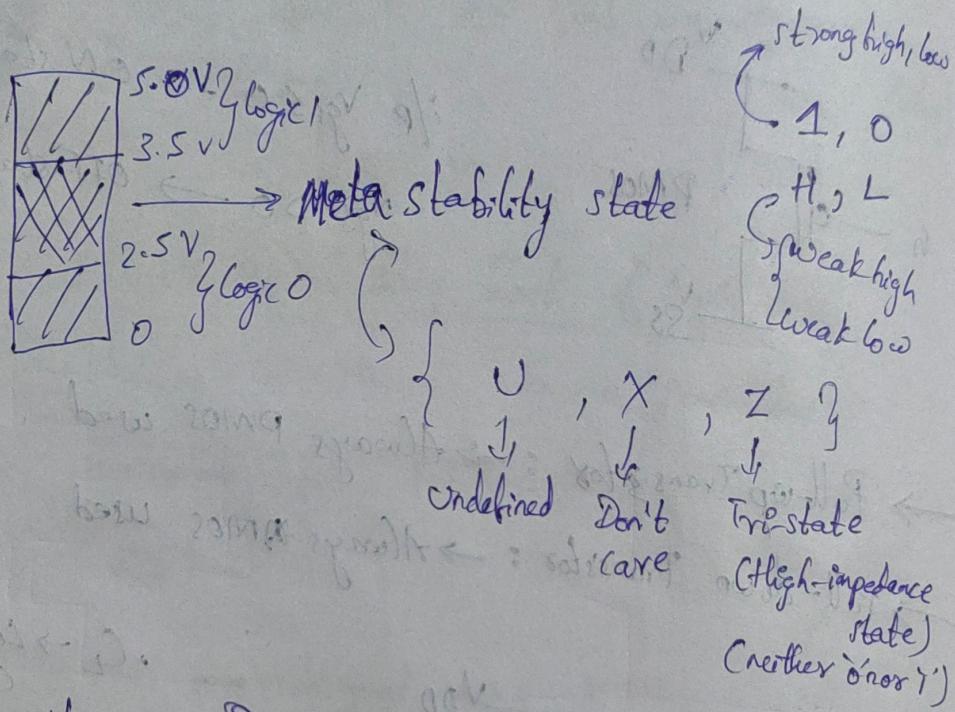


Case(ii) $A=1$



• Operational Transistor Logic (OTL)

- System knows only Left shift & Right shift.
- Adapters, RS232 → Voltage Converters
- Recommended Standard



- We won't use D-MOS, as even when $V_{GS} = 0$, small current flows
- So never use Depletion-MOS for Inversion

17/01/2023

CMOS Logic Implementation and Analysis

- If P-MOS & N-MOS swapped in the inverter circuit, then we might get a Buffer.

Case 1: A=0, PMOS & NMOS - starts and C_C-starts charging till V_{DD} and logic '1'

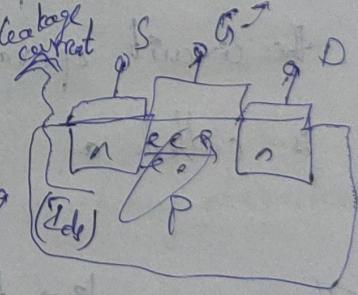
17/01/2023

Power dissipations:

$$P_{\text{Total}} = P_{\text{static}} + P_{\text{dynamic}} + P_{\text{leakage}}$$

- The total power dissipations in a circuit is the sum of static power, dynamic power dissipation & leakage power dissipation.

- Dynamic Power \rightarrow Transition from one form to other
- Static Power \rightarrow circuit in a single state for a long time.
- Leakage Power \rightarrow When L' - length of channel is then leakage current doubles.
- Based on V_{GS} applied, the length of channel changes.
- Changing the length of channel is called as Channel Length Modulation
- Sub-threshold current:
 \rightarrow Current due to recombination of e^- & e^+ (e^- in p substrate)
- Leakage current: Current goes out through some cracks, when $V_G < V_S$.
- The sub-threshold current need to go out, but it cannot go out through gate or drain and so it comes out through SiO_2 from substrate.

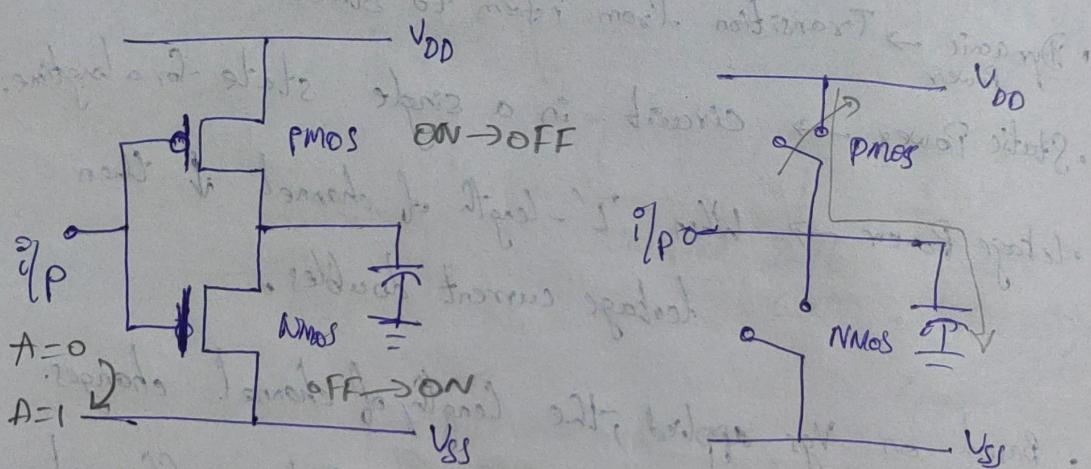


- Substrate terminal comes to picture to avoid reduce body effects and controls leakage currents.

- MOSFET is a 4 terminal device.

Static Power Dissipation :

(CMOS Inverter Logic)



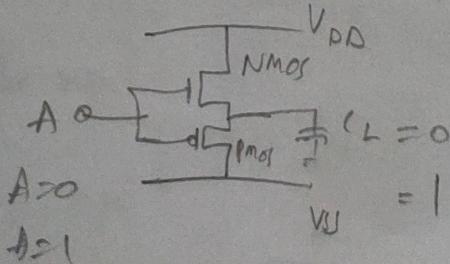
- The power dissipation observed in a circuit, when the circuit operating in a single state continuously is called as Static Power dissipation.

- The power dissipation observed when circuit continuously changing from different states, is called as Dynamic Power Dissipation.

- When Transition of one state to other state

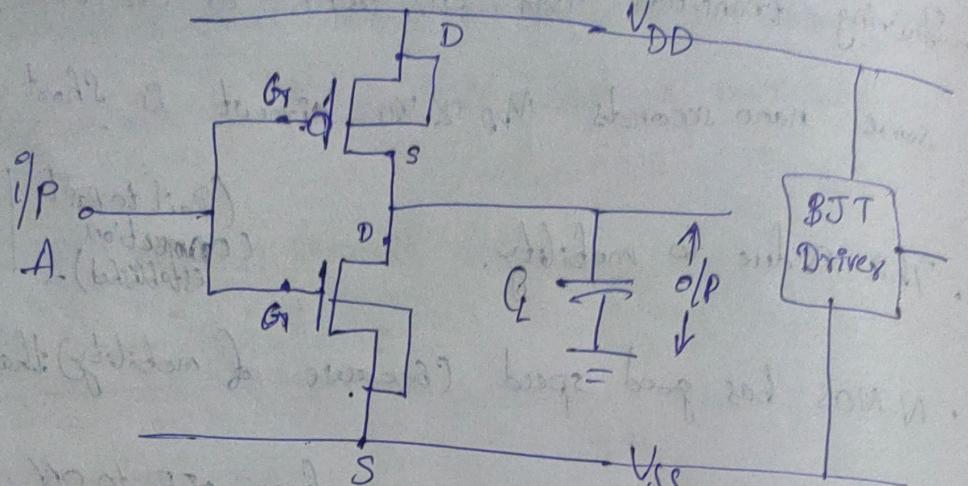
- During transition, from ON to OFF or OFF to ON, for some nano seconds V_{DD} & V_{SS} circuit is short circuited.
- This is due to mobility.
- N-MOS has good speed (because of mobility) than PMOS
- During transition, NMOS goes from OFF to ON, but the PMOS will be in ON state i.e. continuing to come to OFF state.
- Switching characteristics does not match.
- Capacitor charging and discharging does not happen desirably.
- And so, Inverter logic cannot be achieved.
- To avoid this and match the switching characteristics, we need to change the geometry of transistors.
- Design in such a way that both switching characteristics matches.

Aspect ratio: $Z = \frac{W}{L}$



D-Slope?

$A = 0$	$D_1 = 0$
$A = 1$	$D_1 = 1$



- Body effects of Substrate: $V_{BS} > 0$ efficiency

- While fabrication, by proper doping concentration, we can avoid/control the body effects. (at fabrication level)
- By using substrate terminals, we can control body effects in the circuit

In figure, Substrate connected to V_{DD} in Pull-up transistor terminal and substrate terminal connected to V_{SS} in Pull-down transistor and so overall body effect of the circuit is nullified.

- Power dissipated when circuit operated in a single steady state continuously — P_{static} .

o/p of 1 circuit should be given to next circuit as the input, for this Driver circuit is used.

$$\text{CMOS} + \text{BJT} \implies \text{BiCMOS}$$

Logic Design Driver circuit

In BJT, high power dissipation happens

20/01/2023

Implementation of cascode logic for different circuits :

Implementation of any logic using CMOS, then the o/p of the circuit is the complementary function.

Ex: $f = a(b+c)$ - Implement using CMOS logic
 $\rightarrow P' \rightarrow \text{CMOS} \rightarrow f$ (NOT gate)

$a(b+c) \rightarrow \text{CMOS} \rightarrow \overline{(a)(b+c)} \rightarrow \text{Do } a(b+c)$
 \rightarrow But using inverter logic/NOT gate
 after CMOS logic is not suggestible, as →
 (Jitters - noise - transistors)

→ So, apply inverter logic at the input.

Input : $f = \overline{a(b+c)}$

- ↳ Delay increased
- ↳ Burden on power supply P
- ↳ IC area \uparrow
- ↳ No. of Transistor T (as to implement inverter logic $\rightarrow 2$ transistors are required)
- ↳ Power dissipation \uparrow
- ↳ Die size \uparrow

20/01/2023

De Morgan's Law : $\overline{a \cdot b} = \overline{a} + \overline{b}$

$$\overline{a+b} = \overline{a} \cdot \overline{b}$$

Sol: $f = \overline{a(b+c)}$

$$f = \overline{a} + \overline{(b+c)}$$

$$\Rightarrow \boxed{\overline{f} = \overline{a} + \overline{b} \cdot \overline{c}} \rightarrow (\text{MOS} \rightarrow f = a(b+c))$$

Formulae

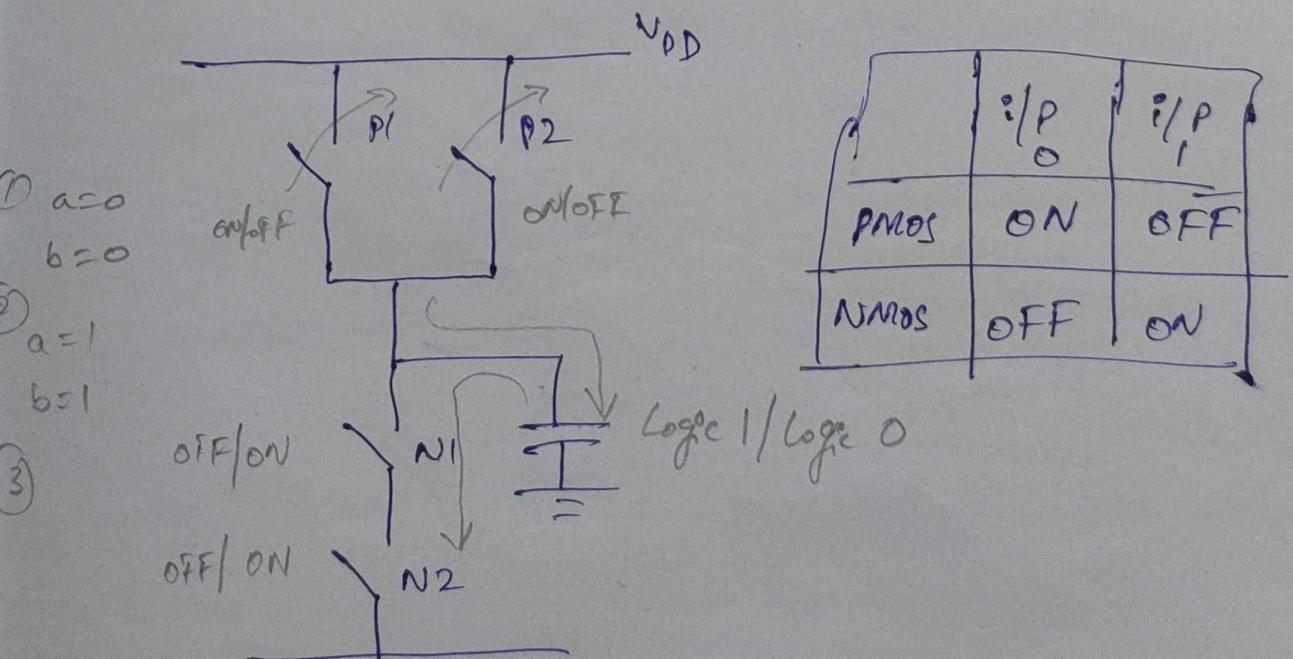
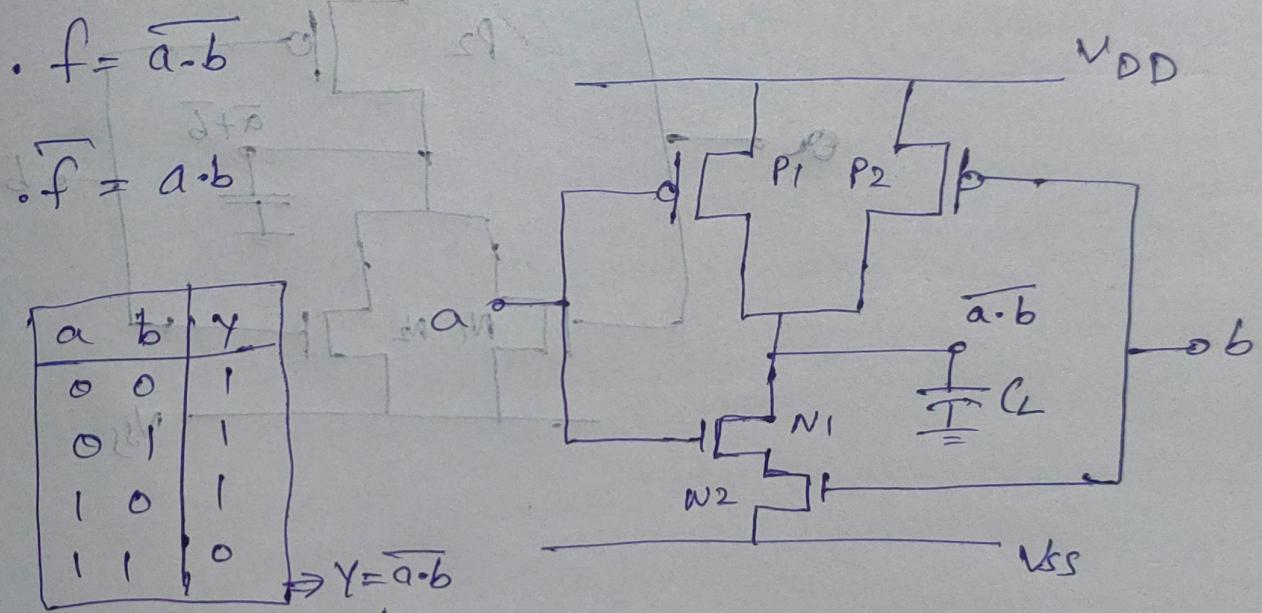
Rule1: If in the given boolean function/ expression, (terms are in) the variables are in product then PMOS transistors should be connected in parallel, and NMOS transistors should be connected in series.

Rule2: If in the given boolean expression, the variables are in summation then, PMOS should be connected in series and NMOS should be connected in parallel.

NOTE: $\star \star \star P - P - P$ (product - PMOS - Parallel)

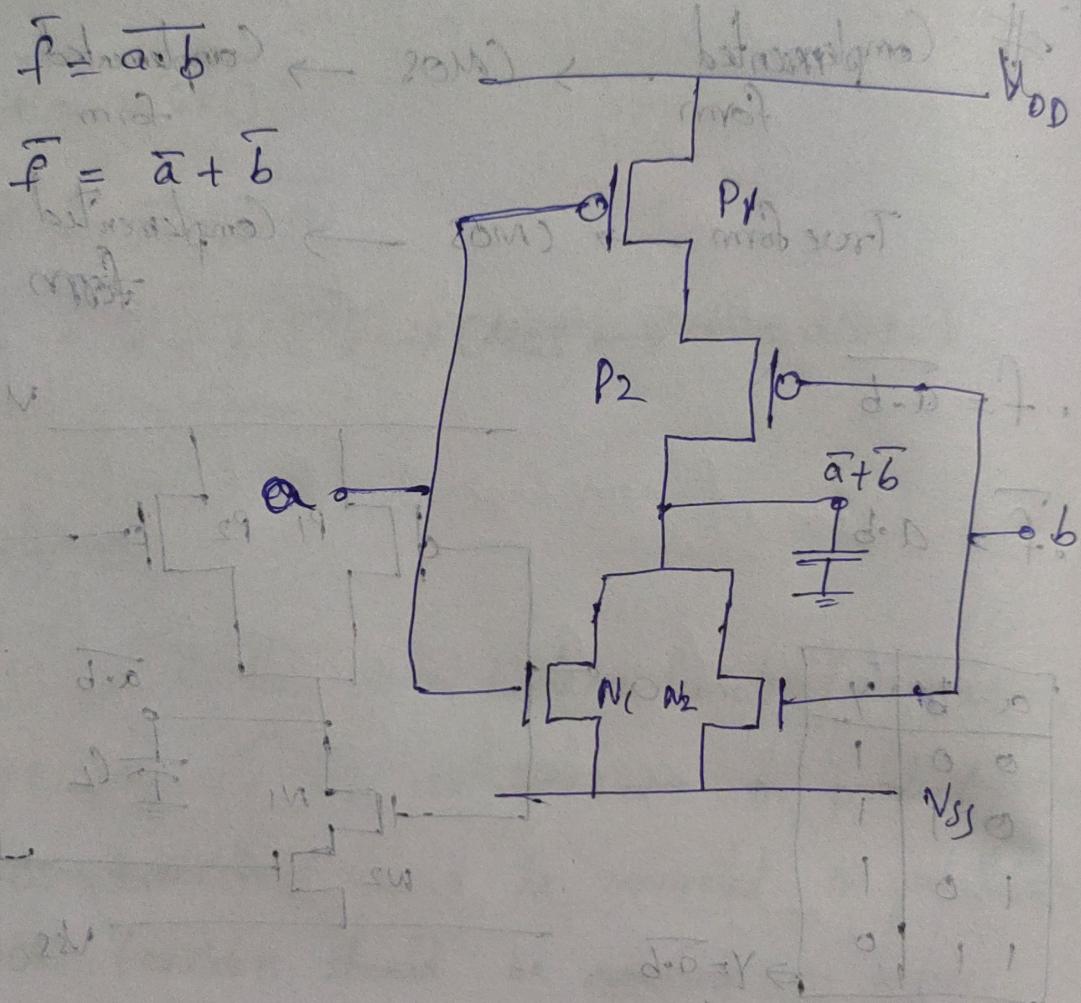
Eg: Implement $f = \overline{a \cdot b}$ (The boolean expression) using CMOS logic.

Sol: # Complemented form \rightarrow CMOS \rightarrow Complemented form
 True form \rightarrow CMOS \rightarrow Complemented form

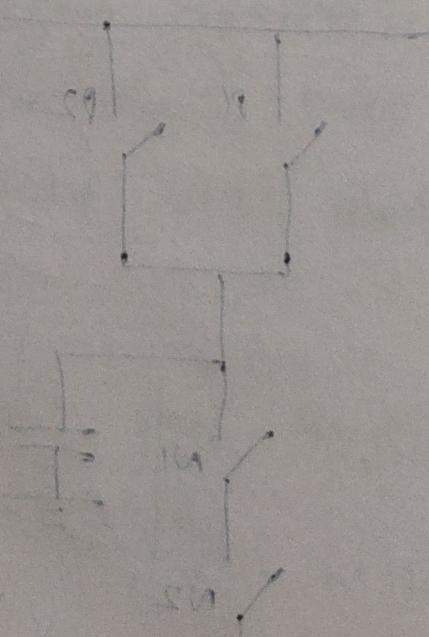


Ex: Implement $f = a \cdot b$ using CMOS Logic

so $f = a \cdot b$ (using De Morgan's Law) (\because it is in true form)



1	1	1
1	0	0
0	1	0



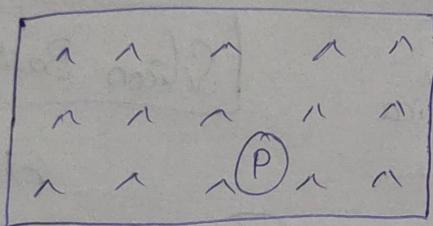
① On nMOS fabrication : p-substrate i.e. dope Si with trivalent elements like B, Al.

→ Pure Silicon chip using PVD or CVD process, it is doped.

→ nMOS has p-type substrate.

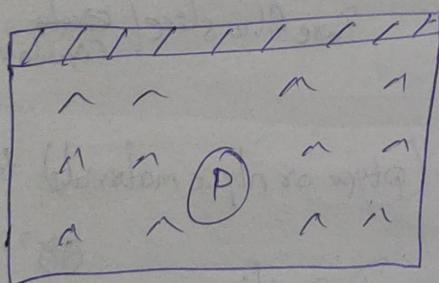
→ p-type : Dope Si chip with trivalent elements like B, Al

Step 1 :



- Pure Si is taken and doped with B/Al using PVD or CVD process.
- p-type substrate formed.

Step 2 :

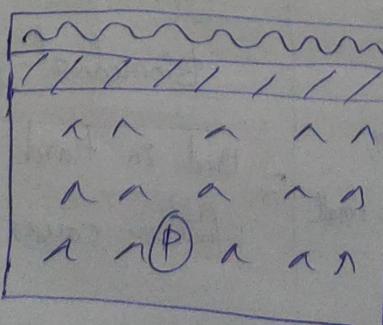


$\rightarrow \text{SiO}_2$ layer is grown deposited over the surface of p-type substrate.

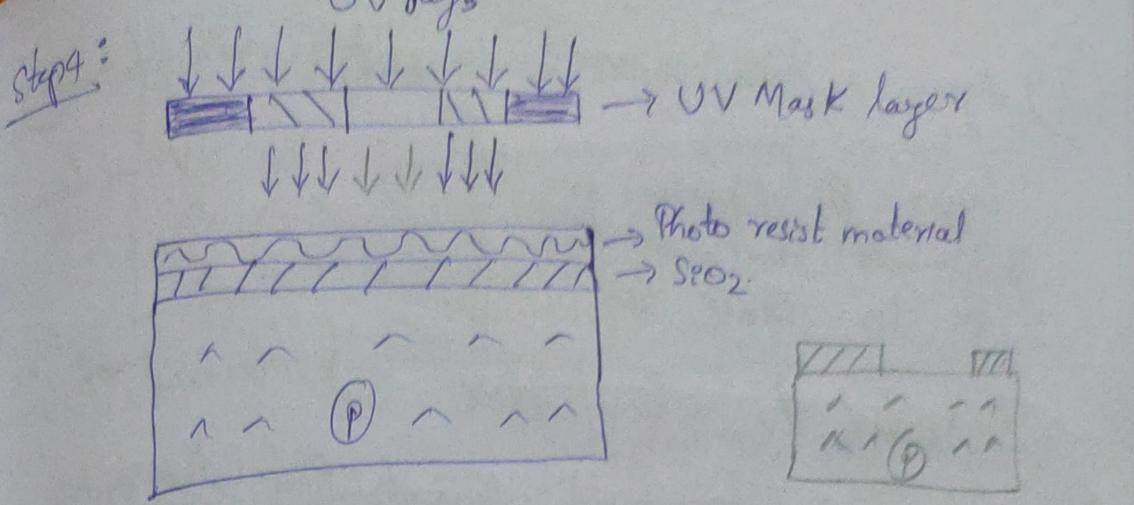
. SiO_2 has crystalline structure.

- Photo resistive material used, as SiO_2 properties may change if direct exposure to UV rays.
- Over the SiO_2 layer, photo resistive material is deposited and then subjected to spinning process.

Step 3 :



→ Photo resist layer
→ SiO_2
- after spinning process, it is uniformly distributed on SiO_2 layer.

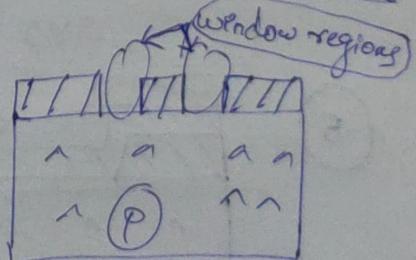


(UV rays are exposed through UV mask layer)

- In order to create ^{define} window regions for source and drain and gate terminal respectively, the p-type substrate is exposed to the UV rays through UV mask layer.
- Once, UV rays are exposed at the defined window regions, SiO_2 layer becomes very hard, then it has been hatched off.
- This complete phenomenon is called "Photo-Lithography process"

• Window region - The space where Drain, Source, Gate need to be created

• Laying a layer on SiO_2 & setup exposed to UV rays through UV mask layer & SiO_2 layer is hatched off
- Photo Lithography Process



⑤ Again a SiO_2 layer is deposited, again photoresist layer is exposed to UV rays via UV mask layer & so gate terminal is achieved

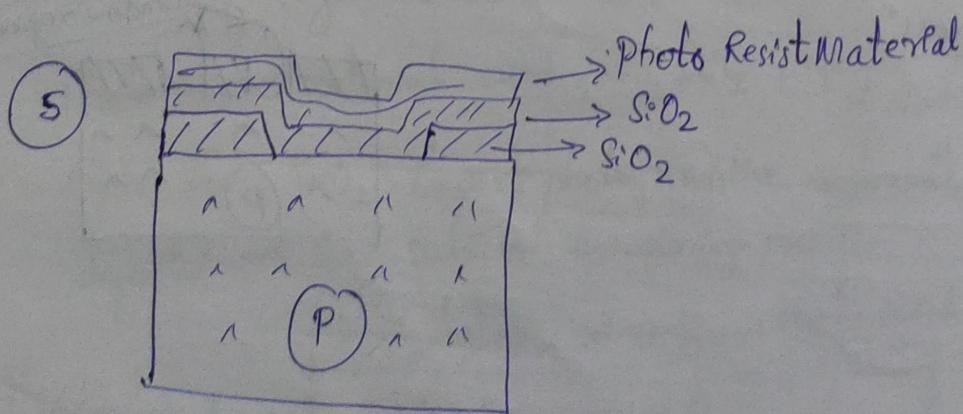
→ In order to achieve define gate terminal, it is again processed through Photolithographic process

⑦ PolySilicon deposited - Photo Lethographic process

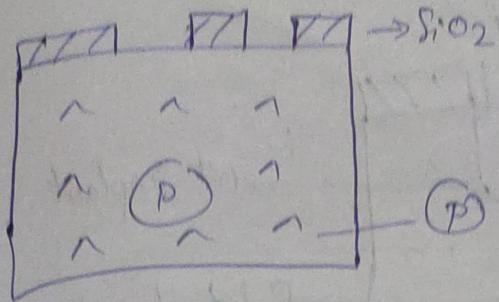
⑧ Poly deposited on gate terminal Region

⑨ n^+ implant, CVD/PVD process is used for n^+ implantation. n^+ implants are diffused

⑩ Al layer deposited over the layer.

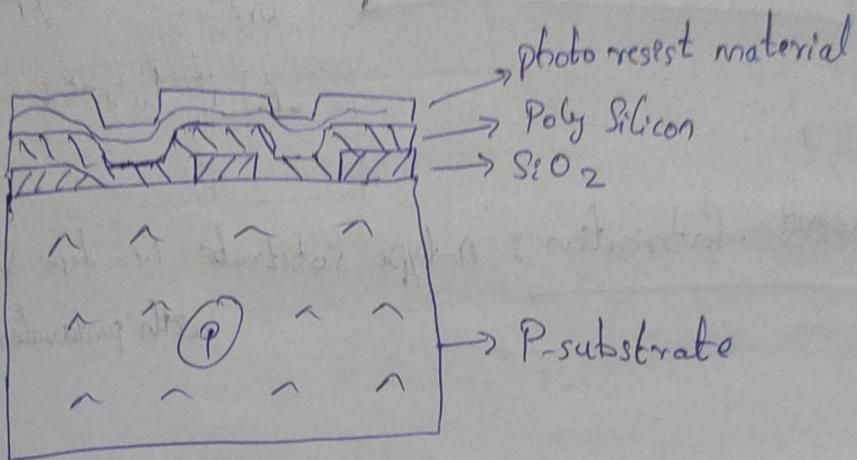


⑥

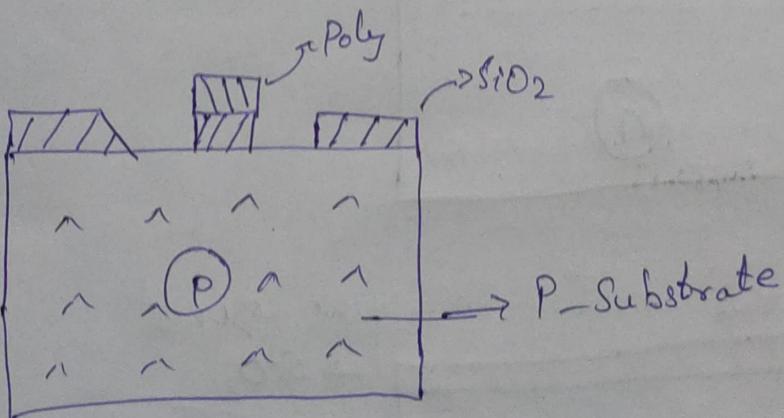


⑥ Substrate / Body / Bulk

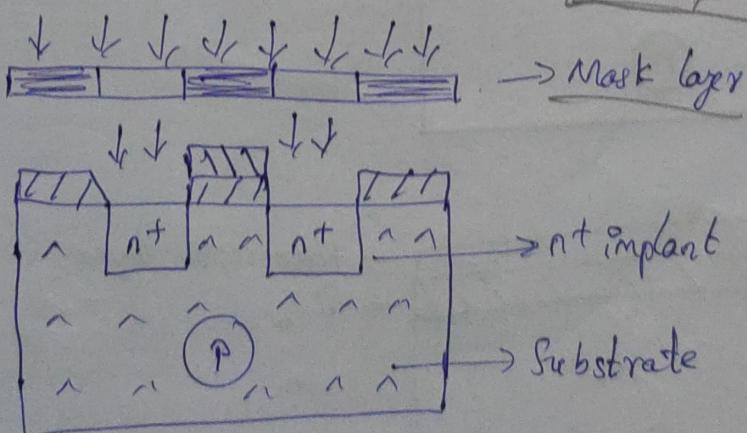
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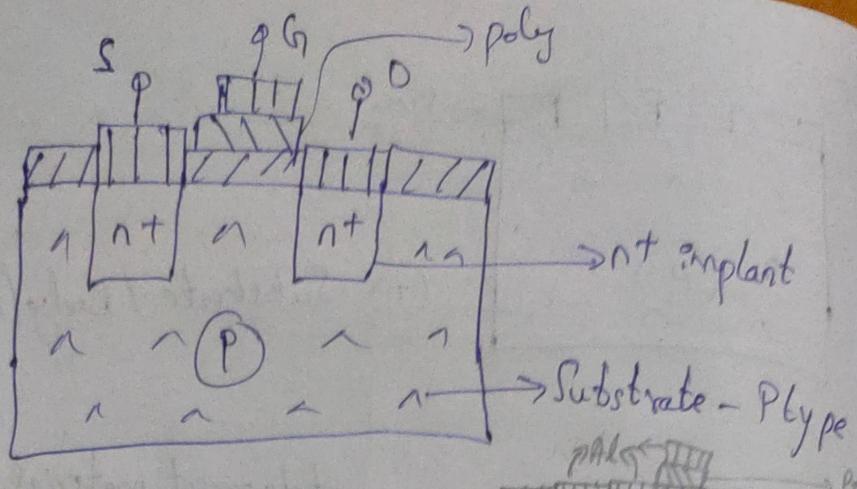
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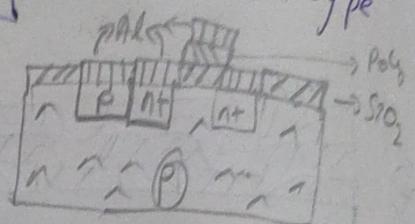
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(10)

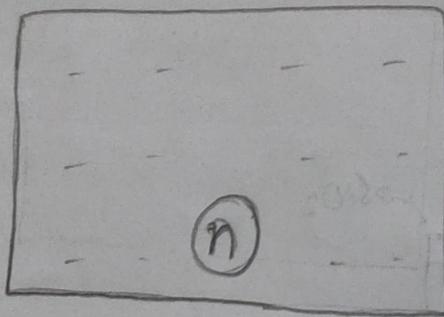


S.S terminal :

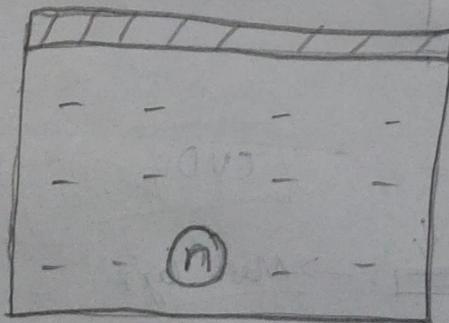


P-MOS fabrication : n-type substrate i.e. dope Si with pentavalent elements

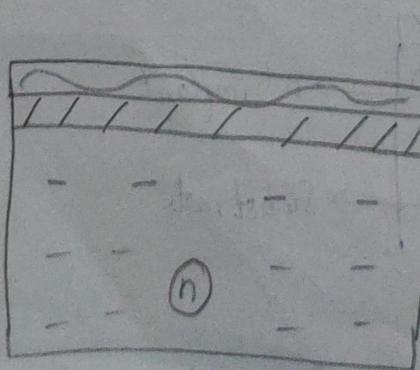
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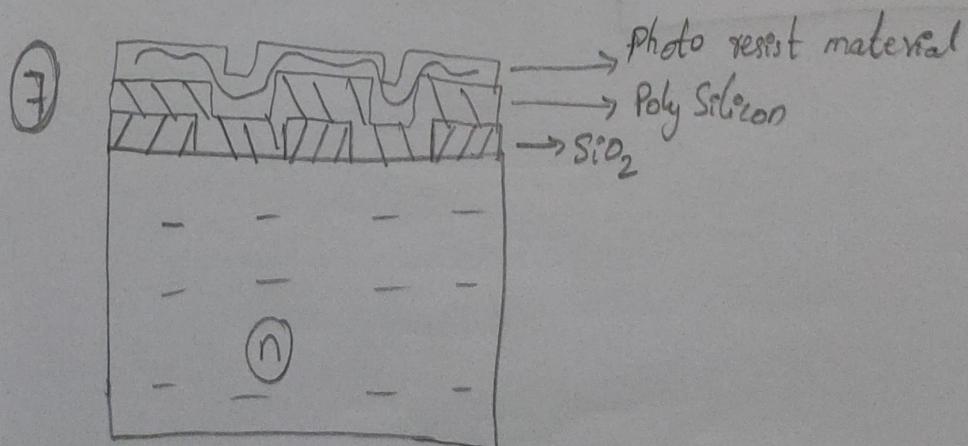
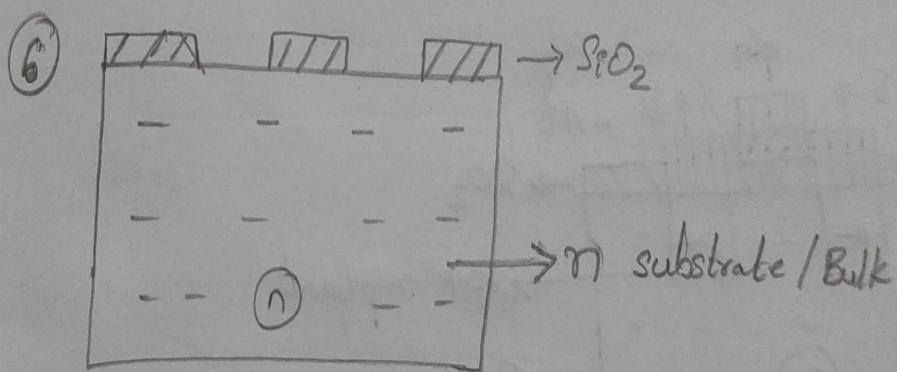
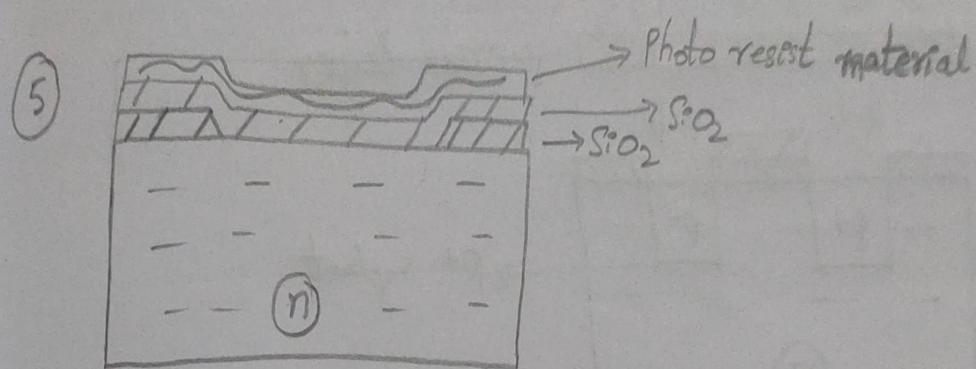
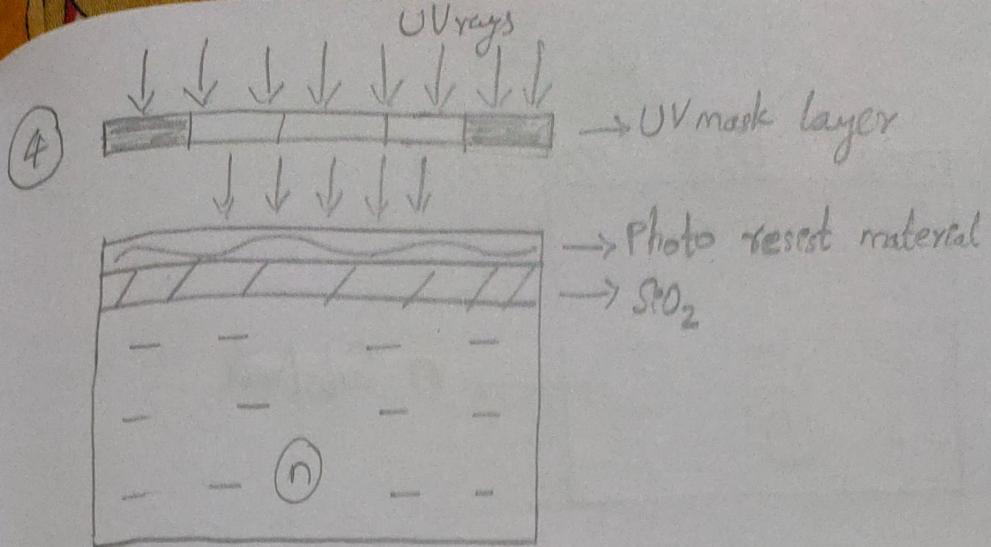


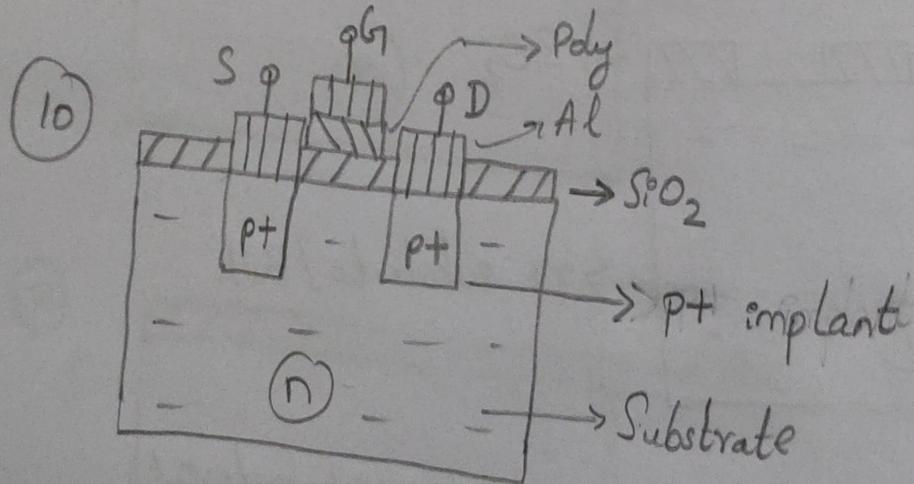
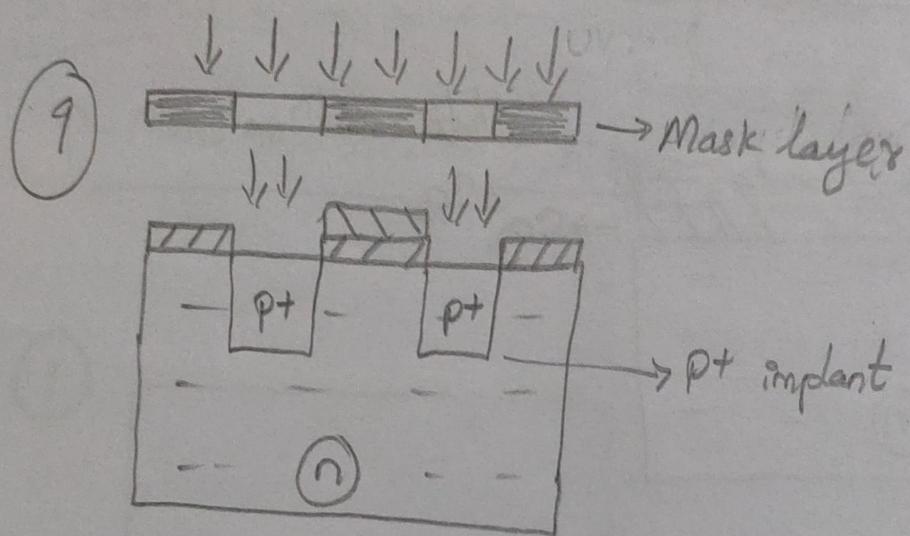
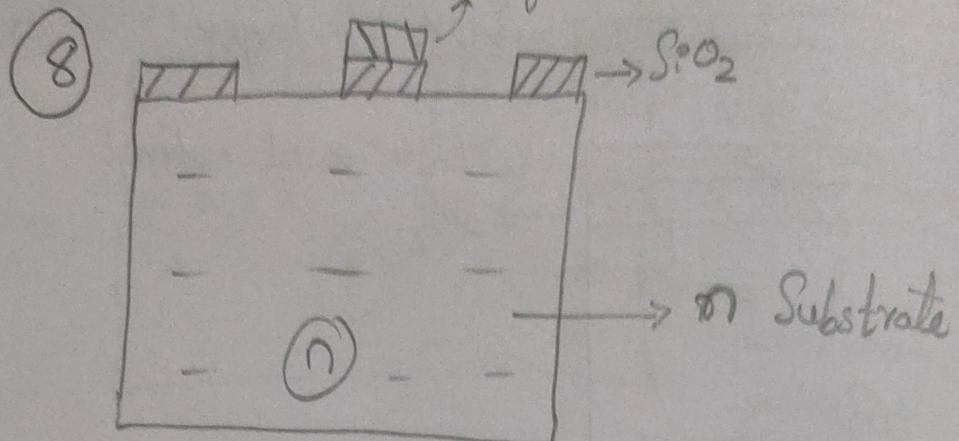
(2)



(3)



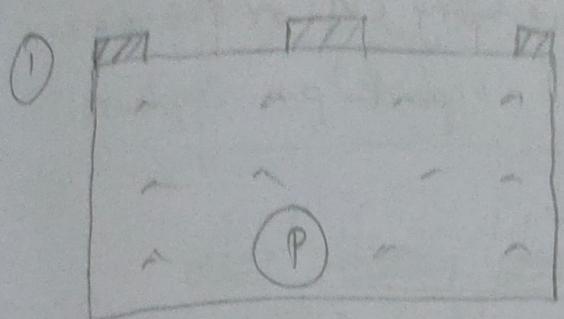




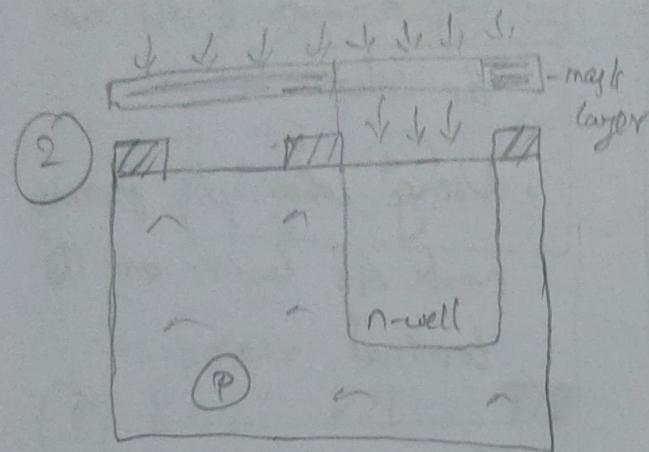
③ CMOS Fabrication process

30/01/2023

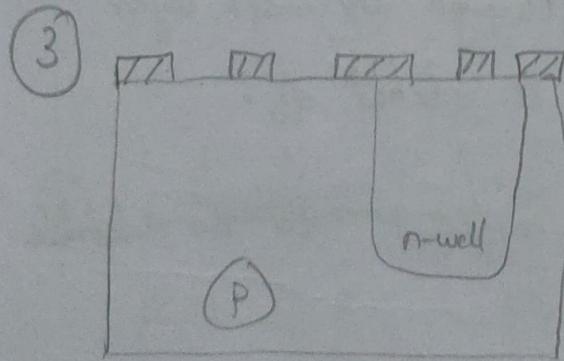
(i) n-well process :



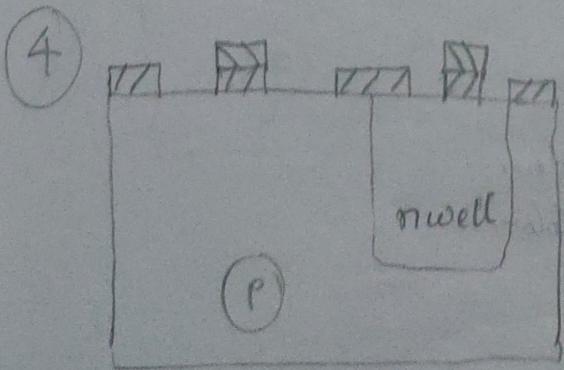
- Take a p-type substrate
- Lay SiO_2 layer over the substrate surface
- Using Photolithography process, create window regions



- Using CVD or PVD process, implant n-well

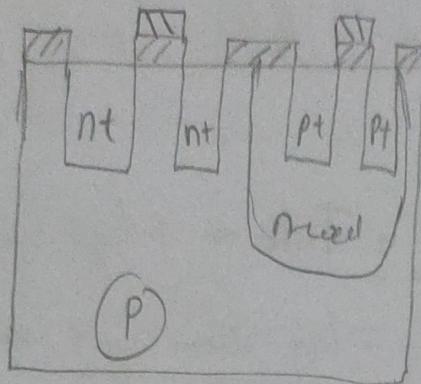


- Lay a layer of SiO_2 over the setup
- Using Photolithography process create gate terminal regions



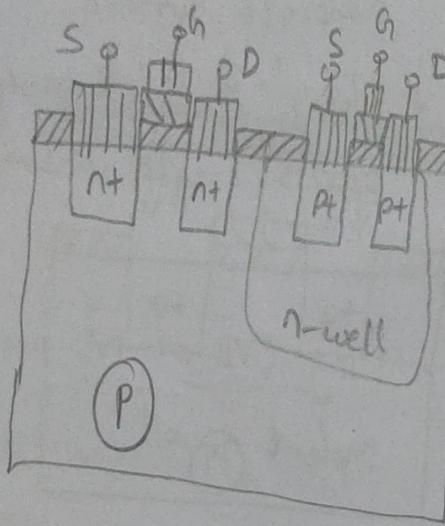
- Lay a layer of poly silicon
- Using photolithography process create poly layer on gate terminal regions

(5)



- Using CVD or PVD process implant n+ implants
- Using CVD or PVD process implant pt implants

(6)



- Lay a layer of Al over the setup
- Using ^{photo} Lethography process, create Al layers over the terminal regions.

→ Lethography process: Laying a layer & exposing the setup to UV rays, through UV mask layer and the unnecessary layer is etched off.

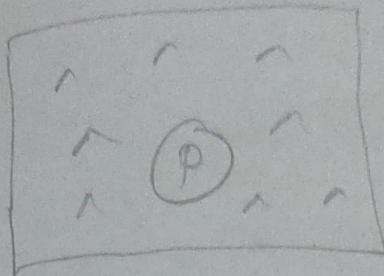
→ CVD process: n+/pt implants implanted into the substrate via mask layer

• 2 Types of SiO_2 Thin ($0.1 \mu\text{m}$)
 Thick ($10 \mu\text{m}$)

• 2 Types of Poly Silicon - I - Red colour
 - II - Orange colour

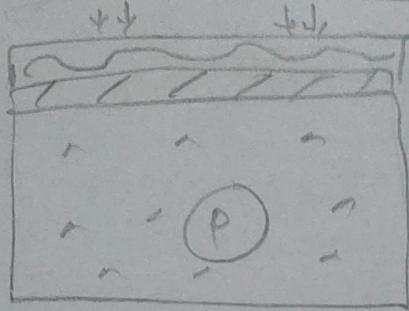
N-well process

(1)

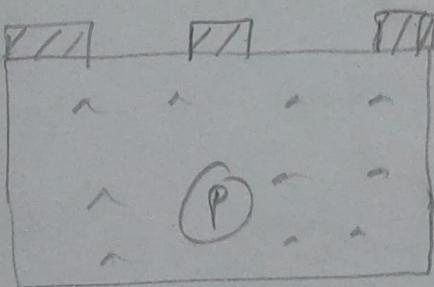


UV-ray

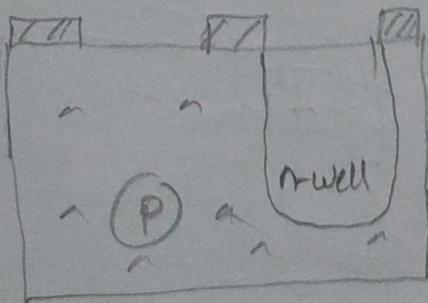
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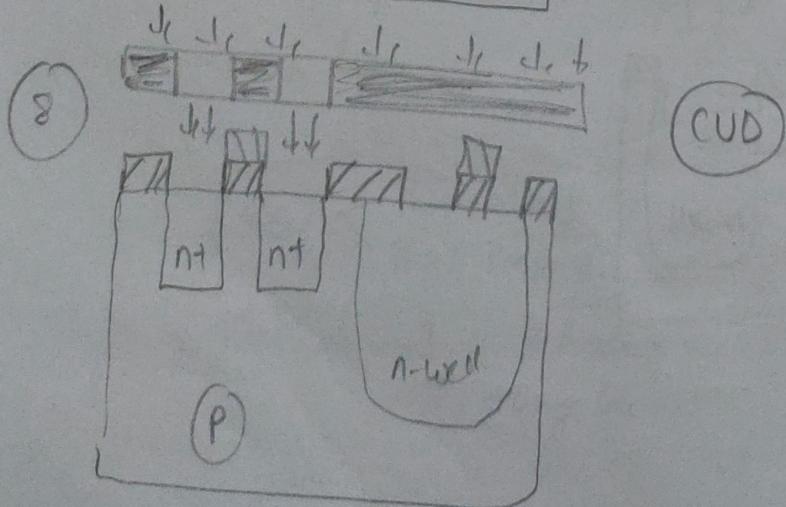
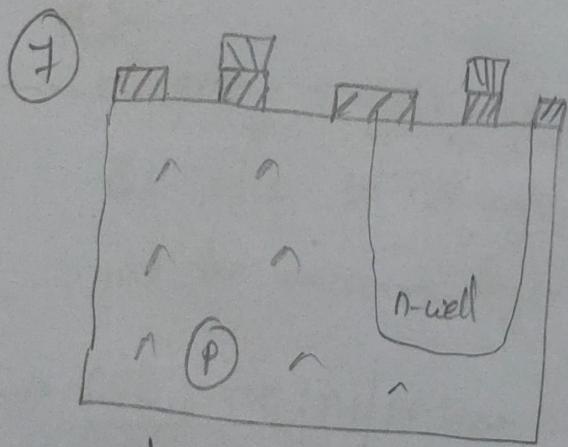
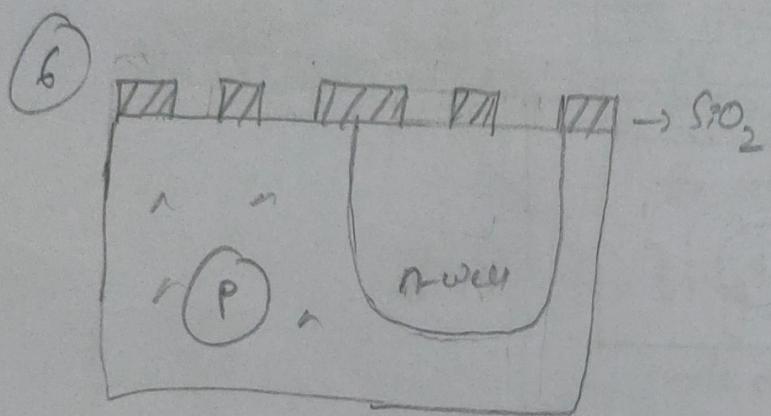
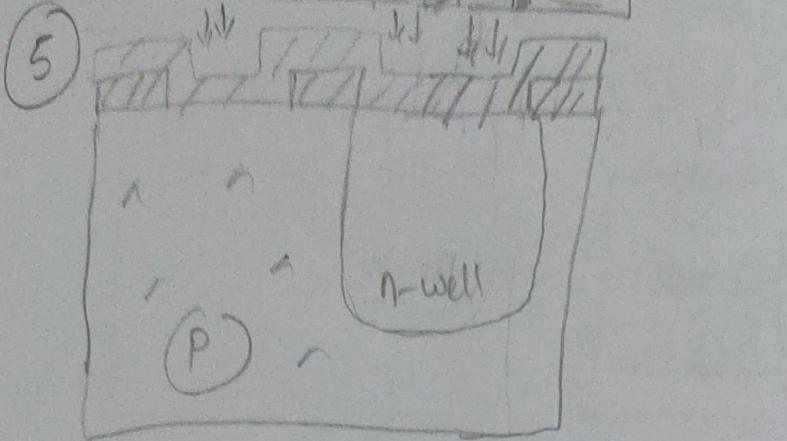


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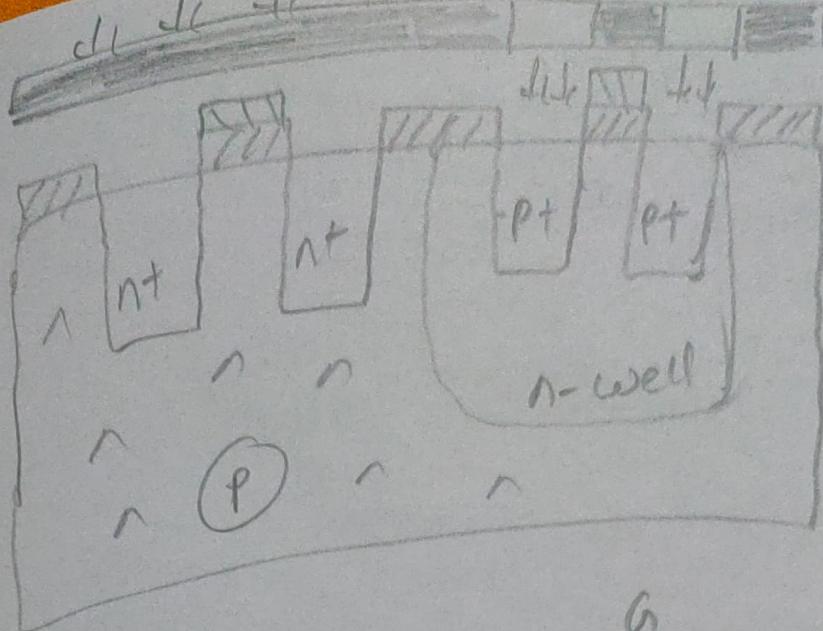


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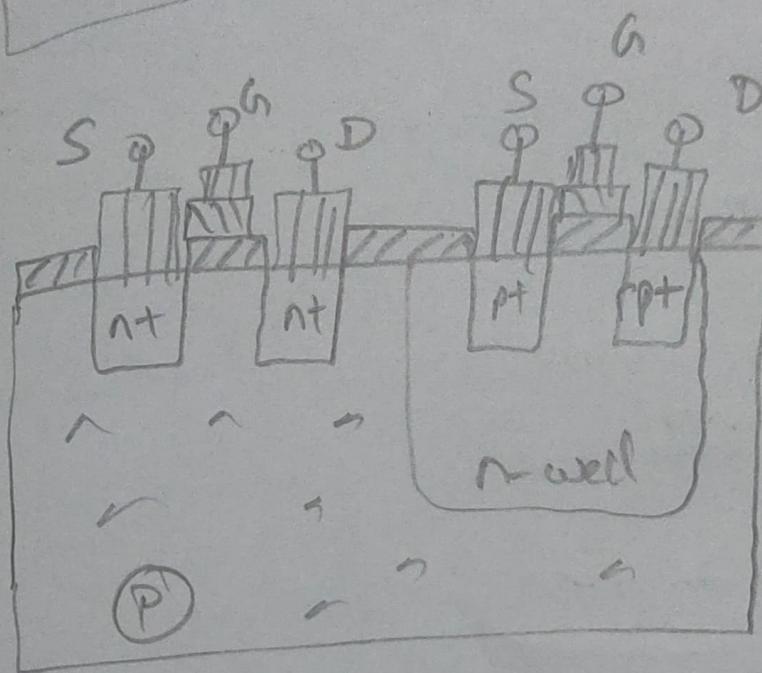


⑨

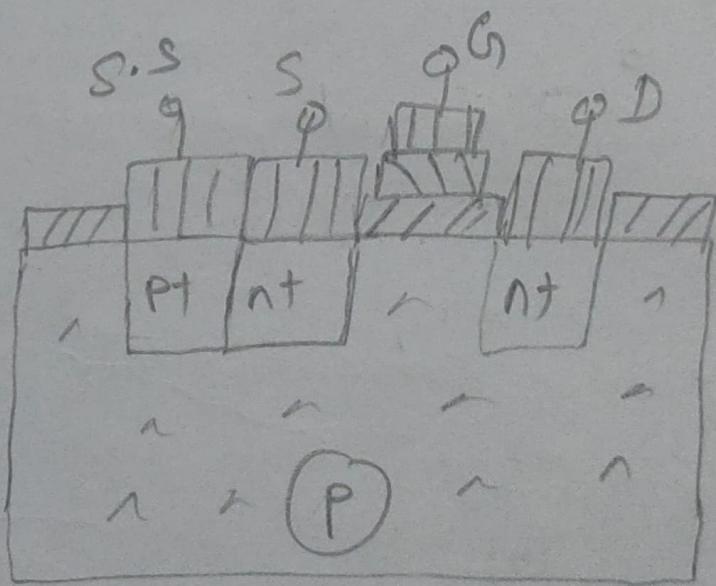


CVD

⑩

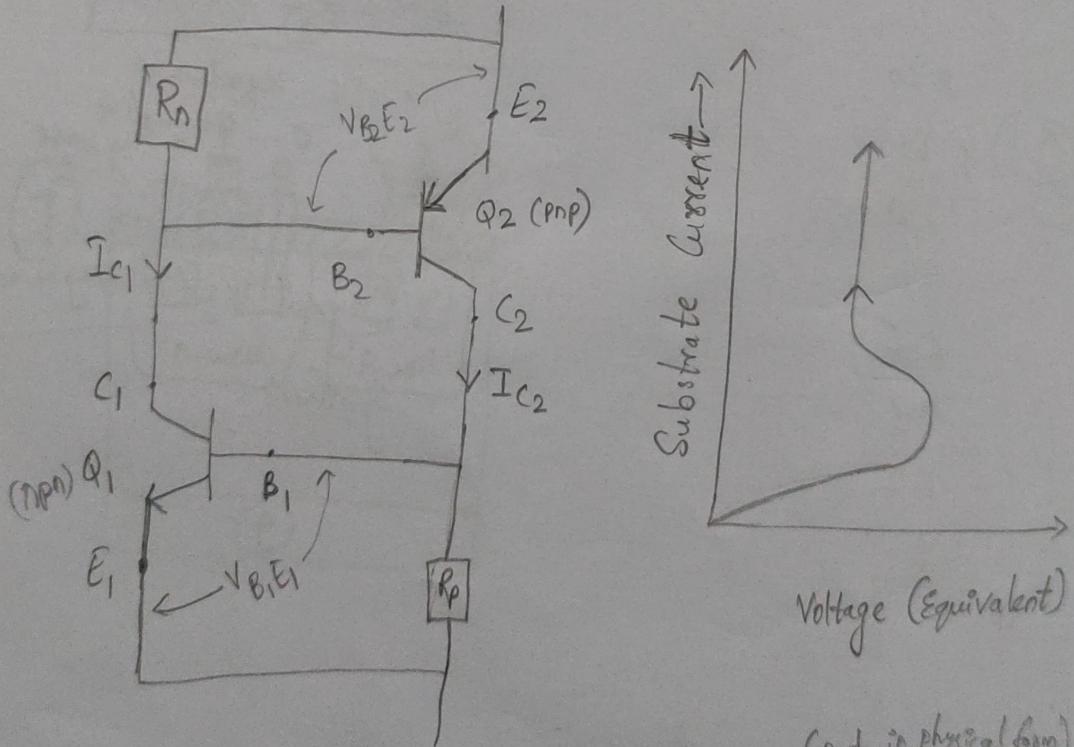
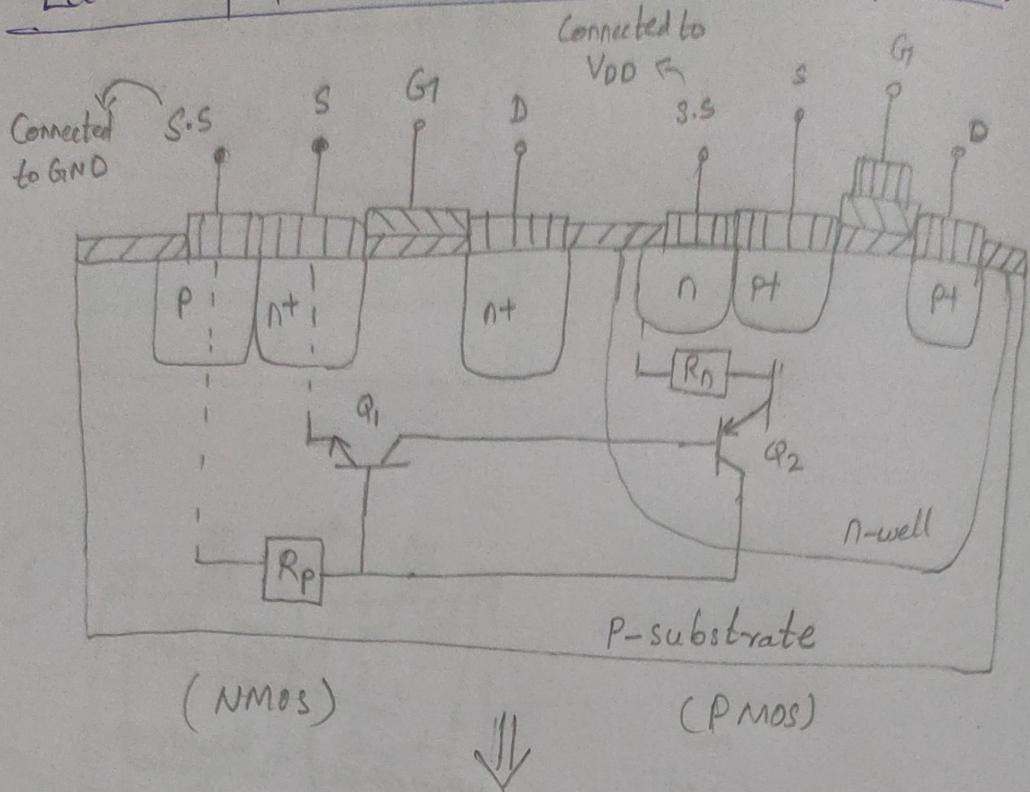


(NMOS -



- We come across with latch-up problem in case of n-well & p-well process.
- n-type & p-type implants in n-well or p-well process has a virtue of formation of npn & pnp BJT transistors.
- A closed path observed.
- If one transistor starts triggering, it triggers the other transistor.
- Transistor-2 comes to ON state, it again triggers Transistor-1.
- Transistor-1 comes to saturation state and triggers Transistor-2.
- Transistor-1 & 2 in saturation state, & so leads to damage of IC.
- This Latch-up problem is overcome in Twin-Tub process.
- Using Isolation Technique, virtual transistor formation is avoided, this is achieved by using Epitaxial layer
Crystalline SiO₂

Latch-up problem in CMOS fabrication process.

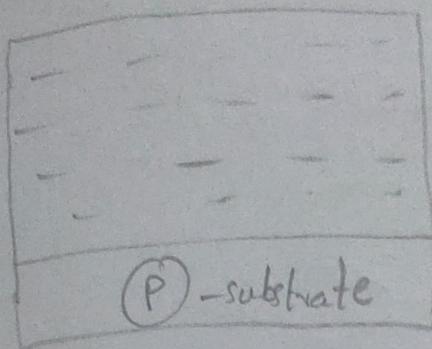


- R_p - Equivalent resistance in p-substrate } (not in physical form)
- R_n - Equivalent resistance in n-well } formed at the fabrication level

↳ depends on doping conc. & depth of implants
↳ litho

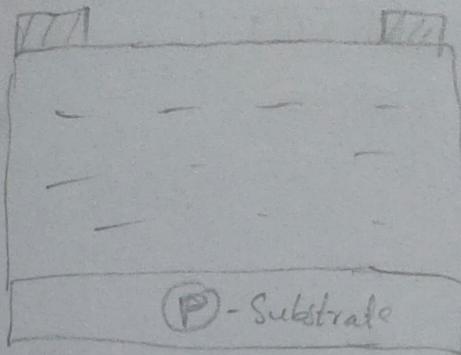
Twin-Tub process

①

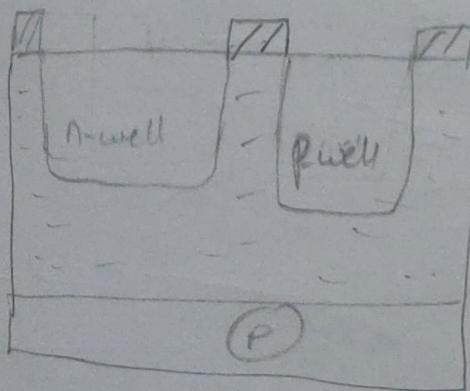


→ 75% of p-substrate
is grown with a
Epitaxial layer.
↳ (Has neither +ve nor -ve
potential)

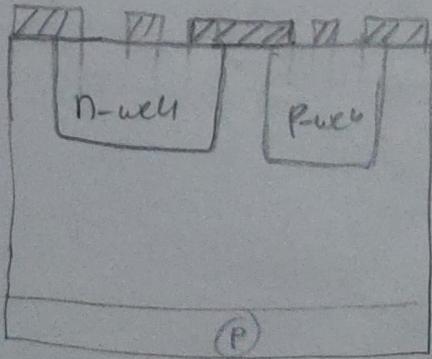
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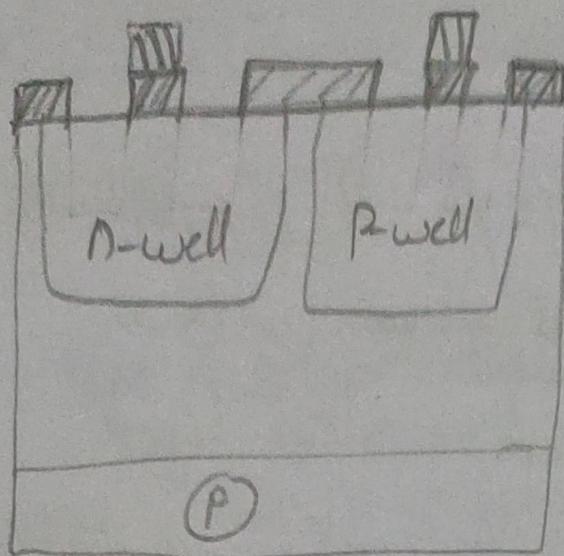
③



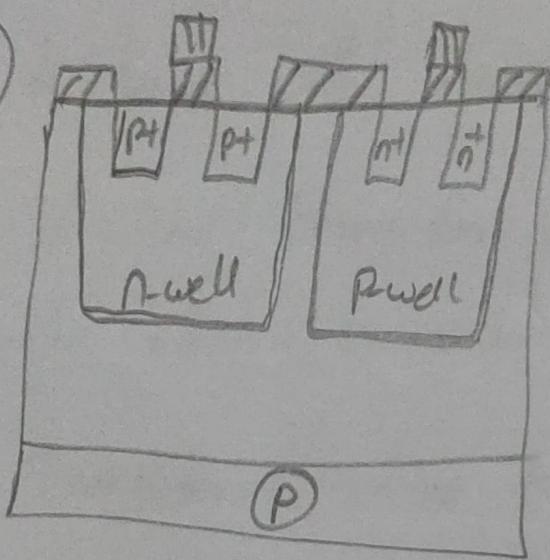
④



(5)



(6)



(7)

