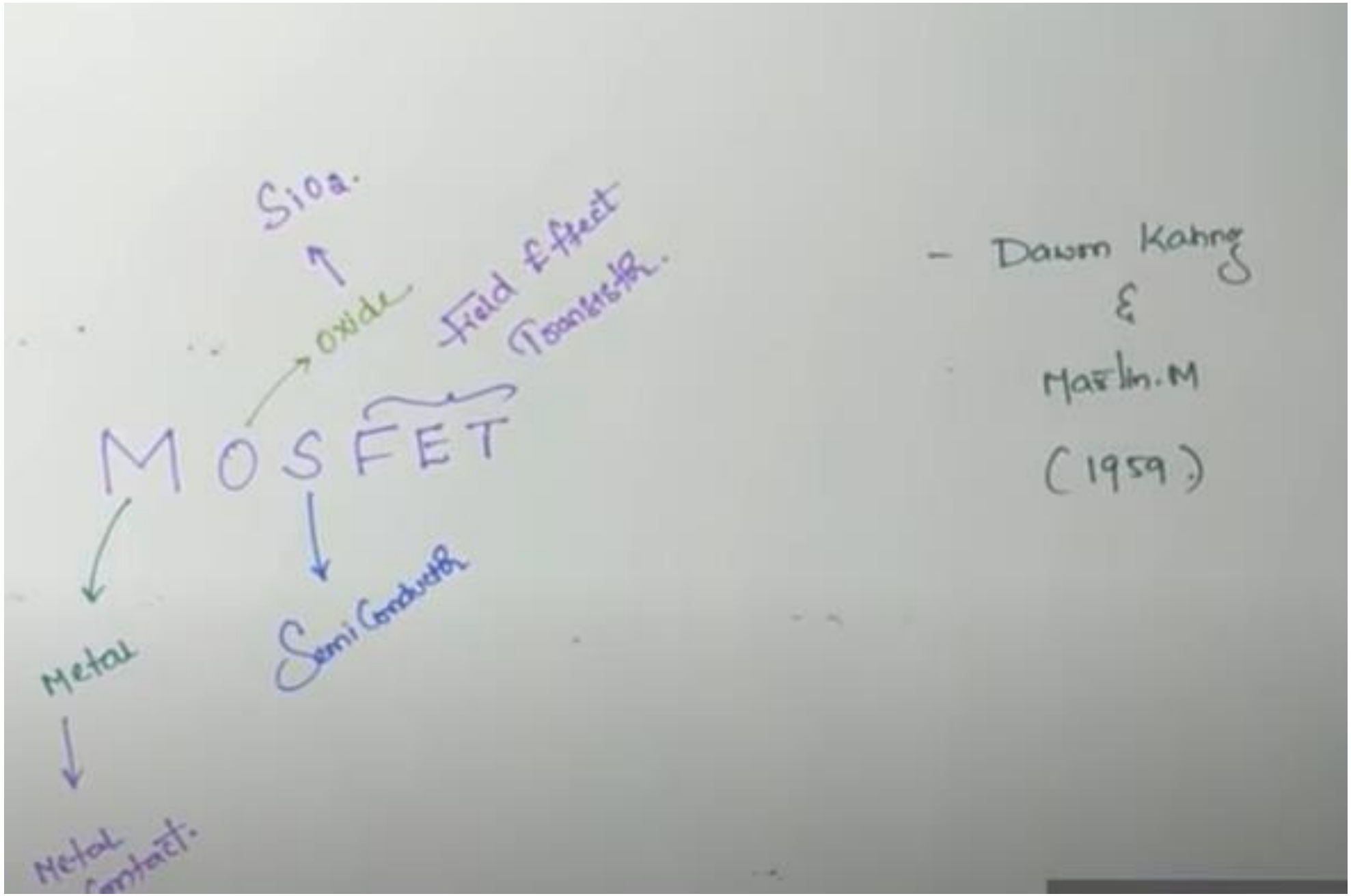
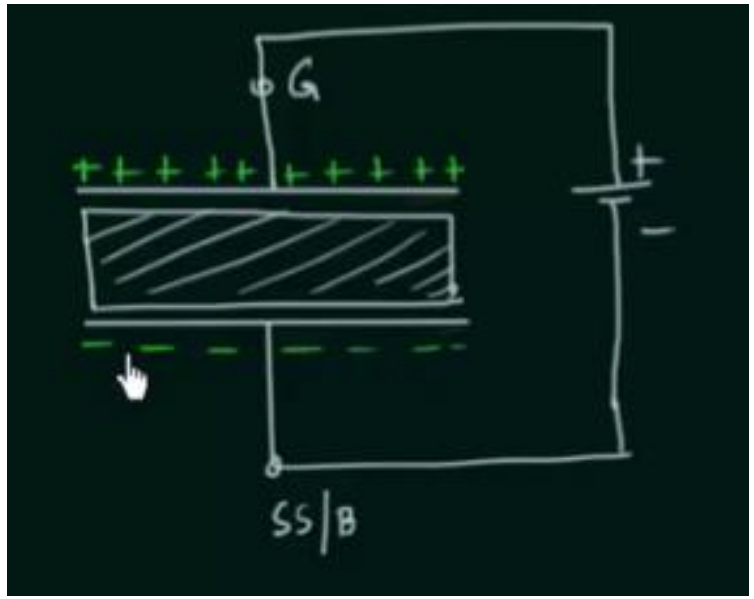

SiO2.
oxide
Field Effect Transistor.
MOSFET
Metal
Semiconductor
Metal contact.
- Dawon Kahng
&
Martin. M
(1959.)

1) Depletion – type → n-ch.
Ch. ν D & S → p-ch.

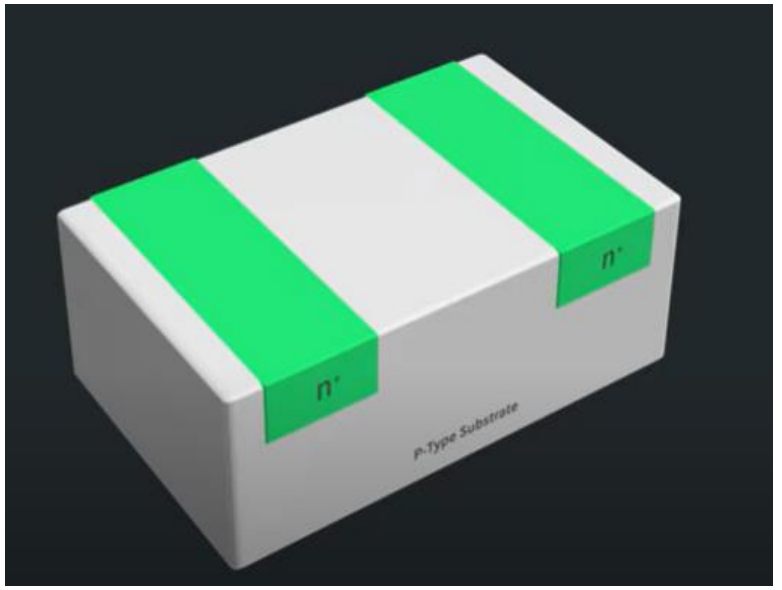
2) Enhancement – type → n-ch.
→ p-ch.

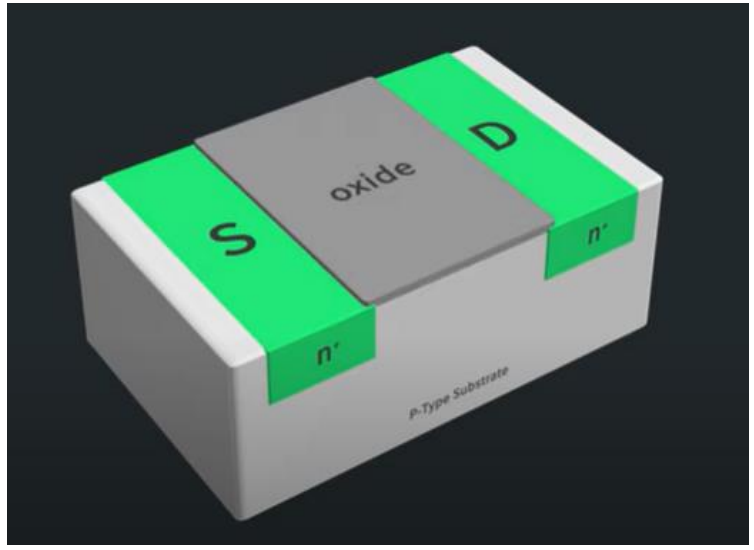
Ch. X D & S

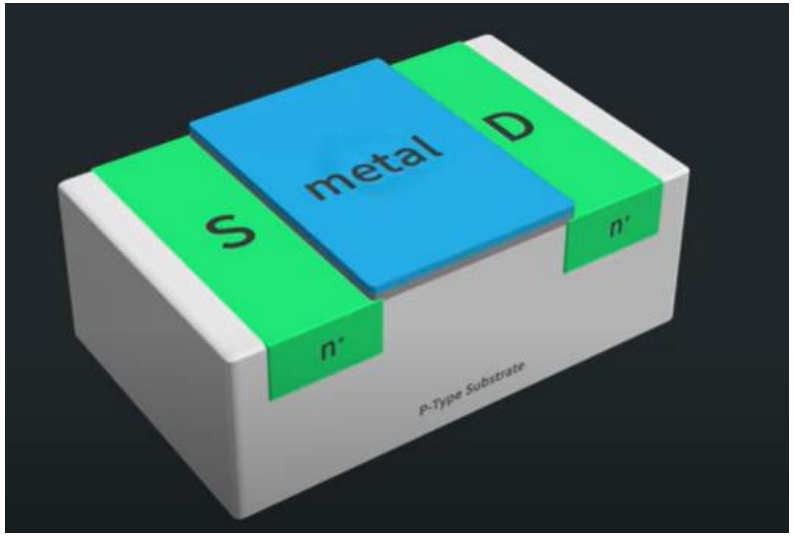
Substrate / body (P)

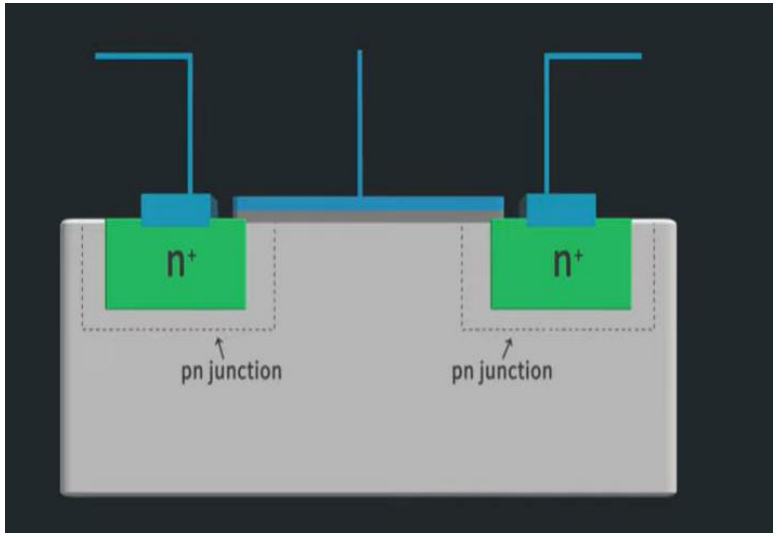

G
+
−
SS/B


P-Type Substrate


n+
n+
P-Type Substrate


S
oxide
D
n+
n+
P-Type Substrate


S
metal
D
n+
n+
P-Type Substrate


n+
n+
pn junction
pn junction

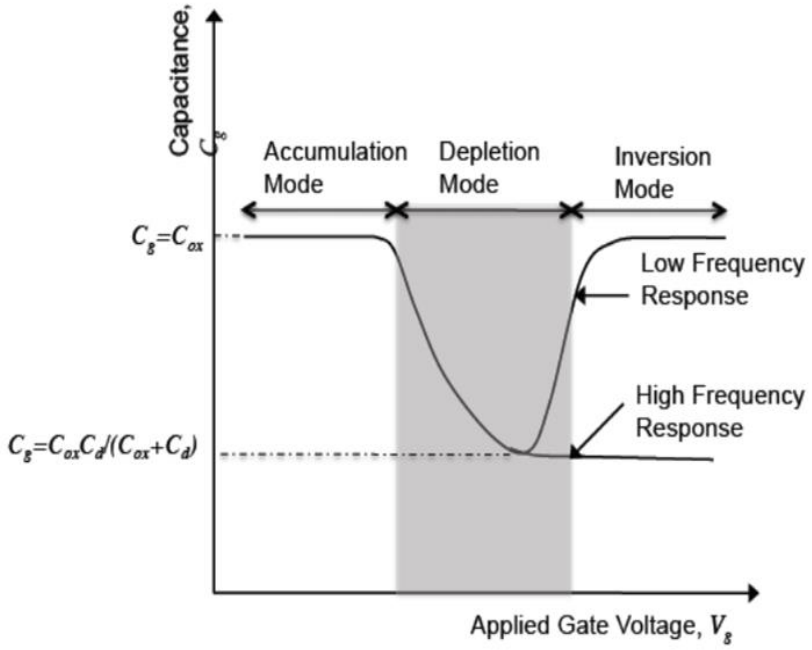
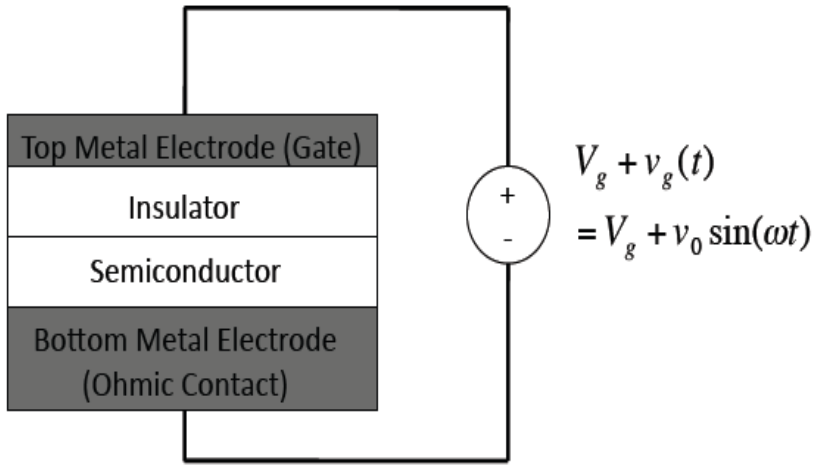


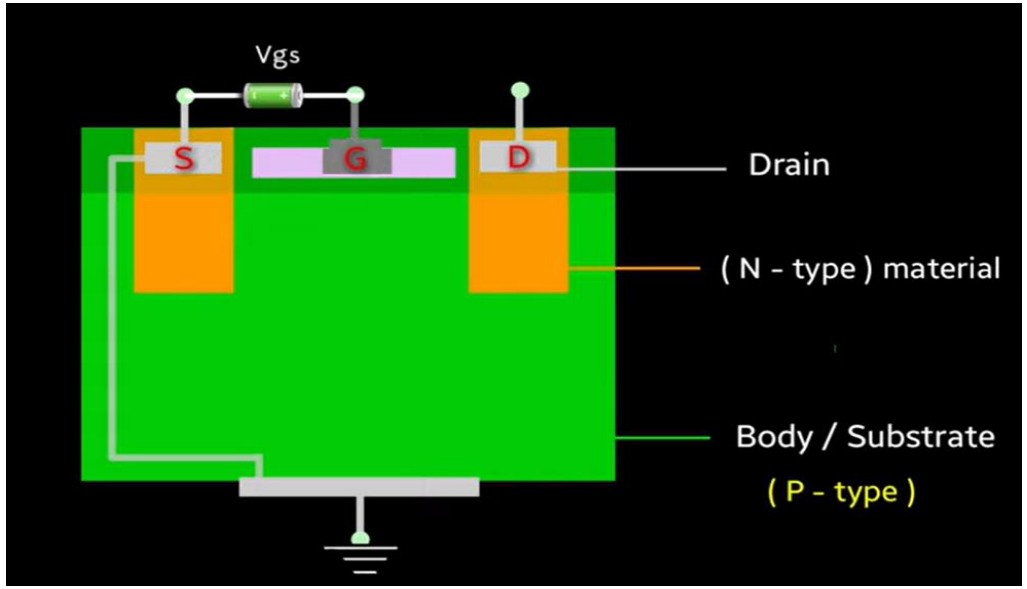
FIGURE 2.10
Capacitance-Voltage (CV) characteristics of a MOS capacitor with a p-type substrate.

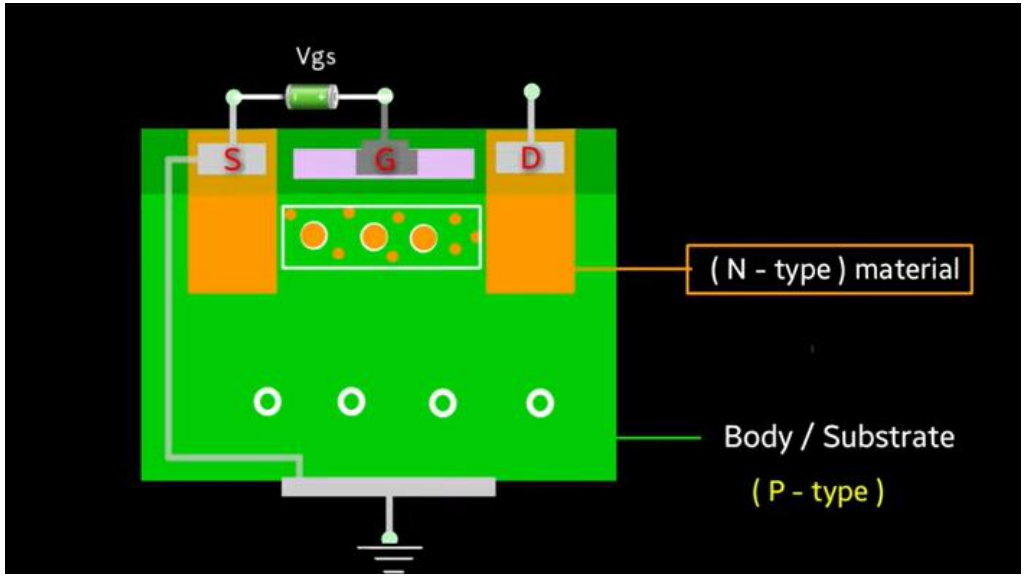


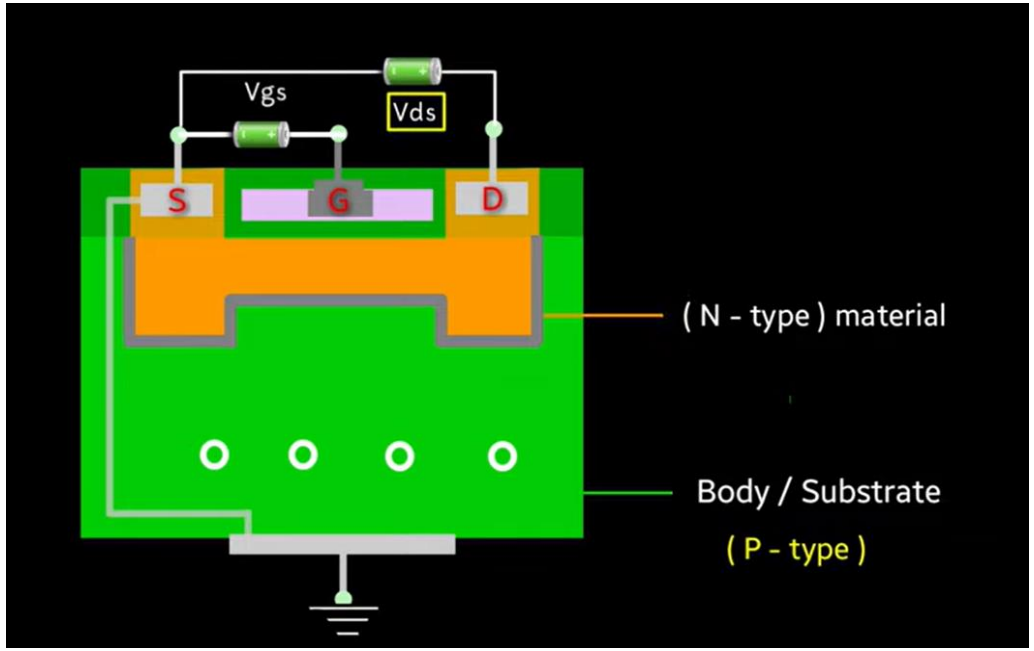
When Vg is lowered signicantly below Vfb, the gate electrode is negative with respect to ground, and holes in the semiconductor accumulate at the semiconductor-insulator interface. This is called the **accumulation mode of operation.**

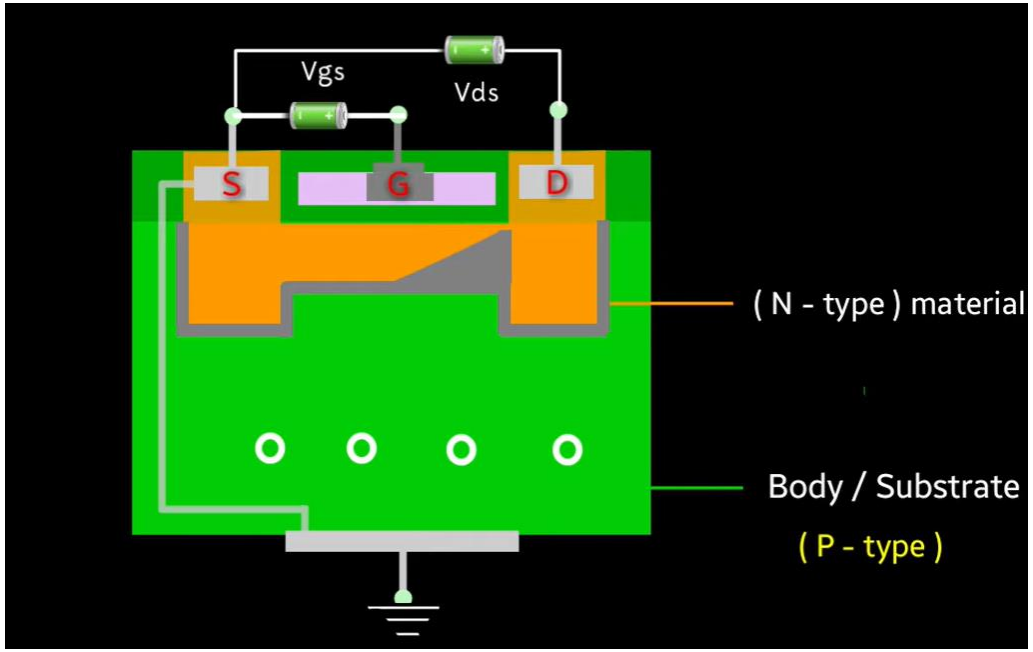
If the acceptor ion concentration is NA per unit volume, the band bending in the semiconductor depletes the semiconductor-insulator interface of any free carriers to a distance xd. The only free carriers present in this depletion region is due to the thermal generation of electron-hole pairs within the region. This is called the **depletion mode of operation.**

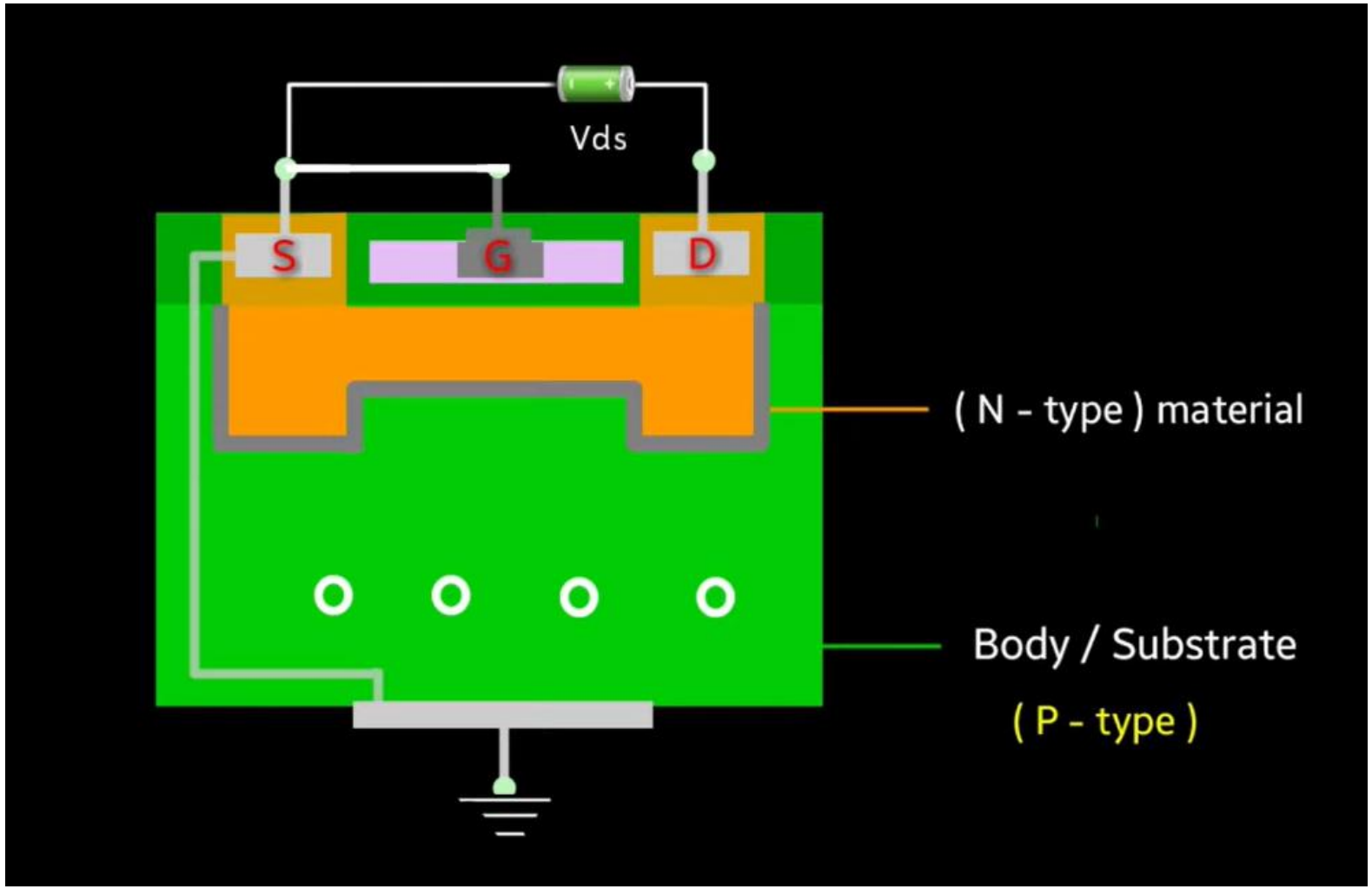
As V_g is increased further, the band bending at the semiconductor-insulator interface becomes so steep (implying the electric eld is so strong) that the electrons begin to accumulate at the surface. Since the channel now contains carriers of the opposite type as compared to the accumulation mode of operation, this is called **the inversion mode of operation.**


Vgs
S
G
D
Drain
(N - type) material
Body / Substrate
(P - type)


Vgs
S
G
D
(N - type) material
Body / Substrate
(P - type)

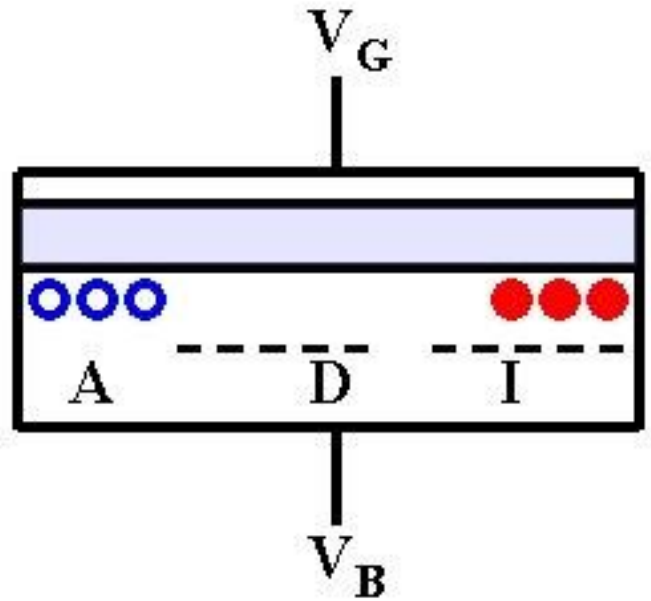

Vgs
Vds
S
G
D
(N - type) material
Body / Substrate
(P - type)


Vgs
Vds
S
G
D
(N - type) material
Body / Substrate
(P - type)


Vds
S
G
D
(N - type) material
Body / Substrate
(P - type)

MOS Transistor Basics
Two Terminal Structure

Two terminal structure (p-substrate): The MOS capacitor



- **Important derived parameters. With $V_G = V_B = 0$:**
  - ϕ_F – **Buck Fermi Potential** (Substrate)
  - ϕ_S – **Surface Potential** (Substrate)

MOS Transistor Basics
Two Terminal Structure (Continued)

- V_{FB} – **Flat Band Voltage** (applied external voltage to G-B to flatten bands of substrate – equal to built-in potential difference of MOS – equal to **work function difference** ϕ_{GB} between the substrate (channel) and gate.

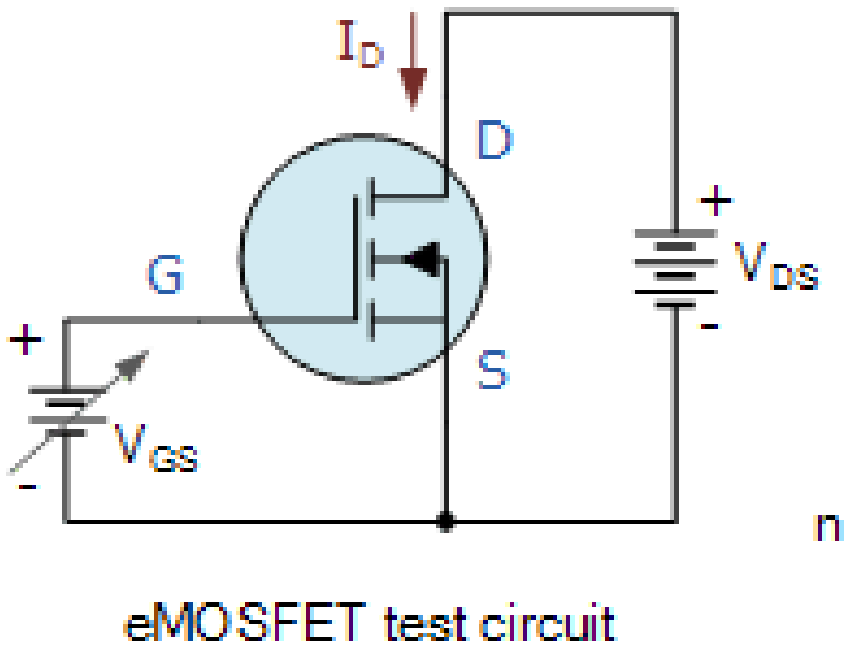
- **Operation**

  With $V_G<0$, $V_B=0$, Accumulation – Holes accumulate at substrate-oxide interface due to attraction of negative bias

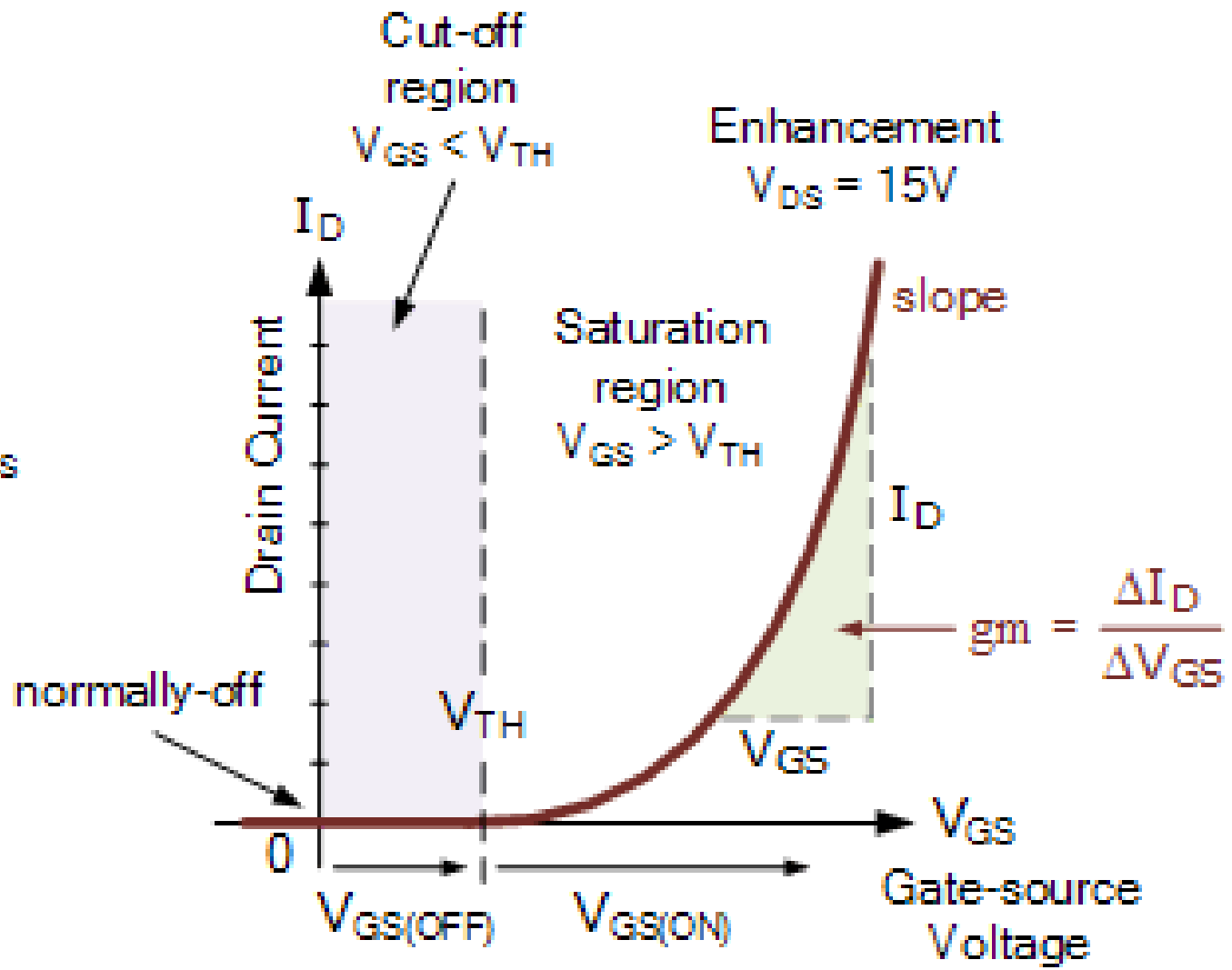
  With $V_G>0$, but small, $V_B=0$, Depletion – Holes repelled from substrate-oxide interface due to positive bias leaving negatively charged fixed acceptors ions behind. The result is a region below the interface that is depleted of mobile carriers.

- **Depletion region thickness**

$$x_d = \sqrt{\frac{2\varepsilon_{Si}\left|\phi_s - \phi_F\right|}{q N_A}}$$

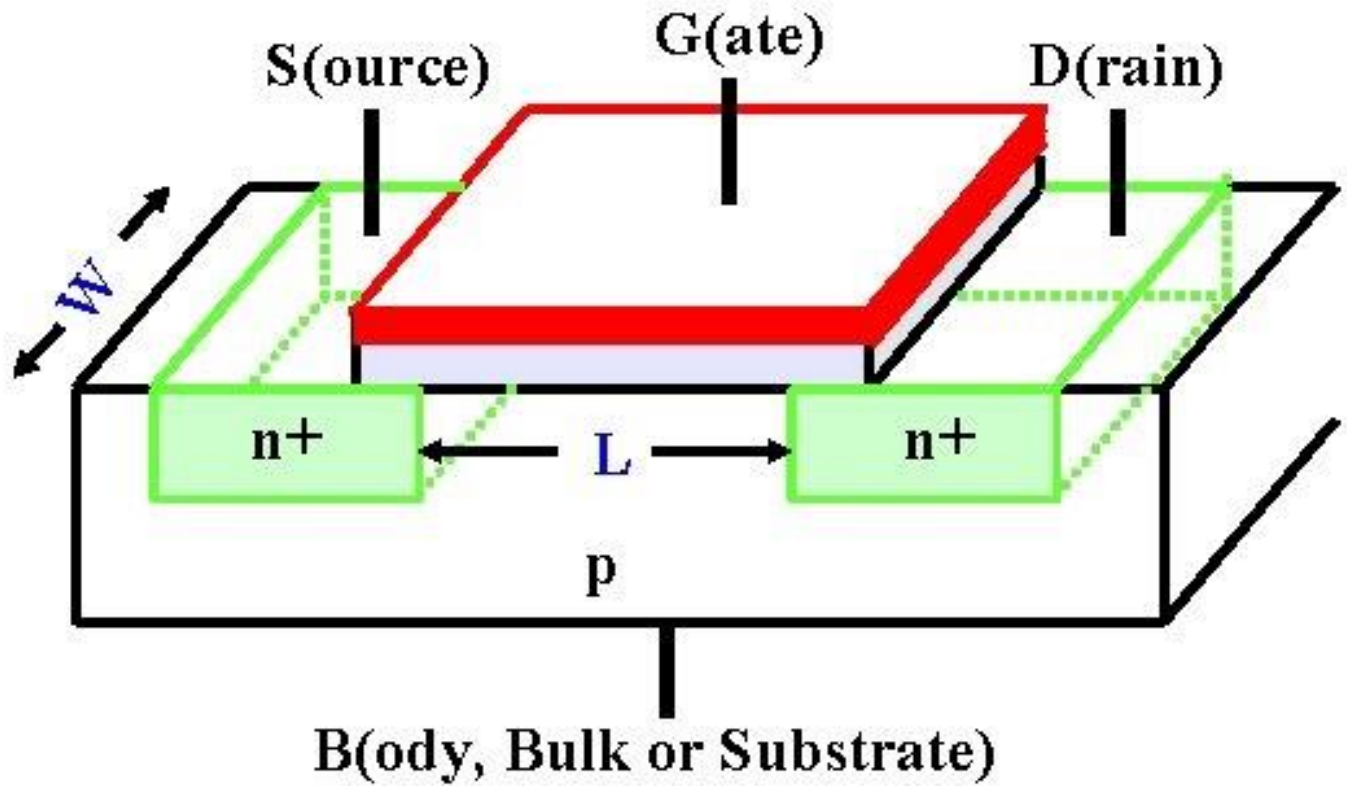


eMOSFET test circuit



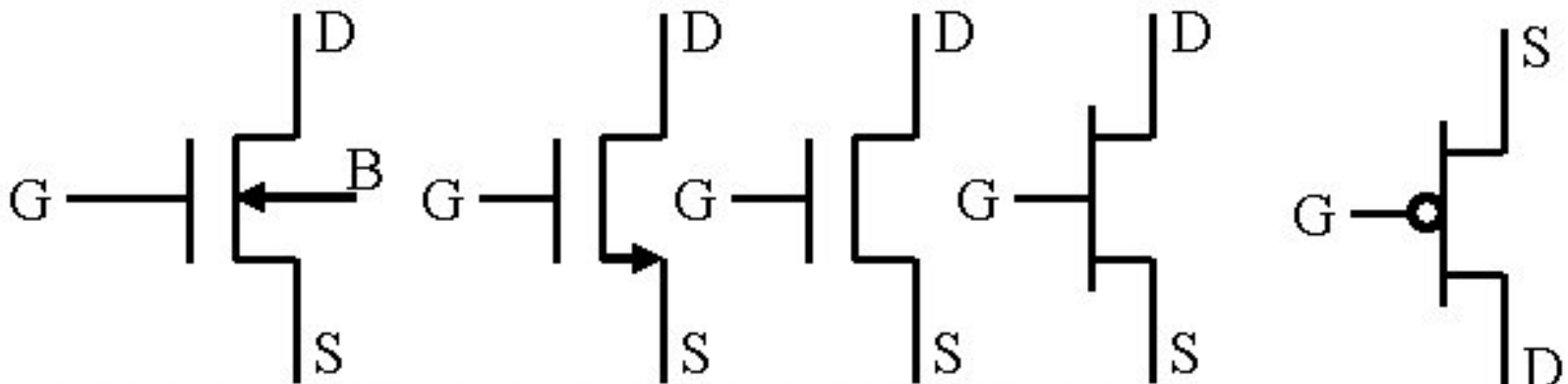
MOS Transistor Basics
Four Terminal Structure

- p-Substrate
- The MOS n-channel transistor structure:



MOS Transistor Basics
Four Terminal Structure (Continued)

- **Symbols: n-channel - p-substrate; p-channel – n-substrate**



N-channel (for P-channel, reverse arrow or add bubbles)

P-channel

- **Enhancement mode:** no conducting channel exists at $V_{GS} = 0$
- **Depletion mode:** a conducting channel exists at $V_{GS} = 0$

Threshold Voltage Components

- Consider the prior 3-D drawing: Set $V_S=0$, $V_{DS}=0$, and $V_{SB}=0$.
  - Increase V_{GS} until the channel is inverted. Then a conducting channel is formed and the depletion region thickness (depth) is maximum as is the surface potential.
  - The value of V_{GS} needed to cause surface inversion (channel creation) is the ***threshold voltage*** V_{T0}. The 0 refers to $V_{SB}=0$.
  - $V_{GS}< V_{T0}$: no channel implies no current flow possible. With $V_{GS}> V_{T0}$, existence the channel implies possible current flow.

Threshold Voltage Components

1) Φ_{GC} work function difference between gate and channel material which is the built-in voltage that must be offset by voltage applied to flatten the bands at the surface.
2) Apply voltage to achieve surface inversion $-2\phi_F$

Threshold Voltage Components (Cont.)

3) Additional voltage must be applied to offset the depletion region charge due to the acceptor ions. At inversion, this charge with $V_{SB}=0$ is $Q_{B0}= Q_0$.

For V_{SB} non-zero,

$$Q = -\sqrt{2q N_A \varepsilon_{Si} \left| -2\phi_F + V_{SB} \right|}$$

The voltage required to offset the depletion region charge is defined by $-Q_B/C_{ox}$ where $C_{ox} = \varepsilon_{ox}/t_{ox}$ with t_{ox}, the oxide thickness, and C_{ox}, the gate oxide capacitance per unit area.

4) The final component is a fixed positive charge density that appears at the interface between the oxide and the substrate, Q_{ox}. The voltage to offset this charge is:

$$\frac{-Q_{ox}}{C_{ox}}$$

Threshold Voltage Components (Cont.)

- These components together give:

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

- For $V_{SB}=0$, V_{T0} has Q_B replaced by Q_{B0}. This gives a relationship between V_T and V_{T0} which is:

$$V_T = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

- Thus the actual threshold voltage V_T differs from V_{T0} by the term given. Going back to the definition of Q_B, this term is equal to:

$$+\gamma\left(\sqrt{\left|-2\phi_F + V_{SB}\right|} - \sqrt{\left|2\phi_F\right|}\right)$$

- In which γ is the **substrate-bias (or body effect) coefficient**.

Threshold Voltage Components (Cont.)

Those parameters in the V_T equation are signed. The following table gives their signs for nMOS and pMOS transistor.

Parameter	nMOS	pMOS
ϕ_F	−	+
Q_B, Q_{B0}	−	+
γ	+	−
V_{SB}	+	−

- For real designs, the threshold voltage, due to variation in oxide thickness, impurity concentrations, etc., V_{T0} and γ should be measured from the actual process.

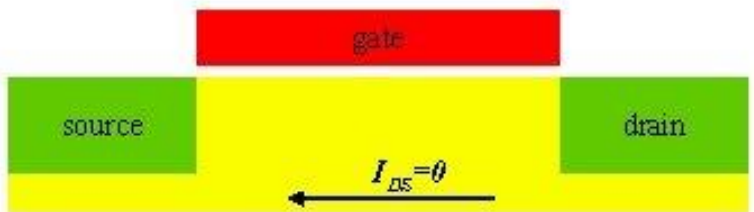
MOSFET Modes of Operation

Cutoff

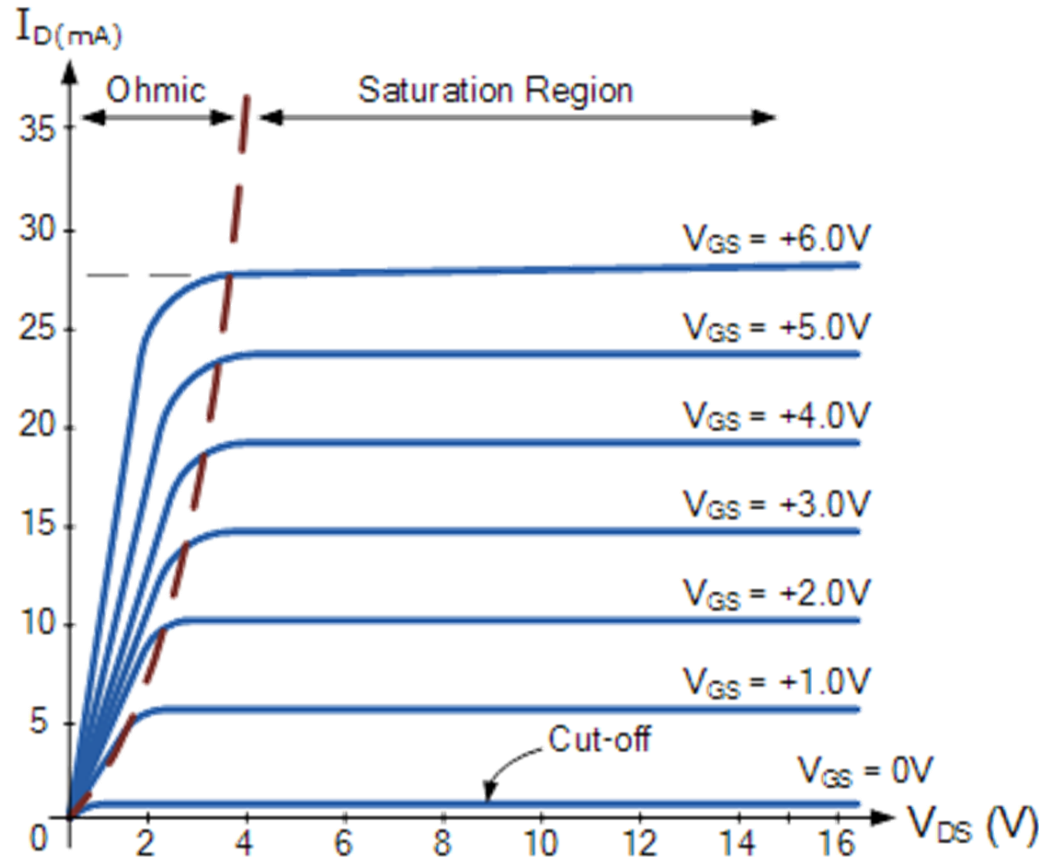
- **Assume n-channel MOSFET and $V_{SB}=0$**

Cutoff Mode: $0 \leq V_{GS} < V_{T0}$

- The channel region is depleted and no current can flow



$V_{GS} < V_{T0}$

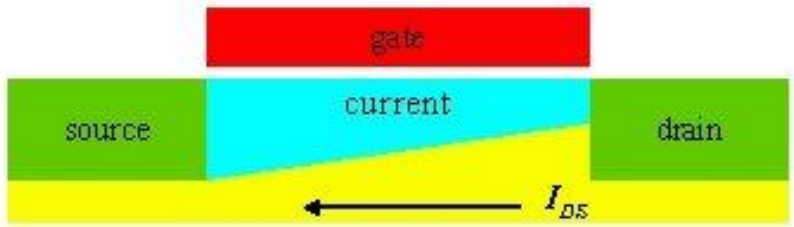


MOSFET Modes of Operation

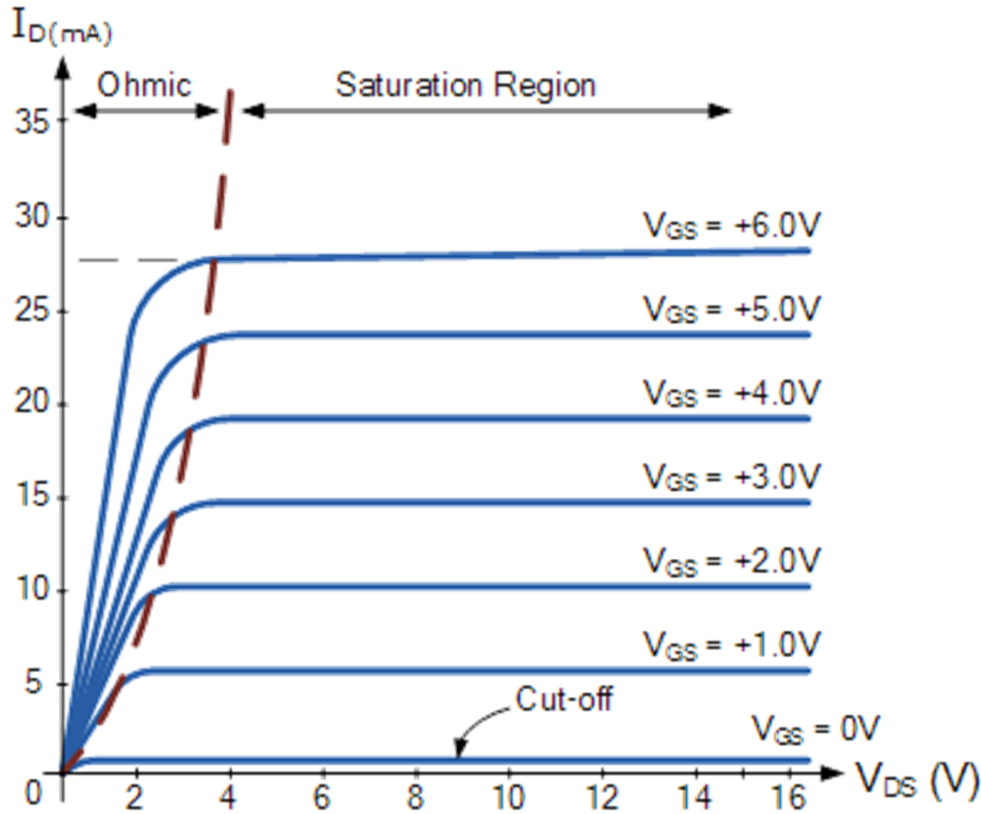
Linear

Linear (Active, Triode) Mode: $V_{GS} \geq V_{T0}$, $0 \leq V_{DS} \leq V_{D(SAT)}$

- Inversion has occurred; a channel has formed
- For $V_{DS} > 0$, a current proportional to V_{DS} flows from source to drain
- Behaves like a voltage-controlled resistance



$$V_{DS} < V_{GS} - V_{T0}$$

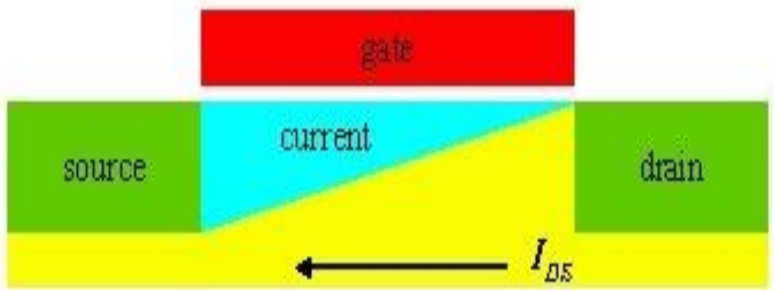


MOSFET Modes of Operation

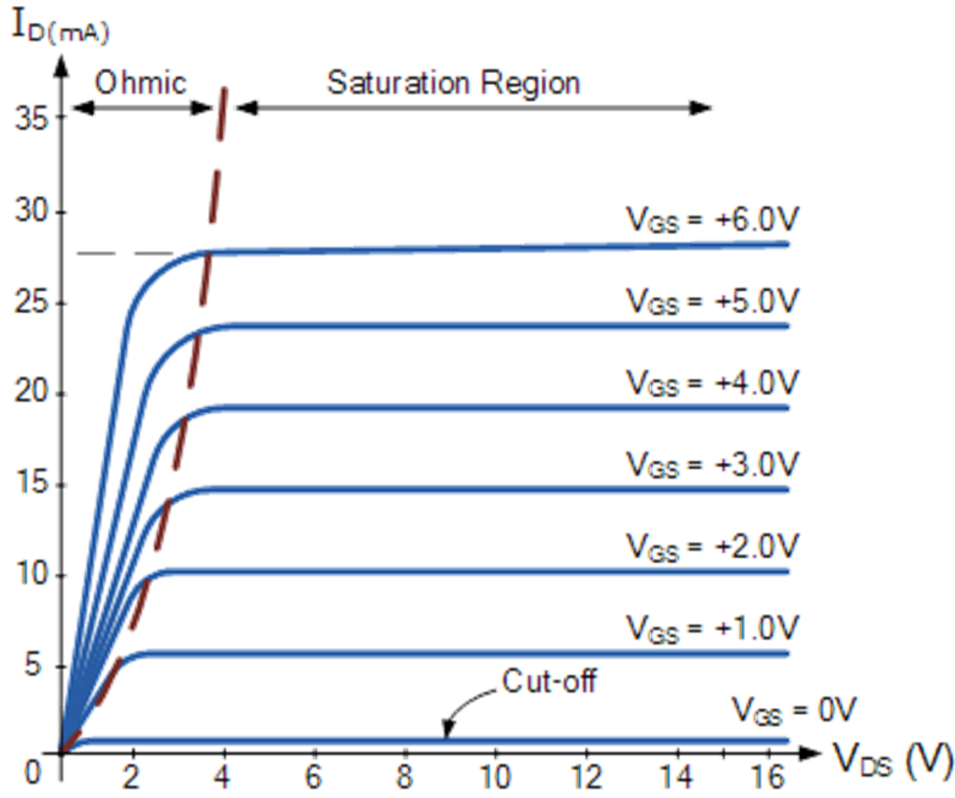
Pinch-Off

Pinch-Off Point (Edge of Saturation) : $V_{GS} \geq V_{T0}, V_{DS} = V_{D(SAT)}$

- Channel just reaches the drain
- Channel is reduced to zero inversion charge at the drain
- Drifting of electrons through the depletion region between the channel and drain has begun



$$V_{DS} = V_{GS} - V_{T0}$$

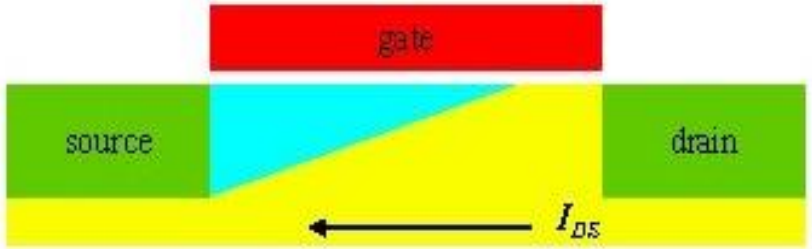


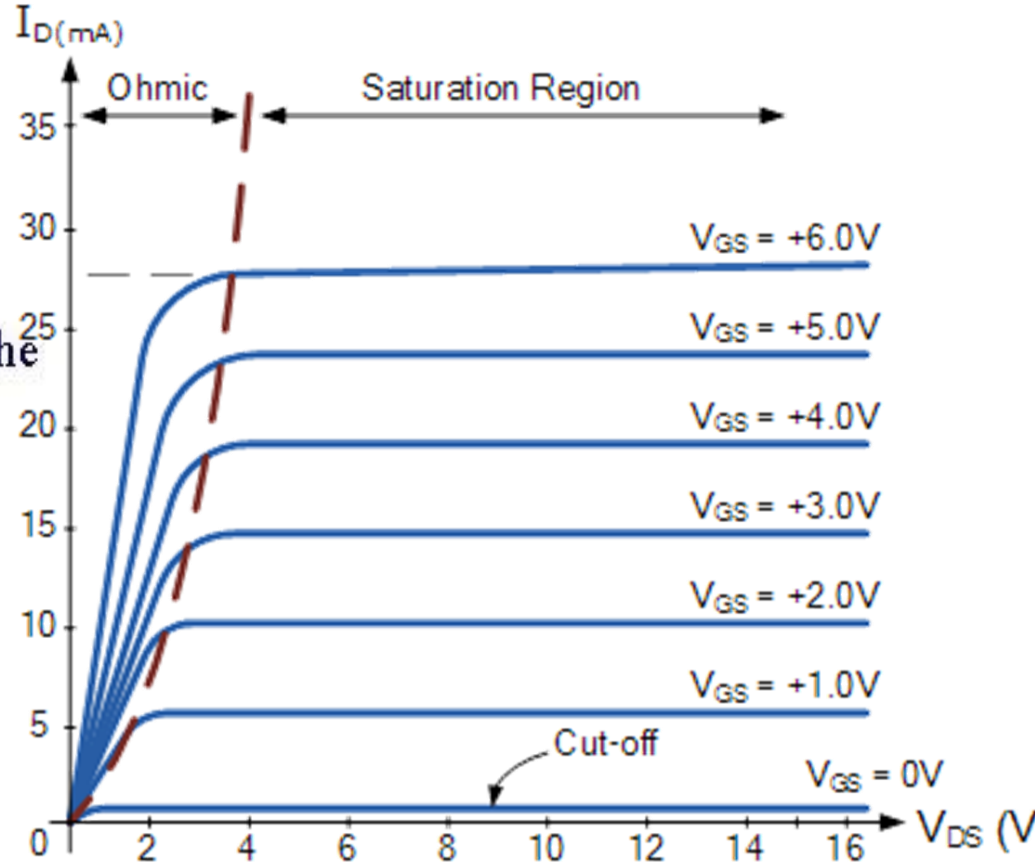
MOSFET Modes of Operation

Saturation

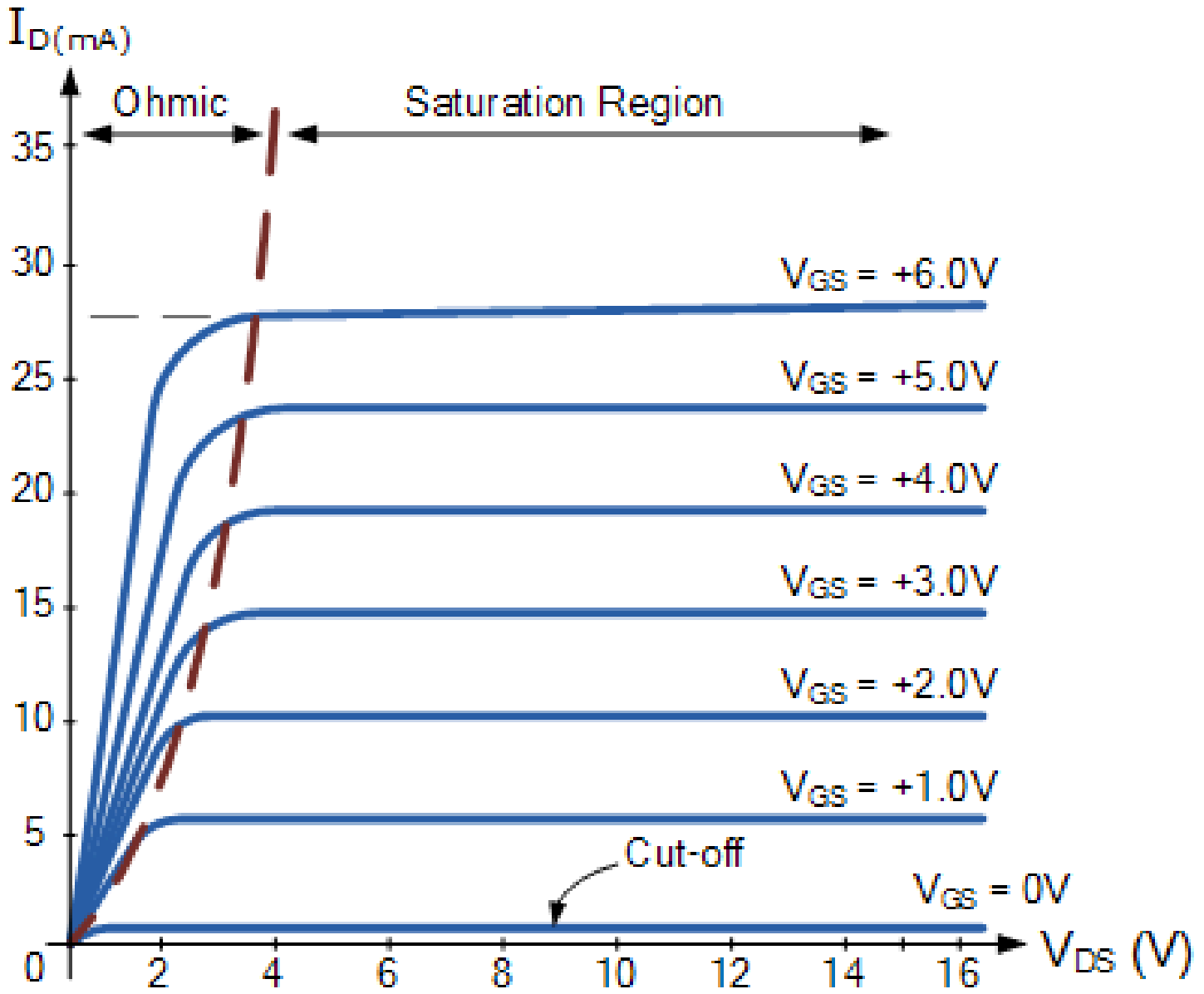
Saturation Mode: $V_{GS} \geq V_{T0}$, $V_{DS} \geq V_{D(SAT)}$

- Channel ends before reaching the drain
- Electrons drift, usually reaching the drift velocity limit, across the depletion region to the drain
- Drift due to high E-field produced by the potential V_{DS}-$V_{D(SAT)}$ between the drain and the end of the channel





$$V_{DS} > V_{GS} - V_{T0}$$

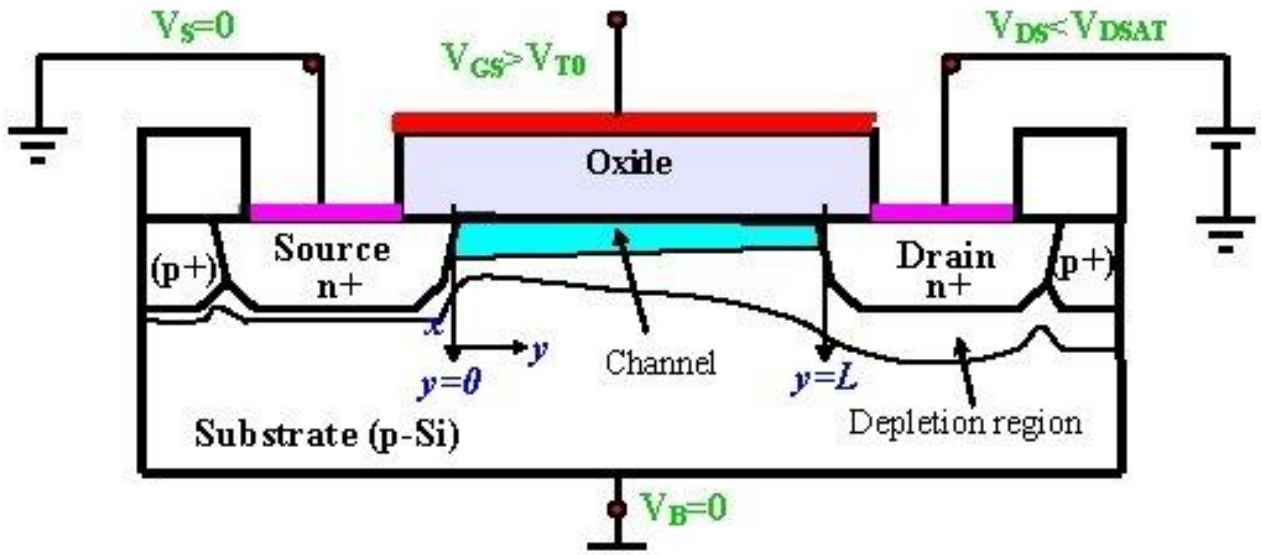

$I_{D(mA)}$
Ohmic
Saturation Region
35
30
25
20
15
10
5
0
V_{GS} = +6.0V
V_{GS} = +5.0V
V_{GS} = +4.0V
V_{GS} = +3.0V
V_{GS} = +2.0V
V_{GS} = +1.0V
Cut-off
V_{GS} = 0V
2
4
6
8
10
12
14
16
V_{DS} (V)

MOSFET I-V Characteristics
Gradual Channel Approximation

- **Preliminaries**
  - Gradual channel approximation will reduce the analysis to a one-dimensional current flow problem.
  - Assumption
    - » $V_{SB}=0$
    - » V_{T0} is constant along the entire channel
    - » E_y dominates $E_x \Rightarrow$ Only need to consider the current-flow in the y-dimension
- **Cutoff Mode: $0 \leq V_{GS} < V_{T0}$**
  - $I_{DS(cutoff)} = 0$

Gradual Channel Approximation
Linear Mode

- **Linear Mode:** $V_{GS} \geq V_{T0}$, $0 \leq V_{DS} \leq V_{D(SAT)} \Rightarrow V_{DS} - V_{GS} < V_{T0}$
  - The channel reaches to the drain.
  - $V_c(y)$: Channel voltage with respect to the source at position y
  - Boundary Conditions: $V_c(y=0)=V_s=0$; $V_c(y=L)=V_{DS}$

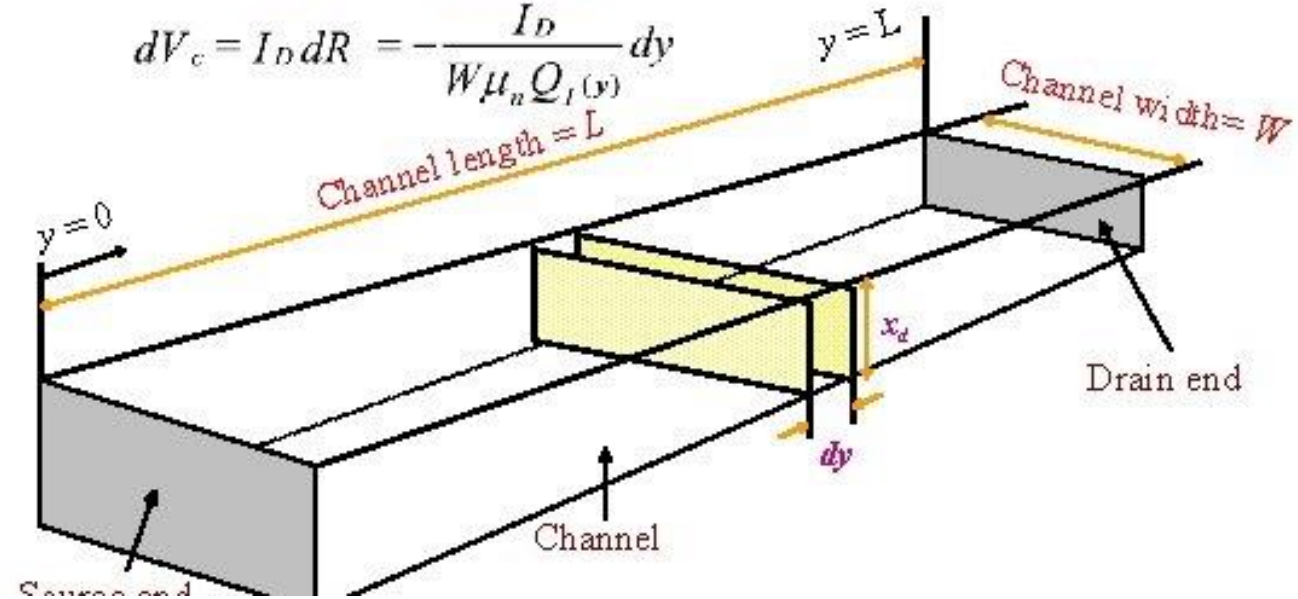


Gradual Channel Approximation
Linear Mode (Cont.)

- The differential resistance (dR) of the channels can represented in terms of the mobile electron charge ($Q_I(y)$) in the surface inversion layer, and the **electron surface mobility μ_n** (about ½ of the bulk electron mobility)

$$dR = -\frac{dy}{\sigma_n A_n} = -\frac{dy}{q\mu_n N_A W x_d(y)} = -\frac{dy}{W\mu_n Q_I(y)}$$

$$dV_c = I_D dR = -\frac{I_D}{W\mu_n Q_I(y)} dy$$



Gradual Channel Approximation
Linear Mode (Cont.)

- Finally, the drain current is

$$I_{D(lin)} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2\right]$$

- To simplify the equation, we define

$$\kappa = \kappa' \frac{W}{L} = \mu_n C_{ox}\frac{W}{L}$$

κ': the *process transconductance parameter*

κ: the *device transconductance parameter*

Gradual Channel Approximation
Pinch-Off, Saturation

Pinch-Off Point (Edge of Saturation) : $V_{GS} \geq V_{T0}$, $V_{DS}=V_{D(SAT)}$

- Channel just reaches the drain but is reduced to zero inversion charge at the drain
- Electrons drift through the depletion region between the channel and drain

Saturation Mode: $V_{GS} \geq V_{T0}$, $V_{DS} \geq V_{GS} - V_{T0}$

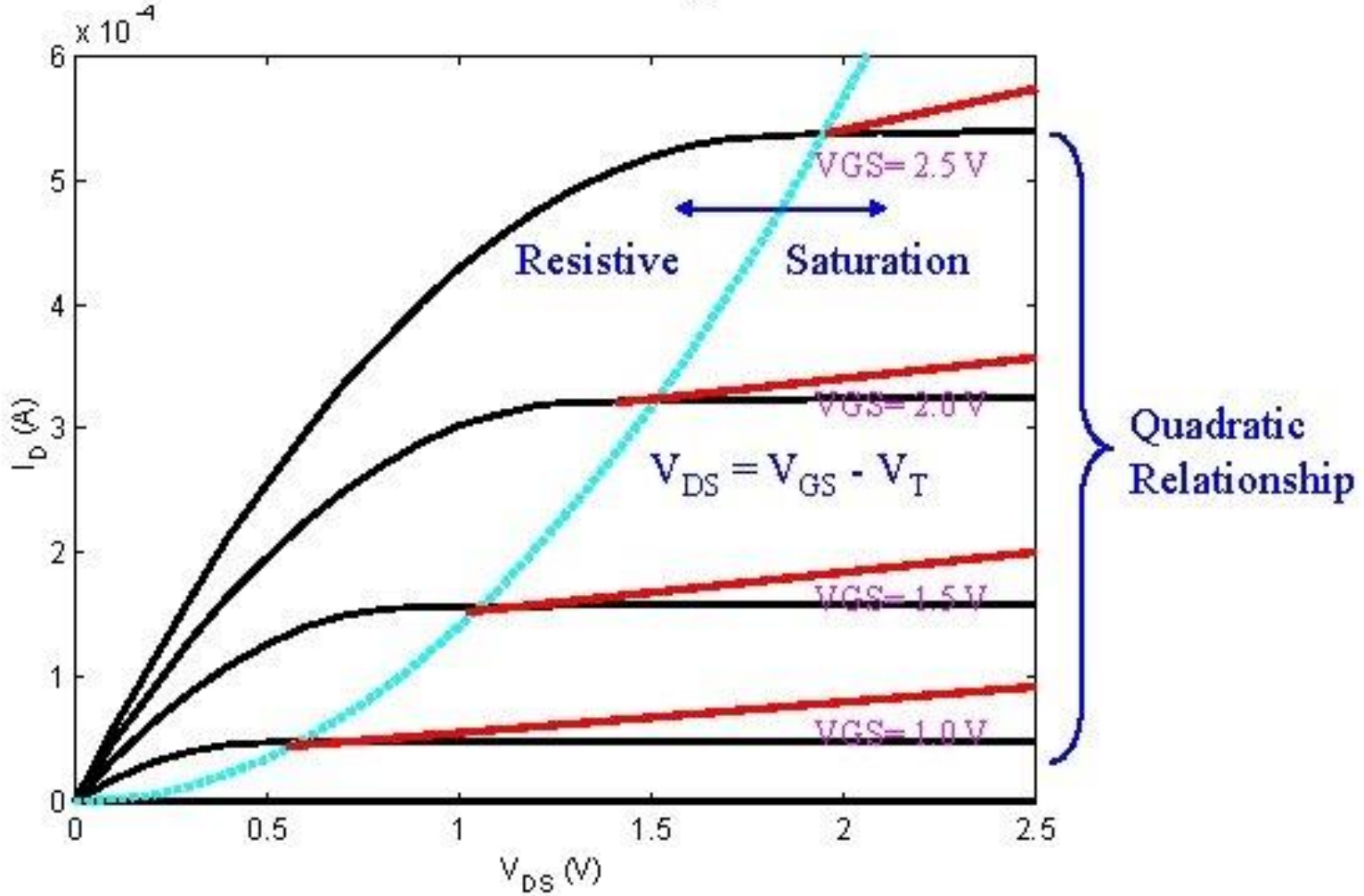
- In pinch-off voltage from the channel end to the source is $V_{D(SAT)}=V_{GS} - V_{T0}$. Substituting this for V_{DS} in the equation for I_D gives:

$$I_{D(SAT)} = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{T0})^2$$

MOSFET I-V Characteristics

I-V Plots, Channel Length Modulation

- Saturation equation yields curves independent of V_{DS}. Not sure! So we consider the effect of channel length modulation.



MOSFET I-V Characteristics
Channel Length Modulation

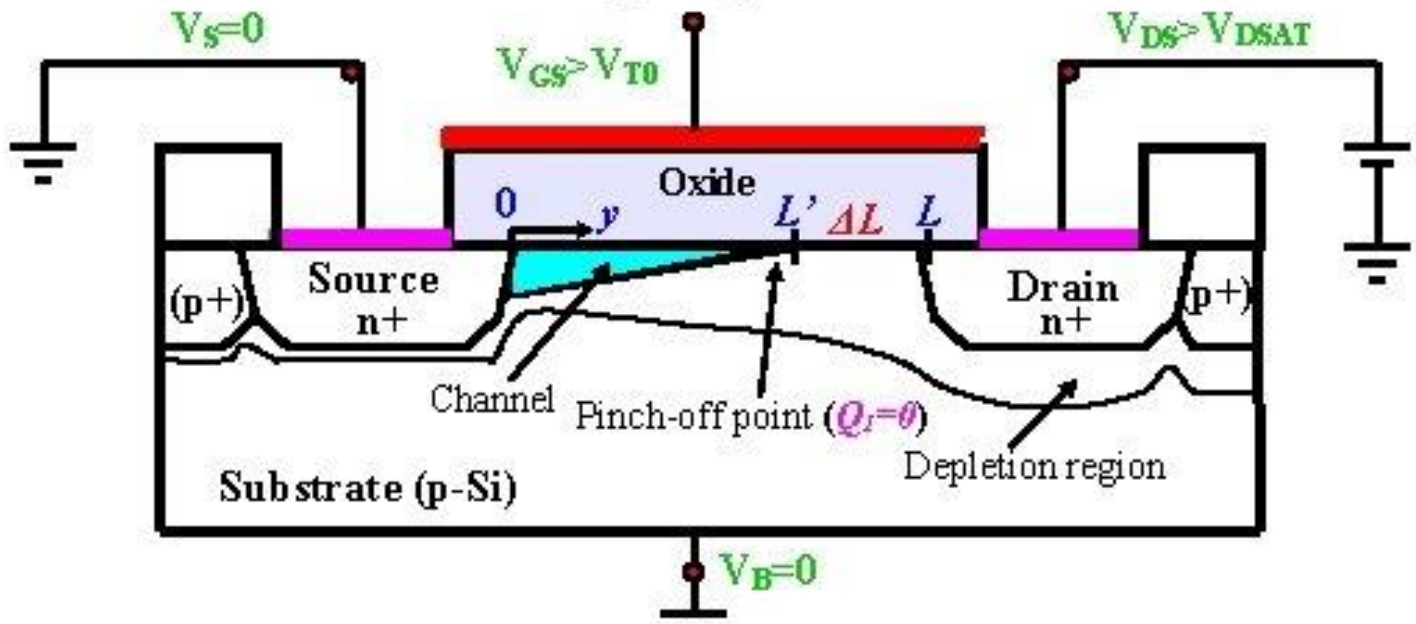
Channel Length Modulation

- With pinch-off the channel at the point y such that $V_c(y)=V_{GS}-V_{T0}$. The effective channel length is equal to $L' = L - \Delta L$

  ΔL is the length of channel segment over which $Q_I=0$.

- Place L' in the $I_{D(SAT)}$ equation:

$$I_{D(SAT)} = \frac{\mu_n C_{ox}}{2}\frac{W}{L'}(V_{GS}-V_{T0})^2$$



MOSFET I-V Characteristics
Channel Length Modulation

ΔL increases with an increase in V_{DS}. We can use

$$\frac{1}{L'} = \frac{1}{L-\Delta L} = \frac{1}{L}\frac{1}{\frac{L-\Delta L}{L}} = \frac{1}{L}\frac{1}{1-\frac{\Delta L}{L}} = \frac{1}{L}\frac{1}{1-\lambda V_{DS}} = \frac{1}{L}\left(1+\lambda V_{DS}\right)$$

λ: channel length modulation coefficient

$I_{D(SAT)}$ can be rewritten as

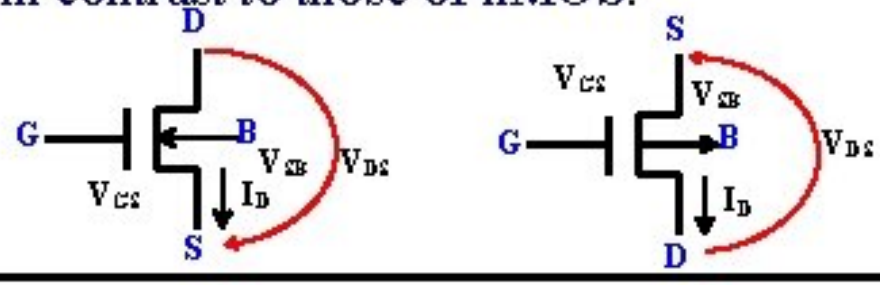
$$I_{D(SAT)} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2(1+\lambda V_{DS})$$

- The above form produces a discontinuity of current at $V_{DS}=V_{GS}-V_{T0}$. We can include the term in $I_{D(lin)}$ with little error since λ is typically less than 0.1. We will usually ignore λ in manual calculations.

MOSFET I-V Characteristics

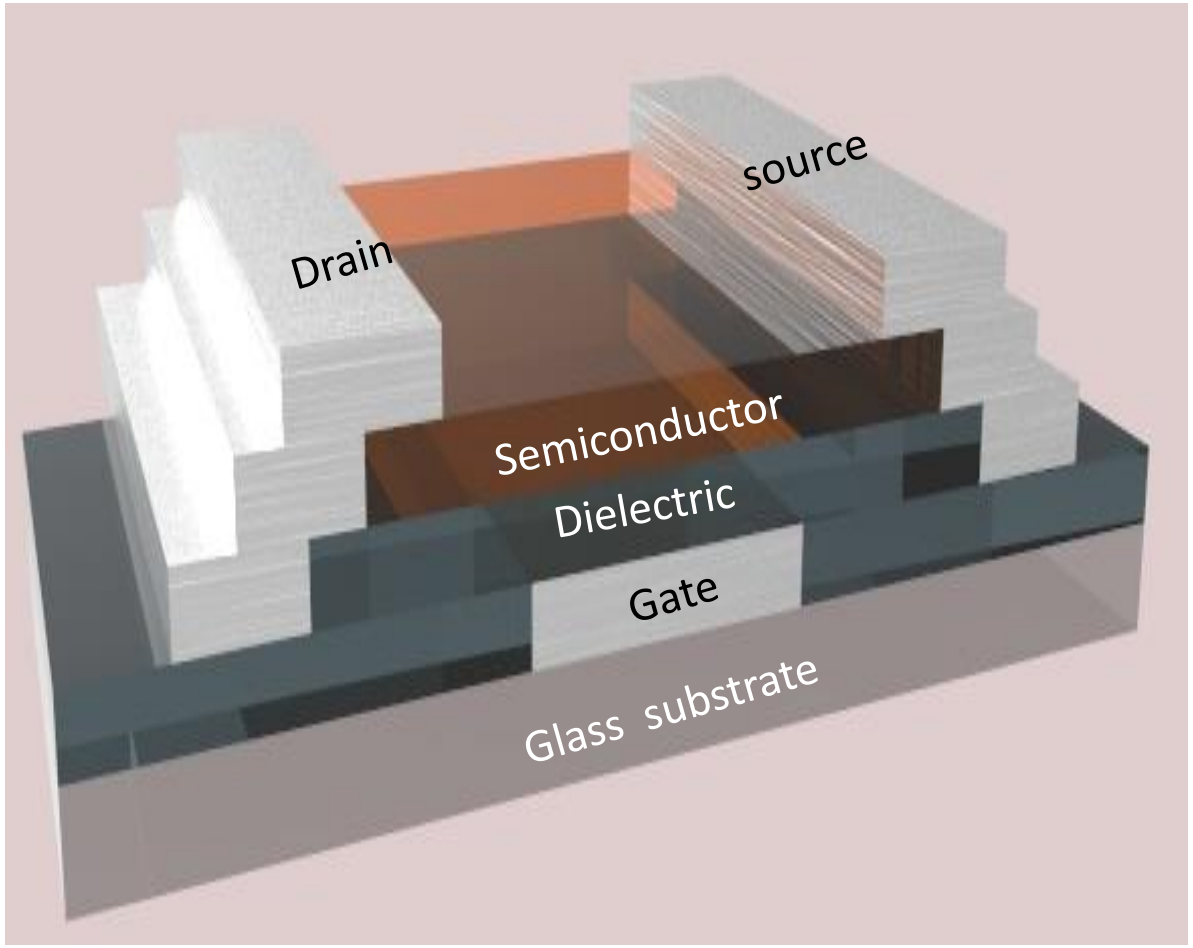
Summary of Analytical Equations

- The voltage directions and relationships for the three modes of pMOS are in contrast to those of nMOS.

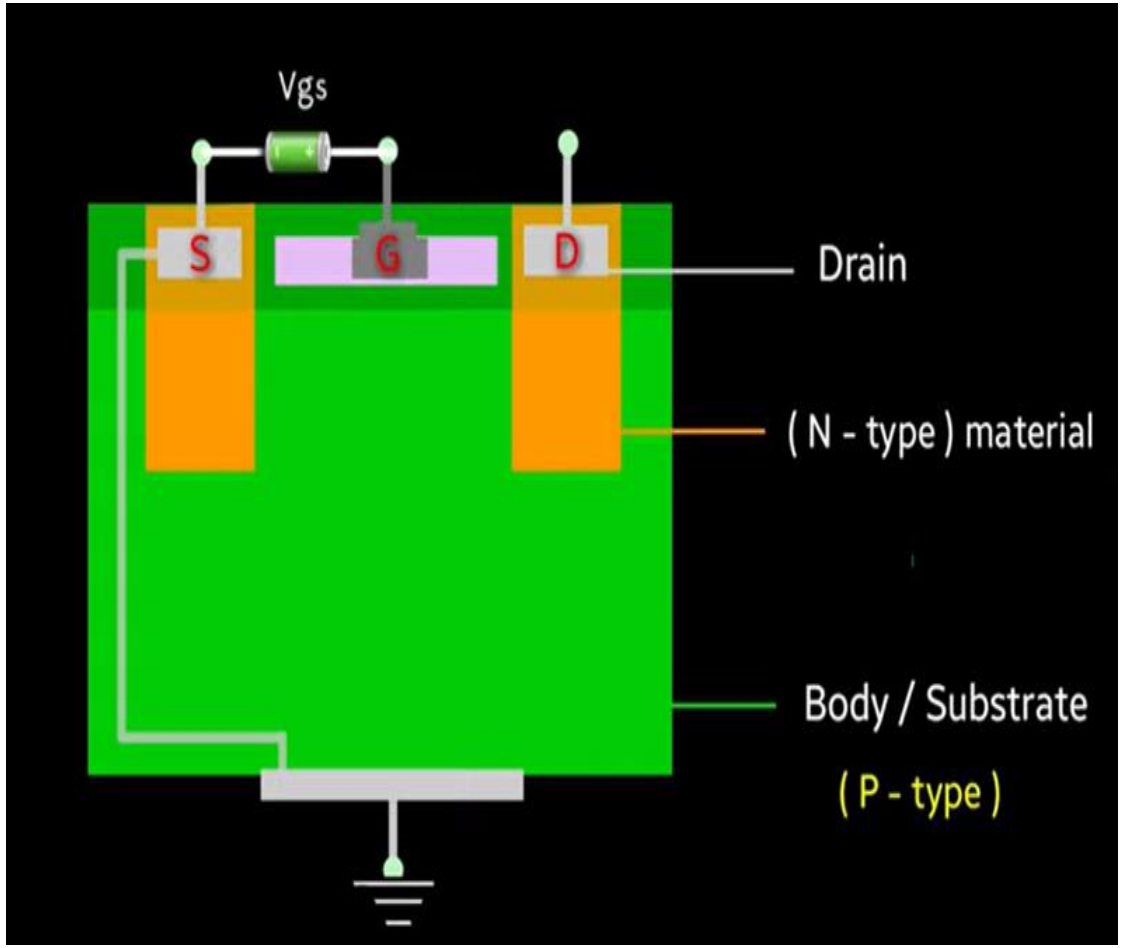


nMOS		
Mode	I_D	**Voltage Range**
Cut-off	0	$V_{GS} < V_T$
Linear	$(\mu_n C_{ox}/2)(W/L)[2(V_{GS}-V_T)V_{DS}-V_{DS}^2]$	$V_{GS} \geq V_T$, $V_{DS} < V_{GS}-V_T$
Saturation	$(\mu_n C_{ox}/2)(W/L)(V_{GS}-V_T)^2(1+\lambda V_{DS})$	$V_{GS} \geq V_T$, $V_{DS} \geq V_{GS}-V_T$
pMOS		
Cut-off	0	$V_{GS} > V_T$
Linear	$(\mu_n C_{ox}/2)(W/L)[2(V_{GS}-V_T)V_{DS}-V_{DS}^2]$	$V_{GS} \leq V_T$, $V_{DS} > V_{GS}-V_T$
Saturation	$(\mu_n C_{ox}/2)(W/L)(V_{GS}-V_T)^2(1+\lambda V_{DS})$	$V_{GS} \leq V_T$, $V_{DS} \leq V_{GS}-V_T$

THIN FILM TRANSISTORS

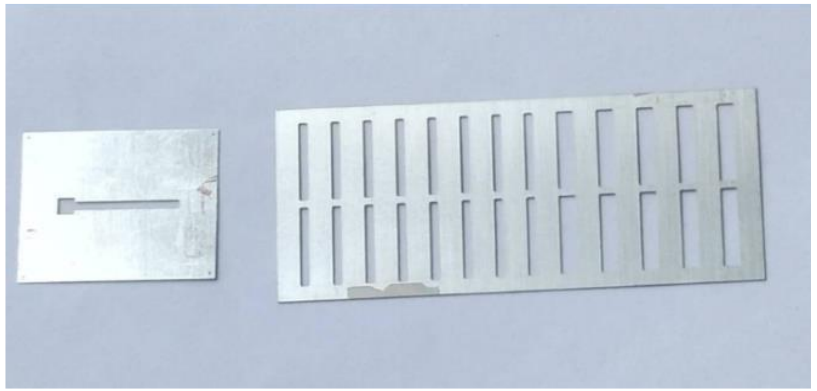


TFTs



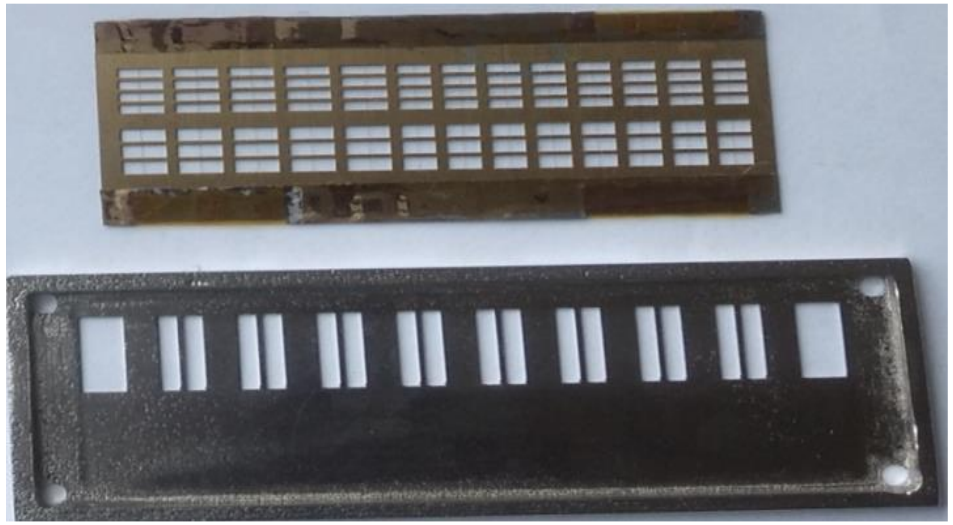
MOSFETs

Spiral Inductor - 1mm gap, 1mm width, No of turns-6.



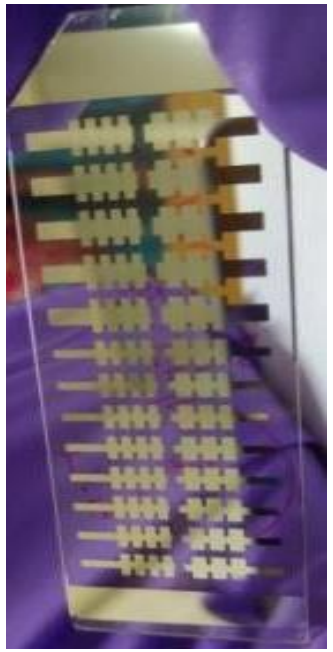
Gate mask-1mm, 1.5,2mm,3mm and 2cm

Dielectric Mask- 6cmX 1.5 cm



Drain and source mask-L-80 μm /W-1mm,1.5mm,2mm,3mm and 250 μm L/W-2mm.

TFTs ON GLASS ELECTRICAL CHARACTERISTICS

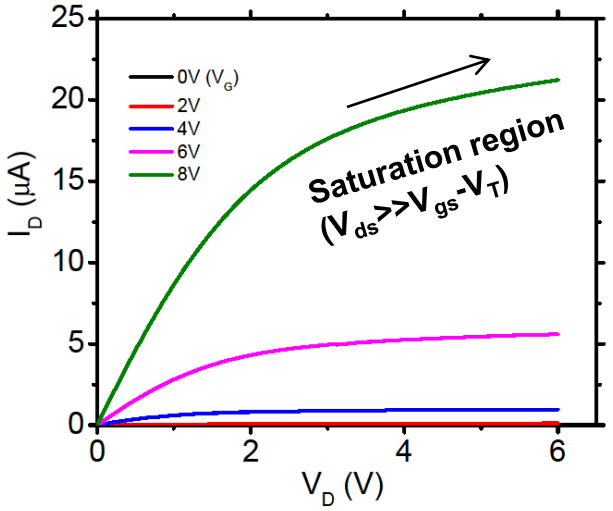


Fabricated
TFTs device

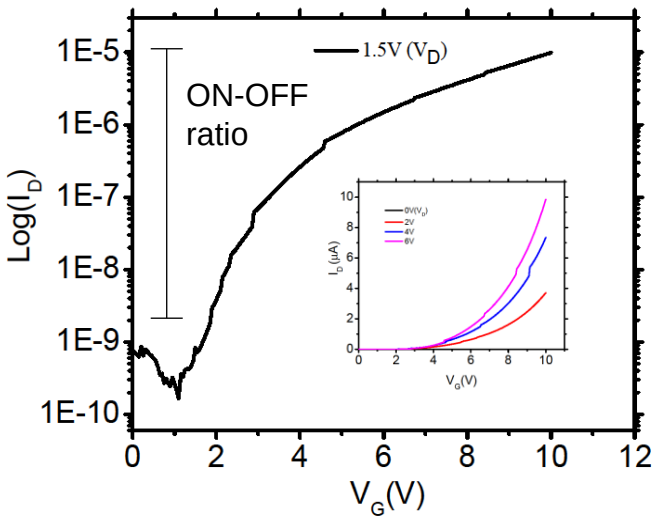
W-1 mm
L-80µm

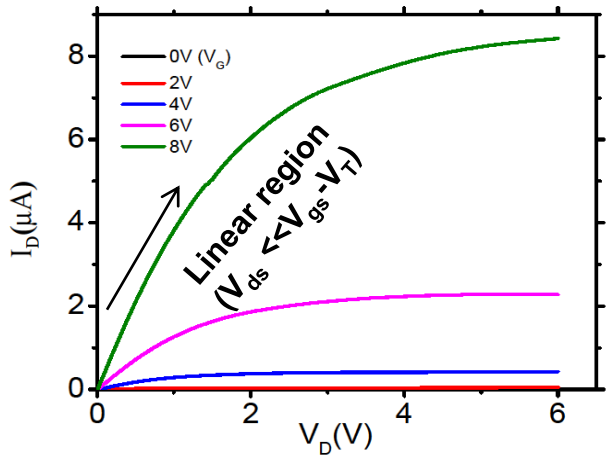
Al-150nm
Al_xO_y-250nm
ZnO-20nm
Al-150nm

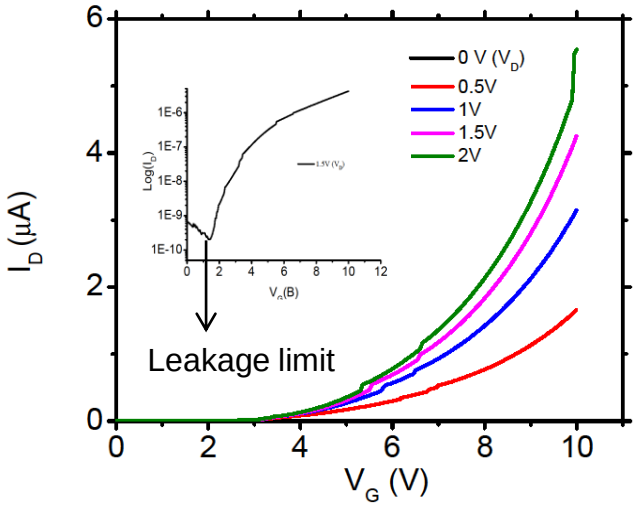
Output characteristics



Transfer characteristics

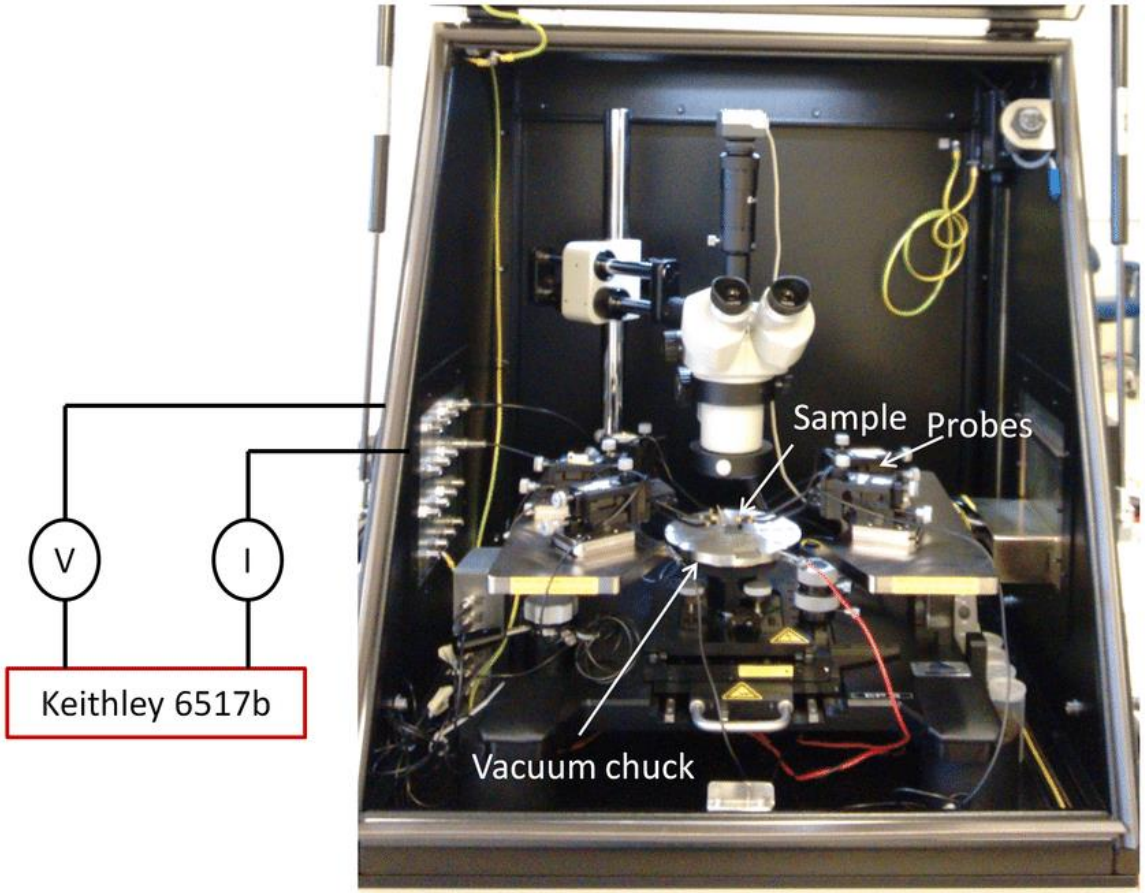






Threshold Voltage (V_T) = **1.5 V to 2 V.**

Mobility (µ) = **2 cm^2/V sec to 3 cm^2/V sec.** ON-OFF Ratio = **$2E^{04}$ to $3E^{04}$.**


V
I
Keithley 6517b
Sample
Probes
Vacuum chuck

Output Characteristics

With the gate voltage fixed, an increase of the drain voltage from zero causes small channel resistance so that the drain current increases linearly with drain voltage. An additional increase of the drain voltage causes the drain current to increase at a smaller rate and, eventually, the increase of the drain voltage, causes the channel to be pinched at the drain end. The drain voltage at the onset of pinch-off is known as saturation drain voltage, Vsat. For voltages greater than the saturation voltage, further pinching of the channel takes place and the pinched-off region spreads out in the channel to the source, effectively isolating the channel from the drain.

If $V_{DS} < V_{GS} - V_{TH}$, the TFT is in linear mode and I_{DS} is described by

$$I_{DS} = \mu_{lin} C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right), \; V_{DS} < V_{GS} - V_T$$

where,

μ_{lin}- Mobility (Linear region).

Cox – Gate capacitance per unit area.

W – Channel width.

L – Channel length of the device.

W/L– Aspect Ratio.

V_{GS}- Voltage gate to source.

V_T-Threshold Voltage

$$I_{DS} = \mu_{lin} C_{ox} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right), V_{DS} < V_{GS} - V_T$$

If $V_{DS} > V_{GS} - V_{TH}$, the device is in saturation mode. I_{DS} is independent of V_{DS} and is described by:

$$I_{DS} = \mu_{sat} C_{ox} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right), \quad V_{DS} \geq V_{GS} - V_T$$

$$I_{DS} = \mu_{sat} C_{ox} \frac{W}{L} \left(V_{GS} - V_T\right)^2$$

Threshold Voltage

It is the minimum gate voltage required for the formation of a channel from drain to source (along the length of the channel) and is denoted by V_T. It can be obtained from transfer characteristics for a specific drain voltage. From transfer characteristics, a tangent is drawn from the transfer characteristic curve (where the current increases from 0 A) and it is extended to the V_G axis the point of intersection of a tangent with the V_G axis gives the threshold voltage of the transistor.

ON/OFF RATIO

It is defined as the ratio between the channel currents when the transistor is in the conduction mode (I_{on}) and when it is switched off (I_{off}). Since the ideal I_{off} value is minimal (to avoid power consumption when not operating), I_{on} /I_{off} should be the highest as possible. It is also the ratio of the maximum to minimum I_{DS}

$$On-OffRatio = \frac{I_{DS}(max)}{I_{DS}(min)}$$

Trans conductance (g_m):

It is the ratio of the change in drain current to the change in gate voltage over a defined, arbitrarily small interval on the drain-current versus gate-voltage curve.

$$g_m = \frac{dI_{DS}}{dV_{GS}}$$

Mobility **Mobility**

The **electron mobility** characterizes how quickly an electron can move through a metal or semiconductor when pulled by an electric field. In semiconductors, there is an analogous quantity for holes, called **hole mobility**. The term **carrier mobility** refers in general to both electron and hole mobility in semiconductors. Electron mobility is almost always specified in units of cm2 /(V·s).

$$\mu_{lin} = m \frac{L}{WC_{ox}V_{DS}}$$

$$\mu_{sat} = m^2 \frac{2L}{WC_{ox}}$$

Sub-threshold slope:

For $V_G<V_T$ region the line would be linear in the plot log (I_D) vs. V_G. The slope of this line is the sub-threshold slope. It represents how fast the I_D ramps up for an increase in V_G. Steep slope means the device gets out of the sub-threshold region faster or in other words, has lower V_T and therefore conducts better.

$$subthresholdslope = \frac{dlog(I_{DS})}{dV_{GS}}$$

Sub-threshold Swing:

It is defined as the change in gate voltage which must be applied to create a one-decade increase in the output current. Small sub-threshold swing means better channel control. It is generally the inverse of the sub-threshold slope. Sub-threshold swing is denoted by ‘s’.

$$s = \left[\frac{dlog(I_{DS})}{dV_{GS}}\right]^{-1}$$