# Level-1

FPGAspeaks

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## 1 Introduction

In this level you will get started with basic Gate level in Verilog which are building blocks for any boolean function.

## 2 Pre-requisites

basic knowledge of Logical Gates.

## 3 Tools/Requirements

1. **Xilinx Vivado/Xilinx ISE** : If you have this tools then directly you can start. Visit my youtube video where you can learn how to create a project in vivado(similarly ISE).
   Click Here
   for time being need is till Simulation. Need not to worry beyond Simulation.

**OR**

2. **Linux Ubuntu Terminal** : (Ubuntu OS expected) If your Laptop doesn't support such Heavy tools or performs slower dont loose hope. In terminal we will be able to perform till Simulation and can view Wave-forms. However, we need above tools to go beyond Simulation.
   Visit my youtube video Click Here Also my verilog work in terminal Github repo Click for Git

## 4 What you are supposed to do ?

You are supposed to do all Verilog programs in Level-1 and make a collection similar to this in Git-Hub.

### 4.1 Note

We all have high tendency to forgot what we have learnt thus, Having collection of your work is highly encourageable, Create a Git-Hub repo named **FPGAspeaks** where you can have collection of your work for all Levels.