MUX

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So, Why MUXes are one of main element in FPGA or ASIC?

There are several reasons but I liked this one the most.

Logic Function Implementation : Any boolean expression can be implemented using a multiplexer *aka* MUX.
A multiplexer is a combinational logic circuit that selects one of many input signals and forwards it to a single output line based on the control inputs.
By appropriately setting the control inputs of a MUX, you can effectively implement any boolean expression.

Let us see

EXOR: $F = W_1 \oplus W_2$ This, can be implemented using 4×1 mux in which 4 data inputs are constants and select lines are driven by W_1 and W_2.

w_1	w_2	f
0	0	0
0	1	1
1	0	1
1	1	0

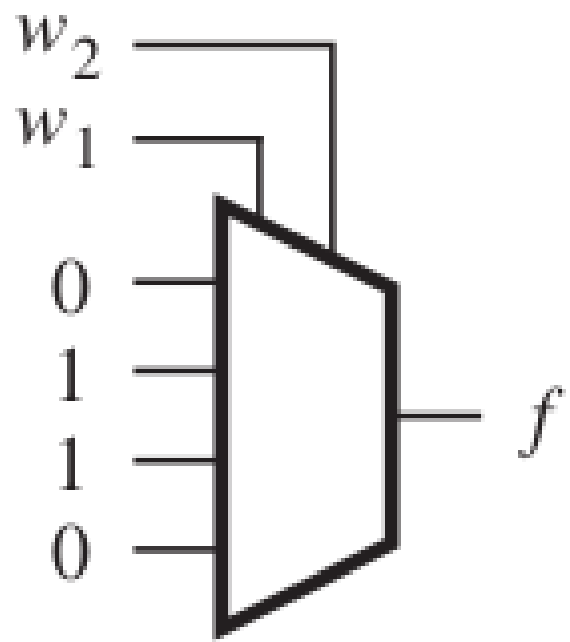


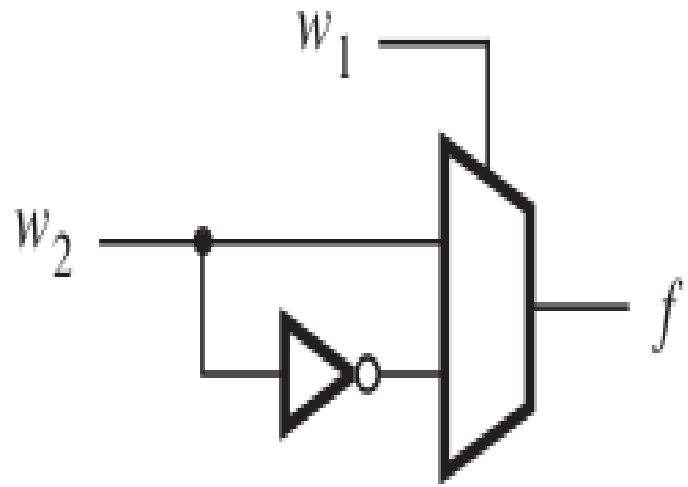
Figure: Implentation using a 4×1 mux

more compact can be done, by using 2×1 mux and one of the input as select line and other as data line.

w_1	w_2	f
0	0	0
0	1	1
1	0	1
1	1	0

w_1	f
0	w_2
1	$\bar{w}_2$

(a) Modified truth table



(b) Circuit

Figure: Using 2×1 mux

Let us see

3-Input EXOR: $F = W_1 \oplus W_2 \oplus W_3$

w_1	w_2	w_3	f	
0	0	0	0	
0	0	1	1	$w_2 \oplus w_3$
0	1	0	1	
0	1	1	0	
1	0	0	1	
1	0	1	0	$\overline{w_2 \oplus w_3}$
1	1	0	0	
1	1	1	1	

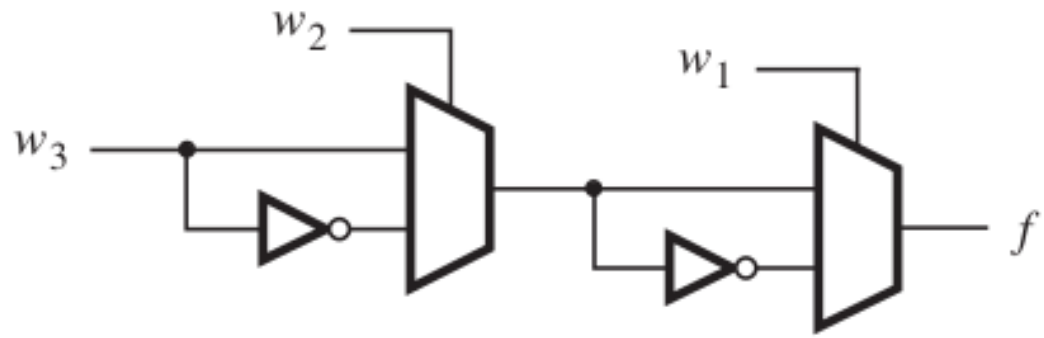


Figure: Three-input XOR implemented with 2×1 multiplexers.

w_1	w_2	w_3	f	
0	0	0	0	w_3
0	0	1	1	
0	1	0	1	$\overline{w}_3$
0	1	1	0	
1	0	0	1	$\overline{w}_3$
1	0	1	0	
1	1	0	0	w_3
1	1	1	1	

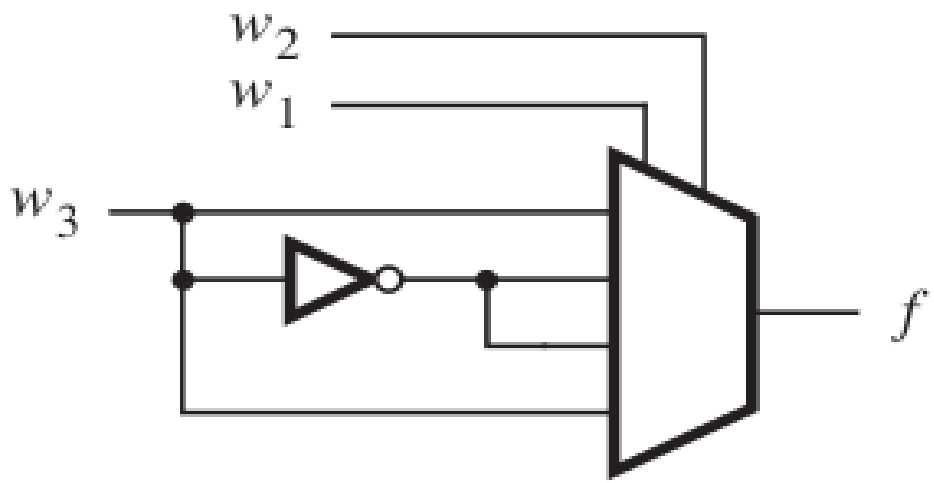


Figure: Three-input XOR implemented with 2×1 multiplexers.

Now, lets see

3-bit Majority function: So, in this 3 bits are given as input and if there are more bits with logic 0 then output is 0 otherwise 1.(vice versa too).

w_1	w_2	w_3	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

w_1	w_2	f
0	0	0
0	1	w_3
1	0	w_3
1	1	1

Figure: Modified truth table

Using, 4×1 Mux.

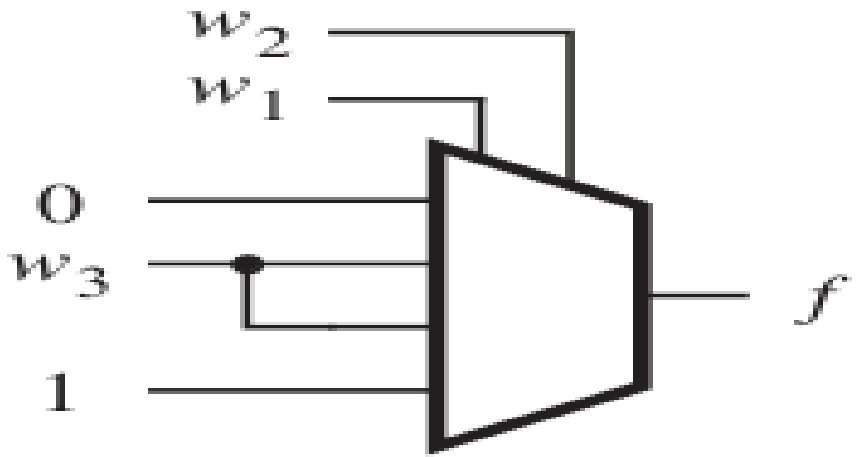


Figure: Using 4×1 mux

One more way of doing it.

See, we have three inputs if we select one input as select line remaining two can be fed as data input to mux after suitable operation according to truth table.

w_1	w_2	w_3	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

w_1	f
0	$w_2 w_3$
1	$w_2 + w_3$

Figure: Truth-Table

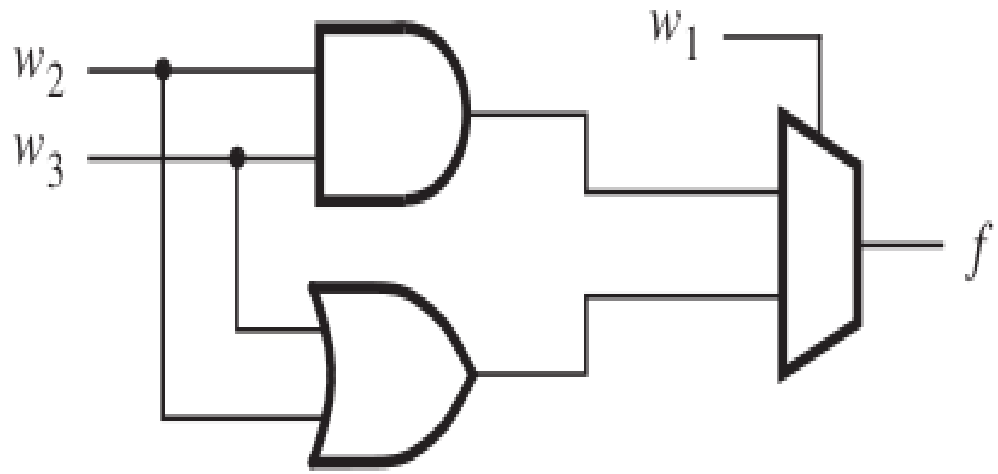


Figure: The three-input majority function implemented using a 2×1 multiplexer.

Reference: Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, Elizabeth A. Jones, 2002.

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