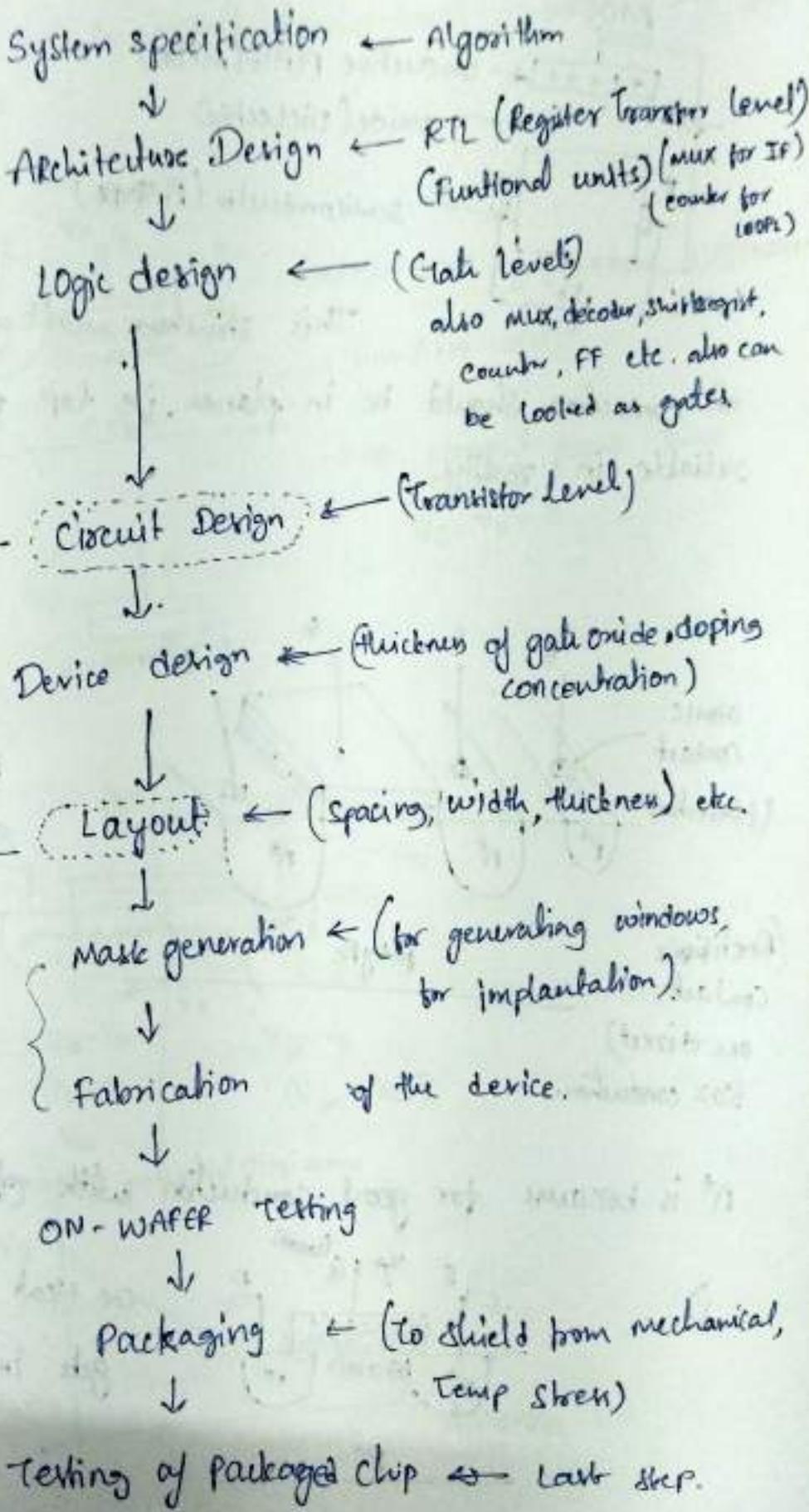


DIGITAL CMOS VLSI DESIGN (EC61006)

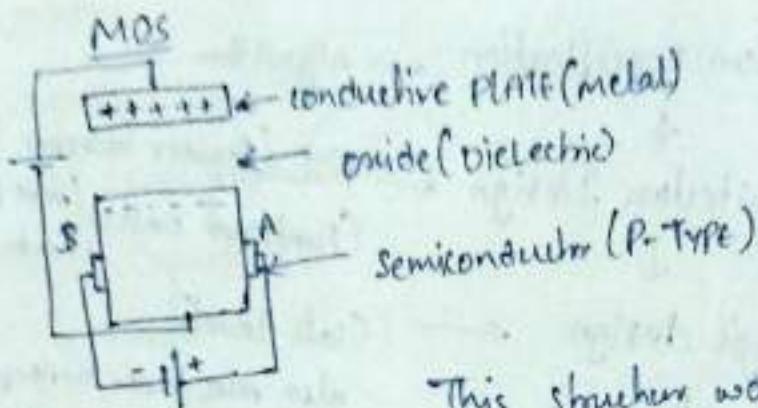
independent of
Fabrication facilities
Portable design

Physical design

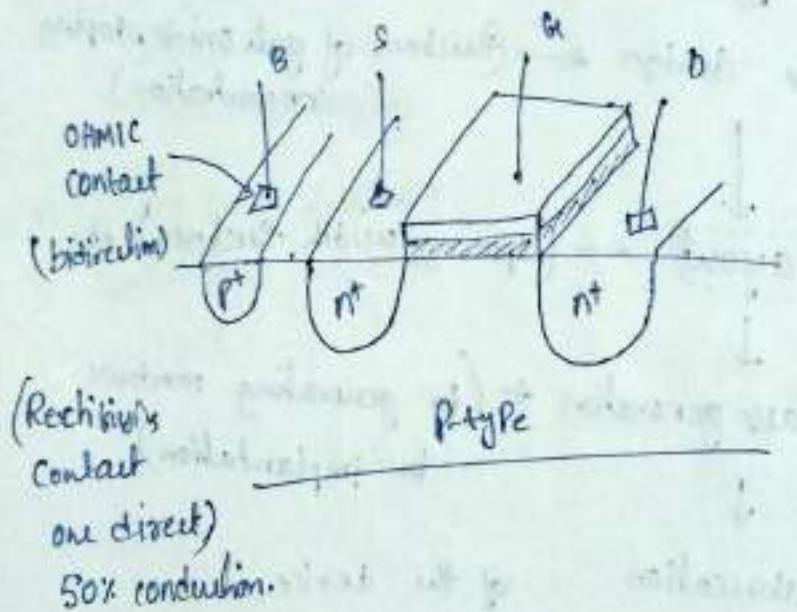
very less
work
in this
course



MOSFET (NMOS)

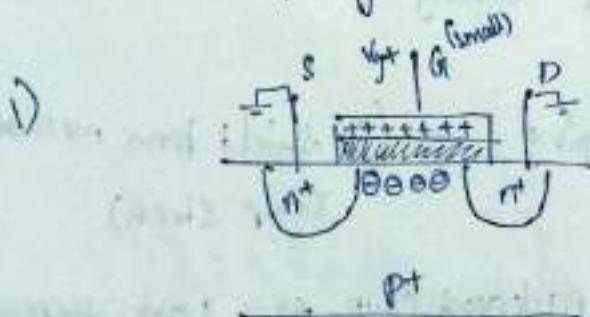


This structure won't work physical.
all connection should be in planar. i.e top plane. not
reliable in reality.



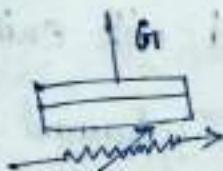
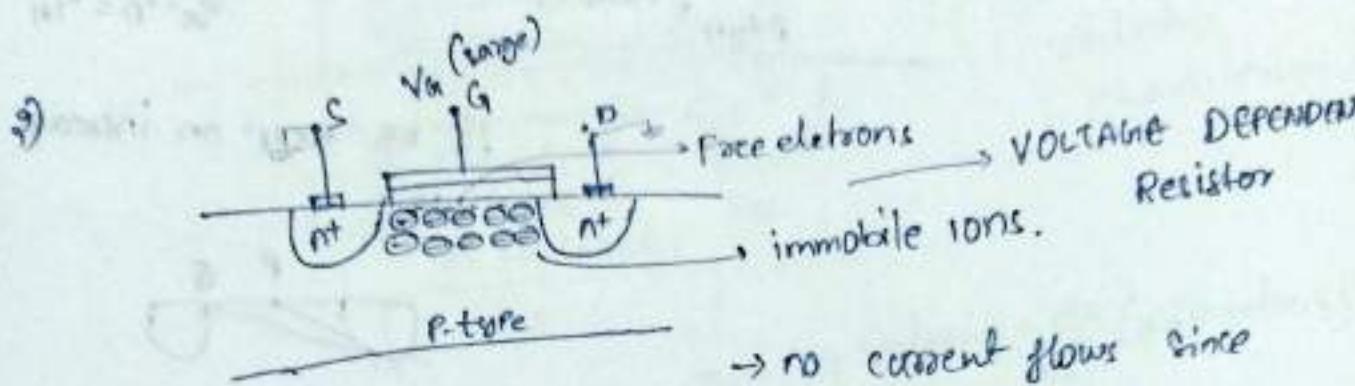
Symmetric,
because of S,D
are interchangeable

n⁺ is because for good conduction with Ohmic contact.

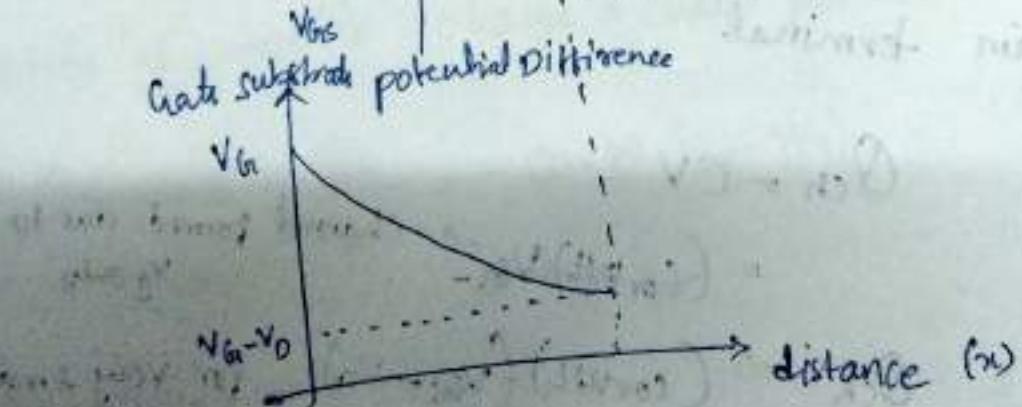
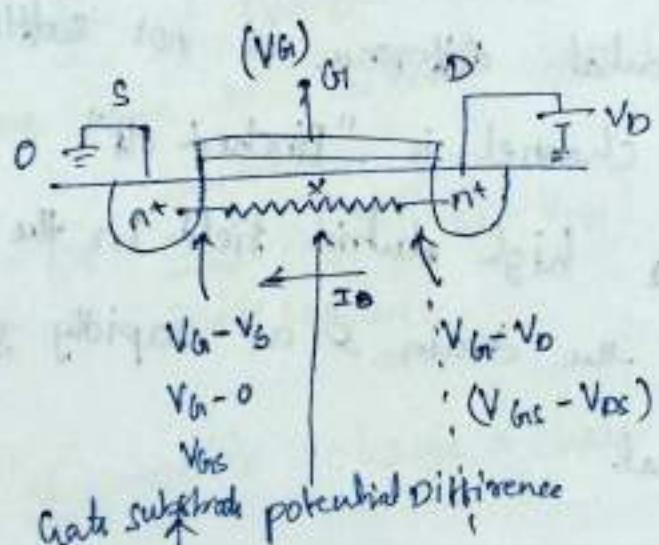


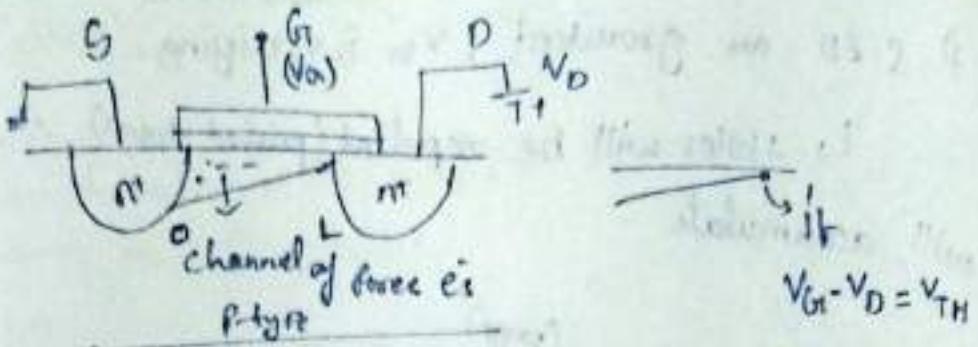
1) S & D are grounded, V_G is varying.

\hookrightarrow holes will be repelled (pushed down), \therefore immobile -ve ions will accumulate

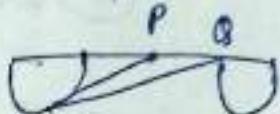


3)





if we keep on increasing V_D



- Due to high V_D , electric field will exist and which pulls electrons from source \rightarrow channel, so, current will not be zero.
- Gate-substrate potential difference is not sufficient at all to attract e's \rightarrow channel is "pinched off".
- The e's experience high electric field in the depletion region surrounding the drain & are rapidly swept into the drain terminal.

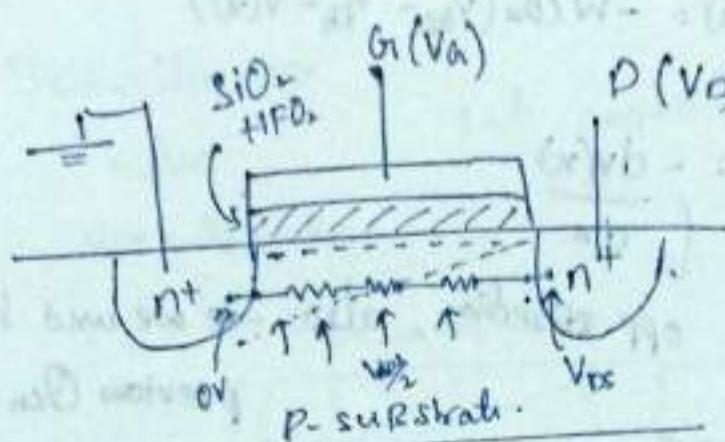
$$Q_{ch} = CV$$

$= (C_{oxWL})V_{Gs}$ → channel formed due to V_g only

$$Q_{ch} \Rightarrow (C_{oxWL})(V_{Gs} - V_{TH}) \text{ for very small value of } V_{Gs} Q_{ch} \neq 0$$

for Q_{ch} not be zero $\Rightarrow V_{Gs} - V_{TH}$

NMOS transistor



HFO_x modern
↓
for better dielectric characteristics

$$velocity = \frac{dx}{dt} \text{ (drift velocity)}$$

$$V_{Gn} > V_{TH}$$

$$x=0$$

$$x=L$$

→ Two electric fields, V_{Gn} due to V_g and V_D , no current due to E_{Vn} due to high impedance.

→ concentration of charges along the channel will not be same due to different potentials.

$$\delta_{Ch} = CV = \frac{Cox(WL)(V_{GS} - V_{TH})}{\text{oxide cap/unit area}}$$

→ Density of mobile charge = charge per unit length.

$$\therefore \delta_{Ch, \text{density}} = \frac{\delta_{Ch}}{L} = -CoxW(V_{GS} - V_{TH})$$

④ @ source terminal ($x=0$)

$$\delta_{Ch, \text{density}}(x) = \delta_{Ch, \text{density}}(0)$$

$$= -W Cox(V_{GS} - V_{TH})$$

at $x > 0$,

$$Q_{ch, \text{density}}(x) = -W \cos(V_{AS} - V_{TH} - V(x))$$

$$E(x) = -\frac{dV(x)}{dx}$$

$$\left(\frac{dV}{dx}\right)$$

opp direction, also -ve we used in
previous Qch eqn.

drift velocity

$$V_d = \frac{dx}{dt} = Mn E(x) = -Mn \frac{dV(x)}{dx}$$

$$I_{DS} = \frac{dQ}{dt} = \frac{dQ}{dx} \cdot \frac{dx}{dt}$$

charge / unit time, i.e. we are not
differentiating

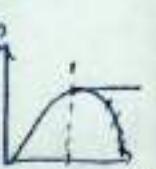
solve for

$$I_{DS} = \frac{W \cos(V_{AS} - V_{TH} - V(x))}{L} Mn \frac{dV(x)}{dx}$$

$$\int_{x=0}^L I_{DS} dx = \int_0^{V_{DS}} Mn W \cos(V_{AS} - V_{TH} - V(x)) dV(x)$$

$$I_{DS} \cdot L = Mn W \cos \left[(V_{AS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_{DS} = Mn \frac{W}{L} \cos \left[\left(V_{AS} - V_{TH} \right) - \frac{V_{DS}^2}{2} \right] V_{DS}$$



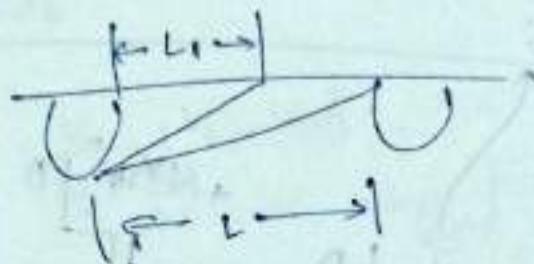
NMOS transistor is in Linear region.

not saturation, we haven't consider pinchoff.

→ in pinchoff Length of channel is less than L .

$I_{DS} = I_{DS, \text{max}}$
when sat current.

$$V_{DS} = V_{GS} - V_{TH}$$



sat current derivation

$$\int_{x=0}^{L_1} I_{DS} dx = \mu n C_{ox} W (V_{GS} - V_{TH} - V(x)) dV(x)$$

$$I_{DS} L_1 = \mu n C_{ox} W \left[(V_{GS} - V_{TH}) V(x) - \frac{1}{2} V^2(x) \right]_0^{V_{GS} - V_{TH}}$$

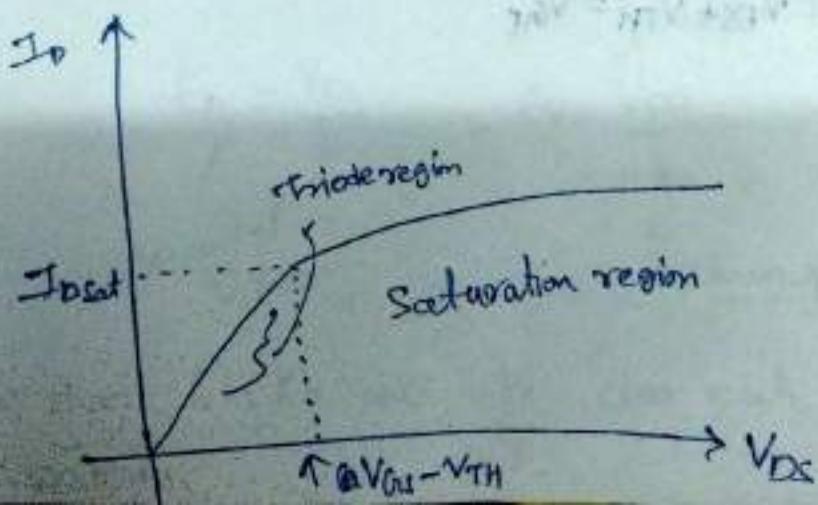
$$I_{DS} = \frac{1}{2} \mu n C_{ox} \frac{W}{L_1} (V_{GS} - V_{TH})^2$$

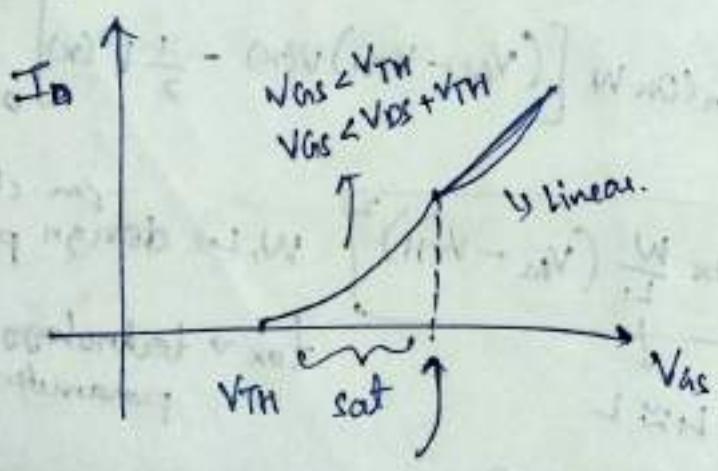
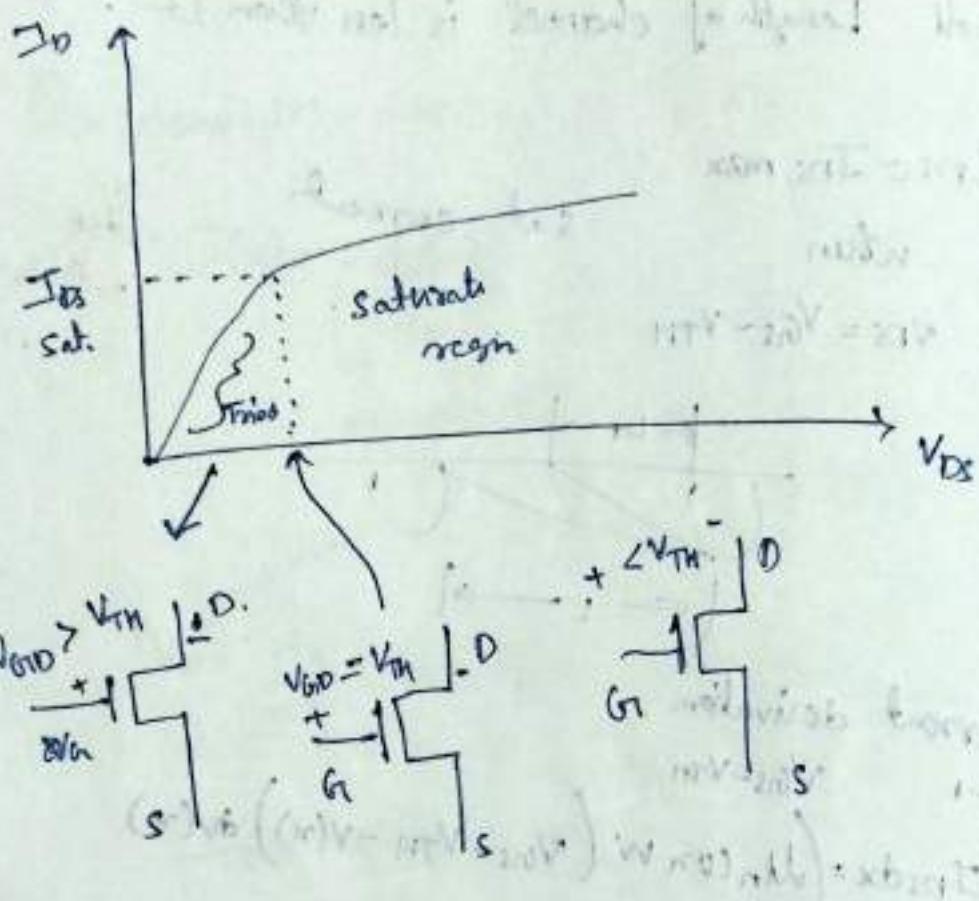
$L_1 \approx L$

not so deep.

for chanc
W, L → design parameters.

fix → technology Can't
parameters, chanc

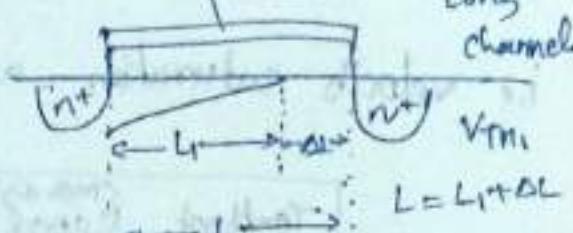




$$V_{DS} + V_{TH} = V_{GS}$$

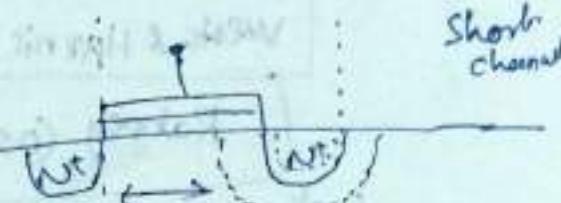
channel length modulation

$$I_{D,sat} = \frac{1}{2} \mu n C_{ox} \frac{W}{L_1} (V_{GS} - V_{TH})^2$$



$$= \frac{1}{2} \mu n C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_{TH})^2$$

$$= \frac{1}{2} \mu n C_{ox} \frac{W}{L(1 - \frac{\Delta L}{L})} (V_{GS} - V_{TH})^2$$



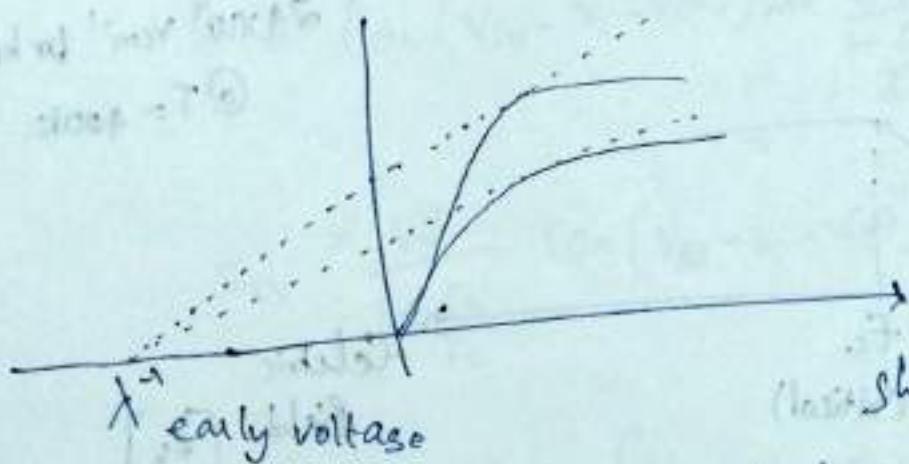
$$= \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \frac{\Delta L}{L}\right)$$

$V_{TH_1} > V_{TH_2}$
 $L - \Delta L \neq L$

$$I_{D,sat} = \frac{1}{2} \mu n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \left(1 + \lambda V_{DS}\right)$$

$$\frac{\Delta L}{L} \propto V_{DS}$$

$$\frac{\Delta L}{L} = \lambda V_{DS}$$



short length channel

$$E_h = \frac{V_{DS}}{L}, \quad E_v = \frac{V_{DD}}{t_{ox}}$$

vertical E field

horizontal E field

thickness of oxide

In short E_h, E_v both will cross each other, electron scatters.

Then electron cannot go beyond certain velocity i.e. velocity saturation and due to this sat current.

Tentbook Kangle (ablebita 3rd edition)
new edition
? Short chapt

Analysis & design of DiC, Hodges.

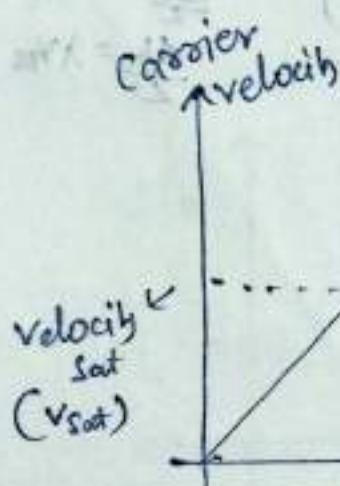
Weste, & Harris & Benjyjee CMOS VLSI Design

Raboeij (D Int Cts)

Hodges book

$$V = MeE = Me \frac{E_h}{1 + \frac{E_h}{E_c}}$$

$$1 + \frac{E_h}{E_c}; E_h < E_c$$



$$E_c = \begin{cases} 6 \times 10^4 \text{ Vcm}^{-1} \text{ for electrons} \\ 24 \times 10^4 \text{ Vcm}^{-1} \text{ for holes} \end{cases}$$

@ T = 400K

Electric field [E_h]

$$V_d = V_{sat}; E_h > E_c$$

$$V = V_{sat} \text{ when } E_h = E_c$$

$$\text{result} : V = Me \frac{E_c}{1 + \frac{E_c}{E_c}} = \frac{Me E_c}{2}$$

$$\left\{ \begin{array}{l} -E_c = \frac{2V_{ds}}{W} \\ \text{Me} \end{array} \right.$$

For linear mode of operation.

I_{DS} = charge density \times carrier velocity \times channel width.

✓
per unit area

$$\frac{Q}{m^2} \times \frac{m}{s} \cdot m$$

doubt.

I_{DS}

$$I_{DS} = \frac{Cox WE}{WE} (V_{GS} - V_T - v(x)) Me \frac{E_h}{1 + E_h} \cdot W$$

\downarrow
per area

$$\rightarrow Cox (V_{GS} - V_T - v(x)) Me \frac{E_h}{1 + E_h} W$$

$$\left\{ \begin{array}{l} E_h = \frac{dV(x)}{dx} \\ \cdot \end{array} \right.$$

$$I_{DS} = \frac{W}{1 + E_h} Cox [V_{GS} - V_T - v(x)] Me E_h$$

$$I_{DS} + \frac{E_h}{E_c} I_{DS} = W Cox [V_{GS} - V_T - v(x)] Me E_h$$

$$I_{DS} + \frac{\partial I_{DS}}{\partial x} \frac{dv(x)}{dx} = W Cox [V_{GS} - V_T - v(x)] Me \frac{dv(x)}{dx}$$

$$\int_0^{V_{DS}} I_{DS} dx + \int_0^{V_{DS}} \frac{I_{DS}}{E_c} dv(x) = \int_0^{V_{DS}} W Cox [V_{GS} - V_T - v(x)] Me dv(x)$$

$$- \int_0^{V_{DS}} W Cox Me v(x) dv(x)$$

$$\frac{I_{DSL}}{L} + \frac{I_{DS}V_{DS}}{E_c L} = M_e W C_{ox} (V_{GS} - V_T) V_{DS}$$

- $\frac{W C_{ox} M_e V_{DS}^2}{2}$

÷ by L to get $\frac{W}{L}$

$$I_{DS} \left(1 + \frac{V_{DS}}{E_c L} \right) = \frac{W}{L} M_e C_{ox} \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$

$$I_{DS} = \frac{W}{L} \cdot \frac{M_e C_{ox}}{1 + \frac{V_{DS}}{E_c L}} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

linear

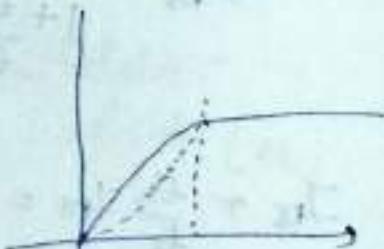
31/July/24

$$E_c = \frac{2V_{sat}}{M_e} \rightarrow V_{sat} = \frac{M_e E_c}{2}$$

$$I_{DS(\text{lin})} = \frac{W}{L} \frac{M_e C_{ox}}{1 + \frac{V_{DS}}{E_c L}} \left(V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \rightarrow ①$$

then $I_{DS(\text{sat})} = ?$

for saturation point.



$V_{DS,sat} = V_{GS} - V_T$
logarithmic

$$I_{DS} = ① \times W \times V_{sat}$$

$$I_{DS,sat} = C_{ox} (V_{GS} - V_T - V_{DS}) W \frac{M_e E_c}{2} \xrightarrow{V_{DS}} ②$$

$$I_{DS(\text{lin})} = I_{DS}$$

(1) = (2)

$$\frac{W}{L} \frac{\text{McCon}}{1 + \frac{V_{DS,\text{sat}}}{E_c L}} (V_{GS} - V_T - \frac{V_{DS,\text{sat}}}{2}) V_{DS,\text{sat}} = \text{McCon} (V_{GS} - V_T - \frac{V_{DS,\text{sat}}}{2})$$

~~$\frac{W}{L} \text{McCon}$~~

$$\Rightarrow \left(V_{GS} - V_T - \frac{V_{DS,\text{sat}}}{2} \right) V_{DS,\text{sat}} = K \cdot \left(\frac{E_c L + V_{DS,\text{sat}}}{E_c K} \right) (V_{GS} - V_T - \frac{V_{DS,\text{sat}}}{2}) \frac{E_c}{2}$$

$$(V_{GS} - V_T) V_{DS,\text{sat}} - \frac{V_{DS,\text{sat}}^2}{2} = \frac{E_c L}{2} (V_{GS} - V_T) + \frac{V_{DS,\text{sat}} (V_{GS} - V_T)}{2} - \frac{E_c L V_{DS,\text{sat}}}{2} - \frac{V_{DS,\text{sat}}^2}{2}$$

$$\frac{(V_{GS} - V_T) V_{DS,\text{sat}}}{2} = \frac{E_c L}{2} (V_{GS} - V_T - \frac{V_{DS,\text{sat}}}{2})$$

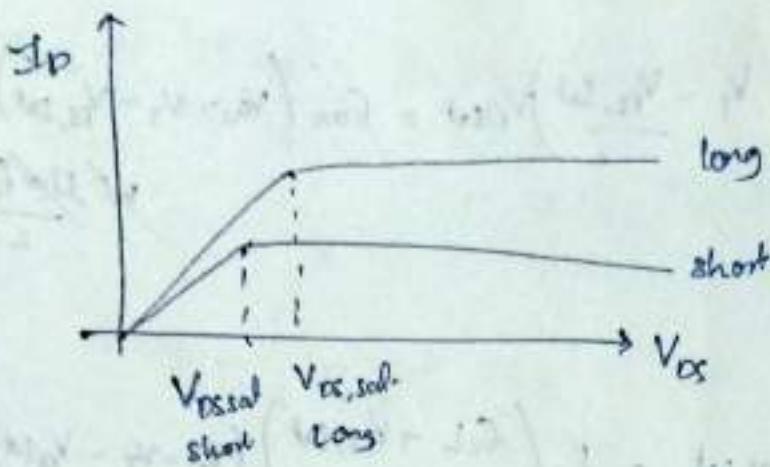
Hodges
numerical
eg:

$$V_{DS,\text{sat}} = \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L} \quad \rightarrow ③$$

Short channel has lower Sat voltage than longer channel.

$$\therefore \text{for short channel} \quad V_{DS} \geq \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L} ; \text{ sat}$$

$$V_{DS} < \frac{(V_{GS} - V_T) E_c L}{(V_{GS} - V_T) + E_c L} , \text{ linear}$$



→ Short saturate early than long.

$$I_{DS, \text{sat}} = W V_{GS, \text{sat}} C_{ox} \left(\frac{V_{GS} - V_T}{C_{GS}} - \frac{(V_{GS} - V_T) E_C L}{(V_{GS} - V_T) + E_C L} \right)$$

$$I_{DS, \text{sat}} = W V_{GS, \text{sat}} C_{ox} \frac{(V_{GS} - V_T)^2}{(V_{GS} - V_T) + E_C L}$$

for short channel

Try to fit this in long.

For a long channel devices, $\boxed{E_C L \gg (V_{GS} - V_T)}$

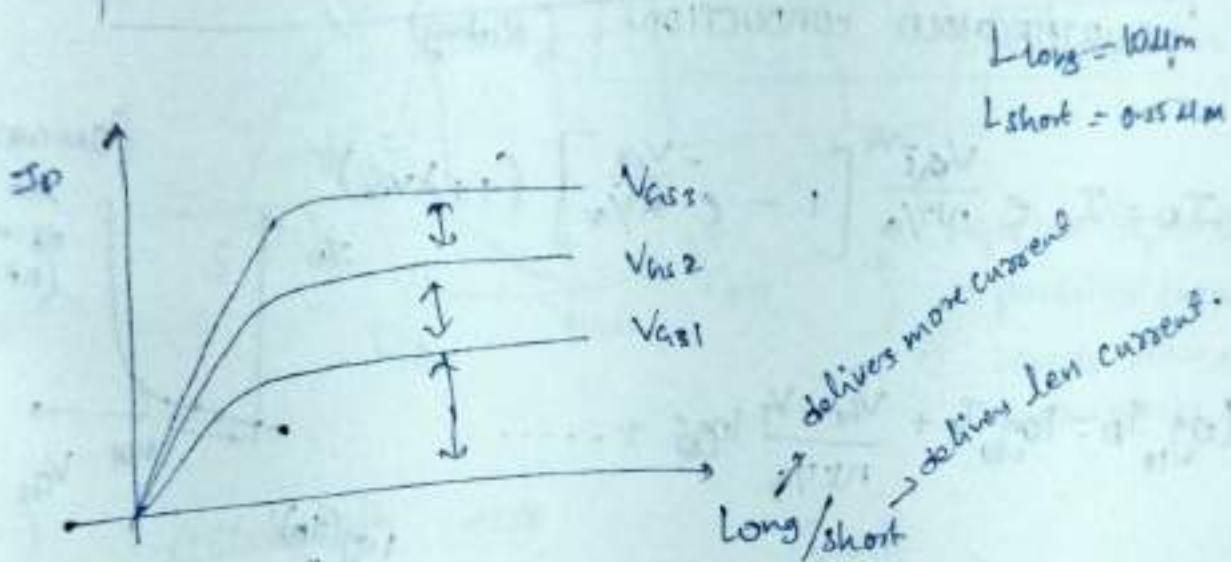
$$I_{DS, \text{sat}} = W \frac{M e E_C}{2} C_{ox} \frac{(V_{GS} - V_T)^2}{E_C L}$$

$$\boxed{I_{DS, \text{sat}}^{\text{long}} = \frac{1}{2} M e C_{ox} \frac{W}{L} (V_{GS} - V_T)^2} \quad (5)$$

For a short channel devices, $E_C L \ll (V_{GS} - V_T)$

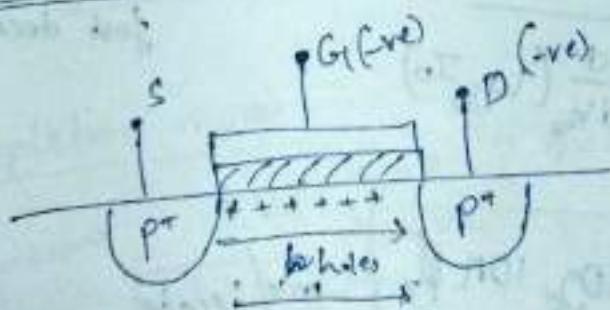
$$I_{DS,sat} = \frac{W \cdot C_{ox} \cdot V_{DS} \cdot \text{Cos}(V_{GS} - V_T)}{(V_{GS} - V_T)^2}$$

$$I_{DS,sat} = W \cdot C_{ox} \cdot \text{Cos}(V_{GS} - V_T) \quad \rightarrow (1)$$



diff in long channel is more due to Quadratic factor
 diff in short channel is less & linear.

PMOS Transistor



if $I_{DS}=0$, $V_{GS} > V_{TP}$
 when V_{TP} is -ve

$$= \mu_p C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

N-Type

Linear

$$V_{GS} < V_{TP}$$

$$V_{DS} > V_{GS} - V_{TP}$$

$$V_{GS} - V_D \leq V_{TP}$$

$$V_{GS} - V_D \leq V_{TP}$$

$$V_{GS} - V_{TP} \leq V_{DS}$$

$$\Rightarrow V_{DS} \geq V_{GS} - V_{TP}$$

$$I_{SP,sat} = \frac{1}{2} \mu_p C_{ox} \frac{W}{L} (V_{GS} - V_{TP})^2$$

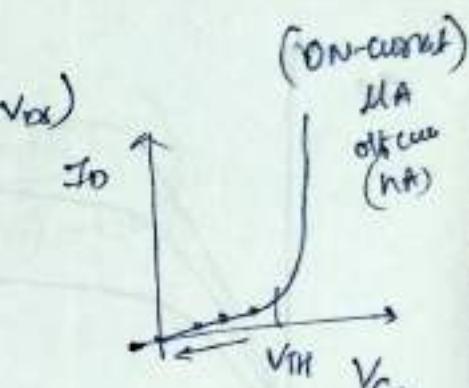
$$V_{GS} < V_{TP}$$

$$V_{DS} \leq V_{GS} - V_{TP}$$

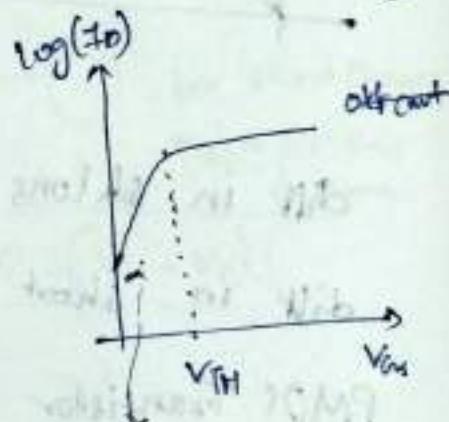
SUBTHRESHOLD CONDUCTION (Rabey)

$$I_D = I_s e^{\frac{V_{GS}-V_T}{nKT/q}} \left[1 - e^{-\frac{V_{DS}}{nKV/q}} \right] (1 + \lambda V_{DS})$$

$$\log_{10} I_D = \log_{10} I_s + \frac{V_{GS} - V_T}{nKT/q} \log_{10} e + \dots$$



$$\frac{d}{dV_{GS}} (\log_{10} I_D) = \frac{\log_{10} e}{nKT/q} = \frac{\log_{10} e}{n \phi_F}$$



Subthreshold slope $S = \frac{1}{\frac{d}{dV_{GS}} (\log_{10} I_D)}$

fast decay is preferred

$$S = \log_{10} \frac{10n\phi_F}{kT} \text{ mV/decade}$$

$S_{ideal} = 60 \text{ mV/decade}$ best case

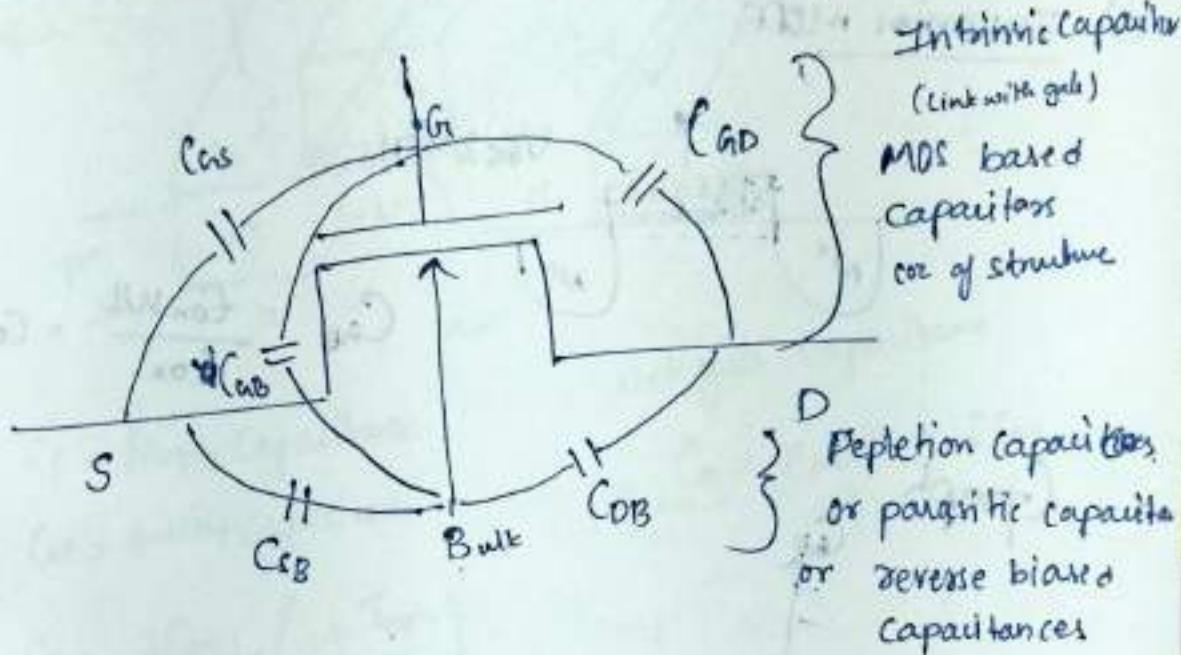
$S_{spread} = 20 \text{ mV/decade}$

for 90mV decrease in V_{GS} /decade change

Assignment DIBL, Punch-through, Hot-electron effect.

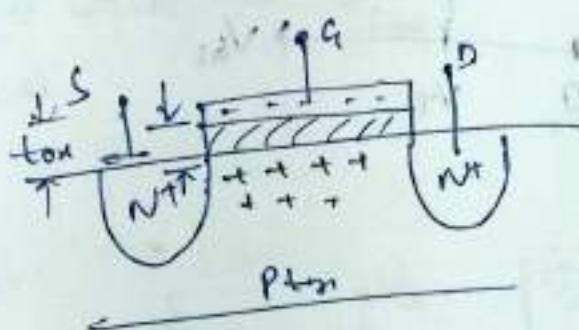
MOSFET capacitances

essential capacitive "coz" of proper functioning.



① Accumulation mode

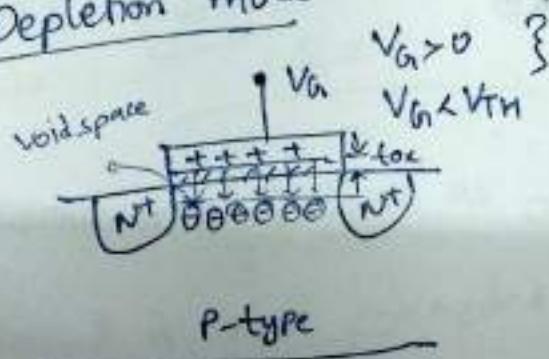
(Werbe Harris)



$$V_{GS} < 0$$

$$\textcircled{1}. C_{GS} = \frac{\epsilon_{ox} WL}{t_{ox}} = C_0$$

② Depletion mode

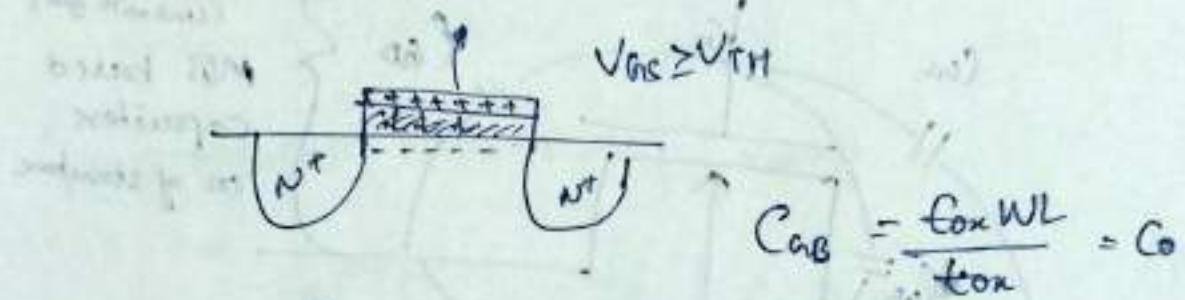


$$\left. \begin{array}{l} V_G > 0 \\ V_G < V_{TH} \end{array} \right\} 0 < V_{GS} < V_{TH}$$

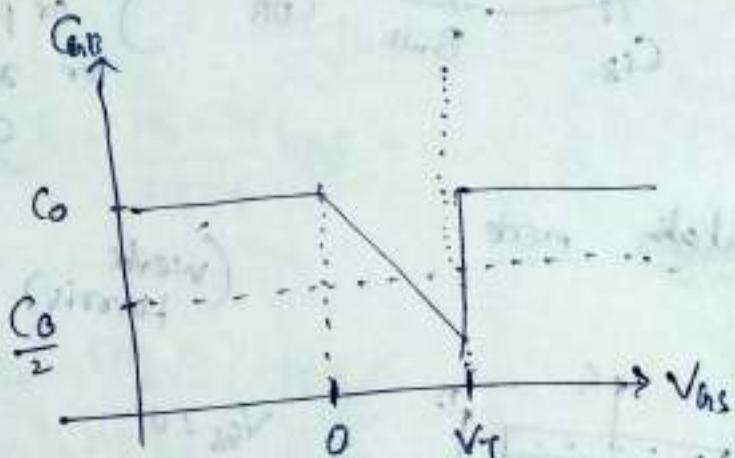
$$C_{GS} = \frac{\epsilon_{ox} WL}{>t_{ox}} < \frac{C_0}{2}$$

⇒ Oxide capacitance is in series with the depletion capacitance.

③ Inversion mode



Graph



④ Cut-off mode

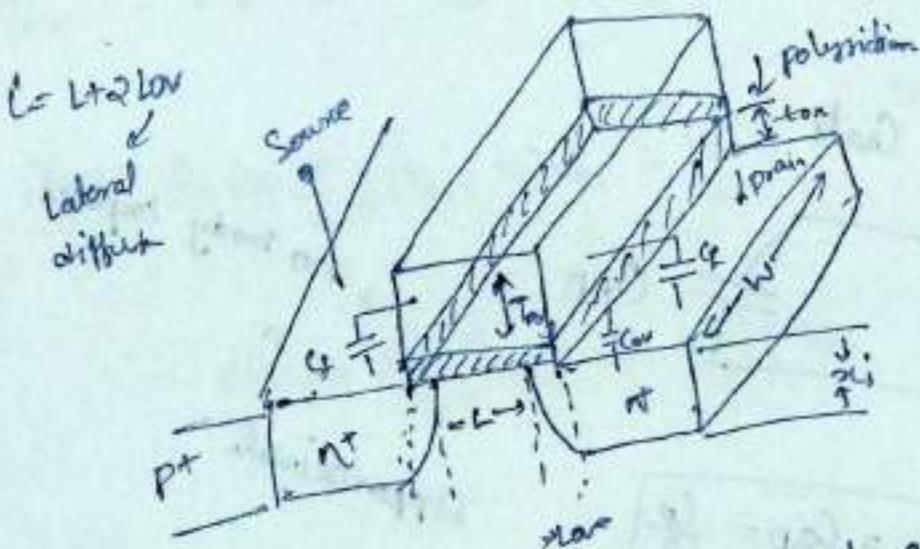
- * $V_{ds} = 0$

- * channel is not inverted

- * $\text{obs } C_{ds} = C_0 = \frac{C_{ox}WL}{t_{ox}}$

- * $C_{ds} = 0, C_{gd} = 0$

Sat Aug 24



C_f = fringing Capacitance

C_{ov} = overlap capacitance

$$C_f = \frac{2\epsilon_0 \alpha}{\pi} \ln \left(1 + \frac{T_{poly}}{t_{ox}} \right)$$

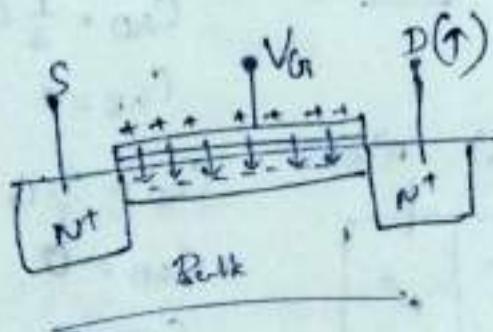
Net gate capacitance

$$C_n = C_{ov}WL + 2C_f$$

Cutoff
Cut-off $C_G C_{ov} = C_0 = \frac{\epsilon_0 WL}{t_{box}}$
($V_{GS} \approx 0$)

Linear

Grate
 $\frac{1}{1} \frac{1}{1} \frac{1}{1} \frac{1}{1} \frac{1}{1}$
 Bulk

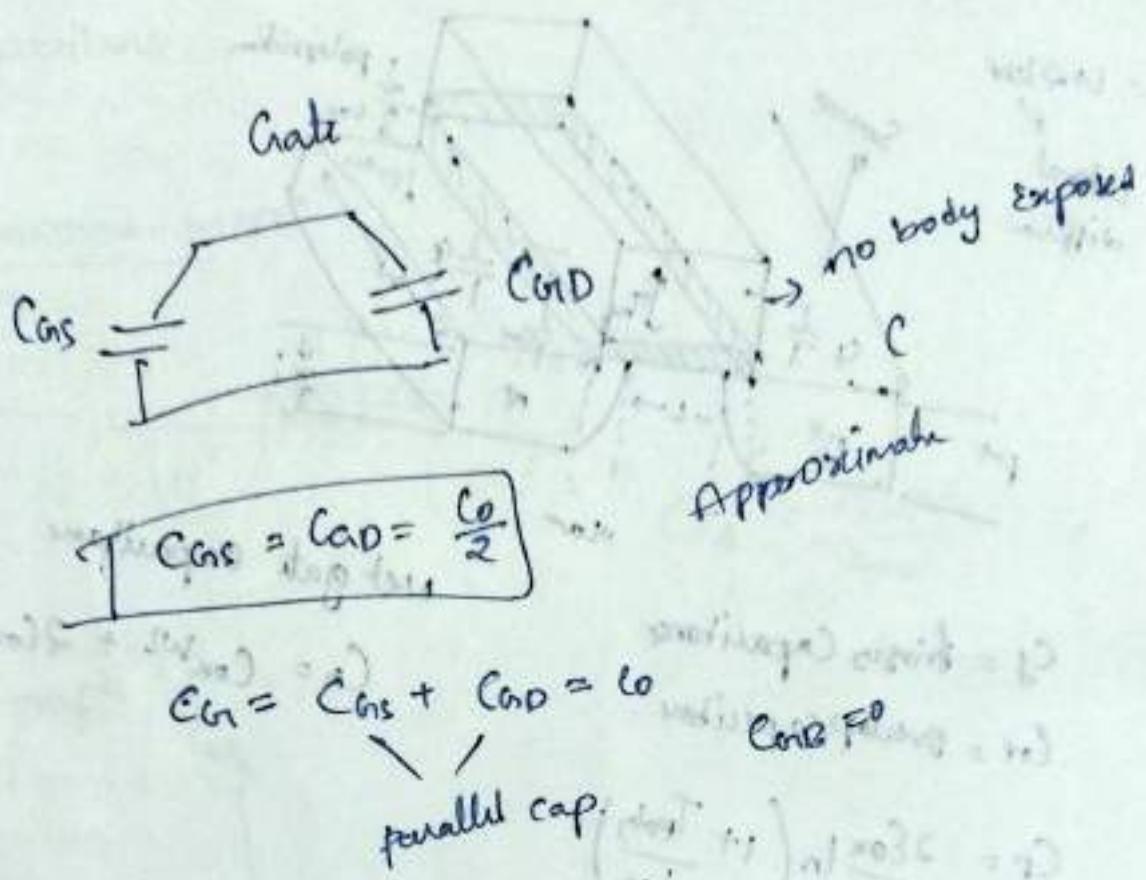


no body is exposed
 $\therefore C_{GB} = 0$

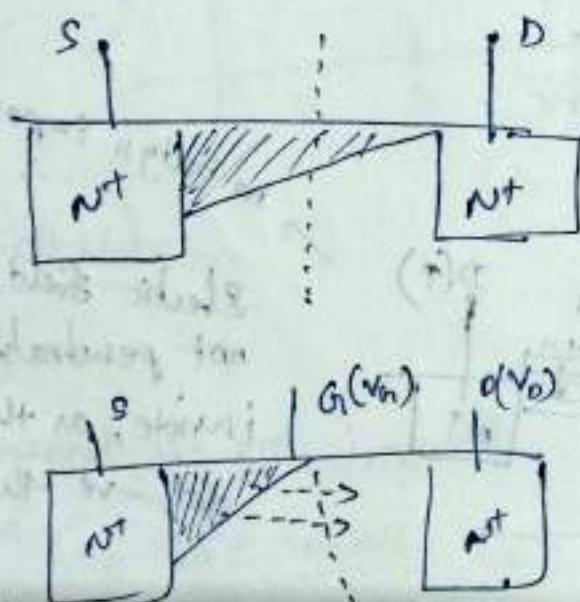
electric field line can
 not penetrate deeper
 inside, as they already
 got -ve there itself.

- Channel inverts & serves as a good conducting bottom plate.
- Channel is now connected to the drain & source, rather than the body.

→ channel charge is roughly shared b/w source & drain



Saturation



$$C_{GS} = \frac{2}{3} C_0$$

$$C_{GD} = \frac{1}{3} C_0$$

$$C_{AB} = 0$$

$$C_{GS} = \frac{2}{3} C_0$$

$$C_{GD} = 0$$

$$C_{AB} = 0$$

total

$$Q_{\text{tot}} = C_{\text{tot}} V_{\text{tot}} \approx C_{\text{ox}} W \int_0^L (V_{GS} - V_T - V(x)) dx \quad \text{--- (1)}$$

$$I_{DS} = M_n C_{\text{ox}} \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right).$$

linear
linea ~~I_{DS}~~
 \downarrow
sat I_{DS}

$$V_{GS} - V_T - \frac{V_{DS}}{2} = V_{GS} - V_T - V_s - \left(\frac{V_D - V_s}{2} \right)$$

$$= V_{GS} - V_T - \left(\frac{V_D + V_s}{2} \right)$$

~~($V_D = V_s$)~~

$V(x)$

$$I_{DS, \text{lin}} = M C_{\text{ox}} \frac{W}{L} \left(V_{GS} - V_T - V(x) \right) V_{DS}.$$

$$= M C_{\text{ox}} W \left(V_{GS} - V_T - V(x) \right) \left(\frac{V_{DS}}{L} \right) \frac{dV(x)}{dx}$$

$$dx = \frac{M_n C_{\text{ox}} W}{I_{DS, \text{lin}}} \left(V_{GS} - V_T - V(x) \right) dV(x) \quad \text{--- (2)}$$

(2) in (1)

$$Q_{\text{tot}} = \frac{M_n C_{\text{ox}} W}{V_D \approx V_{GS, \text{sat}}} \left(V_{GS} - V_T - V(x) \right) \frac{M C_{\text{ox}} W}{I_{DS, \text{lin}}} \left(V_{GS} - V_T - V(x) \right) dV(x)$$

$V_D \approx V_{GS, \text{sat}}$

$V_C \approx 0$ @ sat.

\downarrow
I_{DS, sat}

$$= \frac{dW^2(\text{con})}{\frac{1}{2} dC_{\text{sat}} \frac{W^2}{L} (V_{G_S} - V_T)^2} \int_0^{V_{G_S, \text{sat}}} (V_{G_S} - V_T - v(z))^2 dv(z)$$

$$= - \frac{2WL \text{con}}{(V_{G_S} - V_T)^2} \left[\frac{(V_{G_S} - V_T - v(z))^3}{3} \right]_0^{V_{G_S, \text{sat}}}$$

$$= + \frac{2WL \text{con}}{3(V_{G_S} - V_T)^2} \cdot \left[(V_{G_S} - V_T - V_{\text{sat}})^3 - (V_{G_S} - V_T)^3 \right] \approx 0$$

$$\Rightarrow \frac{2}{3} [WL \text{con}] (V_{G_S} - V_T)$$

$$\text{QV: } \Theta_{\text{tot}} = \frac{2}{3} C_0 (V_{G_S} - V_T)$$

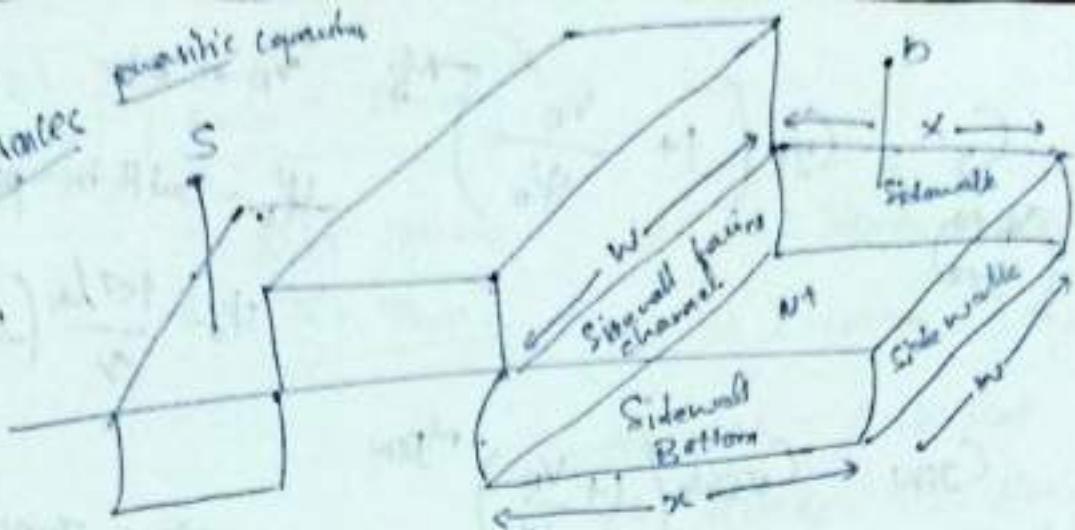
Cutoff linear sat

$$C_{\text{as}} \quad C_0 \quad 0 \quad 0$$

$$C_{\text{as}} : 0 \quad \frac{C_0}{2} \quad \frac{2}{3} C_0$$

$$C_{\text{ao}} \quad 0 \quad \frac{C_0}{2} \quad 0 \text{ to } \frac{1}{3} C_0$$

Depletion Capacitance plastic capacitor



$$C_{SB}$$

$$C_{DD}$$

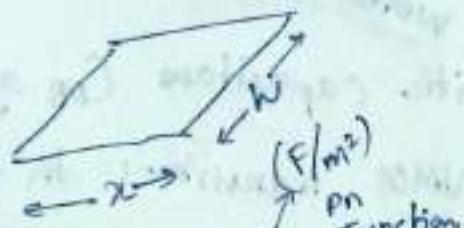
↑
as minor
possible

$$\text{Area} = \pi k W x$$

$$\text{perimeter} = 2(w+x)$$

Bottom plate Capacitance +

Sidewall Capacitance



$$C_{bottom} = C_{J,0} \frac{x}{w} (w x)$$

zero biased capacitance per unit area



$$C_{sidewall,0} = C_{J0} \left(x_j \frac{2}{w+x} \right)$$

$$= [C_{J0} x_j] \frac{2}{w+x}$$

$$= C_{JSW,0} \frac{2}{w+x}$$

$\frac{F}{m}$

Now

$$C_N = C_{bottom} + C_{sidewall}$$

$$V_D > 0$$

$$V_S = 0$$

$$= (C_{J0} \frac{w}{w+x}) + C_{JSW,0} \frac{2}{w+x}$$

$$B.P.S = \frac{2}{w+x}$$

$$= C_{J0} \frac{w}{w+x} + C_{JSW} \frac{2}{w+x} + C_{JSW} \frac{w}{w+x}$$

+ main

Beneath the
gate.

$$C_J = C_{J0} \left(1 + \frac{V_D}{\psi_0} \right)^{-M_J} \quad V_D \text{ or } \psi_V$$

ψ_0 : built-in potential
 $(V_D \neq 0)$
 $V_S \neq 0$

ψ_0 : built-in potential

$$\psi_0 = \frac{kT \ln}{n} \left(\frac{n n_D}{n_i^2} \right)$$

$$C_{JSW} = C_{JSW0} \left(1 + \frac{V_D}{\psi_0} \right)^{-M_{JSW}}$$

all 3-sides.

M_J = Junction grading
 M_{JSW} Coefficient
 M_{JSW0} Coefficient

$$C_{JSWH} = C_{JSWH0} \left(1 + \frac{V_D}{\psi_0} \right)^{-M_{JSWH}}$$

Gate

Problem

WertenHarris

- Calculate the diffusion parasitic capacitance C_{DB} of the drain of a circuit sized NMOS transistors in a 180nm process, when the drain is @: a) 0V b) $V_{PD} = 1.8V$
 Assume that the substrate is grounded and a unit size diffusion contact is $w \lambda \times 5\lambda$ ($r_s = \frac{w}{4}$)
 where λ is half the feature size of the process.

Transistor size parameters are:

$$C_{J0} = 0.98 \text{ fF}/\mu\text{m}^2$$

$\therefore F_{D0} = 10^{15}$

$$M_J = 0.36 \quad C_{JSW0} = 0.22 \text{ fF}/\mu\text{m}$$

$$M_{JSW} = 0.10 \quad C_{JSWH0} = 0.35 \text{ fF}/\mu\text{m}$$

$$M_{JSWH} = 0.11; \quad \psi_0 = 0.75 @ 200mV$$

$$\left[\begin{array}{l} L_{\min} = 2\lambda \\ \lambda = \frac{1}{2} L_{\min} \end{array} \right] \quad \left[\begin{array}{l} L_{\min} = 180 \text{ nm} \end{array} \right]$$

$$\therefore 2\lambda = 180 \text{ nm}$$

$$1\lambda = 90 \text{ nm}$$

$$W = 4\lambda = 360 \text{ nm} \approx 0.36 \mu\text{m}$$

$$X = 5\lambda = 450 \text{ nm} \approx 0.45 \mu\text{m}$$

$$A_S = W X = 0.362 \mu\text{m}^2$$

$$P_S = \rho (W + X) = 1.62 \text{ N/m}$$

$$P_S \cdot W = 1.26 \text{ Nm}$$

a) $V_D = 0 \text{ V}$

$$C_{OB} \Big|_{V_D=0} = C_{J0} (1 + 0) + C_{JCWD} (P_S - w) + C_{JSWH} (w)$$

$$\Rightarrow 0.98 \times 0.162 + 0.22 \times 1.26 + 0.33 \times 0.36 = 0.55 \text{ fF}$$

b) $V_D = 1.8 \text{ V}$

$$C_{OB} \Big|_{V_D=1.8} = 0.98 \left(1 + \frac{1.8}{0.75} \right)^{-0.36} \times 0.162 + 0.22 \left(1 + \frac{1.8}{0.75} \right)^{-0.10} \times 1.26 + 0.33 \left(1 + \frac{1.8}{0.75} \right)^{-0.11} \times 0.36$$

$$= 0.44 \text{ fF}$$

Chapter 2 Werner Harris, Exercise Söhe #1 et..

7/Aug/24
 Q) An NMOS transistor has a threshold voltage of 0.4V and a supply voltage of $V_{DD} = 1.2V$. A circuit designer is evaluating a proposal to reduce V_t by 100mV to obtain faster transistors. Assume $\lambda=0$

Two terms

- a) By what factor would the saturation current increase @ $V_{GS}=V_{DS}=V_{DD}$ if the transistor were ideal?
- b) By what factor would the subthreshold leakage current increase @ room temperature @ $V_{GS}=0$? Assume $n=14$
- c) By what factor would the subthreshold leakage current increase @ 120°C? Assume the threshold voltage is independent of temperature

$$I_D = I_S e^{\frac{V_{GS}-V_T}{nKT/q}} \left[1 - e^{-\frac{V_{DS}}{KT/q}} \right] (1 + \lambda V_{DS})$$

Ans $V_T |_{25^\circ C + 273} = \frac{KT}{qV} = 0.0256V$
 $= 29.8K$

$$V_T = \left(\frac{KT}{qV} \right)$$

a) New: $V_T = V_{T_1}$
 $= 0.4V - 0.1V = 0.3V$

origin $V_T = V_{T_2}$
 $= 0.4V$

$$\frac{I_{DSS1}}{I_{DSS2}} = \frac{(V_{GS} - V_{T_1})^2}{(V_{GS} - V_{T_2})^2} = \frac{(1.2 - 0.3)^2}{(1.2 - 0.4)^2} = 1.2556$$

$$b) \frac{I_{D1}}{I_{D2}} = \frac{e^{\frac{V_{GS} - V_T}{nKT/V}}}{e^{\frac{V_{GS} - V_T}{nKT/V}}} = \frac{e^{-\frac{0.3}{1.4 \times 0.0256}}}{e^{-\frac{0.4}{1.4 \times 0.0256}}} = 16.2839$$

$$c) V_T|_{120^\circ C} = \frac{kT}{q} = 0.0339 \text{ V}$$

$$\frac{I_{D1}}{I_{D2}} = \frac{e^{\frac{-0.3}{1.4 \times 0.0339}} \left(1 - e^{\frac{-1.2}{0.0339}}\right)}{e^{\frac{-0.4}{1.4 \times 0.0339}} \left(1 - e^{\frac{-1.2}{0.0256}}\right)} = 126.40$$

MOSFET scaling ~~in~~ (EANh) Book

- * Improvement in process technology enables fabrication of MOSFET with smaller dimensions.
- ⇒ improves packing density, functional density.
- ⇒ reduction of Si area

scaling factor.

$$w/L \cdot w \rightarrow \frac{w}{S} \cdot L \rightarrow \frac{L}{S_1} \quad (S > 1)$$

* CONSTANT FIELD SCALING (FULL SCALING)

* CONSTANT VOLTAGE SCALING.

i) Constant Field scaling.

$$\text{electric Field} = \frac{\text{Voltage}}{\text{distance}_{fox}} = \frac{\text{Voltage}}{\text{distance}/c}$$

$N_{A,S} \leftrightarrow S_{NA}$ → acceptor conc
 $N_{D,S} \leftrightarrow S_{ND}$ → donor conc

If we increase electric field then there will be breakdown

$$EV = \frac{V_{GS}}{\frac{t_{ox}}{L}} , \quad EH = \frac{V_{DS}}{L} \quad t_{ox}, L, W \leftarrow \times \frac{1}{S}$$

$\frac{W}{L}$ ratio is preserved after scaling.

1) $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \rightarrow C_{ox,s} = \frac{\epsilon_{ox}}{t_{ox}/s} = sC_{ox}$ (per unit)

2) $C_{ox}' = \frac{\epsilon_{ox} A}{t_{ox}} \Rightarrow C_{ox,s}' = \frac{1}{s} C_{ox}'$

3) process transconductance parameter = $M_n C_{ox}$

$$k_n = M_n C_{ox}$$

$$k_{ns} = M_n s C_{ox}$$

$$= S k_n$$

4) $I_{DS(\text{lin})} = k_n \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$

$$= \frac{S k_n}{S^2} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

$$I_{DS(\text{lin}),s} = \frac{I_{D,\text{lin}}}{S}$$

$$7) I_{DS, \text{sat}} = k_m \frac{W}{L} (V_{GS} - V_T)^2$$

$$I_{DS, \text{sat}, s} = \frac{I_{DS, \text{sat}}}{s}$$

$$6) P = V \cdot I$$

$$\Rightarrow P_s = \frac{P}{s^2}$$

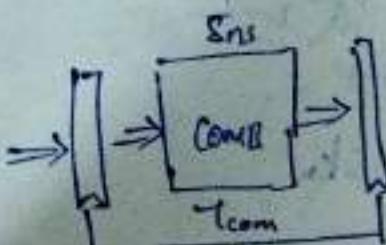
$$7) \text{Power density} = \frac{\text{Power}}{\text{Area}}$$

$$TP_{DS} = PD$$

$$8) \text{Current density} / \cancel{s} = \frac{I}{A}$$

$$(CD\cancel{A})_s = s(CD\cancel{A})$$

$$9) R = \frac{V_{DD}}{I_{DS}} \Rightarrow R_s \approx R$$



$$10) \text{Gate delay} \Rightarrow \tau = RC.$$

$$\tau_s = \frac{\tau}{s} = \frac{R.C}{s}$$

\therefore close frequency improves.

FLFLFLFLFL
 $\therefore T_{CE} \geq T_{ComB}$

$$ii) P_{\text{dynamic}} = C V_{DD} f_{CK}$$

$$= \frac{C}{S} \cdot \frac{V_{DD}^2}{S^2} f_{CK}$$

$$= \frac{1}{S^3} P_{\text{dynamic}}$$

(why) we need to scale
all connected devices
like, CPU, keyboard,
monitor, printer
for proper communication

Constant voltage scaling

$$N_{AS} = S^2 N_A$$

$$N_{OS} = S^2 N_D$$

$V_{DS}, V_{DD}, V_T \leftarrow$ remain unchanged

$$t_{on}, w, L \leftarrow \frac{1}{S}$$

$$\boxed{S > 1}$$

$$f). P_S = SP.$$

$$i) C_{ox}, s = s C_{ox}$$

$$j) R_s = \frac{R}{S}$$

$$k) C_{ox} = \frac{1}{S} C_{ox}$$

$$l) \gamma_s = \frac{\gamma}{S^2} \quad (\text{higher dielectric})$$

$$m) \left(\frac{W}{L} \right)_s = \left(\frac{W}{L} \right)$$

$$n) \text{Power density}_s = S^3 (PD)$$

$$o) I_{in} = S I_{in}$$

$$p) \text{Current density}_s = \frac{A}{S^2} J_D = S^3 (CD)$$

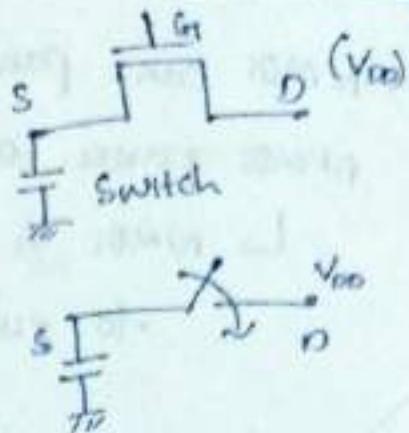
$$q) I_{DS(\text{lim},s)} = S I_{DS(\text{lim})}$$

{change
current source

$$r) I_{DS(\text{sat})} = S I_{DS(\text{sat})}$$

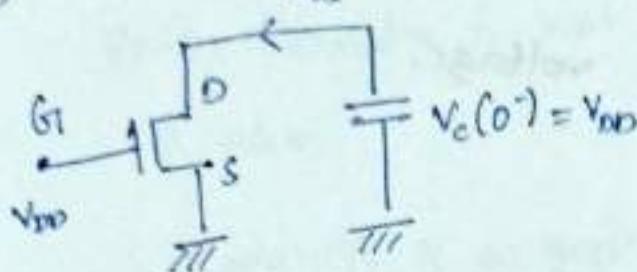
switching properties of MOSFETs.

→ PNP Transistors



DC characteristics

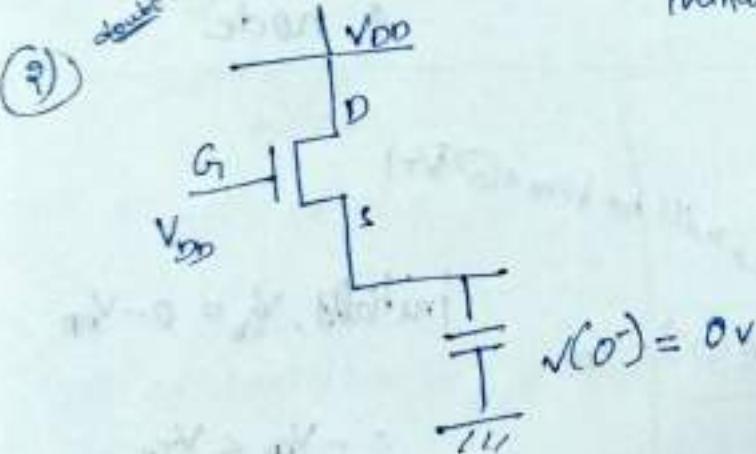
① $I_{DS} \rightarrow$ discharge current.



$$V_{GS}(L) = V_{DD} > V_{TN} \text{ (NMDOS: ON)}$$

→ initially if it was V_{DD} so I_{DS} will in sat. \therefore faster discharge

→ later V_{DD} decreases to discharge slow.



$$\begin{aligned} \text{initial } V_{DS} &= V_D - V_S \\ &= V_{DD} - 0 \\ &= V_{DD} \end{aligned}$$

$$\begin{aligned} V_{GS} - V_T &= V_G - V_S - V_T \\ &= V_{DD} - 0 - V_T \\ &\therefore V_{DD} - V_T \end{aligned}$$

$$V_{GS} > V_T$$

$$V_{DD} - V_T > V_S$$

when S is @ $V_{DD} - V_T$

$$V_{DD} - V_C > V_T$$

$$V_S \leq V_{DD} - V_T$$

$$\begin{aligned} V_{HC} &= V_{DD} - (V_{DD} - V_T) \\ &\approx V_T \end{aligned}$$

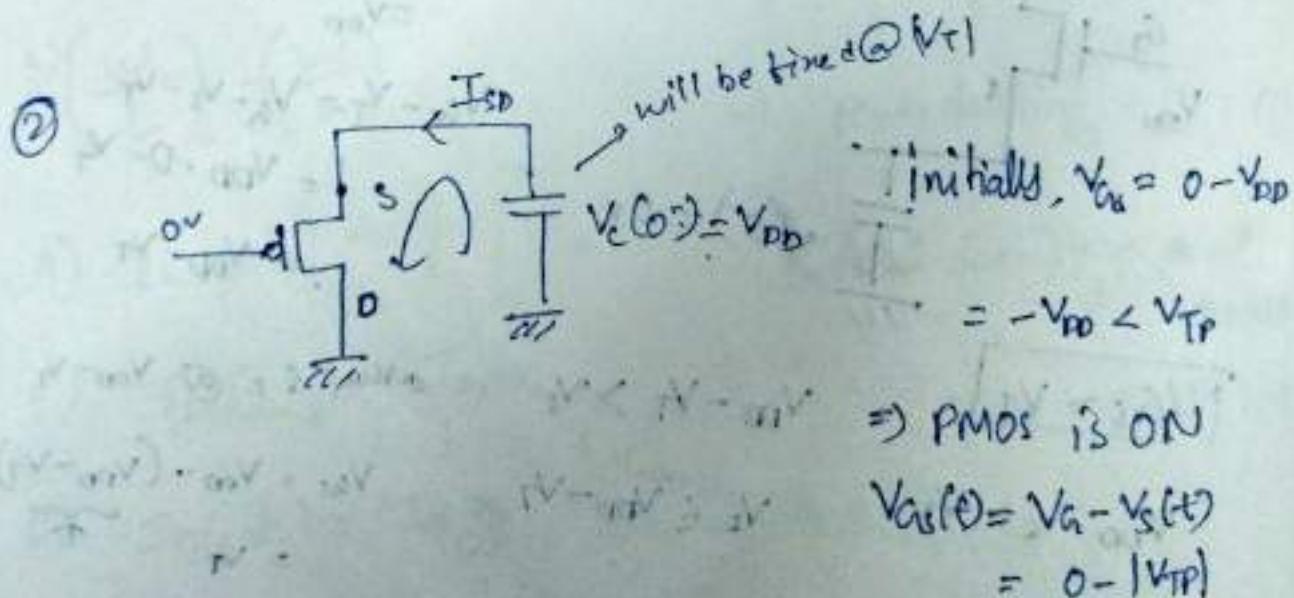
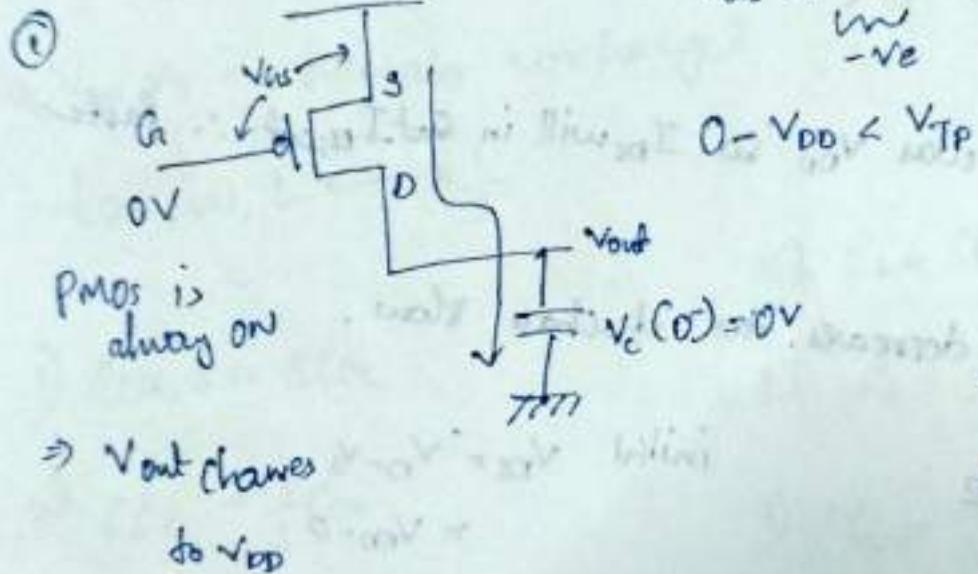
→ NMOS can pull logic 0 completely.

NMOS pulls logic 1 poorly.

↳ NMOS is not a good candidate
to pull up a node voltage.

↳ NMOS is a good candidate to
discharge a node voltage.

PMOS Transistor



$$\textcircled{a} \quad V_{GS}(t) = V_{TP}$$

$$\begin{aligned} V_{GS} &= 0 - 0.3 \\ &= -0.3 \\ &> V_{TP} \\ &\approx -0.4. \end{aligned}$$

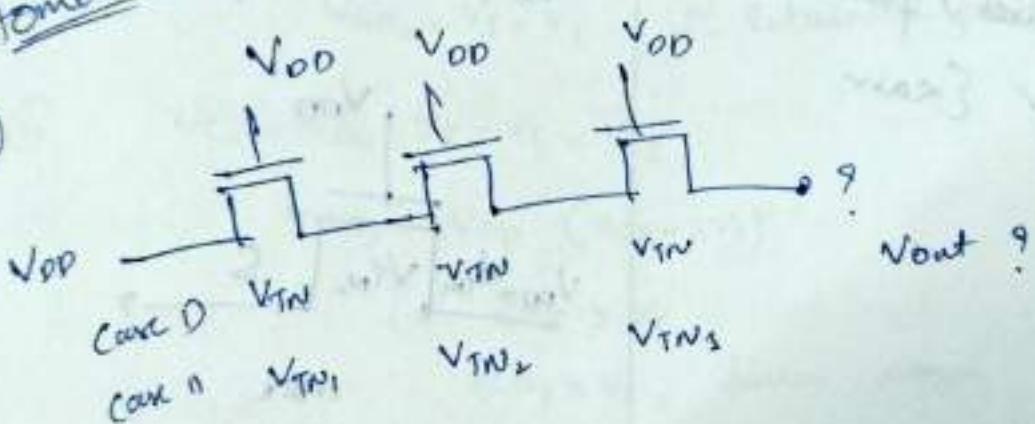
This situation can never arise as PMOS will turn off.

PMOS transistor is not a good candidate for discharging a node.

→ however, it is a good candidate for charging a node.

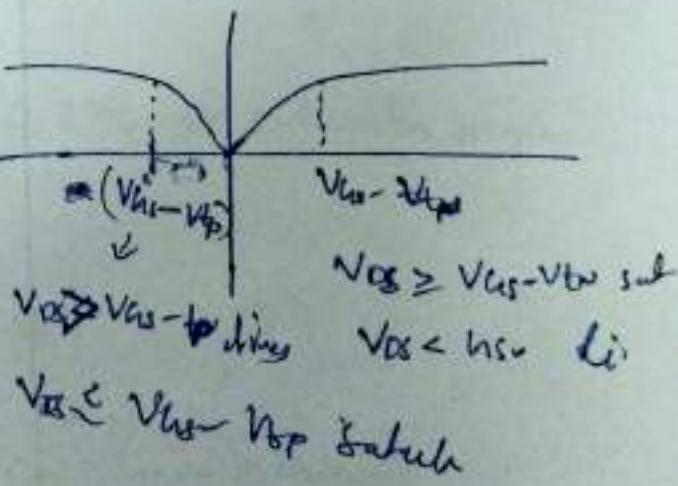
Homework

\textcircled{b}



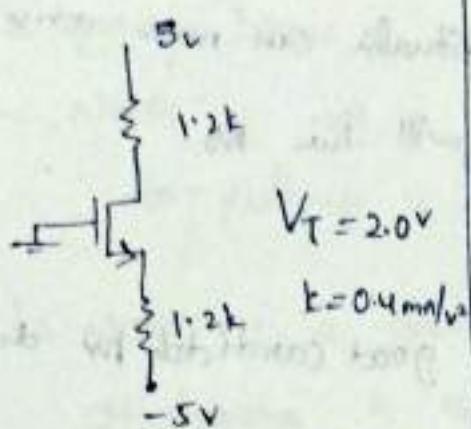
NMOS

PMOS



Practice problem

①



Assume Saturation.

$$\begin{aligned} V_{DS} &> V_{DS} \\ V_{DS} &> V_{DD} - V_T \end{aligned}$$

f=NP-MOS, NMOS in
Series / Parallel
for Exam

Sire Solving problem

$$V_{GSAT} > V_{TN}$$

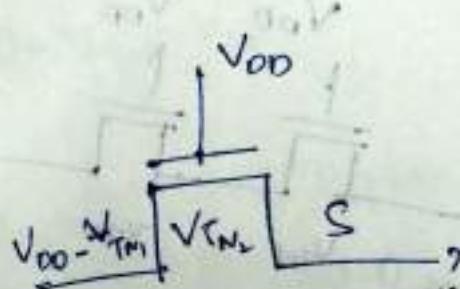
$$V_{DD} - V_{SA} > V_{TN}$$

$$V_{DD} - V_{TN} > V_{SA}$$

$$V_{SA} \leq V_{DD} - V_{TN}$$

for V_{T1}, V_{T2}, V_{T3}

$$V_{DD} - \max(V_{TN1}, V_{TN2})$$



max

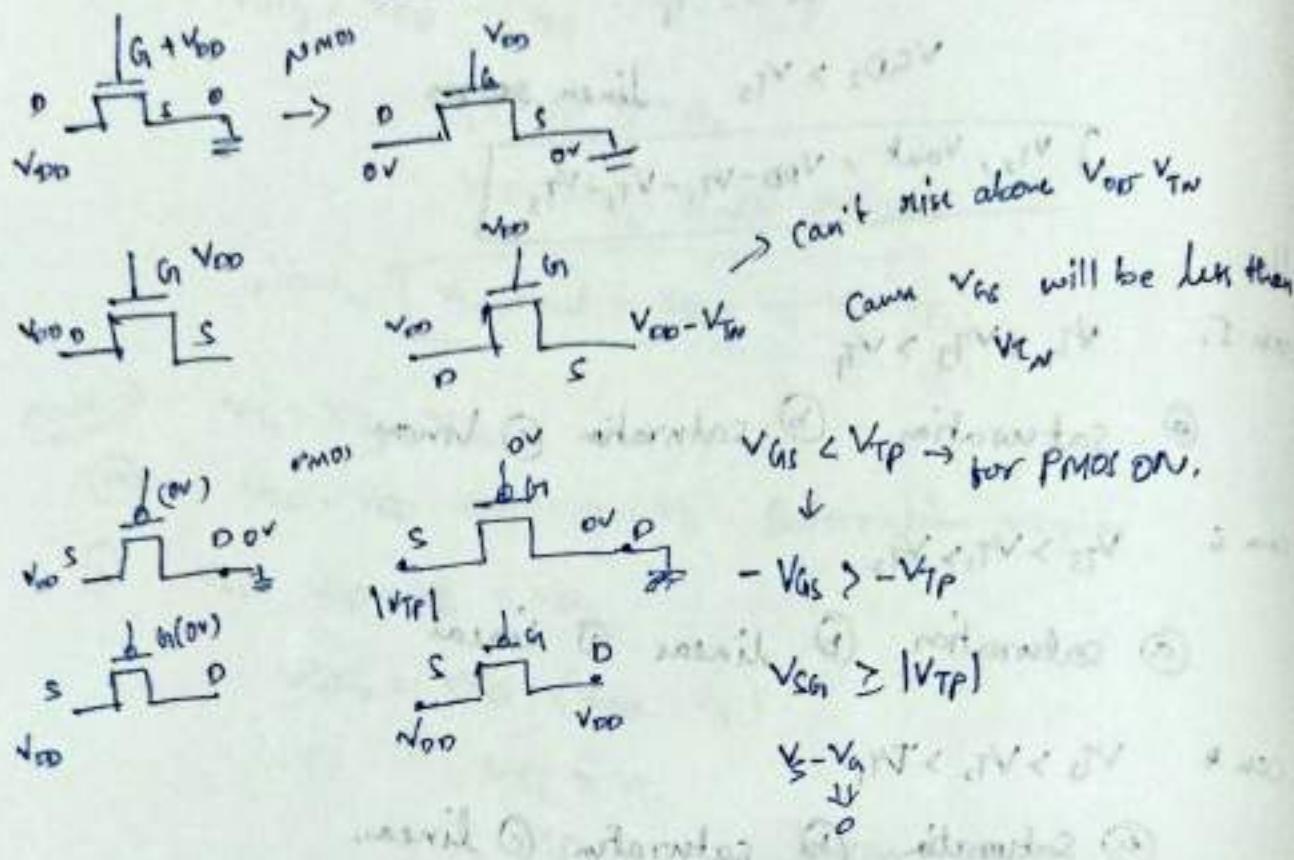
$$\bullet V_{DD} - V_{TN2}$$

or

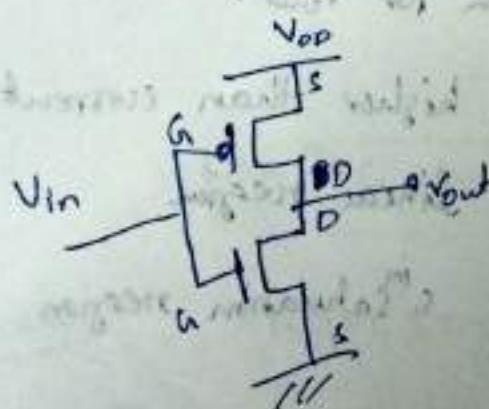
$$\min(V_{DD} - V_{TN1}, V_{DD} - V_{TN2})$$

$$V_{DD} - \max(V_{TN1}, V_{TN2}, V_{TN3})$$

12 Aug 29

RecapCMOS Inverter

V_{in}	V_{out}
0	1 (PMOS) \rightarrow connected V_{DD}
1	0 (NMOS) \rightarrow connected ground



When $V_{in} = 0$, $V_{GSN} = 0$ (off)

$$\therefore V_{GSp} = 0 - V_{DD} < V_{TP} (\text{ON})$$

$$\Rightarrow V_{out} \approx V_{DD}$$

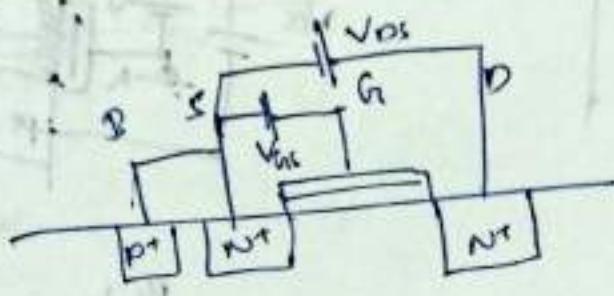
when

$$V_{in} = V_{DD}$$

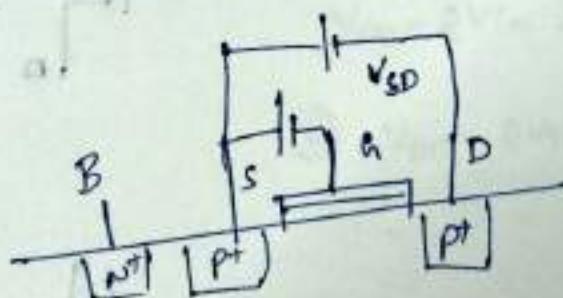
$$V_{GSP} = V_{DD} - V_{DD} = 0V > V_P \text{ (off)}$$

$$V_{GSN} = V_{DD} - 0 = V_{DD} > V_{Th} \text{ (on)}$$

$$V_{out} = 0V$$



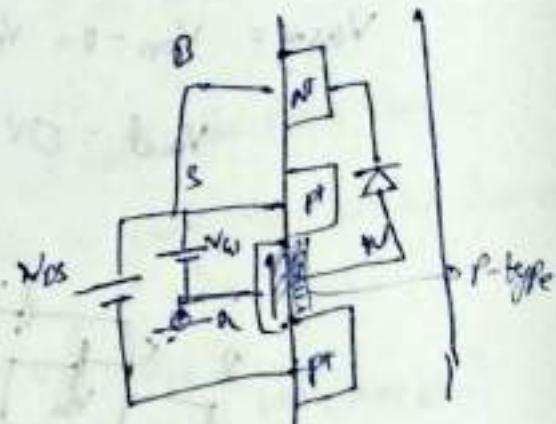
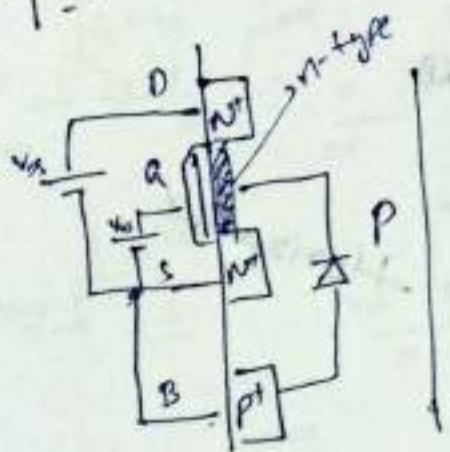
p-type (NMOS)



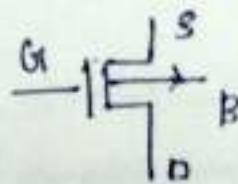
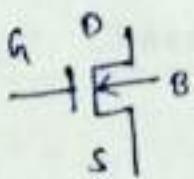
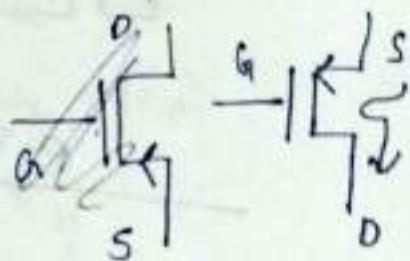
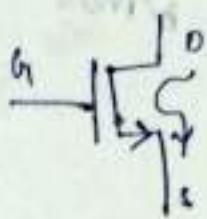
n-type.

vertical

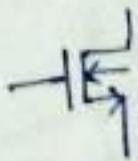
$\frac{1}{T} \rightarrow$



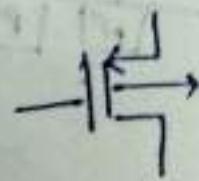
N-MOS



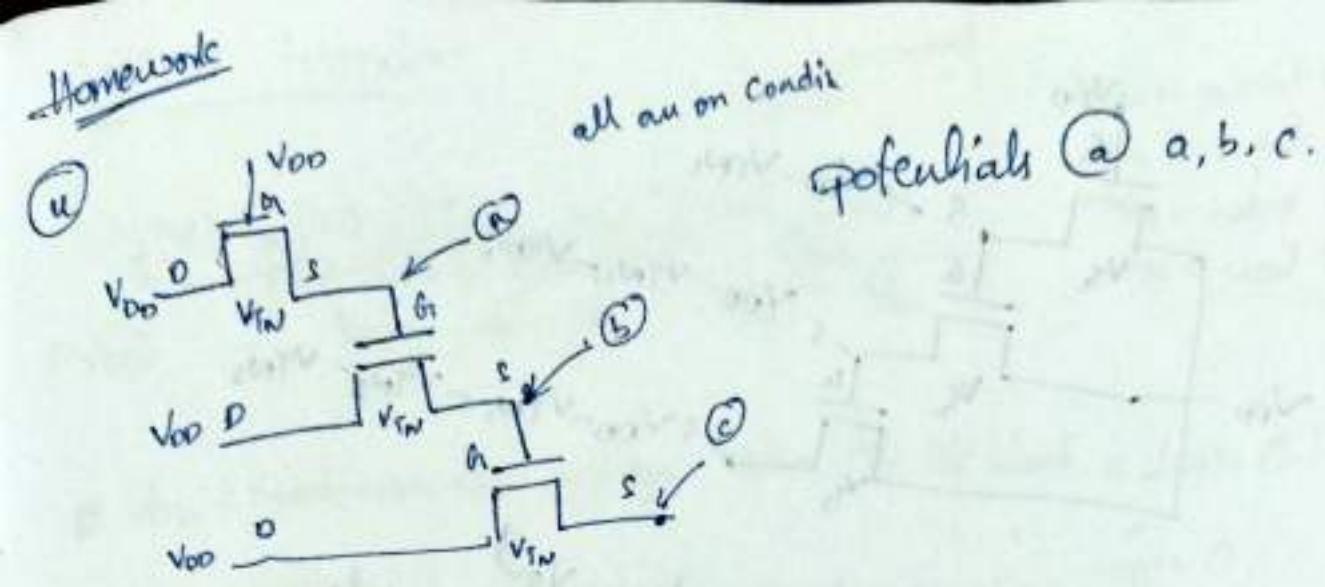
-Also



N-MOS



P-MOS



(a) $V_{DD} - V_{TN}$

$$\therefore V_{Gib} = V_{DD} - V_{TN}$$

now for ON. ~~Get~~ $V_{Gib} \geq V_{TN}$

$$V_{DD} - V_{TN} - V_{Sb} \geq V_{TN}$$

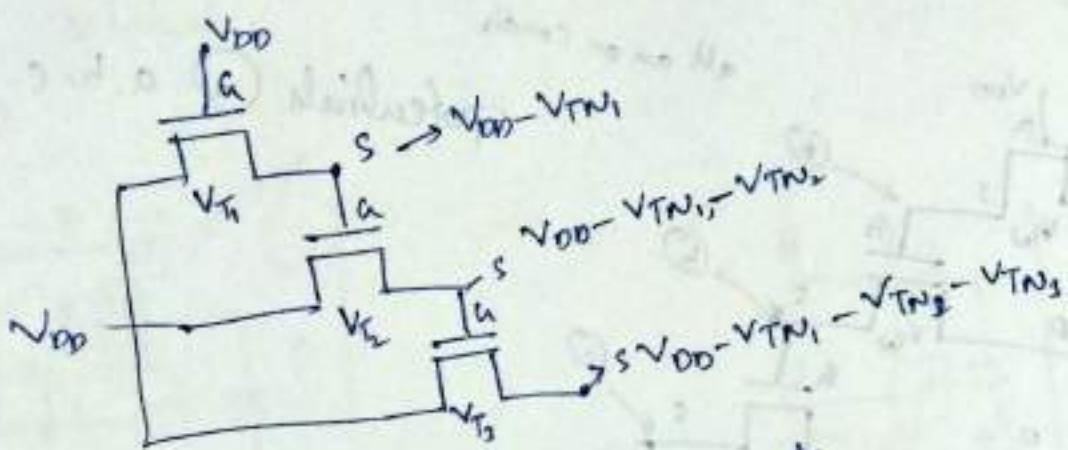
$$V_{DD} - 2V_{TN} \geq V_{Sb}$$

(b) $V_{DD} - 2V_{TN}$

$$V_{hc} = V_{DD} - 2V_{TN}$$

(c) $V_{DD} - 2V_{TN} - V_{Sc} > V_{TN}$

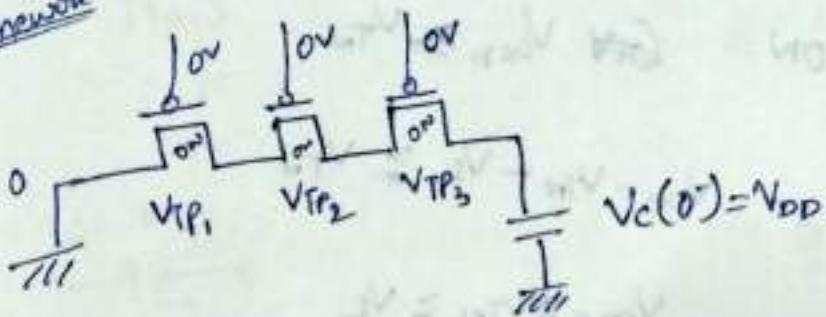
$$V_{Sc} \leq V_{DD} - 3V_{TN}$$



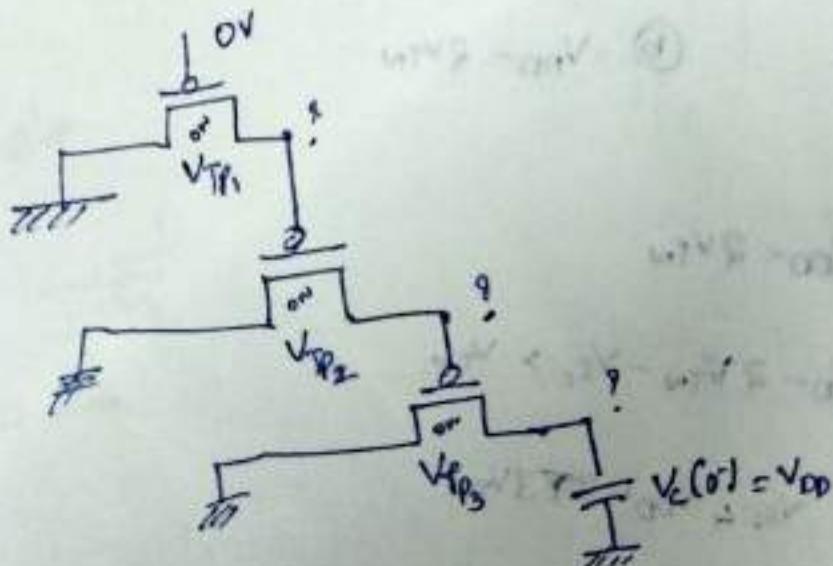
very less V_{out}
 \rightarrow bad cascadis style

Homework

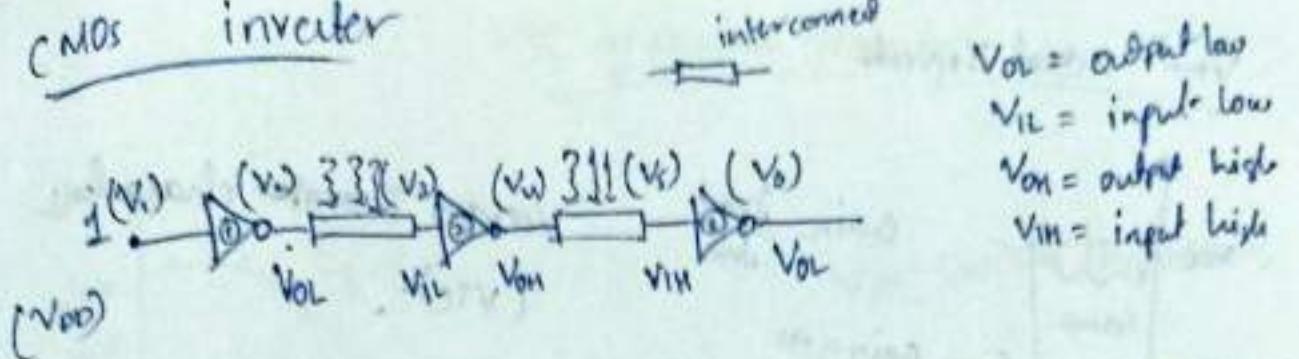
(4)



(5)



C MOS inverter



V_{OL} = output low
 V_{IL} = input low
 V_{OH} = output high
 V_{IH} = input high

• V_{OL} = minimum o/p voltage when the o/p level is logic 0. (0-1v)

V_{IL} : maximum " " " " logic 0.

V_{IL} : maximum ^{allowable} i/p voltage which can still be interpreted as logic 0.

Noise Margin (NM)

$NM_L = V_{IL} - V_{OL}$ = noise margin for low signal levels.

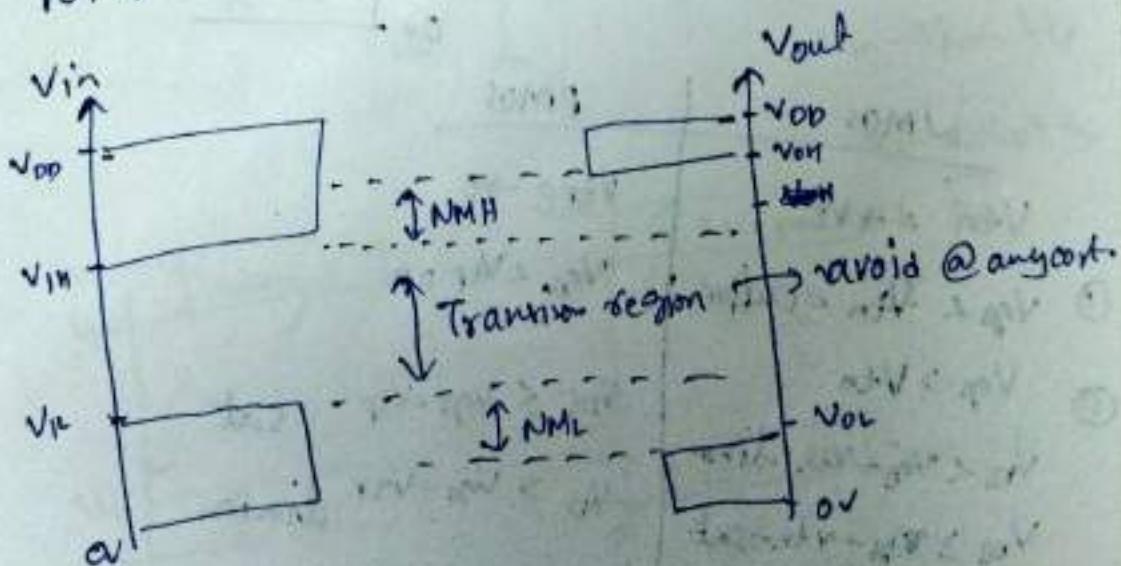
V_{OH} = maximum o/p voltage when the o/p level is logic 1.

V_{IH} = minimum ^{allowable} i/p voltage which can still be interpret as logic 1.

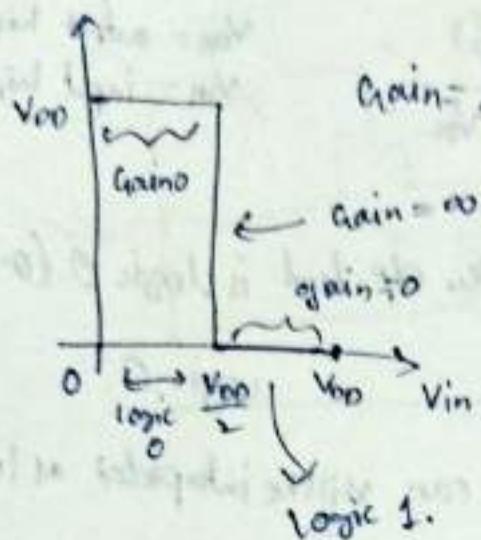
but high enough to ensure logic 0 output.

Noise margin (NM)

$NM_H = V_{OH} - V_{IH}$ = noise margin for high signal levels.



V_{out} Ideal Invert



voltage Transfer character. (VTC).

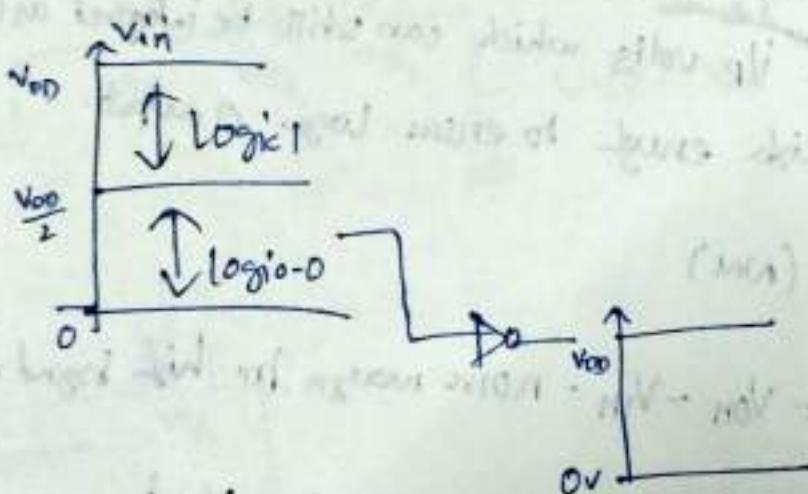
2-reg.

two. 0-gain region

one. ∞ -gain region

$$\left(\frac{V_{DD}}{2} - \Delta \right) \quad \left(\frac{V_{DD}}{2} + \Delta \right)$$

↑ Logic 0 ↑ Logic 1



N MOS PMOS

$$V_{tn} = +ve$$

① $V_{gs} < V_{tn}$ = cut off

② $V_{op} > V_{tn}$

$$V_{ds} < V_{gs} - V_{tn}$$
 linear

$$V_{ds} \geq V_{gs} - V_{tn}$$
 sat

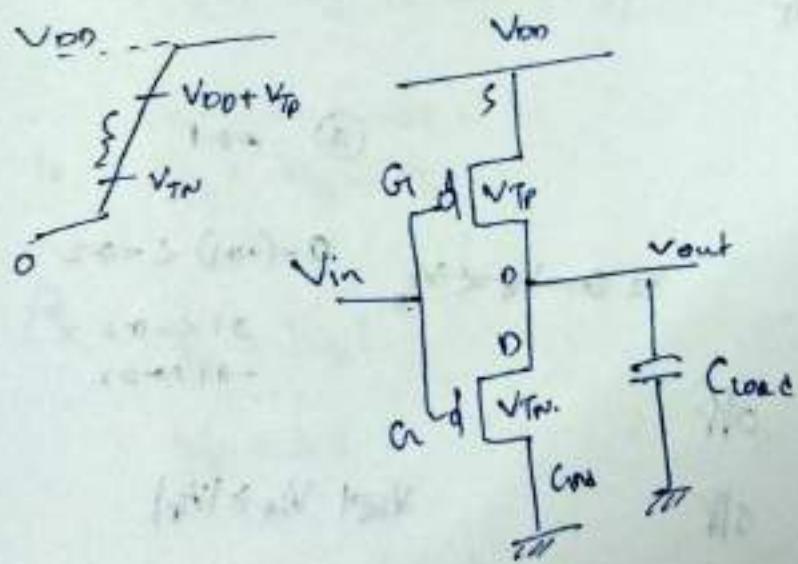
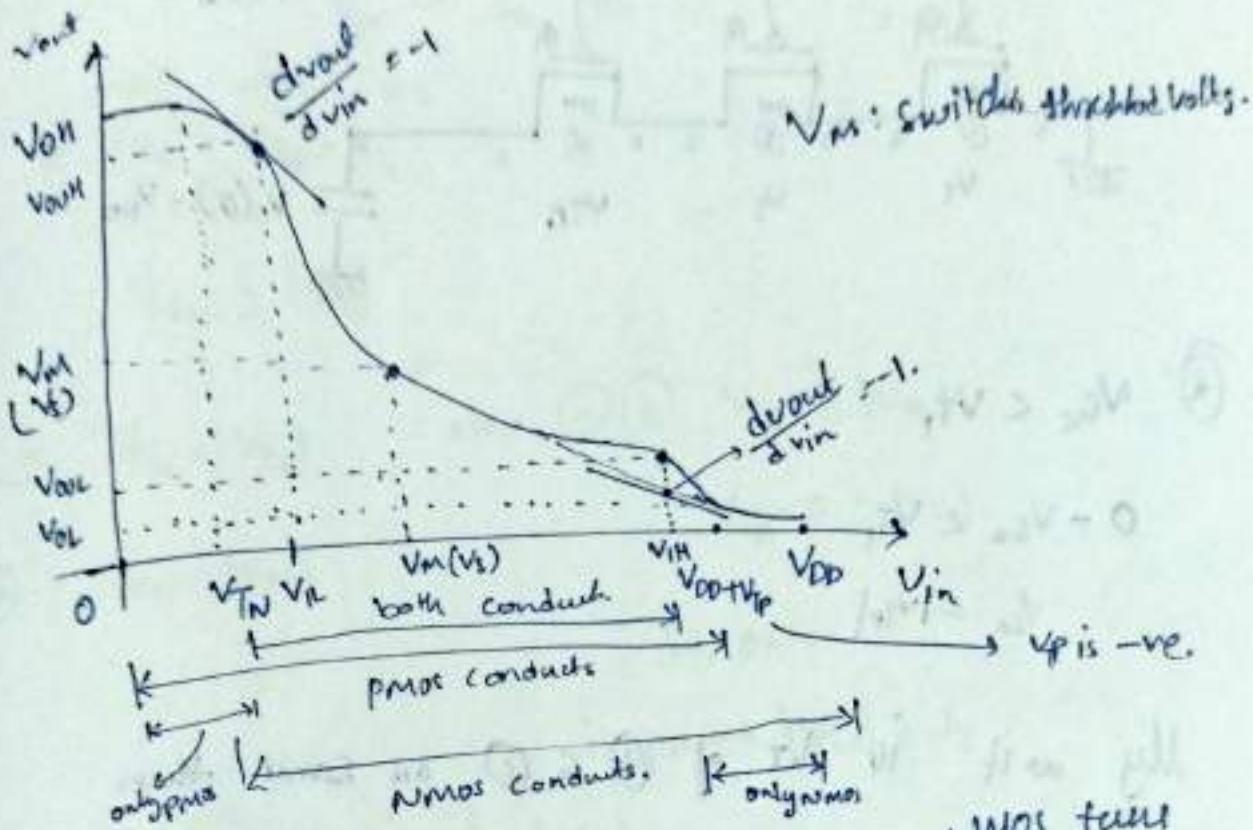
$$V_{tp} = -ve$$

$$V_{gp} < V_{tp}$$
 on.

$$V_{ds} \leq V_{gs} - V_{tp}$$
 sat

$$V_D > V_{gs} - V_{tp}$$
 linear

VTC of practical inverter



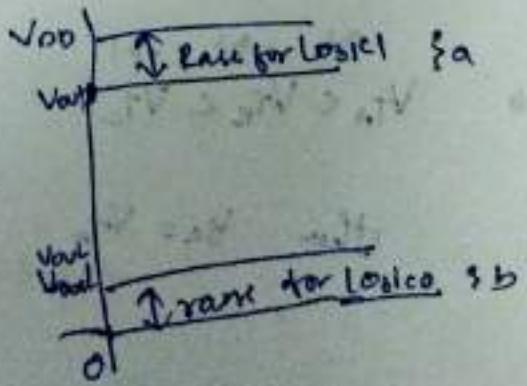
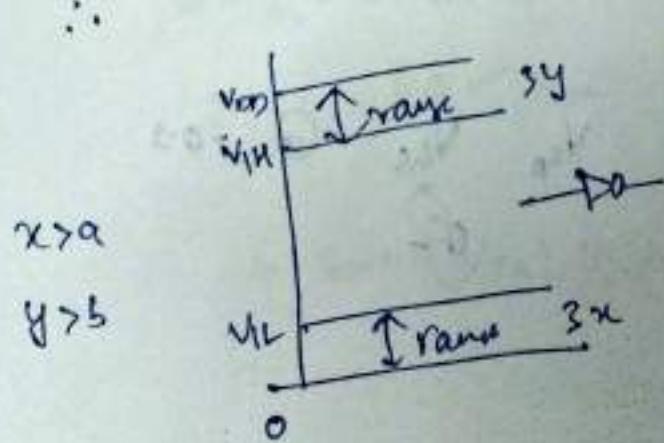
NMOS fails
ON when $V_{in} > V_{TN}$
 ∇V_{in}

PMOS fails ON
when $V_{in} -$

$V_{CS} < V_{TP}$

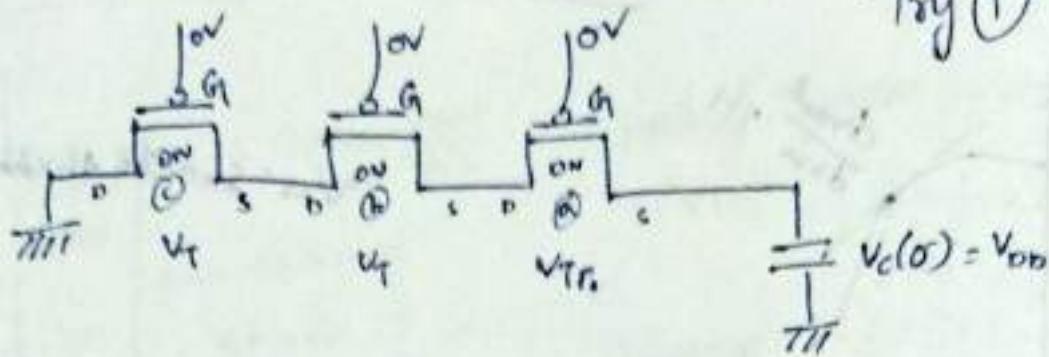
$V_{in} - V_{DD} < V_{TP}$

$V_{in} < V_{DD} + V_{TP}$



Homework

Try ①



④ $V_{GS} < V_{T_1}$

$$0 - V_{SA} < V_{T_1}$$

$$V_{SA} = |V_{rel}|$$

My wait is V_T of ② & ③ are same then

$$V_{SB} = V_{SC} = V_T$$

$$-0.1 \quad -0.2 \quad -0.3$$

$$\text{if } V_{TA} > V_{TB} > V_{TC}$$

then

$$V_{SA} = V_{TA}$$

$$V_{SB} = V_{TB} \text{ off}$$

$$V_{SC} \neq V_{TC} \text{ off}$$

$$-0.3 \quad -0.2 \quad -0.1$$

$$\text{if } V_{TA} < V_{TB} < V_{TC}$$

$$\text{then } V_{SA} = V_{TA}$$

$$V_A \quad 0 - V_B < V_{TB}$$

$$0 - (+0.1) < -0.2$$

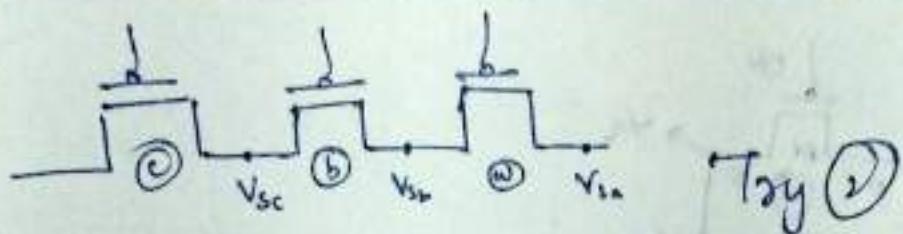
$$0.1 < -0.2 \times$$

$$-0.1 < +0.2$$

$$\text{so } V_{SA} \geq V_{TB}$$

$$V_{SB} \quad V_{AS}$$

$$0 - 0.1$$



-0.1 -0.2 -0.3

If $V_{TA} > V_{TB} > V_{TC}$

$$V_{SG_A} \geq |V_{TA}|$$

(a) $V_{SA} = |V_{TA}|$

now (a)(b). $V_{SA} \geq |V_{TB}|$

(b) $V_{DA} = |V_{TB}|$

$$|V_{TA} - 0| \geq |V_{TB}|$$

So, on.

it passes $|V_{TA}|$ only.

\therefore (c) V_{SG_A} is also $|V_{TA}|$

-0.3 -0.2 -0.1

If $V_{TA} < V_{TB} < V_{TC}$

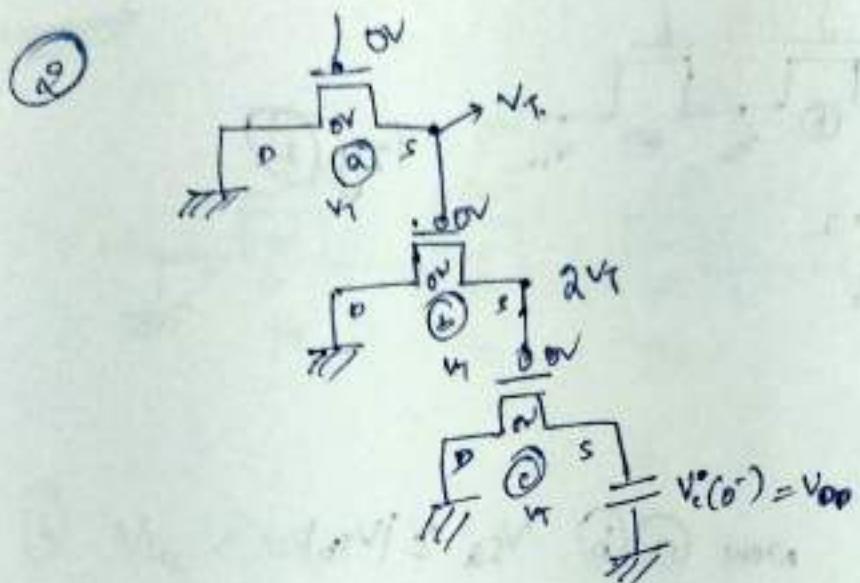
(a) $V_{SA} = |V_{TA}|$

$$V_{SA} = 0.3$$

now (b) $V_{SG_B} \geq |V_{TB}|$

$$0.3 - 0 \geq 0.2 \checkmark \text{ True}$$

so same (V_{TA}) is passed on.



$$\underline{V_{S_{10}} \geq 0}$$

$$V_{S_{10}} \geq |V_T|$$

$$V_{S_{10}} - 0 \geq |V_T|$$

$$V_{S_{10}} - V_T \geq V_T$$

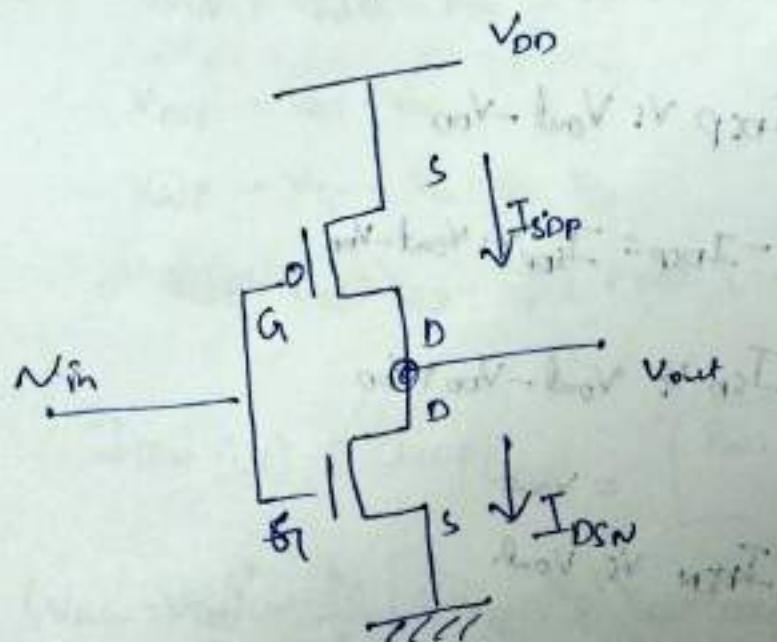
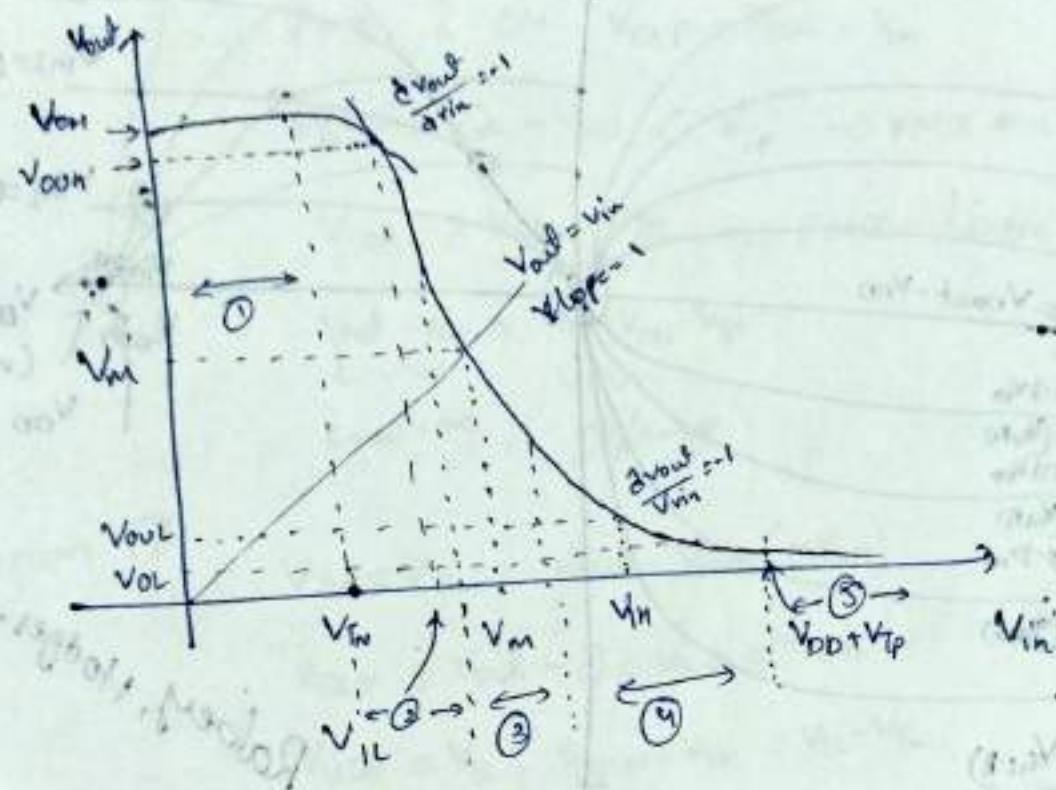
$$V_{S_{10}} \geq 2V_T$$

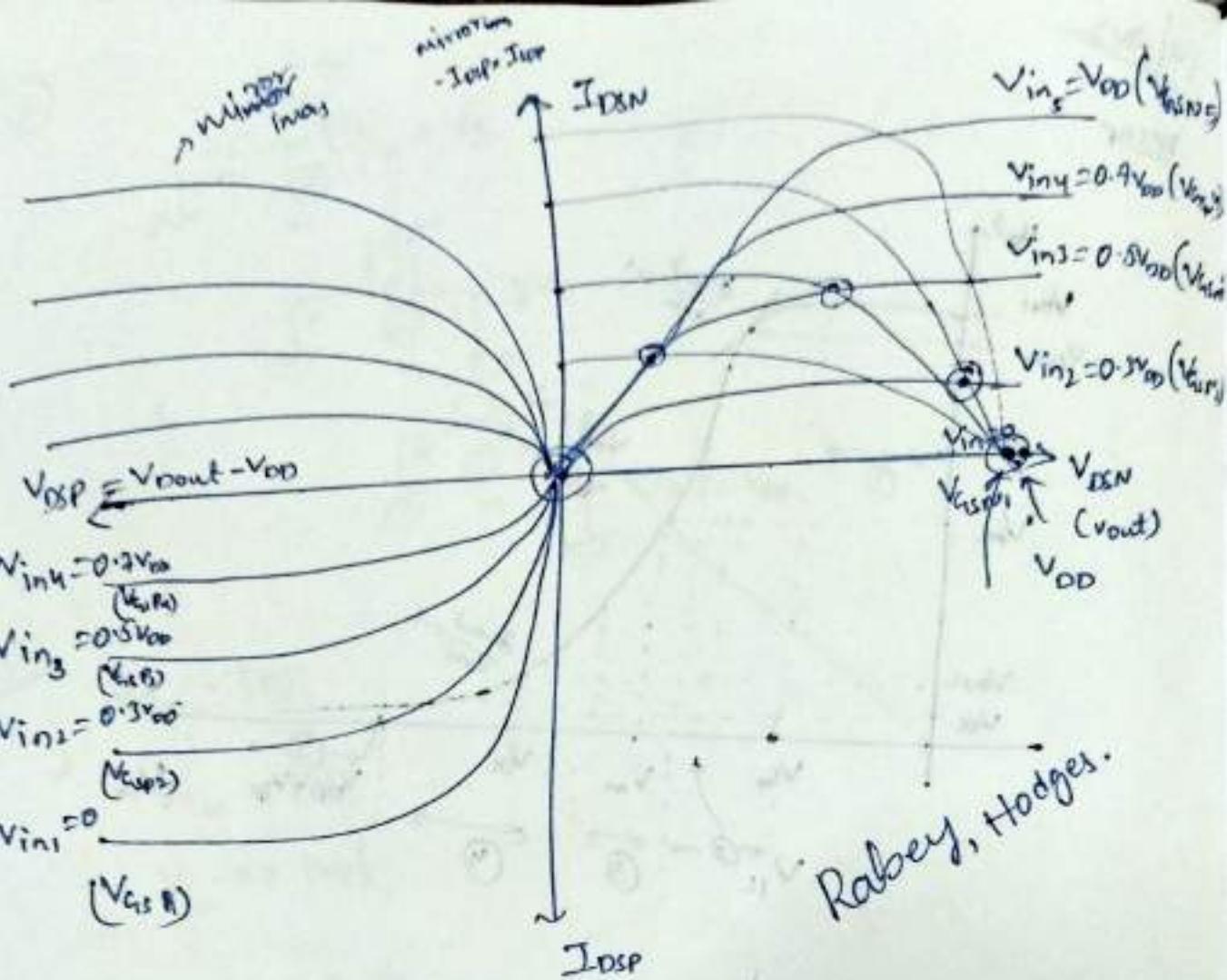
$$V_{S_{10}} - 2V_T \geq V_T$$

$$\therefore V_{S_{10}} \geq 3V_T$$

14/Aus

Verlauf





3rd : $I_{DSR} \propto V_{out} - V_{DD}$

2nd : $-I_{DSR} = I_{SOP} \propto V_{out} - V_{DD}$

1st : $I_{SD} \propto V_{out} - V_{DD} + V_{DD}$

$$= V_{out}$$

$I_{DSN} \propto V_{out}$

in Region ① $0 < V_{in} < V_{TN} \Rightarrow NMOS$ is in cut off.

$$V_{out} = V_{DD}$$

PMOS is ON $V_{DSP} = V_{out} - V_{DD}$

$V_{GSP} = V_{in} - V_{DD} < V_{TP} \Rightarrow PMOS$ is ON.

$V_{DDP} > V_{GSP} - V_{TP} \Rightarrow PMOS$ is linear

$$V_{out} - V_{DD} > V_{in} - V_{DD} - V_{TP}$$

$\sim \quad \sim$

small-ve high-ve

Region ②

$$V_{in} = V_{IL} \quad V_{out} = V_{OH} (\approx V_{DD})$$

$$V_{DSN} = V_{out} - 0 = V_{out} \approx V_{OH}$$

$$V_{GSN} = V_{IL}, \quad V_{GSN} - V_{TN} = V_{IL} - V_{TN}$$

$V_{DSN} > V_{GSN} - V_{TN} \Rightarrow NMOS$ is saturation.

$$V_{DSP} = V_{OH} - V_{DD}$$

$$V_{GSP} - V_{TP} = V_{IL} - V_{DD} - V_{TP}$$

$\therefore V_{GSP} - V_{DSP} > V_{GSP} - V_{TP} \Rightarrow PMOS$ is in linear region.

NOW

$$I_{DSN}(\text{sat}) = I_{DSP}(\text{line})$$

$$\left. \begin{aligned} B_N &= M \cdot \text{Log}\left(\frac{W}{L}\right) \\ S_P &= \dots \end{aligned} \right\}$$

$$\frac{B_N}{2} (V_{GSN} - V_{TN})^2 = \frac{\beta_P}{2} \left[2(V_{GSP} - V_{TP}) V_{DSP} - V_{DSP}^2 \right]$$

$$\frac{B_N}{2} (V_{GSN} - V_{TN})^2 = \beta_P \left[2(V_{in} - V_{DD} - V_{TP})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2 \right]$$

$$@ V_{IL}, \frac{d V_{out}}{d V_{in}} = f_{IL} V = g_{IL} V$$

$$\frac{\partial \beta_N}{\partial V_{IN}}(V_{IN} - V_{TN}) = \beta_P \left[2 \left(V_{IN} - V_{DD} - V_{TP} \right) \left(\frac{\partial V_{OUT}}{\partial V_{IN}} \right)^{-1} + \beta \left(V_{OUT} - V_{DD} \right) \right. \\ \left. - \beta \left(V_{OUT} - V_{DD} \right) \left(\frac{\partial V_{OUT}}{\partial V_{IN}} \right)^{-1} \right]$$

$$\beta_N(V_{TB} - V_{TN}) = \beta_P \left[(V_{IL} - V_{DD} - V_{TP}) (-1) + V_{OUT} - V_{DD} + V_{OUT} - V_{DD} \right]$$

$$\beta_N(V_{IL} - V_{TN}) = \beta_P \left(-V_{IL} + V_{DD} + V_{TP} + V_{OUT} - V_{DD} + V_{OUT} - V_{DD} \right)$$

$$V_{IL}(\beta_N + \beta_P) = \beta_P \left(\beta_N V_{OUT} + V_{TP} - V_{DD} \right) + \beta_N V_{TN}$$

$$\boxed{\frac{\beta_N}{\beta_P} = \beta_R}$$

$$V_{IL} (\beta_R + 1) = 2V_{OUT} + V_{TP} - V_{DD} + \beta_R V_{TN}$$

$$\boxed{V_{IL} = \frac{\beta_N V_{OUT} + V_{TP} - V_{DD} + \beta_R V_{TN}}{\beta_R + 1}}$$

Region 4: $V_{IN} = V_{IH}$; $V_{OUT} = V_{OH}$

$$V_{DSN} = V_{OUT} \approx V_{OH} \quad \left. \begin{array}{l} \{ \\ \} \end{array} \right. V_{DSN} < V_{OH} - V_{TN}$$

$$V_{GSN} - V_{TN} = V_{IH} - V_{TN} \quad \text{NMOS: linear}$$

$$V_{DSP} = V_{OUT} - V_{DD} \approx V_{OH} - V_{DD}$$

$$V_{GSP} - V_{TP} = V_{IN} - V_{DD} - V_{TP}, \quad \left\{ \begin{array}{l} V_{DSP} < V_{GSP} - V_{TP} \\ \text{PMOS: sat.} \end{array} \right.$$

$$\therefore I_{DSN} = I_{DSP}$$

$$@ V_{in} = V_{IH}, \frac{dV_{out}}{dV_{in}} = -1.$$

$$I_{DSN} = I_{DSP}$$

$$\frac{\beta_R N}{2} \left[(V_{GSP} - V_{TN}) V_{DSN} - V_{DSN}^2 \right] = \frac{\beta_P}{2} \left[V_{GSP} - V_{TP} \right]^2$$

$$\beta_R N \left[2(V_{in} - V_{TN}) V_{out} - V_{out}^2 \right] = \beta_P \left[V_{in} - V_{DD} - V_{TP} \right]^2$$

$$V_{IH} = \frac{\beta_P (V_T + 2V_{out}) + V_{DD} + V_{TP}}{1 + \beta_R}$$

Region-3

$$V_M = V_{in} = V_{out}$$

$$\text{N MOS} \quad V_{DSN} = V_{GSP}$$

$\therefore \text{N MOS: sat}$

$$\text{PMOS} \quad V_{DSP} = V_{out} - V_{DD}$$

$$V_{GSP} - V_{TP} = V_M - V_{DD} - V_{TP}$$

$$V_{DSP} < V_{GSP} - V_{TP}$$

$\Rightarrow \text{PMOS: sat.}$

$$I_{DSN}(\text{sat}) = I_{DSD}(\text{sat})$$

$$\frac{\beta_N}{2} \left(\frac{\sqrt{V_S - V}}{V_{TN}} - V_T \right)^2 = \frac{\beta_P}{2} \left(V_{IN} - V_{DD} - V_{TP} \right)^2$$

$$\beta_N (V_{IN} - V_{TN})^2 = \beta_P (V_{IN} - V_{DD} - V_{TP})^2$$

$$\beta_N (V_M - V_{TN})^2 = \beta_P (V_M - V_{DD} - V_{TP})^2$$

$$\sqrt{2S} = \pm 5$$

$$\underbrace{\sqrt{\beta_N} (V_M - V_{TN})}_{\substack{+ve \\ \frac{V_{DD}}{2} - V_{TN}}} = \underbrace{\sqrt{\beta_P} (V_M - V_{DD} - V_{TP})}_{\substack{-ve \\ \frac{V_{DD}}{2} - V_{DD} - V_{TP}}} \quad \text{ideally } V_M = V_{DD} = \frac{V_{DD}}{2}$$

+ve \neq -ve

so keep -ve RHS.

$$\sqrt{\beta_N} (V_M - V_{TN}) = -\sqrt{\beta_P} (V_M - V_{DD} - V_{TP})$$

$$V_M - V_{TN} = -\frac{1}{\sqrt{\beta_R}} (V_M - V_{DD} - V_{TP})$$

$$V_M = \frac{V_{TN} + \sqrt{\frac{1}{\beta_R} (V_{DD} + V_{TP})}}{1 + \sqrt{\frac{1}{\beta_R} - \frac{1}{\beta_P}}}$$

$$\beta_R = \left(\frac{V_{DD} + V_{TP} - V_M}{V_M - V_{TN}} \right)^2$$

$V_M = \frac{V_{DD}}{2}$ (ideal inverter), $V_{TN} = |V_{TP}|$, substitute

$$\beta_R = \left(\frac{0.5V_{DD} + V_{TP}}{0.5V_{DD} - V_{TN}} \right)^2 = \frac{\beta_N}{\beta_P}$$

$V_{TN} = |V_{TP}| \Rightarrow$ symmetric inverter

$V_{TN} = -V_{TP} \Rightarrow$ symmetric I/p - O/p characteristics.

$$\beta_R = \left(\frac{0.5V_{DD} - V_{TN}}{0.5V_{DD} + V_{TP}} \right)^2 - 1 = \frac{\beta_N}{\beta_P}$$

$$M_n C_{ox} \left(\frac{w}{L}\right)_N = M_p C_{ox} \left(\frac{w}{L}\right)_P$$

$$M_n \left(\frac{w}{L}\right)_N = M_p \left(\frac{w}{L}\right)_P$$

$$\Rightarrow \left(\frac{w}{L}\right)_N / \left(\frac{w}{L}\right)_P = \frac{M_p}{M_n} \approx \frac{230 \text{ cm}^2/\text{V}_s}{580 \text{ cm}^2/\text{V}_s}$$

$$\left(\frac{w}{L}\right)_P \approx 2.5 \left(\frac{w}{L}\right)_N, \quad W_{PMOS} \approx 2.5 W_N \\ w_p \approx 2 w_n$$

NOW

$$V_{IL} = \frac{2V_{out} + V_{TP} - V_{DD} + \beta_R V_{IN}}{1 + \beta_E}$$

$$V_{IH} = \beta_R (V_{TN} + 2V_{out}) + (V_{DD} + V_{TP})$$

for

$$\underline{V_{IH}} \Rightarrow V_{TN} = |V_{TP}| \Rightarrow \beta_E = 1$$

$$V_{IN} = \frac{V_{TP} + 2V_{out} + V_{DD} - V_{TN}}{2}$$

$$\boxed{V_{out} = V_{IH} - \frac{V_{DD}}{2}}$$

Region 4

$$@ V_{in} = V_{IH}$$

$$V_{TN} = |V_{TP}|$$

$$R_P = R_S$$

$$\beta_R = 1$$

$$\Rightarrow \frac{\beta_R}{2} \left[2(V_{ASN} - V_{TN})V_{DSN} - V_{DSN}^2 \right] = \frac{\beta_R}{2} (V_{TP} - V_{TP})^2$$

$$\Rightarrow 2(V_{ASN} - V_{TN})V_{out} - V_{out}^2 = (V_{IH} - V_{DD} - V_{TP})^2$$

$$2(V_{in} - V_{TN})V_{out} - V_{out}^2 = (V_{IH} - V_{DD} - V_{TP})^2$$

$$\Rightarrow 2(V_{in} - V_{TN})(V_{IH} - \frac{V_{DD}}{2}) - (V_{IH} - \frac{V_{DD}}{2})^2 = (V_{in} - V_{DD} - V_{TP})^2$$

$$\Rightarrow 2 \left[V_{IH}^2 - V_{IH} \frac{V_{DD}}{2} - V_{in}V_{TN} + V_{TN}\frac{V_{DD}}{2} \right] - \left[V_{IH}^2 + \frac{V_{DD}^2}{4} - V_{IH}V_{DD} \right]$$

$$= V_{IH}^2 + V_{DD}^2 + V_{TP}^2 - 2V_{IH}V_{DD} - 2V_{IH}V_{TP} + 2V_{DD}V_{TP}$$

$$-2V_{IH}V_{TN} + V_{TN}V_{OD} - \frac{V_{OD}}{4} = V_{OD}^2 + V_{TN}^2 - 2V_{IH}V_{OD} + 2V_{IH}V_{TN} - 2V_{IH}V_{TN}$$

$$\Rightarrow 2V_{IH}V_{OD} - 4V_{IH}V_{TN} = \frac{5}{4}V_{OD}^2 - 3V_{OD}V_{TN} + V_{TN}^2$$

$$\Rightarrow 4V_{IH}\left(\frac{V_{OD}}{2} - V_{TN}\right) = \frac{5}{4}V_{OD}^2 - \frac{5}{2}V_{OD}V_{TN} - \frac{1}{2}V_{OD}V_{TN} + V_{TN}^2$$

$$\Rightarrow 4V_{IH}\left(\frac{V_{OD}}{2} - V_{TN}\right) = \frac{5}{2}V_{OD}\left(\frac{V_{OD}}{2} - V_{TN}\right) - V_{TN}\left(\frac{V_{OD}}{2} - V_{TN}\right)$$

$$\boxed{V_{IH} = \frac{1}{8}(5V_{OD} - 2V_{TN})}$$

$$\boxed{V_{IL} + V_{IH} = V_{DD}}$$

$$NM_L = V_{IL} - V_{OL}$$

$$NM_H = V_{OH} - V_{IH}$$

Homework

$$\underline{V_{IL}} \quad V_{OD} = V_{IL} + \frac{V_{OD}}{2}$$

$$V_{IH} \rightarrow V_{OL}, V_{IL} \rightarrow V_{OH}$$

$$V_{out}, V_{OL} = V_{IH} - \frac{V_{DD}}{2}$$

$$\downarrow$$

$$\frac{1}{8}[5V_{OD} - 2V_{TN}] - \frac{V_{DD}}{2}$$

$$V_{out}, V_{OL} = \frac{1}{8}[3V_{OD} + 2V_{TN}] + \frac{V_{OD}}{2}$$

final

$$\boxed{V_{IL} = \frac{1}{8}(3V_{OD} + 2V_{TN})}$$

for CMOS INverter

$$V_{OL} = 0$$

$$\therefore NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

$$= V_{IL}$$

19 Aug/24

Region 5 ($V_{DD} + V_{TP} < V_{GS}$)

PMOS

$$V_G > V_{DD} + V_{TP}$$

$$V_{GSP} > V_{DD} + V_{TP} - V_{OD}$$

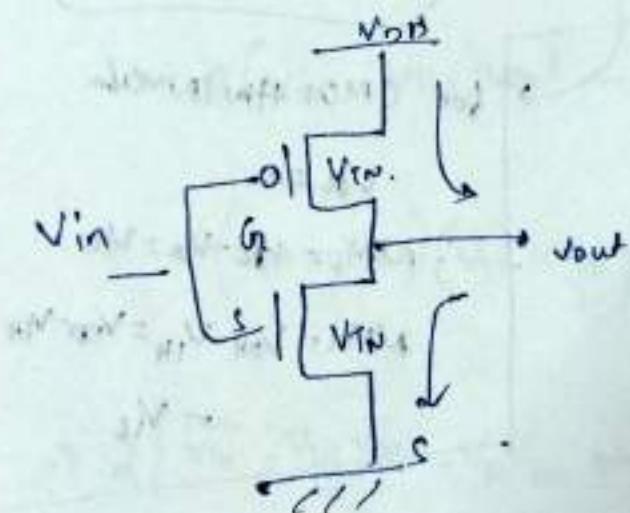
$$V_{GSP} > V_{TP} \text{ (pmos cutoff)}$$

NMOS $V_{DSN} \geq V_{GSN} - V_{TN} \Rightarrow \text{NMOS linear}$

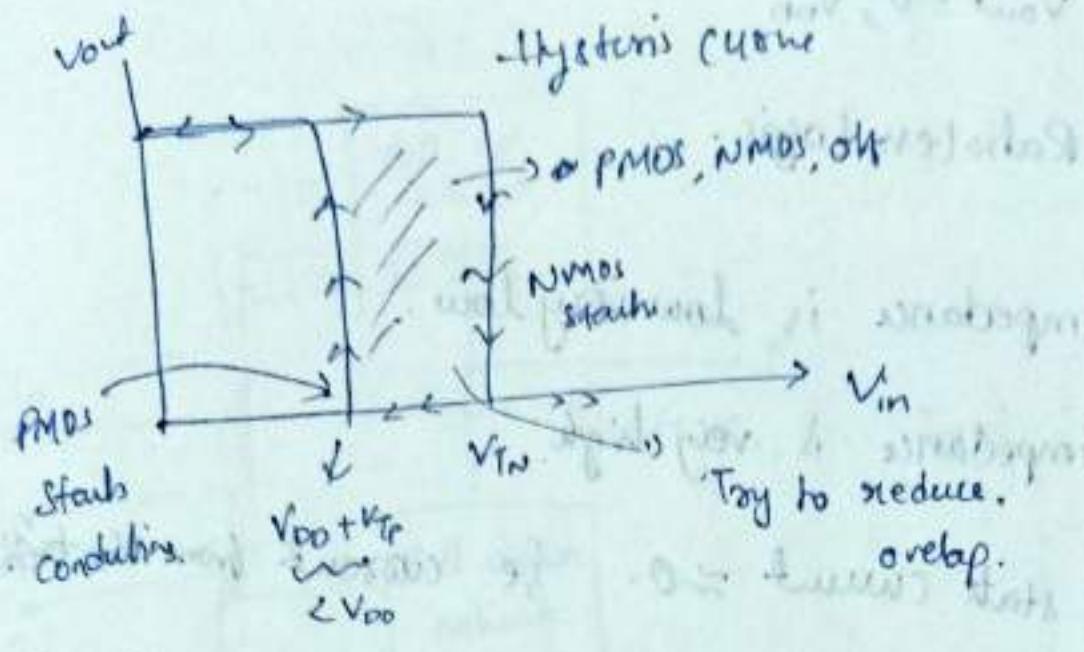
$$V_{GSN} - V_{TN} > V_{DD} + V_{TP} - 0 - V_{TN}$$

$$V_{GSN} - V_{TN} > V_{DD} - 2V_{TN}$$

for static CMOS INV



for static CMOS logic any
one of the Transistor
should conduct.



$$V_{DD} + V_{TP} = V_{TN}$$

$$V_{DD} = V_{TN} - V_{TP}$$

$$V_{DD\min} = V_{TN} + |V_{TP}|$$

STATIC CMOS inverter (circuit) Rabeis

① Rail to Rail voltage swing

logic 0 - 0 logic 1 - V_{DD}

⇒ high noise margin

⇒ robust (low sensitivity to noise)

② Logic levels (0 & V_{DD})

Diagram showing the voltage drop across the resistors R_{ON,P} and R_{ON,N}:

V_{DD}

$R_{ON,P}$

$R_{ON,N}$

$V_{out} = \frac{R_{ON,N}}{R_{ON,N} + R_{ON,P}} \cdot V_{DD} \Rightarrow \frac{V_{DD}}{1 + \left(\frac{R_{ON,P}}{R_{ON,N}} \right)}$

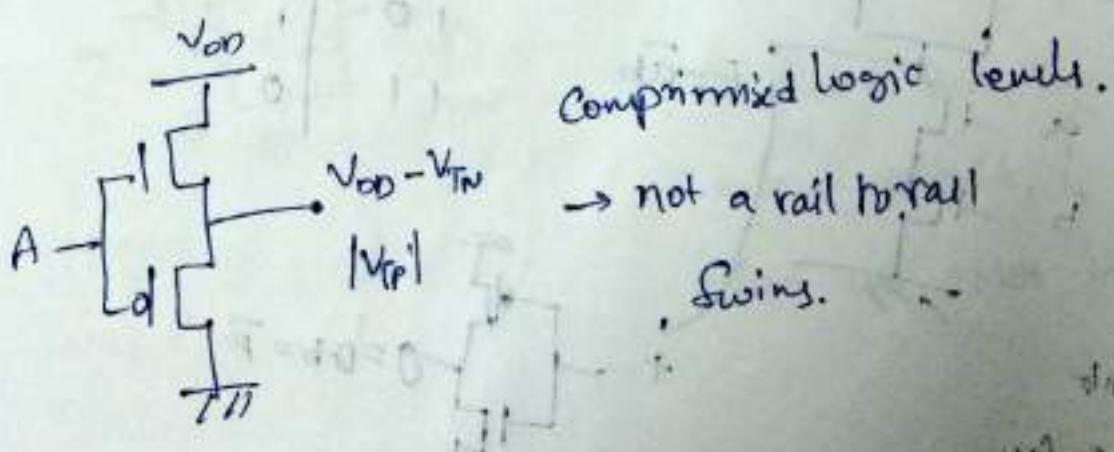
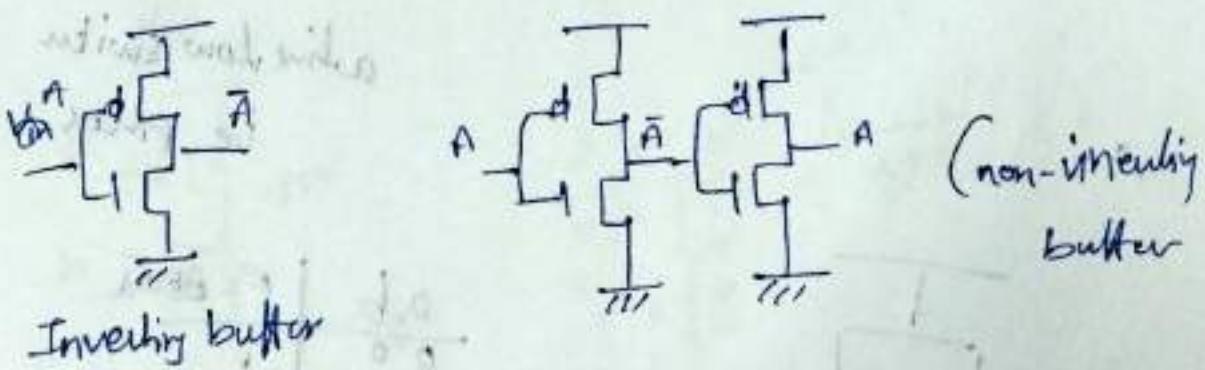
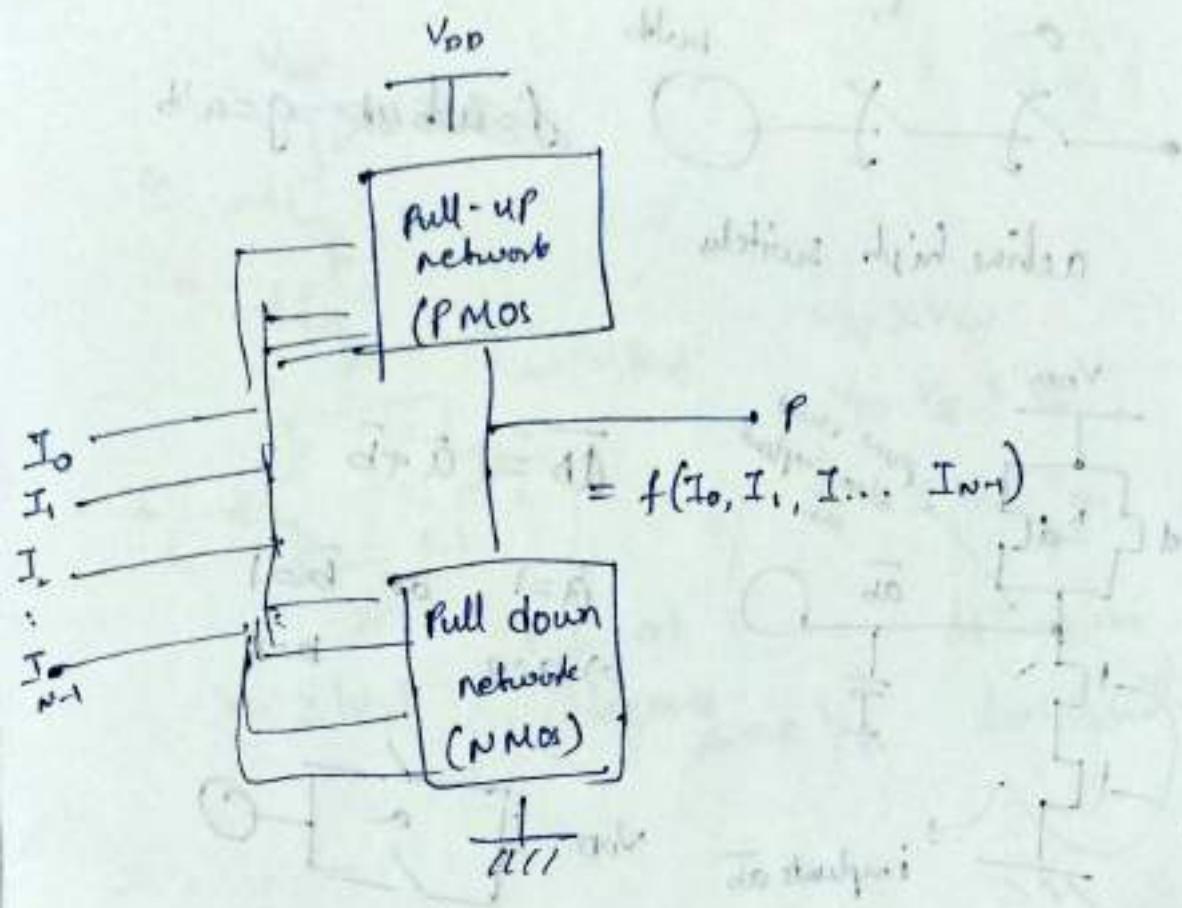
Still $V_{out} = 0, V_{DD}$

\therefore Ratioken logic.

- 3) O/p impedance is low very low.
- 4) I/p impedance is very high.
- 5) Steady state current ≈ 0 . i.e. current from V_{DD} to GND
 \Rightarrow low power consumption with no static power dissipation.
(Assuming negligible leakage current).

STATIC CMOS LOGIC (Invertig in NATURE)

- * They have well defined output once the I/P are stabilized.
- * At every point in time, the output is either connected to V_{DD} or GND .
- * O/P of the gate at all times assumes the value of the Boolean fn, implement by the ckt.

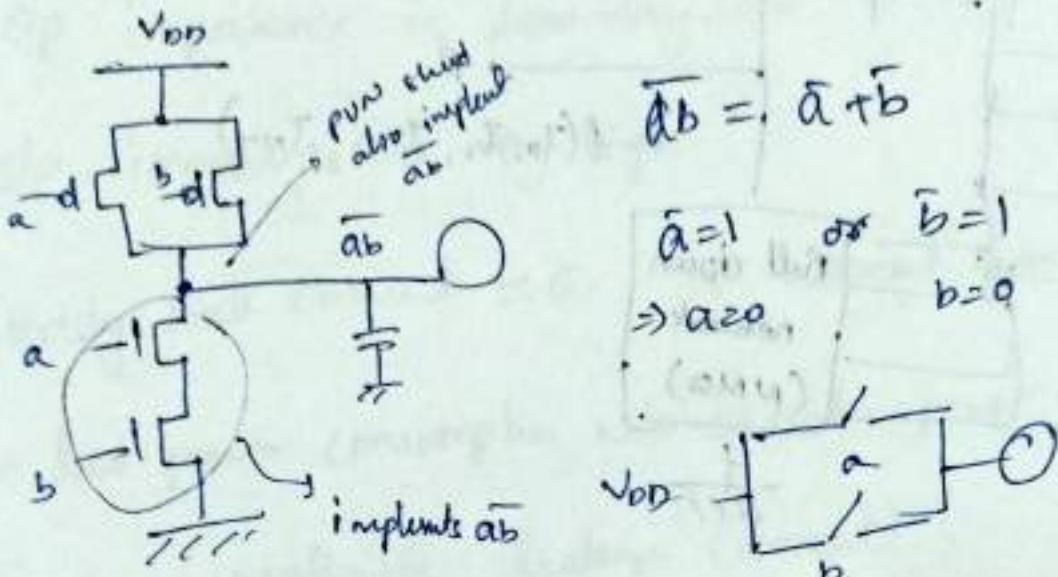
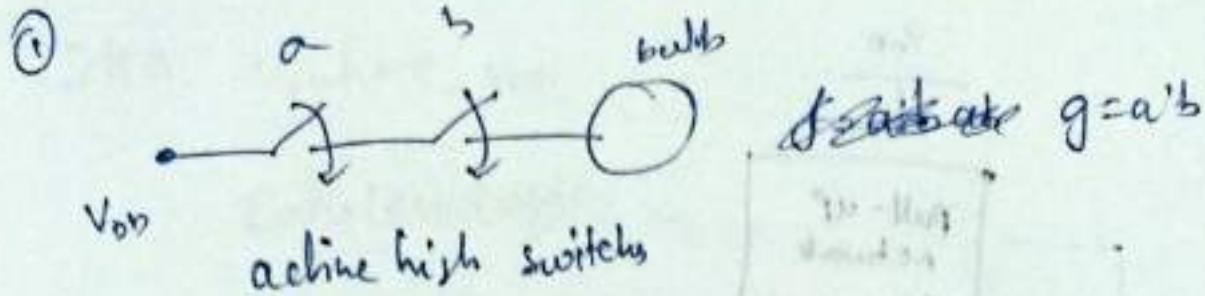


Comprised logic levels.

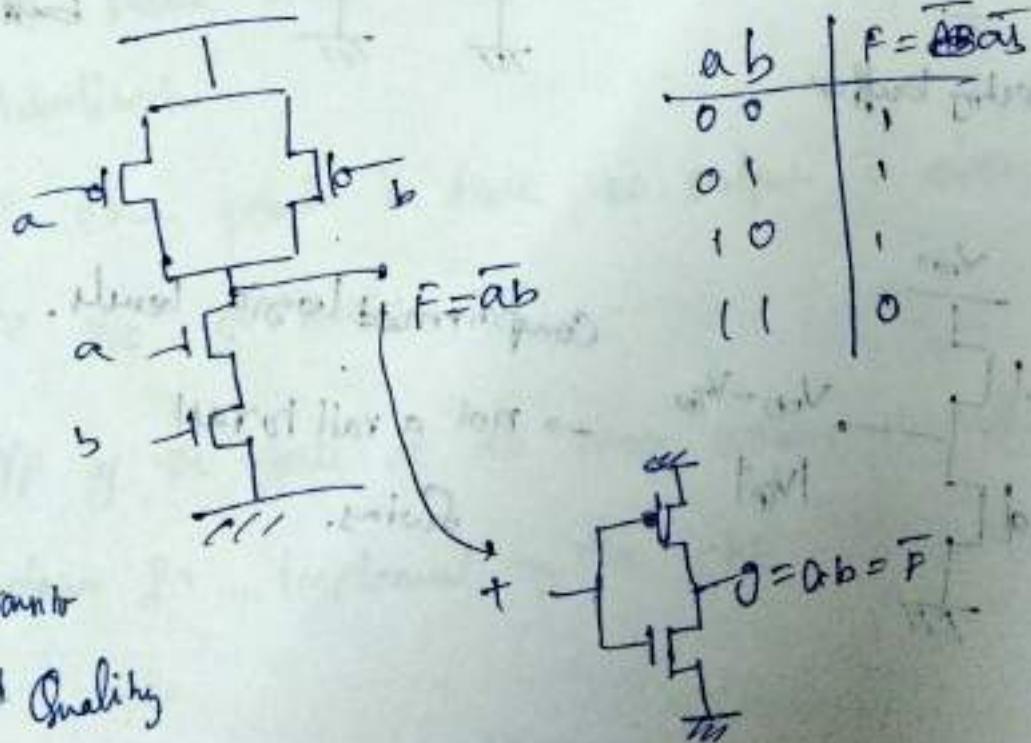
→ not a rail to rail swing.

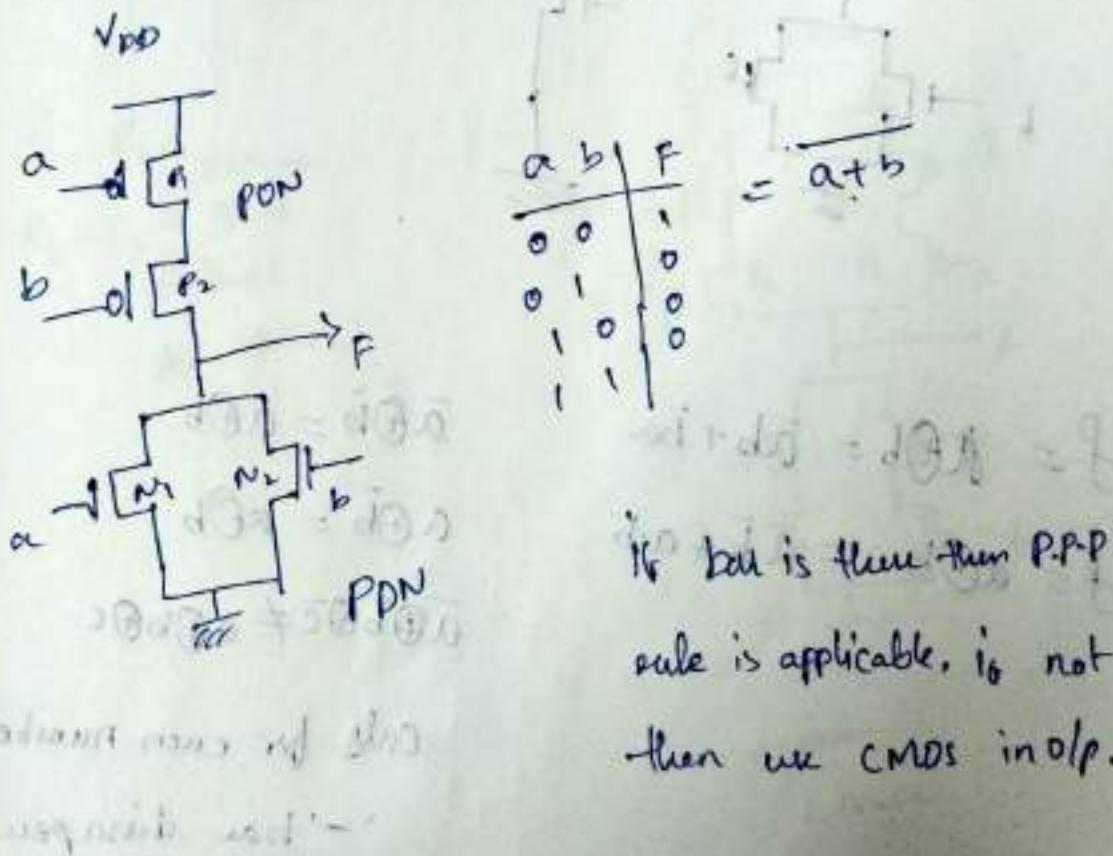
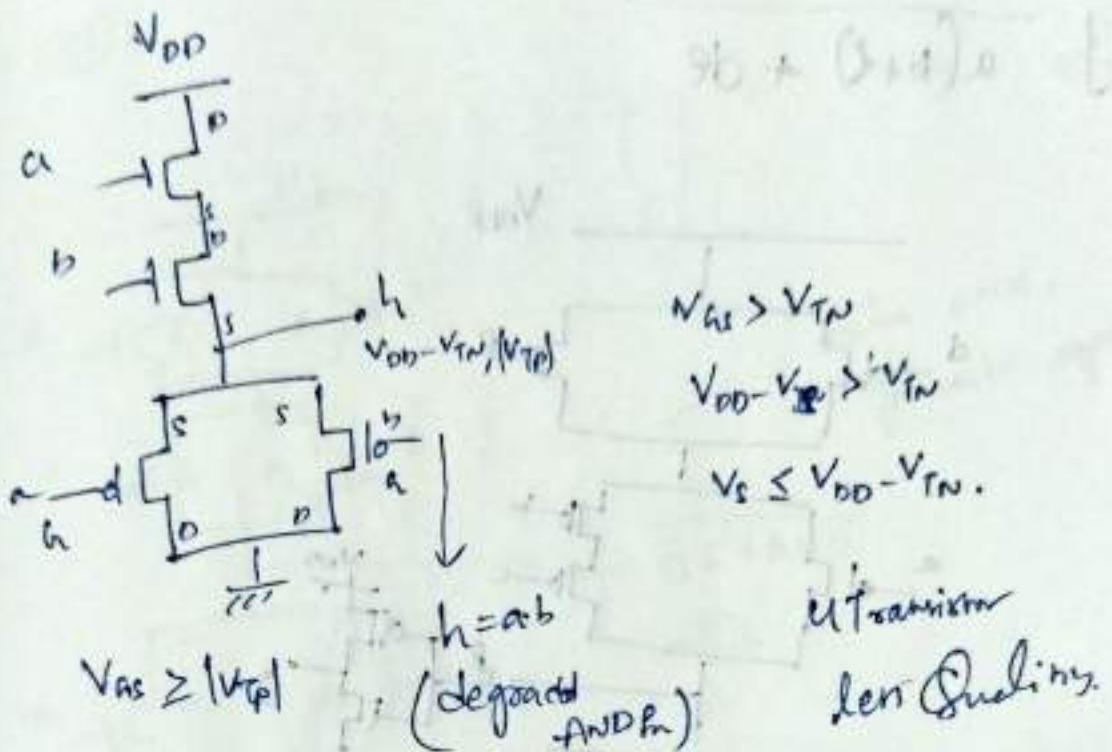
short

middle temp

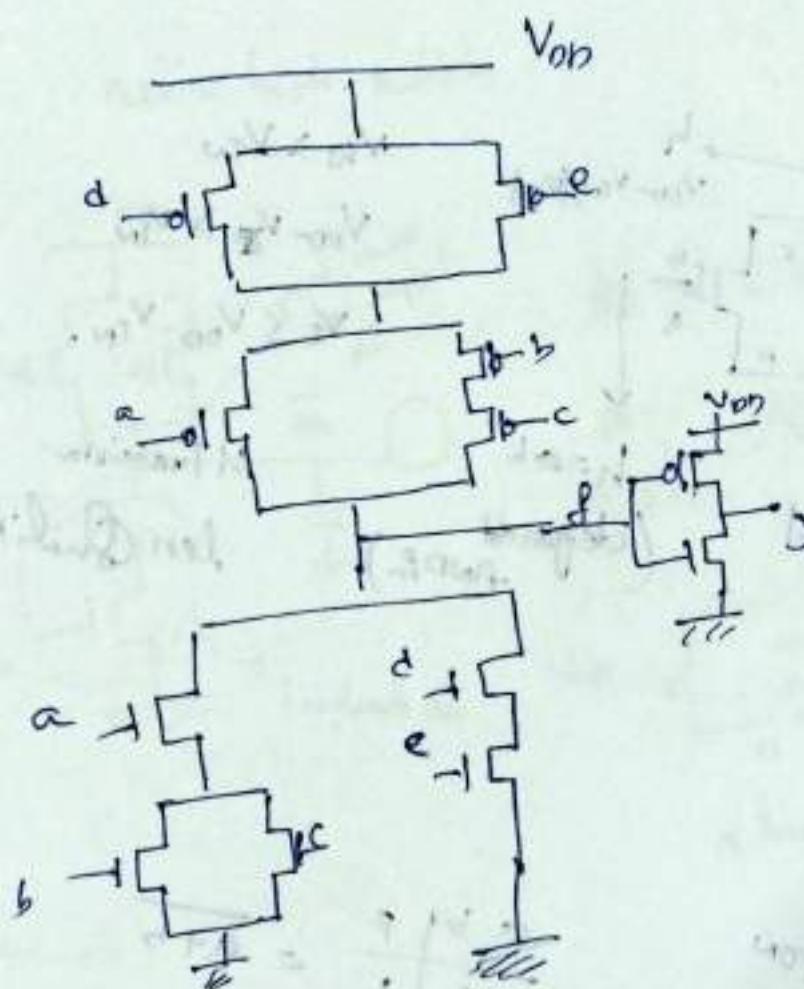


active low switch
ie pmos.





$$① f = \overline{a(b+c)} + de$$



$$③ f = a \oplus b = \bar{a}b + \bar{b}a$$

$$\bar{a} \oplus \bar{b} = \bar{a} \bar{b}$$

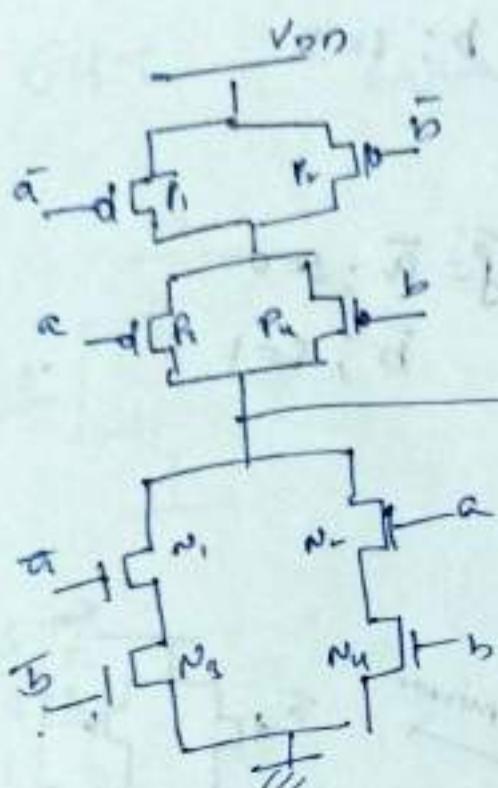
$$a \oplus \bar{b} = a \bar{b}$$

$$\bar{a} \oplus \bar{b} \oplus \bar{c} \neq a \oplus b \oplus c$$

$$f = a \oplus b = \bar{a}b + a\bar{b}$$

only for even number
- bar disappear.

$$f = a \oplus b$$

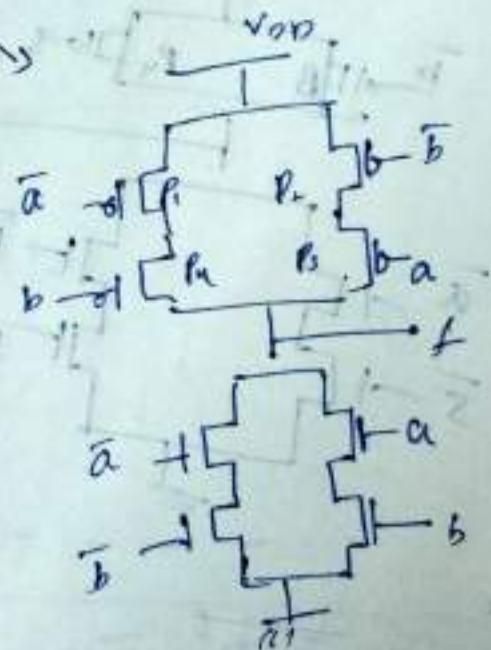


extra wire,
parasitic capacitors

$$f = \overline{\bar{a}b + ab}$$

$$= a \oplus b.$$

$P_1 - P_3 \} \text{ never}$
 $P_2 - P_4 \} \text{ get}$
 activate
 simultaneously

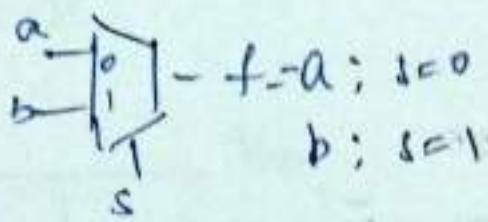


mirror
circuit

Homework EXNOR

$$f = (\overline{P \oplus Q} \oplus R \oplus S)$$

$$f = a\bar{s} + bs$$



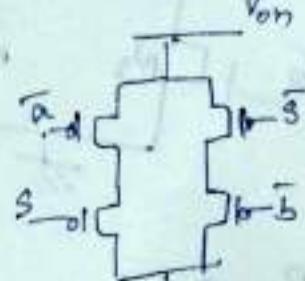
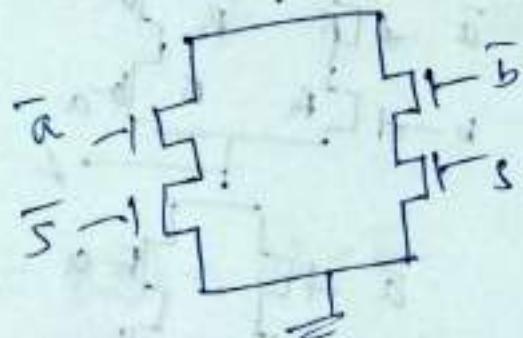
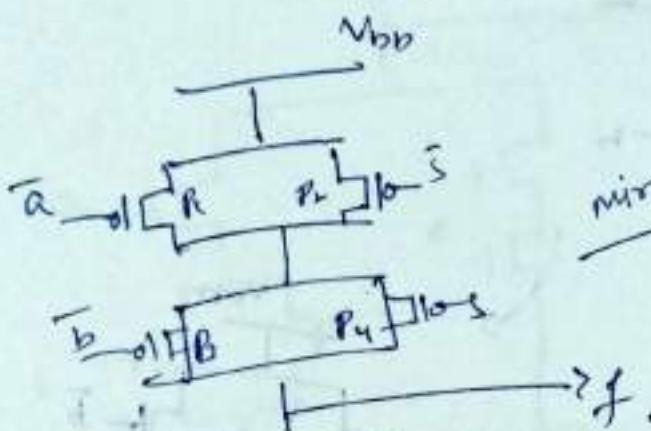
Now

$$f = ?$$

$$= \bar{a}\bar{s} + \bar{b}s$$

$$\bar{f} = \bar{a}; s=0$$

$$\bar{b}; s=1$$

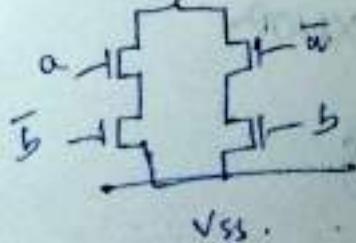
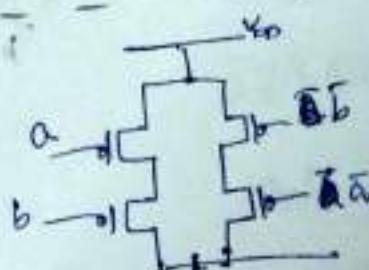


$$(\bar{a}+s), (\bar{s}+b)$$

$$\bar{a}s + s\bar{b} + \bar{a}b$$

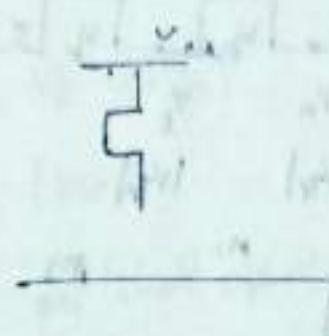
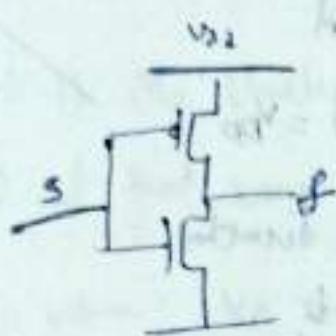
+ homework

$$\text{EX-NOR } F = \overline{ab + \bar{a}b}$$

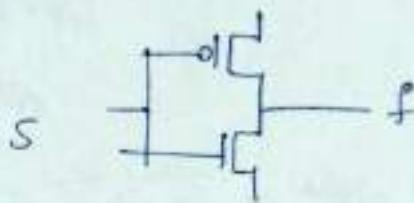


VSS

$\rightarrow 24T$ is separately $(24+4)T$.
 $\rightarrow 64T$ is equation for much



S	0	1
A	0	1
B	0	1



Cmos.

full adder =

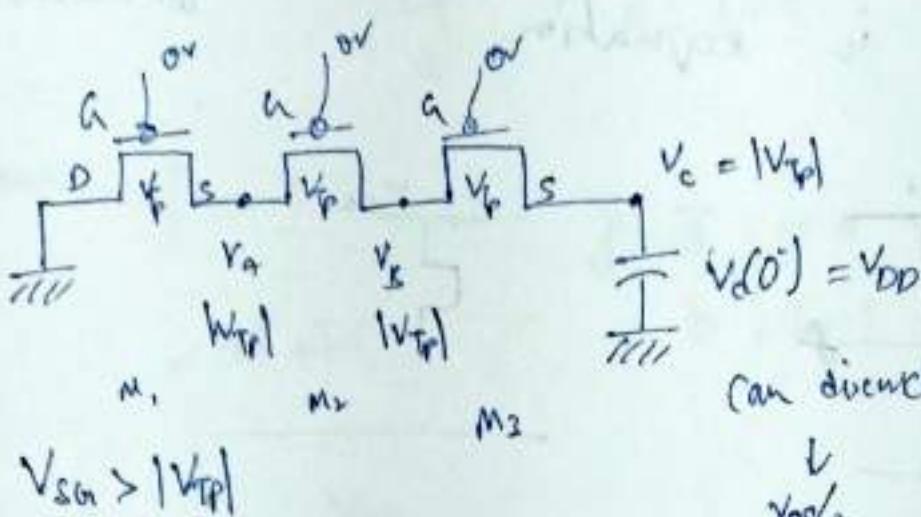
Carry =

Note : for NMOS apply f in in PDN, for PMOS apply f in PDN with inverted inputs.

ad.ayl 24

Problems

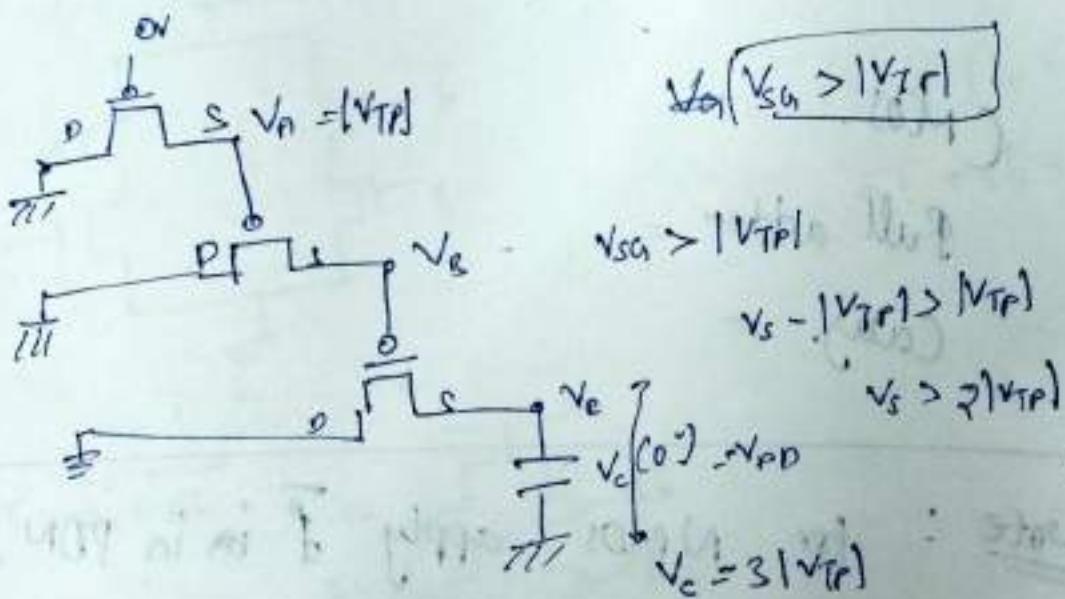
①



(can discharge)

$$\begin{aligned} V_{SGn}/2 \\ V_{SGn}/n \\ \vdots \\ |V_{TP}| \end{aligned}$$

②



$$V_{TP_1} + V_{TP_2} + V_{TP_3}$$

→ If M_2 shuts off first, $V_c = |V_{TP_1}|$

→ at the same time $V_A = |V_{TP_3}|$, $V_B = |V_{TP_2}|$

→ If M_2 shuts off next, $V_B = |V_{TP_2}|$.

→ at that same time $\Rightarrow V_A = |V_{TP_1}|$.

→ when V_A equals $|V_{TP_1}|$, M_1 shut off.

$$|V_{TP_3}| > |V_{TP_2}| > |V_{TP_1}|$$

$$V_{TP_2} < V_{TP_1} < V_{TP_3}$$

⇒ If M_2 shuts off first $\rightarrow |V_{TP_3}|$ is the largest.

$$V_A = |V_{TP_1}|, V_B = |V_{TP_2}|, V_c = |V_{TP_3}|$$

$$V_{out} = V_c = |V_{TP_3}| \text{ (final ans)}$$

$$V_B = |V_{TP_2}| \text{ (final ans)}$$

$$V_A = |V_{TP_1}|$$

$$\text{Q). } V_{TN} = 0.6V \quad V_{TP} = -0.7V$$

$$M_n C_{ox} = 60fA/V^2$$

$$M_p C_{ox} = 25fA/V^2$$

$$(w/l)_N = F \quad (w/l)_P = 12$$

$$V_{DD} = 3.3V$$

Calculate $V_M, V_{H}, V_{L}, V_{OL}$

and V_{OH} .

$$V_M = V_{TN} + \frac{1}{\sqrt{B_N}} (V_{DD} + V_{TP})$$

$$1 + \frac{1}{\sqrt{B_P}}$$

$$\beta_R = \frac{\beta_N}{\beta_P} = \frac{M_N \cos\left(\frac{\omega}{L}\right)}{M_P \cos\left(\frac{\omega}{L}\right)_P}$$

$$V_{12} = \frac{1}{8} (3V_{DD} + 2V_{TN}) , V_{IN} = \frac{1}{8} (5V_{DD} - 2V_{TN})$$

$$\Rightarrow (\beta_0 = 1, |V_{TP}| = V_{TN})$$

$\Rightarrow I_{DNNMOS} = I_{SDPMOS} \rightarrow$ (unknow exactly V_{IN}, V_{out})

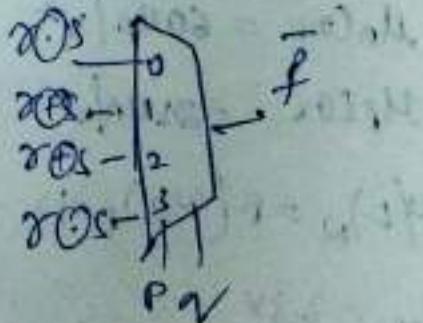
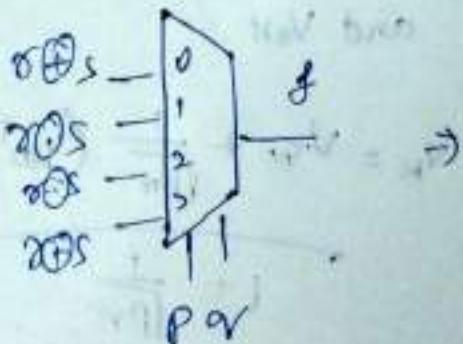
(sat)	(lin)	then $\frac{dV_{out}}{dV_{in}} = -1$
(lin)	(sat)	

$$f = P \oplus Q \oplus R \oplus S = (\bar{P}Q + \bar{P}\bar{Q}) \oplus (\bar{R}S + RS)$$

$$\Rightarrow (\bar{P}Q + \bar{P}\bar{Q})(\bar{R}S + RS) + (PQ + Q\bar{P})(\bar{R}S + RS)$$

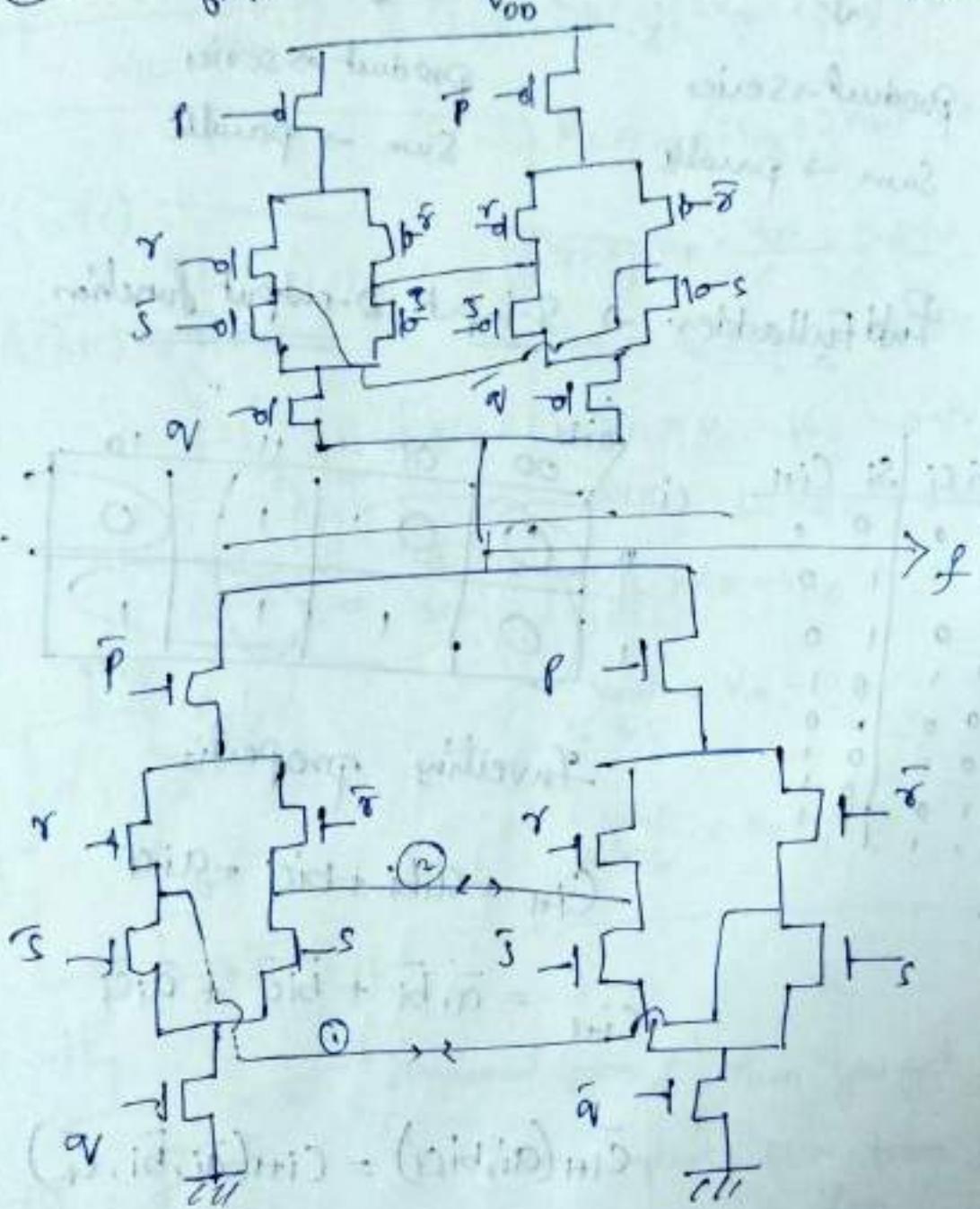
$$\Rightarrow \bar{P}Q\bar{R}S + \bar{P}QRS + \bar{P}\bar{Q}\bar{R}S + \bar{P}\bar{Q}RS + PQ\bar{R}S + PQRS + \bar{P}N\bar{R}S + \bar{P}\bar{Q}RS$$

$$\Rightarrow \bar{P}Q(\bar{R}S + RS) + \bar{P}\bar{Q}(\bar{R}S + RS) + PQ(\bar{R}S + RS) + \underbrace{\bar{P}\bar{Q}(RS + RS)}_{PUN, used}$$



$\therefore f \Rightarrow \bar{f}$ only if r will be negated not selected.

$$\bar{f} = \overbrace{\bar{P}Q(\bar{r}\bar{s} + \bar{s}s)}^{\text{for } P\bar{Q}} + \overbrace{P\bar{Q}(rs + \bar{s}s)}^{\text{for } P\bar{Q}} + \overbrace{PQ(\bar{r}\bar{s} + \bar{s}s)}^{\text{for } Q\bar{P}} + \overbrace{\bar{P}Q(\bar{r}\bar{s} + \bar{s}s)}^{\text{mirror case}}$$



$$\text{Above work} = f = a \oplus b \oplus c \oplus d$$

$$= a \oplus b \oplus c \odot d$$

for PDN

for PUN

\bar{f}

\downarrow

product \rightarrow series

Sum \rightarrow parallel.

f

\downarrow

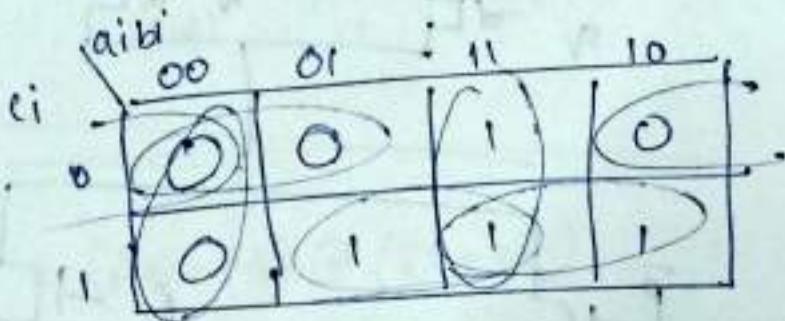
product \rightarrow series

Sum \rightarrow parallel

Mirror

Full adder \rightarrow 3-input 2-output function.

a_i	b_i	c_i	S_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	1
1	1	1	1	1



Inverting properties

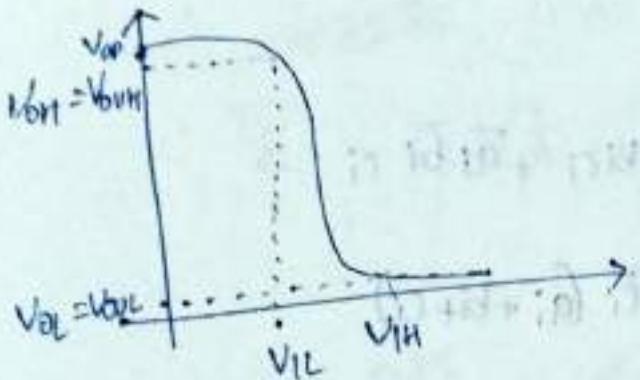
$$C_{i+1} = a_i b_i + b_i c_i + a_i c_i$$

$$\bar{C}_{i+1} = \bar{a}_i \bar{b}_i + \bar{b}_i \bar{c}_i + \bar{a}_i \bar{c}_i$$

$$\bar{C}_{i+1}(a_i, b_i, c_i) = C_{i+1}(\bar{a}_i, \bar{b}_i, \bar{c}_i)$$

$$V_{DD} = 1V, V_{TN} = |V_{TP}| = 0.3V$$

find $V_{IH}, V_{OH}, V_{OL}, NM_L, NM_H$



$$V_{IH} = \frac{1}{8}(8V_{DD} - 2V_{TN}) = 0.85V$$

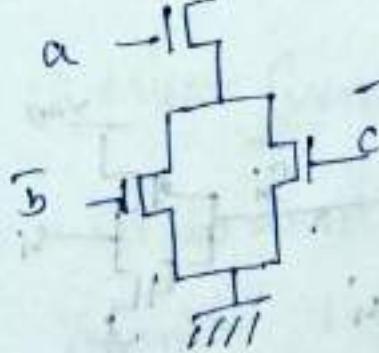
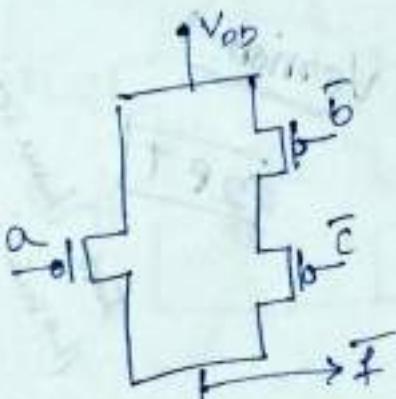
$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{TN}) = 0.45V$$

$$f = a(\bar{b} + c)$$

$$\bar{f} = \overline{a(\bar{b} + c)} = \bar{a} + b\bar{c}$$

$$\bar{f} = 1, \bar{a} = 1 \Rightarrow a = 0$$

$$\begin{array}{l} \boxed{b=1} \\ \downarrow \\ \bar{b}=0 \end{array} \quad \begin{array}{l} \boxed{c=1} \\ \downarrow \\ c=0 \end{array}$$



implement from f , then you get \bar{f} in o/p, now implement PUN from $\bar{f} = 1$ which means $\bar{a} = 1 \Rightarrow a = 0$, $b = 1 \Rightarrow \bar{b} = 0$, $c = 1 \Rightarrow \bar{c} = 0$

because 'PMOS will be ON when = 0'.

$$S_i = a_i \oplus b_i \oplus c_i$$

$$\rightarrow \bar{a}_i b_i \bar{c}_i + a_i \bar{b}_i \bar{c}_i + a_i b_i c_i + \bar{a}_i \bar{b}_i c_i$$

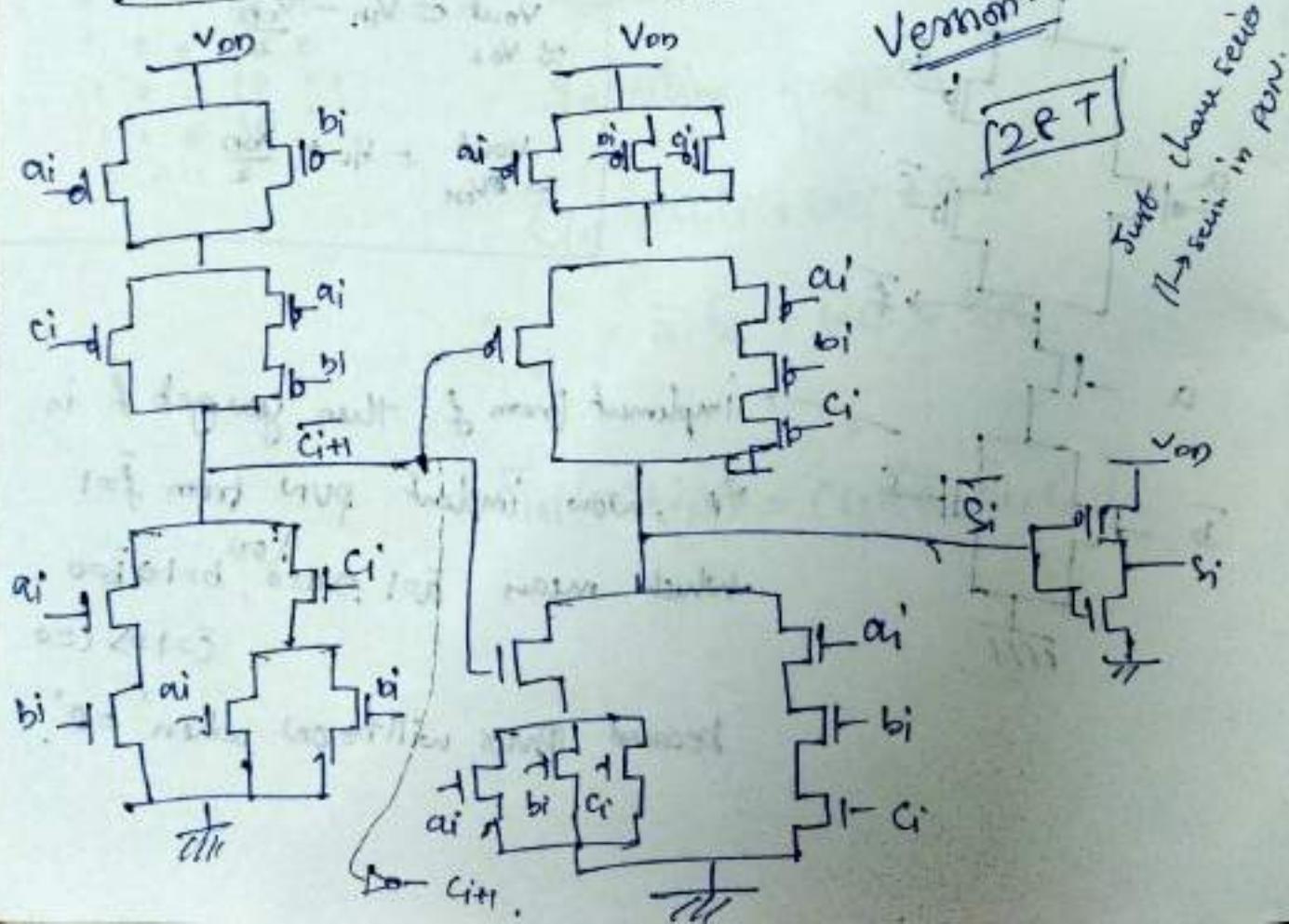
$$= \bar{a}_i \bar{c}_i (a_i + b_i + c_i) + \bar{b}_i \bar{c}_i (a_i + b_i + c_i)$$

$$+ \bar{a}_i b_i (a_i + b_i + c_i) + a_i b_i c_i$$

$$= (\bar{a}_i \bar{c}_i + \bar{b}_i \bar{c}_i + \bar{a}_i b_i) (a_i + b_i + c_i) + a_i b_i c_i$$

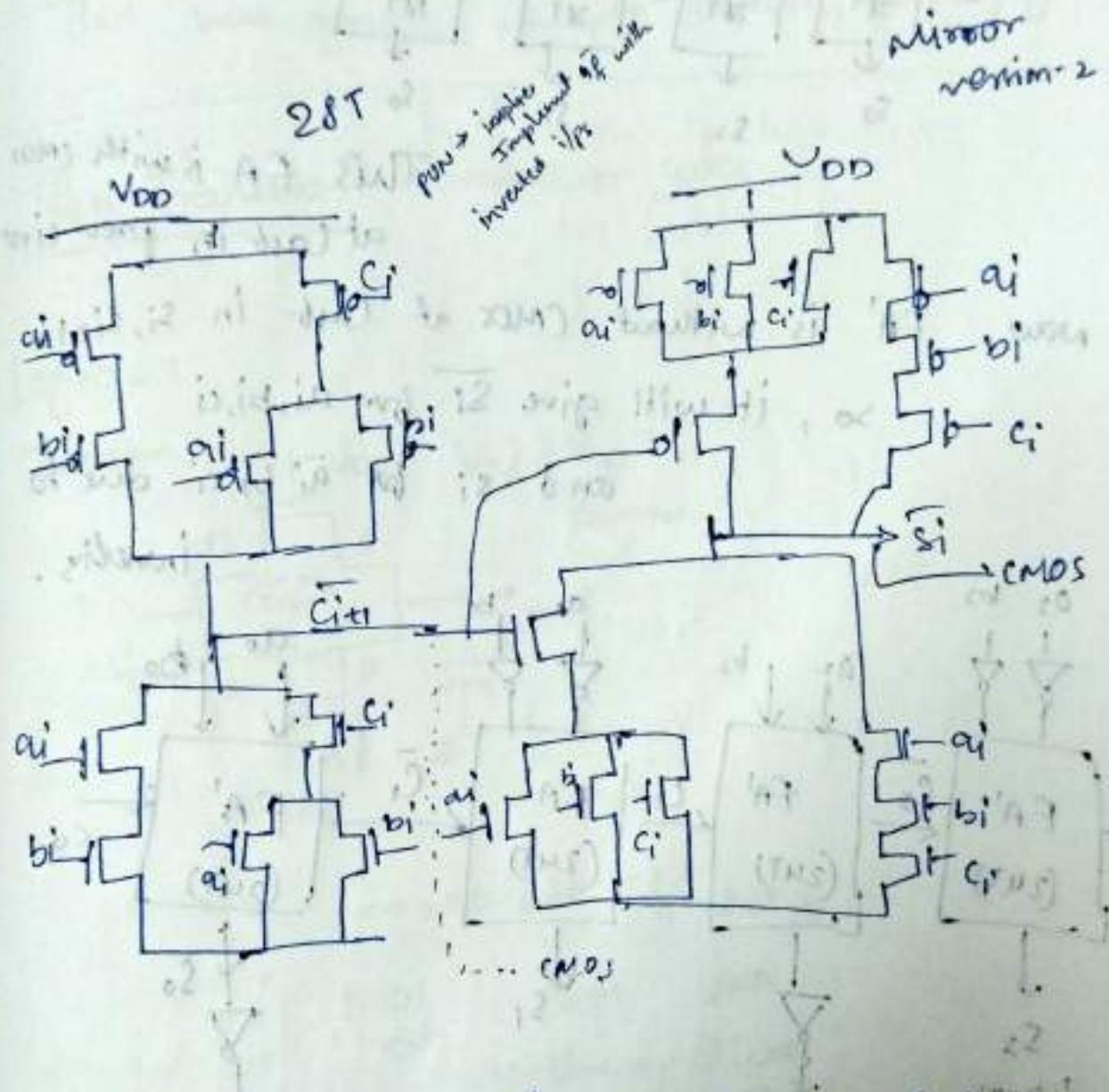
$S_i = \bar{c}_i \bar{a}_i (a_i + b_i + c_i) + a_i b_i c_i$

$C_{i+1} = c_i b_i + c_i (a_i + b_i)$



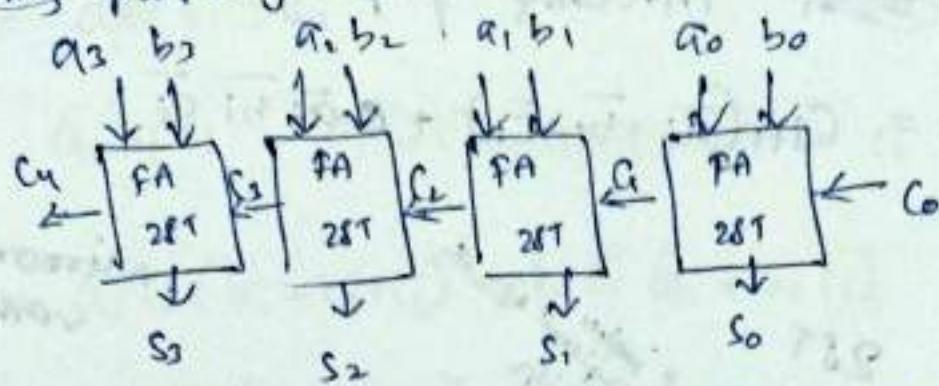
\therefore ~~Si~~ \bar{S}_i inverting property is also for

$$\therefore \bar{S}_i = C_{i+1}(\bar{a}_i + \bar{b}_i + \bar{c}_i) + \Theta \bar{a}_i \bar{b}_i \bar{c}_i$$



\rightarrow Mirror (version 2) charges \bar{s}_i , C_{i+1} fast even in slowest case scenario, because less transition between V_{DD} & \bar{s}_i , C_{i+1}

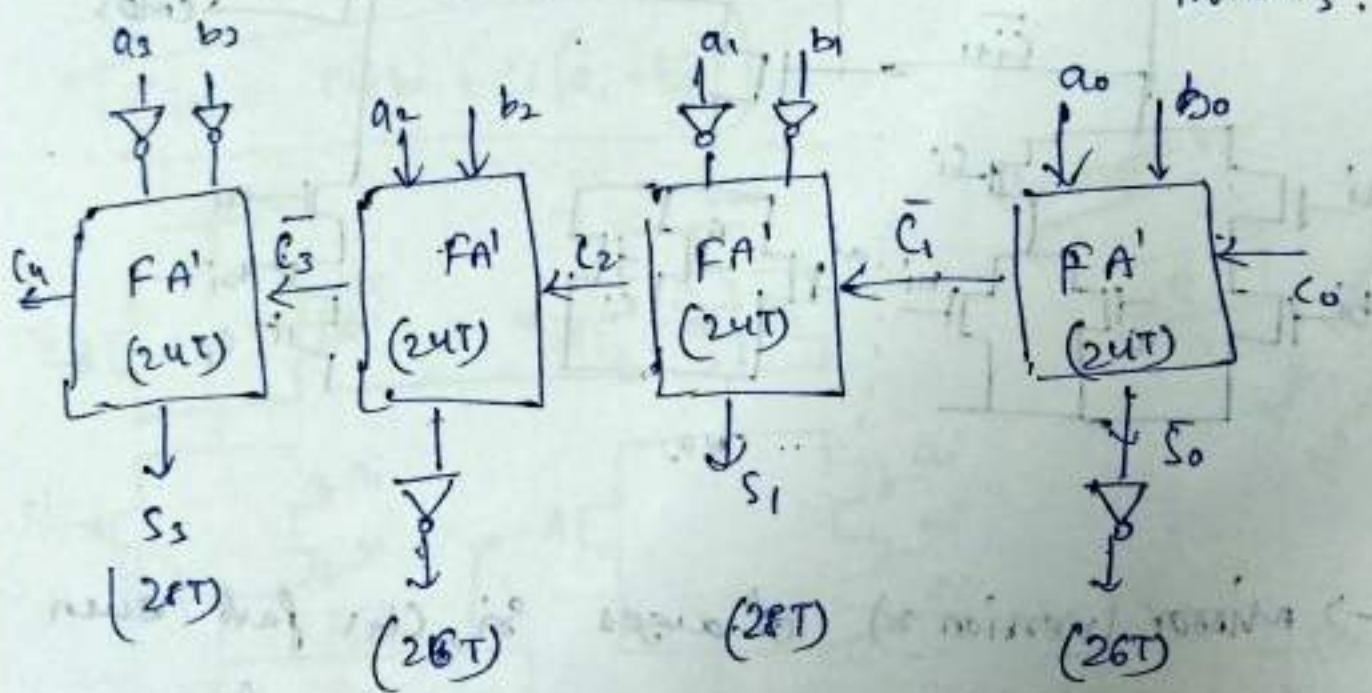
Inverting property to



This FA is with CMOS
at least in previous

now, FA' is without CMOS at least in s_i, \bar{c}_i .

so, it will give \bar{s}_i for a_i, b_i, c_i
and s_i for $\bar{a}_i, \bar{b}_i, c_i$ due to
inverters.



Homework

Subtraction.

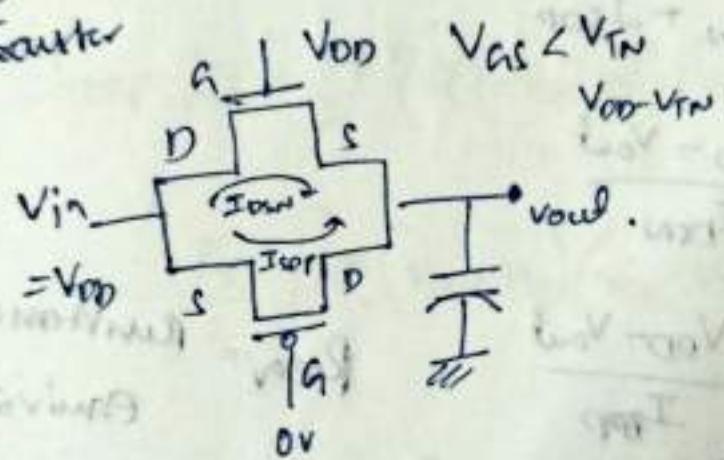
Using FA block \Rightarrow savings, n-bit RCA in transistors (Area wise).
 Reduct in delay = $n \cdot t_{inv}$

This was possible due to inverting property of inverter

Pair Transmission: Transmission gates

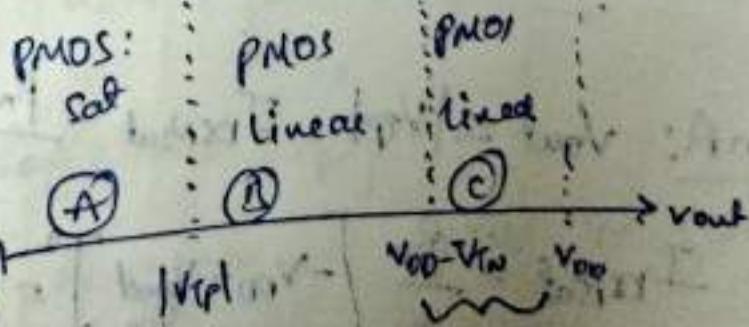
Logic - 1

Transistor



Interactions

\rightarrow NMOS: on \rightarrow NMOS: off



$$V_{ACN} = V_{DD} - V_{out}$$

$$V_{DCN} = V_{DD} - V_{out}$$

$$V_{ASP} = -V_{DD}$$

$$V_{DSP} = V_{out} - V_{DD}$$

$$V_{DSP} \leq V_{T_P} - V_{DD}$$

$$-V_{DD} + V_{out} = -V_{DD} - V_{T_P}$$

$$-V_{DD} + V_{out} < -V_{DD} + |V_{T_P}|$$

$|V| < |V_{T_P}|$: sat

$> |V_{T_P}|$: linear.

$$I_D = I_{DN} + I_{SP}$$

$$R_{eqN} = \frac{V_{DD} - V_{out}}{I_{DN}}$$

$$R_{eqP} = \frac{V_{DD} - V_{out}}{I_{SP}}$$

$R_{eq} = R_{eqN} \parallel R_{eqP}$
resistance
equivalent

$$\boxed{R_{eq} = R_{eqN} \parallel R_{eqP}}$$

Region A: $V_{out} \leq |V_{T_P}|$ $I_{DSNsat} = \frac{\beta_N}{2} [V_{DD} - V_{out} - V_{TN}]^2$

$$I_{DPSat} = \frac{\beta_P}{2} [-V_{DD} - V_{out}]^2 = \frac{\beta_P}{2} [V_{DD} + V_{TP}]^2$$

$$R_{eqN} = \frac{2(V_{DD} - V_{out})}{\beta_N (V_{DD} - V_{out} - V_{TN})^2}$$

$$R_{eqP} = \frac{2(V_{DD} - V_{out})}{\beta_P (V_{DD} + V_{TP})^2}$$

If $\beta_N = \beta_P$ $|V_{TP}| = V_{TN}$ $R_{eqN} > R_{eqP}$.

Region B : $|V_{TP}| < V_{out} < V_{DD} - V_{TN}$

$$I_{DSN, Sat} = \frac{\beta_N}{2} [V_{DD} - V_{out} - V_{TN}]^2$$

$$R_{eqN} = \frac{2(V_{DD} - V_{out})}{\beta_N (V_{DD} - V_{out} - V_{TN})^2}$$

$$I_{DSP, Lin} = \frac{\beta_P}{2} \left[2(-V_{DD} - V_{TP})(V_{out} - V_{DD}) - (V_{out} + V_{DD})^2 \right]$$

$$= \frac{\beta_P}{2} \left[2(V_{DD} + V_{TP})(V_{DD} - V_{out}) - (V_{DD} - V_{out})^2 \right]$$

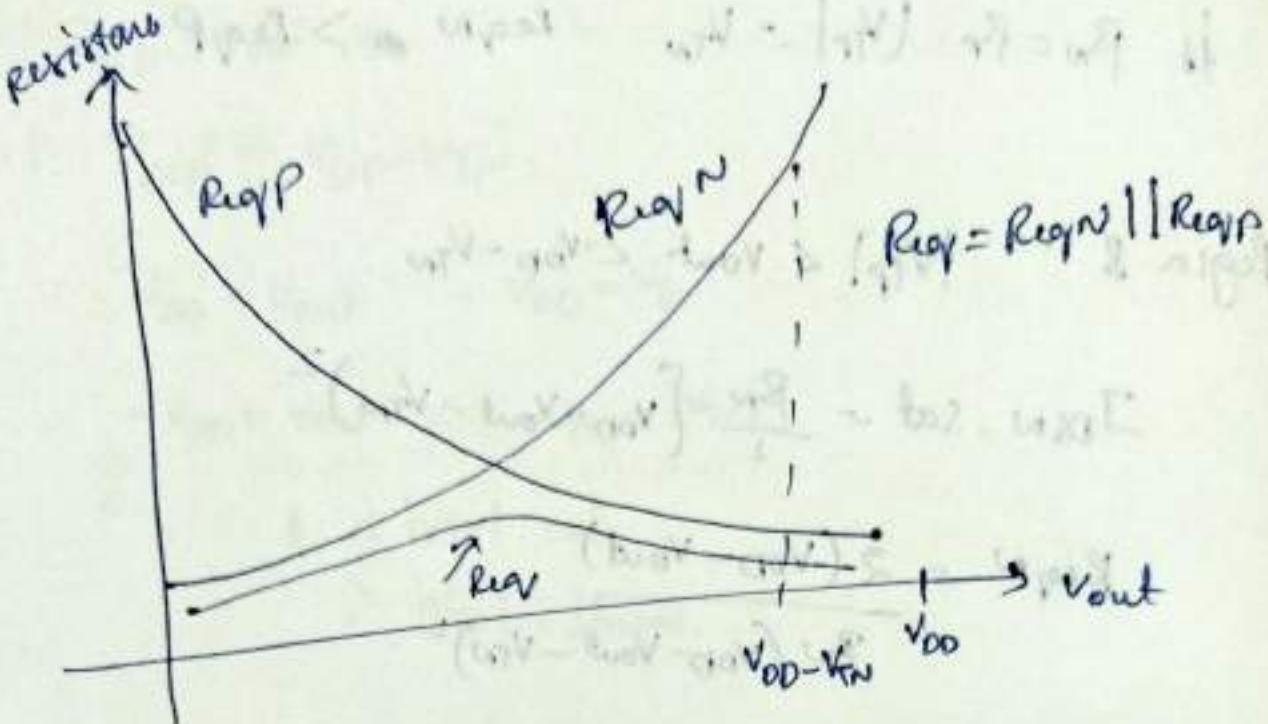
$$\therefore R_{eqP} = \frac{2}{\beta_P [2(V_{DD} + V_{TP}) - (V_{DD} - V_{out})]}.$$

Region C :- $R_{eqNmos} = 0\Omega$ $V_{DD} - V_{TN} < V_{out} < V_{DD}$

$$R_{eqN} = 0\Omega$$

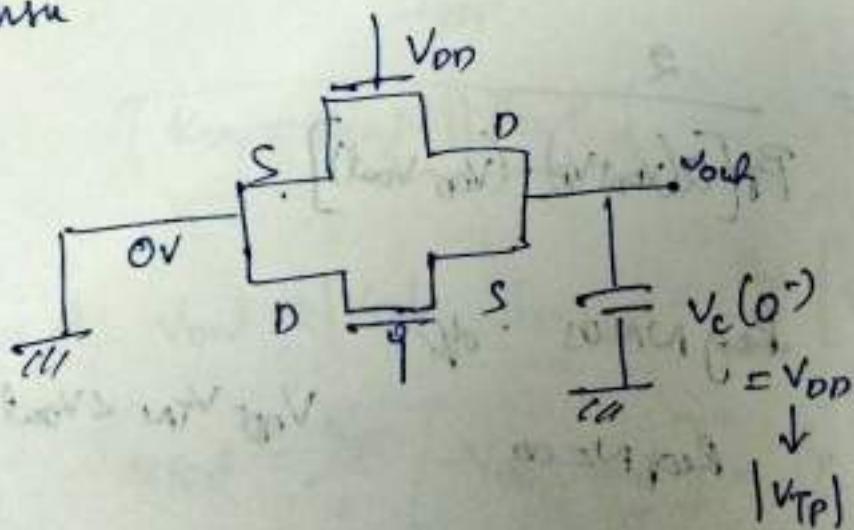
$$R_{eqP} = \frac{2}{\beta_P [2(V_{DD} + V_{TP}) - (V_{DD} - V_{out})]}$$

$R_{eqN}, R_{eqP} \rightarrow$ dependent on V_{out} .

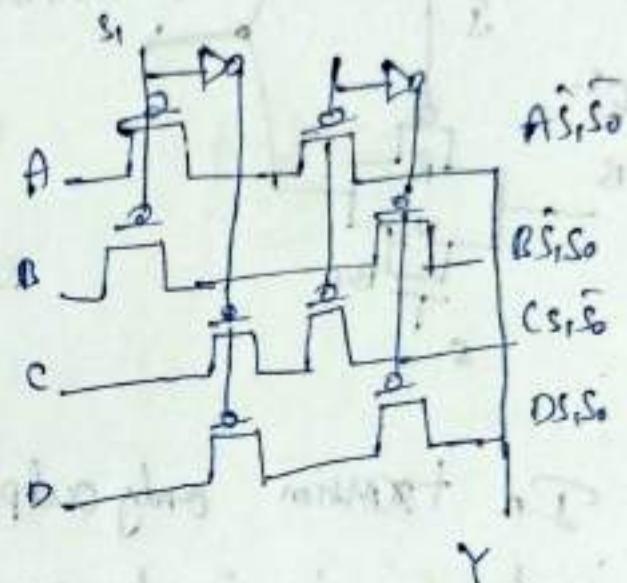
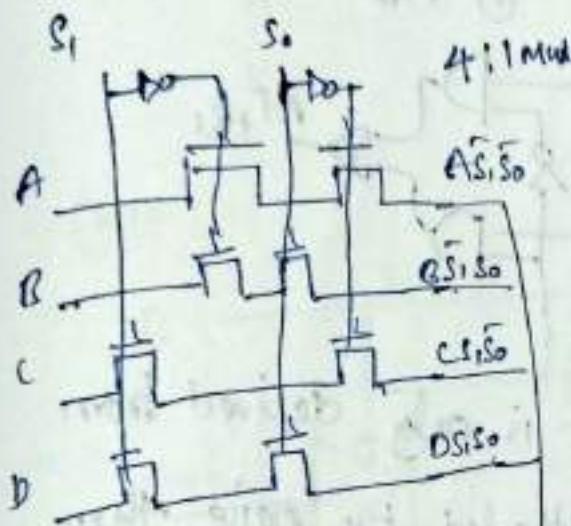
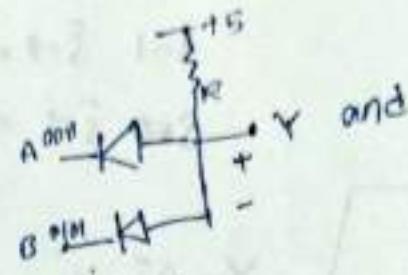
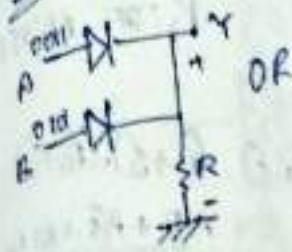


$R_{op} \approx$ almost independent of V_{out}
 (less sensitive)

logic-0
 Transistor

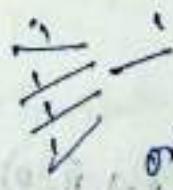


26/Aug/24

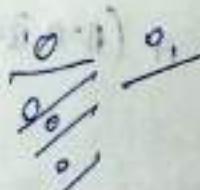


S ₁	S ₀	Y
0	0	A
0	1	B
1	0	C
1	1	D

OR only when

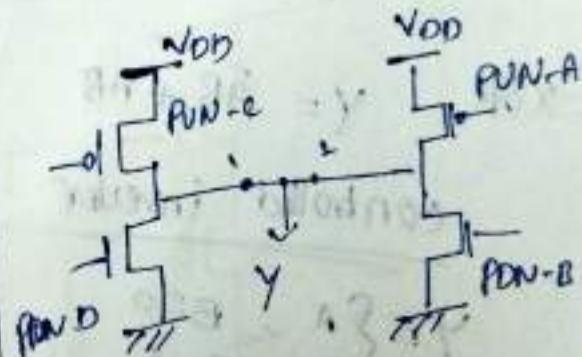


or



if all signal
then don't OR.

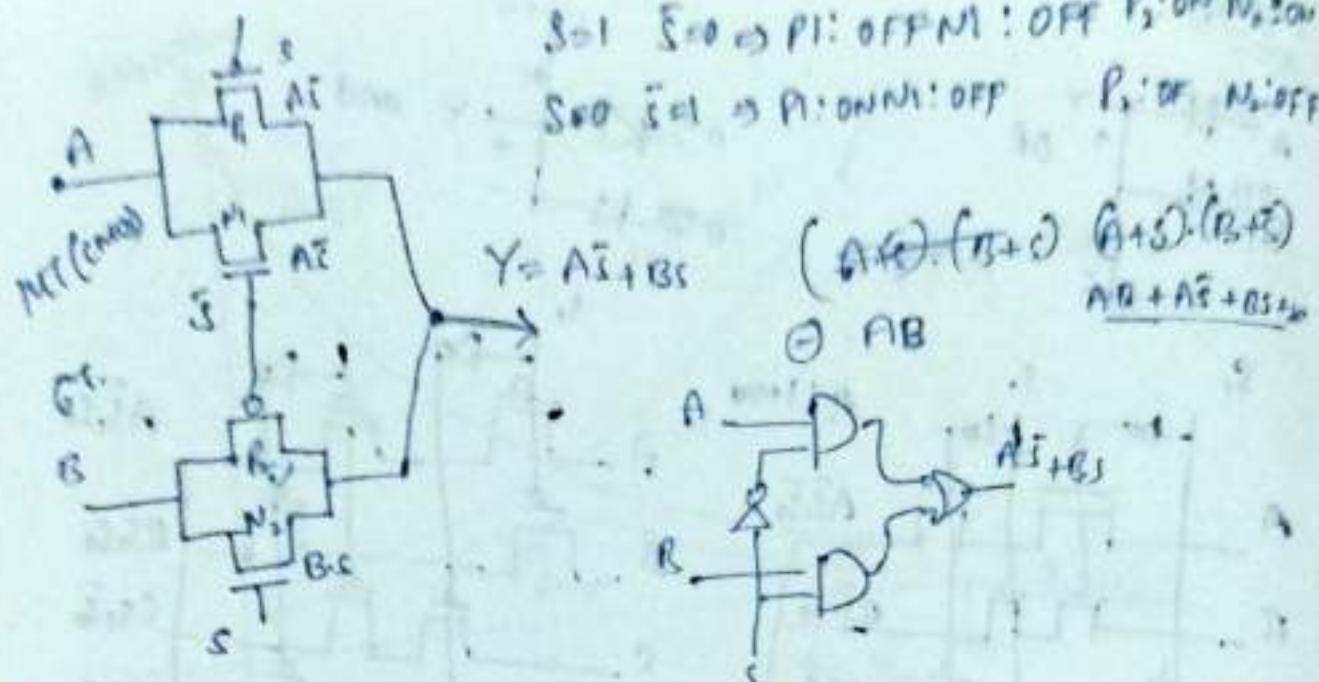
In this
3. signal at
a time is
high impenta
so, only
one signal
can pass.



you can only short 1,2

when C & A are ON
D & B are ON.

C, B ON, A, D are
OFF.



In transmission only output is only derived from input, \therefore if input are affected by noise, then o/p also gets affected. \therefore low noise margin.

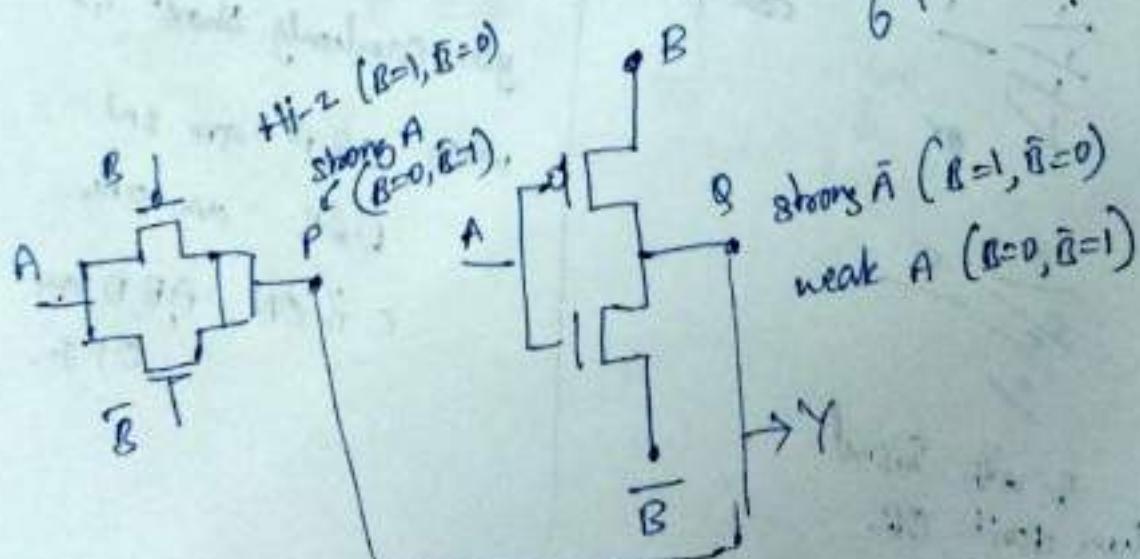
EXOR. $Y = \bar{A}B + A\bar{B}$ 12T (CMOS)

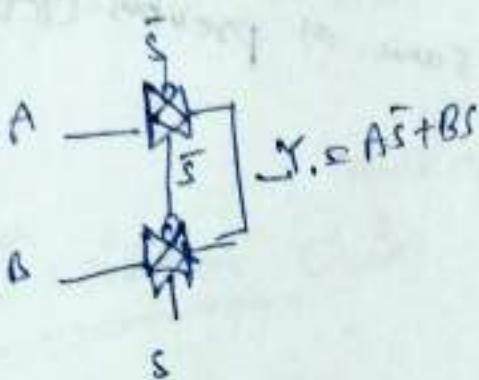
controlled inverter

$$Y = \begin{cases} A & ; B=0 \\ \bar{A} & ; B=1 \end{cases}$$

$$4T + 2E = 6T$$

6T

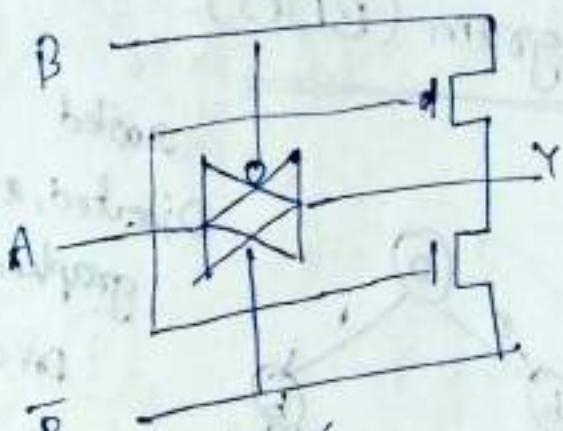




$$Y = A\bar{S} + BS$$

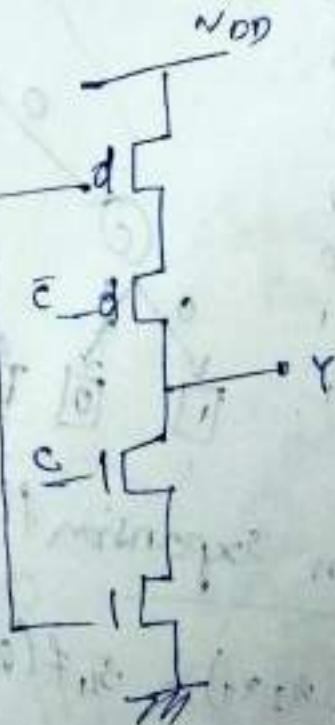


EXOR



Tristate inverter

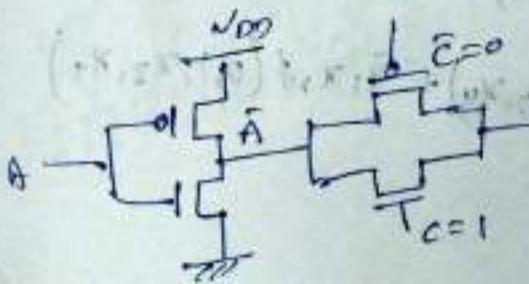
		A	Y
		0	Hi=2
		1	Hi=1
control C	0	0	0
control C	1	0	1
control C	0	1	1
control C	1	1	0



Tristate

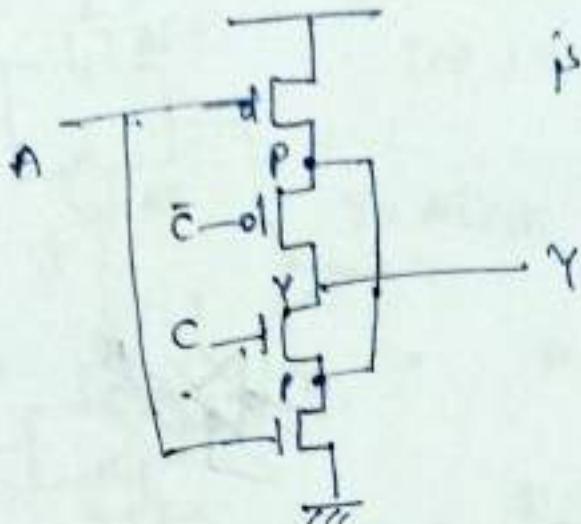
inverter

also



Tristate inverter.

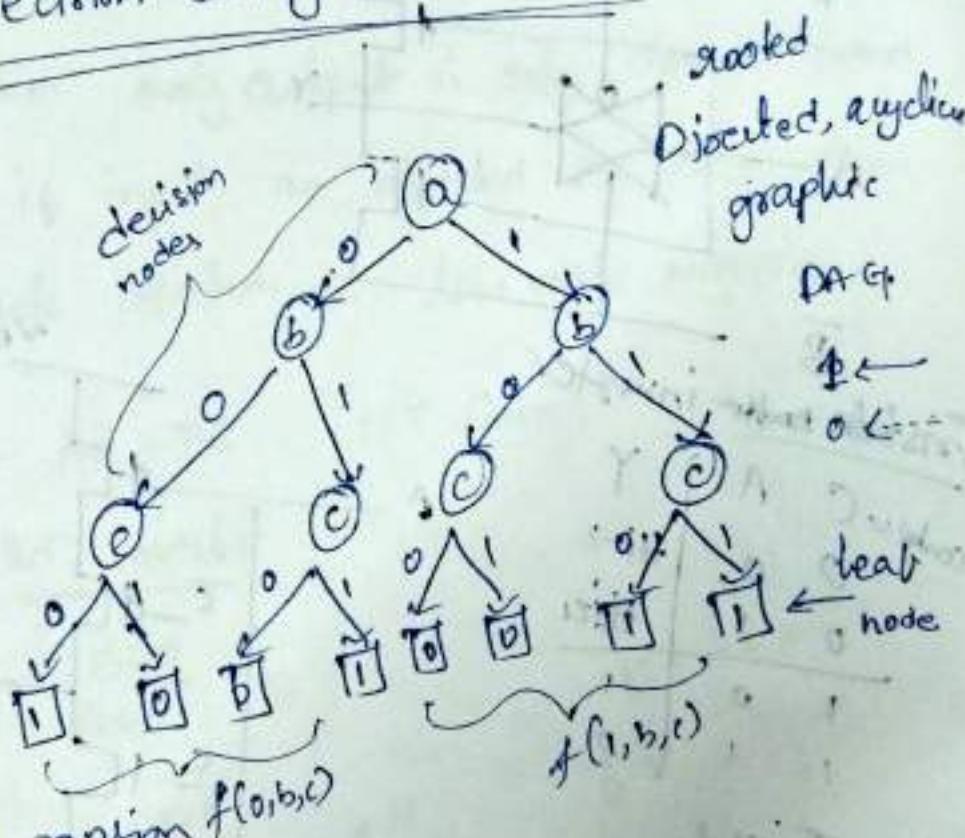
also



is same as previous Clct.

Binary Decision Diagram (BDD)

a	b	c	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Shannon Expansion

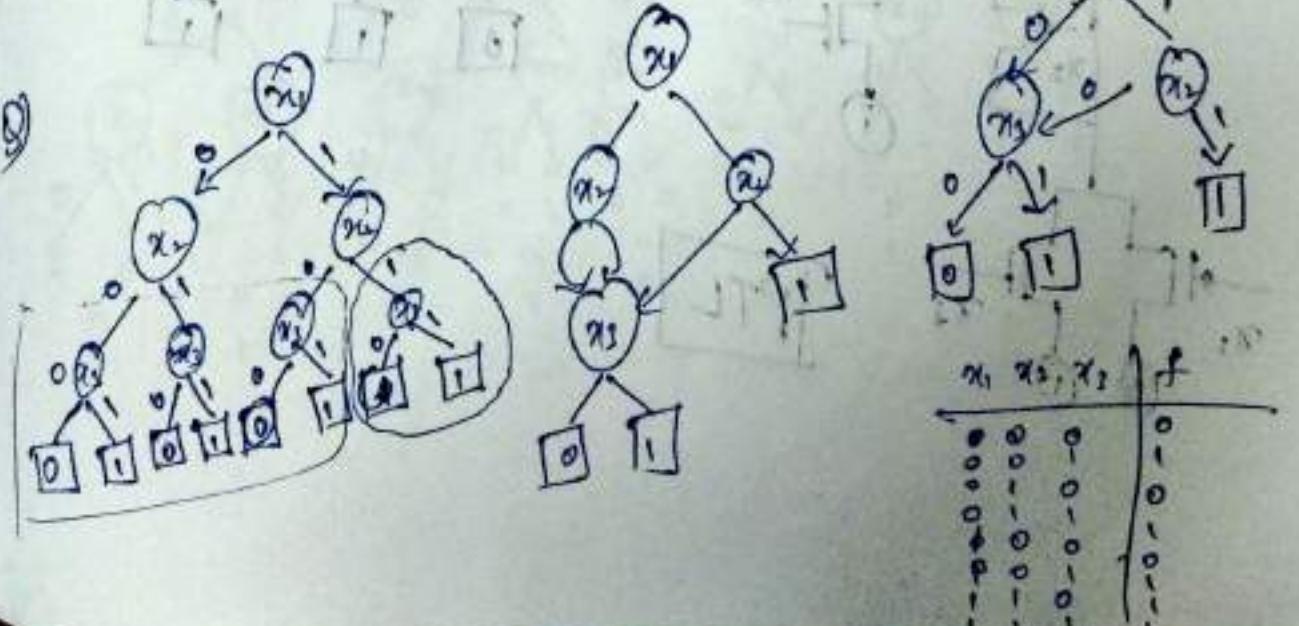
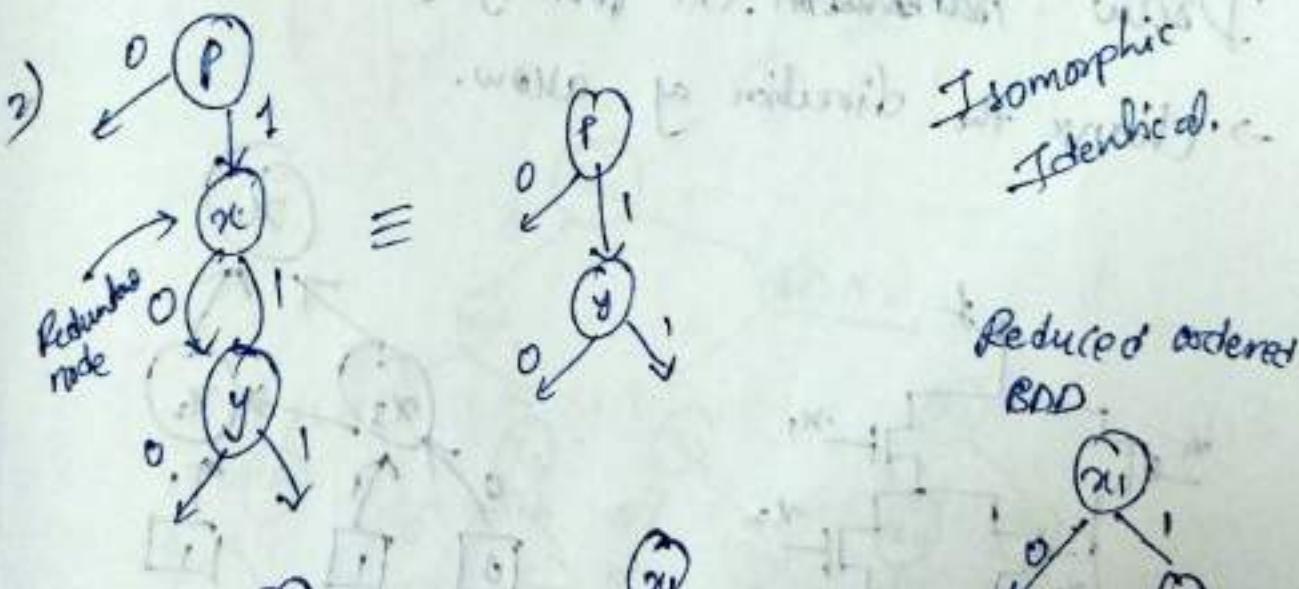
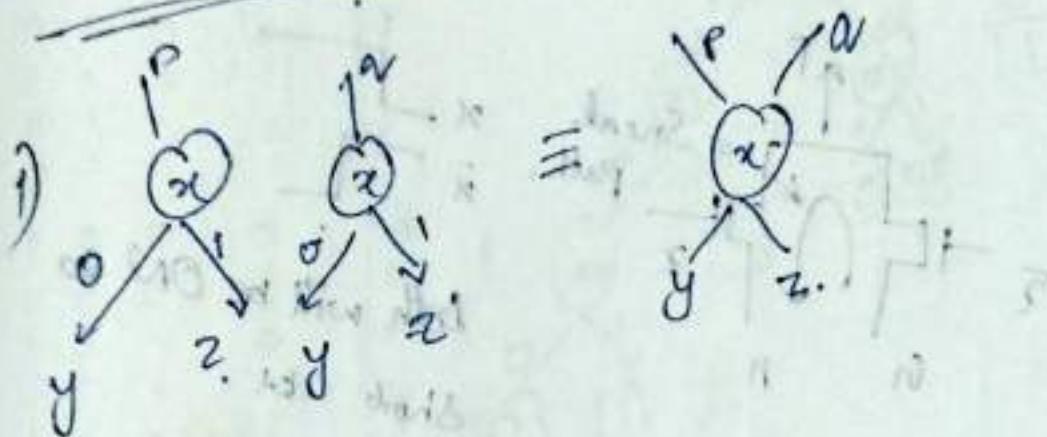
$$\begin{aligned}
 f(x_1, x_2, x_3, x_4) &= \bar{x}_1 f(0, x_2, x_3, x_4) + x_1 f(1, x_2, x_3, x_4) \\
 &= \bar{x}_1 \bar{x}_2 f(0, 0, x_3, x_4) + \bar{x}_1 x_2 f(1, 0, x_3, x_4) + x_1 \bar{x}_2 f(0, 1, x_3, x_4) \\
 &\quad + x_1 x_2 f(1, 1, x_3, x_4)
 \end{aligned}$$

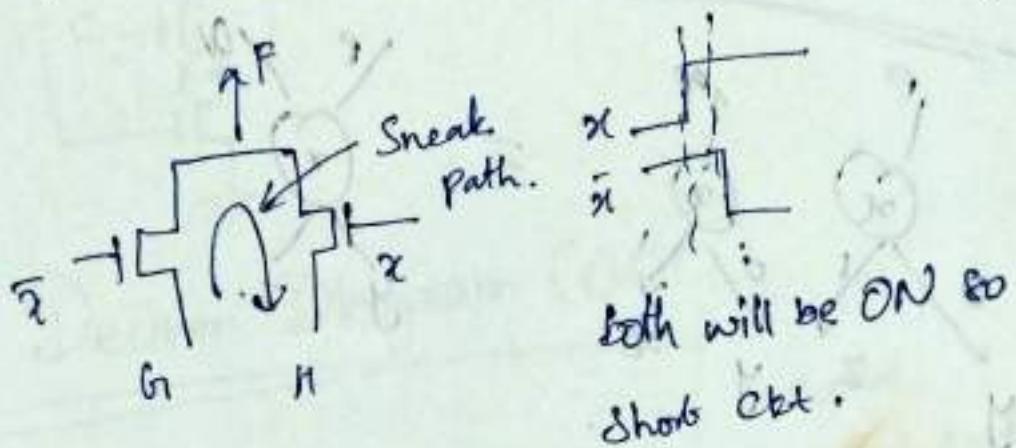
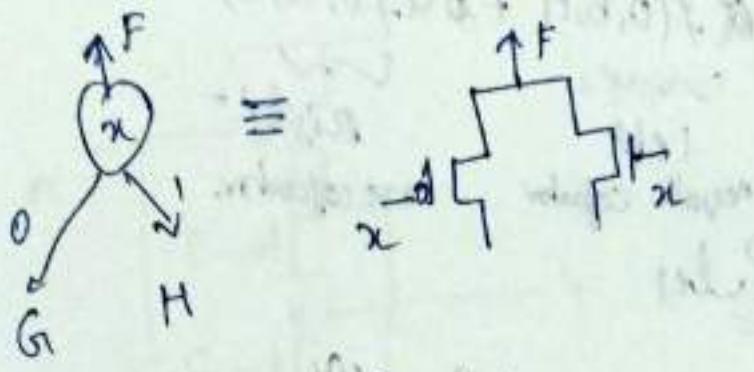
$$\therefore f(a, b, c) = \overline{a}f(0, b, c) + a.f(1, b, c)$$

\leftarrow \text{left} \quad \text{right}

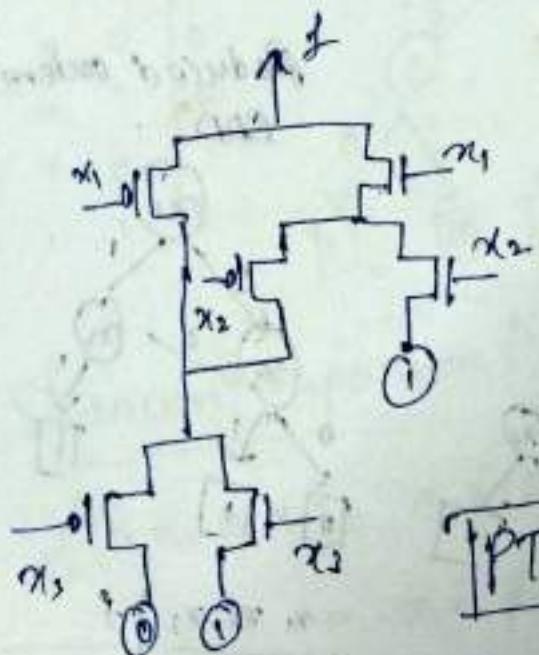
regular cofactor \quad plus cofactor.

Deduction Rules

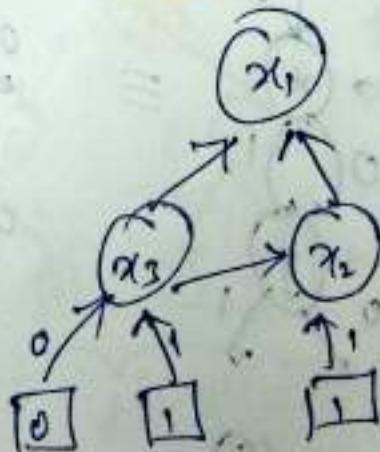




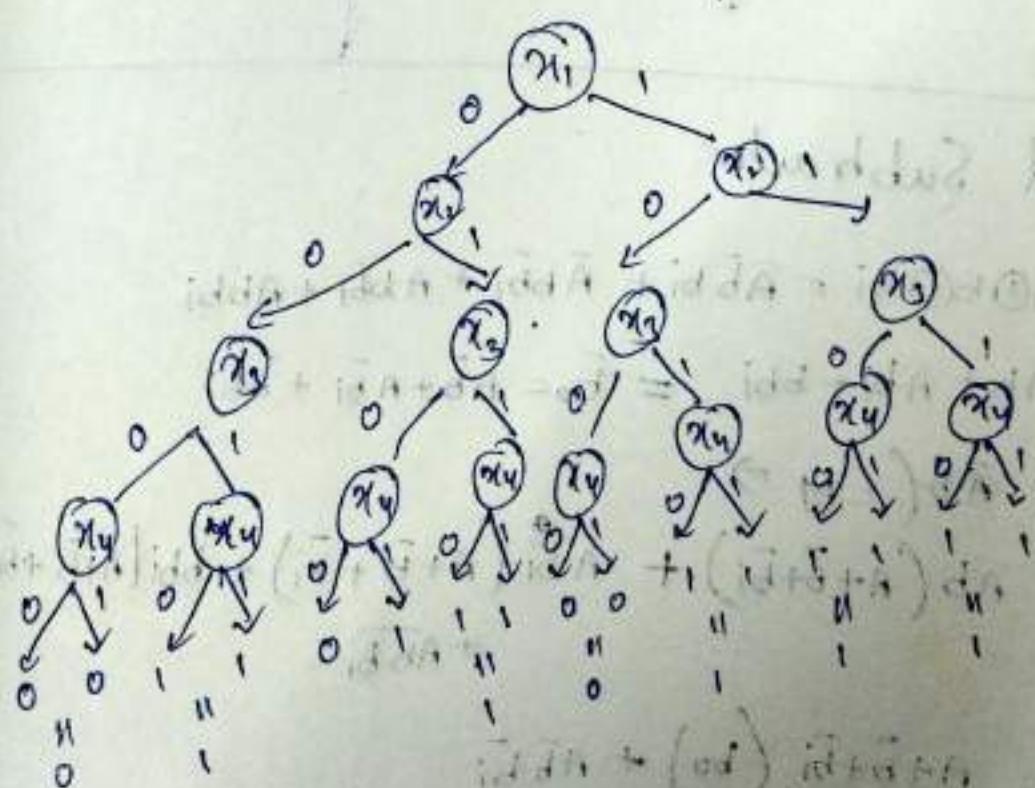
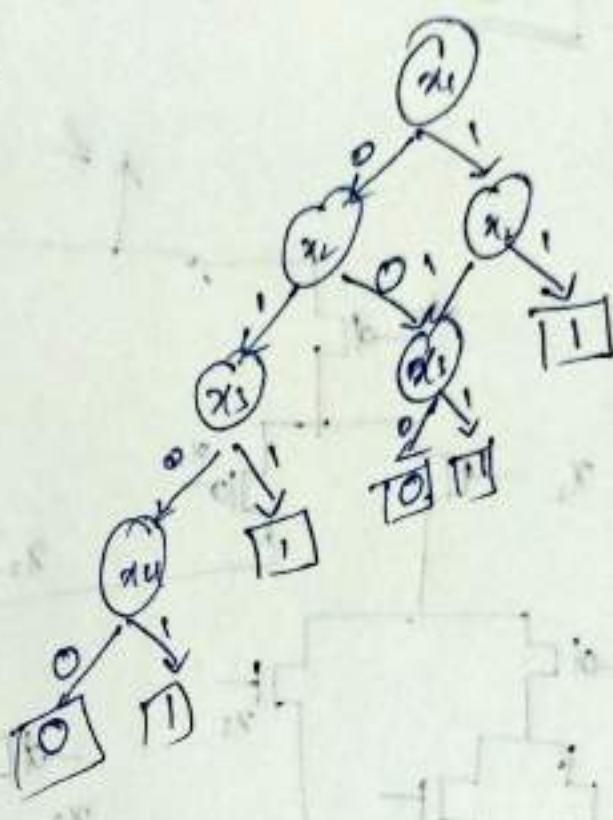
Draw Transmission ckt from graph
→ change the direction of arrow.



PTL

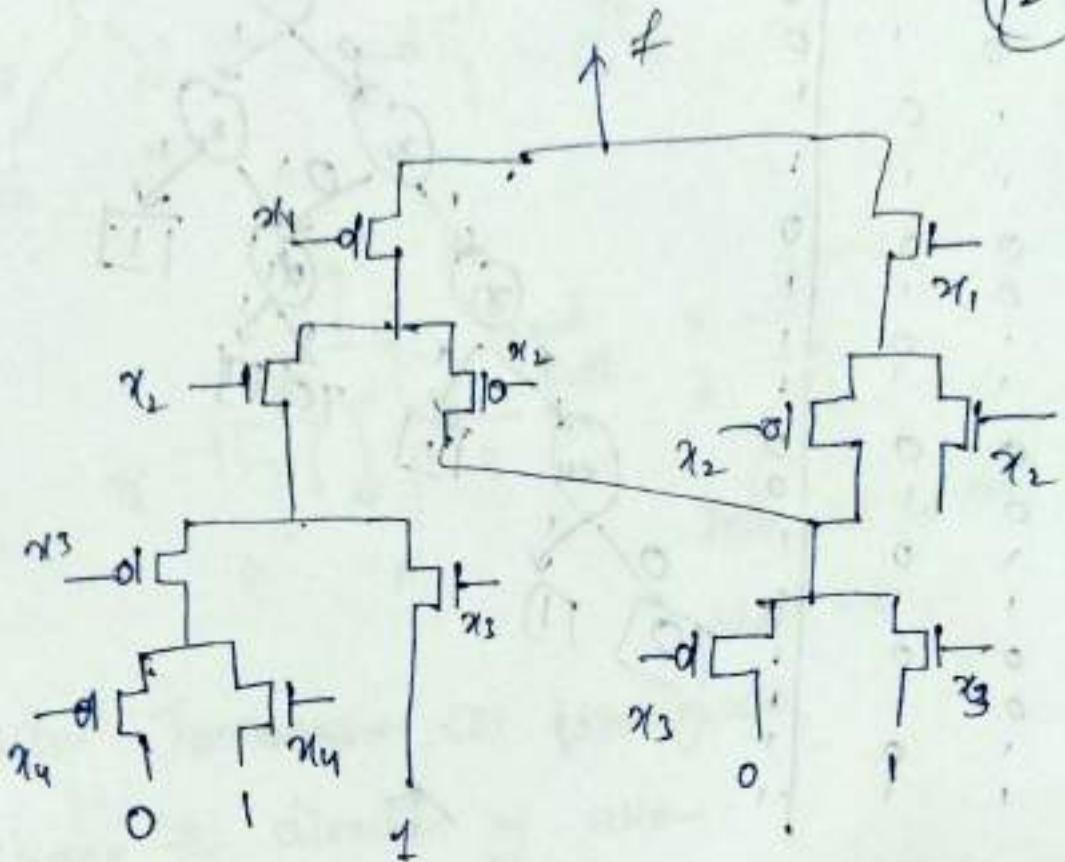


x_1	x_2	x_3	x_4	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



PTL

(12 T)



Full Subtractor

$$\delta d = A \oplus b \oplus b_i = \bar{A} \bar{b} b_i + \bar{A} b \bar{b}_i + A \bar{b} \bar{b}_i + A b b_i$$

$$b_o = \bar{A} b + \bar{A} b_i + b b_i = \bar{b}_o = A \bar{b} + A \bar{b}_i + \bar{b} \bar{b}_i$$

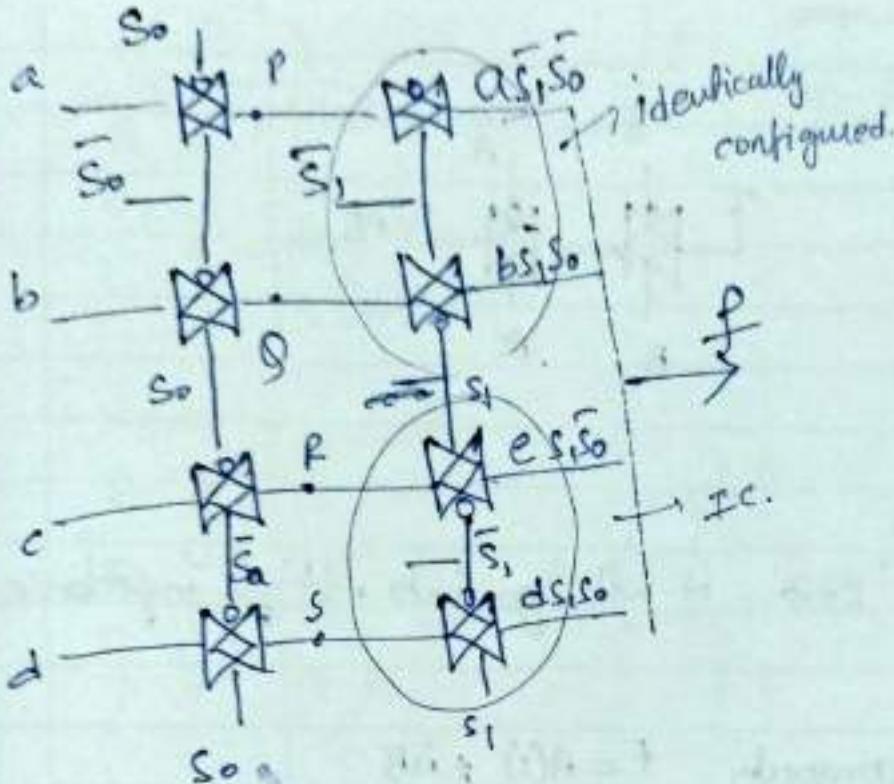
$$\Rightarrow \cancel{\bar{A} b} (\cancel{- b}) \Rightarrow$$

$$\Rightarrow \bar{A} b (A + \bar{b} + \bar{b}_i) + \bar{A} b_i (A + \bar{b} + \bar{b}_i) + b b_i (A + \bar{b} + \bar{b}_i) \\ + \bar{A} \bar{b} \bar{b}_i$$

$$d = A + \bar{b} + \bar{b}_i (b_o) + A \bar{b} \bar{b}_i$$

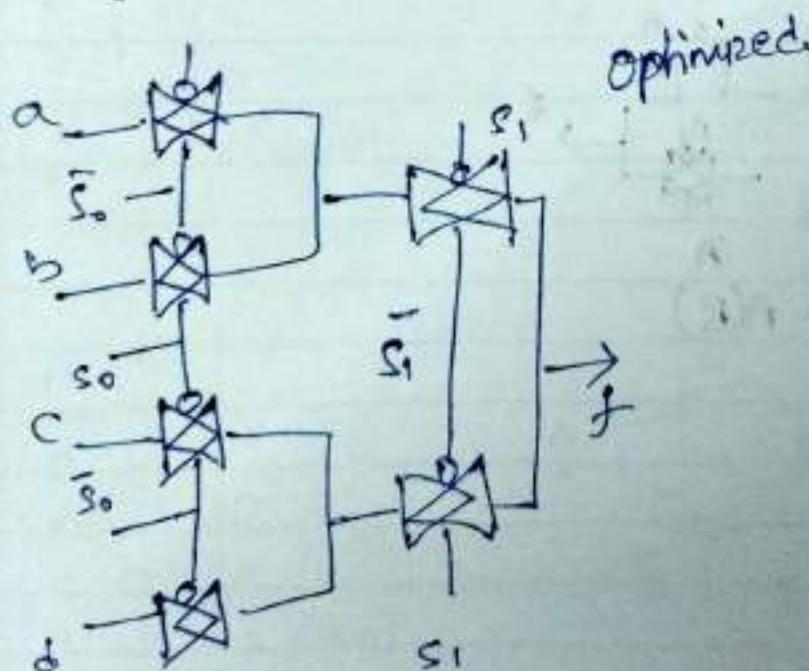
$$\delta = (A + b_o + b_i)(\bar{b}_o) + \bar{A} b b_i$$

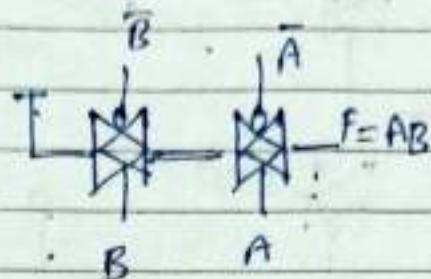
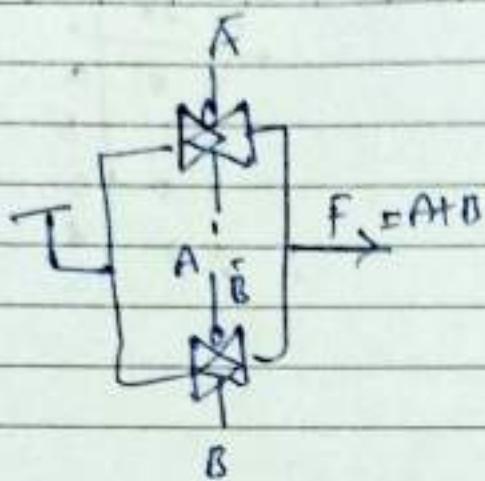
28/Aug/27



S_1	S_0	f
0	0	a
0	1	b
1	0	c
1	1	d

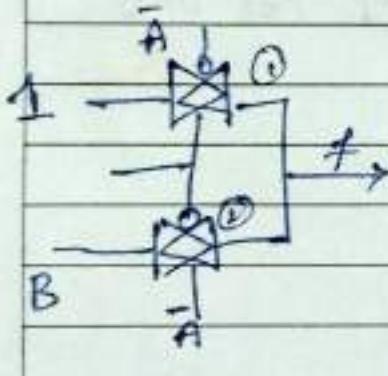
P, Q and can be short circled i.e OR co. only
only will work.



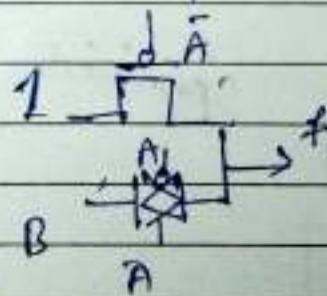


This are wrong for 'zero' it will go into High impedance state.

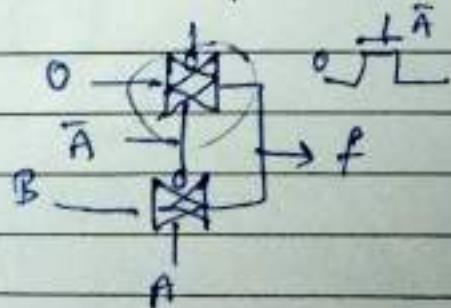
Or can be done properly $F = A(1) + \bar{A}B$



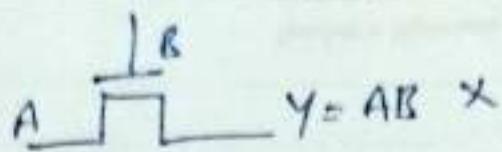
① only Vdd is passing so only PMOS can be used.



AND. $\Rightarrow F = \bar{A}(0) + A(B)$

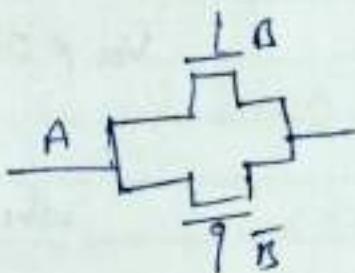


A	B	Y
0	0	Hi-Z
0	1	0
1	0	Hi-Z
1	1	$\frac{1}{(V_{DD} - V_T)}$



$$Y = AB \times$$

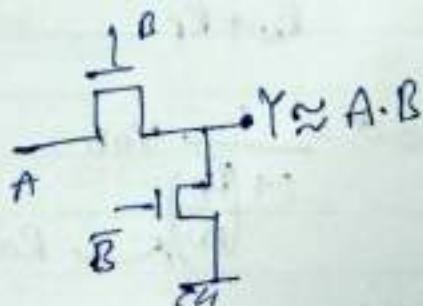
A	B	Y
0	0	Hi-Z
0	1	0
1	0	Hi-Z
1	1	1



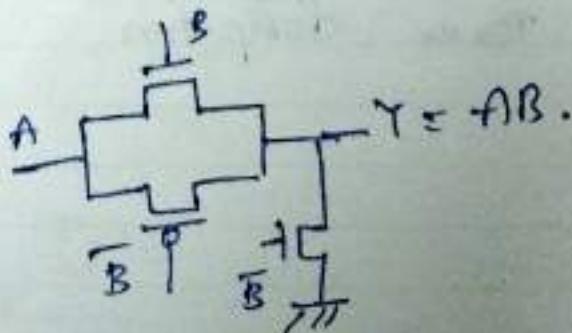
$$Y \approx AB.$$

$V_{DD} - V_T$ problem
solved.

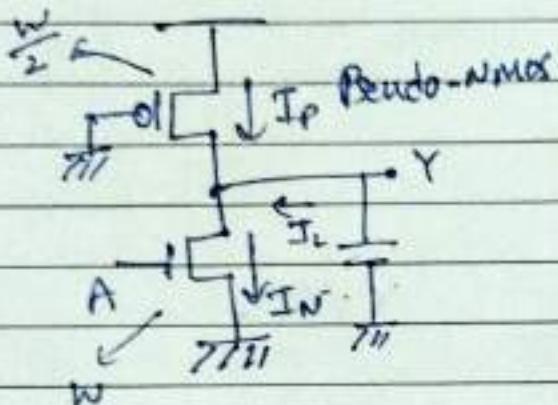
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	$\frac{1}{(V_{DD} - V_T)}$



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	$1 (V_{DD})$



Ratioed logic



takes more time to charge up capacitor.

$$I_N = I_{P} + I_K$$

$$V_{OL} \neq 0V$$

when bulkiness becomes issue

$$R_{out} = \frac{R_N}{R_N + R_P}$$

$$V_{out} = \frac{V_{DD}}{1 + \left(\frac{R_P}{R_N}\right)} \text{ Ratioed}$$

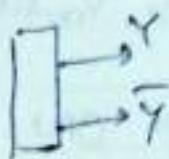
- ① Suffers from
- ② Reduced noise margin
- ③ static power dissipation.

Differential logic

x) dual rail logic (as& \bar{a})

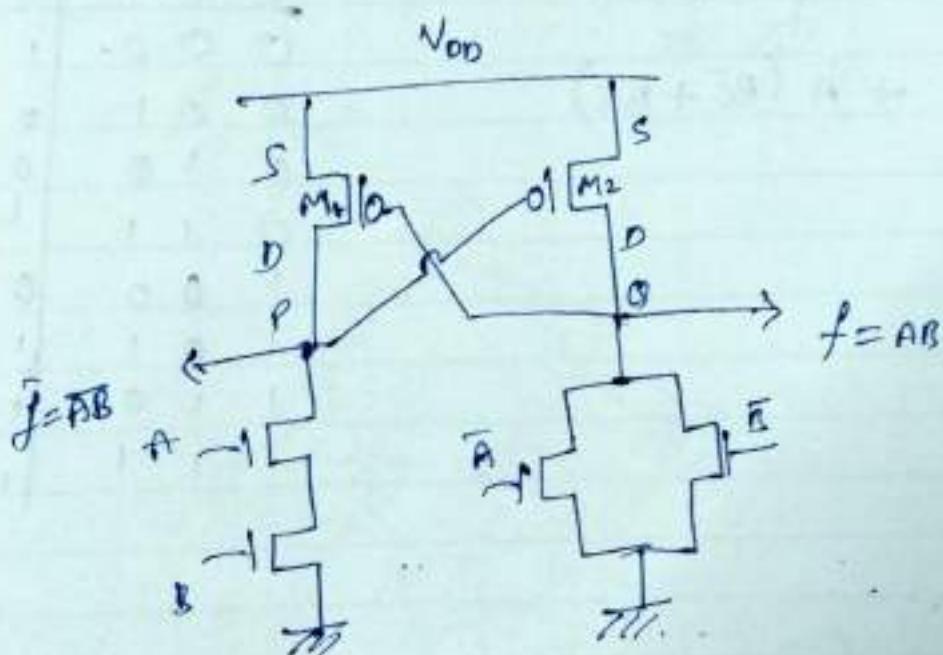
e.g: Cascade voltage switch

logic : (CVSL)



without D_S

- * eliminates static current
- * provide rail to rail swing (0 to V_{DD})
- * generates uncomp & comp o/p without using extra inverter



@ t<0 let $\bar{f}=1$ ($P=1$)

@ t>0 A=1, B=1.

P starts discharging $\Rightarrow \bar{f}$ falls

$$\hat{f} : V_{DD} \rightarrow V_{DD} + V_{TP} \quad (V_{DD} - |V_{TP}|)$$

M_2 turns ON.

Q starts charging $\Rightarrow f$ rises.

M_1 turns OFF eventually, $V_{DS} < V_{TP}$.

\bar{f} discharging even more faster.

M_2 is heavily conducting.

$\Rightarrow f$ rises faster.

\Rightarrow Rail to Rail swing.

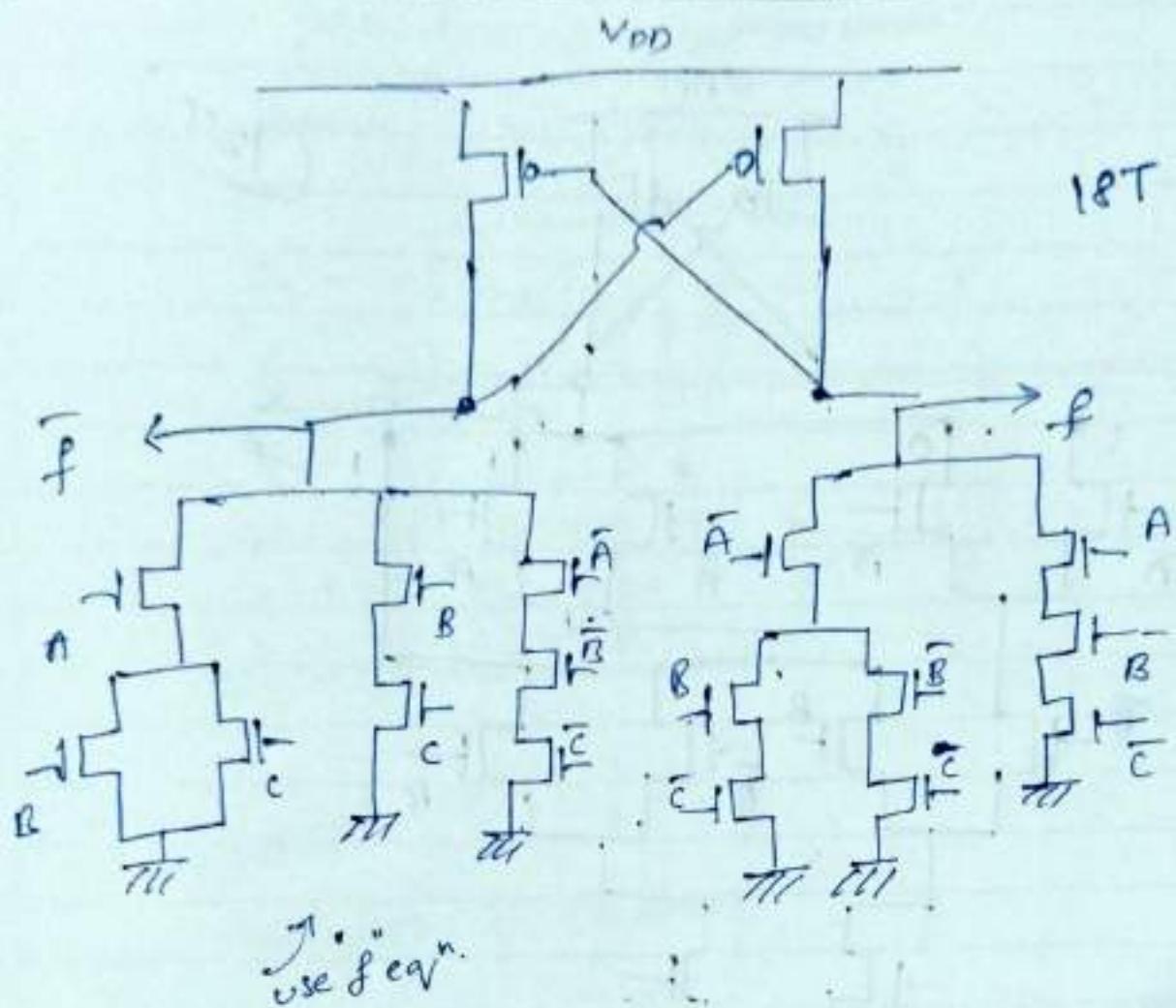
$$\text{Eq: } f = A(B+c) + BC + \bar{A}\bar{B}\bar{C}$$

$$\hat{f} = A\bar{B}\bar{C} + \bar{A}(B\bar{C} + \bar{B}C)$$

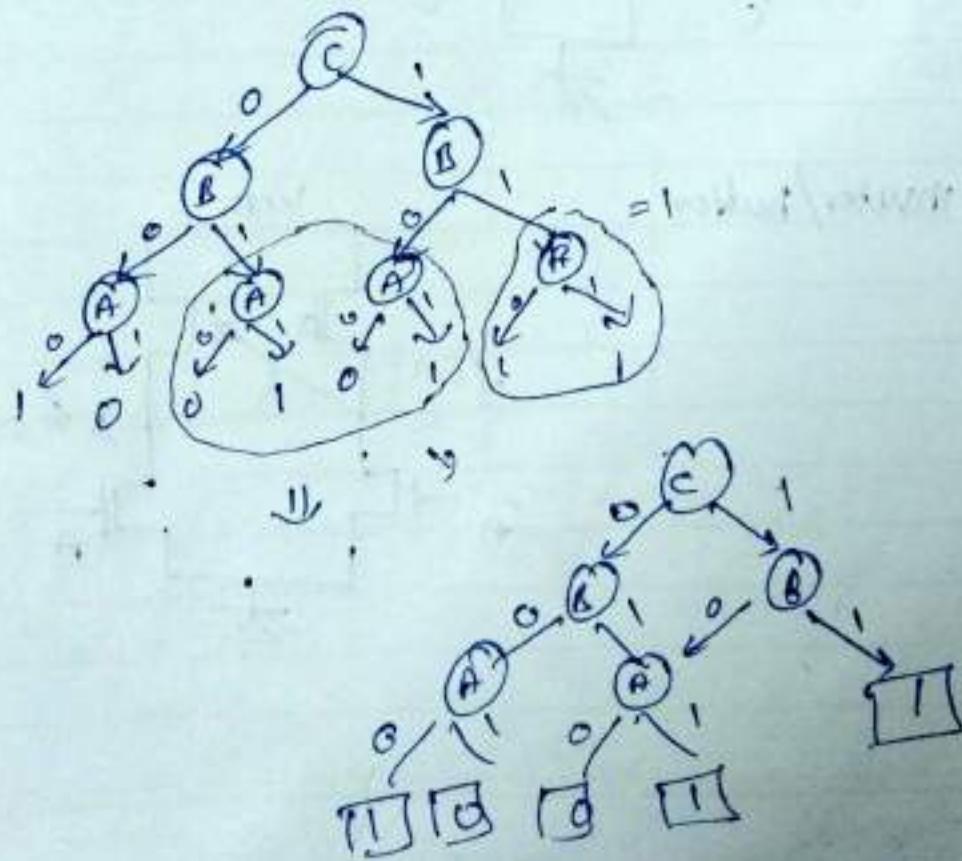
C	B	A	f
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

proposed by PULFREY, CHU / CSVL

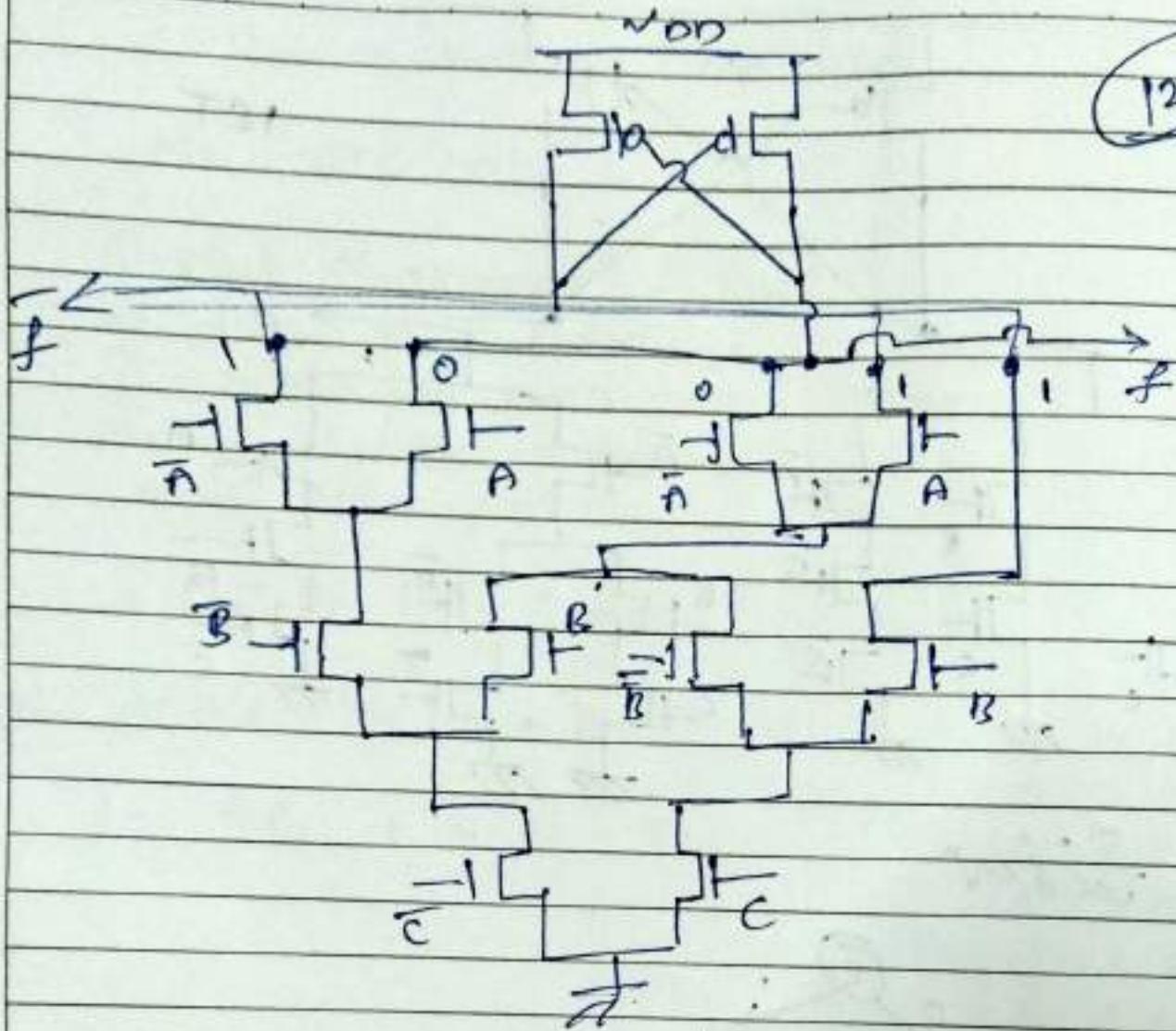
Hedges



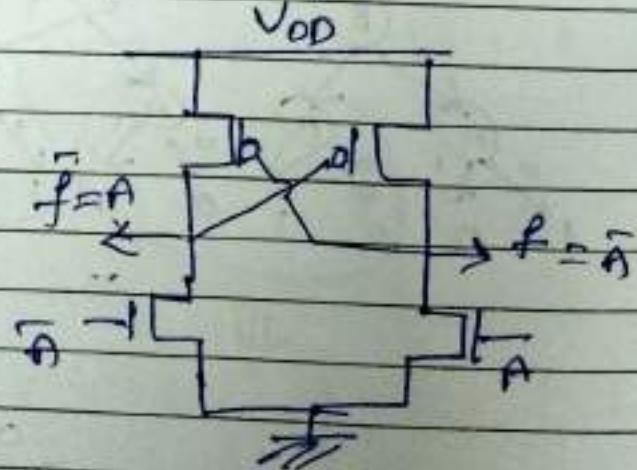
use & eqn.



127



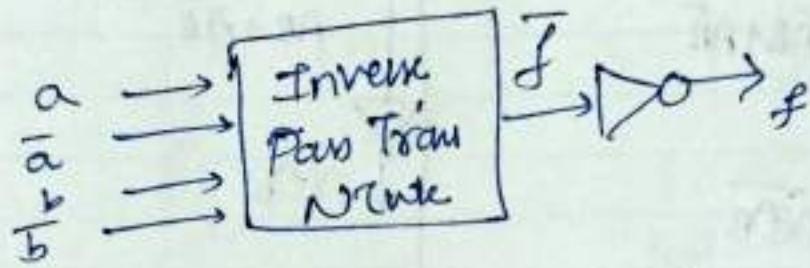
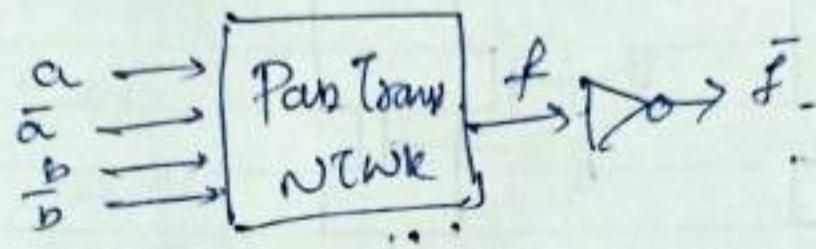
CSVL inverter/buffer



long term

Differential pair transistor logic

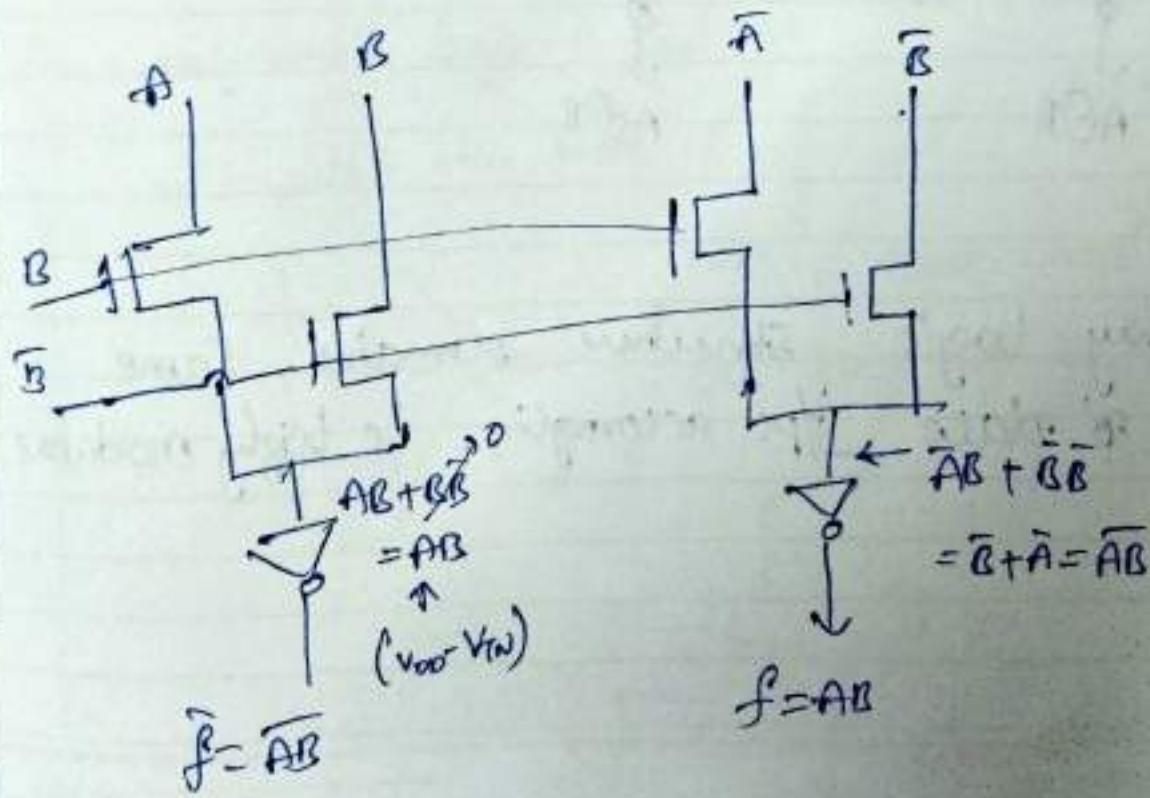
- * complementary Pass Transistor Logic (cPL)

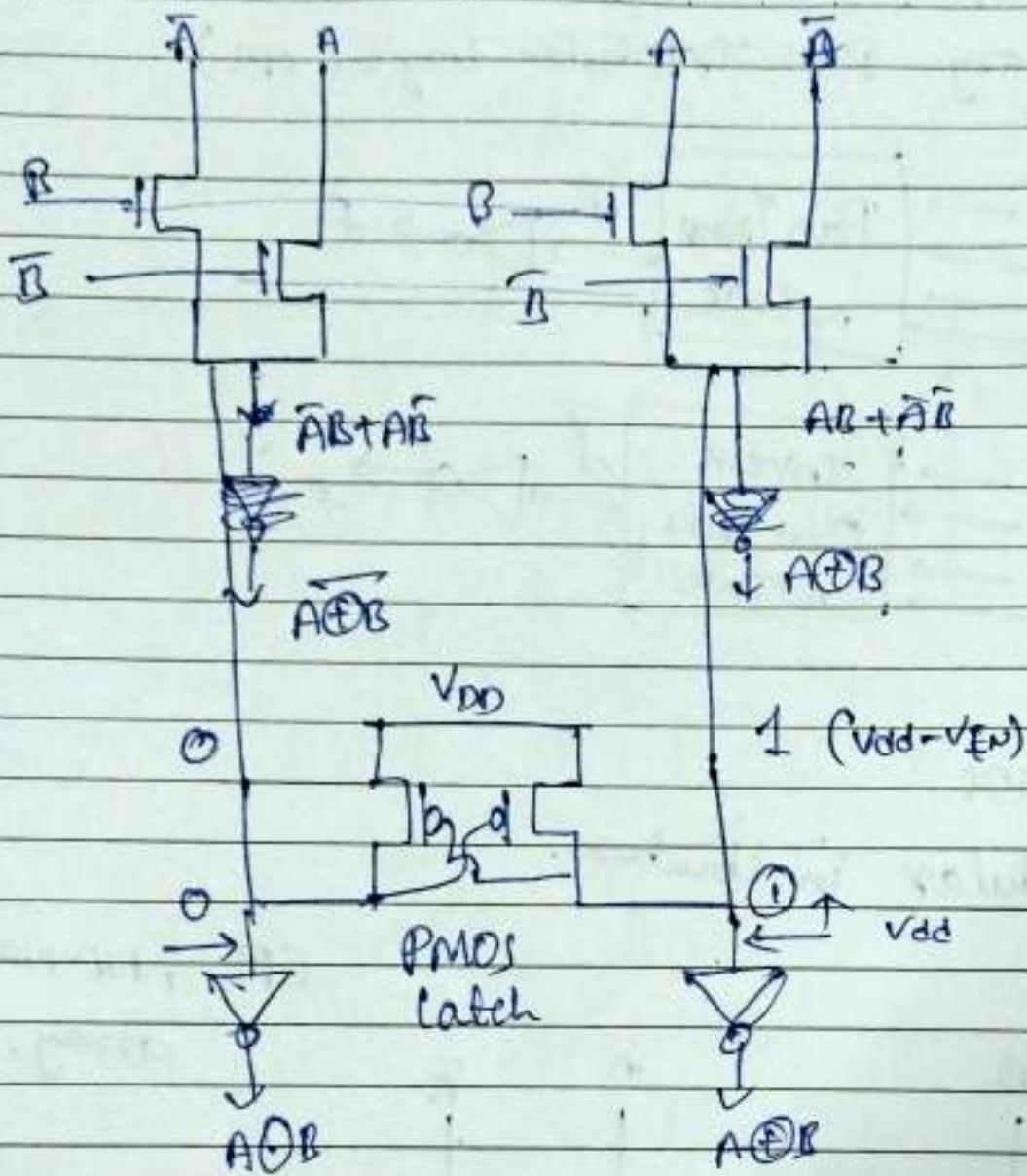


cPL

- * purely NMOS
- * highly modular in structure.

CPL AND-NAND
array.

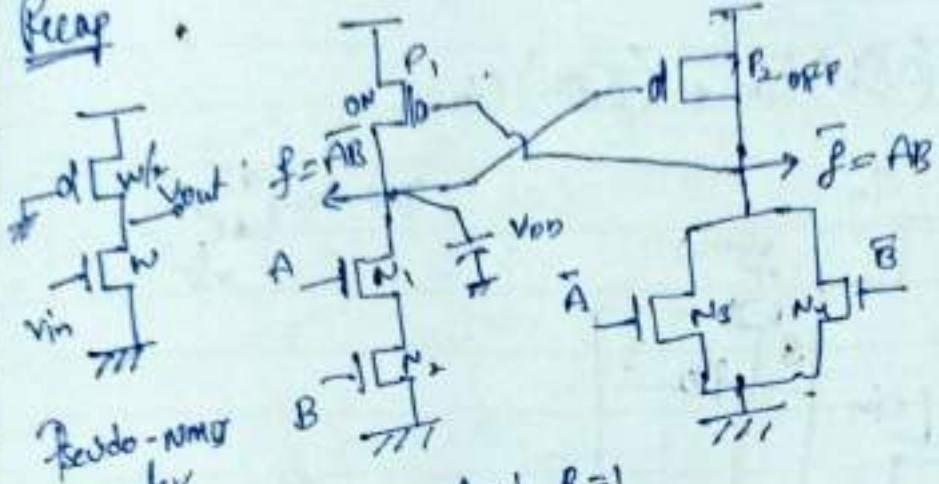




for any logic structure remains same
Just place if's according. ie highly modular

desp29 Kang, Rabey

Recap



PMOS ON

$$v_{in}=0 \rightarrow 1$$

NMOS should

be more strong

than PMOS

$$R_p \gg R_n$$

$$R_{N1} + R_{N2} \ll R_p$$

via ratios.

a_i	b_i	c_i	s_i	c_{in}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
..	..	1	1	1

$$S = a \oplus b \oplus c_{in}$$

$$out = ab + c_{in}(a \oplus b)$$

$$= ab + c_{in}(ab)$$

$$= ab\bar{c}_{in} + c_{in}(ab)$$

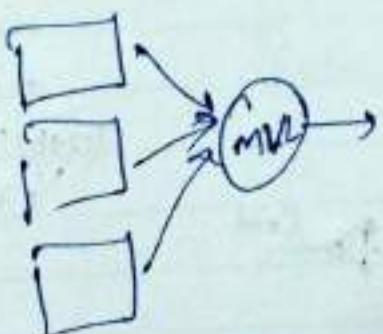
$$S = (\bar{a} \oplus b) \bar{c}_{in} + (\bar{a} \oplus b) c_{in}$$

$$= (\bar{a}b + a\bar{b}) \bar{c}_{in}$$

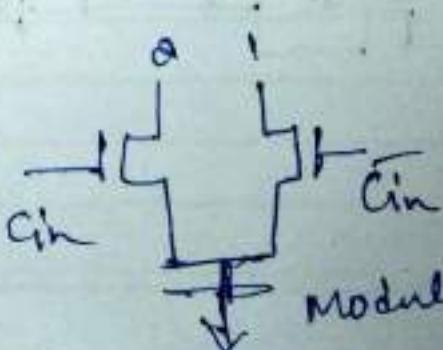
$$+ (ab + \bar{a}\bar{b}) c_{in}.$$

majority voting logic is out.

we triplicate the block

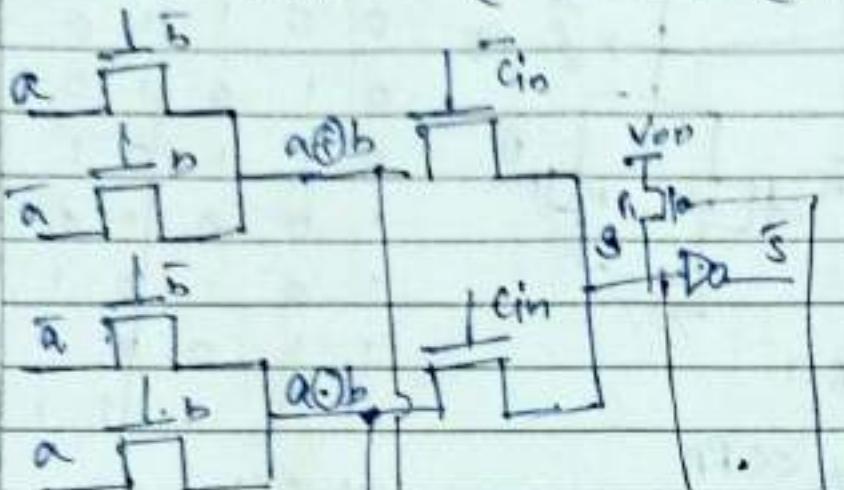


even if error creeps in only
one block will get affected.



modular in nature

$$S = a \oplus b \oplus \bar{c}_{in} = (\bar{a} \oplus b) \bar{c}_{in} + (\bar{a} \oplus b) c_{in}$$



$$\bar{S} = (\bar{a} \oplus b) c_{in} + (a \oplus b) \bar{c}_{in}$$

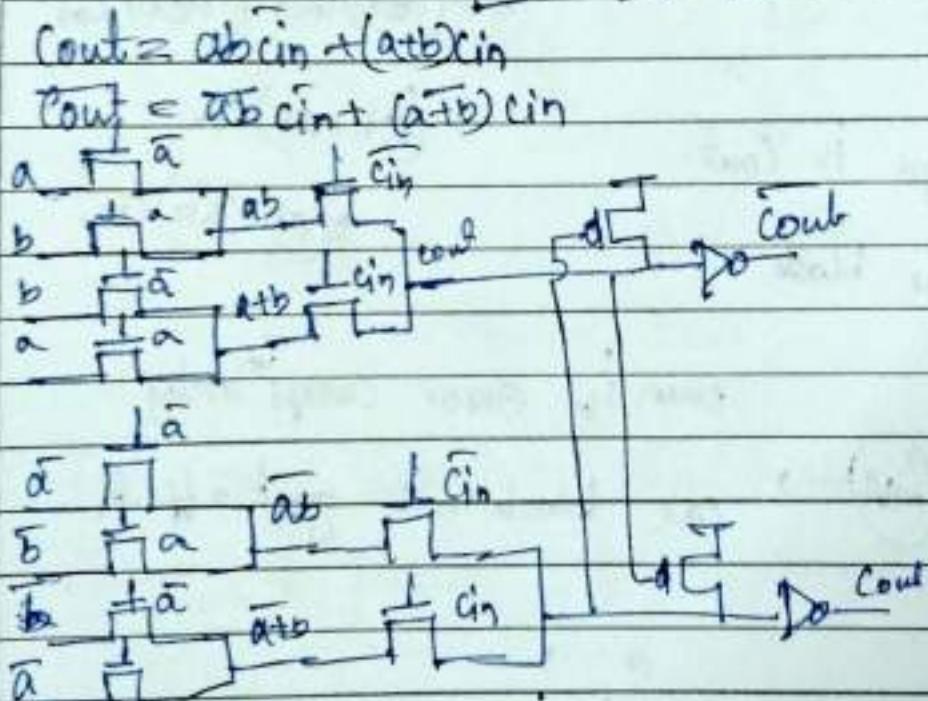
PIP, used for
a little pull up
logic out, has
to be weak.

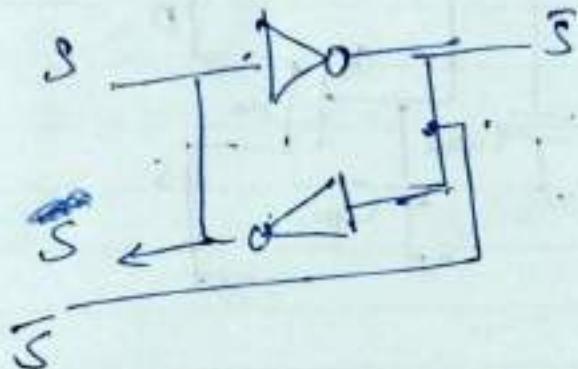
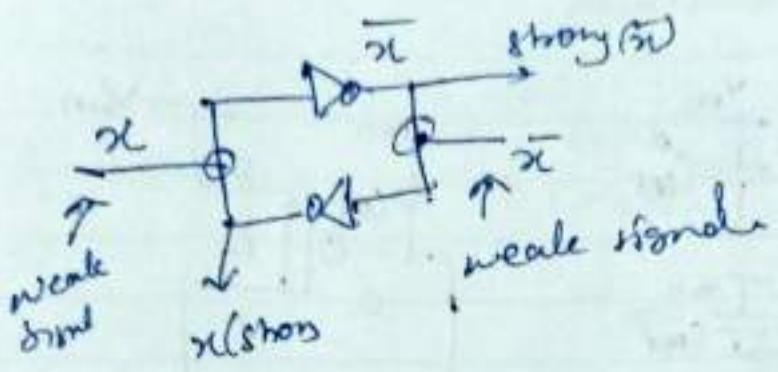
$$\begin{aligned} ab &= \bar{a}(a) + a(\bar{b}) \\ &= \bar{a}(0) + a(1) \end{aligned}$$

$$\begin{aligned} a+b &= a + \bar{a}b \\ &= a(1) + \bar{a}(b) \\ &= a(1) + \bar{a}(0) \end{aligned}$$

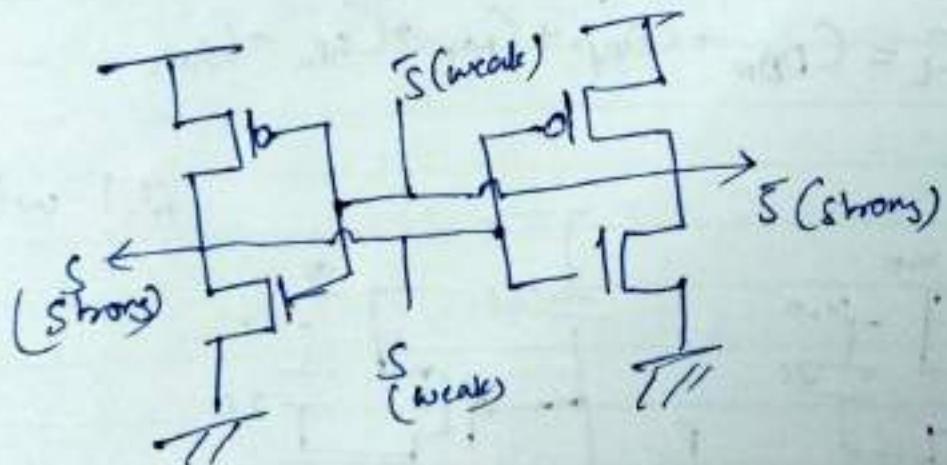
$$\begin{aligned} \bar{ab} &= \bar{a} + \bar{b} = \bar{a} \bar{a} \bar{b} \\ &= \bar{a}(a) + a(\bar{b}) \\ &= \bar{a}(1) + a(0) \end{aligned}$$

$$\begin{aligned} (\bar{a}+b) &= \bar{a}(b) + a(\bar{a}) \\ &= \bar{a}b \end{aligned}$$



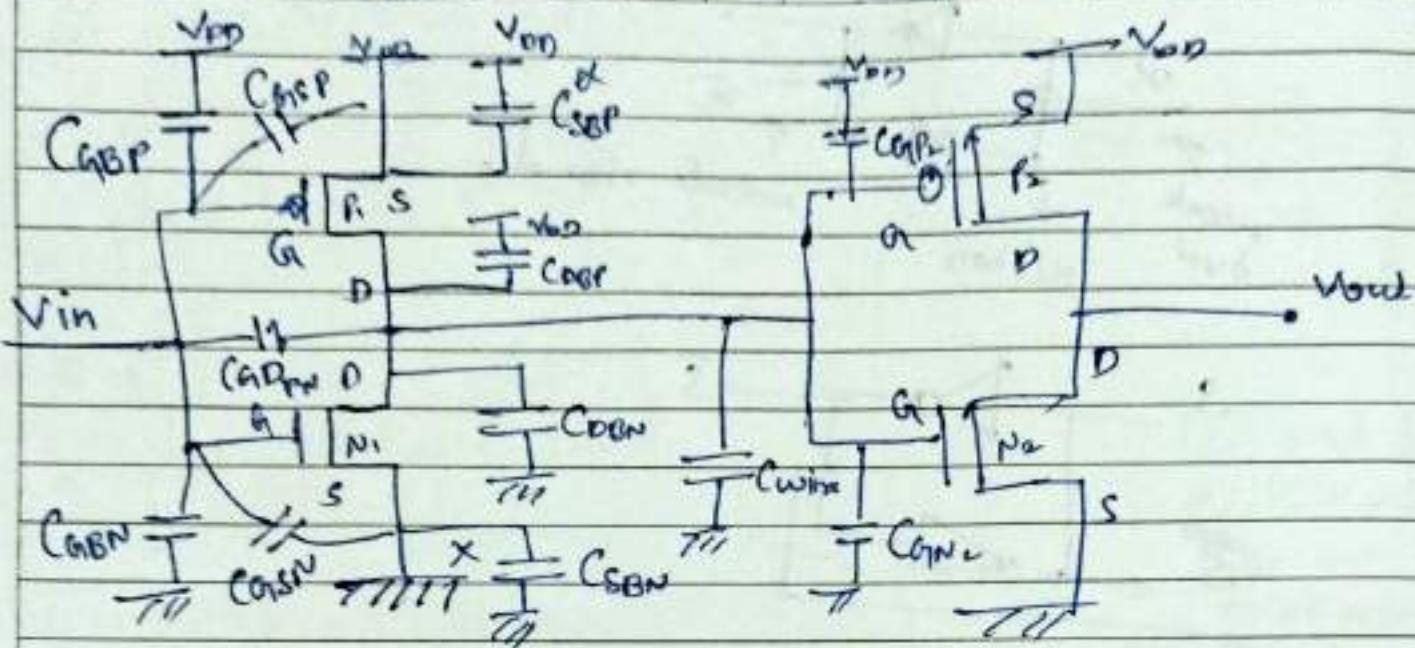


SRPL (Swingswing Resistor Pass Transistor Logic)

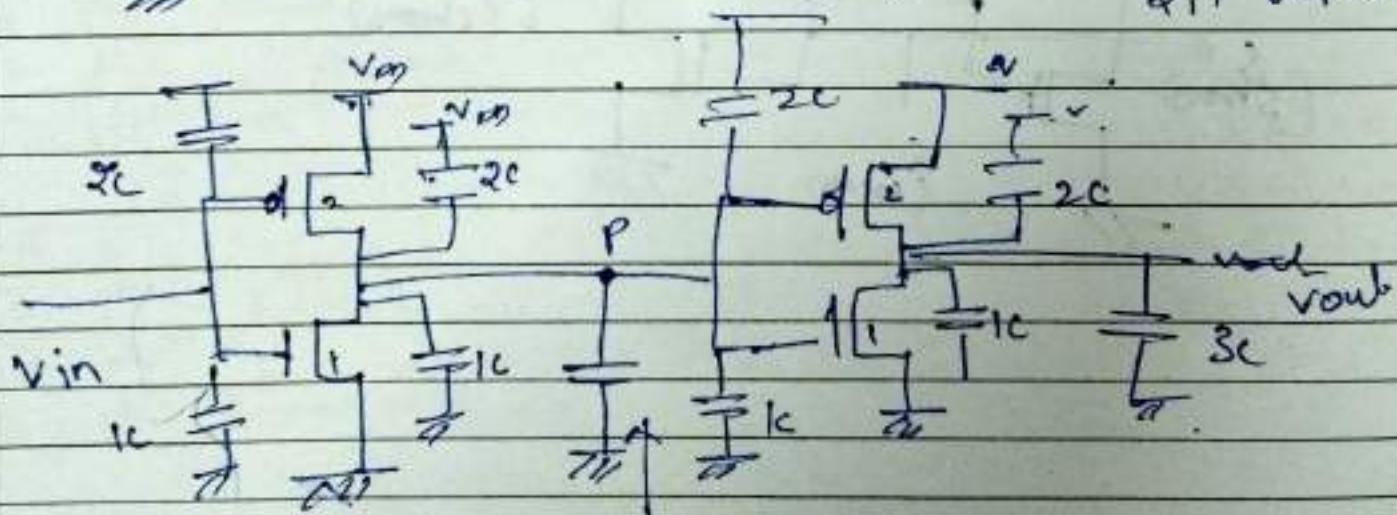
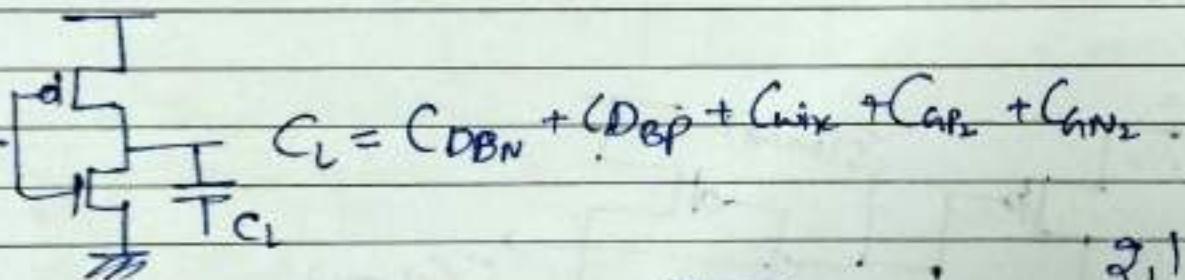


X → now switching

Teacher's Signature

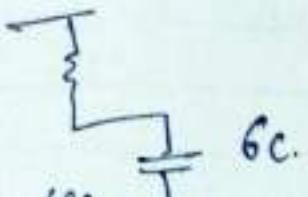


in AC analysis all vdd is made zero so, 11d.

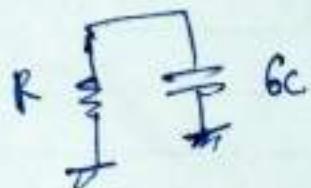


qL + qC + lette

= 6CC



$$\begin{cases} \text{TPDR}_{\text{ise}} = 6RC \\ (\text{V}_{\text{in}} \rightarrow \text{P}) \end{cases}$$



$$\begin{cases} \text{TPDR}_{\text{full}} = 6RL \\ (\text{V}_{\text{in}} \rightarrow \text{P}) \end{cases}$$

$$\begin{cases} \text{TPDR}_{\text{P} \rightarrow \text{Vout}} = 3RC \end{cases}$$

$$\begin{cases} \text{TPDF} = 3RL \\ (\text{P} \rightarrow \text{Vout}) \end{cases}$$

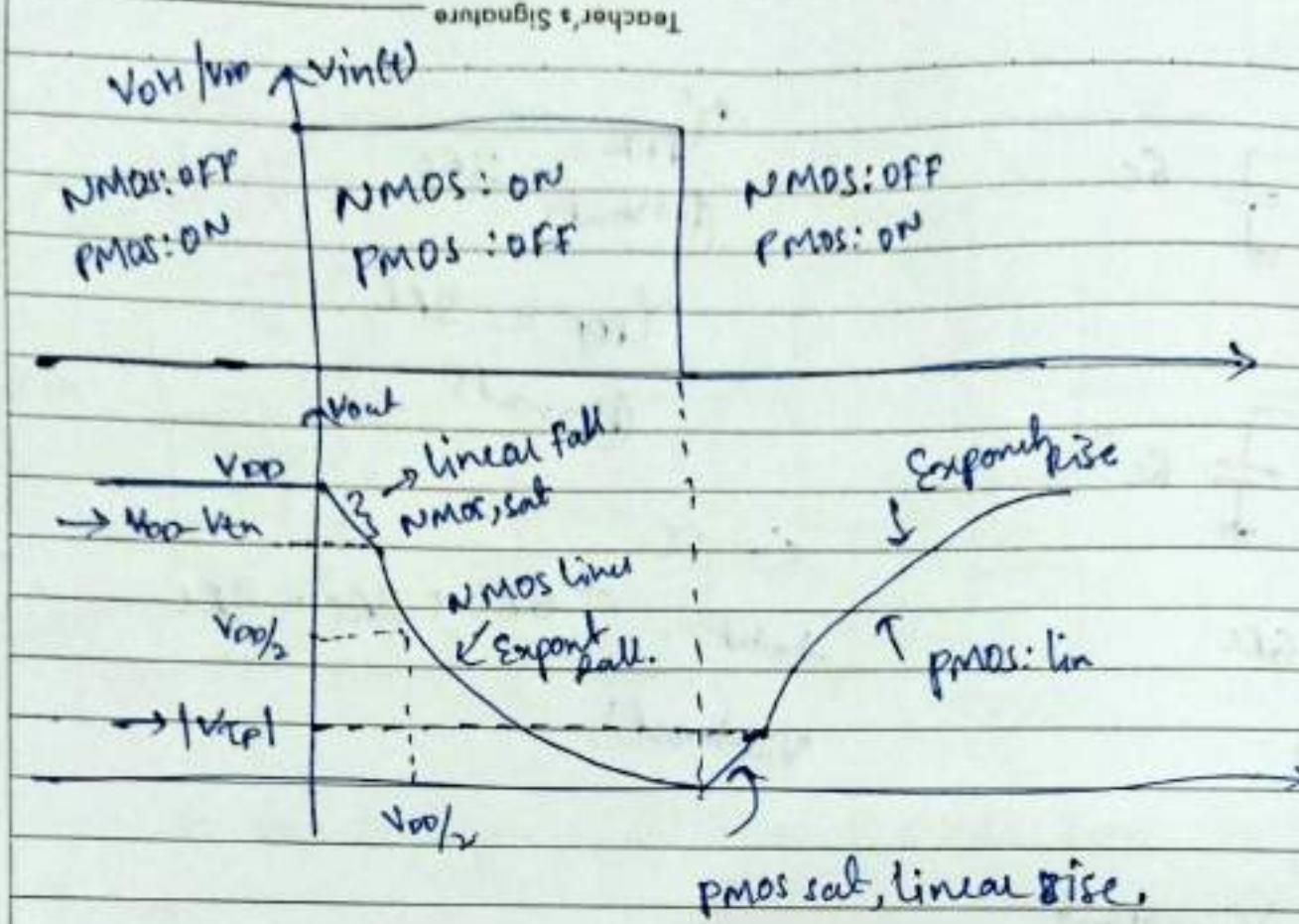
$$\therefore \text{Z}_{\text{dot.bal}} = 6RL + 3RC = 9RL$$

$\text{V}_{\text{in}} \rightarrow \text{Vout}$

$\left\{ \begin{array}{l} \text{V}_{\text{in}} \rightarrow \text{Vout} \\ \text{V}_{\text{in}} \rightarrow \text{P} \end{array} \right.$

$$= \begin{cases} \text{TPDR} \\ \text{V}_{\text{in}} \rightarrow \text{P} \end{cases} + \begin{cases} \text{TPDF} \\ \text{P} \rightarrow \text{Vout} \end{cases}$$

$$= \begin{cases} \text{TPDF} \\ \text{V}_{\text{in}} \rightarrow \text{P} \end{cases} + \begin{cases} \text{TPDR} \\ \text{P} \rightarrow \text{Vout} \end{cases}$$

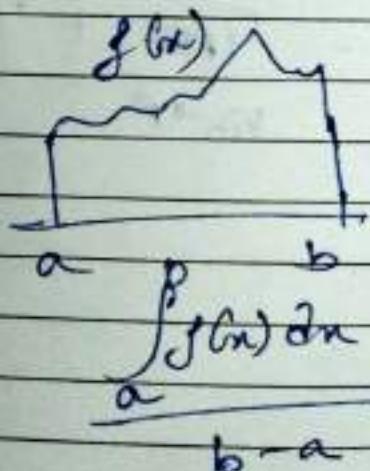


Switching resistance

presented in class, written

* Ratio of V_{DS}/I_{DS} averaged across the switching voltage of interest

* $\frac{V_{DS}}{I_{DS}}$ = DC resistance



$$R_{\text{switch}} = \frac{1}{V_{DD}} \int_0^{V_{DD}} \frac{V_{DS}}{I_{DS}} dV_{DS}$$

Switching = average of voltage weighted DC resistance

$t_{PDf} \rightarrow V_{out}$ from 1 to 0
i.e. : V_{DD} to $\frac{V_{DD}}{2}$

$$R_{switch} = \frac{1}{V_{final} - V_{init}} \int_{V_{init}}^{V_{final}} \left(\frac{V_{DS}}{I_D} \right) dV_{DS}$$

$$= \frac{1}{\frac{V_{DD}}{2} - V_{DD}} \int_{\frac{V_{DD}}{2}}^{V_{DD}} \left(\frac{V_{DS}}{I_{DS}} \right) dV_{DS}$$

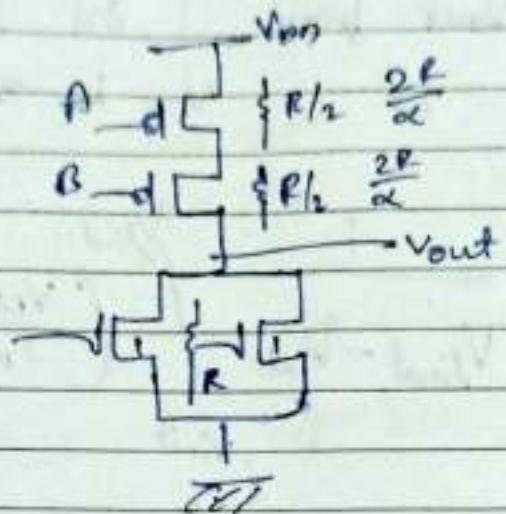
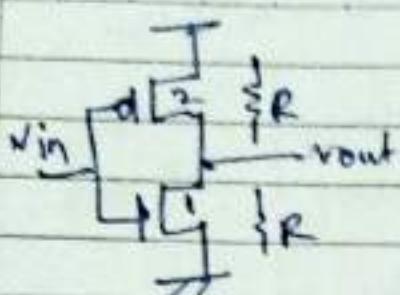
$$\Rightarrow -\frac{2}{V_{DD}} \left[\int_{V_{DD}}^{V_{DD}-V_T} \frac{V_{DS}}{I_{DS, sat}} dV_{DS} + \int_{V_{DD}-V_T}^{\frac{V_{DD}}{2}} \frac{V_{DS}}{I_{DS, line}} dV_{DS} \right]$$

$$\Rightarrow -\frac{2}{V_{DD}} \left[\int_{V_{DD}}^{\frac{V_{DD}-V_T}{2}} \frac{V_{DS}}{\beta/(V_{DD}-V_T)} dV_{DS} + \int_{V_{DD}-V_T}^{\frac{V_{DD}}{2}} \frac{V_{DS}}{\beta(V_{DD}-V_T - \frac{V_{DS}}{2})} dV_{DS} \right]$$

After rearranging

$$\Rightarrow -\frac{2}{V_{DD}} \left[\frac{2}{\beta(V_{DD}-V_T)^2} \frac{V_{DD}^2}{2} \right]_{V_{DD}}^{V_{DD}-V_T} + \frac{-2}{\beta} \ln \left(\frac{\frac{2}{\beta} V_{DD} - V_T}{V_{DD} - V_T} \right)$$

$$\text{Final} \Rightarrow \frac{2}{V_{DD}} \left[\frac{V_{DD}^2 - (V_{DD}-V_T)^2}{\beta(V_{DD}-V_T)^2} + \frac{2}{\beta} \ln \left(\frac{\frac{2}{\beta} V_{DD} - V_T}{V_{DD} - V_T} \right) \right]$$



$$\frac{2F}{\alpha} + \frac{2L}{\alpha} = R$$

$$\frac{4F}{\alpha} = R \Rightarrow \alpha = 4$$

$$I = R$$

$$\alpha = R/\lambda$$

$$\begin{array}{c} \rightarrow | \\ - | \end{array} \quad \alpha = 2F$$

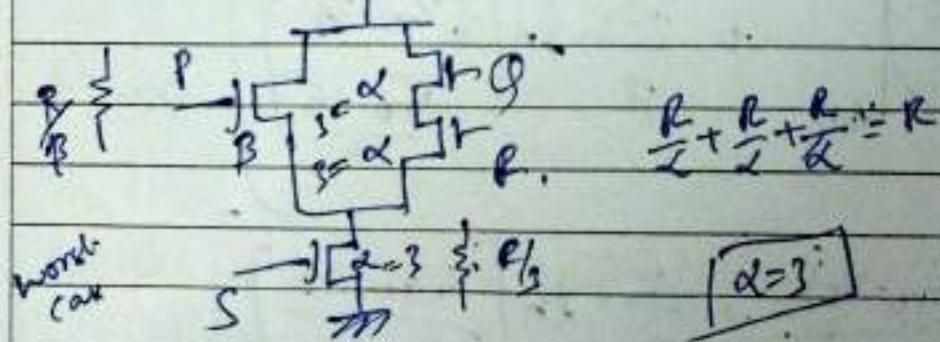
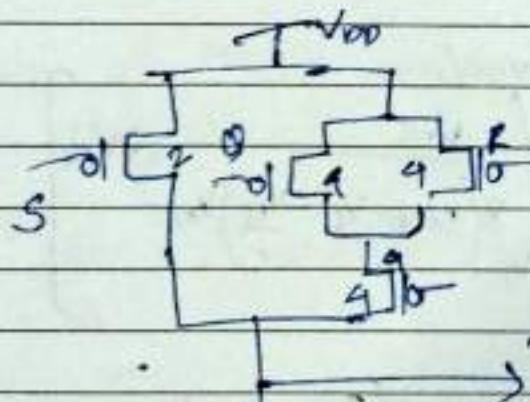
$$\begin{array}{c} - | \\ \rightarrow | \end{array} \quad \alpha = R$$

$$\begin{array}{c} \rightarrow | \\ - | \end{array} \quad \alpha = R$$

$$\alpha = \frac{2R}{\alpha}$$

$$Y = (\overline{P+Q})RS$$

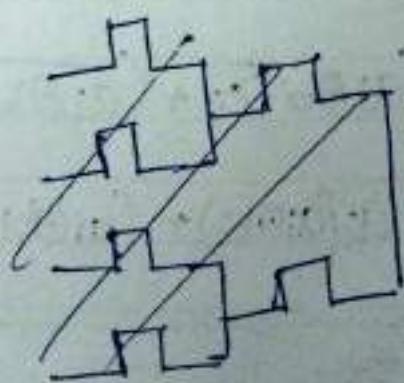
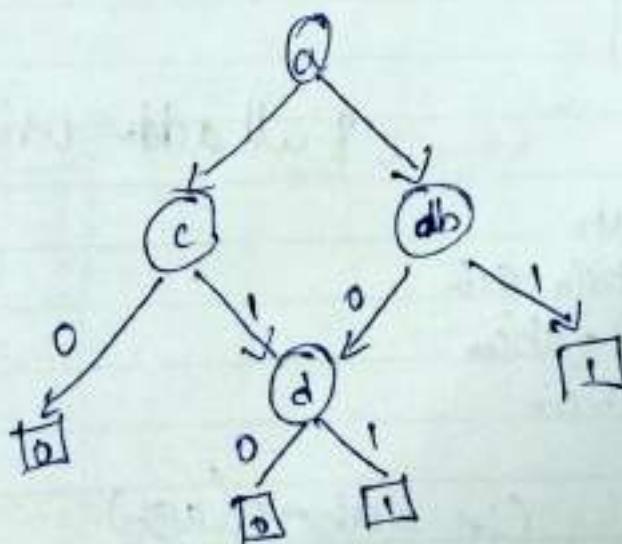
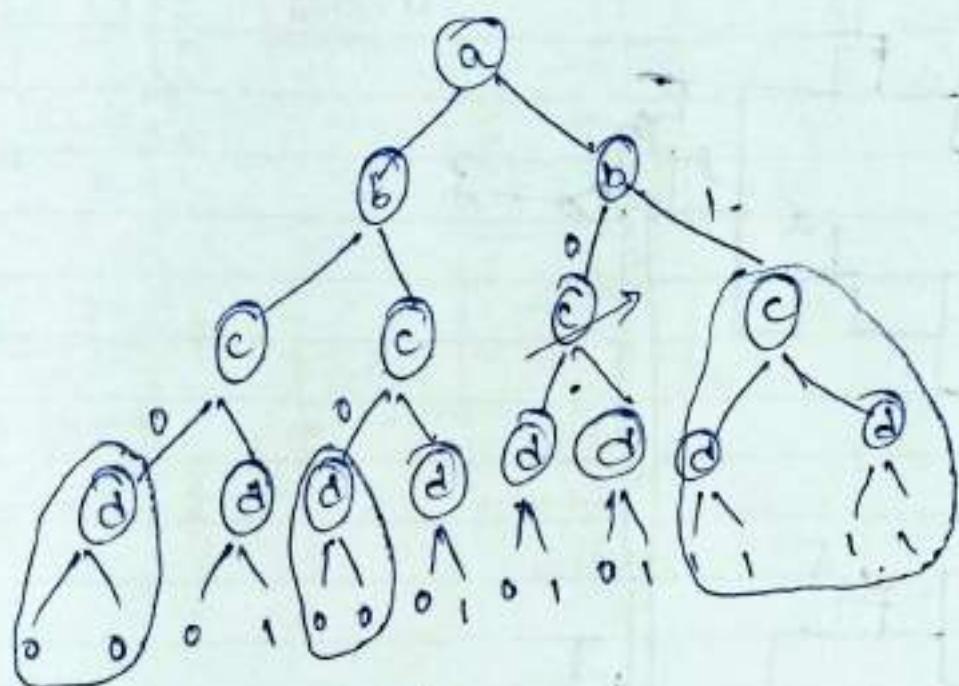
inversely
proper
unitary mat.



$$\frac{R}{2} + \frac{R}{2} = R$$

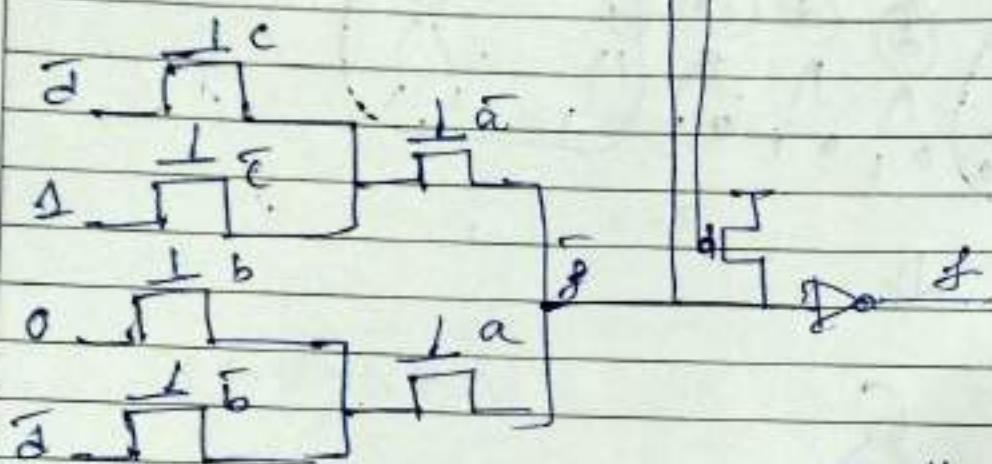
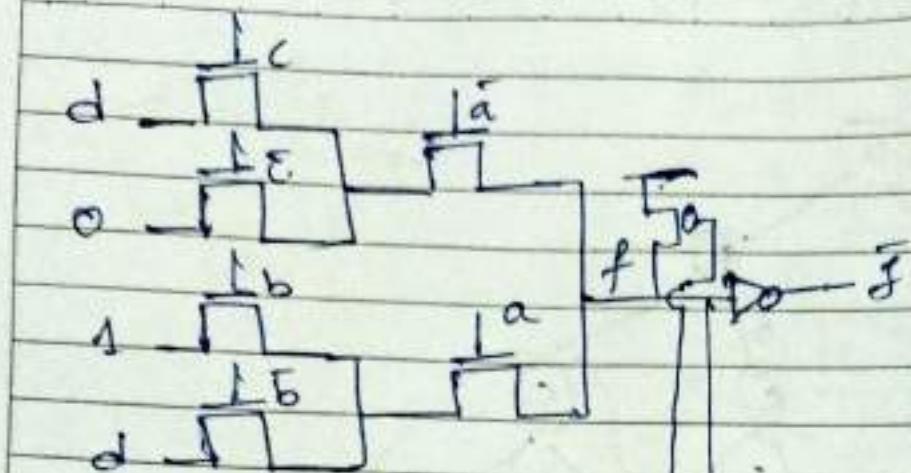
$$\frac{1}{\beta} = \frac{2}{3} \quad R = \frac{9}{2}$$

$f(a, b, c, d) = \sum(3, 4, 9, 11, 12, 13, 14, 15)$ Reduced ordered BDD for



$$f = a\bar{s} + bs$$

$$\bar{f} = \bar{a}\bar{s} + \bar{b}s$$



Full adder using Txgates

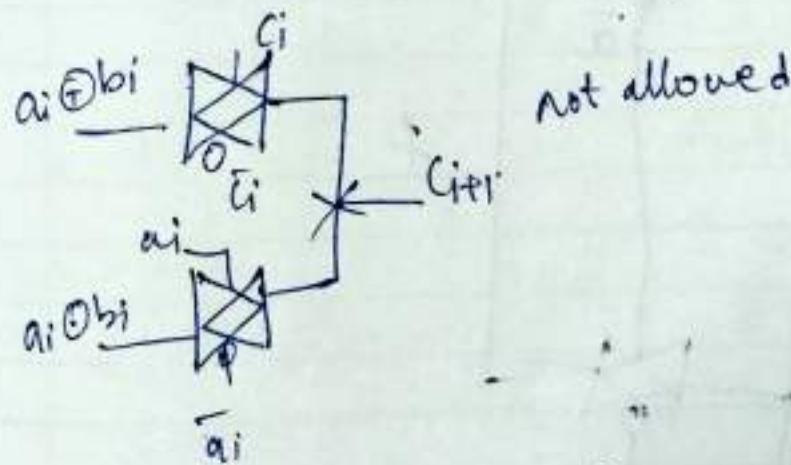
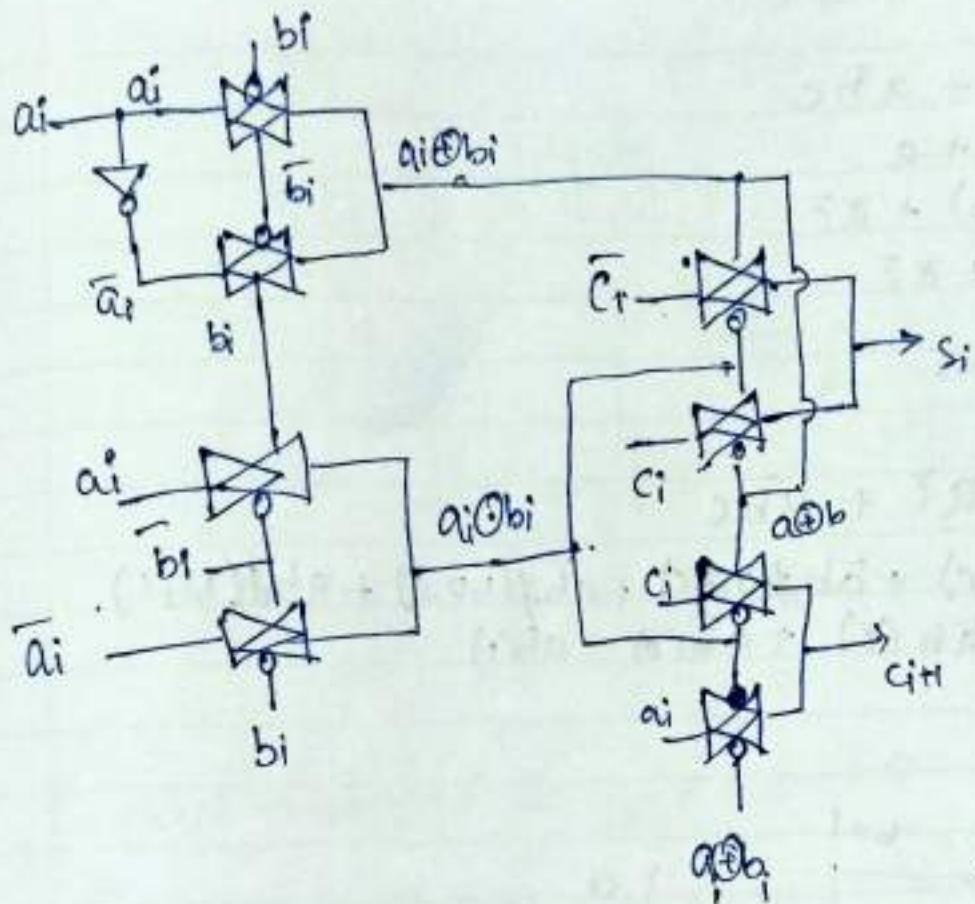
$$\begin{aligned}
 C_{out} &= ab + b\bar{c}_{in} + a\bar{c}_{in} \\
 &= ab(c_{in} + \bar{c}_{in}) + b\bar{c}_{in} + a\bar{c}_{in} \\
 &= c_{in}(ab + a + b) + ab\bar{c}_{in} \\
 &= c_{in}(a+b) + ab\bar{c}_{in}
 \end{aligned}$$

$$S_i = (a_i \oplus b_i) \oplus c_i, \quad C_{i+1} = ab + c_i(a \oplus b)$$

$$S_i = (a_i \oplus b_i)\bar{c}_i + (\bar{a}_i \oplus \bar{b}_i)c_i$$

$$C_{i+1} = a_i(\bar{a}_i \oplus b_i) + (a_i \oplus b_i)c_i$$

$$(a_i+b_i)(\bar{a}_i+\bar{b}_i)(a_i\bar{b}_i+a_i\bar{b}_i)$$



$$f = ab + a\bar{c} + \bar{a}bc$$

$$\Rightarrow abc + ab\bar{c} + a$$

$$\Rightarrow a(\bar{b}c + b) + \bar{a}\bar{c}$$

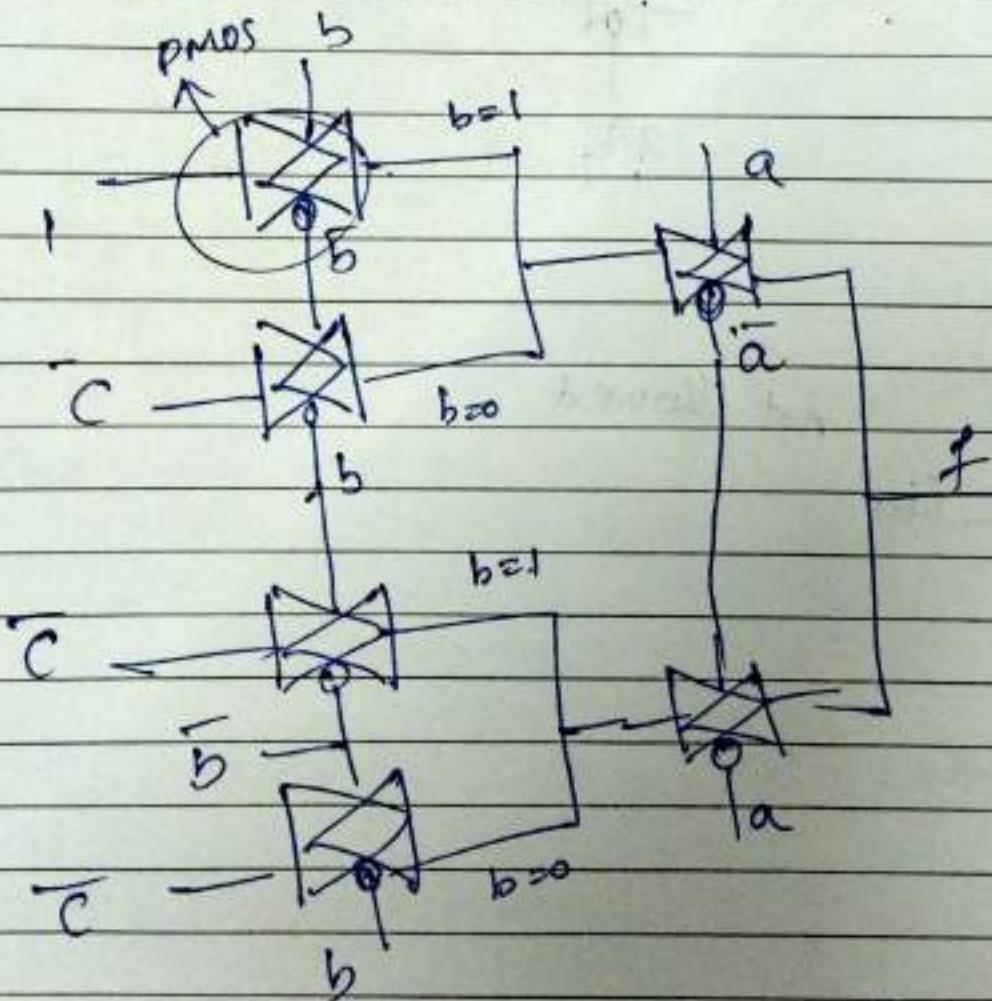
$$\Rightarrow a(b+c) + \bar{a}\bar{c}$$

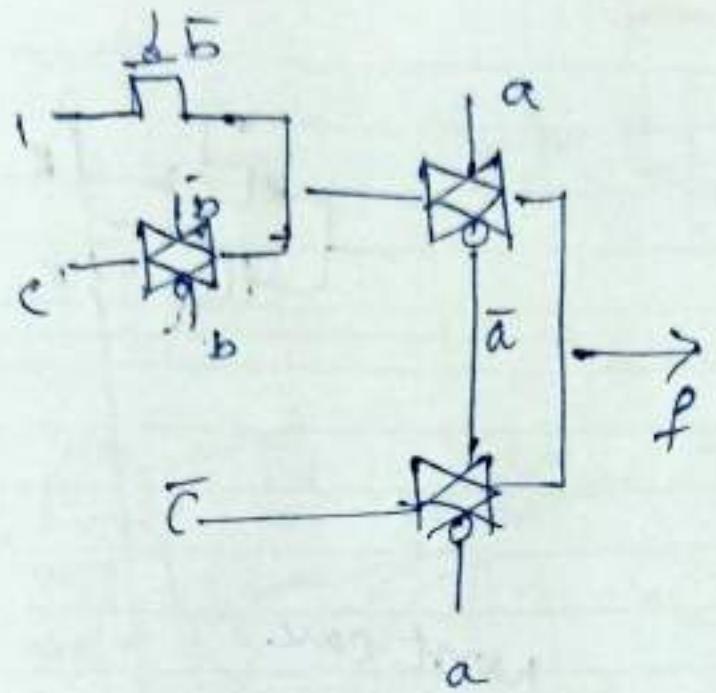
side shanon wins

$$f(a,b,c) = ab + a\bar{c} + \bar{a}bc$$

$$\Rightarrow \bar{a}\bar{b}f(0,0,c) + \bar{a}bf(0,1,c) + a\bar{b}f(1,0,c) + abf(1,1,c).$$

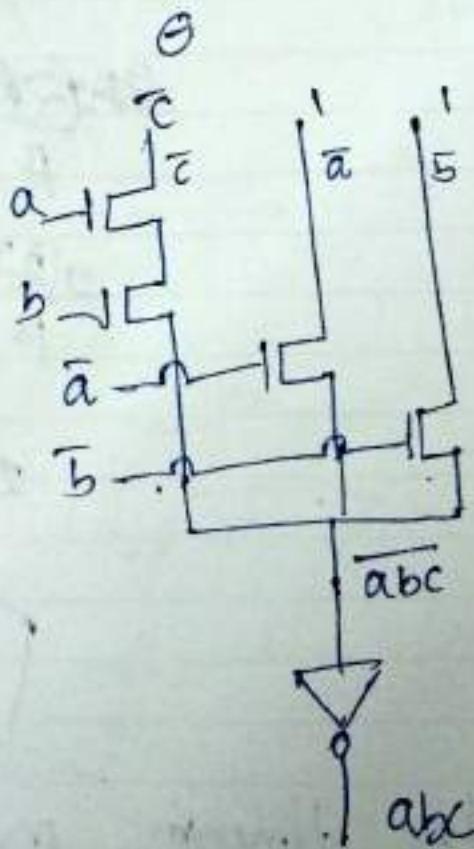
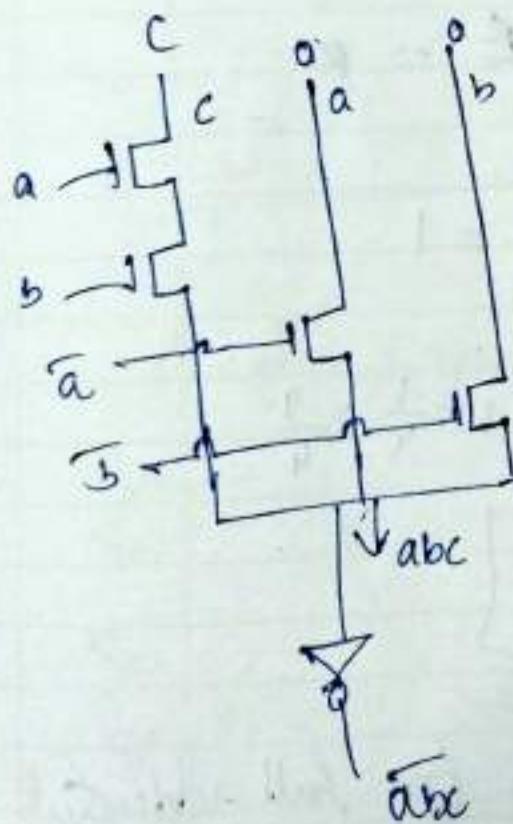
$$\Rightarrow \bar{a}\bar{b}(\bar{c}) + \bar{a}b(\bar{c}) + a\bar{b}(c) + ab(1)$$



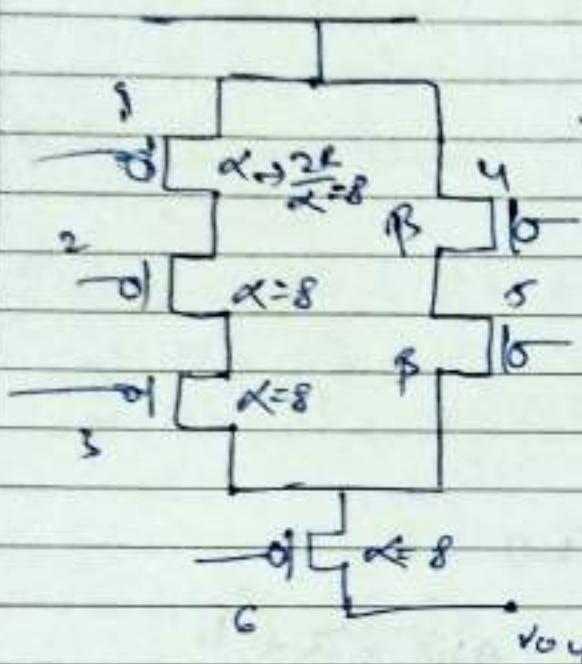


$$f = abc + \bar{a} + \bar{b} + \bar{c} \Rightarrow abc + \bar{a} \cdot 0 + \bar{b} \cdot 0$$

$$\Rightarrow abc \oplus \bar{f} = \bar{abc} = \bar{a} + \bar{b} + \bar{c} \quad abc + \bar{a} + \bar{b}$$



Sizing problem



worst case

$$\frac{2R}{\alpha} \cdot n = R$$

$$\boxed{\alpha = 8}$$

~~$$\frac{2\beta(2R)}{\beta} + \frac{2R}{\alpha} = R$$~~

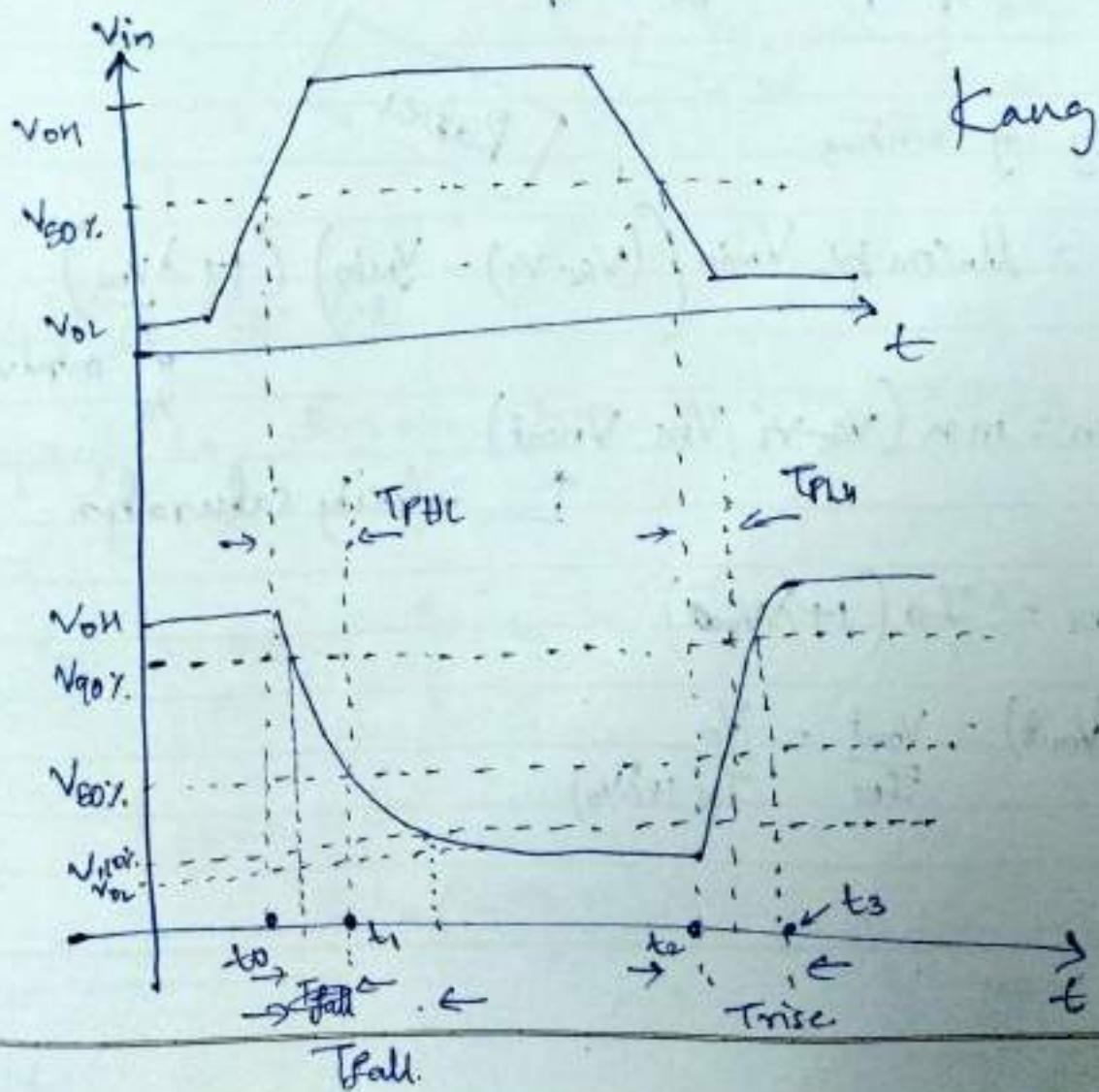
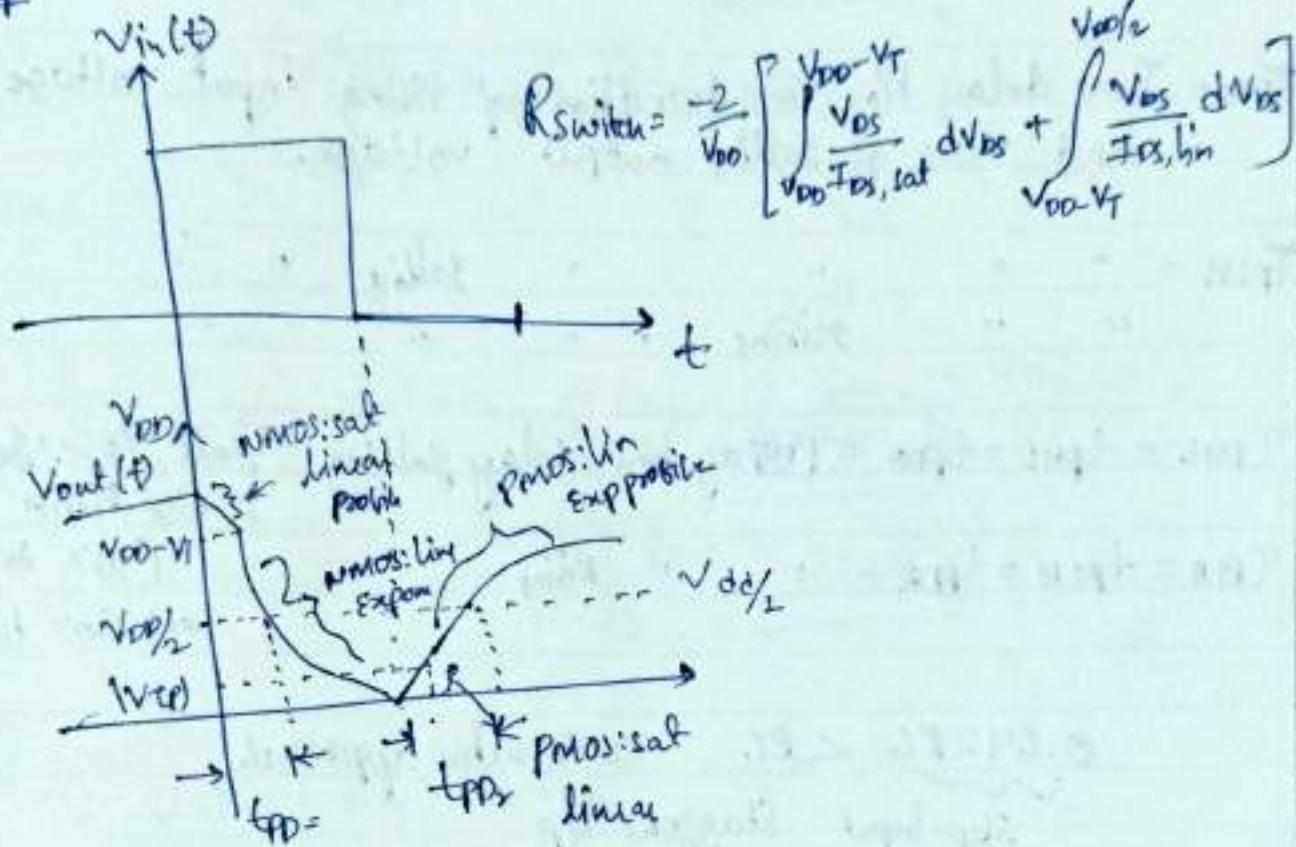
$$\frac{2(2)}{\beta} + \frac{R}{8} = 1$$

$$\frac{2(2)}{\beta} = 1 - \frac{1}{8} = \frac{3}{4}$$

$$\boxed{\beta = \frac{8}{3}}$$

practice dimension matching for full adder/sub

Recap



T_{PHL} = Time delay b/w V_{SOI} transition of rising input voltage and V_{SOI} of falling output voltage.

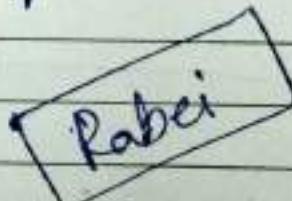
$T_{PLH} = " " " " " \text{ falling} " ..$
 $\text{or } " " \text{ gliding } ? .. "$

$T_{PLH} = t_{PLH} = t_{PDR} = \text{propagation delay falling } T_{fall}, \text{ rise : fall time}$
 $\in \text{rise time}$

$T_{PLH} = t_{PLH} = t_{PDR} = " " \text{ Rising} \quad (10\% \text{ to } 90\%)$
 $\text{or } (20\% \text{ to } 80\%)$

$\underbrace{0.693RC < R_L}_{\text{step input}} \text{ : conservative approach}$
 Staggered Ifp.

One way of writing.



$$I_{ds} = M_n C_{ox} \frac{W}{L} V_{min} \left((V_{ds} - V_T) - \frac{V_{min}}{2} \right) \left(1 + \lambda \frac{V_{ds}}{V_0} \right)$$

✓ \downarrow output vout
v₀

$$V_{min} = \min(V_{ds} - V_T, V_{ds}, V_{dsat})$$

\uparrow velocity saturation

$$I_{ds} = I_0 \left(1 + \lambda \frac{V_{ds}}{V_0} \right)$$

$$f(V_{out}) = \frac{V_{out}}{I_{ds}} = \frac{V_0}{I_0 (1 + \lambda \frac{V_{ds}}{V_0})}$$

$$R_{eq} = \frac{1}{V_f - V_i} \int_{V_i}^{V_f} R(V_o) dV_o \Rightarrow R_{eq} = \frac{-2}{V_{DD}} \int_{V_{DD}/2}^{V_{DD}} \frac{V_o}{I_0(1+\lambda V_o)} dV_o$$

$V_f = V_{DD}/2$
 $V_i = V_{DD}$

$$\Rightarrow \frac{2}{I_0 V_{DD}} \int_{V_{DD}/2}^{V_{DD}} V_o(1-\lambda V_o) dV_o \Rightarrow R_{eq} = \frac{3}{4} \frac{V_{DD}}{I_0} - \frac{1}{12} \frac{\lambda V_{DD}^2}{I_0}$$

$R_{eq} \approx \frac{3}{4} \frac{V_{DD}}{I_0}$

To make $R_{eq} = R_{sat}$ we have to $\int_{V_{DD}/2}^{V_{DD}}$

$$\int_{V_{DD}/2}^{V_{DD}} \frac{V_{DS}}{I_{DS, sat}} dV_{DS}$$

only sat
not linear

Now,
calculating. τ_{PUL}, τ_{PHL}

* capacitor C_L discharges from $V_{DD}/2$ to V_{DD} during

to to I_1

$$\frac{V_{DD}}{2} = V_{DD} - \frac{\beta_N (V_{GS} - V_{TN})^2}{2} \left(\frac{\tau_{PHL}}{C_L} \right) I_1$$

$I_1 = \text{when saturated}$

$$\tau_{PHL} = \frac{C_L}{\beta_N V_{DD} \left(1 - \frac{V_{TN}}{V_{DD}} \right)^2}$$

Capacitor C_L charges from 0 to $V_{DD}/2$ during t_2 to t_3

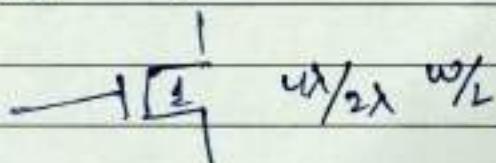
$$\frac{V_{DD}}{2} = 0 + \frac{g_p}{2} (V_{DD} - V_{TP})^2 \left(\frac{\gamma_{PLH}}{C_L} \right)$$

$$\gamma_{PLH} = \frac{C_L}{R_p V_{DD} \left(1 + \frac{V_{TP}}{V_{DD}} \right)^2}$$

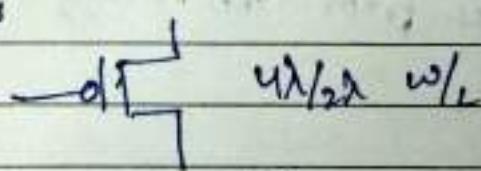
Average propagation delay of an inverter

$$\gamma_p = \frac{T_{PLH} + T_{PHL}}{2} = \frac{C_L}{2V_{DD} \left(1 - \frac{V_T}{V_{DD}} \right)^2} \left[\frac{L_N}{M_N C_{OxN}} + \frac{L_P}{M_P C_{OxP}} \right]$$

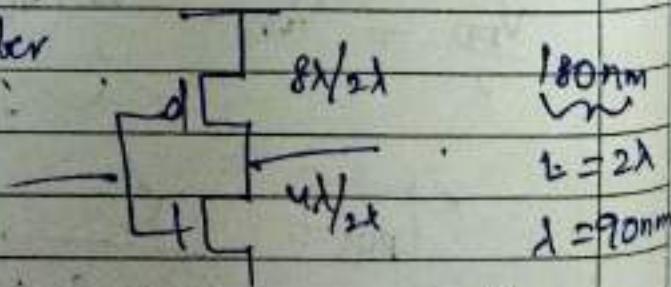
unit NMOS



unit PMOS



But unit inverter



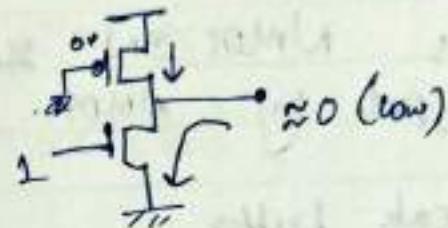
STATIC CMOS POWER DISSIPATION.

DYNAMIC

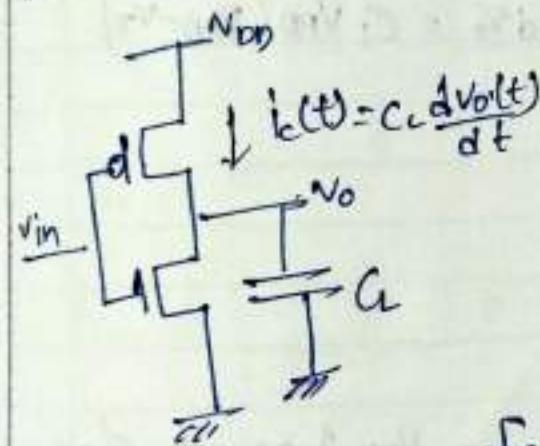
- * Switching power $\propto 1/D$
- * Shortcircuit power
- * Clipping power $\propto T$

STATIC

- * leakage
 - subthreshold
 - diode (reverse bias)
 - gate oxide
- * DC standby (pseudo-NMOS)



Switching power



$E_{0 \rightarrow 1}$ = energy drawn from the power supply during a/p transition from 0 to V_{DD} (PMOS: ON)

$$E_{0 \rightarrow 1} = \int_0^{\infty} P(t) dt = \int_0^{\infty} V_{DD} i_c(t) dt$$

$$\Rightarrow \int_0^{V_{DD}} V_{DD} C_L \frac{d V_o}{dt} dt = V_{DD} C_L \int_0^{V_{DD}} d V_o$$

$$\boxed{E_{0 \rightarrow 1} = C_L V_{DD}^2}$$

$$\text{Energy stored in the capacitor} = \int_0^{\infty} V_o \cdot i_c(t) dt$$

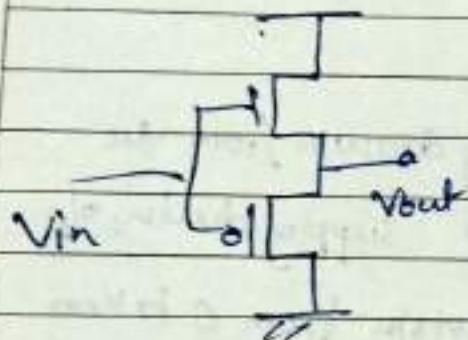
$$= \int_0^{V_{DD}} V_o C_L \frac{dV_o}{dt} dt = C_L \int_0^{V_{DD}} V_o dV_o = \frac{1}{2} C_L V_{DD}^2$$

$$\boxed{E_C = \frac{1}{2} C_L V_{DD}^2}$$

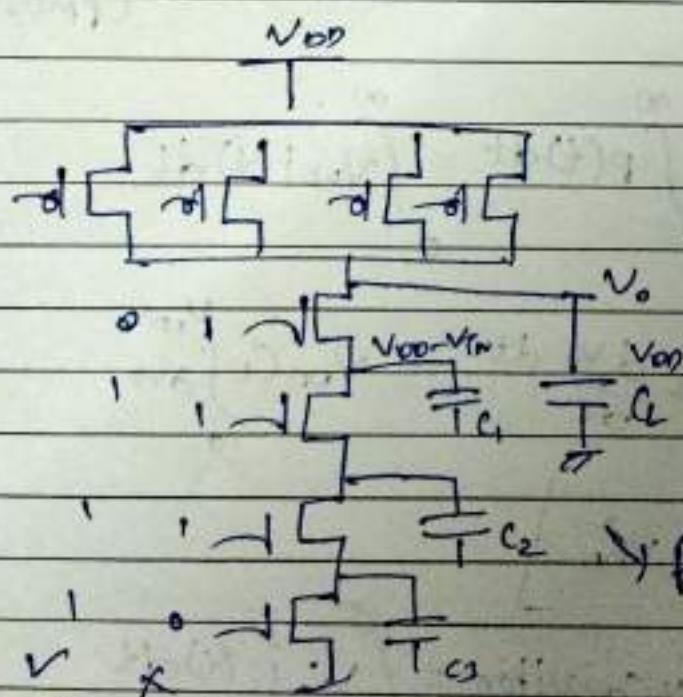
remaining half dissipated
in PMOS Head

During NMOS ON remain half in capacitor will
dissipate by NMOS.

for weak buffer

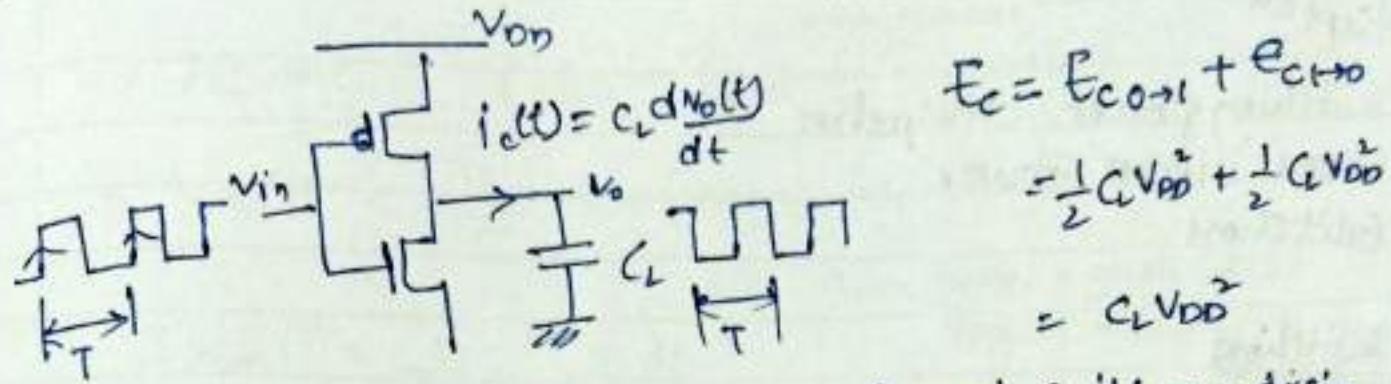


$$E_{ON,1} = \int_0^{V_{DD}-V_T} V_{DD} R_s dV_o = C_L V_{DD} (V_{DD} - V_T)$$



\rightarrow V_{DD} has to change
 $G, C_2, C_1, B_0, \text{much}$
effort

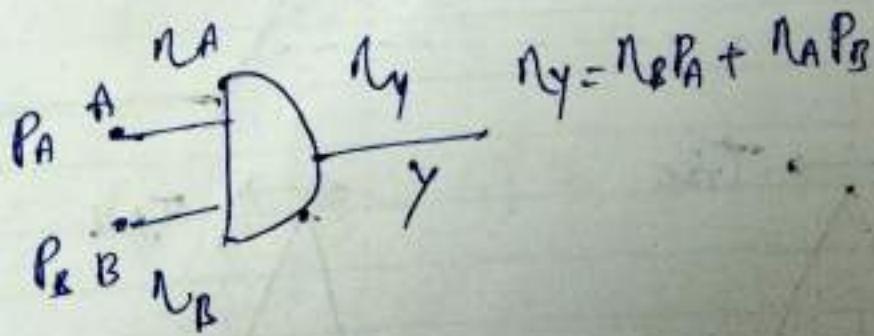
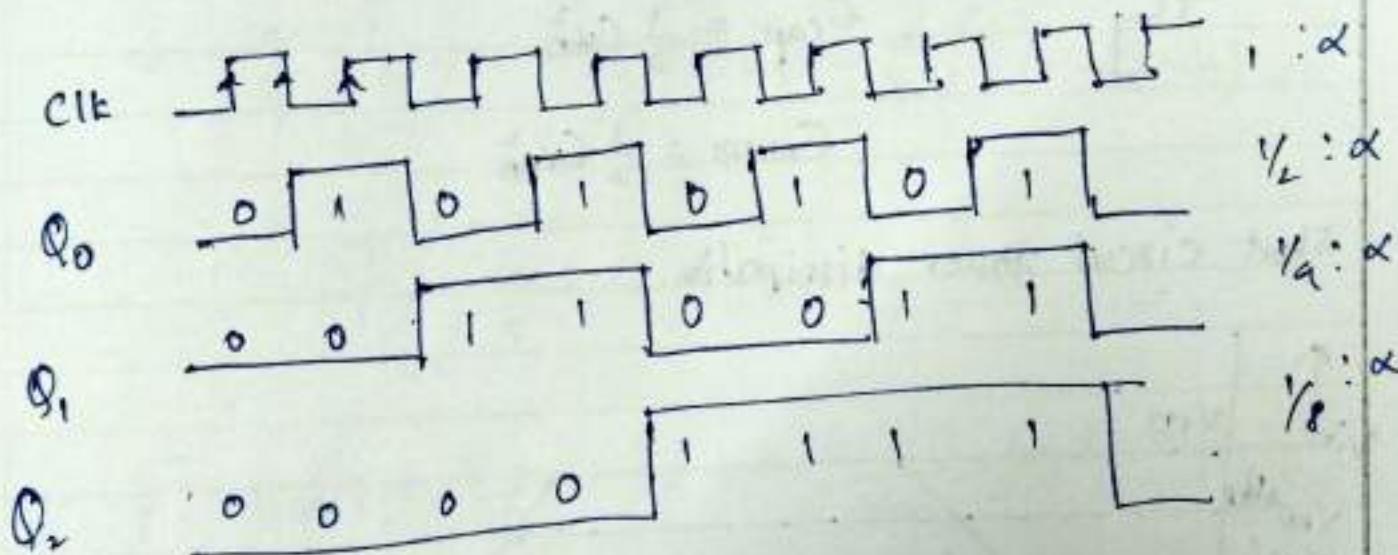
$$P_{SW} = \alpha f_{SW} C_L V_{DD}^2 + \sum_{i=1}^n \alpha_i f_{SW} C_i V_{DD} (V_{DD} - V_T)$$



Dynamic switch power dissipation

$$P = \frac{E}{T_{CLK}} = \frac{C_L V_{DD}^2}{T_{CLK}} = C_L V_{DD}^2 f_{CLK}$$

$$= \alpha f_{CLK} C_L V_{DD}^2 \quad 0 < \alpha \leq 1$$

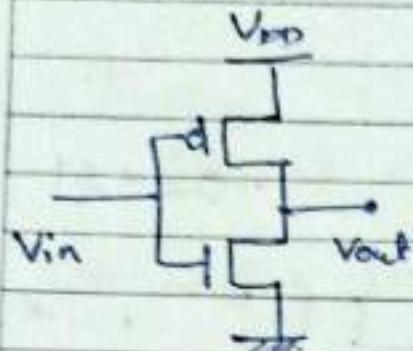


23/Sept/24

Teacher's Signature

- Switching power dissipation
- SHORT CIRCUIT Power
- Glitching

Switching



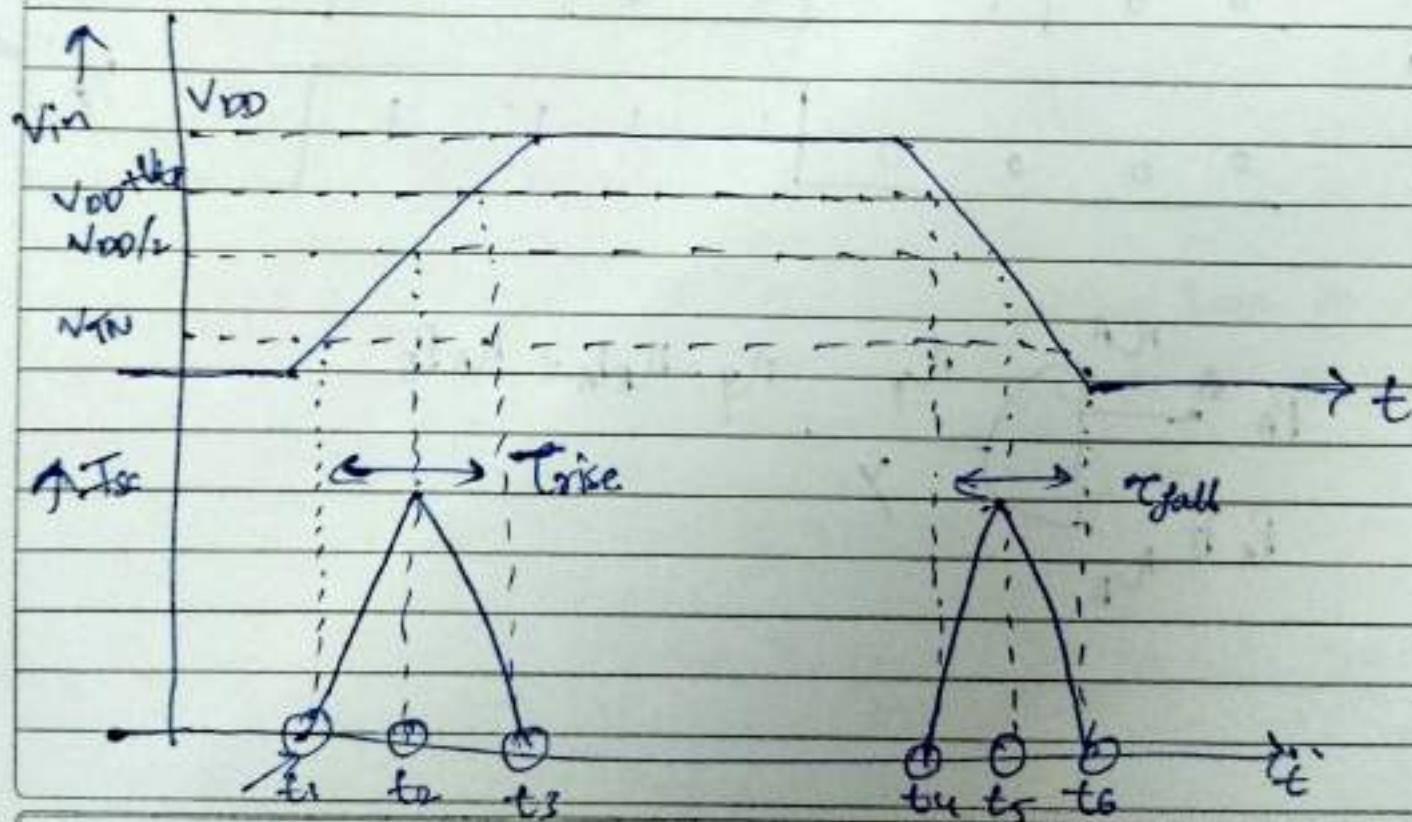
$$\text{Glitchin} = CV_{DD}^2$$

$$E_{PMOS} = \frac{1}{2} CV_{DD}^2$$

$$E_{Cap} = \frac{1}{2} CV_{DD}^2$$

$$E_{NMOS} = \frac{1}{2} CV_{DD}^2$$

Short circuit power dissipation.



→ Assume $T_{rise} = T_{fall} = \tau$ (given)

→ $V_{in}(t) = \frac{V_{DD}}{\tau} t$ (approx) ($y=mx$).

$$I_{mean}(t) = \frac{1}{\tau} \int i(t) dt$$

assume NMOS operates in saturation region during $t_1 - t_2$, time interval.

$$= \left[\frac{1}{\tau} \int_{t_1}^{t_2} i_1(t) dt + \frac{1}{\tau} \int_{t_2}^{t_3} i_2(t) dt \right] \times 2$$

$$\Rightarrow \frac{4}{\tau} \int_{t_1}^{t_2} i_1(t) dt = \frac{4}{\tau} \int_{t_1}^{t_2} i(t) dt = \frac{4}{\tau} \int_{t_1}^{t_2} \frac{P}{2} (V_{in}(t) - V_T)^2 dt$$

$$\Rightarrow \frac{2P}{\tau} \int_{t_1}^{t_2} \left(\frac{V_{DD}}{\tau} t - V_T \right)^2 dt$$

$$\left[V_{in}(t) = \frac{V_{DD}}{\tau} t \Rightarrow t \Rightarrow \frac{V_{in}(t)}{V_{DD}} \text{ @ } t=t_1, t=\frac{V_{in}(t)}{V_{DD}}$$

$$\text{ @ } t=t_2, t=\frac{\tau}{2} \right]$$

$$= \frac{2P}{\tau} \int_{\frac{V_T}{2}}^{\frac{V_T}{2}} \left(\frac{V_{DD}t}{\tau} - V_T \right)^2 dt$$

$\underbrace{V_T}_{V_T = \frac{V_{DD}}{2}}$ $\underbrace{\frac{V_{DD}}{\tau}}$

$$\Rightarrow \frac{V_{DD}t}{\tau} - V_T = P$$

$$\Rightarrow \frac{dP}{dt} = \frac{V_{DD}}{\tau} \Rightarrow dt = \frac{\tau}{V_{DD}} dP$$

when $t = \frac{T}{2} V_T$ $P = 0$

when $t = T/2$ $P = \frac{V_{DD} - V_T}{2}$

$$\Rightarrow \frac{QB}{T} \int_0^{\frac{V_{DD}-V_T}{2}} P^2 \cdot \frac{\pi}{V_{DD}} dP$$

$$\Rightarrow \frac{QB\tau}{2T V_{DD}} \left[P^3 \right]_0^{\frac{V_{DD}-V_T}{2}}$$

$$I_{mean} \Rightarrow \frac{BQ}{T^2 V_{DD}} \left(\frac{(V_{DD} - 2V_T)^3}{T} \right)$$

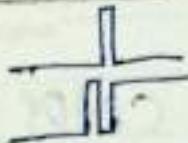
$$P_{sc} = V_{DD} \cdot I_{mean} = \frac{B}{12} (V_{DD} - 2V_T)^3 \tau_f$$

$$P_{sc} \propto (V_{DD} - 2V_T)^3$$

$$P_{sc} \propto \tau \left(\text{rise time / fall time} \right)$$

$$P_{sc} \propto f \left(\text{freq of operation} \right)$$

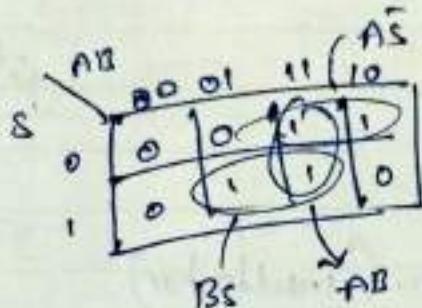
Homework + Static + Dynamic hazard



2x1 mux

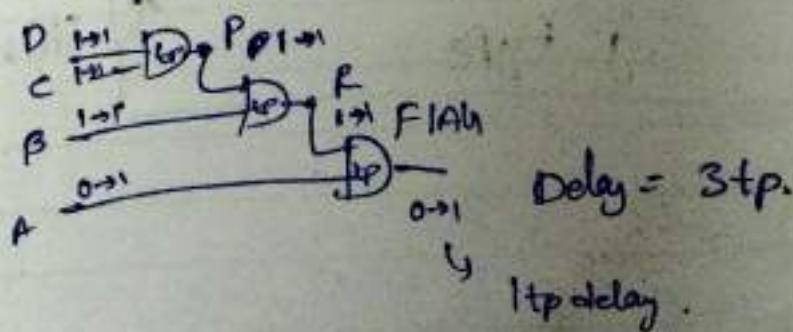
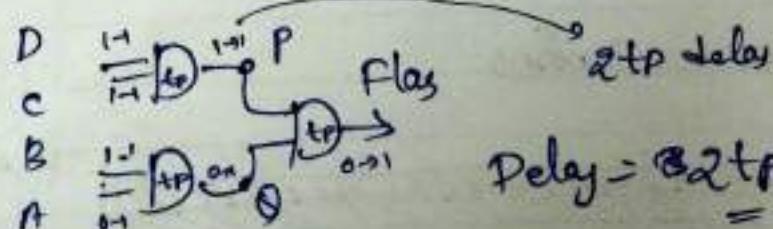
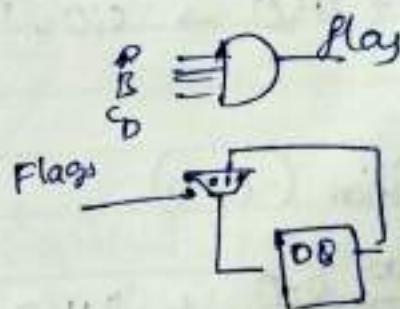
$$Y = A\bar{S} + B\bar{S}$$

S	A	B	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1



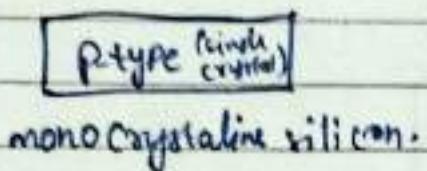
$Y = A\bar{S} + B\bar{S} + (AB)$ → sometimes eliminates
 glitches.
 Redundant.

D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

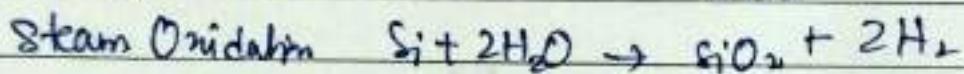
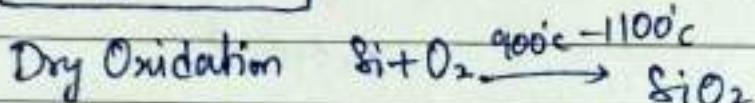
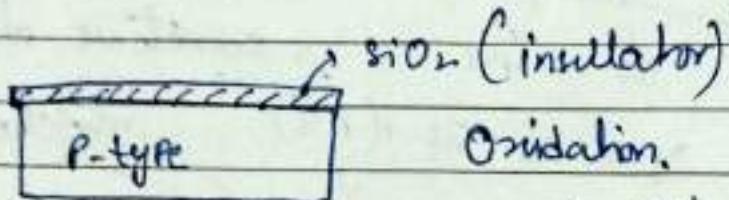


CMOS Fabrication Technology.

i) Bare substrate.

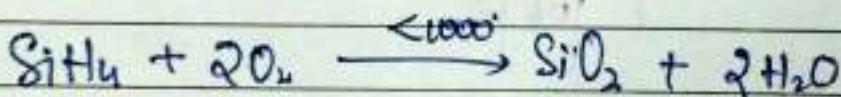


ii)

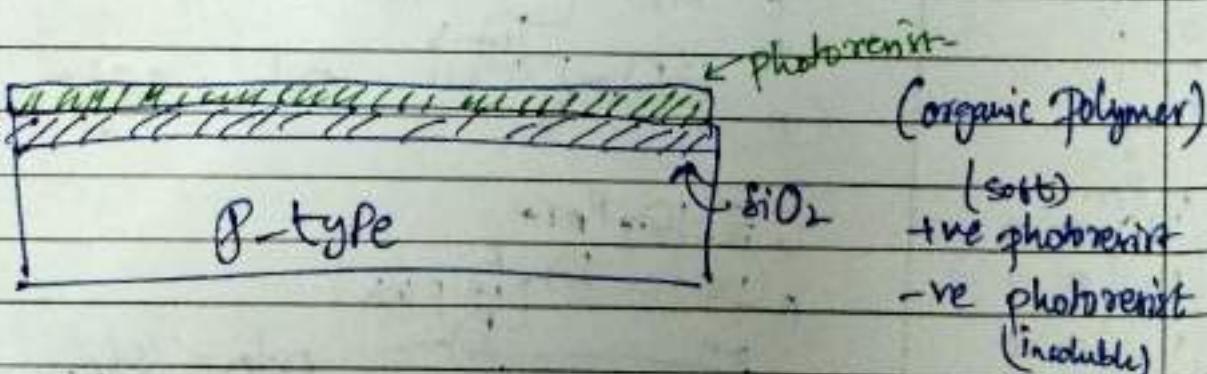


↙ growing SiO_2

iii) Chemical Vapour Deposition (CVD)



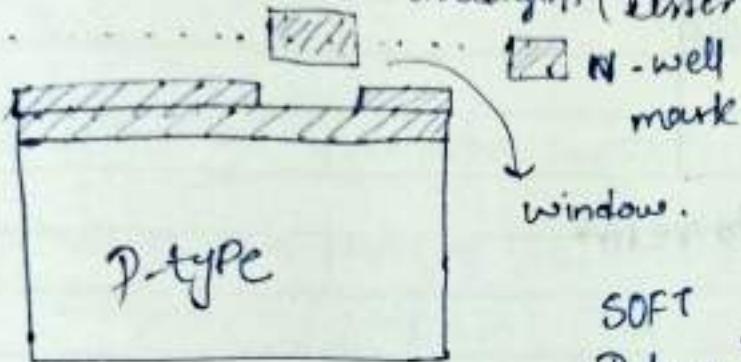
iv) photoresist coating



a) Lithography:

Light \rightarrow photolithography

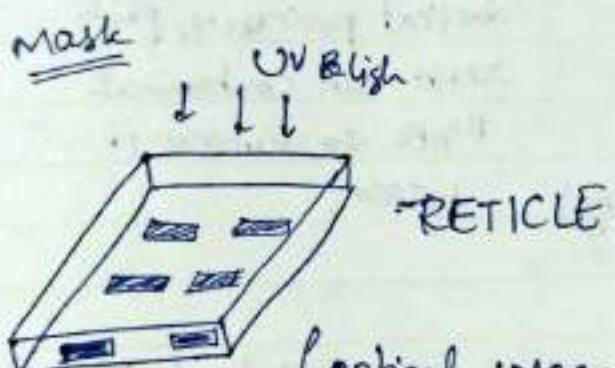
X-rays \rightarrow X-ray lithography (less diffraction) (Smaller sized feature)
Shorter wavelengths (less diffraction)



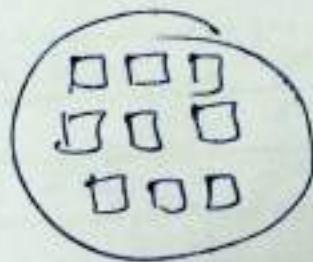
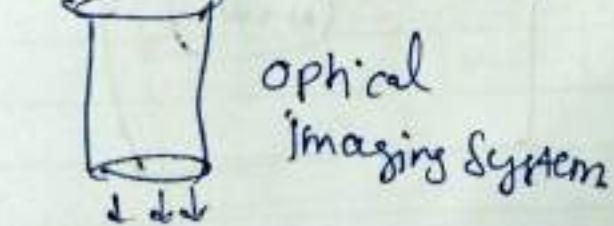
N-well
mark

window.

SOFT
Baking \rightarrow TD Harden remaining
Layer.

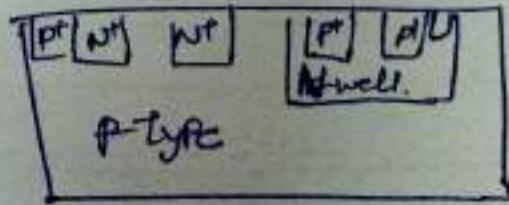


(optical image
of Reticle pattern).



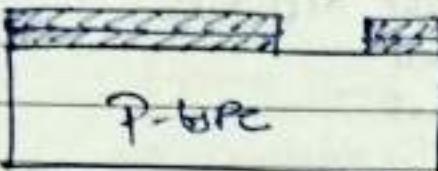
single digit

target



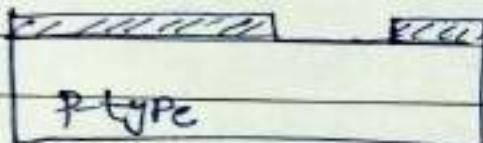
5) Etching

hydrofluoric

Removal of SiO_2 using HF acid

6) Removal of photoresist

- piranha etch.



short time processing, photo
resist can contaminate
P-type so, remove it

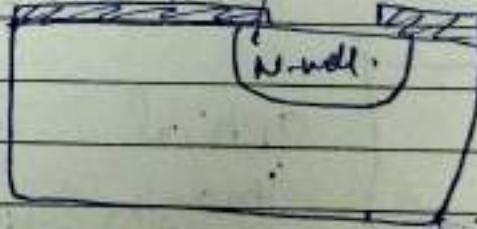
SRD tool (spin, Rinse & Dry)

better.

7) Formation of N-well.

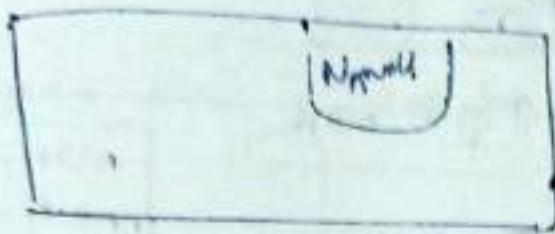
8) Diffusion (2) Ion implantation

lateral diffusion



Nwell diffusion.

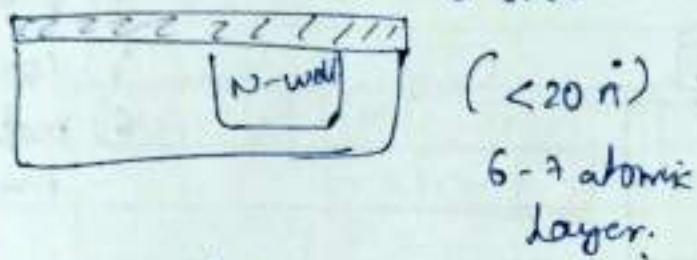
8) Remove the remaining oxide



Patterning of photoresist
with -holes

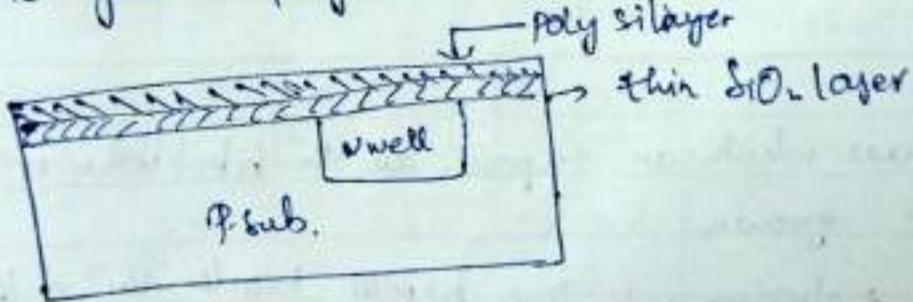
Formation of Transistor Gates

9) Deposit a thin layer of SiO_2



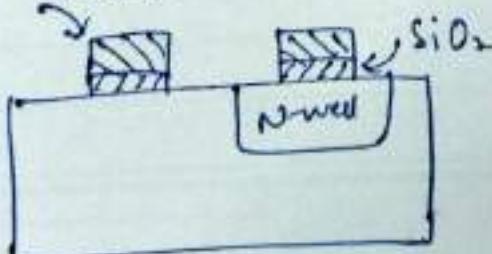
* Thickness determination is important

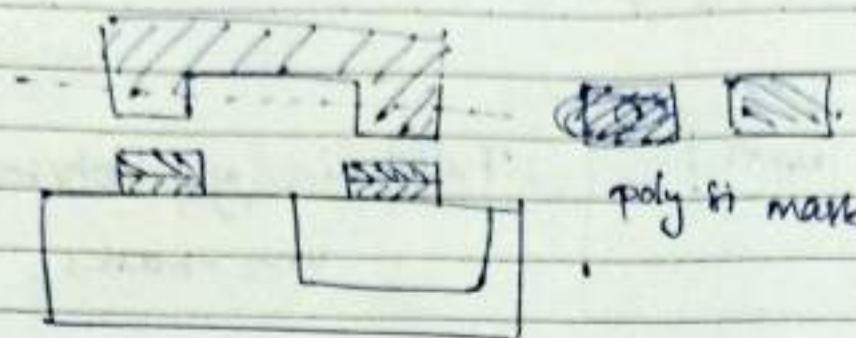
10) wafer is placed in a reactor with silane gas and heated to grow polysilicon layer (using CVD).



11) polysilicon patterning

polysilicon doping poly-Si





poly fit mark

n+ of marks

marks

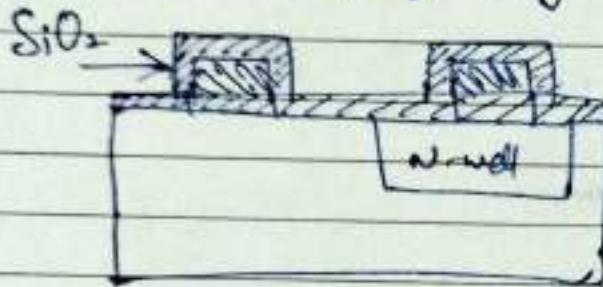
n+ well

→ Poly-n
mark

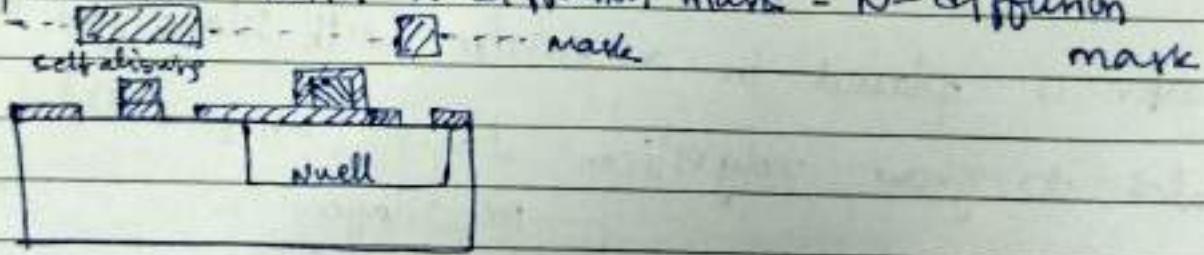
3) n-diffusion

4) p diff

5) contact

6) metal
mark12) protective layer of SiO_2 

13) patterned with n-diffusion marks - n-diffusion



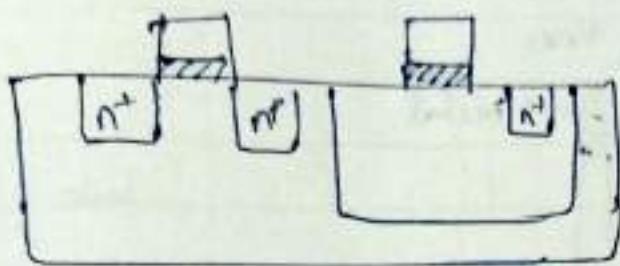
Those areas which are exposed on the fits when n+ region will be grown.

Self-align: poly is唱歌的 ones N-MOS blocks the diffusion

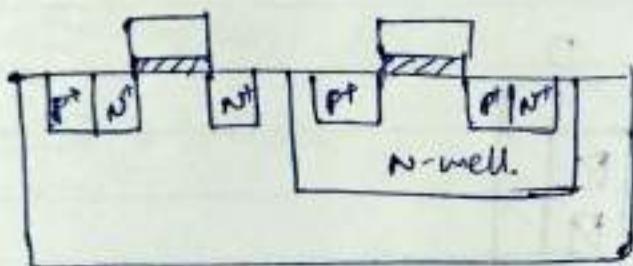
So, source & drain are separated due to the gate.

Source & drain are automatically formed without precisely aligning the mask.

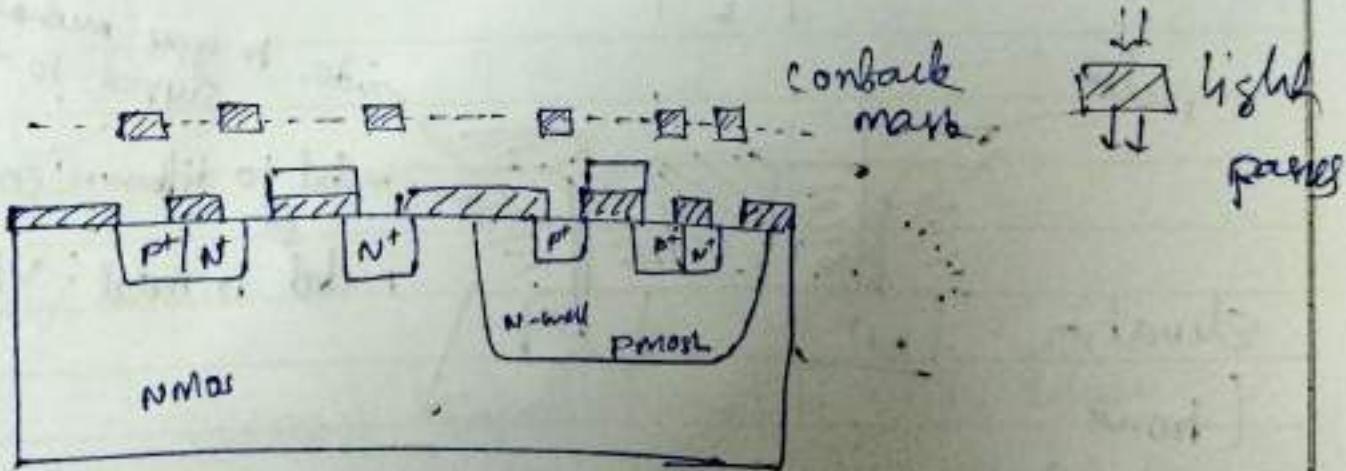
⑭ Diffusion / Ion Implantation by the self aligning process.



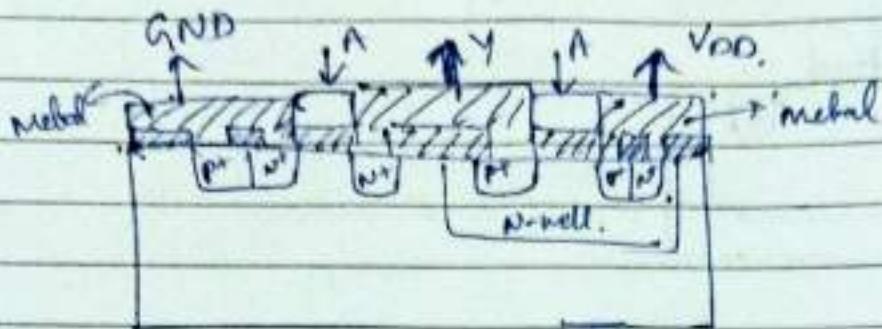
⑮ Self-aligning process for p-type diffusion



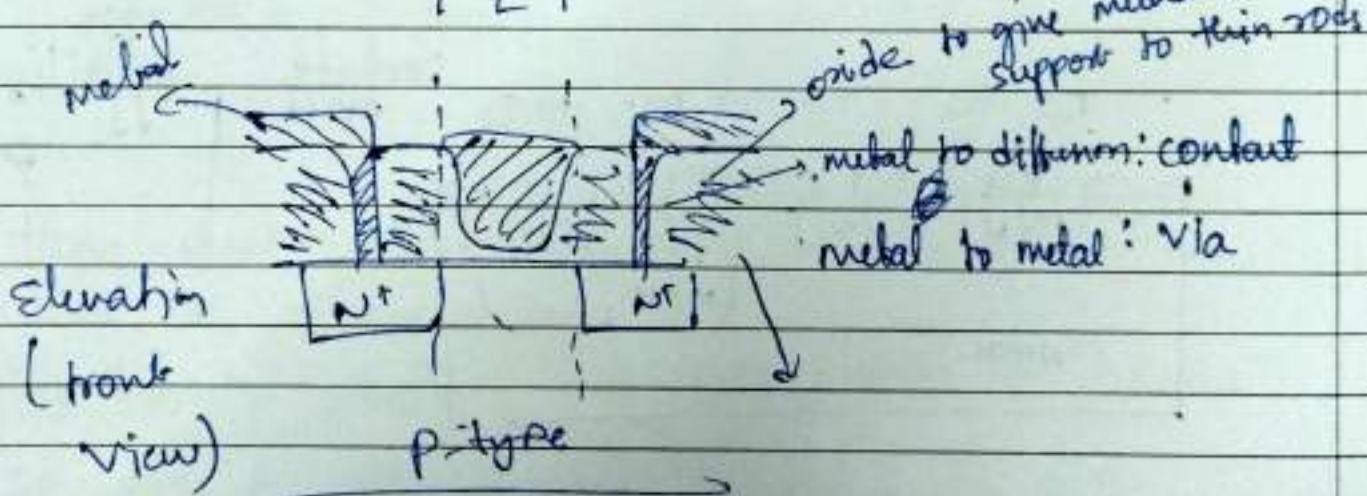
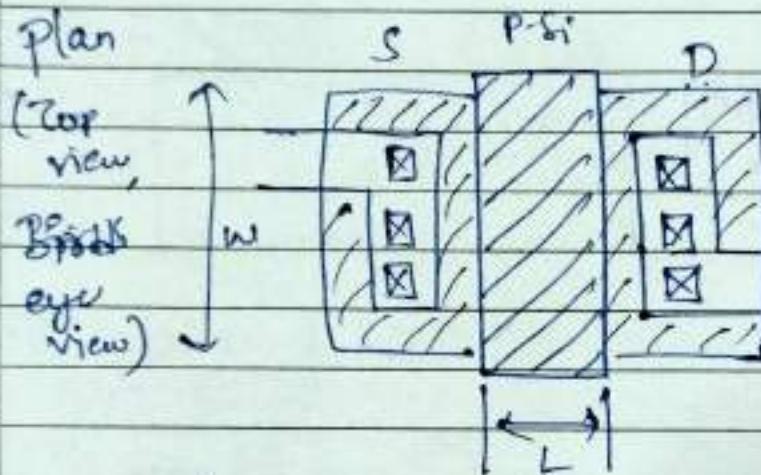
⑯ Contact mask



13) metallization mask

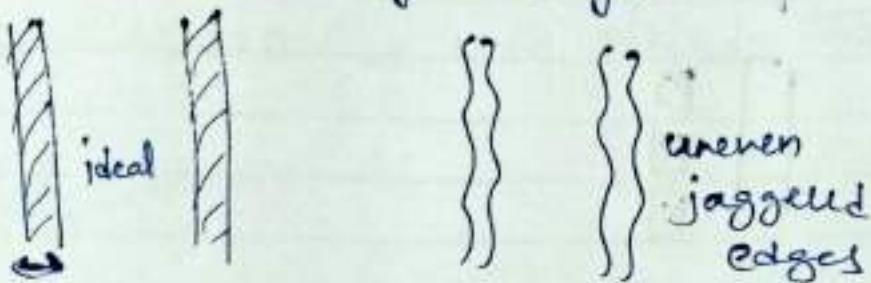


Plan

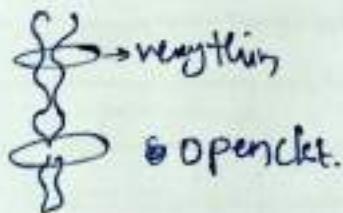


Design Rules

- i) Minimum width of a Layer

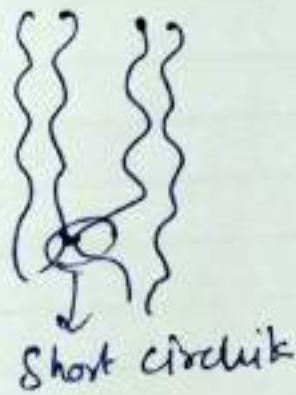


if not maintain min width then



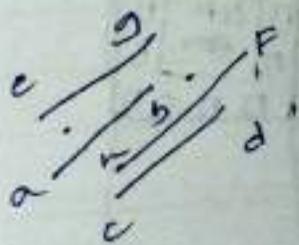
- ii) min space separation b/w 2 layers

similar



short circuit

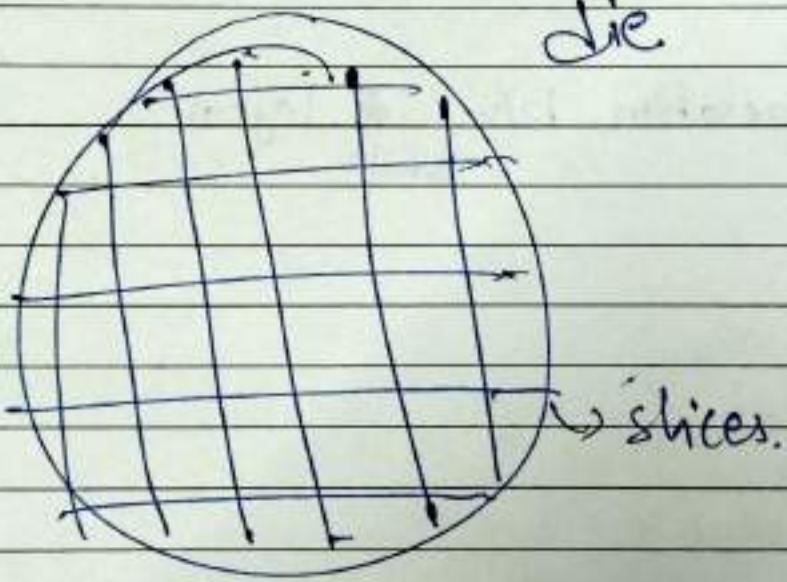
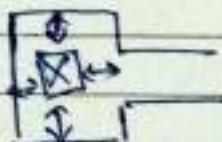
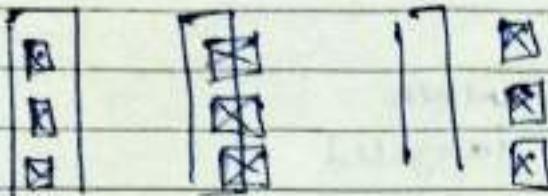
- iii) minimum ~~cross~~ separation b/w diff layers
to avoid parasitic b/w adjacent layers



e.g. e-g is above
h-f is above cd.

N-layer NC₂ rules.

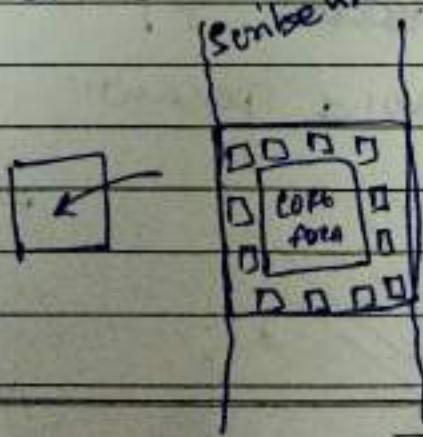
(4) minimum overlap



SCRIBBLE LINES

Roller

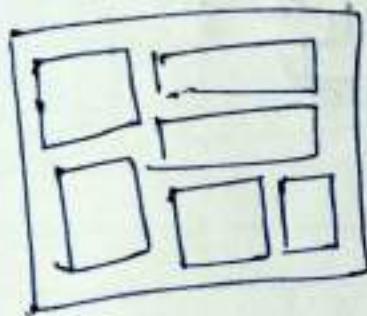
(scribble lines)



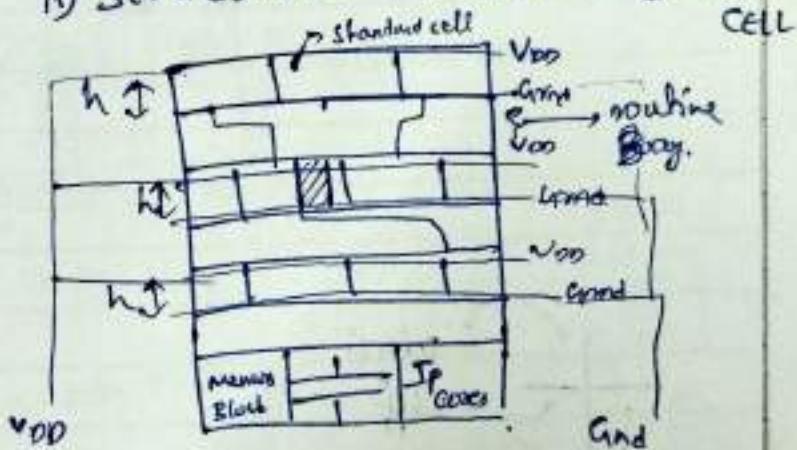
- i) FULL CUSTOM \rightarrow making from scratch (transistor).
to meet certain .
- ii) SEMI CUSTOM \rightarrow using already available.
- iii) Gate ARRAY.

25/Sept/24

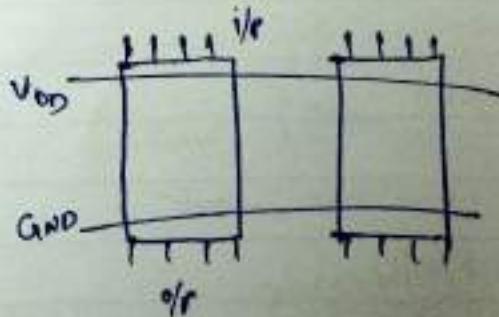
i) FULL CUSTOM DESIGN



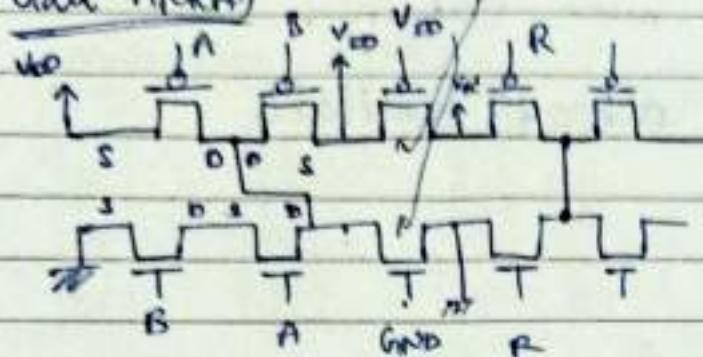
ii) SEMI CUSTOM DESIGN \rightarrow FILLER CELL



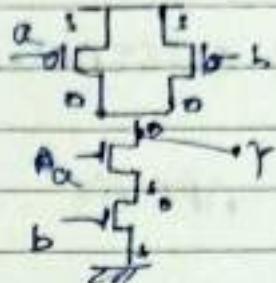
Filler cells : so, that unadjacent layer can connect.



3) Gate -ARRAY

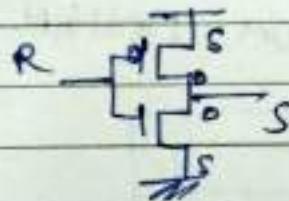


$$f = \overline{a} \cdot b$$

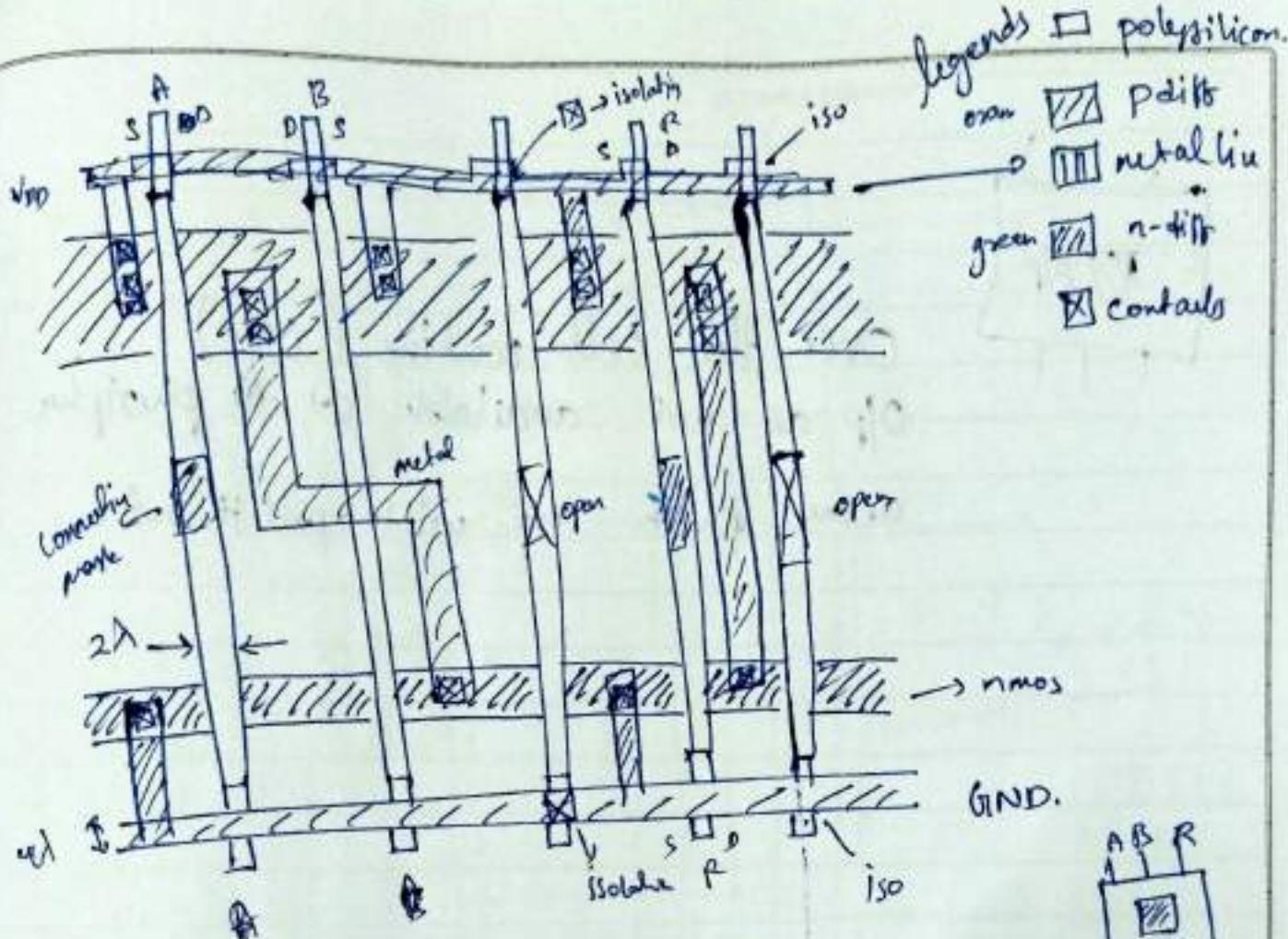


leave one transistor each by connecting

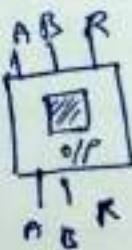
$$\text{PMOS} = \text{VDD} \quad \& \quad \text{NMOS} = \text{GND}$$



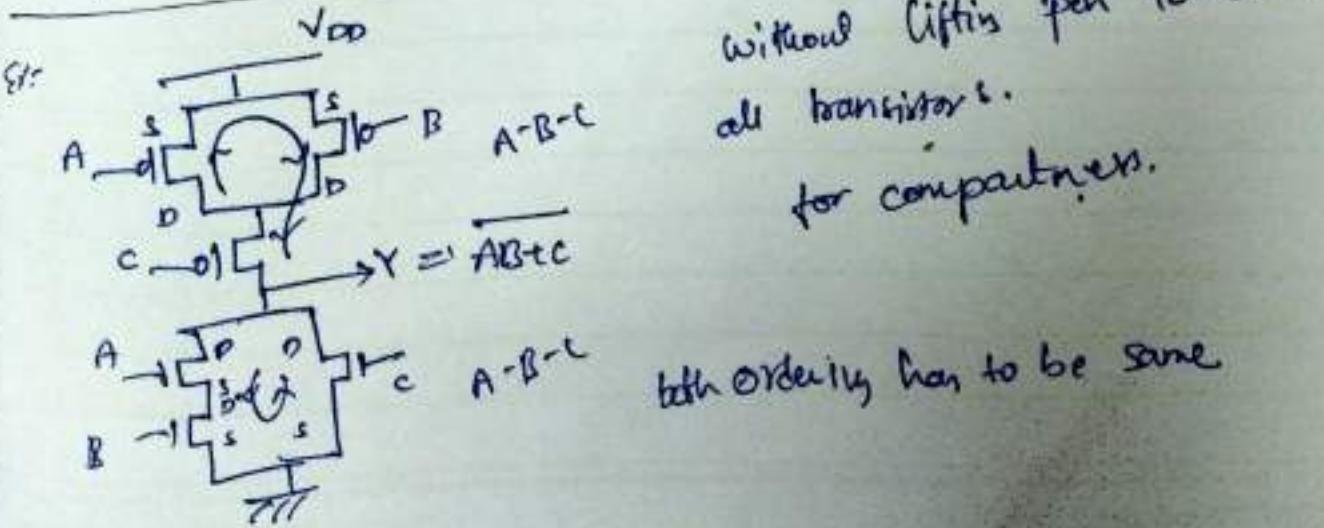
$\text{---} \text{---}$: -polysi.
 $\text{---} \text{---}$ -Diff

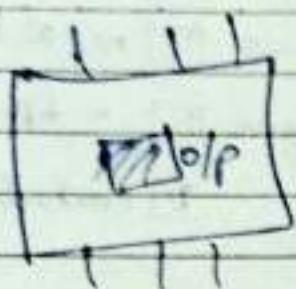


LAUT. Lambda rule

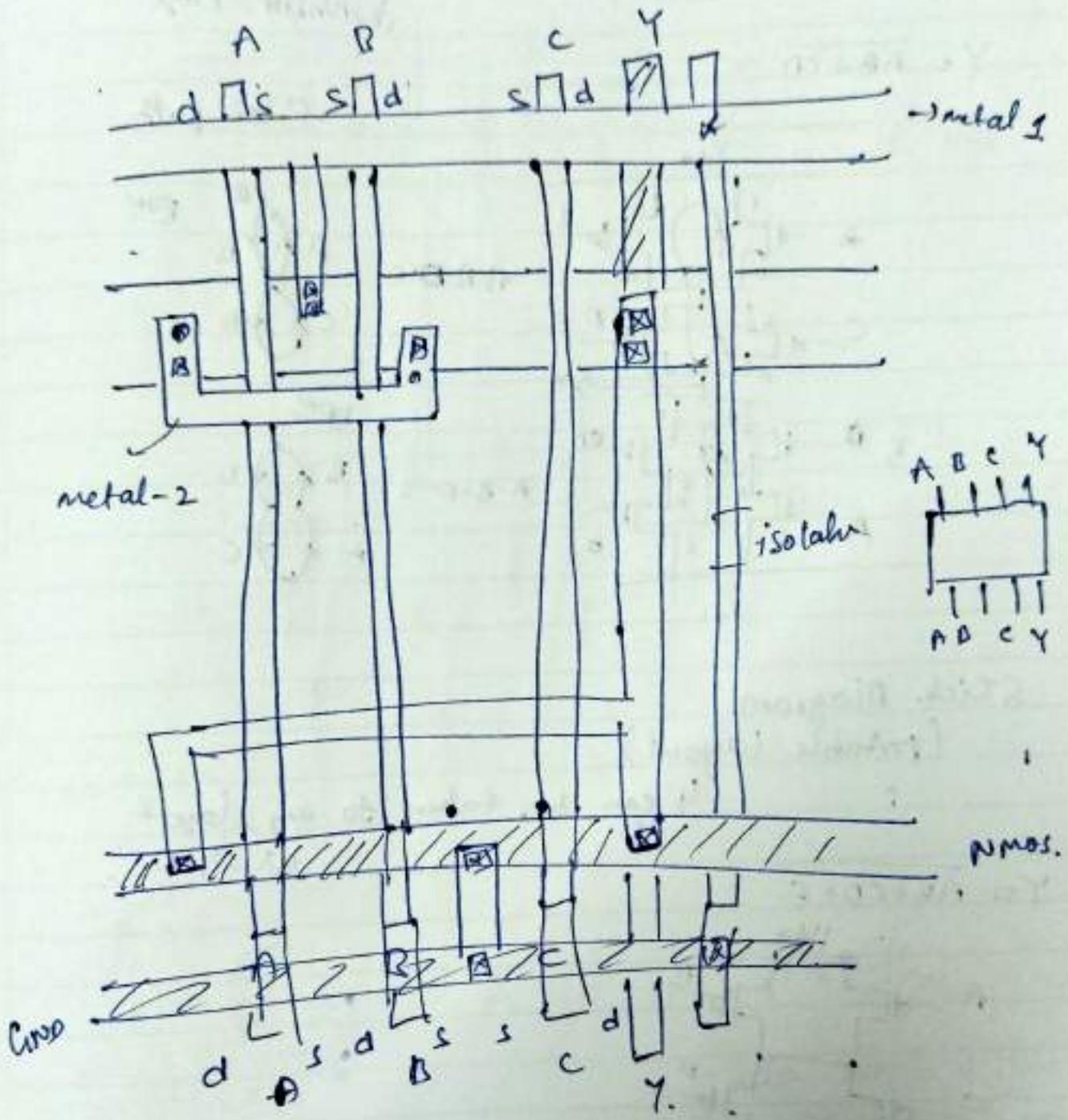


'PITCH' is spatial frequency of repetition of
polymer lines.





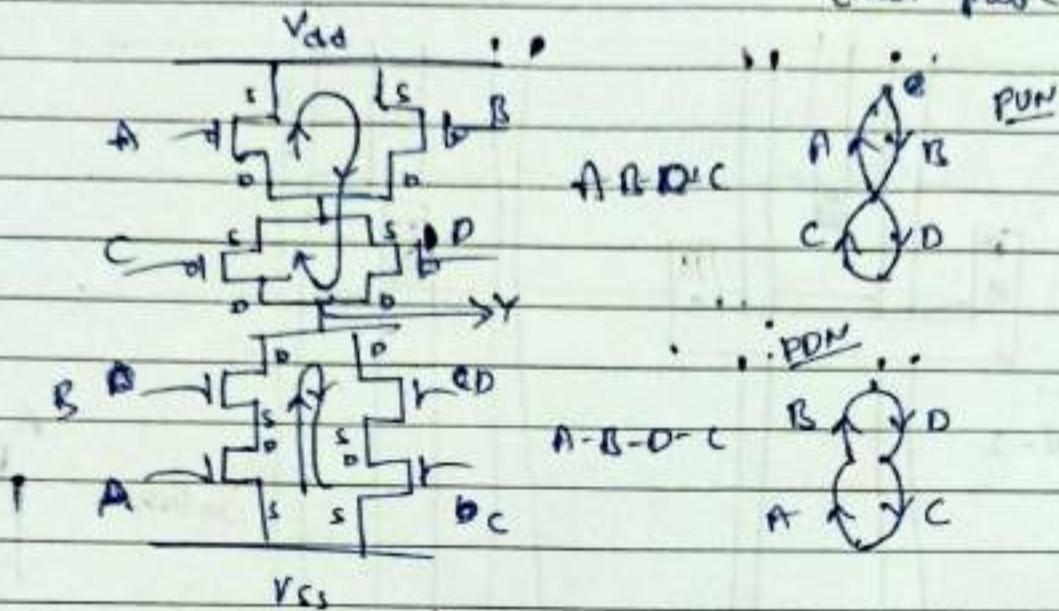
Over the cell routine (OTC)
O/p are not available @ the phosphine
above plain we will pull it out.



~~vanisher = edge~~

$$Y = \overline{AB} + CD$$

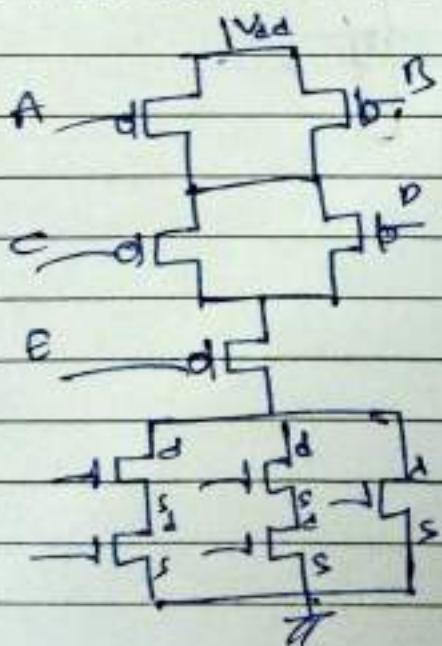
Euler path

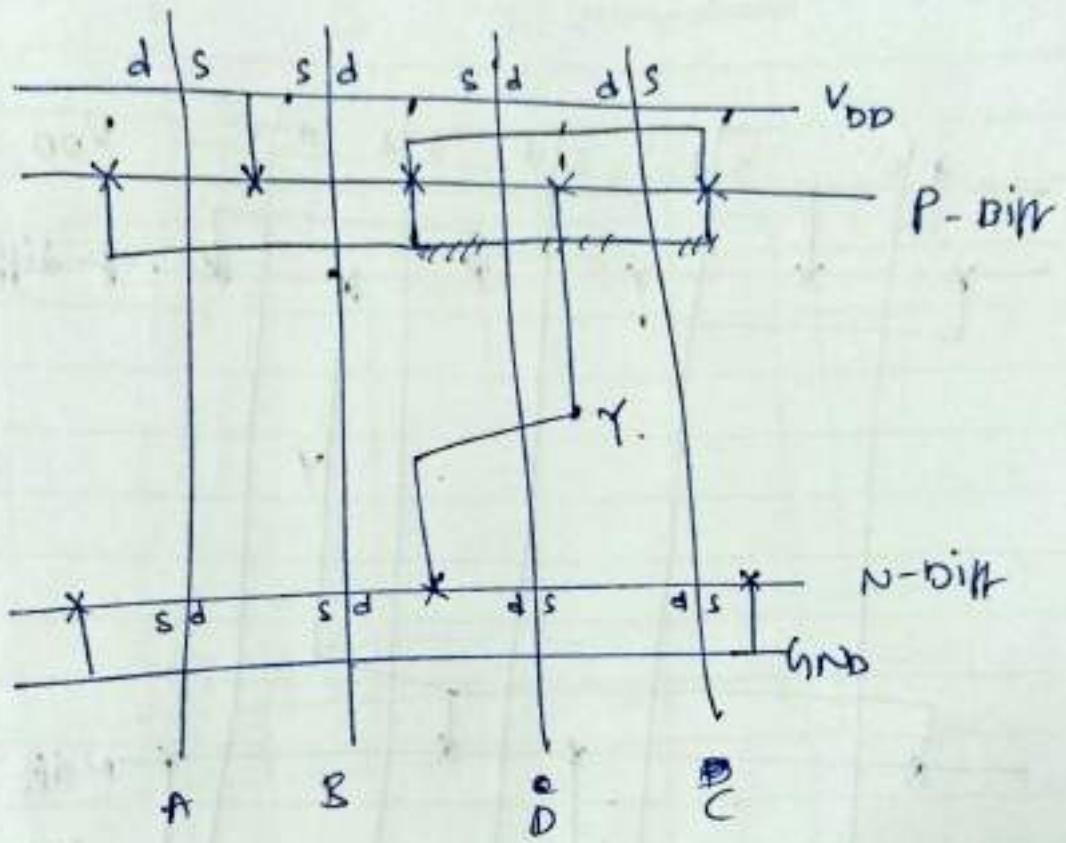


Stick Diagram
(portable layout)

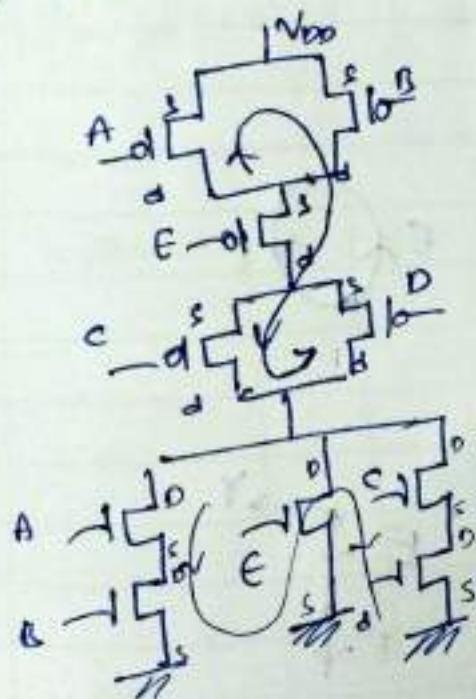
↳ can be taken to any layout
↳ 4x2x3x1

$$Y = \overline{AB} + CD + F$$



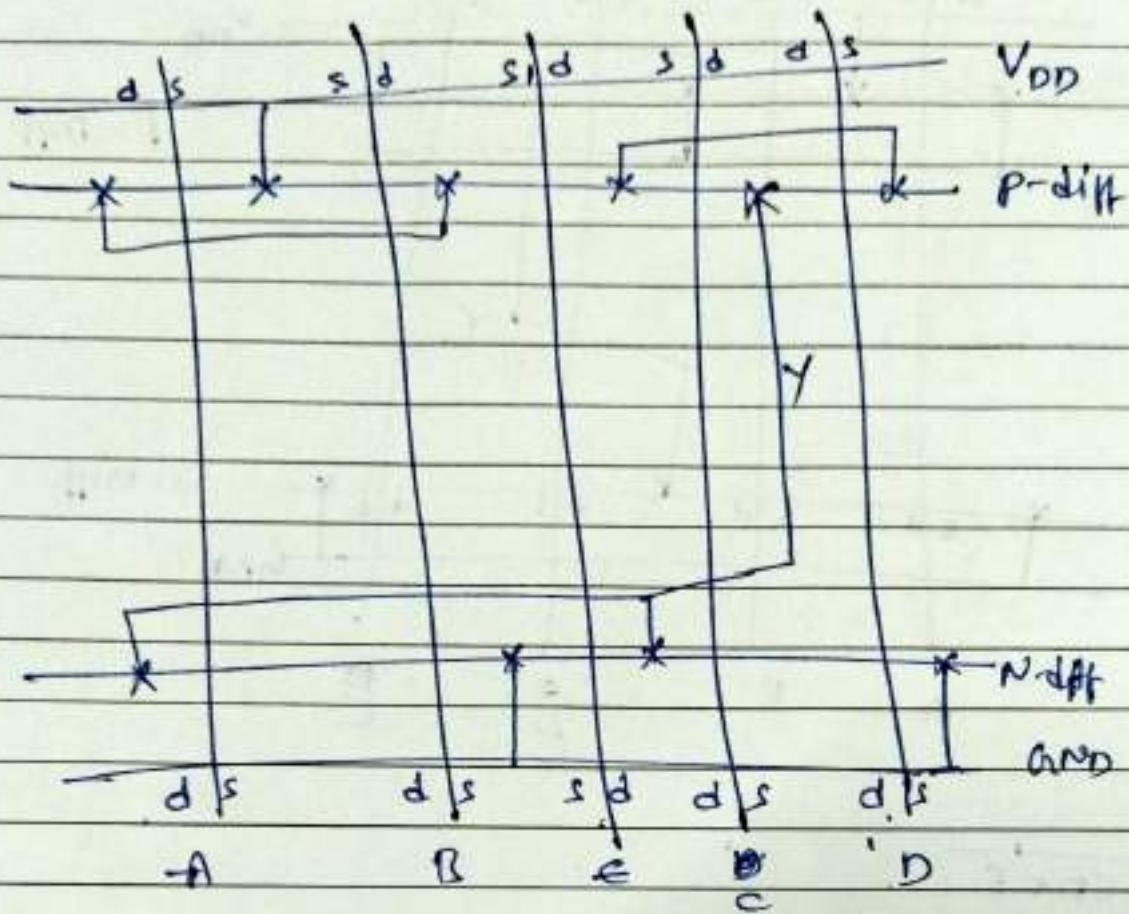


$$Y = \overline{AB + CD + E}$$



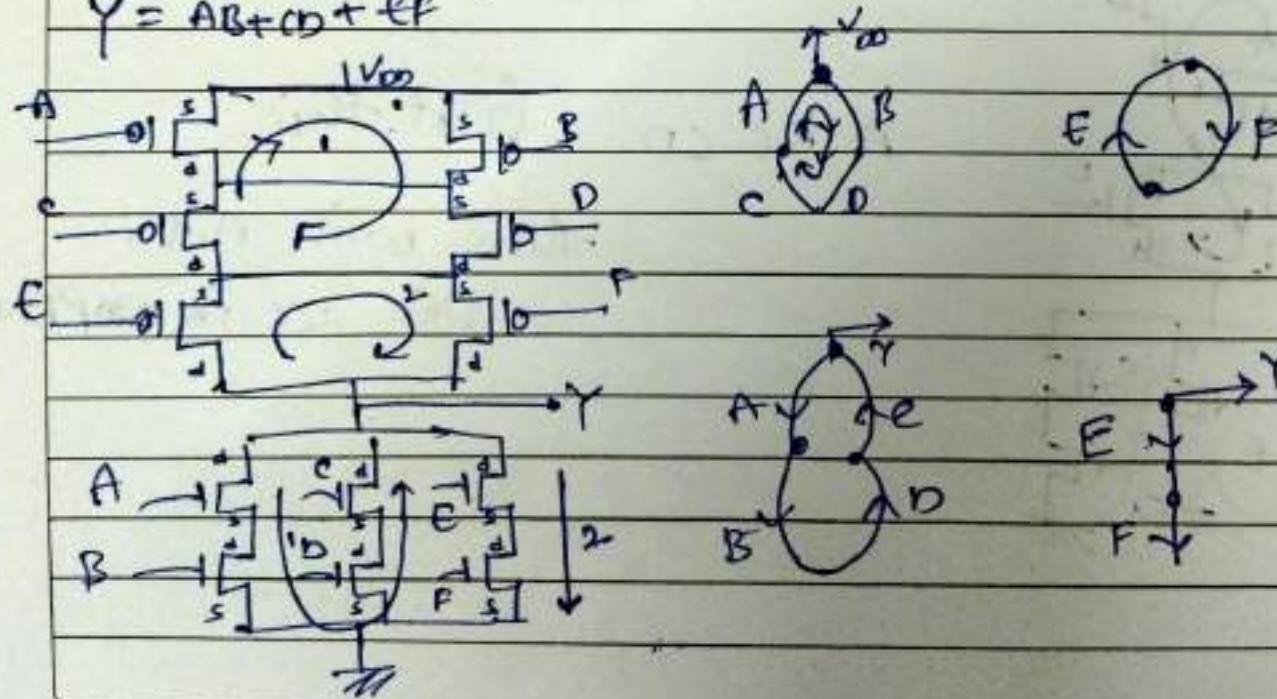
A B C D hint this

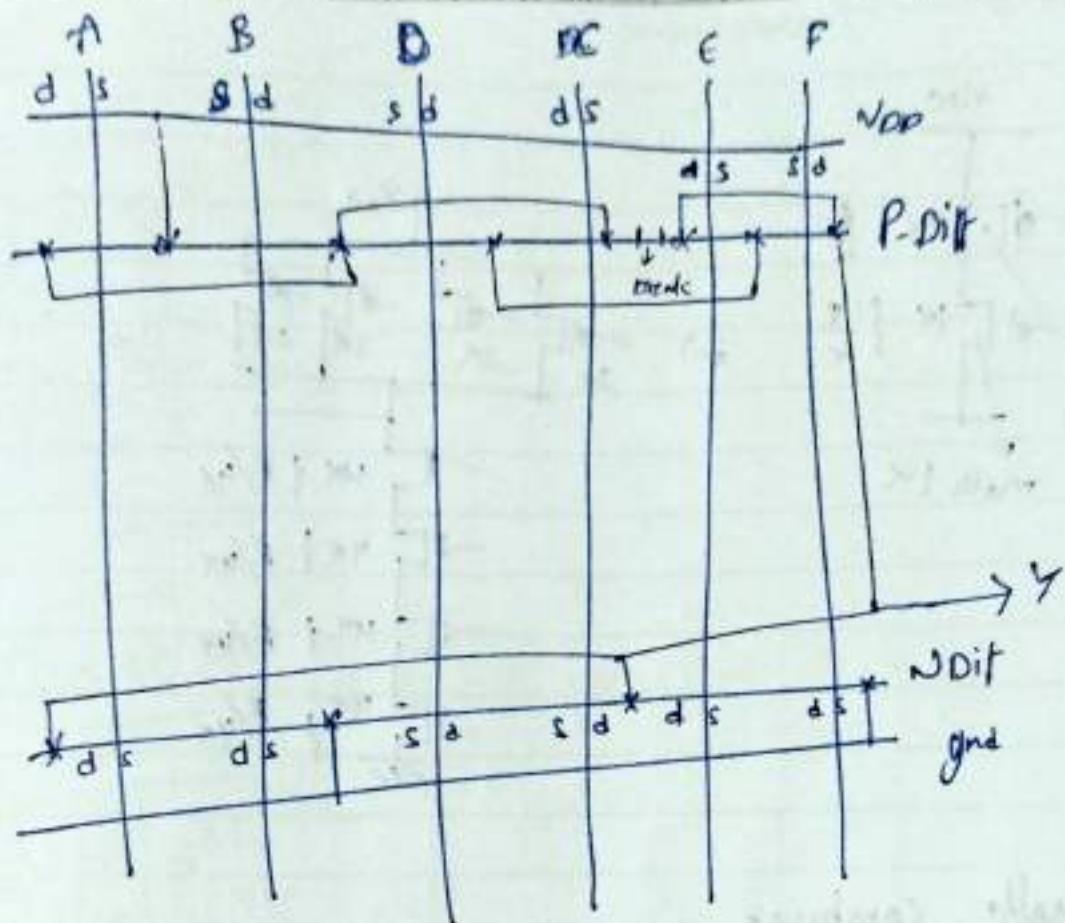
then write A, B, C,
D, E, acc in \oplus PDN.



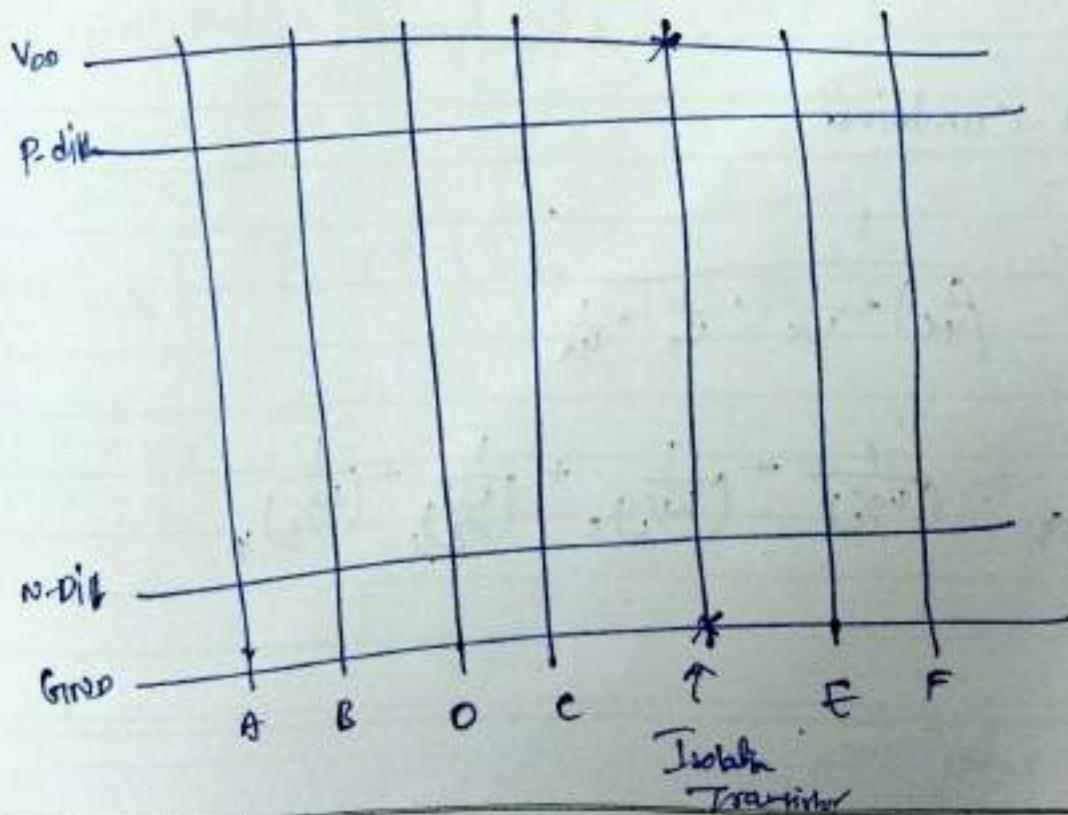
30 Sept/24

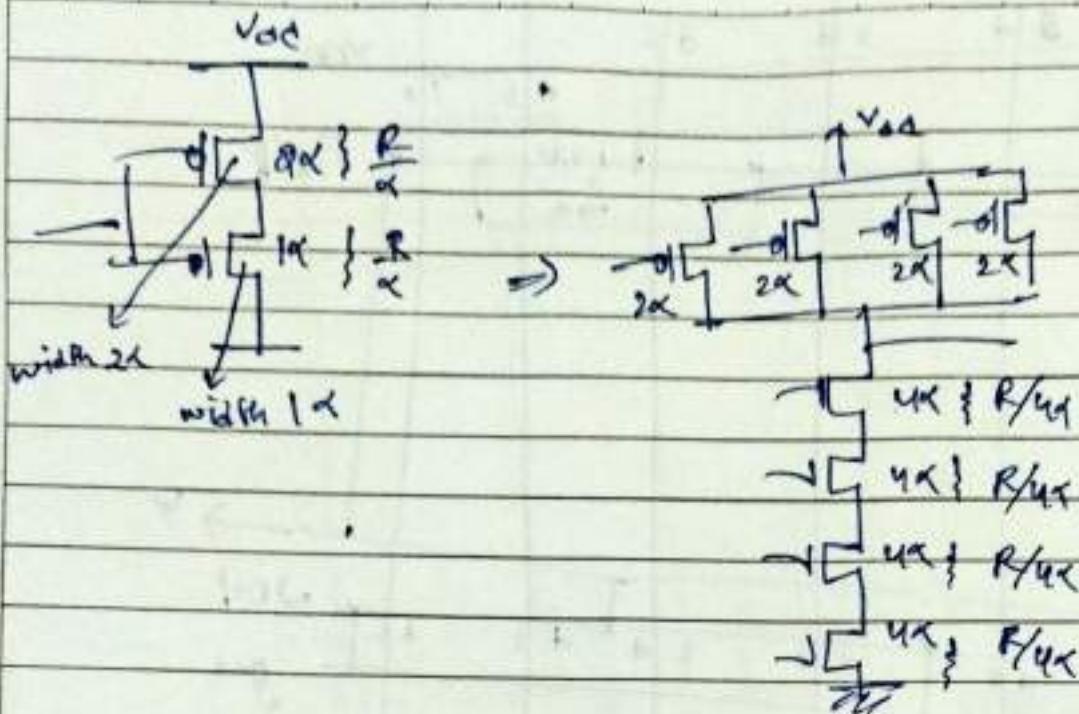
$$Y = \overline{AB + CD + EF}$$





Gate array





Parallel combined

$$\left(\frac{w}{l}\right)_{eq} = \left(\frac{w}{l}\right)_1 + \left(\frac{w}{l}\right)_2 + \left(\frac{w}{l}\right)_3 + \left(\frac{w}{l}\right)_4 = 4 \frac{w}{2k}$$

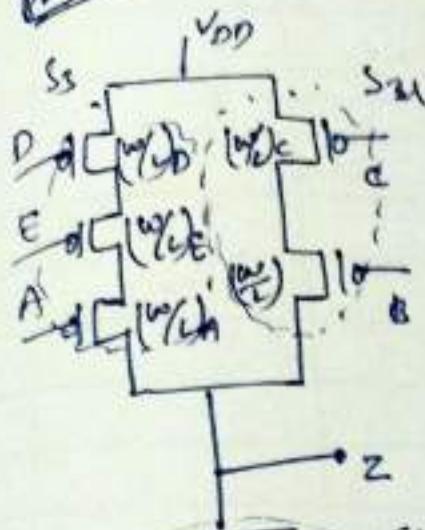
Series combined

$$1/\alpha = \frac{1}{(4k)} + \frac{1}{4k} + \frac{1}{4k} + \frac{1}{4k}$$

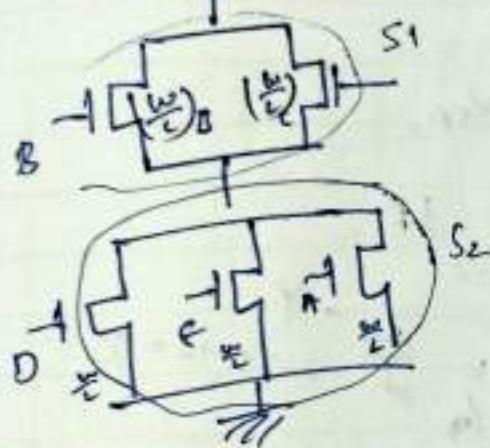
$$\left(\frac{1}{w/l}\right)_{eq} = \left(\frac{1}{w/l}\right)_1 + \left(\frac{1}{w/l}\right)_2 + \left(\frac{1}{w/l}\right)_3 + \left(\frac{1}{w/l}\right)_4$$

Exam → stick + layout + Equivalent/Gerüst
n. all.

problem



$$\Rightarrow -\text{ol} \Gamma \left(\frac{w}{L} \right) \text{PMOS}$$

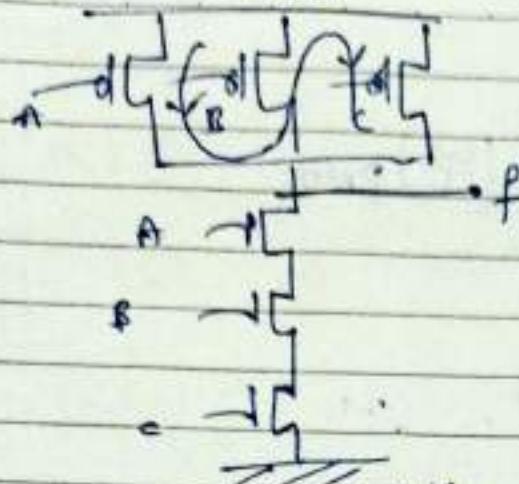


$$\Rightarrow -\text{ol} \Gamma \left(\frac{w}{L} \right) \text{nMOS}$$

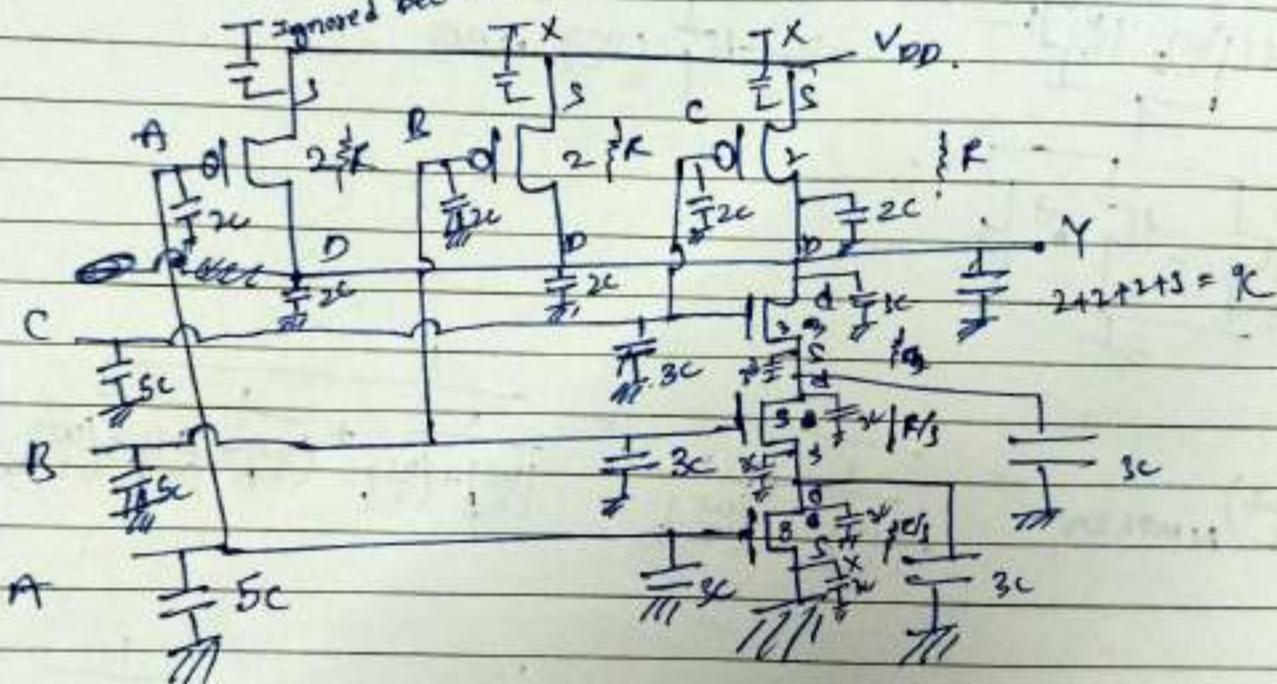
$$\left(\frac{w}{L} \right)_{\text{nMOS, ev}} = \frac{1}{\left(\frac{w}{L} \right)_{S1}} + \frac{1}{\left(\frac{w}{L} \right)_{S2}} = \frac{1}{\left(\frac{w}{L} \right)_B + \left(\frac{w}{L} \right)_C} + \frac{1}{\left(\frac{w}{L} \right)_D + \left(\frac{w}{L} \right)_E + \left(\frac{w}{L} \right)_A}$$

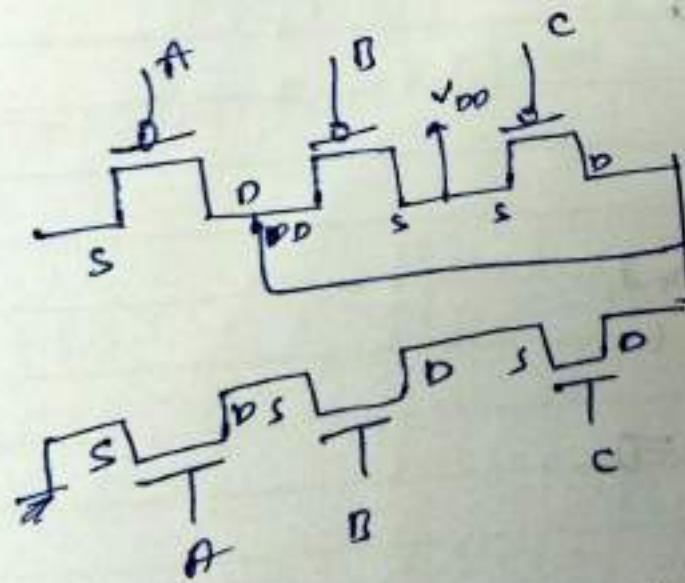
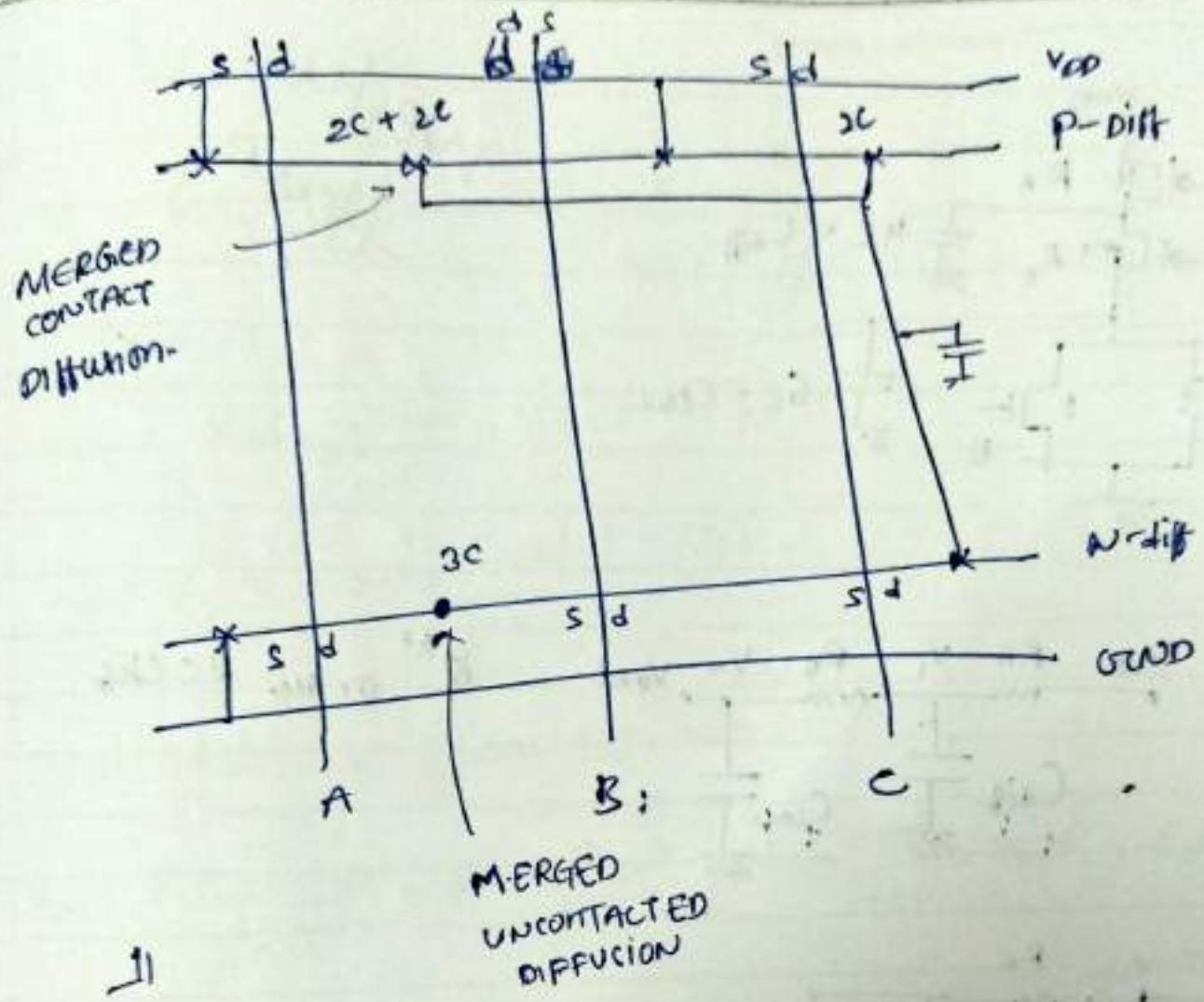
$$\left(\frac{w}{L} \right)_{\text{PMOS, ev}} = \left(\frac{w}{L} \right)_{S3} + \left(\frac{w}{L} \right)_{S4} = \frac{1}{\left(\frac{w}{L} \right)_B + \left(\frac{w}{L} \right)_C + \left(\frac{w}{L} \right)_A} + \frac{1}{\left(\frac{w}{L} \right)_D + \left(\frac{w}{L} \right)_E}$$

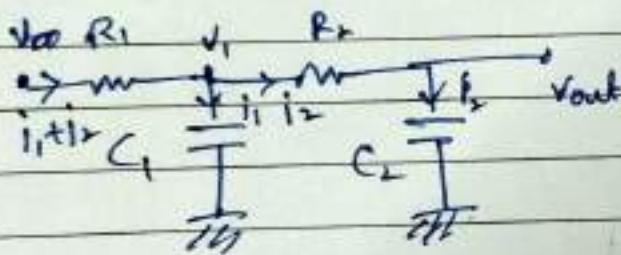
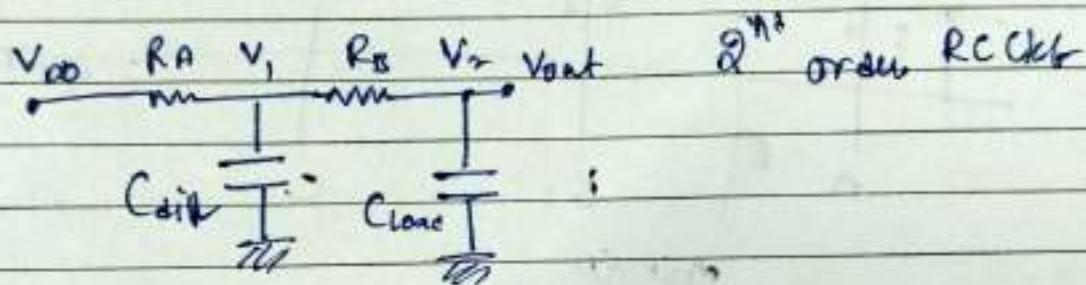
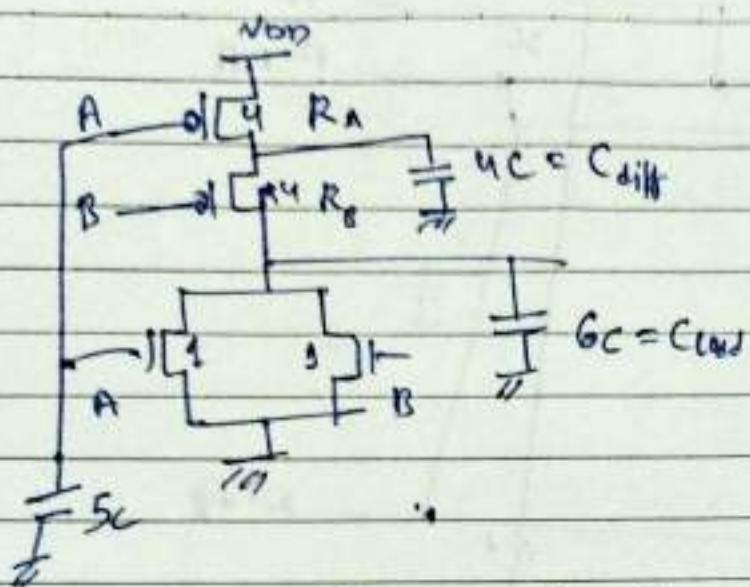
$$J = \overline{ABC}$$



~~newly non-switching~~





Wester
Hans

$$i_1 = C_1 \frac{dv_1}{dt} \quad i_2 = C_2 \frac{dv_{out}}{dt}$$

$$V_{DD} - (i_1 + i_2)R_1 - v_1 = 0$$

$$V_{DD} - R_1 \left(C_1 \frac{dv_1}{dt} + C_2 \frac{dv_{out}}{dt} \right) - v_1 = 0$$

$$V_1 - i_2 R_2 - V_{out} = 0$$

$$V_1 - R_2 C_2 \frac{dV_{out}}{dt} - V_{out} = 0 \quad \textcircled{2}$$

from 2.

$$V_1 = R_2 C_2 \frac{dV_{out}}{dt} + V_{out} \quad \textcircled{3}$$

$$V_{out} = V_1 - R_2 C_2 \frac{dV_{out}}{dt} \quad \textcircled{4}$$

Substituting V_1 from (3) into (1).

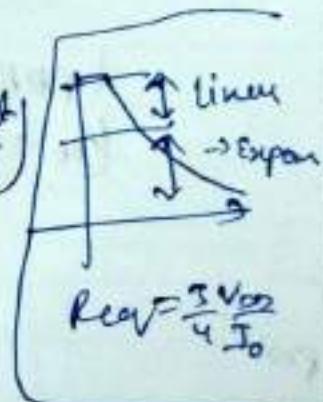
$$V_{DD} - R_1 C_1 \left[\frac{dV_{out}}{dt} + R_2 C_2 \frac{d^2 V_{out}}{dt^2} \right] - R_1 i_2 \frac{dV_{out}}{dt} = V_{out} + R_2 i_2 \frac{dV_{out}}{dt}$$

$$V_{DD} = V_{out} + \left(R_1 C_1 + R_1 C_2 + R_2 C_2 \right) \frac{dV_{out}}{dt} + R_1 C_1 R_2 C_2 \left(\frac{d^2 V_{out}}{dt^2} \right)$$

neglect.

$$V_{DD} - [R_1 C_1 + C_2 (R_1 + R_2)] \frac{dV_{out}}{dt} - V_{out} = 0$$

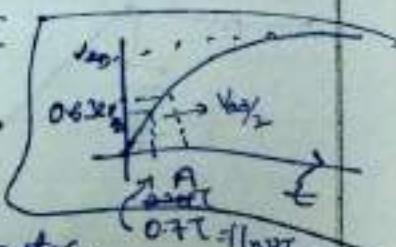
A



$$V_{DD} - A \frac{dV_{out}}{dt} - V_{out} = 0$$

$$V_{out}(t) = (1 - e^{-\frac{t}{TA}}) V_{DD}$$

charging capacitor.



$$t_{PDk} = (R_1 C_1 + R_1 + R_2) C_2 \rightarrow \text{time constant for unit step } (\ln 2) t_{PDk}$$

$V_{DD} \rightarrow V_{ad}$

Try Substitute Vout from ④ to ①

you will get $V_1(t) = V_{DD} \left(1 - e^{-t/B}\right)$

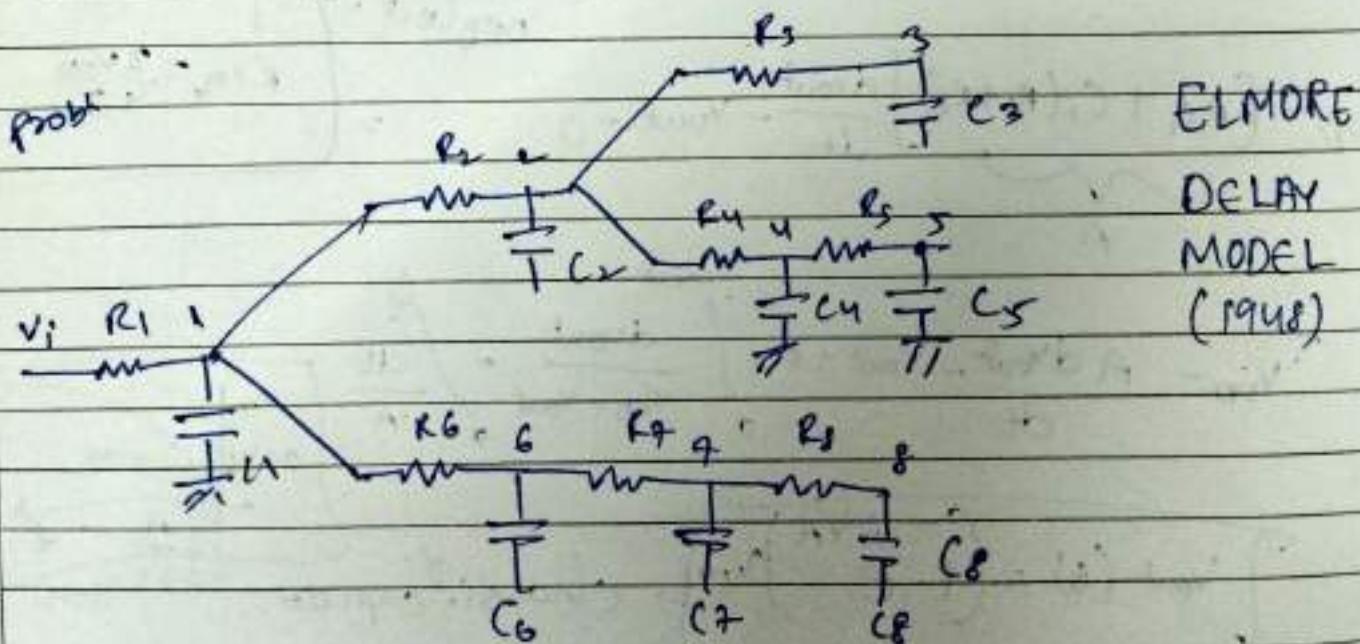
$$\therefore B = R_1 C_1 + R_2 C_2$$

$t_{PDR} (V_{DD} \rightarrow V_1) = R_1 C_1 + R_2 C_2$ (In it \int)

$$t_{PDR} = \frac{C_1 R_1}{R_1 + R_2}$$

shown
steps

$t_{PDR} = C_1 R_1 + C_2 R_2$ only R_1 is shown b/w
 $(V_{DD} \rightarrow V_1)$ V_1 & V_{DD}



$$T_{V_{in-7}} = C_1(R_1) + C_2(R_1) + C_3(R_1) + C_4(R_1) + C_5(R_1) \\ + C_6(R_1 + R_6) + C_7(R_1 + R_6 + R_7) + C_8(R_1 + R_6 + R_7)$$

$$T_{V_{in-5}} = C_1 R_1 + C_2(R_1 + R_3) + C_3(R_1 + R_3) + C_4(R_1 + R_3 + R_4) + C_5 \downarrow \\ (R_1 + R_3 + R_4) + C_6 R_4 \\ + C_7 R_1 + C_8 R_1$$

~~also~~

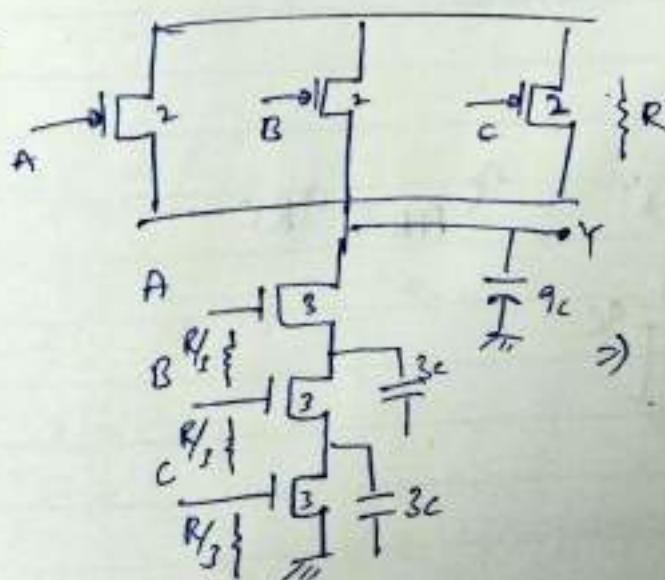
$$T_{V_{in-5}} = R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8)$$

$$+ R_2(C_2 + C_3 + C_4 + C_5)$$

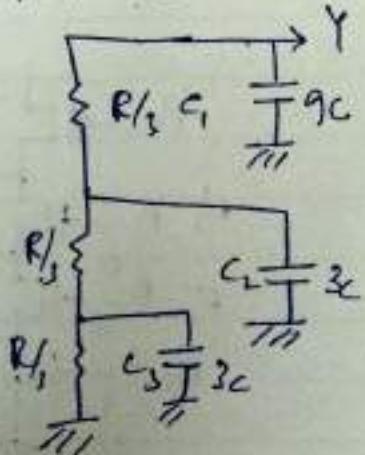
$$+ R_4(C_4 + C_5)$$

$$+ R_S(C_5)$$

pt taken shared
resistance.



T_{PD} falling



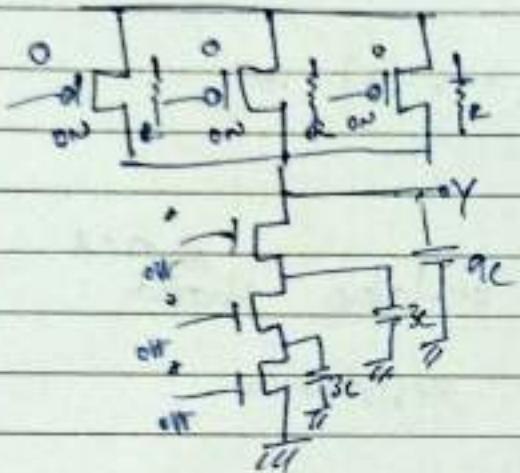
$$T_{PD} = C_1(R_1 + R_2 + R_3) \\ + C_2(R_1 + R_3) \\ + C_3(R_3)$$

$$\Rightarrow 9CR + \frac{3C \cdot 2R}{3} + \frac{3C \cdot R}{3}$$

$$\Rightarrow 9CR + 2CR + 3CR$$

$$\Rightarrow 14CR / 12CR$$

τ_{PDR} Best effect all on "on" to charge Transistors

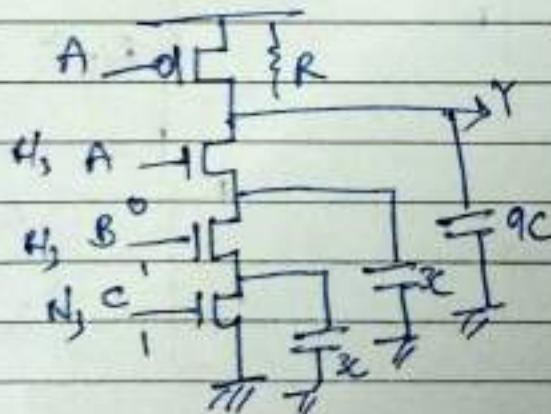


$$\tau_{PDR} = 9CR \text{ effect resistance}$$

$$\approx 3RC$$

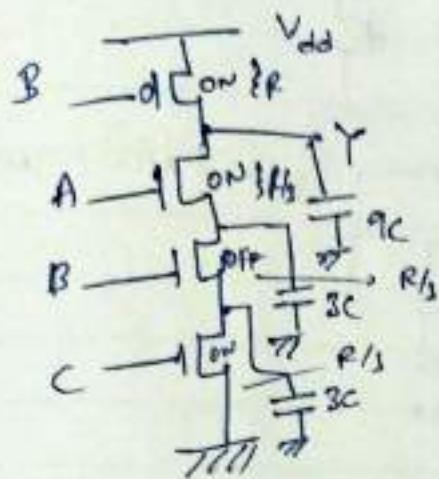
Best case (contamination delay)

for $A=0, B=1, C=1$



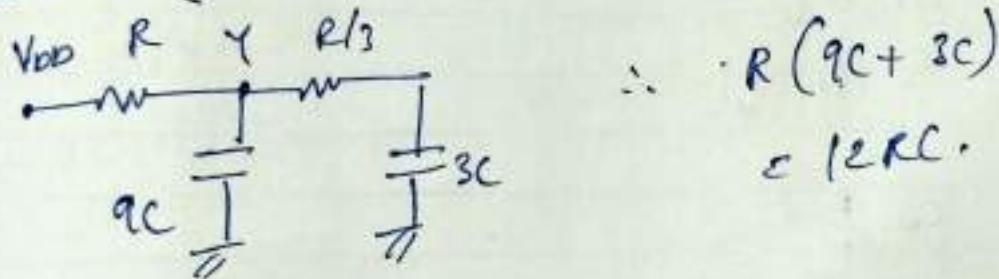
$$\tau_{PPR} = 9RC$$

for $A=1, B=0, C=1$



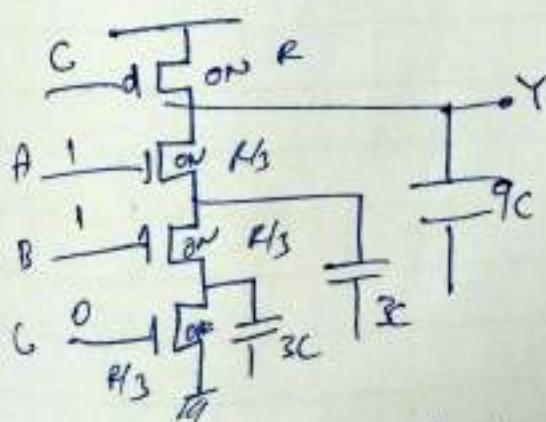
$$\begin{aligned} T_{PDR} &= q_C(R) \\ &+ 3C(R) \\ &\rightarrow \cancel{+} 12RC \end{aligned}$$

other way \rightarrow only shared resistance



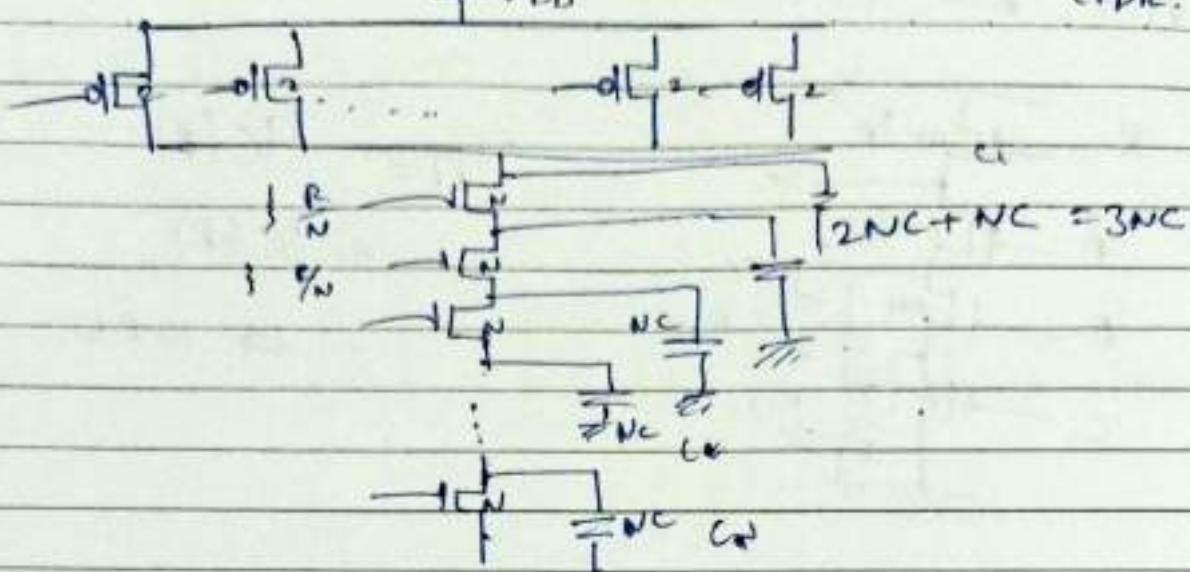
$A=1, B=1, C=0$

worst case



$$\begin{aligned} T_{PDR} &= R(q_C + 3C + 3C) \\ &= 15RC \end{aligned}$$

worst case is called propagation delay.



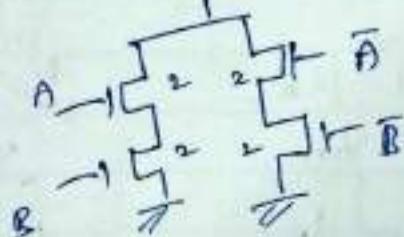
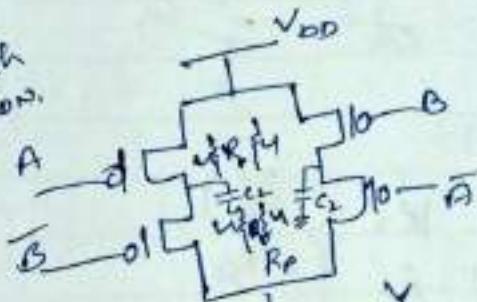
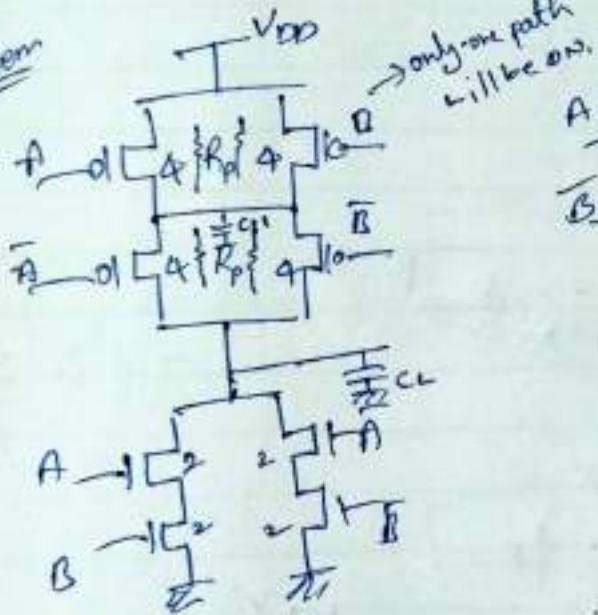
$$\Rightarrow 3NRC + \frac{RC \cdot N(N-1)}{2}$$

$$\Rightarrow \frac{6NRC + N^2RC - NRC}{2} = \frac{5N^2RC + 5NRC}{2}$$

$$\Rightarrow \frac{NRC(N+5)}{2} \Rightarrow \frac{N^2 + 5N}{2} RC \Rightarrow T \propto O(N^2)$$

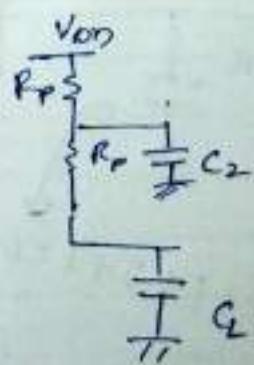
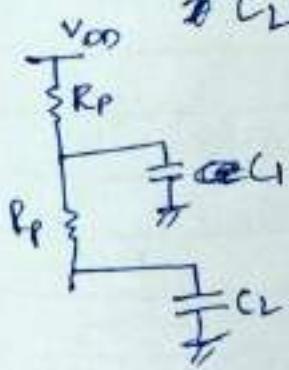
$N \leq (U/S)$ or more delay.

problem



$$T_{PDR} = C_1(R_p)$$

$$T_{PPR} = C_2(R_p + R_p)$$



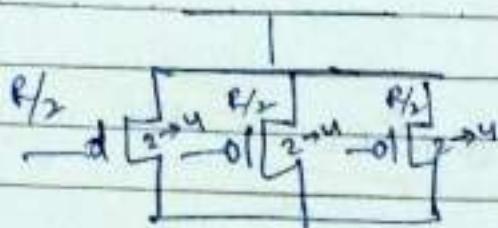
due to 4 transistors

$$C_1 > C_2$$

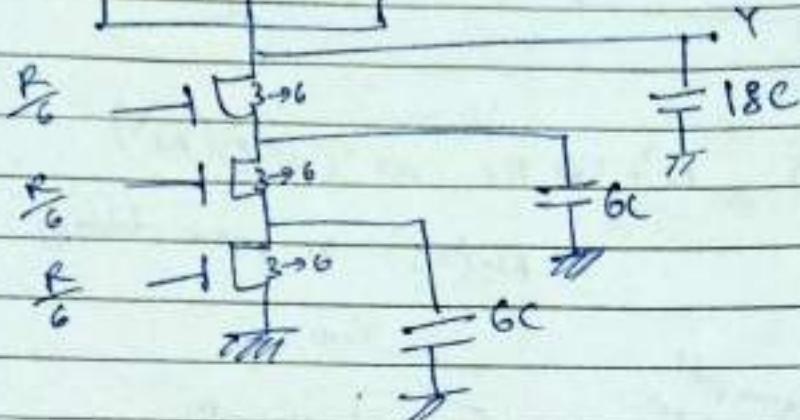
$$T_{PDR} = C_1 R_p + C_2 (2 R_p)$$

(due to only 2 transistors)

$$T_{PDR1} > T_{PDR2}$$



width increase
from 2 → 4
3 → 6

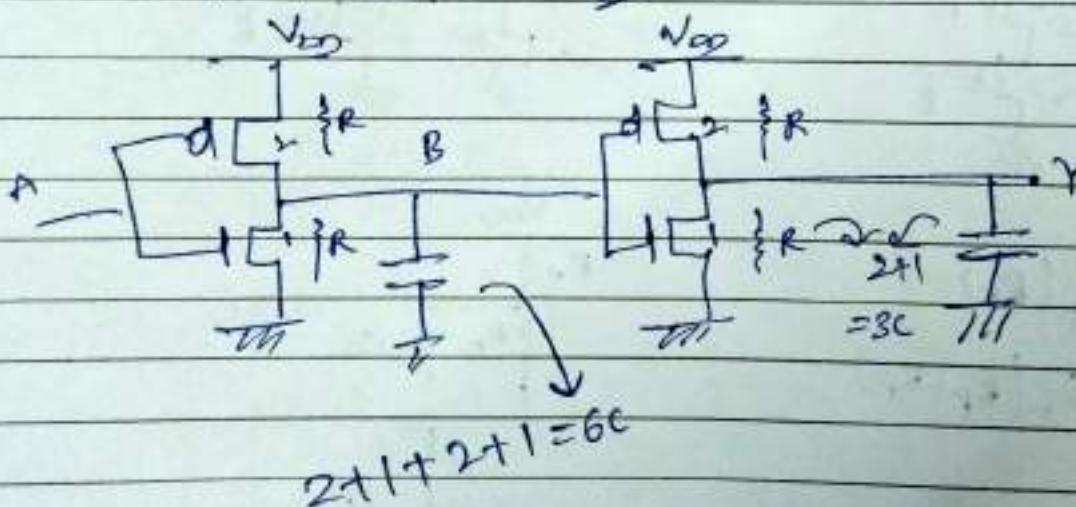


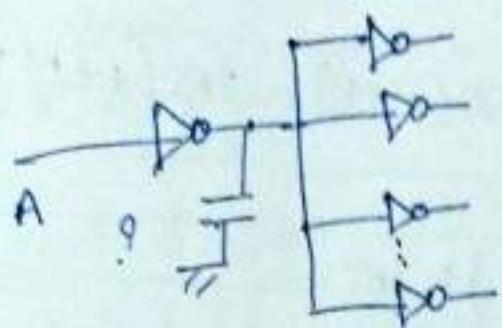
upsizing
by factor
 $x=2$

$$\tau_{PDP} = \frac{1}{R} C \left(\frac{3R}{6} \right) + \frac{1}{R} C \left(2 \cdot \frac{R}{6} \right) + \frac{1}{R} C \left(\frac{R}{6} \right)$$

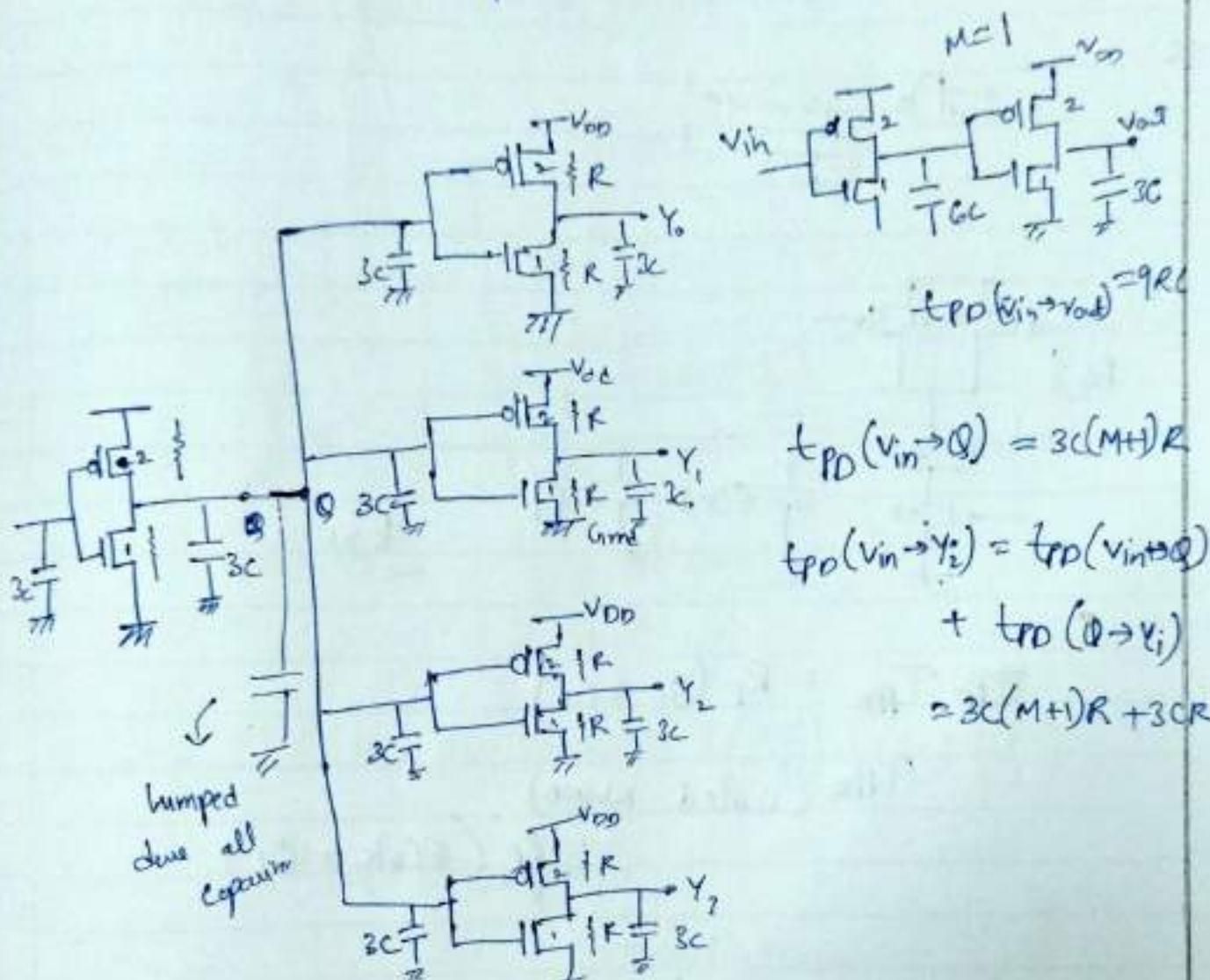
$$\Rightarrow 1/R C$$

~~nullified R, C.~~





unit inverter driving
M identical unit
inverter



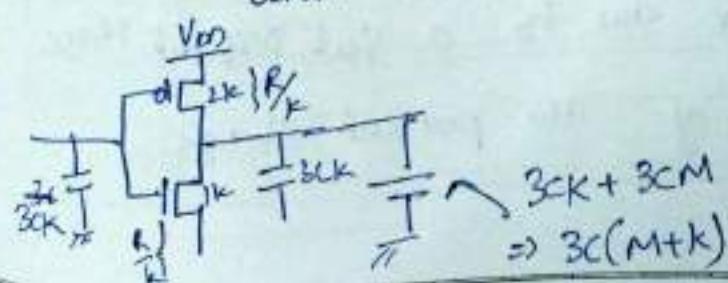
$$t_{PD}(v_{in} \rightarrow Q) = 3C(M+1)R$$

$$t_{PD}(v_{in} \rightarrow Y_i) = t_{PD}(v_{in} \rightarrow Q)$$

$$+ t_{PD}(Q \rightarrow Y_i)$$

$$= 3C(M+1)R + 3CR$$

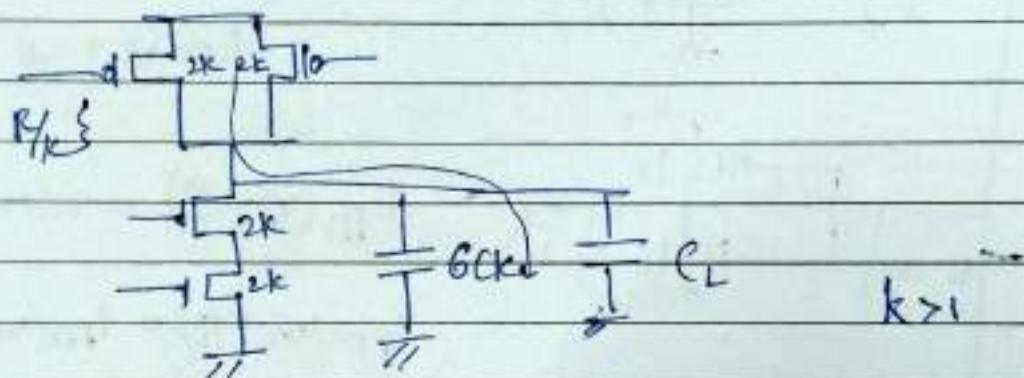
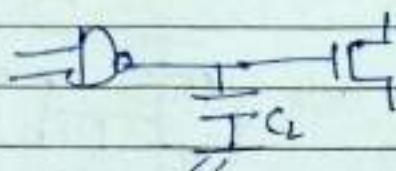
K-scaled unit inverter driving M identical unit inverters.



$$t_{PD}(V_{in} \rightarrow Y) \Rightarrow R_{eq} C_{eq} = \frac{R}{k} 3C(M+k) = 3RC\left(1 + \frac{M}{k}\right)$$

$$t_{PD}(V_{in} \rightarrow Y_i) = 3RC\left(1 + \frac{M}{k}\right) + 3RC.$$

Ans:



$$t_{PD} T_{PD} = R_p (6C_L + C_L)$$

T_{PD} (scaled NAND)

$$= \frac{R_p (6C_L k + C_L)}{k}$$

$h \rightarrow$ fan-out of 4 if all are of unit width inverter
(FO4)

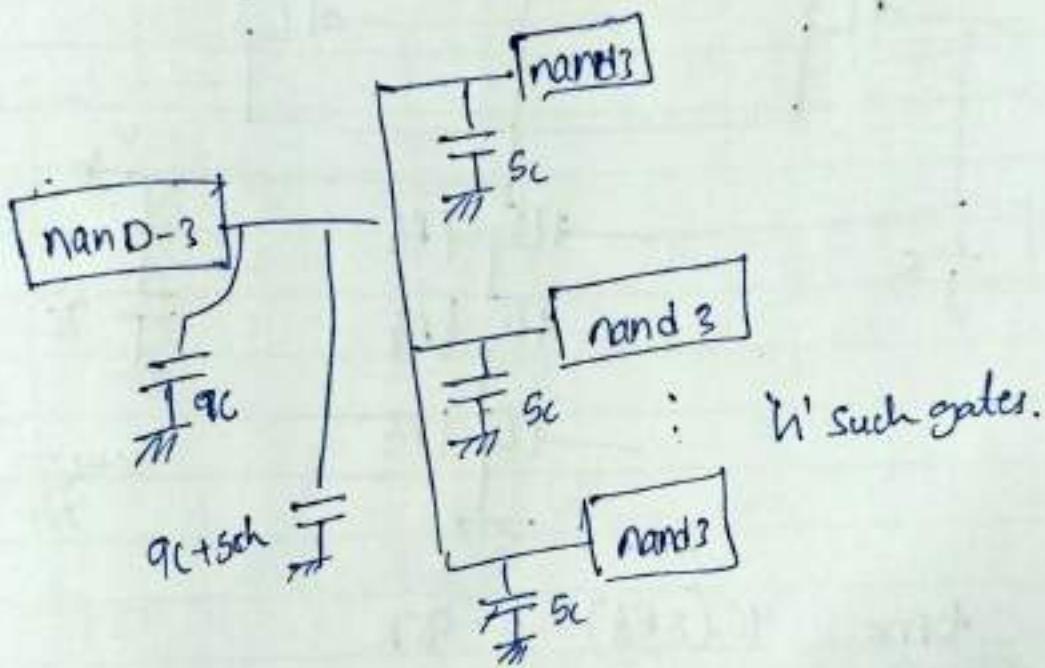
[h = electrical effort.]

h = load capacitance due to a subsequent stage
input cap of the present stage.

$$h = \frac{3c(M)}{sc K} = \cancel{\frac{M}{K}}$$

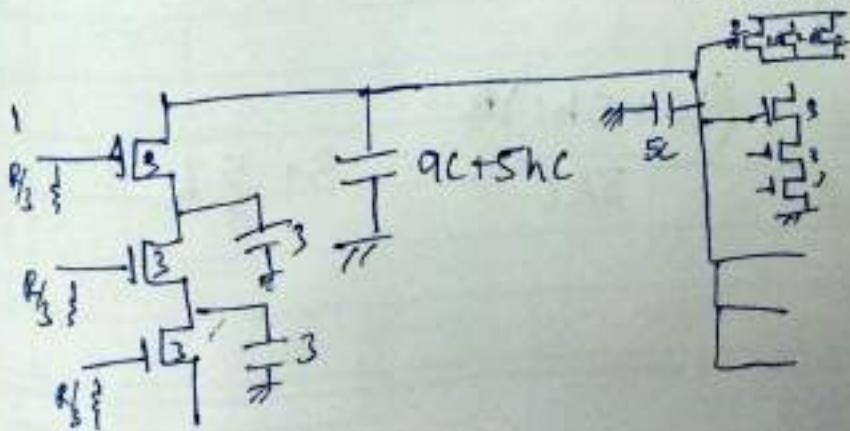
h : electrical effort

= fanout (for identical transistors)...



$$t_{PDF} = (q_C + s_h C)R + (3c) \left(\frac{2R}{3} \right) + (3c) \left(\frac{R}{3} \right)$$

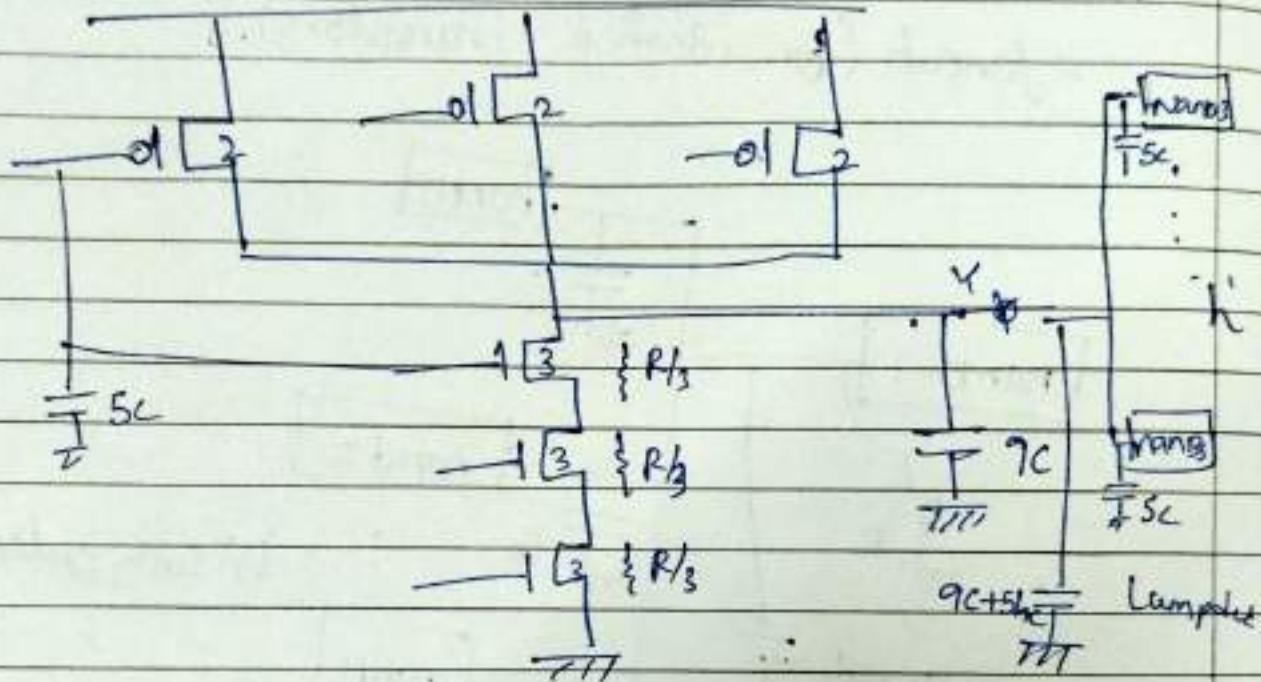
$$t_{PPF} = 12RC + \underbrace{s_h R_C}_{\text{additional term}}$$



LINEAR DELAY MODEL

(does not consider effect of intermediate capacitor).

To generate TPDR value



$$t_{PDR} = 9C(3R_3) = 9CR.$$

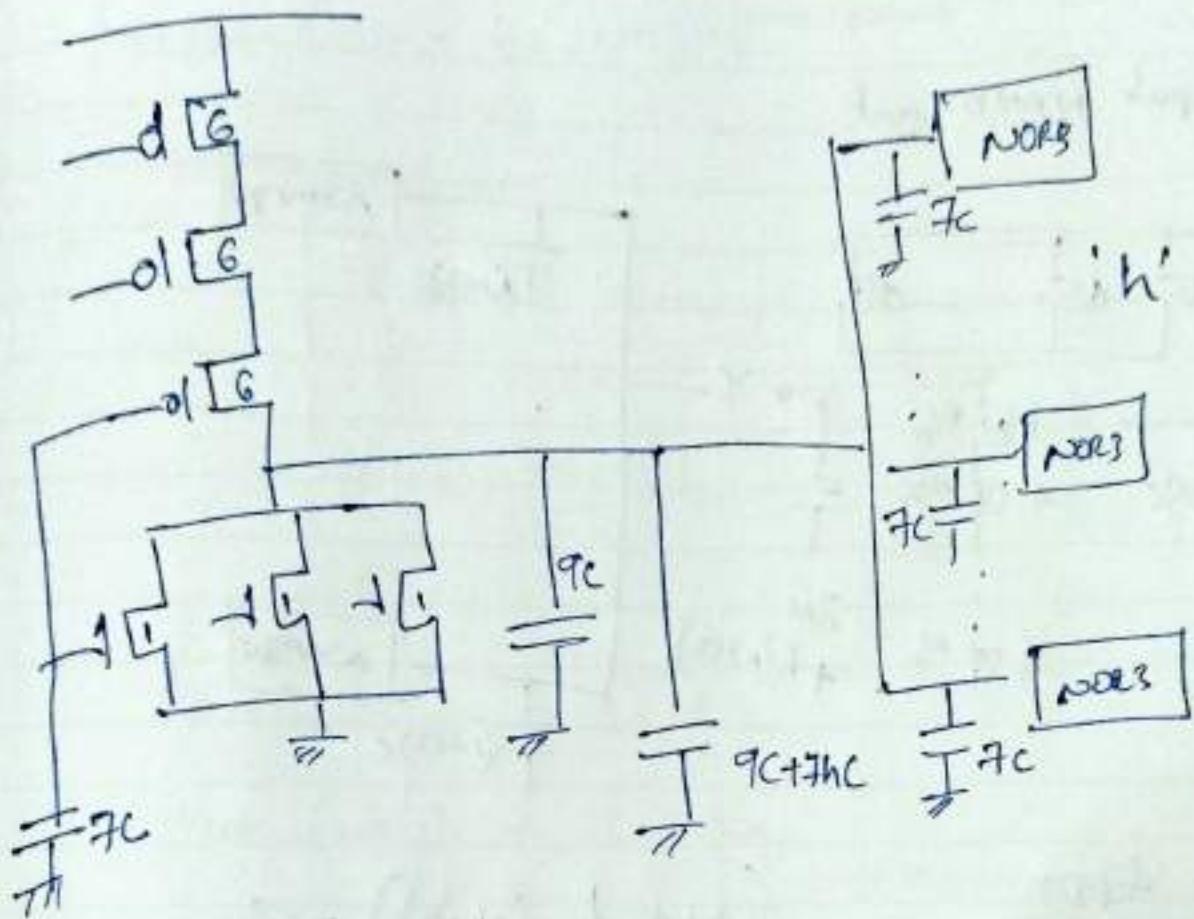
(without external load)

$$t_{PDR} = (9C + 5h_l)R$$

(driven by identical nano-3)

$$t_{PDR} = \frac{(9C + 5h_l)R}{3RC} = 3 + \frac{5}{3} h_l$$

(normalised)



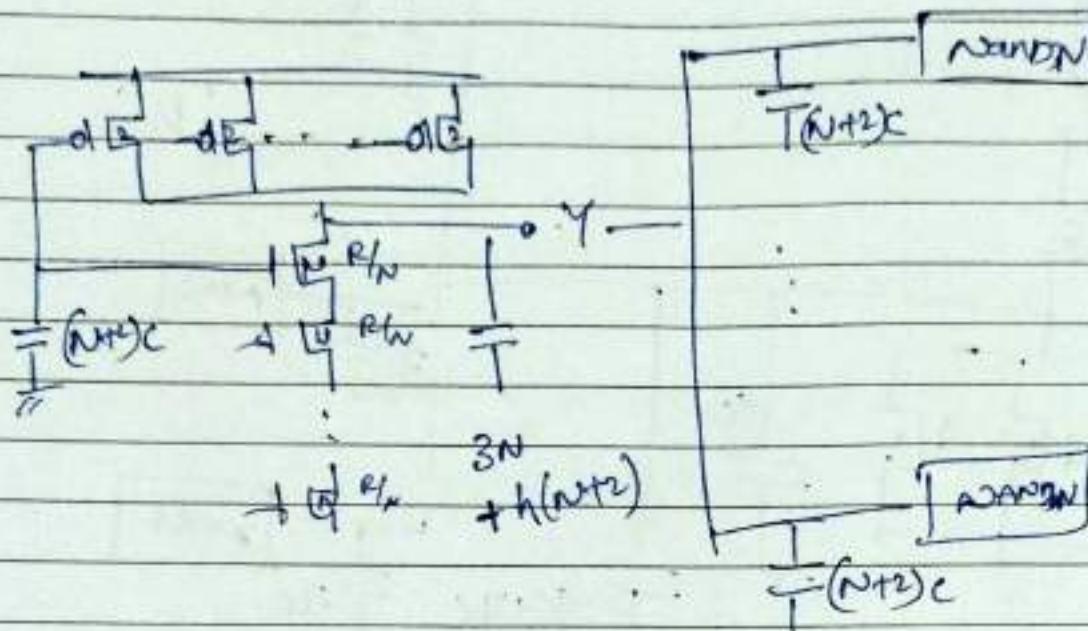
$$t_{PD}\text{P} = (9C + 7hC)R$$

$$T_{PD}\text{P, normalized} = \frac{(9C + 7hC)R}{3CR} = 3 + \frac{7}{3}h$$

N NAND

~~t_{PD}~~ + SR_C

N input NAND gate



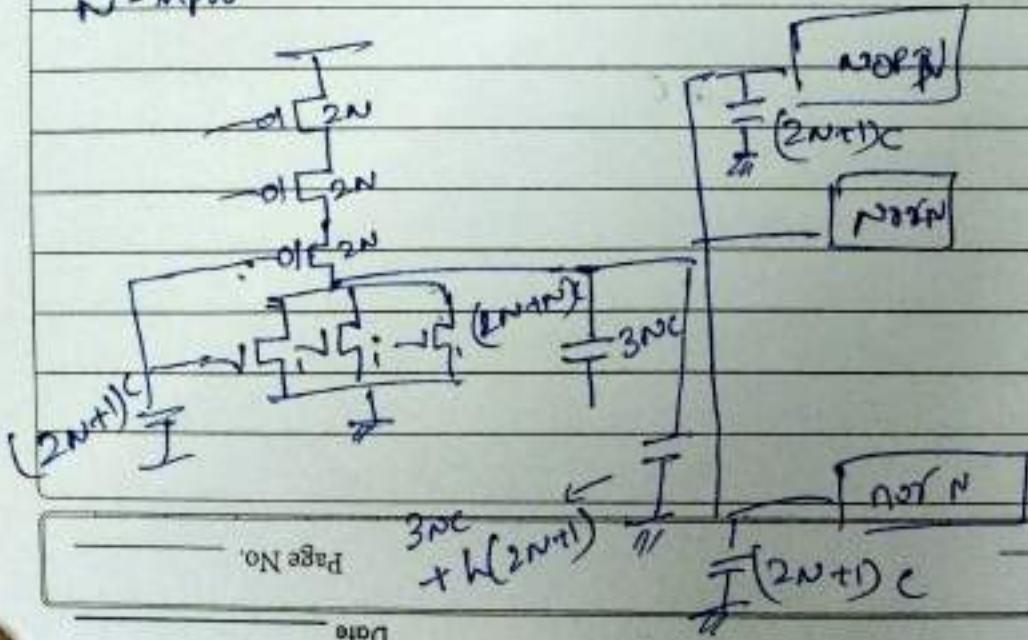
$$\therefore t_{PD} \text{ (ring } n \text{ identical NAND-N)} = \frac{(3N + h(N+2))}{3RC}$$

$$= N + \left(\frac{N+2}{3}\right)h$$

$$t_{PD}(\text{nand}) = 3 + \frac{5}{3}h$$

$$(\text{nor}) = 3 + \frac{7}{3}h$$

N-input



$$t_{PDF} = (3N + h(2N+1))CR$$

t_{PDF} normalized

$$= \frac{[3N + h(2N+1)]RC}{3RC}$$

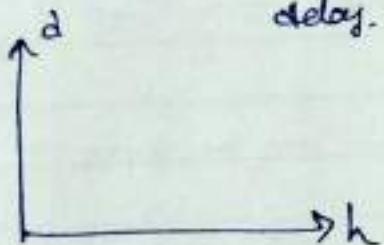
$$= N + \left(\frac{2N+1}{3}\right)h$$

$$t_{PDF(NAND-3)} = 3 + \frac{5}{3}h$$

$$t_{PDF}(NOR-3) = 3 + \frac{7}{3}h$$

↑
parasitic delay.

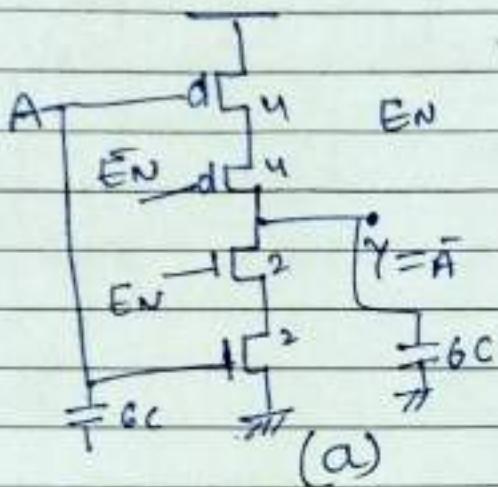
↗ electrical effort
 ↘ logical effort



$$(t_{PDF})d = p + gh$$

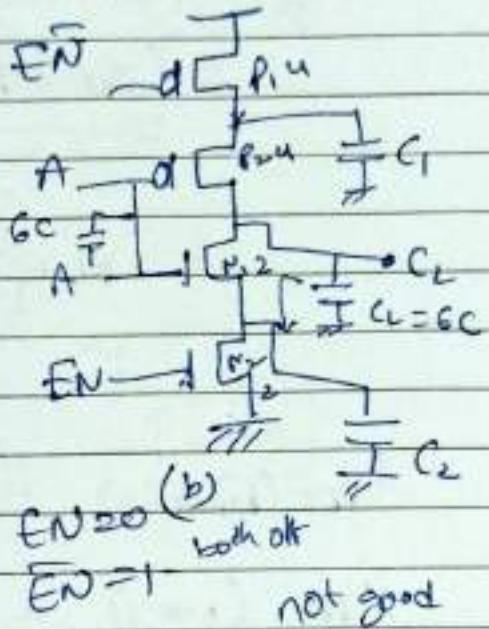
$$\overbrace{T}^d = p \quad \text{when } h=0 \quad \text{for no driving}$$

logical effort = $\frac{\text{I/P gate cap of subsequent stage}}{\text{I/P gate cap of standard CMOS inverter with identical drive strength}}$

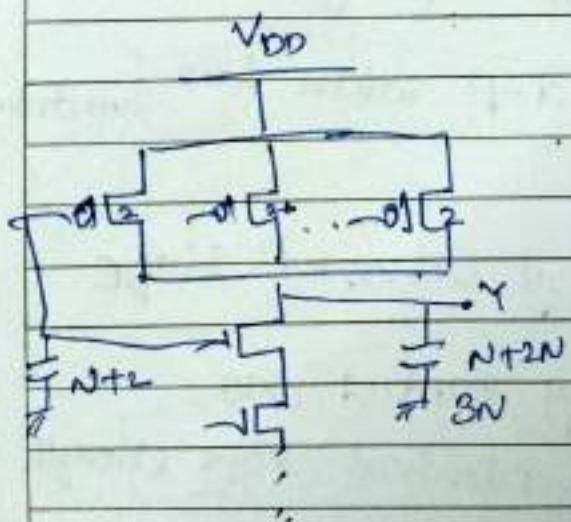
Tristate inverter

$$g_A = \frac{G_C}{3C} = 2.$$

$$p = \frac{G_C}{3C} = 2$$



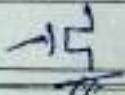
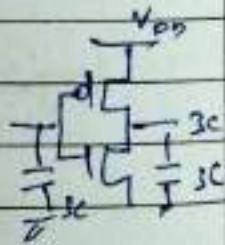
$Y=1$,
 $A=0 \rightarrow 1 \rightarrow$ change change
with C_2

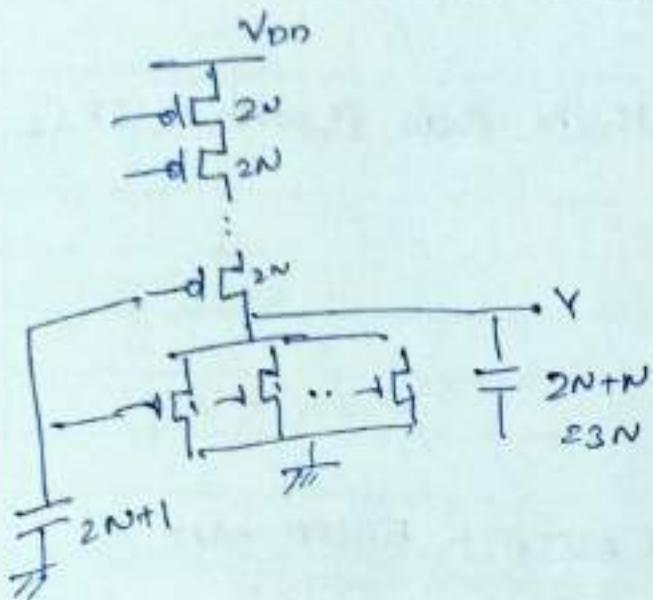


$$d = p + gh$$

$$= N + \frac{N+2}{3} h$$

$$\frac{3Nc}{2C} \quad \frac{(N+2)c}{2C}$$





$$d = N + \frac{2N+1}{3}$$

\uparrow
 $\frac{3NC}{3c}$
 $(.2N+1)3c$

h = External load cap
Input capacitance

g = Input cap of the logic gate (DUT)

Input cap of an inverter that can
drive the same o/p cascode

→ same drive strength

p = o/p diff cap of logic gate (DUT)
o/p diff cap of CMOS inv

$E_{N\otimes O} = 0, E_{N\otimes I} = 1 \Rightarrow$ PMOS, NMOS: off

Then, any change in A should not affect Y.

Case b: assume C_2 is completely discharged & $Y=1$.

$A=0 \rightarrow 1 \Rightarrow N_1$ is ON $\Rightarrow C_L$ shares charge with C_2

$$Y=1 (V_{DD}-\Delta V)$$

Case a) C₂ never gets a path to share C₁ with C₁ or C₂.

$$P = \frac{6C}{3C} = 2$$

$$g_A = \frac{6C}{3C} = 2$$

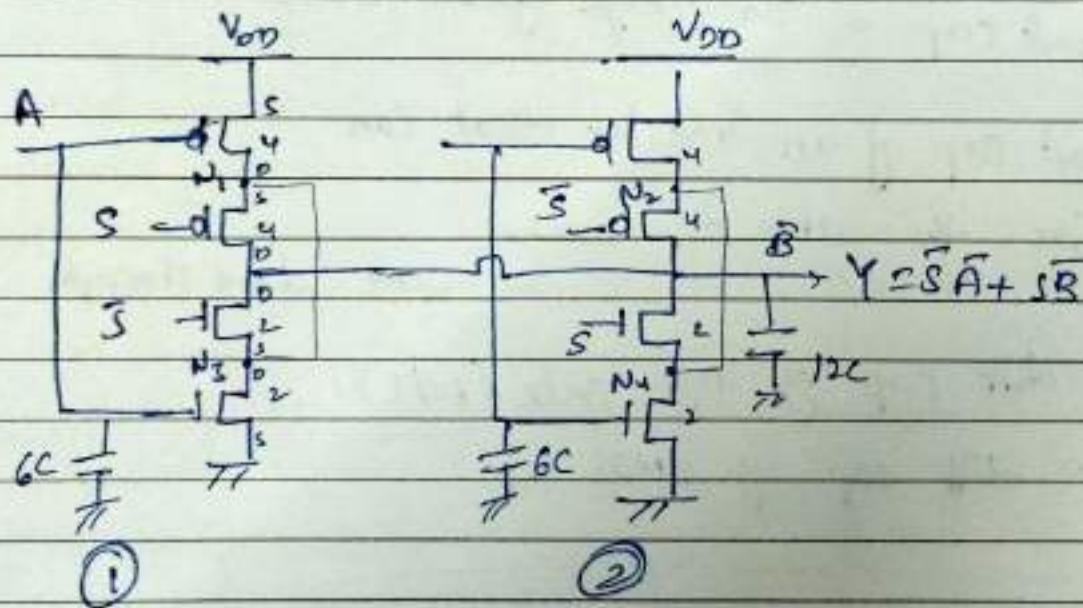
MUXES 2:1 mux

TRISTATE BASED MUX

$$Y = \bar{S}\bar{A} + S\bar{B}$$

$$= A ; S=0 \leftarrow \textcircled{1}$$

$$B \quad S=1 \leftarrow \textcircled{2}$$



$$(\text{logical effort}) (LE)_B = (LE)_A = \frac{6C}{3C} = 2$$

$$P = \frac{12C}{3C} = 4$$

4:1 MUX

$$Y = \bar{S}_1 \bar{S}_0 \bar{A} + \bar{S}_1 S_0 B + S_1 \bar{S}_0 C + S_1 S_0 D$$

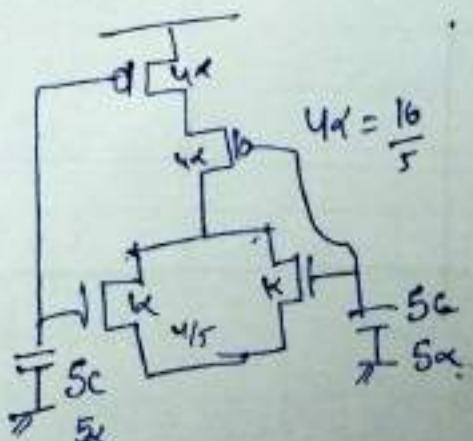
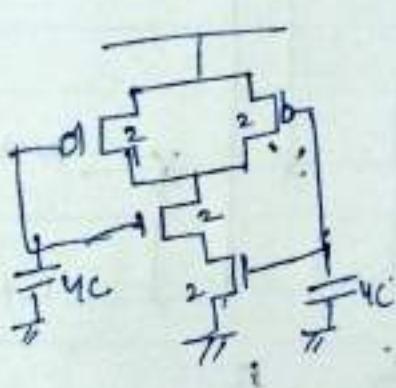
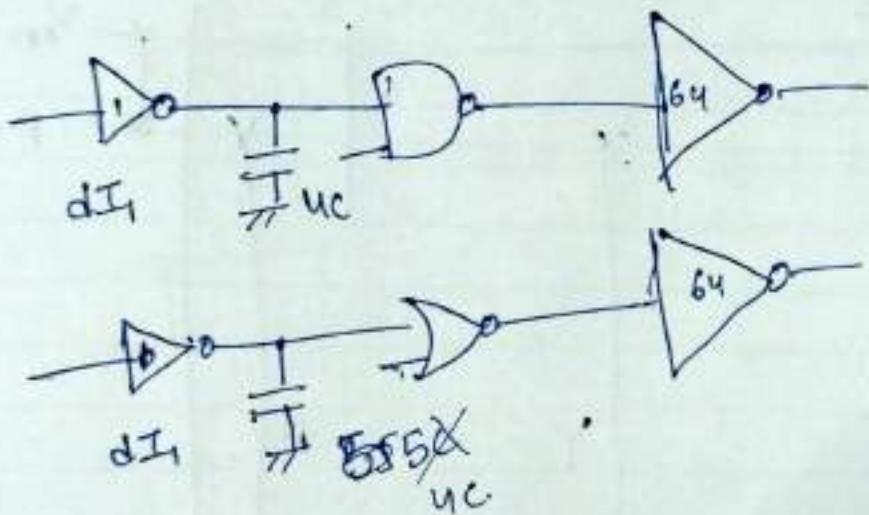
↓
separately generated

4 i/p 4 branch

$$(I_E)_A = (I_E)_B = (I_E)_C = (I_E)_D = 2$$

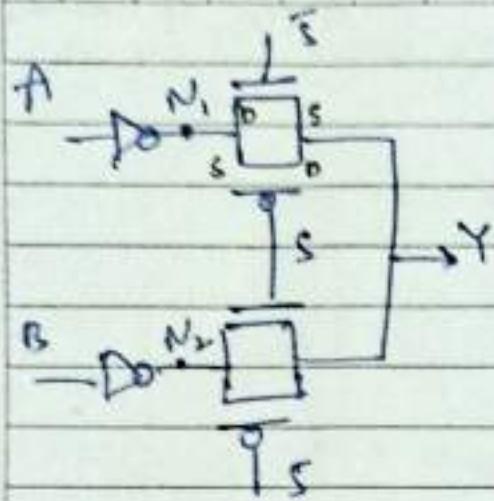
$$P = \frac{(G_C)N}{3C} = 2N$$

→ N-i/p-



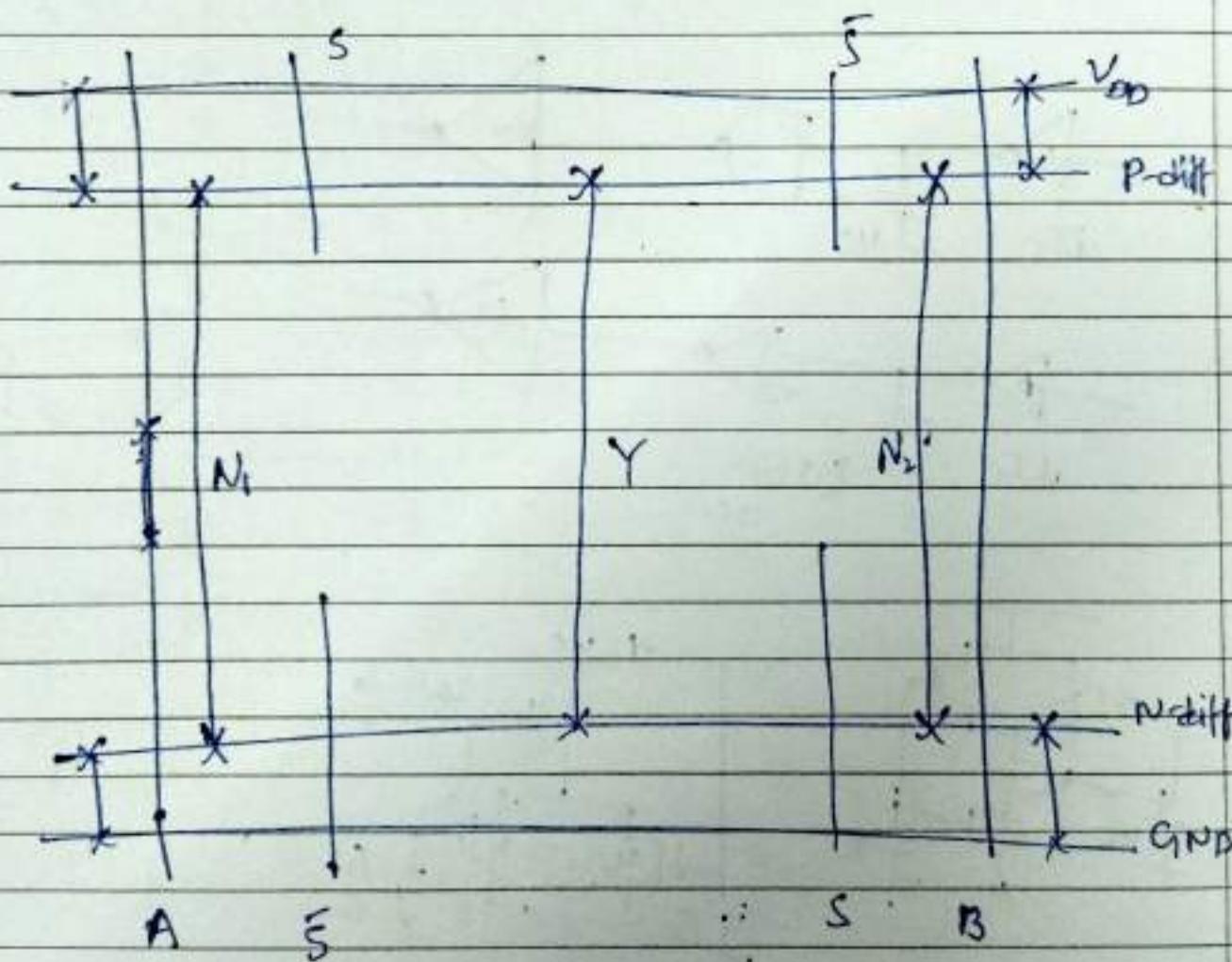
$$5\alpha = 4$$

$$\alpha = \frac{4}{5}$$

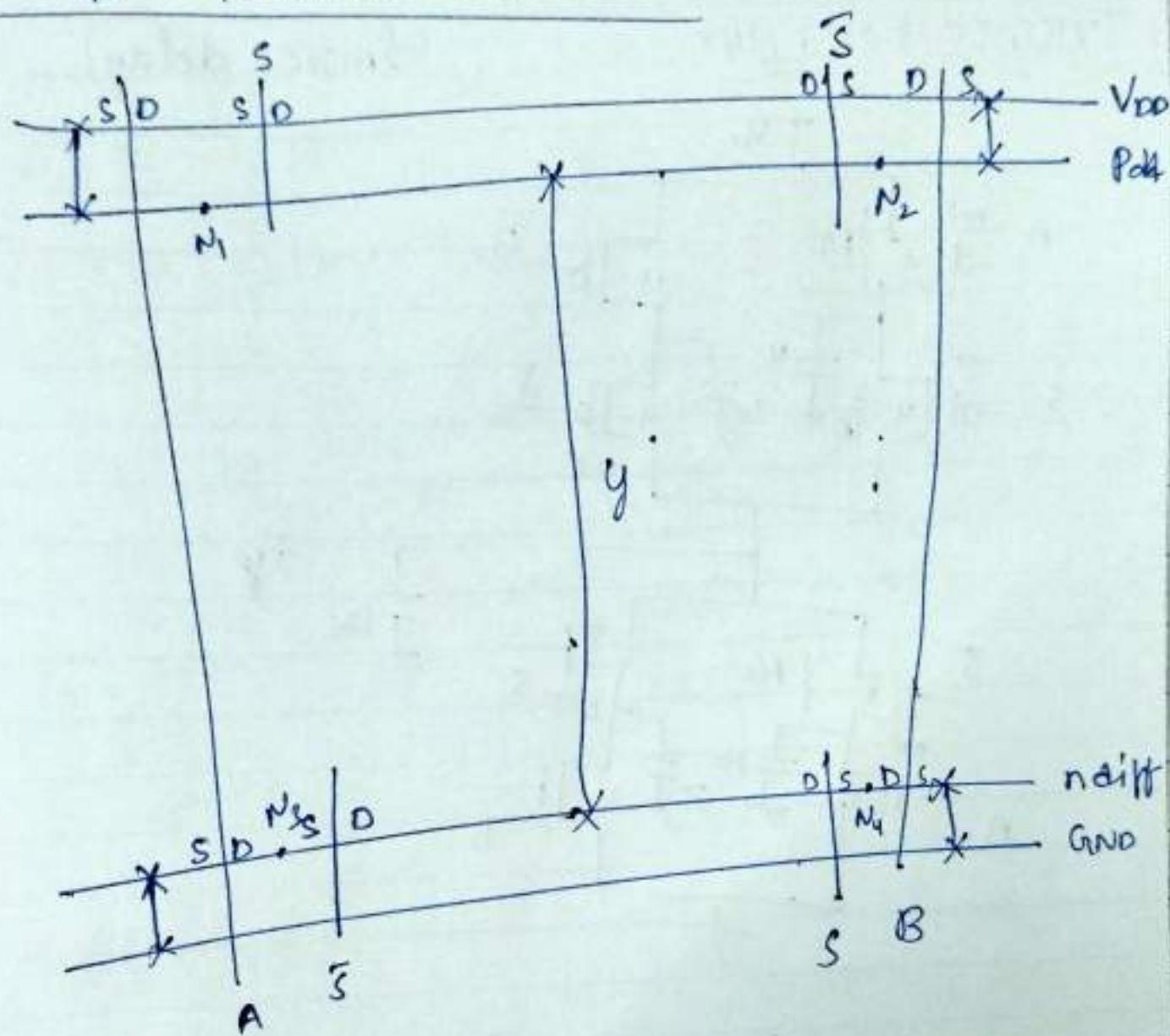


CMOS T-gated MUX

Fab for CMOS T-gated mux.

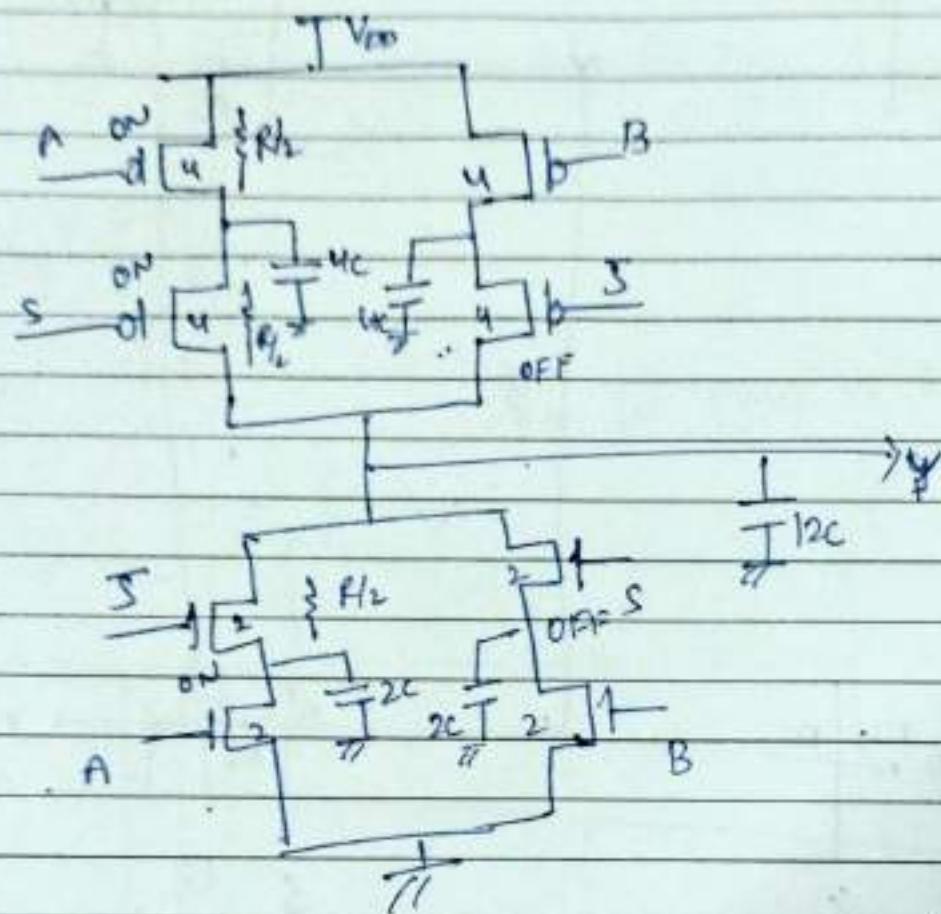


fabctn for TRISTATE based MUX



TRISTATE based NUX

(Elmore delay)

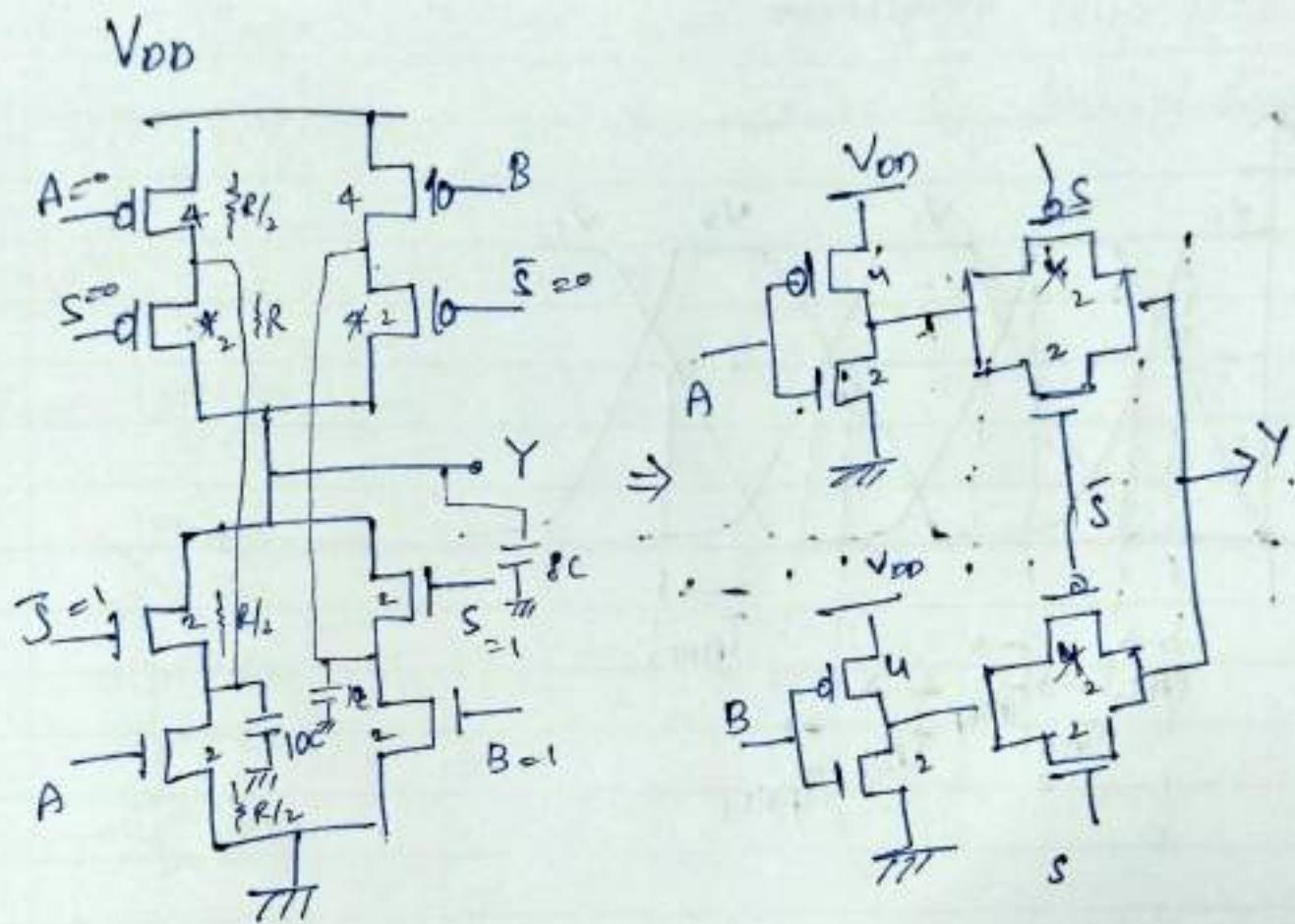


$$\tau_{POP} = 4C\left(\frac{R}{2}\right) + 12C\left(\frac{R}{2} + \frac{R}{2}\right) + 2C\left(\frac{R}{2} + \frac{R}{2}\right)$$

$$= 16RC$$

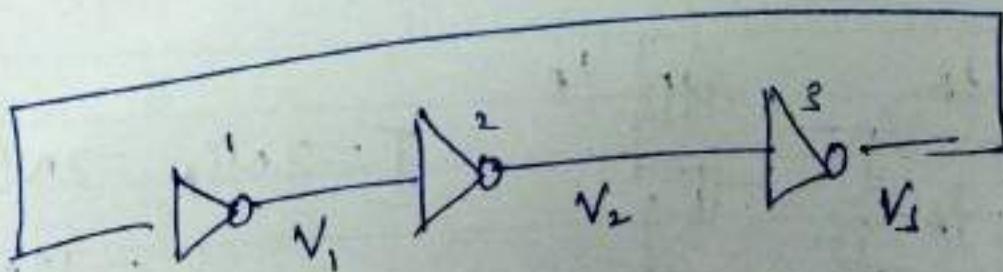
$$\tau_{POP} = 4C\left(\frac{R}{2} + \frac{R}{2}\right) + 12\left(\frac{R}{2} + \frac{R}{2}\right) + 2C\left(\frac{R}{2}\right)$$

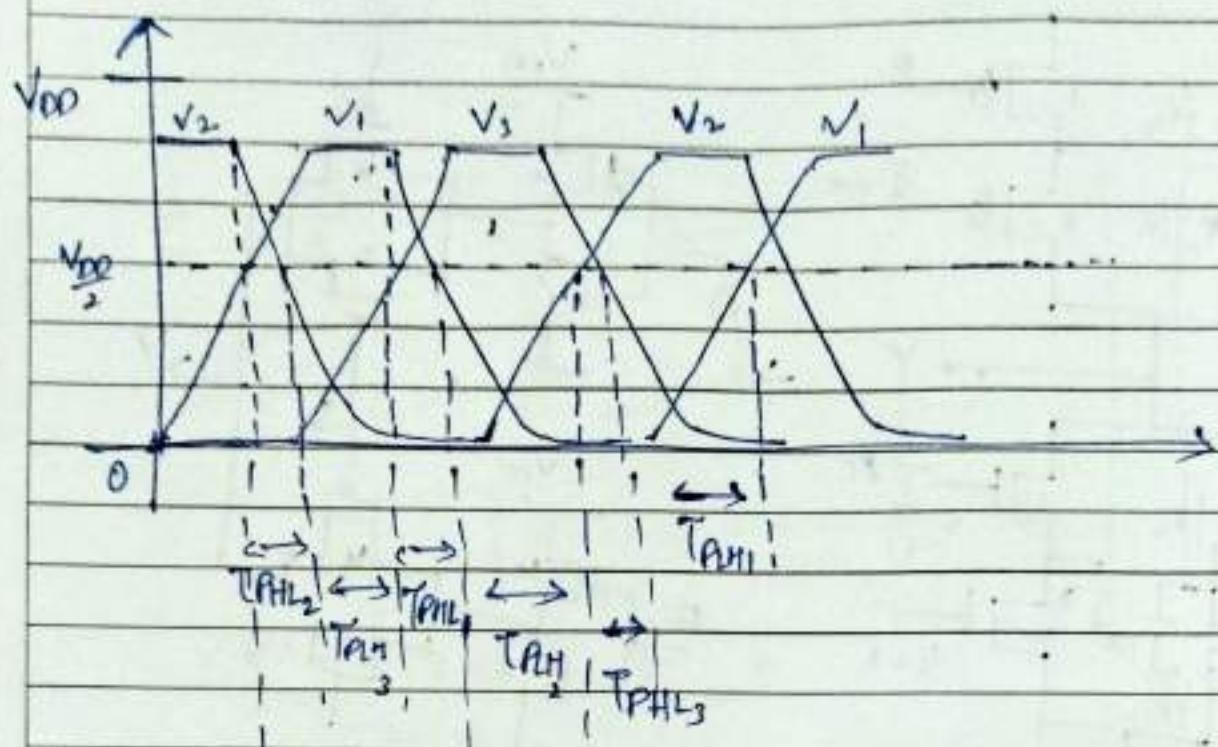
$$S=1 \\ T_3=1 \\ = 17RC.$$



$$\tau_{PDR} = 10C(R_L) + 8C\left(\frac{R}{2} + \left(R \parallel \frac{R}{2}\right)\right) \Rightarrow 8C\left(\frac{5R}{6}\right) + 5RC = 11.67RC$$

$$\tau_{PDP} = 11.67RC$$





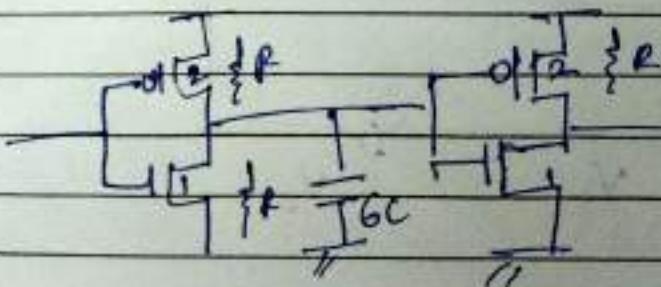
$$T = T_{PHL_2} + T_{PHL_3} + T_{PHL_1} + T_{AHL_3} + T_{PHL_2} + T_{AHL_1}$$

$$= T_p + T_p + T_p + T_p + T_p + T_p$$

$$\approx 6T$$

$$= 2N T_p$$

$$N = \# \text{ no of Inverters (odd)} \\ = 2k + 1$$



$$T = 2N T_p = 2N(6RC)$$

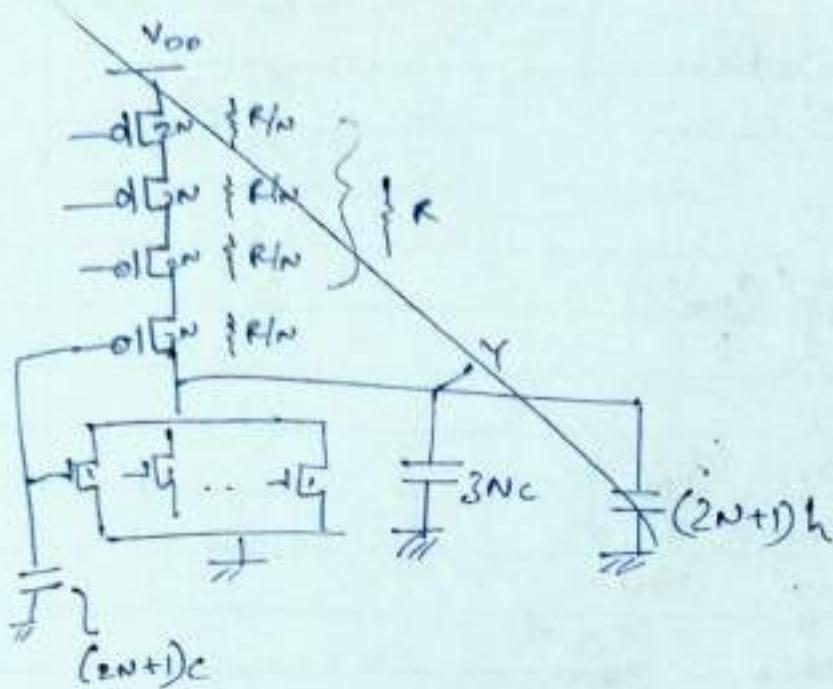
$$= 12NRC$$

$$f = \frac{1}{12NRC}$$

- Ring oscillator can be used to heat chip maliciously
- RD frequencies can be used as signature of chip.

19/09/24 (western Harris)

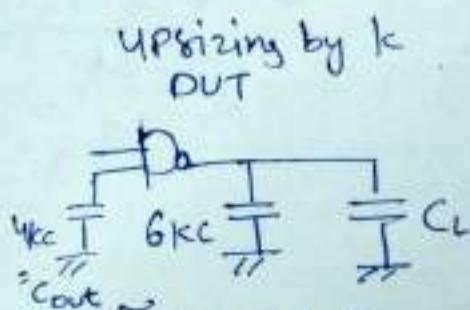
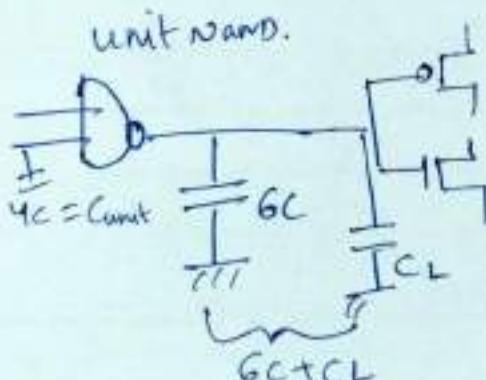
Recap: LINEAR DELAY MODEL



$$\frac{N\text{-input NOR}}{N} \quad p = \frac{2Nt}{3}$$

$$\frac{N\text{-input NAND}}{N} \quad g = \frac{N+2}{3}$$

$$d = p + gh \quad \text{inverter}$$



$$\begin{aligned} T_{PDR} &= \frac{R}{k} (6kC + CL) \\ &= 6RC + \frac{R}{k} C_L^2 \end{aligned}$$

load delay term.
parallel delay term. → independent of drive strength

$$T_{PDR} = R(GC + CL) = T_{PDP}$$

$$\frac{C_{out}}{C_{unit}} = \frac{4kC}{4C} = k$$

$$\therefore \text{delay} = NRC + \frac{R}{\frac{C_{out}}{C_{unit}}} C_L$$

↓
constant

Normalized delay

$$= NRC + \frac{C_{unit} R C_L}{C_{out}}$$

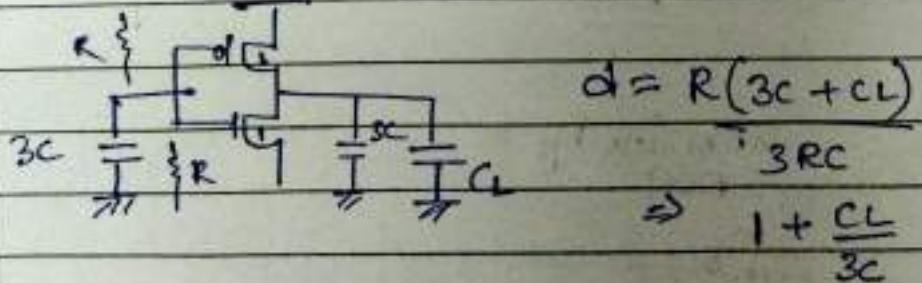
↓
3RC

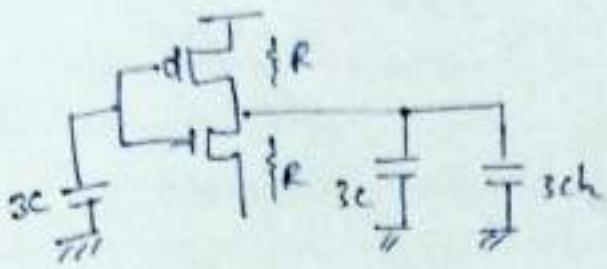
$$\Rightarrow \frac{N}{3} + \left(\frac{C_L}{C_{out}} \right) \left(\frac{C_{unit}}{3C} \right)$$

$$\Rightarrow \tau = \frac{N}{3} + \left(\frac{C_L}{C_{out}} \right) \left(\frac{C_{unit}}{3C} \right)$$

↑
constant ↓
parasitic Electrical logical
delay (P) effort. (E) effort (g).

$$d = P + gh \rightarrow \text{linear delay model.}$$





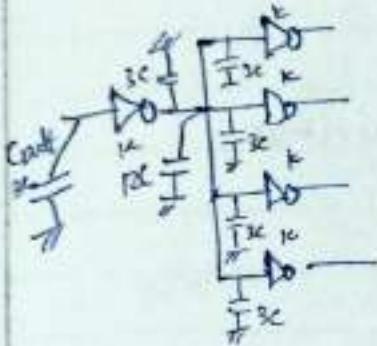
$$d = R \left[3c + 3ch \right] / 3Rc$$

$$d = p + gh$$

p g

Example problems

FD4 delay



$$h = \frac{C_L}{C_{out}} = \frac{12c}{3c} = 4 \quad \text{after scaling} = \frac{12c}{3cc} = 4$$

$$g = \frac{C_{unit}}{3c} = \frac{3c}{3c} = 1 \quad \frac{3c}{3c} = 1$$

$$p = \frac{3Rc}{3Rc} = 1, \quad d = p + gh$$

p g

$$= 1 + 4 \times 1 = 5$$

FD4 delay

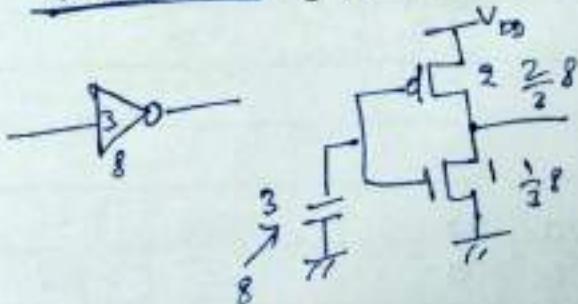
$$d = 5c \quad \text{if uniformly scaled then}$$

$$= \frac{5c}{c} \cdot (3Rc)$$

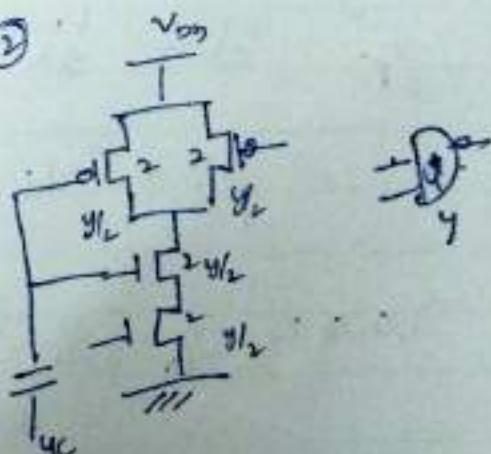
$$d_{scaled} = 5c.$$

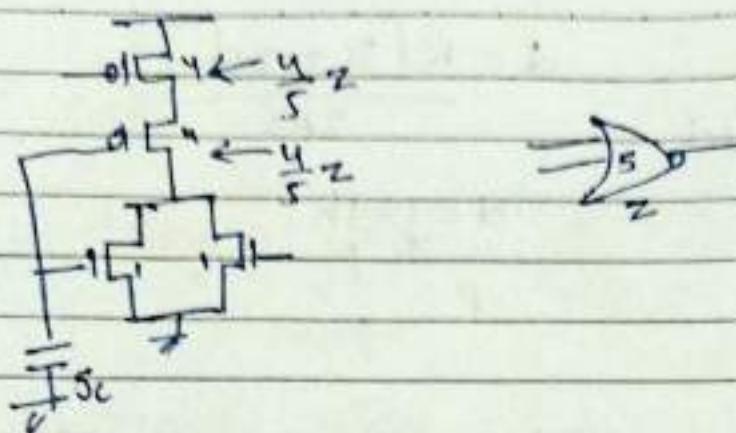
gate sizes (inside gate)

①



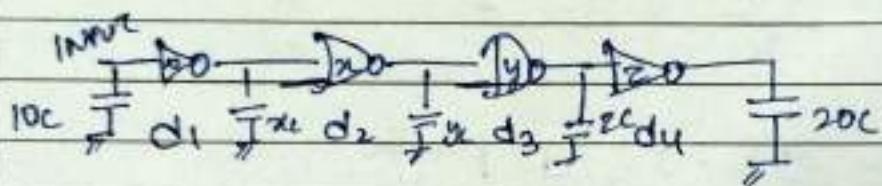
②





Delay in Multi-stage network

i) find x, y and z s.t overall delay for the Ckt is minimum.



$$\text{Overall delay} = d_1 + d_2 + d_3 + d_4$$

$$\Rightarrow (P_1 + g_1 h_1) + (P_2 + g_2 h_2) + (P_3 + g_3 h_3) + (P_4 + g_4 h_4)$$

$$\Rightarrow \left(1 + \frac{1}{10}x\right) + \left(2 + \frac{5}{3}y\right) + \left(2 + \frac{4}{3}z\right) + \left(1 + \frac{1}{2}20\right)$$

$$(h = \frac{C_L}{C_{out}}) \Rightarrow 6 + \frac{x}{10} + \frac{5}{3}y + \frac{4}{3}z + \frac{20}{2}$$

$\sum_i P_i$ $a_1 h_1 = a_1$ $a_2 h_2 = a_2$ $a_3 h_3 = a_3$ $a_4 h_4 = a_4$

$$\Rightarrow \sum_i P_i + \sum_i g_i h_i$$

$$a_1 a_2 a_3 a_4 = \frac{1}{10} \cdot \frac{5}{3} \cdot \frac{4}{3} \cdot \frac{20}{2} = \frac{40}{9}$$

4

$$abcd = 16$$

$$(a+b+c+d)_{\min} = 9$$

$$1 \times 1 \times 1 \times 16$$

$$19$$

$$1 \times 1 \times 8 \times 2$$

$$\text{only } 16$$

$$12$$

$$2 \times 2 \times 2 \times 2$$

$$\left\{ \begin{array}{l} a=b=c=d \\ (16)^{\frac{1}{4}}=2 \end{array} \right.$$

$$8$$

$$(16)^{\frac{1}{n}} = 2$$

$$\therefore a_i = \left(\frac{40}{9} \right)^{\frac{1}{n}} = 1.4519$$

$n = \# \text{ stages}$

minimum delay

$$= 6 + N(f)^{\frac{1}{N^{\text{stages}}}} \Rightarrow 6 + 4 \times 1.4519$$

$$= 11.81.$$

$$\text{when } \Rightarrow \sum_i p_i + \sum_i g_i h_i$$

$g_i = \text{stage effort} = f_i$

$$\therefore [\text{Actual delay} = 11.81 \times 3RC]$$

$$P = \prod_{i=1}^N g_i h_i$$

Path stage effort.

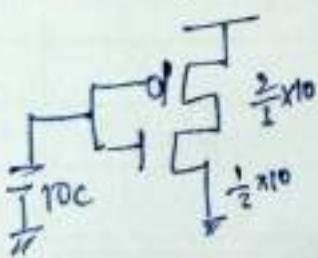
$$g_1 h_1 = \frac{20}{2} = 1.4519 = \boxed{13.47 = z} \quad z$$

$$g_2 h_2 = \frac{4}{2} \frac{13.47}{y} = 1.4519 = \boxed{12.65 = y}$$

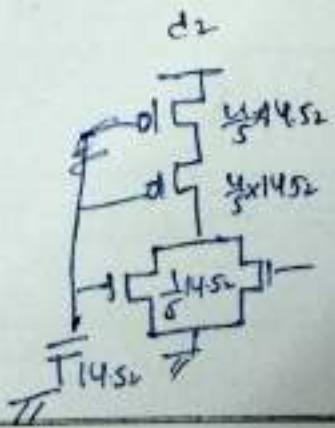
$$g_3 h_3 = \frac{5}{3} \frac{y}{x} = 1.4519 = \boxed{x = 14.52}$$

sizes

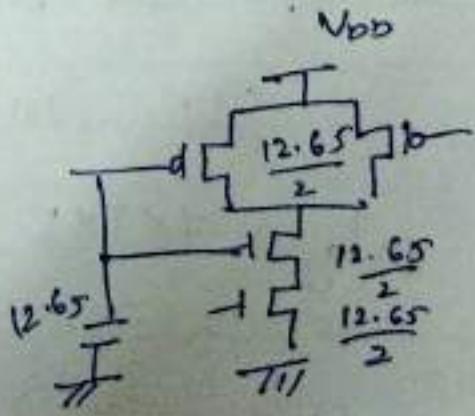
d_1

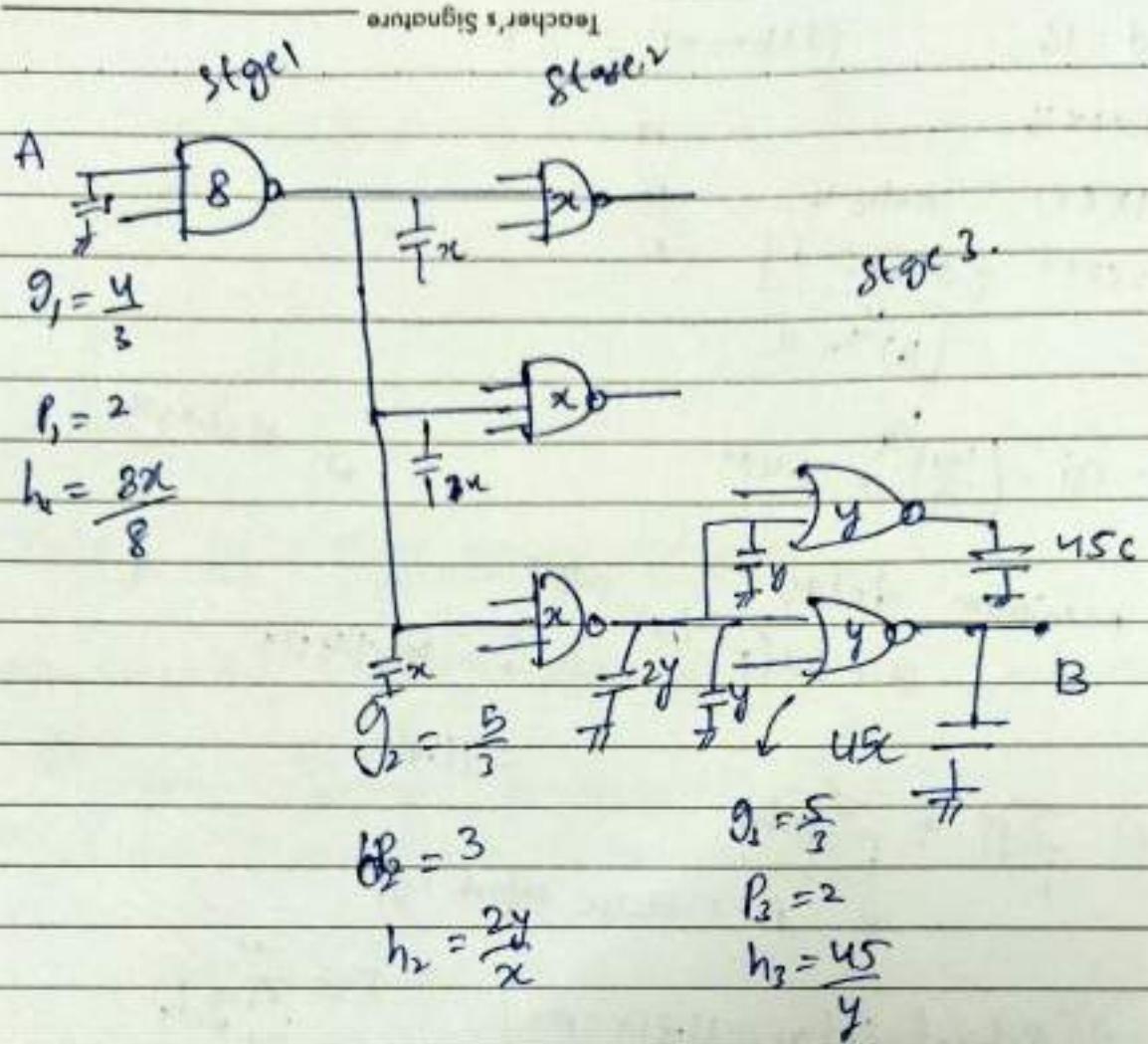


d_2



V_{DD}





$$\text{Delay} = P_1 + g_1 h_1 + P_2 + g_2 h_2 + P_3 + g_3 h_3$$

$$= 7 + \left(\frac{4}{3} \cdot \frac{3x}{8} \right) + \left(\frac{5}{3} \cdot \frac{2y}{x} \right) + \left(\frac{5}{2} \cdot \frac{45}{y} \right)$$

$$\sum g_i h_i = 125$$

min if $g_1 h_1 = g_2 h_2 = g_3 h_3 \Rightarrow \text{delay is min}$

$$g_i h_i = (125)^{1/3} = 5$$

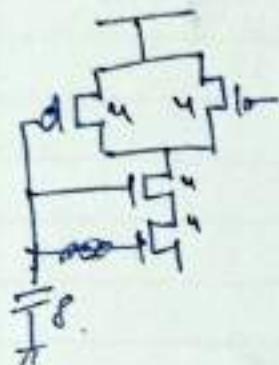
$$\text{Delay} = 7 + 3 \times 5 = 22 \text{ ns}$$

$$\frac{5}{3} \cdot \frac{45}{y} = 5$$

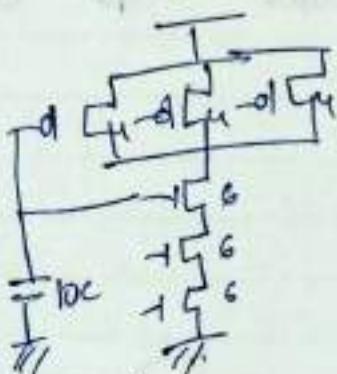
$$Ty = 15$$

$$n=10$$

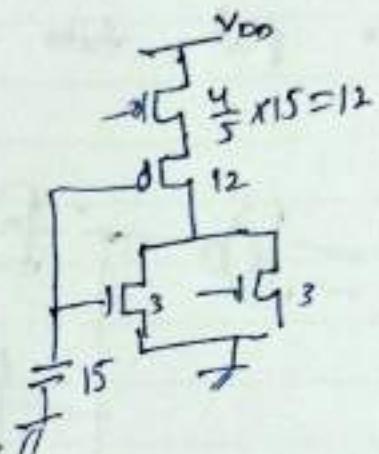
\therefore stage 1



stage 2



stage 3



$$d_1 = P_1 + g_1 h_1 \\ = 2 + 5 \\ = 7$$

$$d_2 = P_2 + g_2 h_2 \\ = 3 + 5 \\ = 8$$

$$d_3 = P_3 + g_3 h_3 \\ = 2 + 5 \\ = 7.$$

$$d_1 + d_2 + d_3 = 7 + 8 + 7 = 22.$$

if $45000c$

$$F = \sum_{i=1}^N g_i h_i = \left(\frac{4}{3} \times \frac{3x}{8}\right) \left(\frac{5}{3} \times \frac{2y}{x}\right) \left(\frac{5}{3} \times \frac{45000}{y}\right) = 125000$$

$$f_i = (F)^{1/3} = 50$$

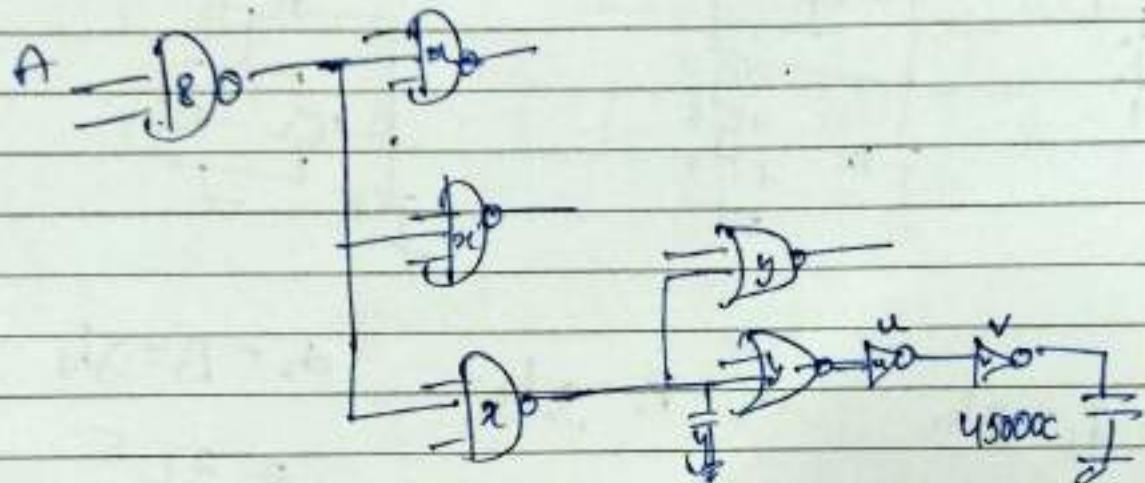
$$\text{Delay} = \sum P_i + N(F)^{1/N}$$

$$= 7 + 3 \times 50 = 157.$$

$$\underset{\text{minimize}}{\uparrow} P_i = \underset{\text{CONSTANT}}{\downarrow} \sum N(F)^{1/N}$$

$N \uparrow \quad N(F)^{1/N} \downarrow$

so put two inverter before load capacitor.



$$N = 3 \rightarrow 5$$

$$f = \frac{5}{\pi R_1 h_i}$$

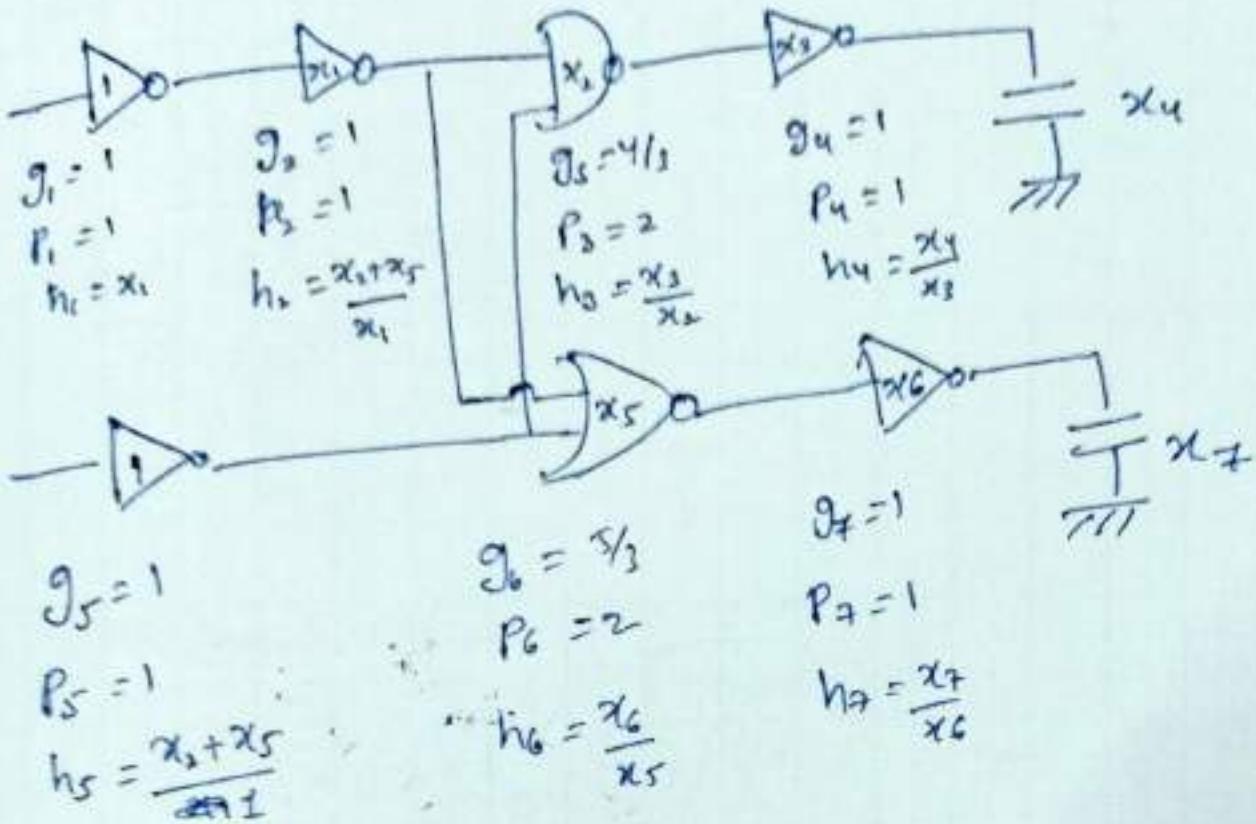
$$= \left(\frac{1}{2} \times \frac{2x}{2} \right) \left(\frac{5}{3} \frac{2y}{x} \right) \left(\frac{5u}{3y} \right) \left(1 \cdot v \right) \left(1 \cdot \frac{45000}{v} \right)$$

$$= 125000.$$

$$\delta_i = (F)^{1/5} = 10.4564 = 1$$

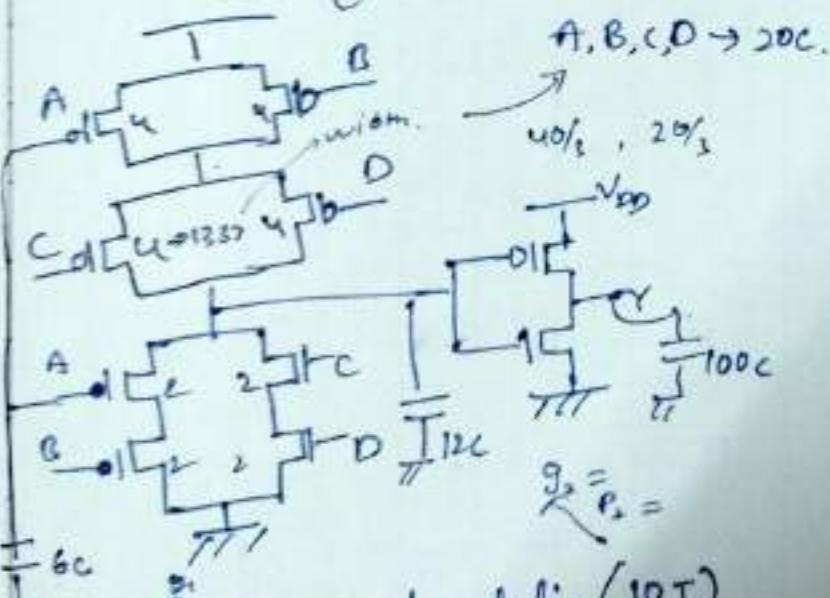
$$\begin{aligned} \text{delay} &= \sum P_i + N(F)^{1/N} \\ &= 9 + 5 \cdot 10.4564 = 61.282. \end{aligned}$$

15/0ct/24



$$Y = AB + CD$$

case I



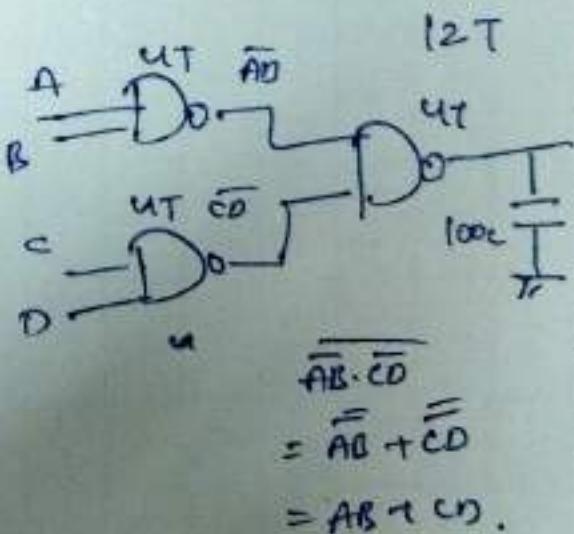
less area

add up the width all.

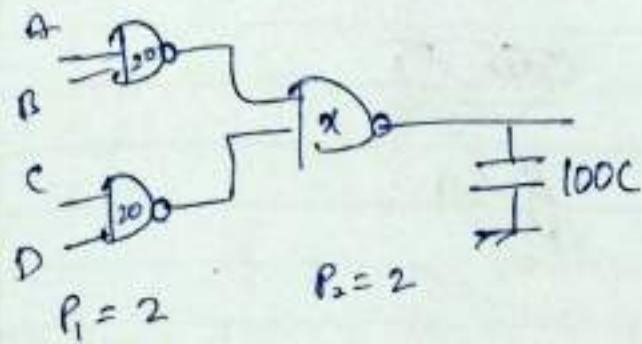
more area

case II 2-ip NANDgate

$$Y = AB + CD$$



Can II



$$g_1 = \frac{4}{3} \quad g_2 = \frac{4}{3}$$

$$F = GM = g_1 g_2 h_1 h_2 = f_1 f_2 = \frac{4}{3} \cdot \frac{x}{20} \cdot \frac{4}{3} \cdot \frac{100}{x} = \frac{80}{9}$$

$$D_{\min} = P_1 + g_1 h_1 + P_2 + g_2 h_2 \Rightarrow P_1 + f_1 + P_2 + f_2 \Rightarrow P_1 + P_2 + (f_1 + f_2)_{\min}$$

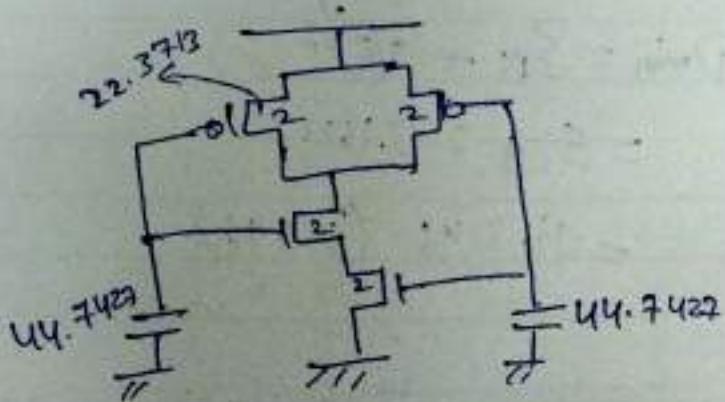
$$\Rightarrow 4 + (f_1 + f_2)_{\min} \Rightarrow 4 + (2.98 \times 2) = 9.96$$

$$\text{now. } (f_1 + f_2)_{\min} = ?$$

$$f_1 = f_2 = f \Rightarrow f^2 = \frac{80}{9} = \sqrt{\frac{80}{9}} = 2.98$$

$$f_2 = \frac{4}{3} \cdot \frac{100}{x} = 2.98$$

$$\Rightarrow \boxed{x = 44.7427}$$

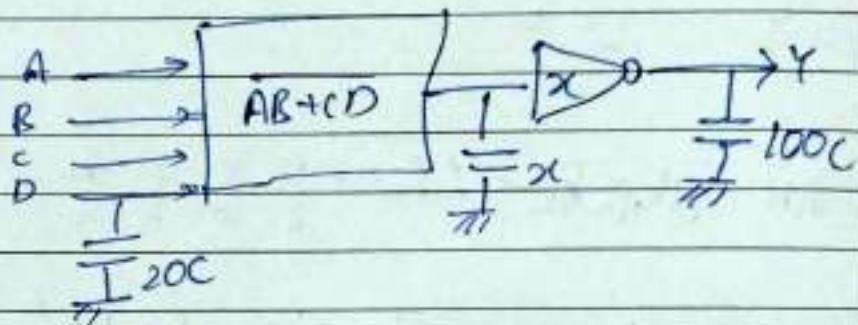


Calc ICalc II

$$g_1 = \frac{6c}{3c} = 2$$

~~g1~~

$$P_1 = \frac{12c}{3c} = 4$$



$$g_2 = 1, P_2 = 1$$

$$F = GH$$

$$= g_1 h_1 g_2 h_2$$

$$= g_1 g_2 h_1 h_2$$

$$= 2 \times 1 \times \frac{100}{20}$$

$$f = (F)^{\frac{1}{2}}$$

$$= \sqrt{10}$$

$$= 3.162$$

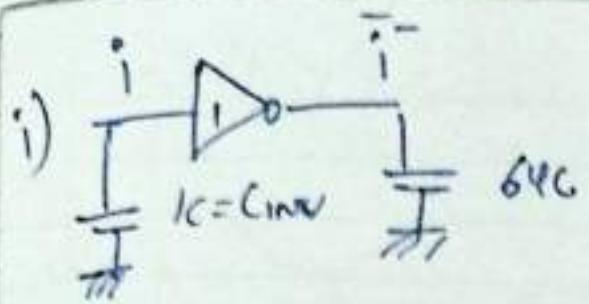
$$D_{min} = \sum P_i + 2(F)^{\frac{1}{2}}$$

$$= 5 + 2 \times 3.162$$

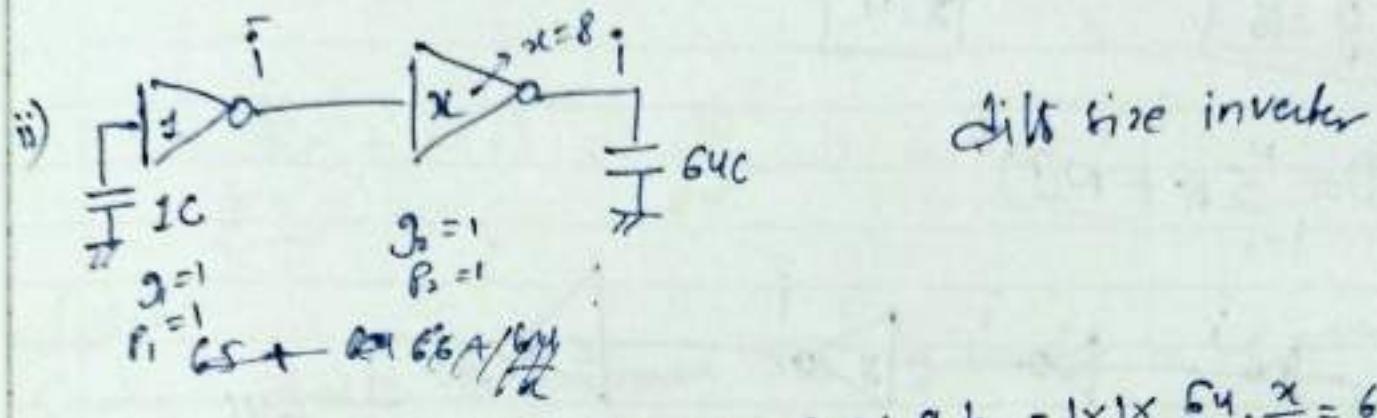
$$= 11.3246 (> 9.96)$$

$$\frac{1.100}{x} = 3.1623$$

$$x = 31.6225$$



$$d_1 = P_1 + g_1 h_1 = 1 + 1 \times \frac{64}{1} = 65.$$



$$d_1 = P_1 + g_1 h_1$$

$$F = GH = g_1 h_1 g_2 h_2 = 1 \times 1 \times \frac{64}{x} \cdot \frac{x}{1} = 64$$

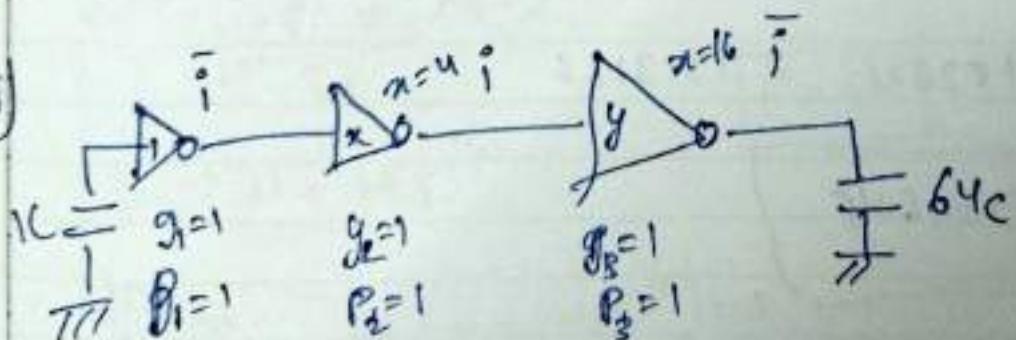
$$f = (64)^{1/2} = 8$$

$$d_1 = 1 + 1.$$

$$d_{\min} = \sum P_i + N(F)^{1/N}$$

$$= 2 + 2 \cdot (8) = 18$$

$$\frac{2L}{1} = 8 \quad \boxed{x=8}$$



$$F = GH = g_1 g_2 g_3 h_1 h_2 h_3$$

$$= 64$$

$$D_{\min} = \sum P_i + 3 \times 4$$

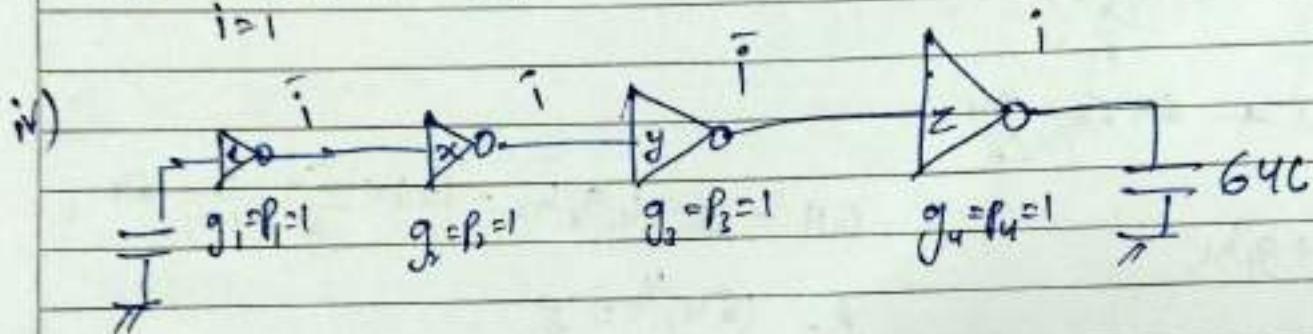
$$= 5 + 12 = 15.$$

$$\frac{64}{4} \cdot 1 = 4 \quad \frac{4}{x} = 4$$

$$\boxed{y = 16}$$

$$\boxed{x=4}$$

$$D = \sum_{i=1}^n p_i + N(F)^{1/n}$$



$$F = GHI - 64$$

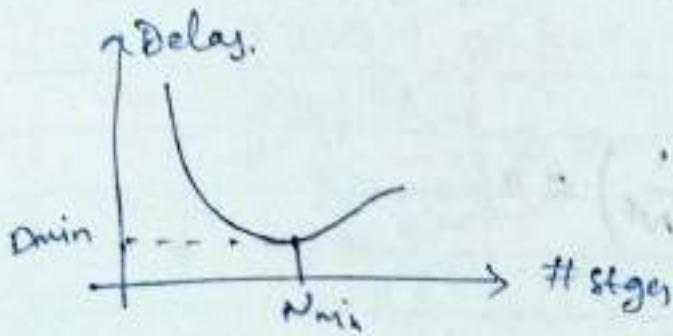
$$f_i = (64)^{1/4} = 2.8284$$

$$\text{delay} = \sum p_i + 4 \times 2.8284$$

$$= 4 + 4 \times 2.828 = 15.3136$$

v)

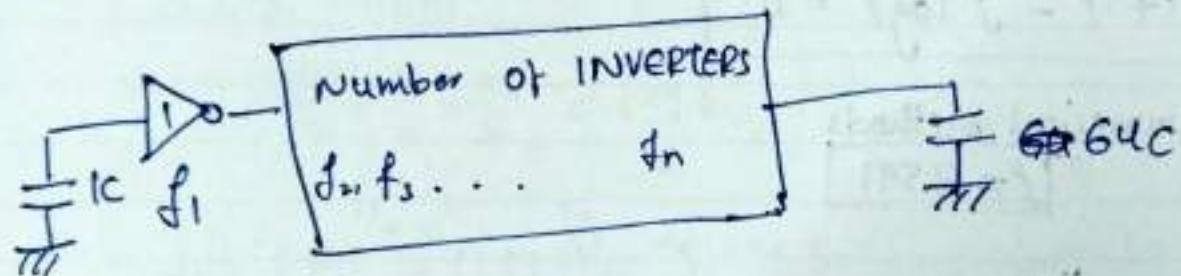
$\boxed{N=5} \quad D=16.48$



$$D = \sum_{i=1}^N p_i + N(F)^{\frac{1}{N}} \Rightarrow \frac{\partial D}{\partial N} = 0 \Rightarrow \boxed{N = ?}$$

Question

Question :- what is the minimum no : of inverter to be added
to get minimum delay for driving a certain load?



$$D = \sum_{i=1}^N p_i + N(F)^{\frac{1}{N}}$$

$$D \Rightarrow N + N(F)^{\frac{1}{N}}$$

$$\frac{\partial D}{\partial N} = 0 \quad \frac{\partial}{\partial N} \left(N + N(F)^{\frac{1}{N}} \right) = 0$$

$$= 1 + (F)^{\frac{1}{N}} + N \cdot \frac{\partial}{\partial N} F^{\frac{1}{N}} = 0$$

$$\frac{d}{dx} a^x = a^x \log a$$

$$\frac{d}{dx} a^{f(x)} = a^{f(x)} \log(a) f'(x)$$

$$\Rightarrow 1 + (F)^{1/N} + \cancel{\mu F^{1/N} \ln(F)} \left(-\frac{1}{N^2} \right) = 0$$

$$\cancel{F(F)^{1/N}} = F$$

$$\Rightarrow 1 + (F)^{1/N} - \frac{F^{1/N}}{N} \ln(F) = 0$$

$$\Rightarrow 1 + (F)^{1/N} - (F)^{1/N} \ln(F^{1/N}) = 0$$

$$\boxed{F^{1/N} = \rho}$$

$$\boxed{1 + \rho - \rho \log \rho = 0}$$

by numerical methods

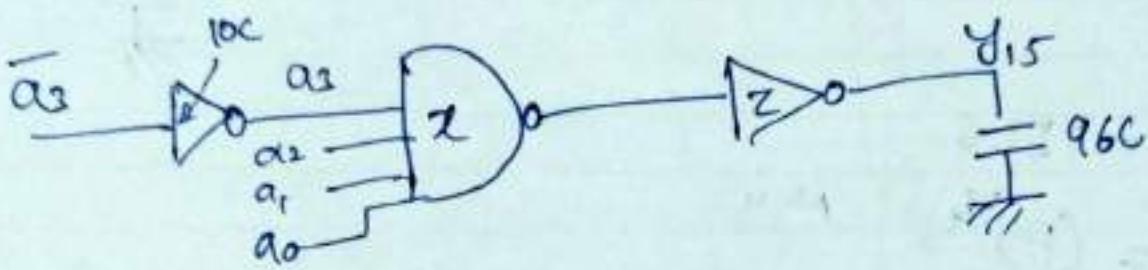
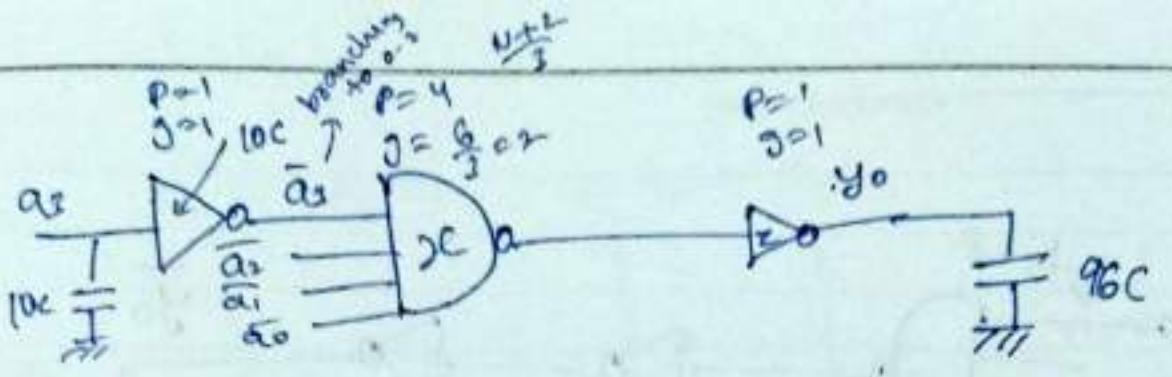
$$\boxed{\rho = 3.591}$$

$$\Rightarrow (F)^{1/N} = 3.591$$

$$\Rightarrow \cancel{\frac{1}{N} \ln F} = \ln 3.591$$

$$\Rightarrow \boxed{N = \frac{\ln F}{\ln 3.591}}$$

$$\therefore N = \frac{\ln 64}{\ln 3.591} = 3.25$$



$$F = GH$$

$$= g_1 g_2 g_3 h_1 h_2 h_3$$

$$= 2 \times \frac{8}{10} \times \frac{2}{x} \times \frac{96}{x} = 153.6$$

$$f_i = (F)^{1/3} = (153.6)^{1/3} = 5.3555$$

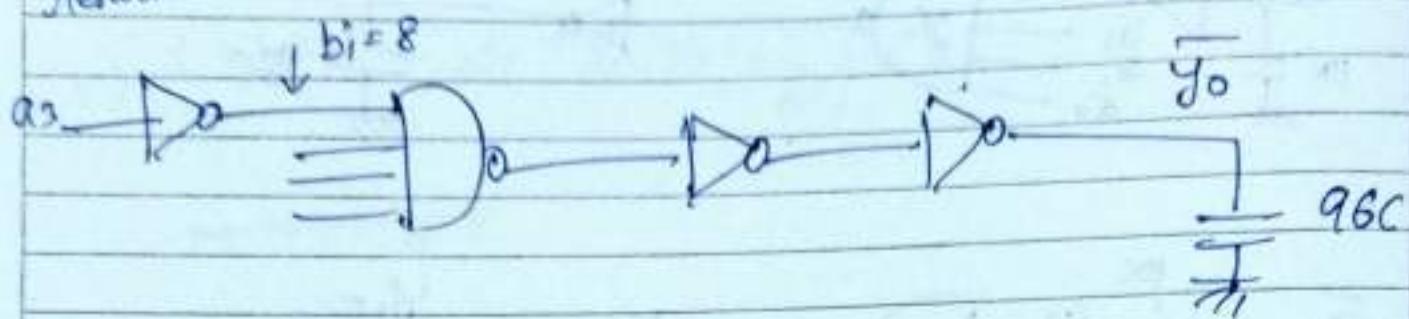
$$D = \sum p_i + \sum g_i h_i$$

$$= (1+u+1) + 3 \times 5.3555 = 22.0665$$

Now, for optimizing

$$N = \frac{\ln F}{\ln 3.591} = \frac{\ln 153.6}{\ln 3.591} = 3.95 \approx 4.$$

gewart



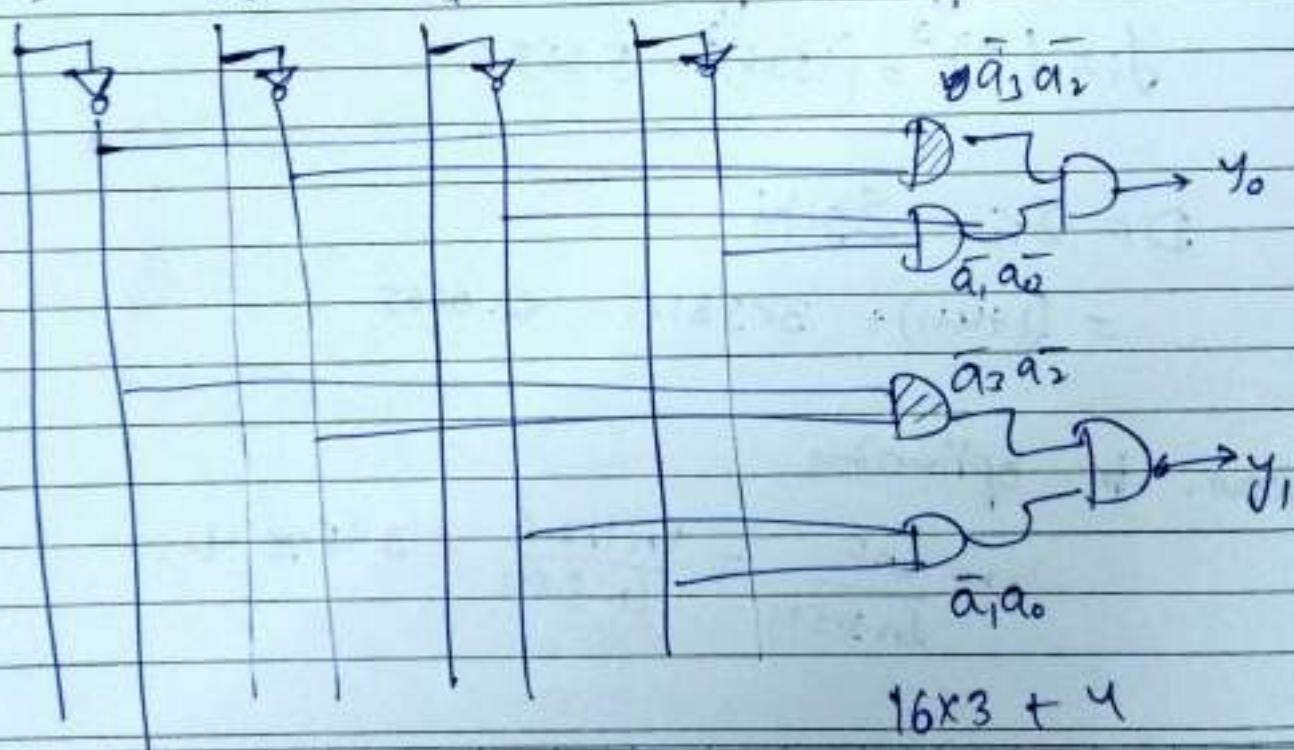
$$F = 153.6$$

$$\begin{aligned} f_i &= (F)^{\frac{1}{n}} \quad n=4 \\ &= (153.6)^{\frac{1}{4}} = 3.5204 \end{aligned}$$

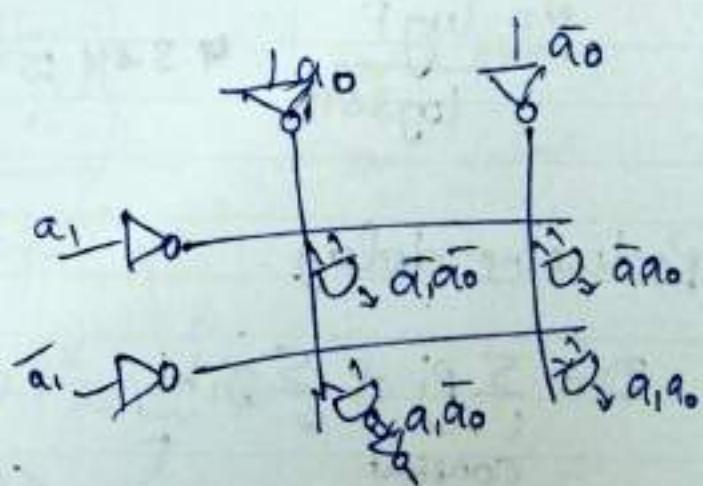
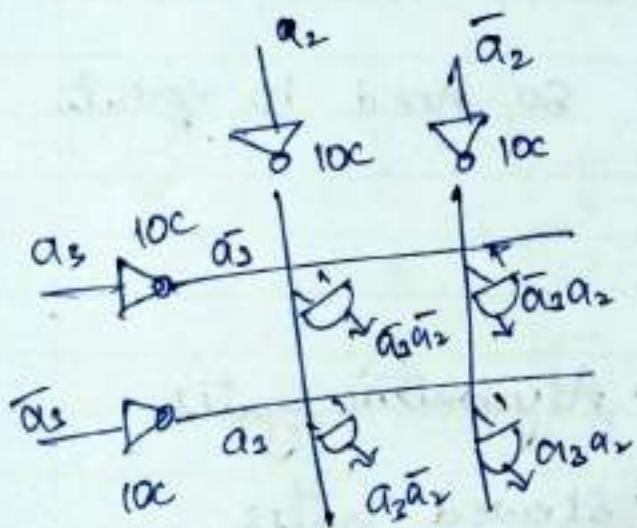
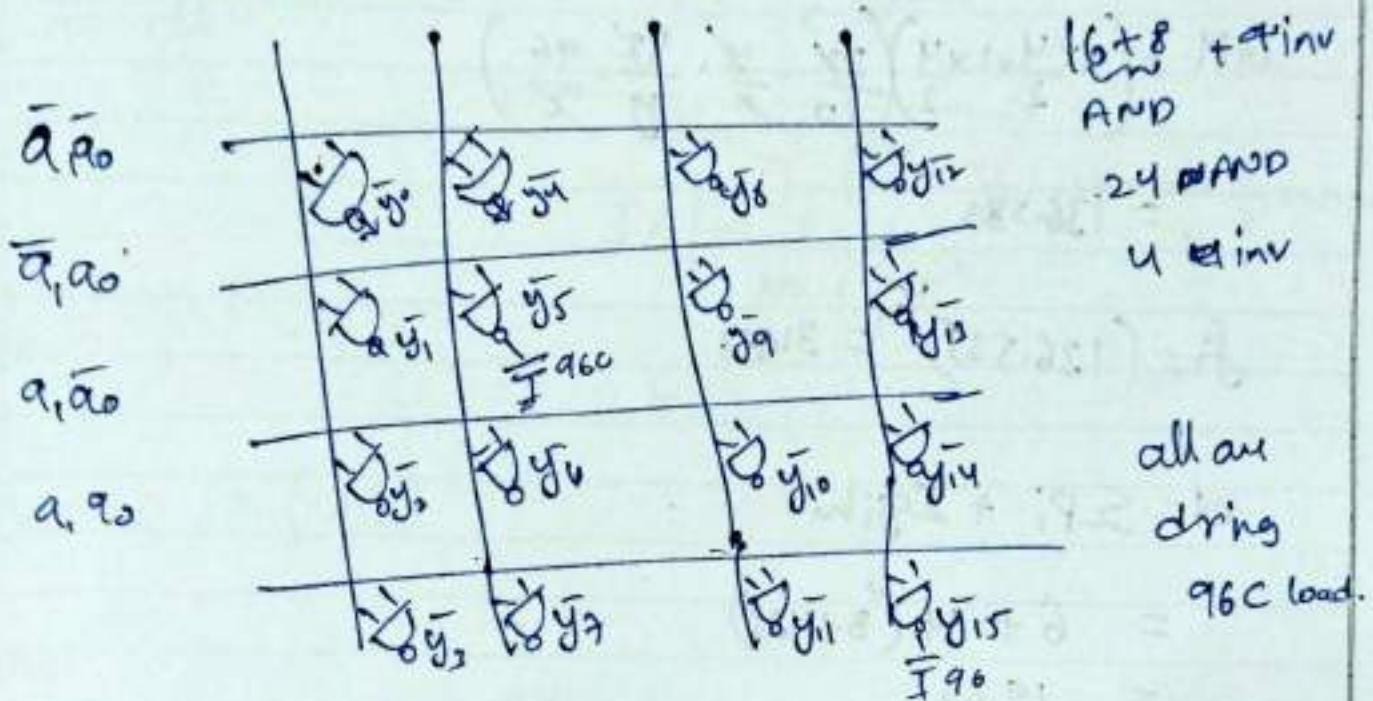
$$= \text{Delay} = 70 + 4(3.5204)$$

$$= 21.08$$

$a_3 \quad a_2 \quad a_1 \quad a_0$



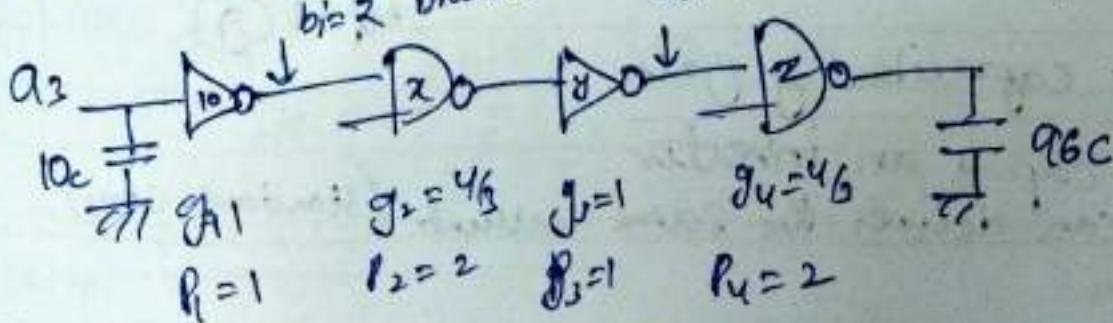
$\bar{a}_3 \bar{a}_2$ $\bar{a}_3 a_2$ $a_3 \bar{a}_2$ $a_3 a_2$



Now, stage step will be

$b_i = 2$ branchis

$b_i = 4$



y_{ij} all are like
this.

$$h_1 = \frac{2}{10} \quad h_2 = \frac{4}{2} \quad h_3 = \frac{4}{1} \quad h_4 = \frac{96}{2}$$

$$GH = \left(\frac{1}{3} \times \frac{4}{3} \times 1 \times \frac{4}{3} \right) \left(\frac{2}{10} \times \frac{4}{\pi} \times \frac{4\pi}{8} \times \frac{96}{2} \right)$$

$$= 136.533$$

$$f_i = (136.533)^{1/4} = 3.4183$$

$$d = \sum p_i + \sum g_i h_i$$

$$= 6 + 4 \cdot (3.4183)$$

$$= 19.67$$

$$N = \frac{\log F}{\log 3.4183} = 3.84 \approx 4 \quad \text{so need 10 update.}$$

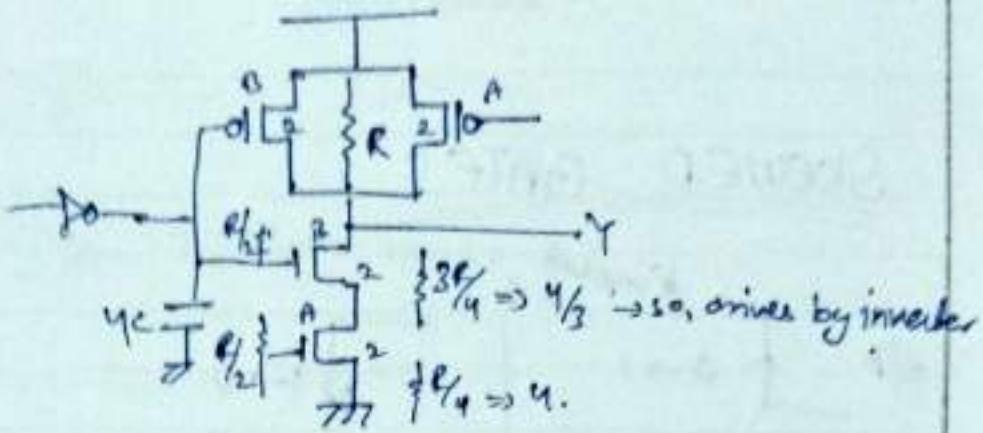
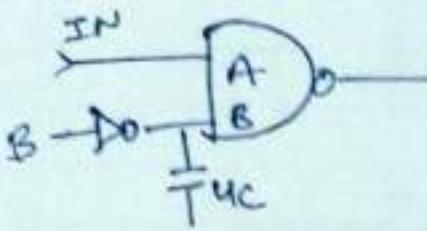
Reducing delay

$$D = \underbrace{\sum p_j}_{\text{constant}} + \underbrace{\sum g_i h_i}_t$$

} Asymmetric gates
 } Skewed gates
 } Reduce logical effort (g)

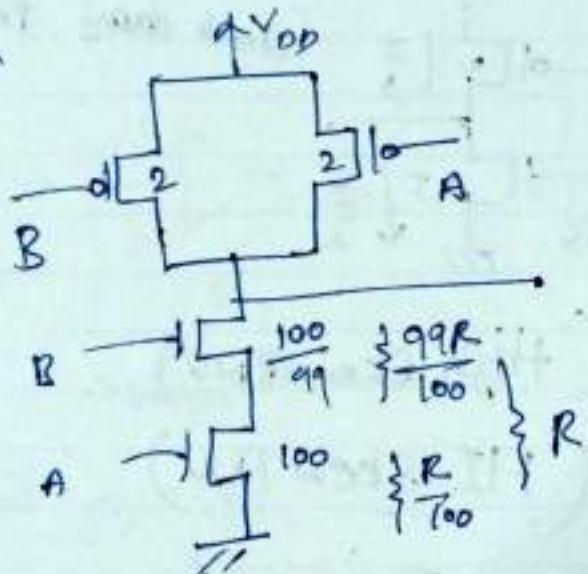
Asymmetric gates

g = Input capacitance of gate
 (I.C) Input cap of an inverter
 that can deliver the same current (standard CMOS)



worst

Bad Design



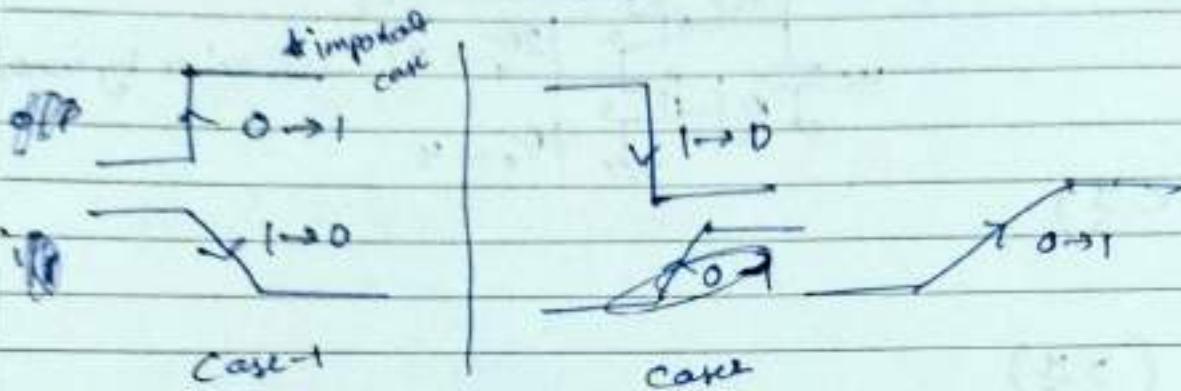
Can't choose
any value

$$g_B = \frac{2 + \frac{100}{99}}{3} \approx 1$$

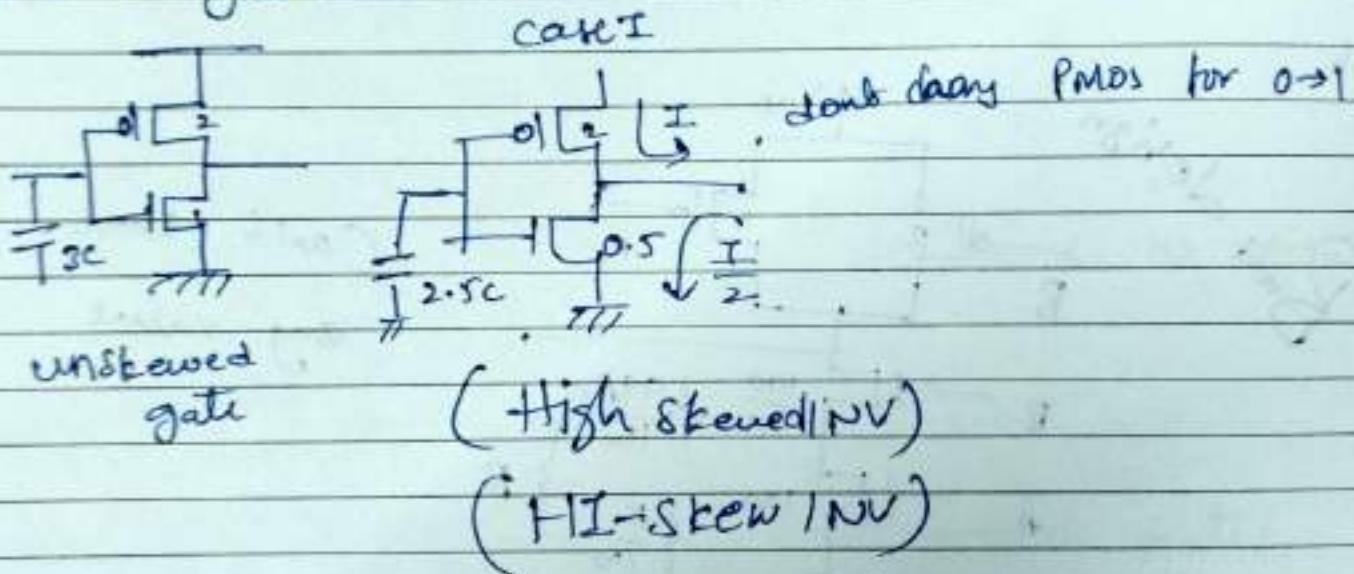
$$g_A = \frac{2 + 100}{3} = \frac{102}{3} = 34$$

// ct2

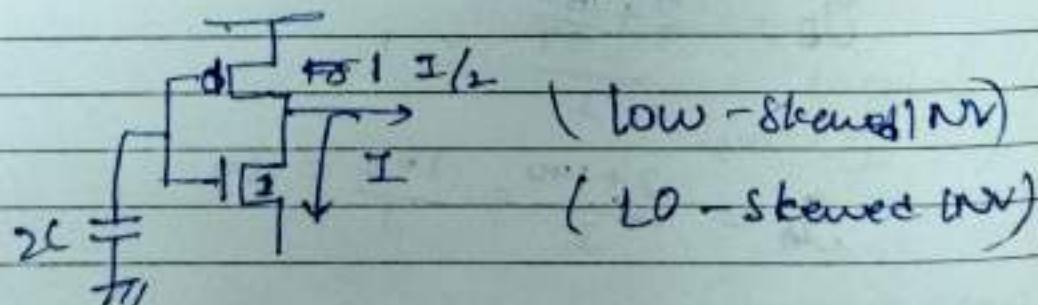
Skewed GATES



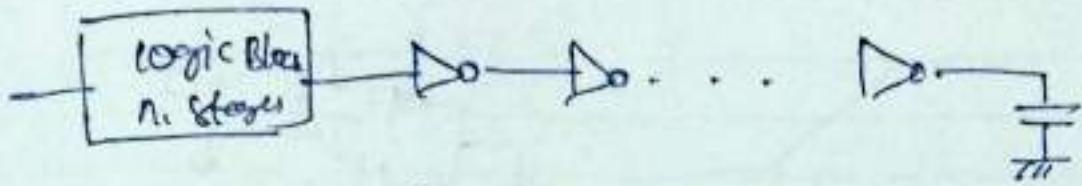
Skewed gates.



case II



21/oct/29

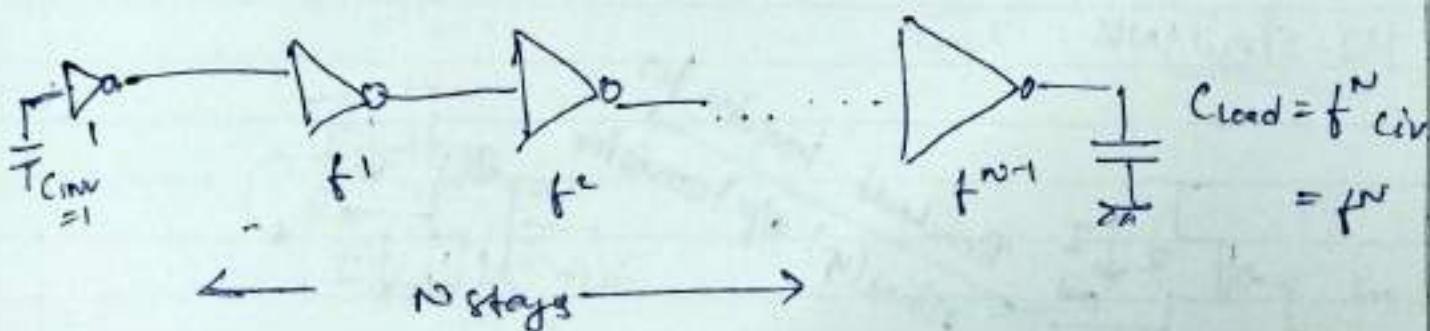


$\rightarrow \text{Do} \rightarrow \text{Do} \dots \leftarrow N-n, \text{Inv} \rightarrow$

$1 \leftarrow n_1 + N - n_1 = n \text{ stages} \rightarrow 1$

$$D = N f^{N^n} + \sum_{i=1}^n p_i + (N-n_1) p_{\text{inv}}$$

$$N = \frac{\ln F}{\ln(2.591)} \quad p_{\text{inv}} = 1$$



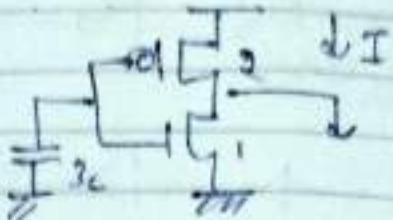
\rightarrow skewed gates :-

+ "Skewing" happens w.r.t unequal drive strengths

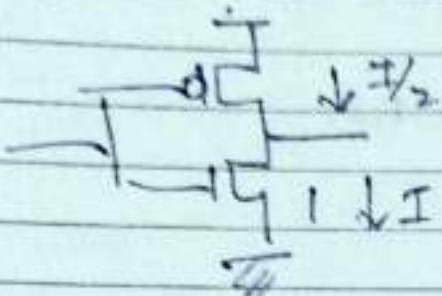
+ g_1 = logical effort for rising (v_p) o/p transition

$g_2 = \dots$ falling (v_n) " "

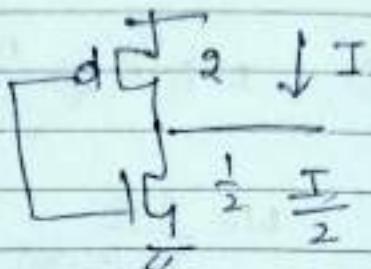
$\frac{g_2}{g_1} = \frac{\text{i/p capacitance of skewed gate}}{\text{i/p capacitance of an unskewed inverter with equal drive for that transition}}$



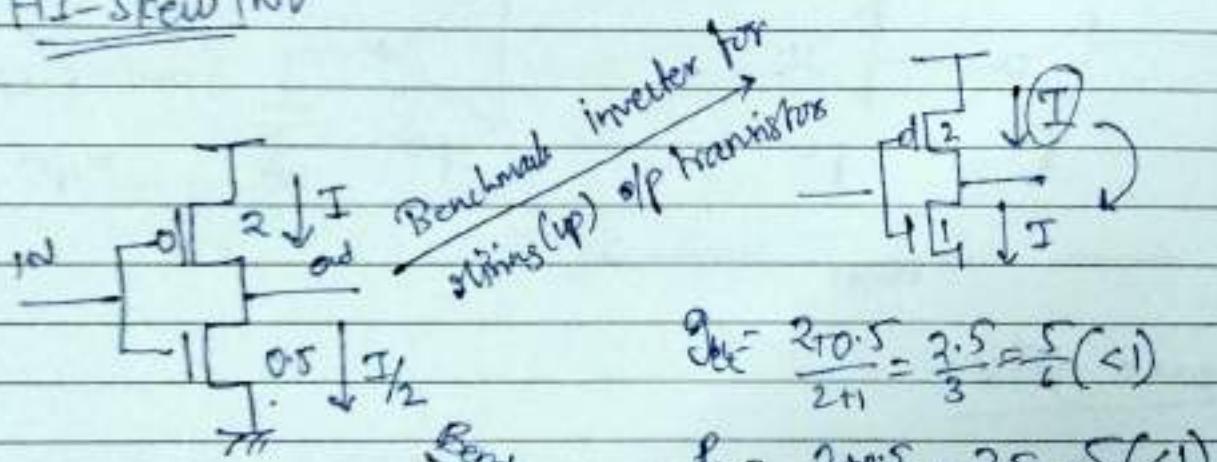
To skew inverter



Hi-skew inver

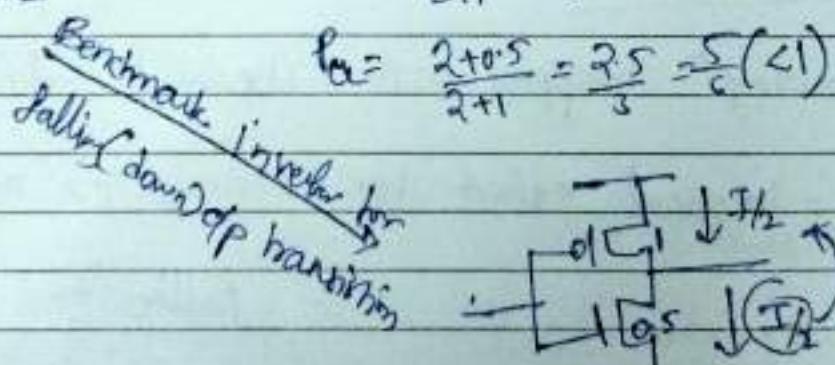


Hi-Skew INV



$$\beta_{dc} = \frac{2+0.5}{2+1} = \frac{2.5}{3} = \frac{5}{6} (< 1)$$

$$\beta_{dc} = \frac{2+0.5}{2+1} = \frac{2.5}{3} = \frac{5}{6} (< 1)$$



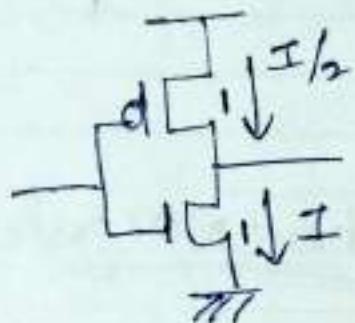
$$\beta_d = \frac{2+0.5}{1+0.5} = \frac{2.5}{1.5} = \frac{5}{3} (> 1)$$

$$\beta_d = \frac{2+0.5}{5+0.5} = \frac{2.5}{5.5} = \frac{5}{11} (> 1)$$

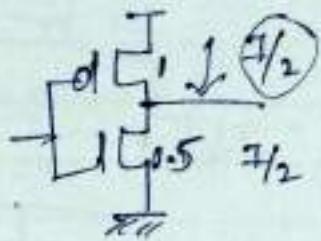
$$g_{avg} = \frac{g_u + g_d}{2} = \frac{\frac{1}{6} + \frac{5}{2}}{2} = \frac{5}{4}$$

$$P_{avg} = \frac{P_u + P_d}{2} = \frac{\frac{1}{6} + \frac{5}{2}}{2} = \frac{5}{4}$$

LO - skewed Inverter



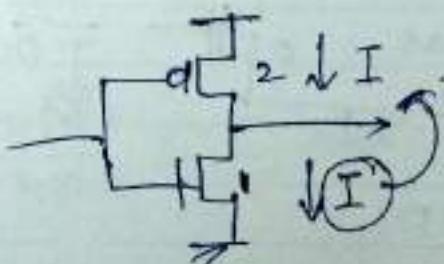
Benchmark Inverter
Rising up O/P branch.



$$g_u = \frac{1+1}{1+0.5} = \frac{2}{1.5} = \frac{4}{3} (\geq 1)$$

$$P_u = \frac{1+1}{1+0.5} = \frac{2}{1.5} = \frac{4}{3} (\geq 1)$$

Benchmark
Falling (down) Invert
O/P branc

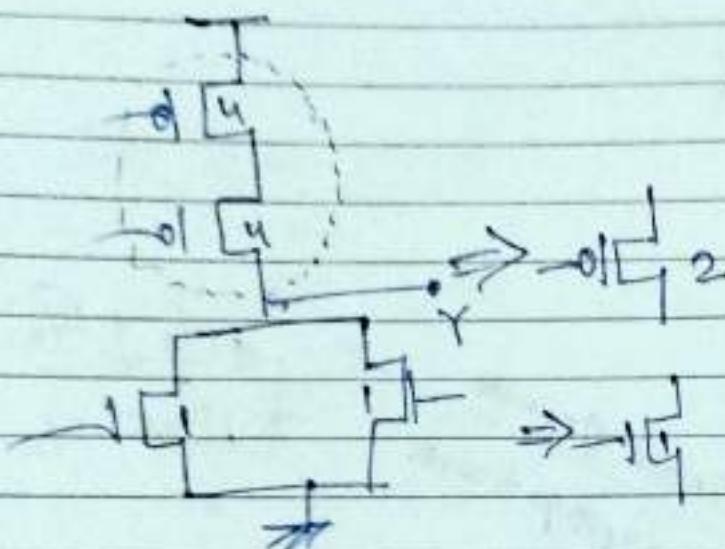


$$g_d = \frac{1+1}{1+2} = \frac{2}{3} (< 1)$$

$$P_d = \frac{1+1}{1+2} = \frac{2}{3} (< 1)$$

$$g_{avg} = \frac{g_u + g_d}{2} = 1$$

$$P_{avg} = \frac{P_u + P_d}{2} = 1$$

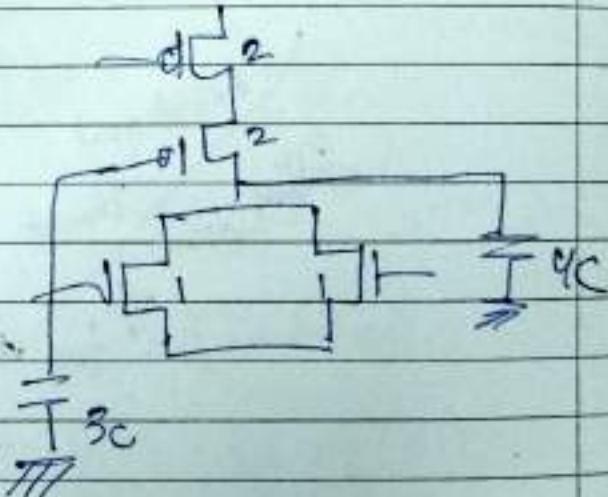
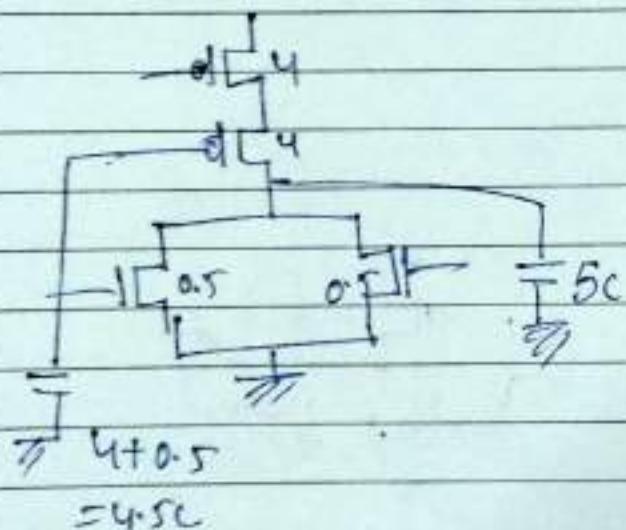
NORHystewLstew

2

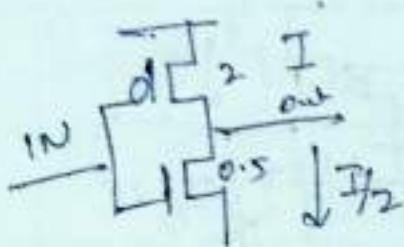
1

0.5

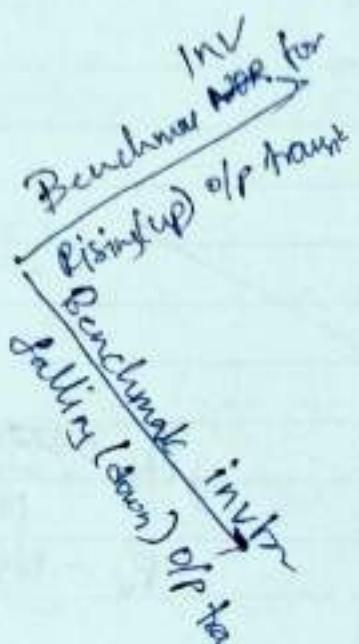
1

Hystew NOR gateLo-Stew NOR gate

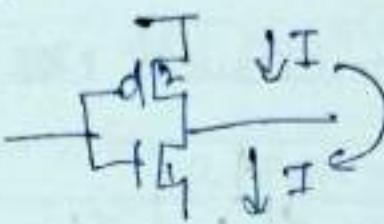
Hf Stew NOR



Easy inv for NOR

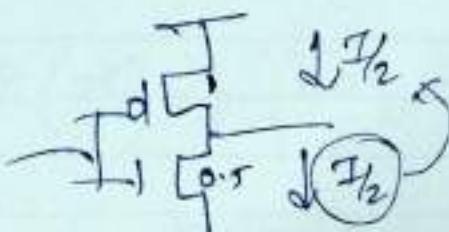


Benchmark INV for NOR



$$g_u = \frac{4+0.5}{2+1} = \frac{4.5}{3} = 1.5 (< 2)$$

$$P_u = \frac{4+0.5+0.5}{2+1} = \frac{5}{3} = 1.67 (> 2)$$



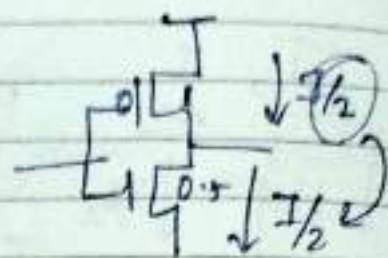
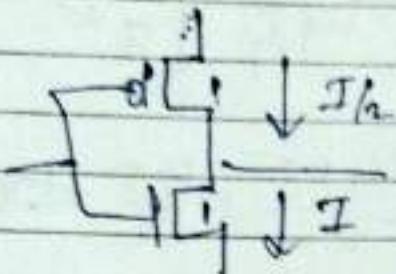
$$g_d = \frac{4+0.5}{1+0.5} = \frac{4.5}{1.5} = 3 (> 2)$$

$$P_d = \frac{4+0.5+0.5}{1+0.5} = \frac{5}{1.5} = 3.33 (\cancel{> 2})$$

$$g_{avg} = \frac{g_u + g_d}{2} = 2.25 (> 2)$$

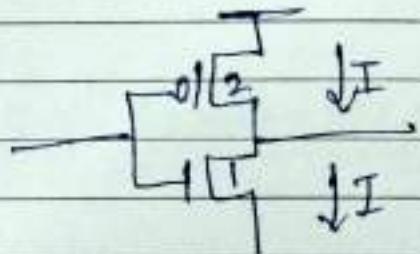
$$P_{avg} = 2.5 (> 2)$$

Lo-skewed NOR



$$\alpha_1 = \frac{4+0.5}{1+0.5} = \frac{4.5}{1.5} = \frac{3}{1.5} = 2 \left(\frac{2}{3} \right)$$

$$\beta_1 = \frac{4+0.5+2}{1+0.5} = \frac{7.5}{1.5} = \frac{4}{1.5} = \frac{8}{3} \left(\frac{8}{3} \right)$$



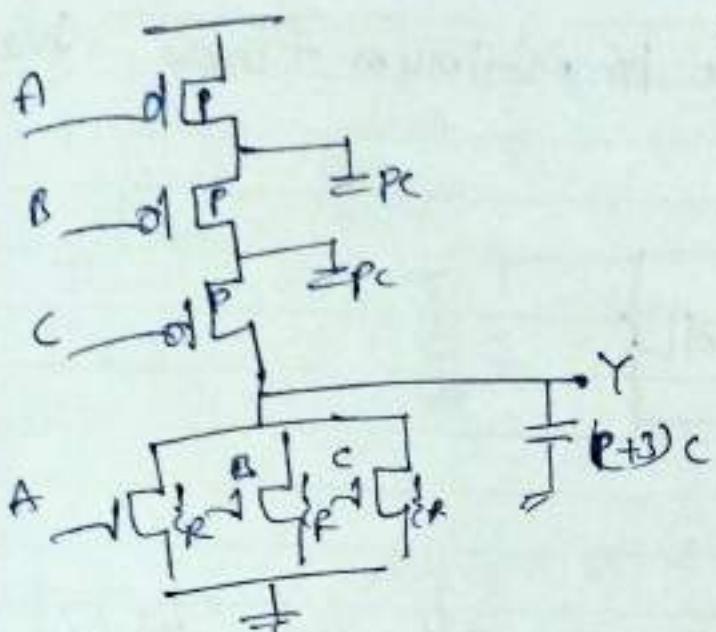
$$g_d = \frac{2+1}{2+1} = 1 \left(< \frac{5}{3} \right)$$

$$P_d = \frac{2+1+1}{2+1} = \frac{4}{3} \left(< 2 \right)$$

$$Gang = \frac{2+1}{2} = 1.5 \left(< \frac{5}{3} \right)$$

$$P_{avg} = \frac{\frac{8}{3} + \frac{4}{3}}{2} = 2 \left(\approx 2 \right)$$

Note: In memory design (as shown above) and



Best P/N ratio for minimum

Elmore delay. $P \rightarrow$ PMOS width

$N \rightarrow 6 \text{ " } N_{NMOS}$

$$\begin{aligned} t_{PPDF} &= (P+3) RC & b=c=0 \\ &\quad + PCR + PCR \\ &= 3RC(P+1) \end{aligned}$$

$$t_{PPDR} = PC\left(\frac{2R}{P}\right) + PC\left(\frac{4R}{P}\right) +$$

$$(P+3)C \cdot \frac{6R}{P}$$

$$\Rightarrow 6RC + \frac{6R}{P}(P+3)C$$

$$D = t_{PDF} + t_{PDR}$$

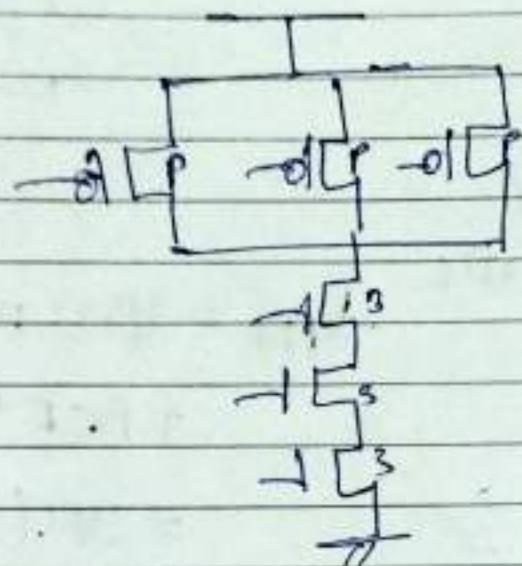
$$= 3PRC + 15RC + 18RC P^{-1}$$

$$\frac{\partial D}{\partial P} = 0 \Rightarrow P = \sqrt{6}$$

so instead of 6 if we keep $\sqrt{6}$ then delay will be minimum.

$$\frac{P}{N} = \frac{\sqrt{6}}{1} = \sqrt{6}$$

Homework : Best P/N ratio for minimum Elmore delay
for NAND



after solving $P=16$

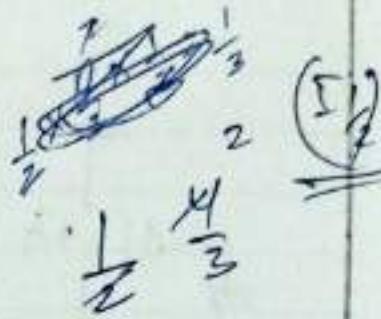
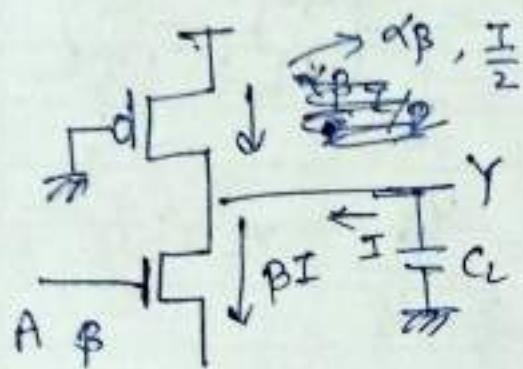
$$\frac{P}{N} = \frac{\sqrt{6}}{3} = \sqrt{\frac{2}{3}}$$

$$\left(\frac{P}{N}\right)_{\text{best}} = \sqrt{\left(\frac{P}{N}\right)_{\text{unskewed unit gate}}}$$

for min delay

unskewed
unit gate

PSEUDO-N-MOS



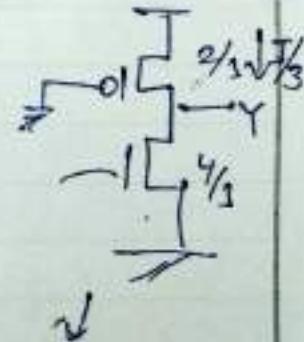
applying KCL @ P.

$$\text{Suppose } \alpha = \frac{1}{2}$$

$$\begin{aligned} \beta I &= \frac{\alpha \beta I}{2} + I \\ \beta &= \frac{\alpha \beta}{2} + 1 \end{aligned}$$

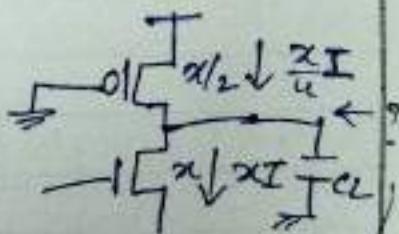
$$\beta \left(1 - \frac{\alpha}{2}\right) = 1$$

$$\boxed{\beta = \frac{1}{1 - \frac{\alpha}{2}}}$$



$$2 \rightarrow I$$

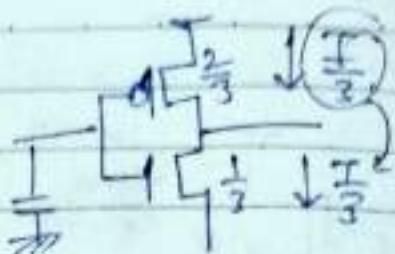
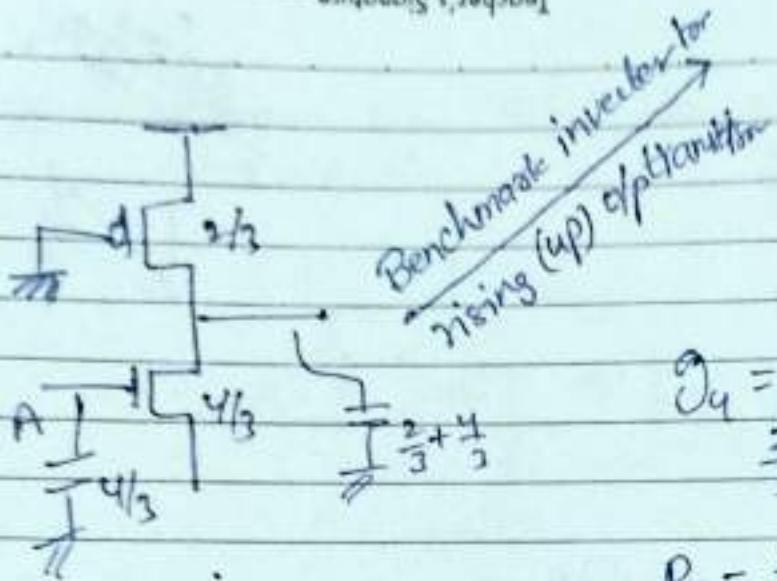
$$\frac{2}{3} \rightarrow \frac{I}{3} \quad \text{for PMOS}$$



$$x_1 I - \frac{x_1 I}{4} = \frac{3x_1 I}{4}$$

$$3x_1 \frac{I}{4} = I$$

$$\boxed{x_1 = 4/3}$$

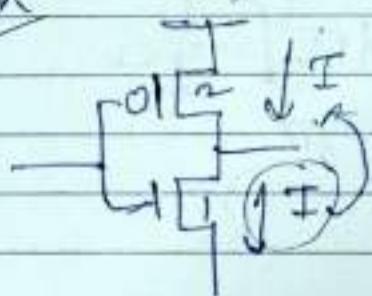


$$g_d = \frac{4/3}{2/3 + 1/3} = 4/3 (> 1)$$

$$P_d = \frac{2/3 + 4/3}{2/3 + 1/3} = 2 (> 1)$$

~~Benchmark inverter for
falling (down) optimization~~

catch



Vel. min. for
Xh

$$g_d = \frac{4/3}{2+1} = \frac{4}{9} (< 1) \quad g_{avg} = \frac{4/3 + 4}{2} = \frac{8}{9} (\approx 1)$$

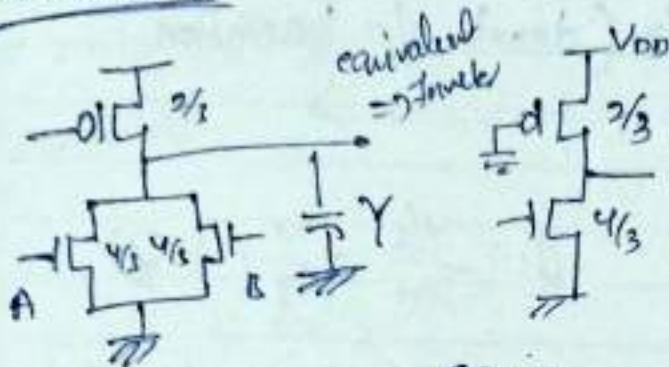
$$P_d = \frac{2/3 + 4/3}{2+1} = \frac{2}{3} (< 1) \quad P_{avg} = \frac{2 + 2/3}{2} = \frac{4}{3} (\approx 1)$$

g_{avg} ten is better than Pang coz it

will get multiplied by h

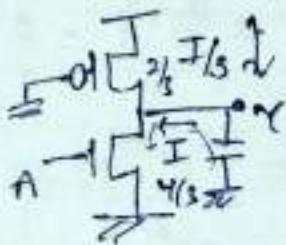
23 Oct 24

Pseudo NOR

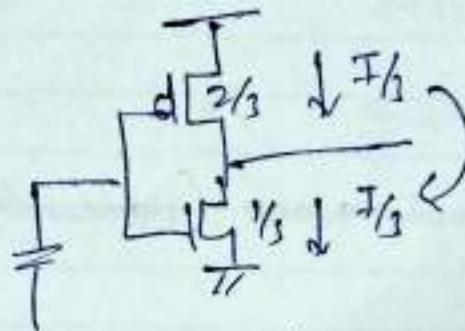
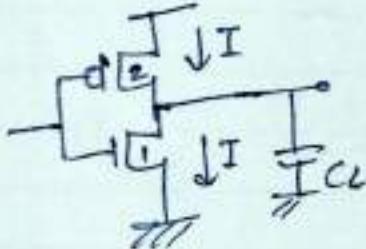


Benchmark Inverter
for rising (up) off
transitions.

Pseudo-inverter



Static CMOS

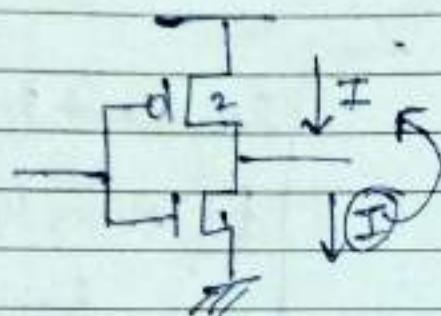


$$g_m = \frac{4/3 \times i_D}{2/3 + 1/3} = \frac{4}{3} (< g_{m1})$$

8

$$P_H = \frac{2/3 + 4/3 + 4/3}{2/3 + 1/3} = 10/3 (> 2)$$

Benchmark inverter for falling (down) o/p transition.



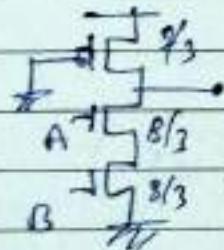
$$g_d = \frac{4/3}{2+1} = \frac{4}{9} (< 8)$$

$$P_d = \frac{2/3 + 4/3 + 4/3}{2+1} = \frac{10}{9} (c_2)$$

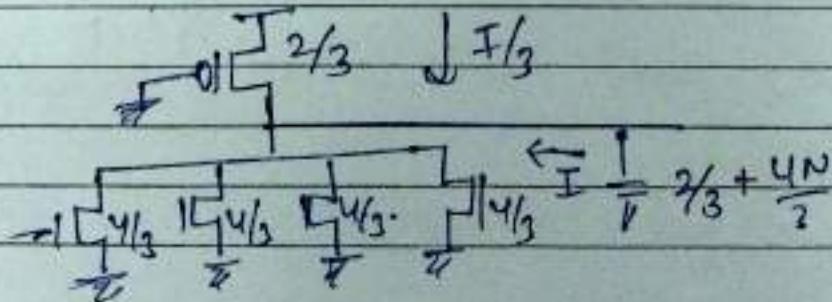
$$g_{avg} = \frac{g_{out} + g_d}{2} = \frac{4 + 4}{2} = \frac{8}{9} (< \frac{10}{3})$$

$$P_{avg} = \frac{P_{out} + P_d}{2} = \frac{10/3 + 10/9}{2} = \frac{20}{9}$$

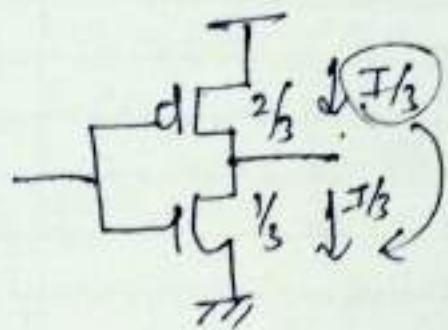
Pseudo-NAND (Homework)



Pseudo NMOS based N-invert NOR gate.



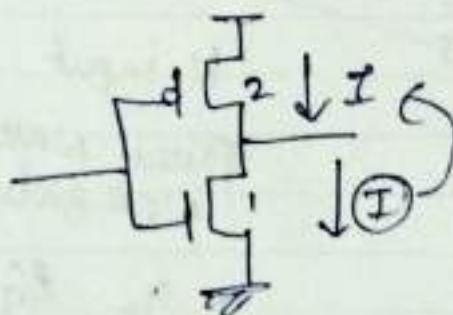
Benchmark inverter
for rising (up) o/p
transition.



$$g_u = \frac{4/3}{2/3 + 1/3} = \frac{4}{3}$$

$$P_u = \frac{\frac{2}{3} + \frac{4N}{3}}{\frac{2}{3} + \frac{1}{3}} = \frac{\frac{2}{3} + \frac{4N}{3}}{1}$$

Benchmark inverter for
falling (down) o/p transition

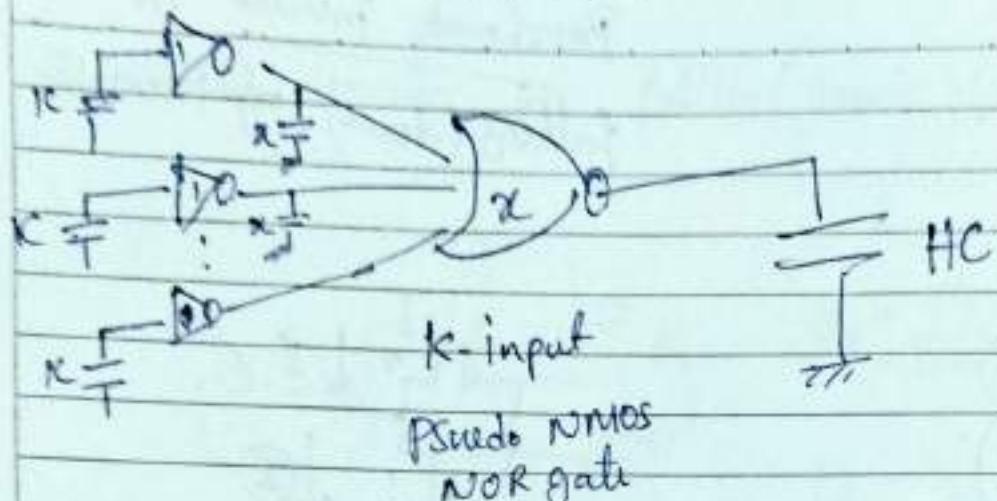


$$g_d = \frac{4/3}{2+1} = 4/9$$

$$P_d = \frac{\frac{2}{3} + \frac{4N}{3}}{3} = \frac{4N+2}{9}$$

$$g_{avg} = \frac{g_u + g_d}{2} = 8/9 \text{ - constant}$$

$$P_{avg} = \frac{P_u + P_d}{2} = \frac{4}{9}(2N+1)$$



$$g_1 = 1$$

$$g_2 = 8/9$$

$$P_1 = 1$$

$$P_2 = \frac{4}{9}(2k+1)$$

$$h_1 = \frac{x}{x} = 1$$

$$h_2 = \frac{H}{x}$$

$$F = g_1 h_1 g_2 h_2$$

$$= 1 \cdot 1 \cdot \frac{8}{9} \cdot \frac{H}{x} = \frac{8H}{9}$$

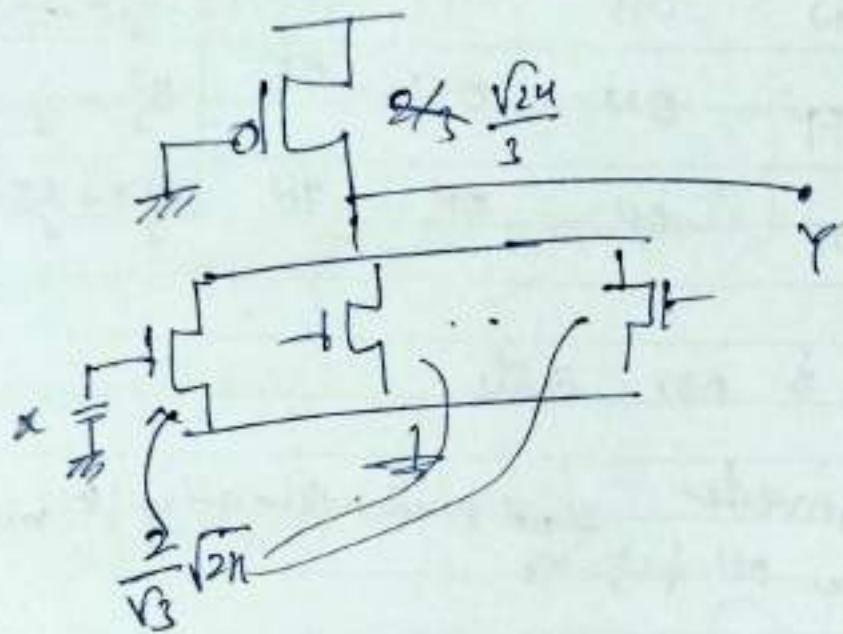
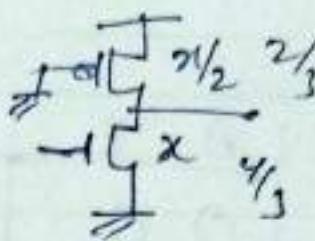
$$f_t = (F)^{1/2} = \sqrt{\frac{8H}{9}} = \frac{2\sqrt{2H}}{3}$$

$$D_{min} = 2L \cancel{\left(\frac{2f_t H}{3} \right)} \quad 1 + \frac{4}{9}(2k+1) + 2 \cdot \cancel{\frac{2f_t H}{3}}$$

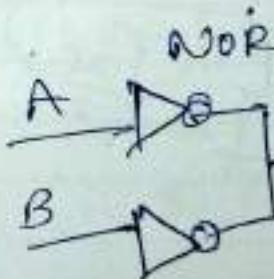
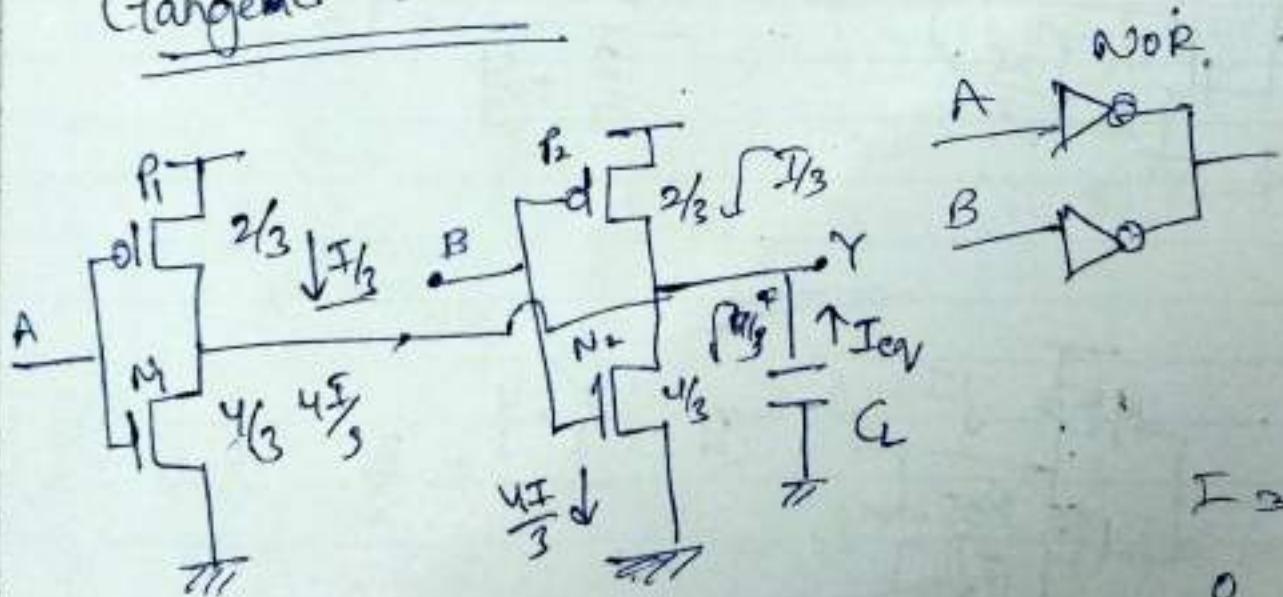
$$\Rightarrow \frac{8k+3}{9} + \frac{4\sqrt{2H}}{3}$$

$$f_i = g_s h_f$$

$$\frac{2\sqrt{2n}}{3} = x$$



Gangended CMOS

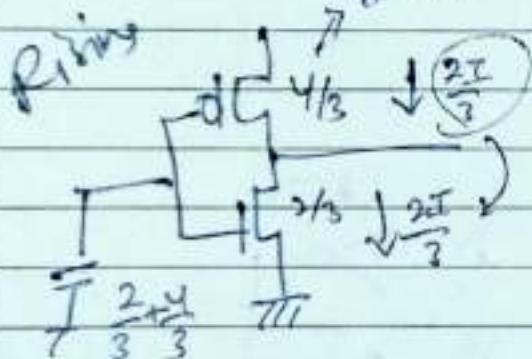


$$I_D = \frac{Q}{L}$$

Y	A	B	P_1	P_2	N_1	N_2	I _{out}
1	0	0	ON	ON	OFF	OFF	$-I_{13} - I_{14} = -2\frac{I}{3}$ change
0	0	1	ON	OFF	OFF	ON	$\frac{4I}{3} - \frac{I}{2} = I$
0	1	0	OFF	ON	ON	OFF	$\frac{4I}{3} - \frac{I}{3} = I$
0	1	1	OFF	OFF	ON	ON	$\frac{4I}{3} + \frac{4I}{3} = \frac{8I}{3} (2I)$

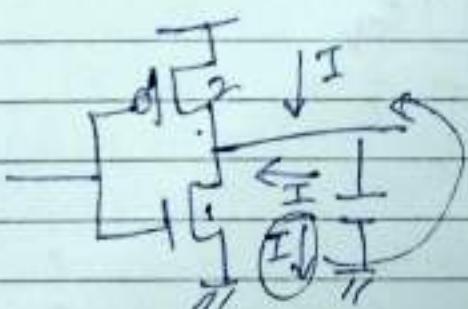
\therefore it is nor gate.

g Benchmark inverter # will parallel will be add up (w/c) but
max ON. $\frac{2}{3} + \frac{2}{3} = \frac{4}{3}$



$$g_d = \frac{\frac{2}{3} + \frac{4}{3}}{\frac{2}{3} + \frac{4}{3}} = 1 < \frac{5}{3}$$

Now



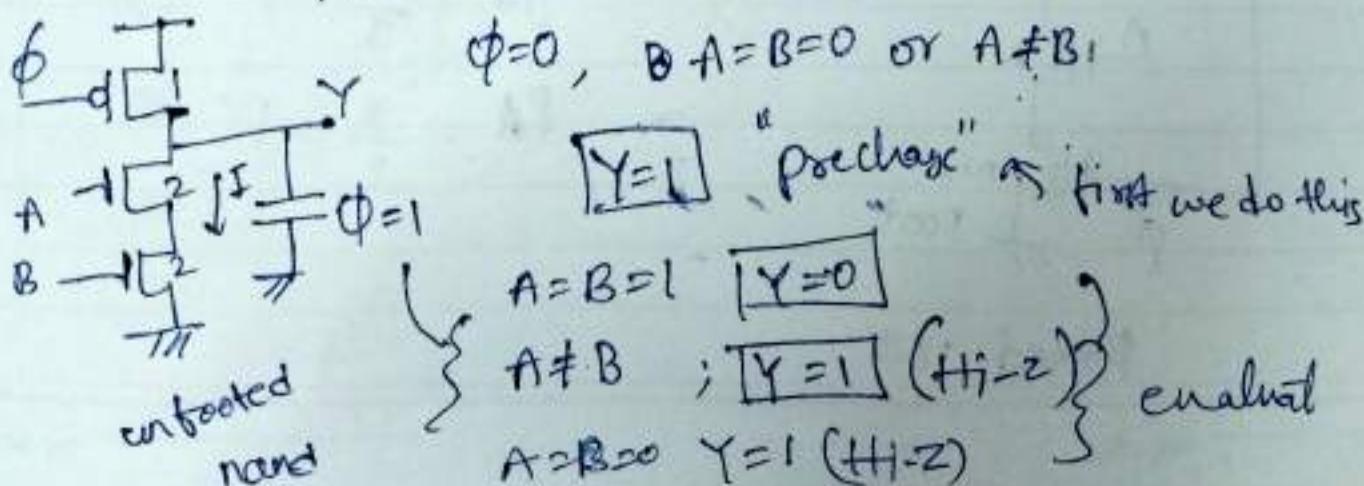
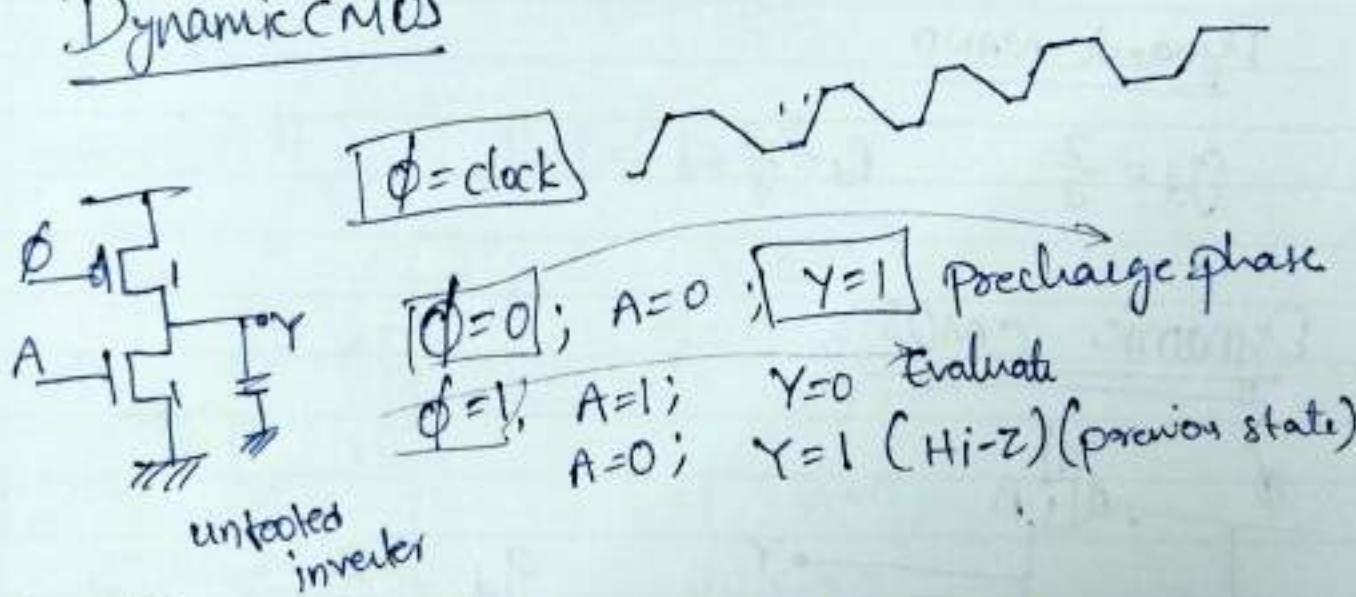
$$g_d = \frac{\frac{2}{3} + \frac{4}{3}}{2+1} = \frac{2}{3}$$

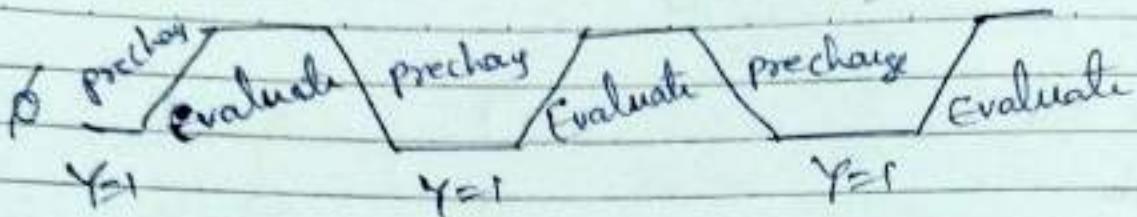
$$g_{avg} = \frac{1+\frac{4}{3}}{2} = \frac{5}{6} (< 5/3)$$

Various ways to reduce delay

- i) equalize stage effort
- ii) add inverter
- iii) asymmetric ganged
- iv) Skewed gate
- v) pseudonMOS
- vi) Ganged CMOS (only for NOR gate)
- vii) Dynamic CMOS

Dynamic CMOS





$g_d = \infty$ $p_u =$ because "1" remains "1"
IRrelevant

Dynamic inverter

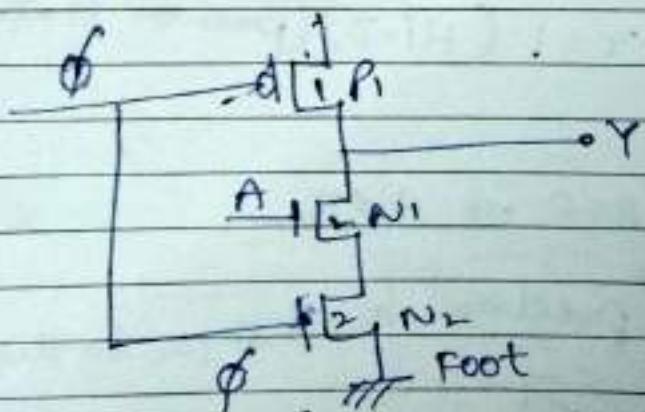
$$g_d = \frac{1}{3c} = \frac{1}{3}$$

$$p_d = \frac{2}{3}$$

Dynamic NAND

$$g_d = \frac{2}{3} \quad p_d = \frac{3}{3} = 1$$

Dynamic CMOS



$$g_d = \frac{2}{3}$$

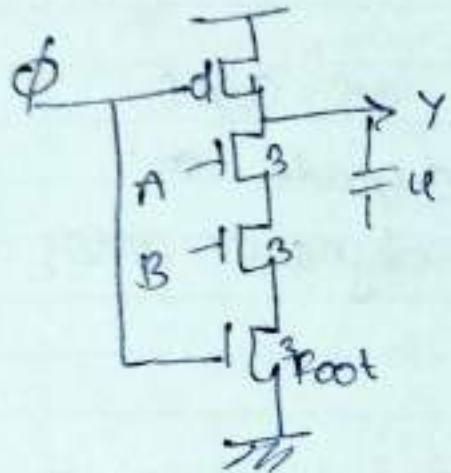
$$p_d = \frac{3}{3} = 1$$

Rooted INV

$$\phi = 0; A = x; Y = 1$$

$$\phi = 1; Y = \bar{A}$$

for NAND



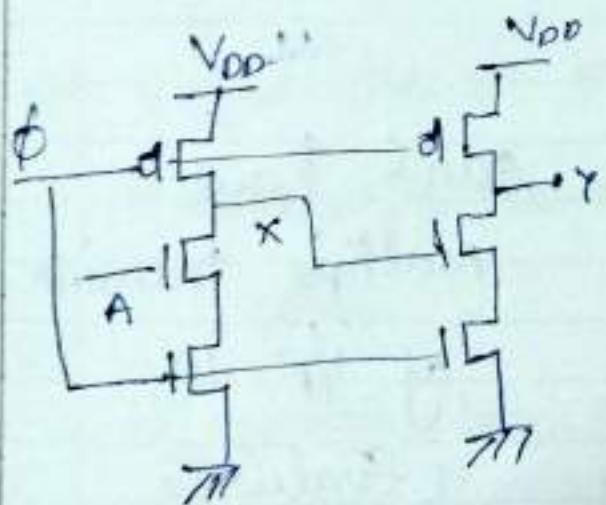
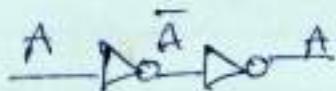
$$\phi = 0, Y = 1$$

$$\phi = 1, Y = \overline{AB}$$

$$g_d = \frac{3}{3} = 1$$

$$P_d = \frac{u}{3} =$$

footed NAND



$$A = 1$$

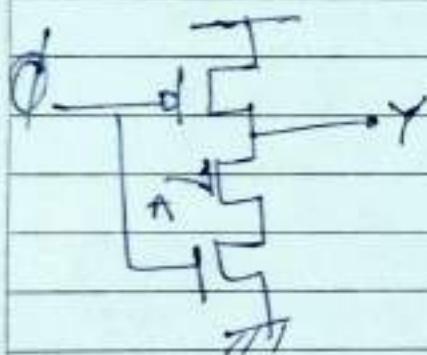
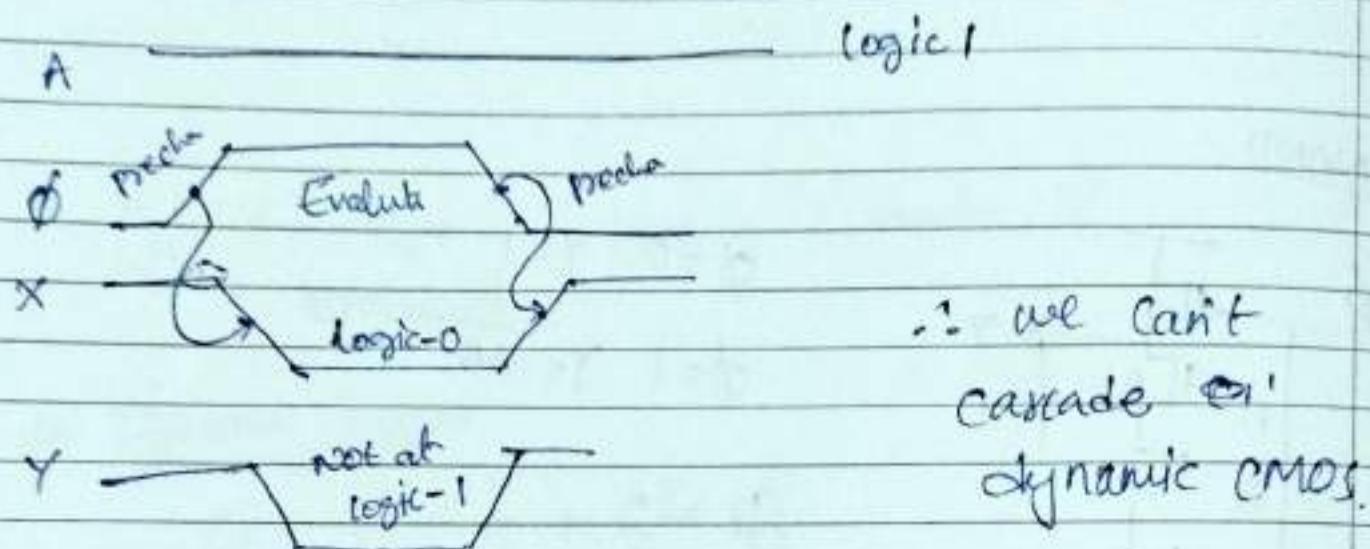
$$\phi = 0; X = 1$$

$$Y = 1$$

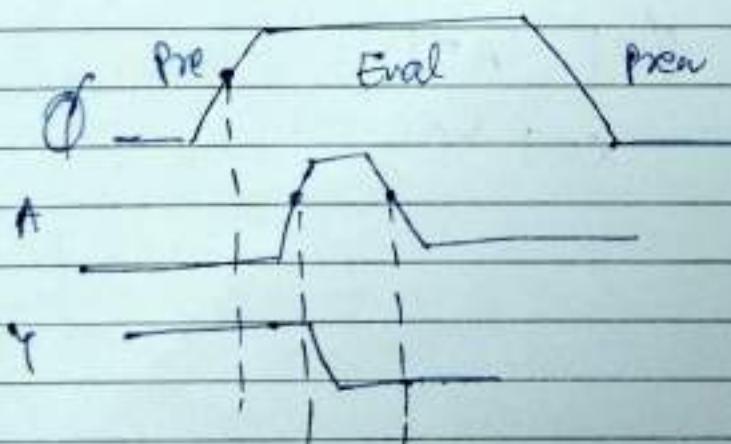
$$\phi = 1, A = 1$$

$$X = 1 \rightarrow 0$$

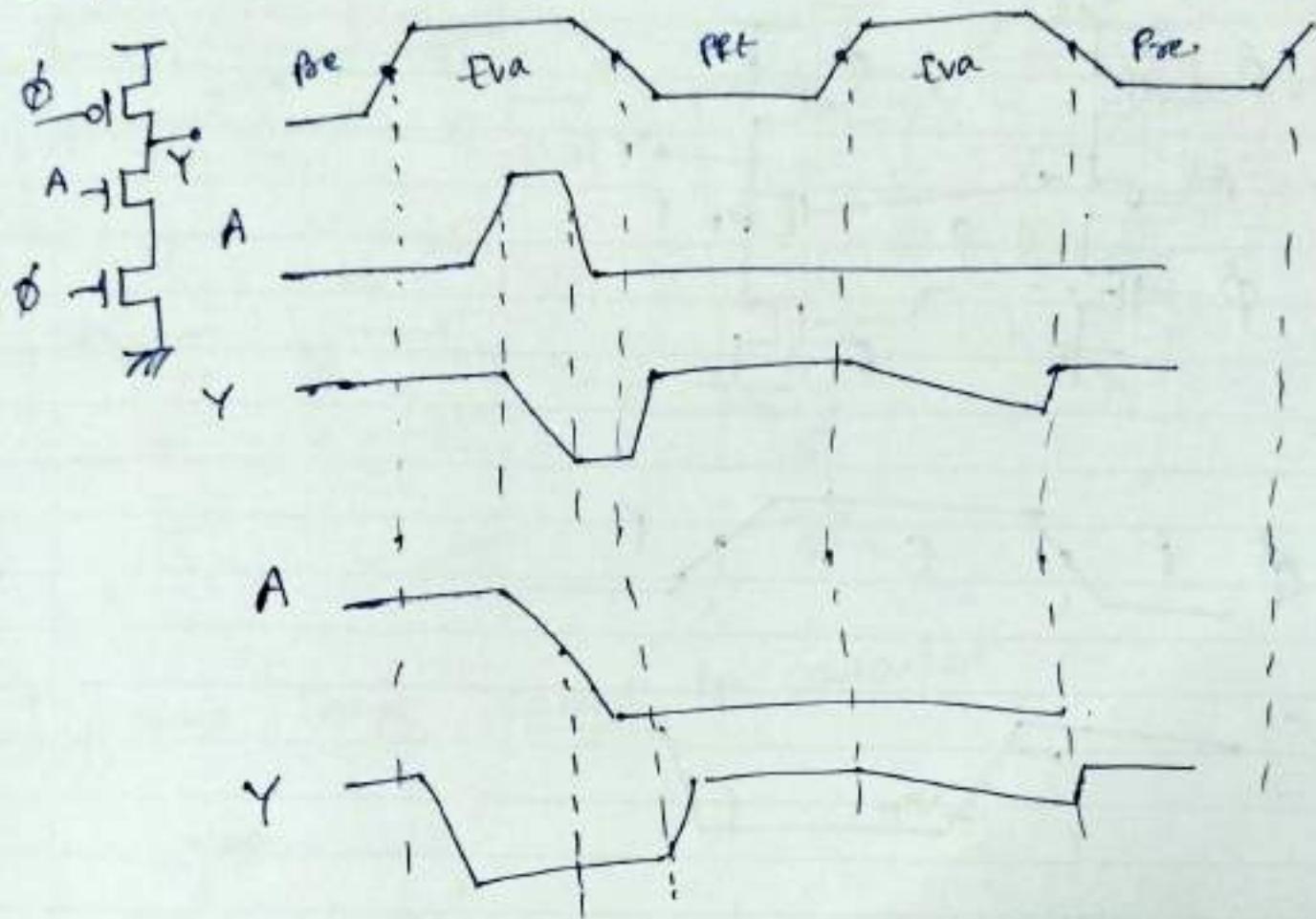
Timing zero.



can't have
multiple transistors
of i/p in
Evaluate
Phase

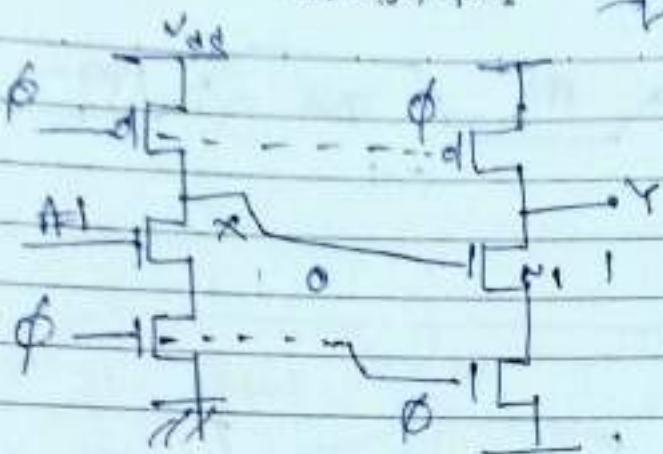


28/06/2024
Recap

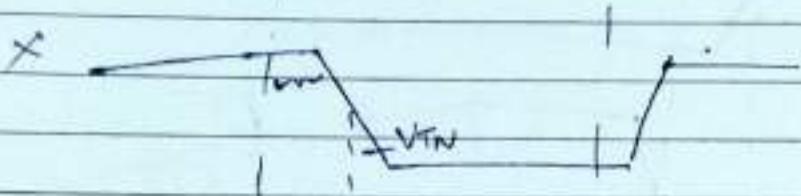


- Note:
- i) input has to be monotonically rising.
 - ii) no multiple transition within one cycle evaluate phase
 - iii) dynamic logic also cannot respond to monotonically falling.

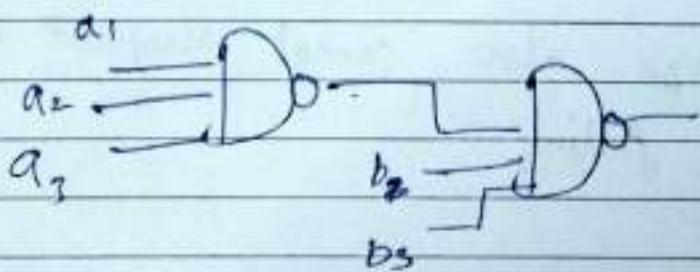
Do Do

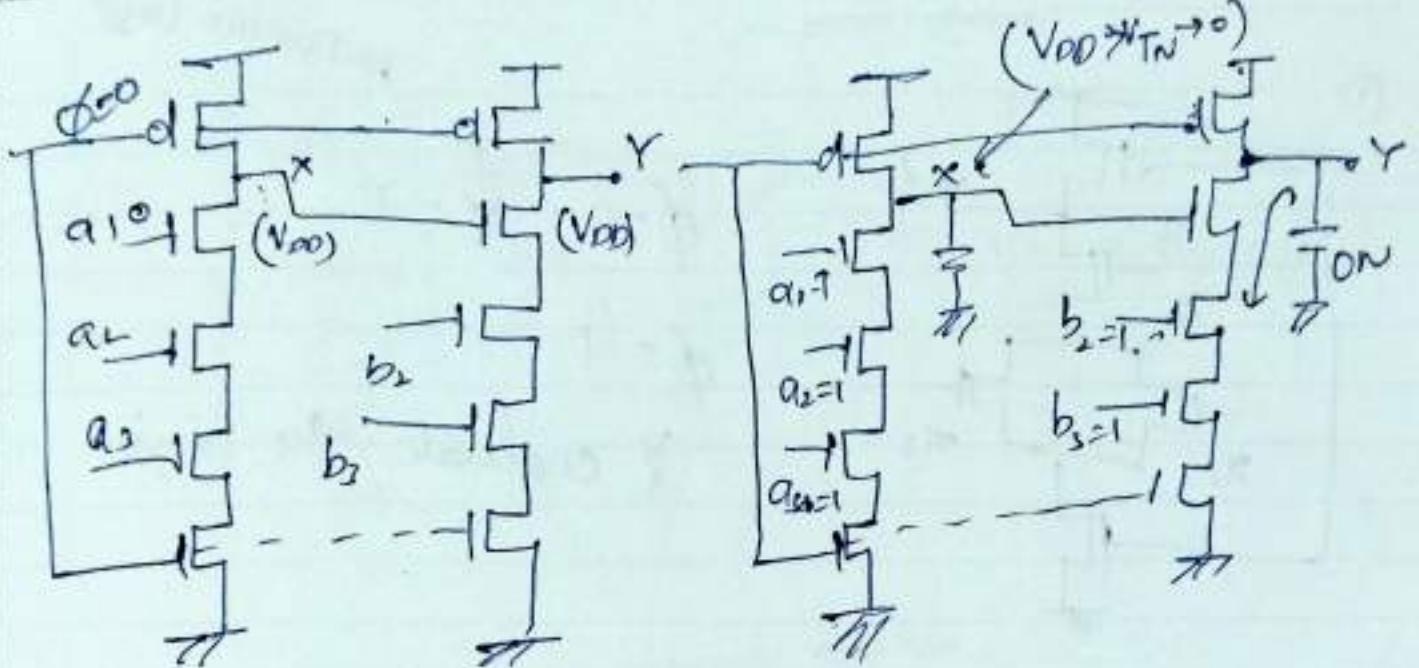


$\phi \rightarrow P \rightarrow E \rightarrow P$

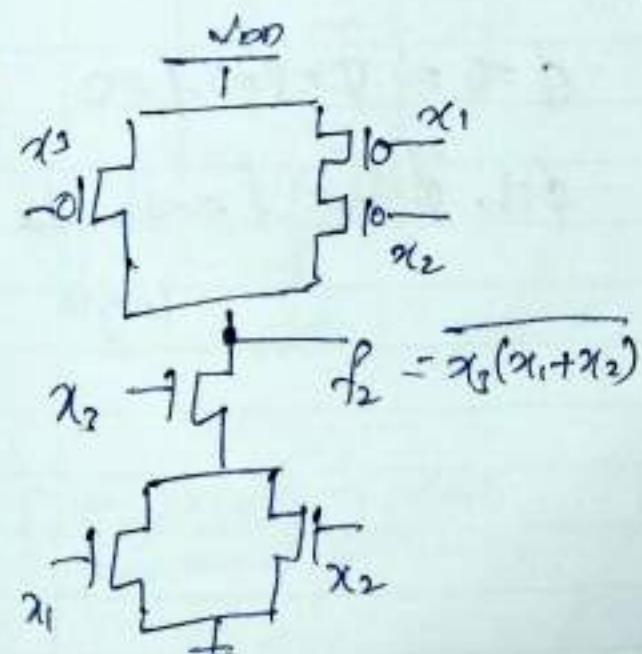


②

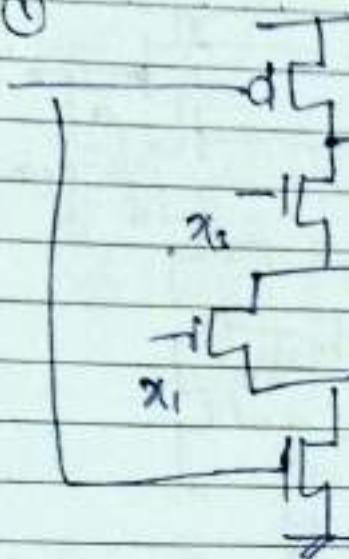




→ Dynamic logic cannot be cascaded



①

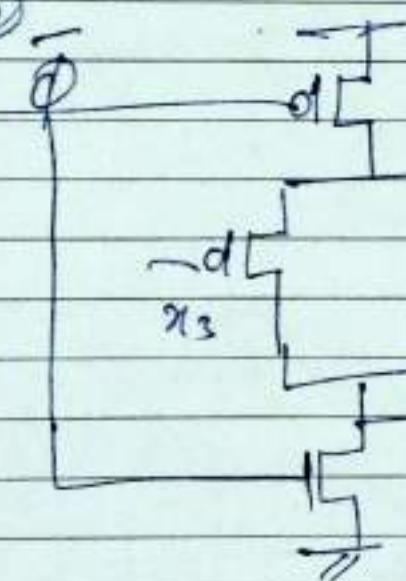


$$\phi = 0 \quad f = 1$$

$$\phi = 1$$

X evaluate the logic

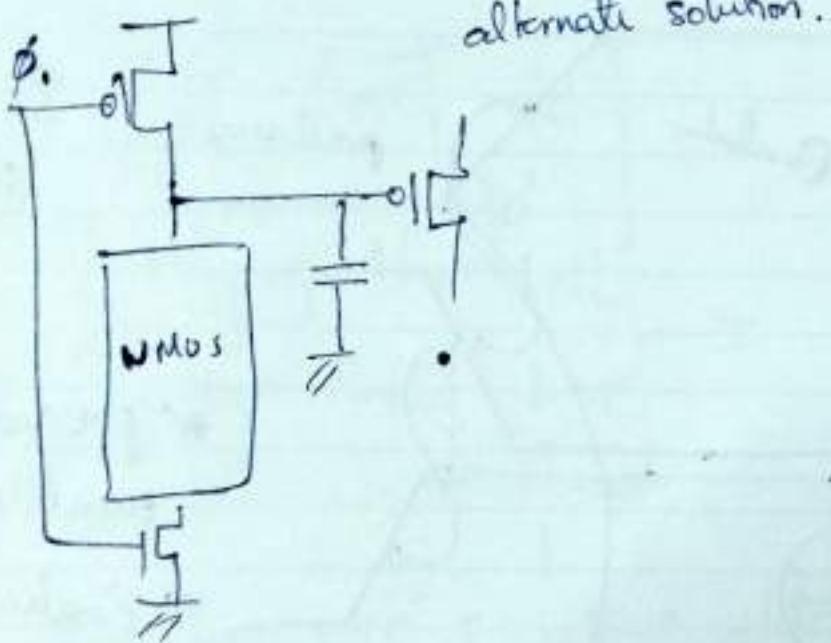
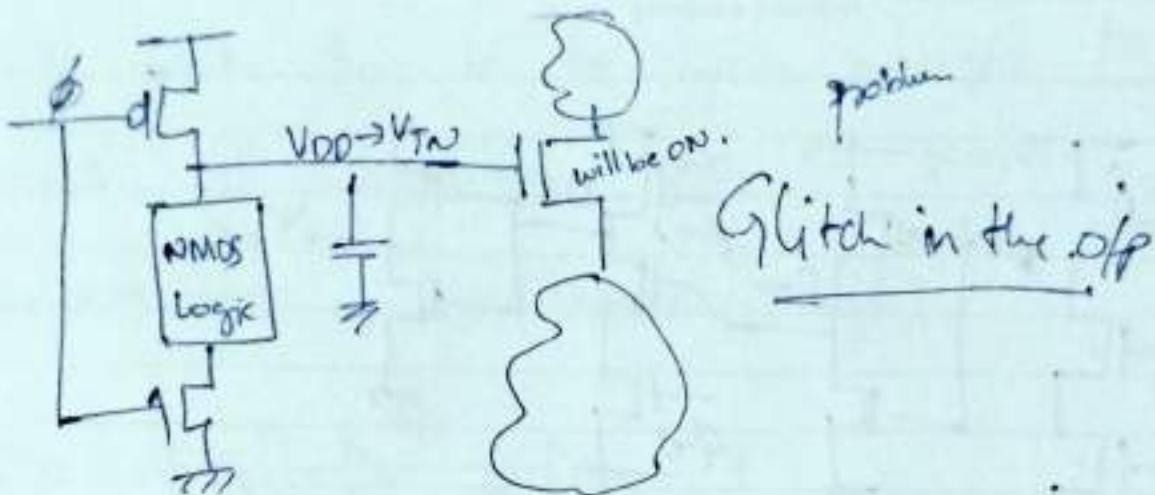
②



Dynamic PMOS

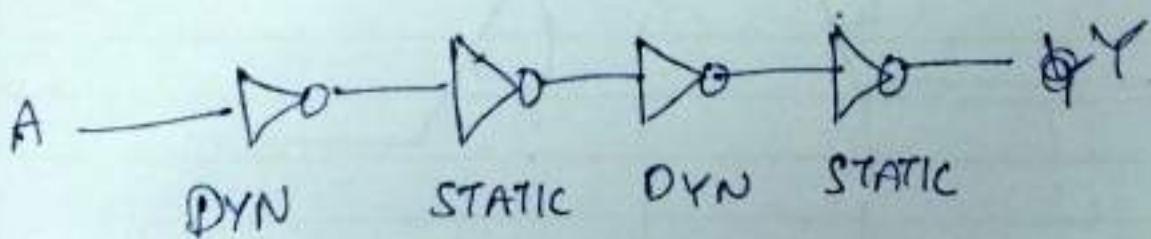
$$\phi = 0 \Rightarrow \bar{\phi} = 1 \Rightarrow f = 0$$

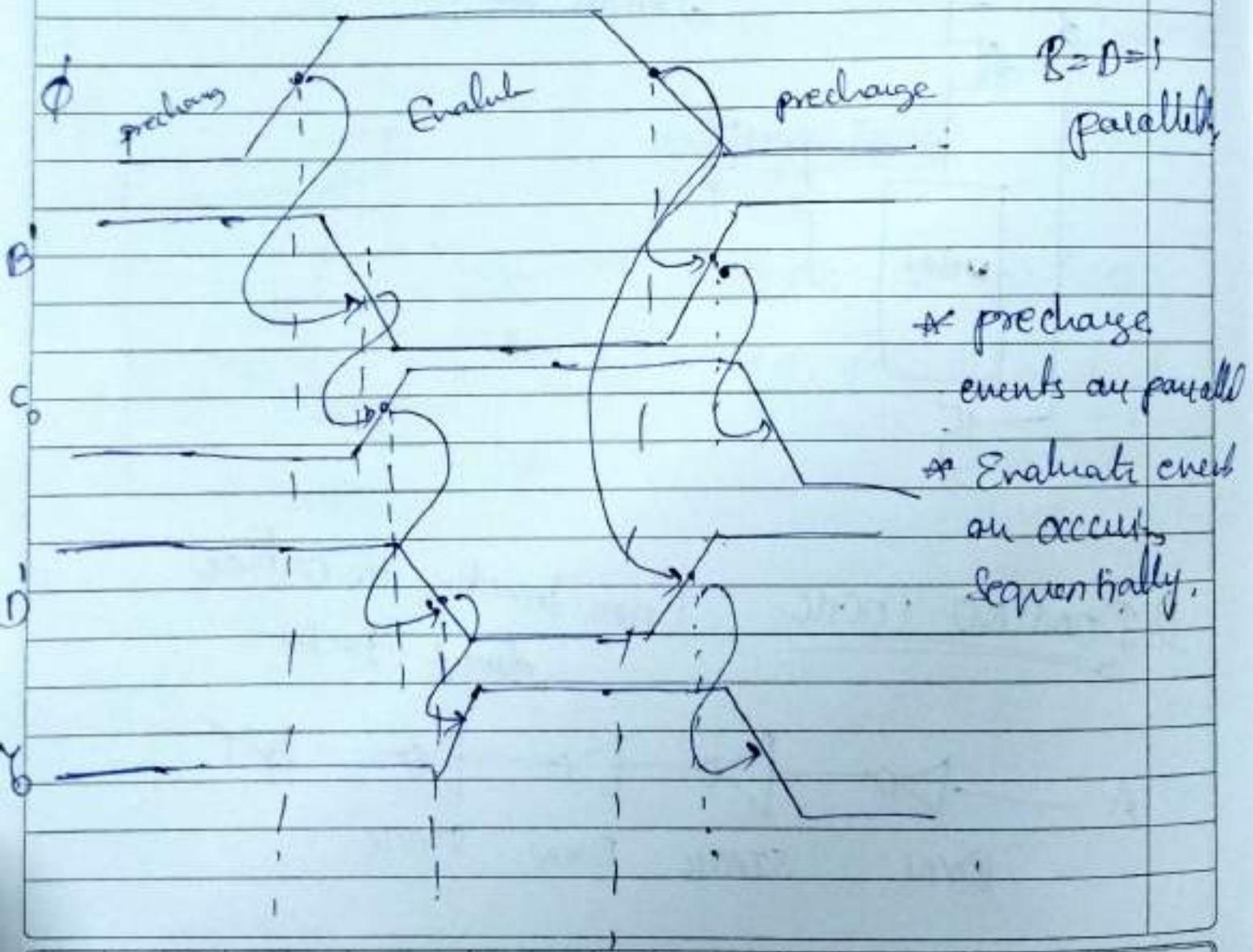
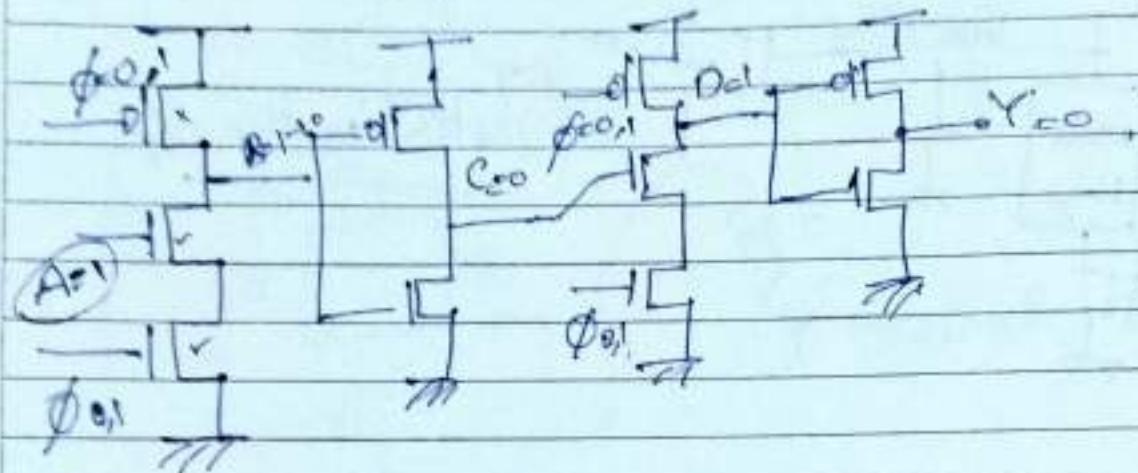
$$\phi = 1, \bar{\phi} = 0 \Rightarrow f \text{ evaluate logic}$$



1) DOMINO LOGIC

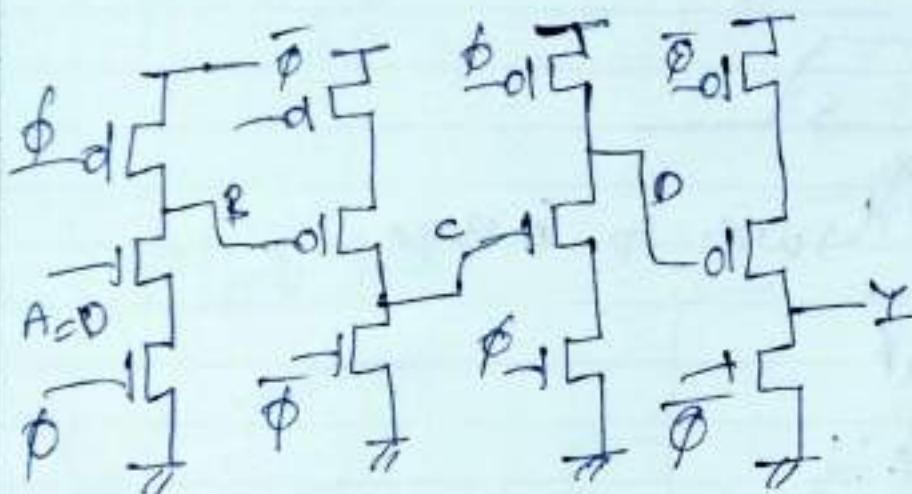
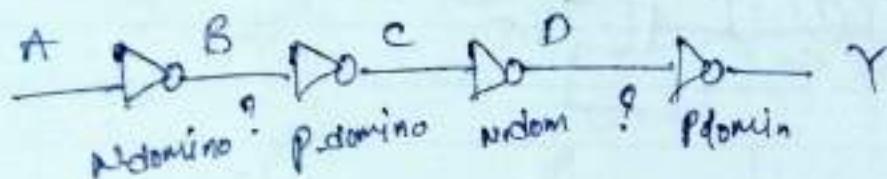
(non-inverting in nature)
always \rightarrow D-D-D





Evaluate parts has to be wide enough to accommodate all transition from all stages.

→ NP-DOMINO logic or NORA (NOT-ORAGE logic)

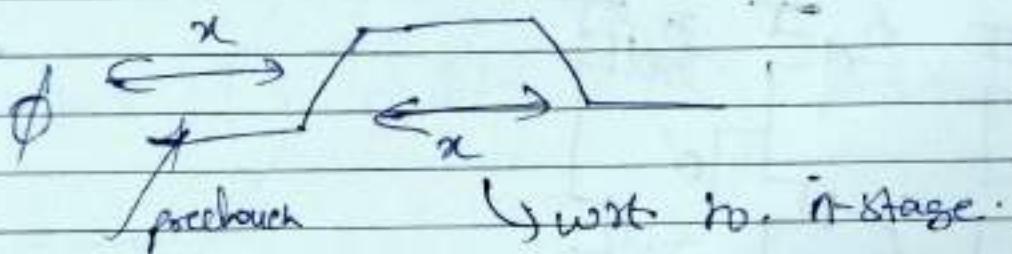
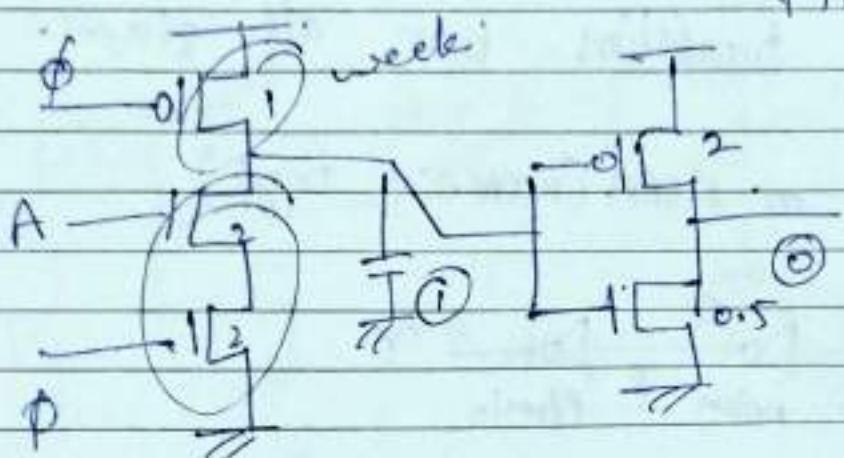


$A=0$
 $\phi=0, \bar{\phi}=1 \Rightarrow B=1, C=0, D=1, Y=0$ (Pre charge)

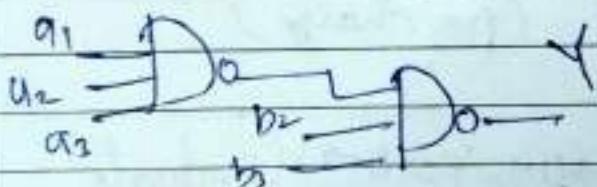
$A=1, \bar{\phi}=0; B=1 \rightarrow 0; C=0 \rightarrow 1; D=1 \rightarrow 0; Y=0 \rightarrow 1$ (Evaluate phase)

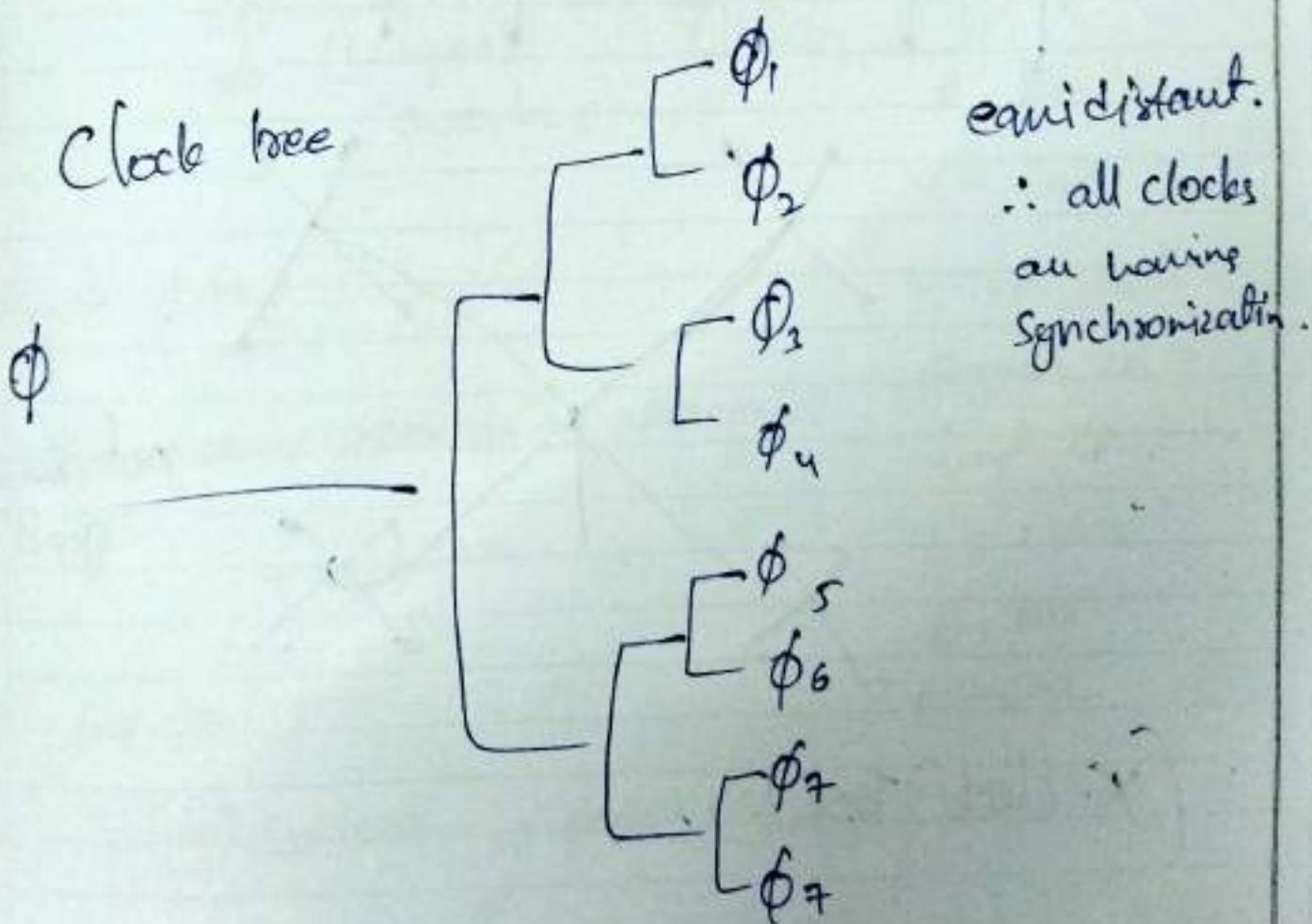
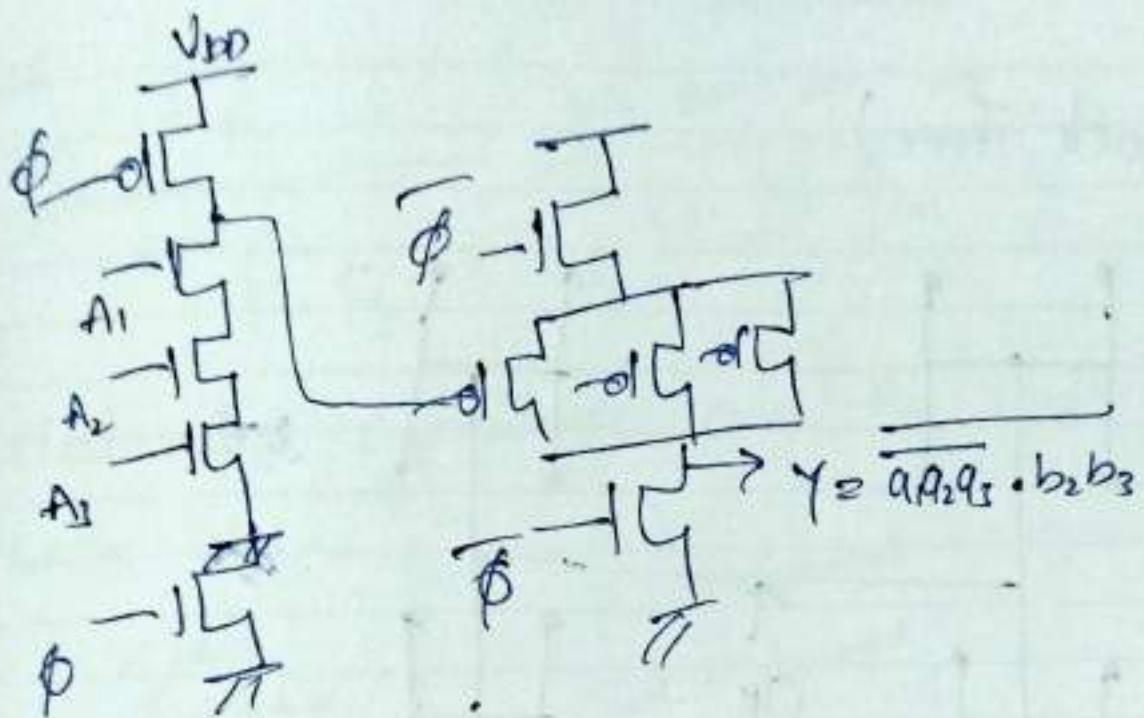
$A=0 \rightarrow 1$

Hiskewed inverter

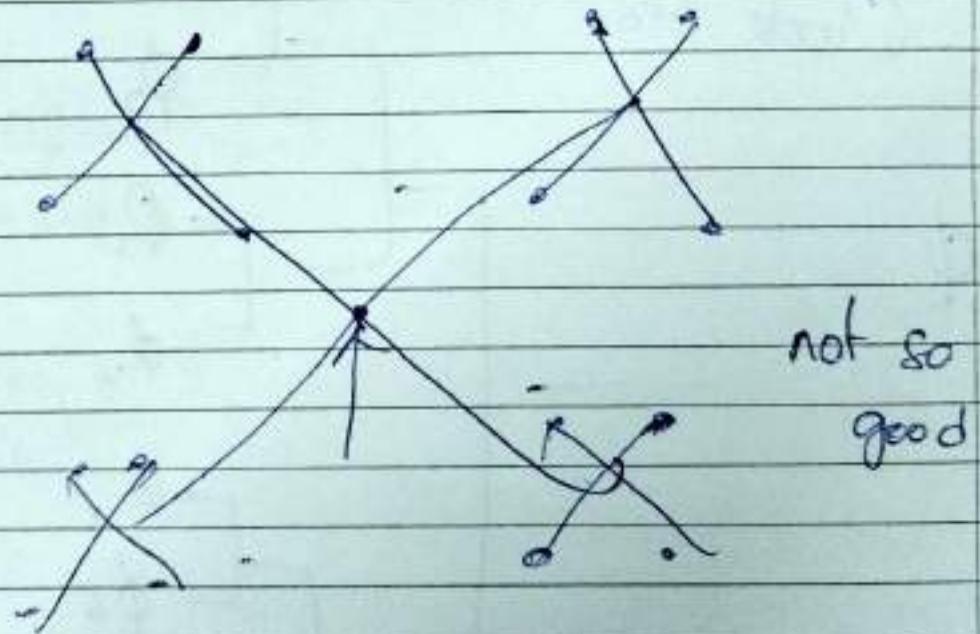
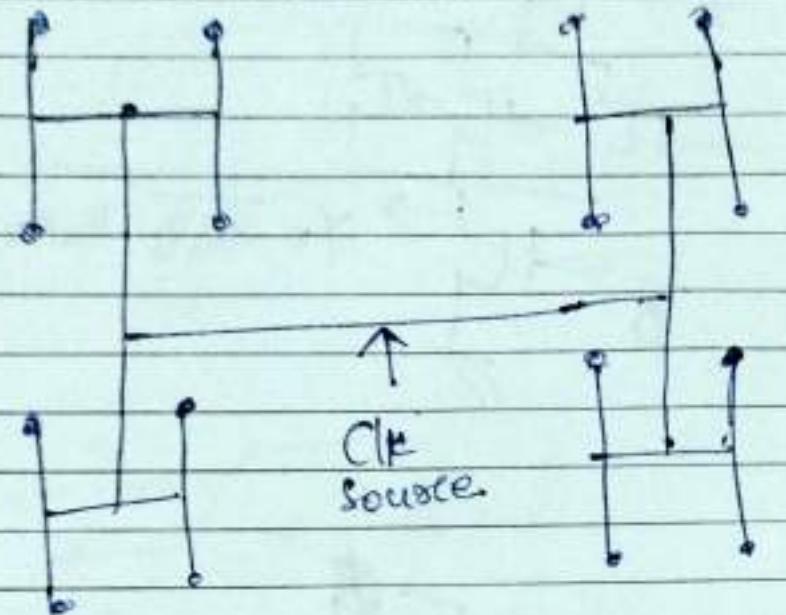


pmos has sufficient
time to close.



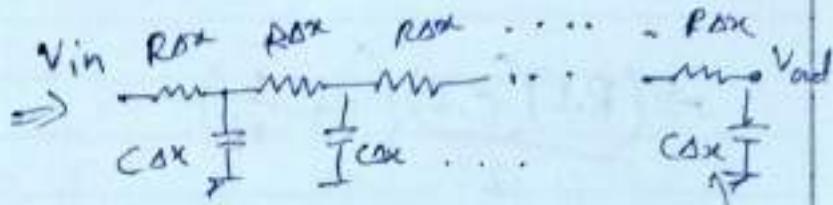
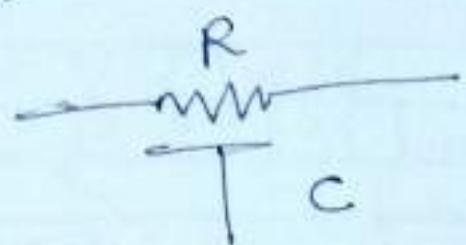


(A) clock Tree)

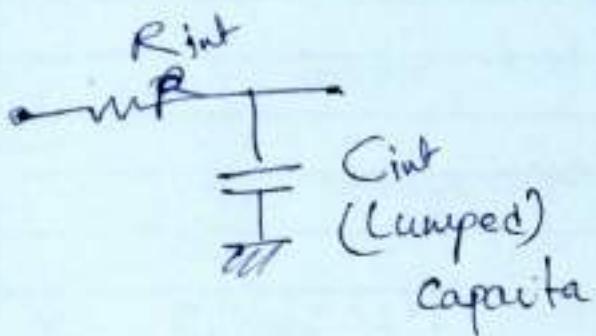


(X-clock Tree)

wire



distributed capacitance over the length of wire



R_{int} = L interconnect
 C_{int} = C interconnect

$$T = RC$$

$R = \text{Res/length}$
 $C = \text{Cap/length}$

Elmore delay.

N such small
segments of
length Δx

$$T = R_{ox} \cdot C_{ox} + 2R_{ox}C_{ox} + 3R_{ox}C_{ox} \\ \dots + NR_{ox}C_{ox}$$

$$L = N \Delta x$$

$$N \rightarrow R_{ox}$$

$$N \rightarrow C_{ox}$$

$$= R_{ox} \cdot C_{ox} (1 + 2 + \dots + N)$$

$$= \frac{N(N+1)}{2} R_{ox} \cdot C_{ox} \Rightarrow R_{ox} \cdot C_{ox} \cdot \frac{N \cdot N}{2} \left(1 + \frac{1}{N}\right)$$

$$\Rightarrow \frac{R(N\Delta x) \cdot C(N\Delta x)}{2} \left(1 + \frac{1}{N}\right)$$

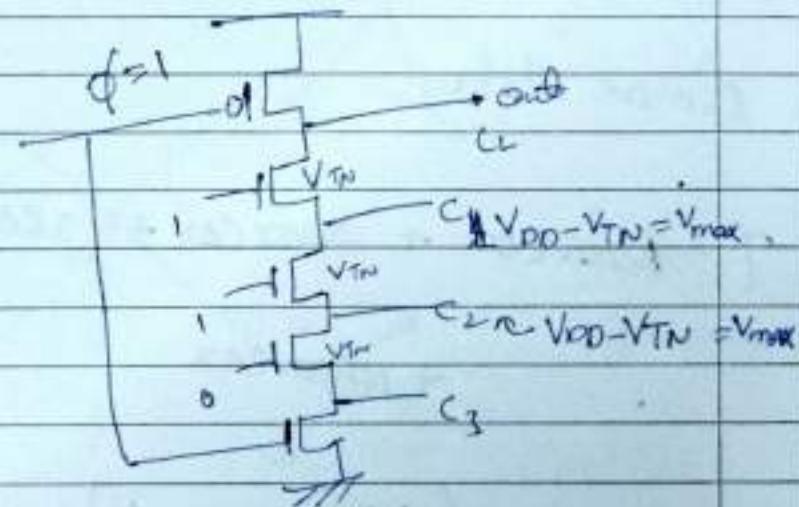
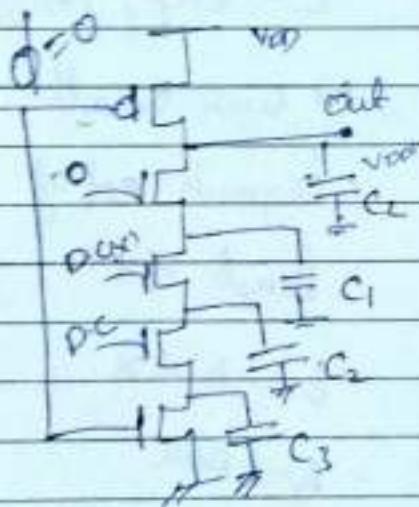
$$\Rightarrow \frac{(R \cdot L)(C \cdot L)}{2} \left(1 + \frac{1}{N}\right)$$

$$= \frac{RCL^2}{2} \left(1 + \frac{1}{N}\right)$$

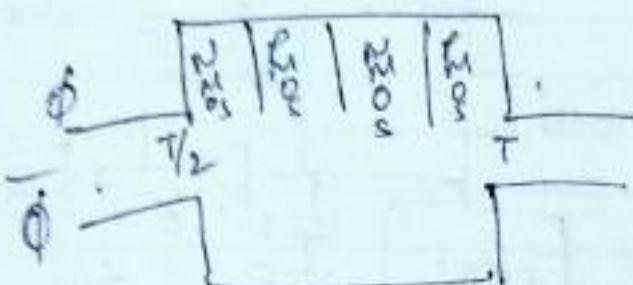
$$r_{N \rightarrow \infty} = \frac{RCL^2}{2} = \frac{(RL)(CL)}{2} \quad T \propto L^2$$

$$= \frac{R_{int} C_{int}}{2}$$

Date: Nov 24

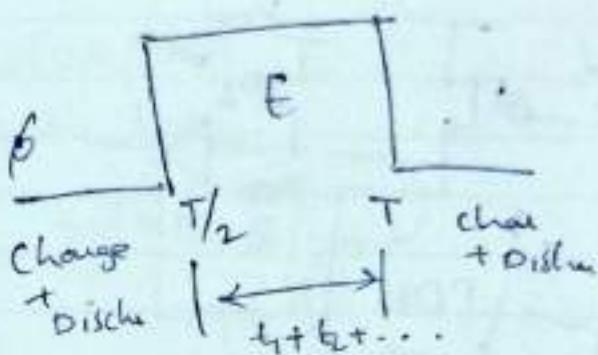


NORA logic



$$\frac{T_{\phi}}{2} \geq t_{F1} + t_{F2} + t_{M1} + t_{M2} + \dots$$

Domino logic



Assume C_1, C_2, C_3 are initially discharged.

$\rightarrow Q = V_{DD}C_L$ Assume that after charge sharing

$V_f = \text{Voltage across all the capacitors}$

$$C_L V_{DD} = C_L V_f + C_1 V_f + C_2 V_f$$

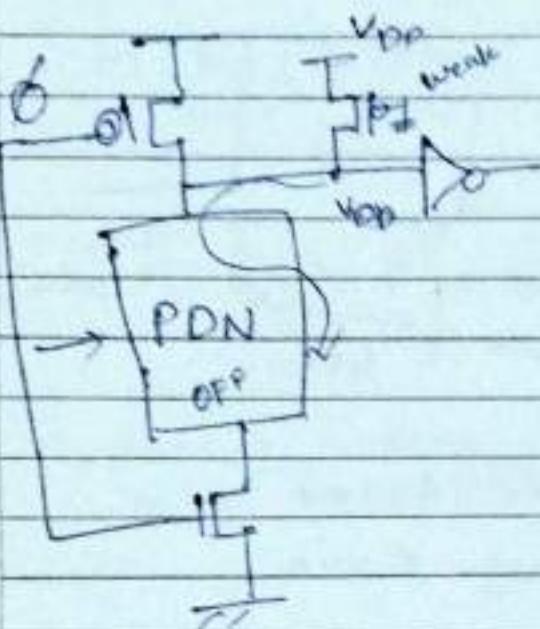
$$V_f = \frac{C_2}{C_L + C_1 + C_2} V_{DD} \quad (L \ll V_{DD})$$

$(C_1 + C_2) \ll C_L$

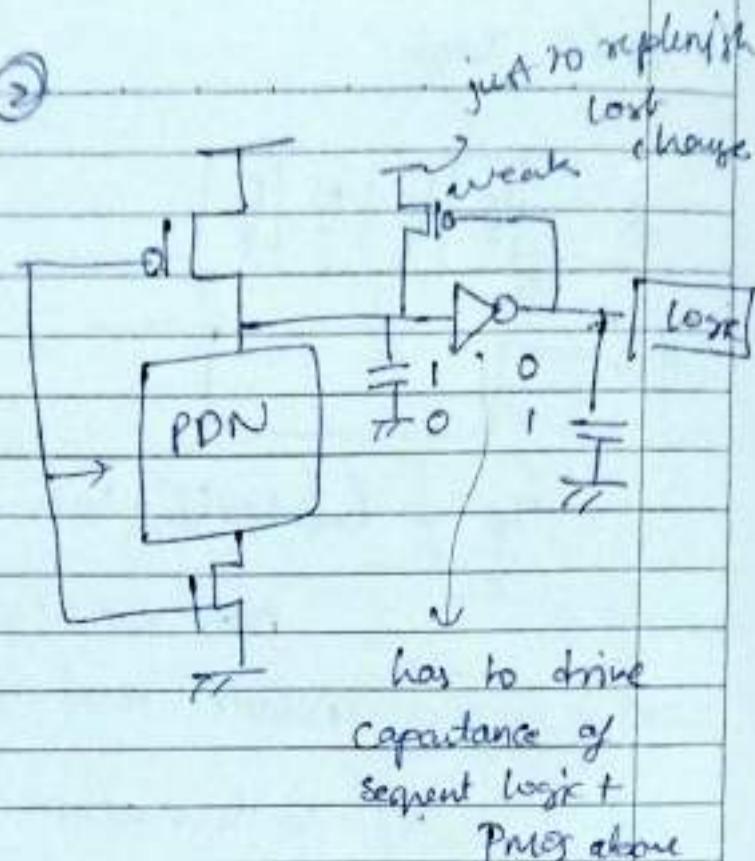
To obtain
 C_L value
because $L \ll V_{DD}$.

* Charge sharing

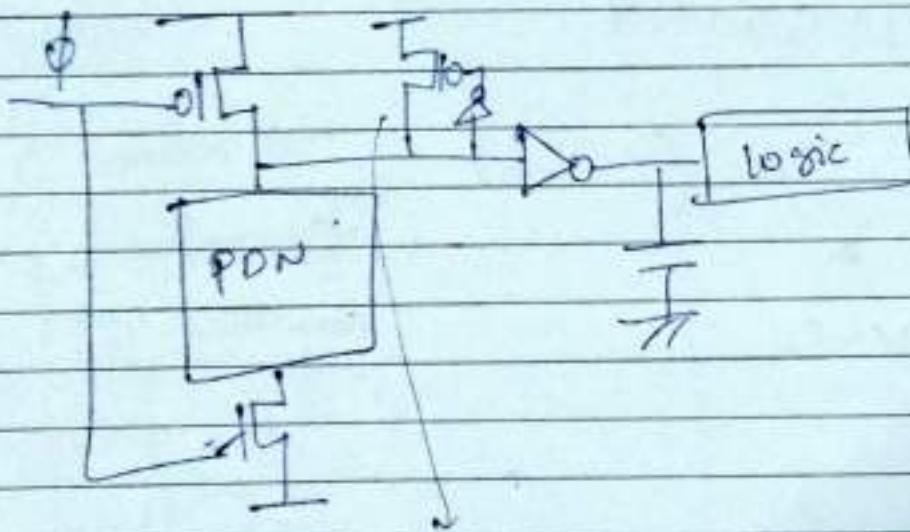
①



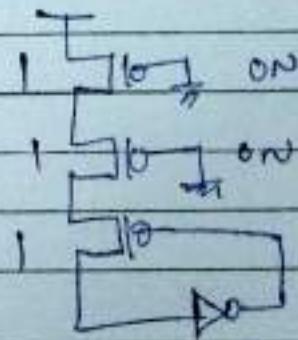
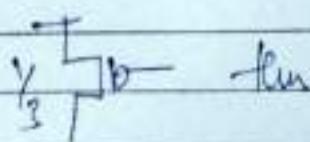
②

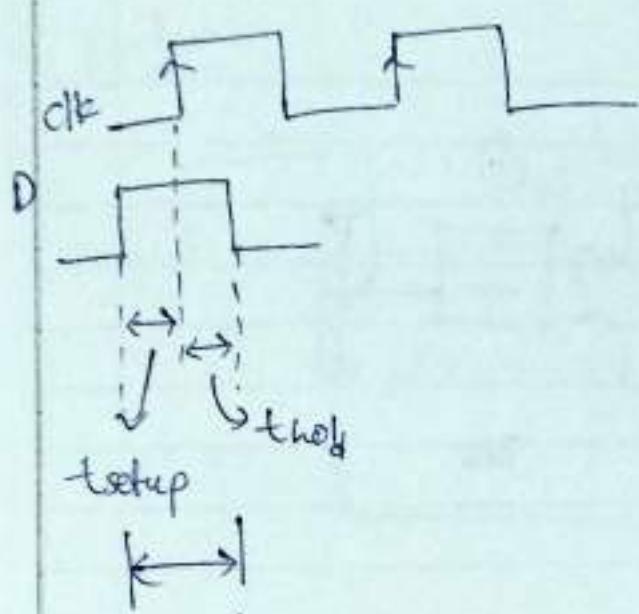


③



it

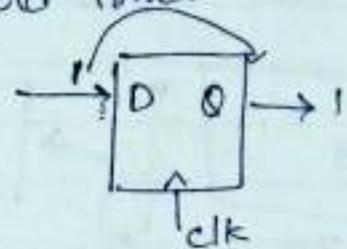




Latch : level
→ flip flop : edge

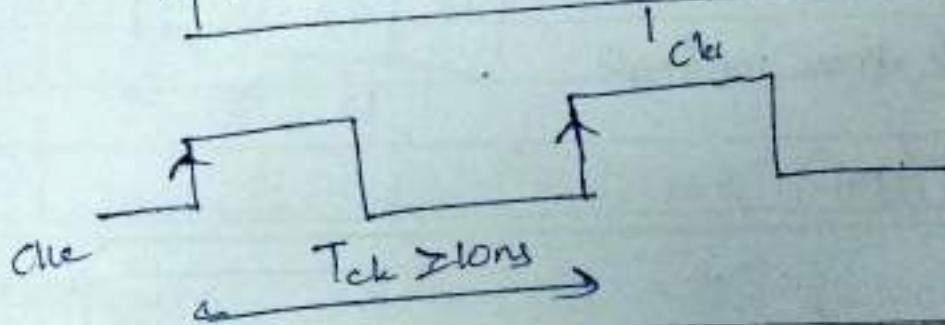
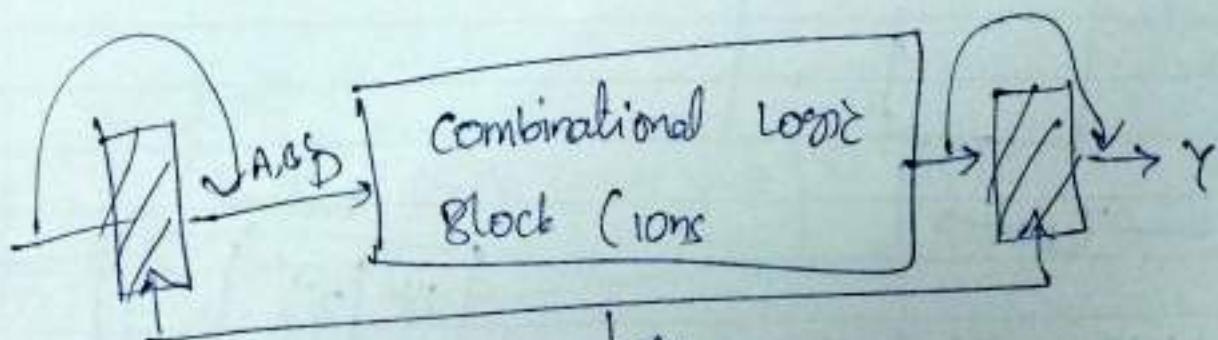
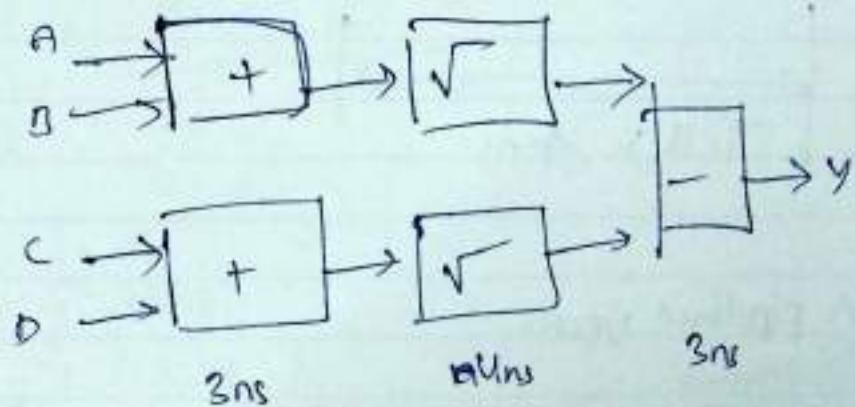
Setup time

Hold time.



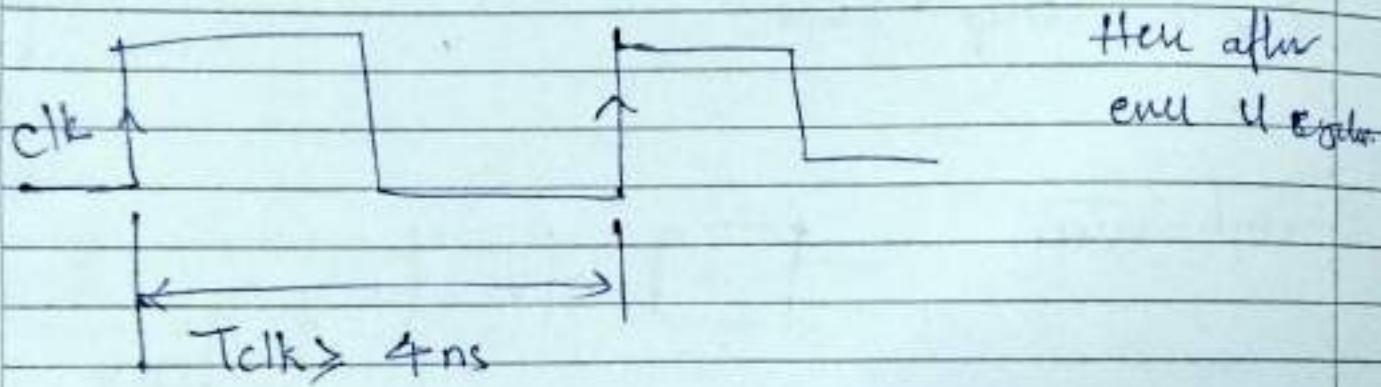
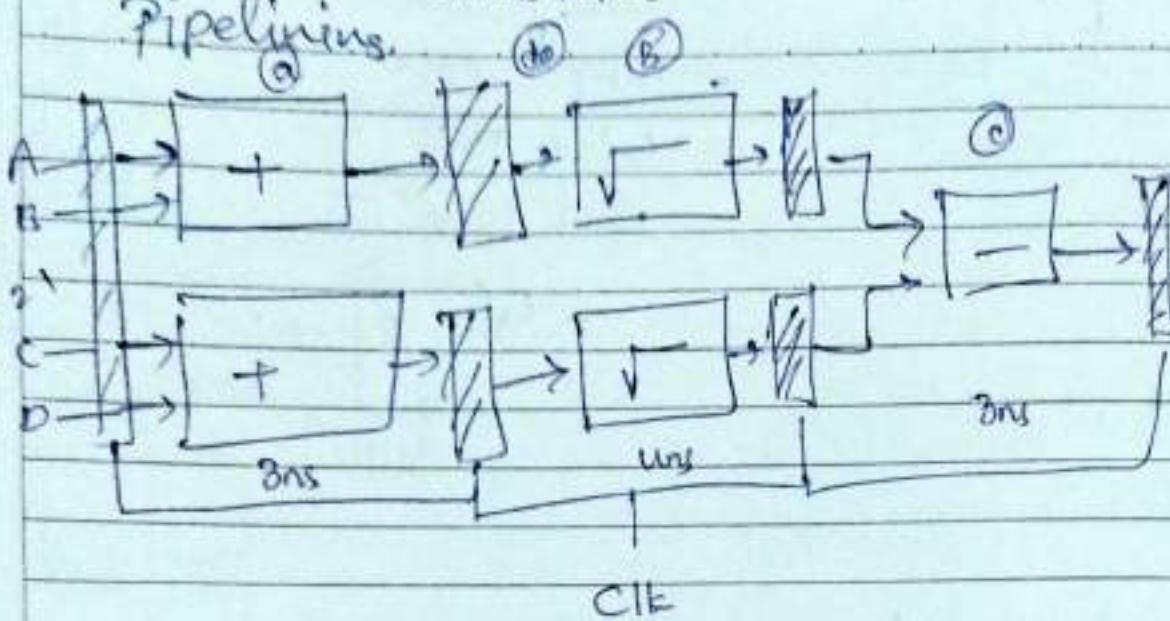
$$\text{Time } t_a = t_{\text{setup}} + t_{\text{hold}}$$

$$Y = \sqrt{A+B} - \sqrt{C+D}$$

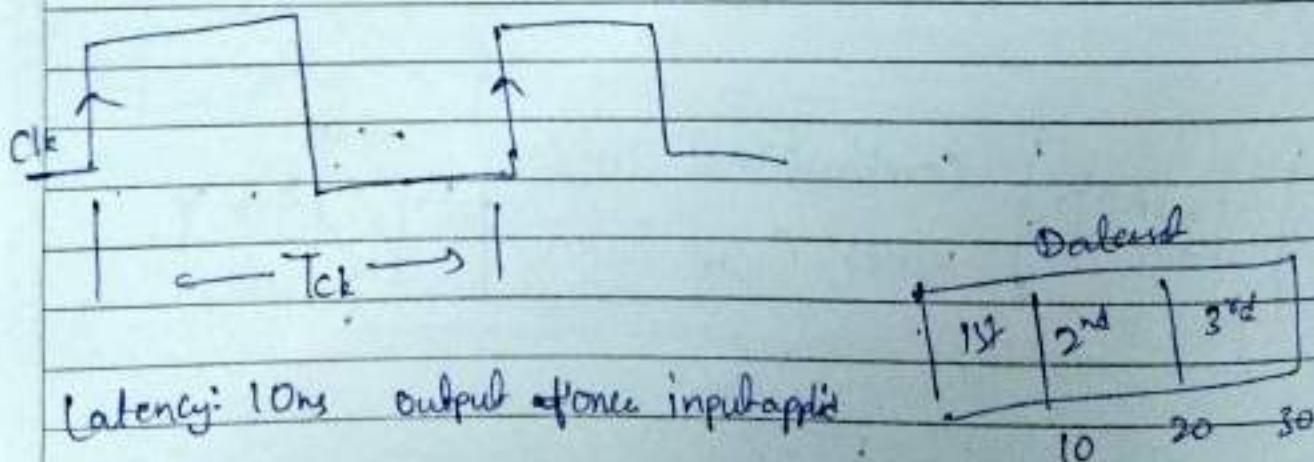


Pipelining

Teacher's Signature



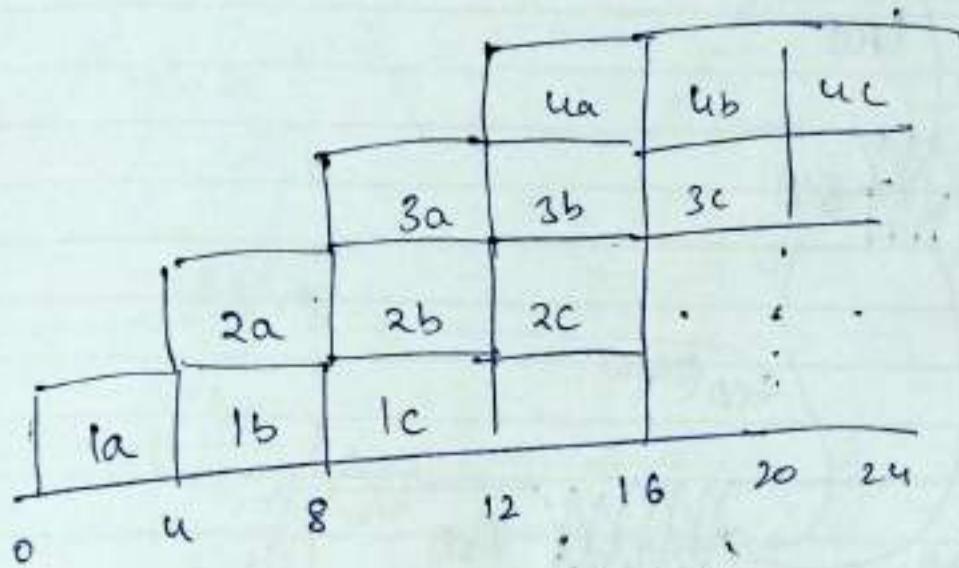
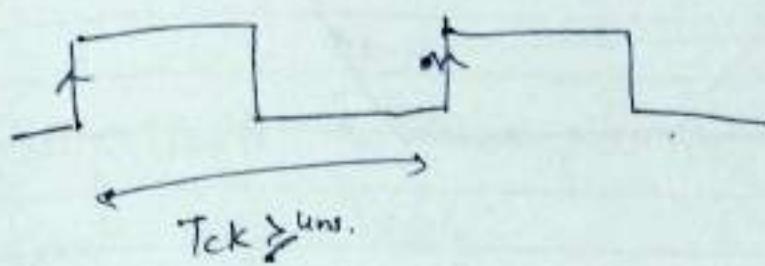
non pipelined version



Latency: 10ns output once input applied

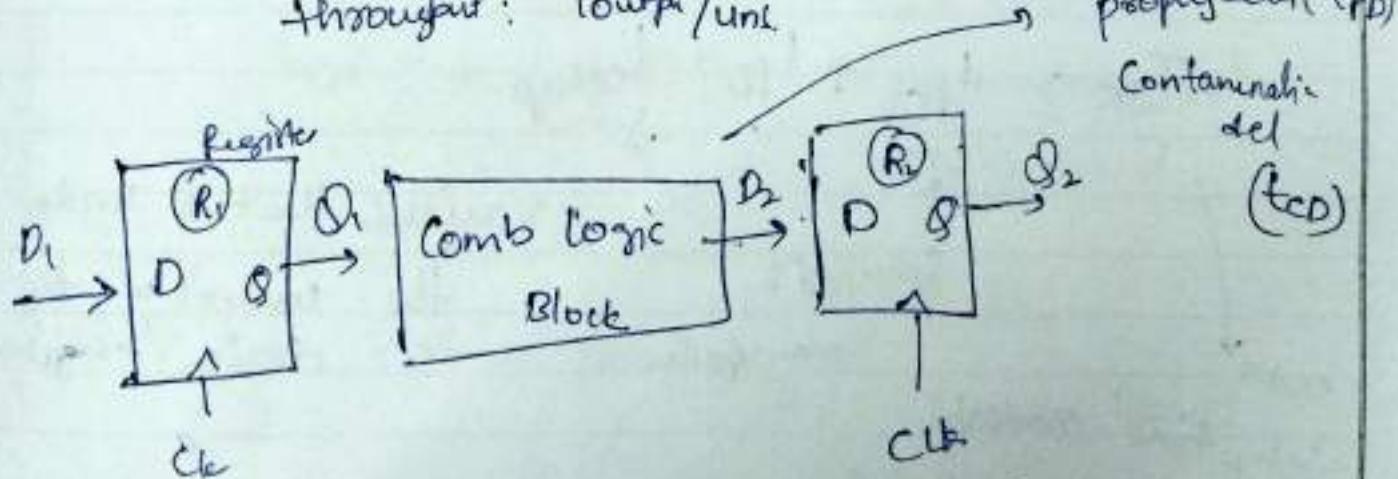
Throughput: 1 output / 10ns

Pipeline



Latency: 12ns

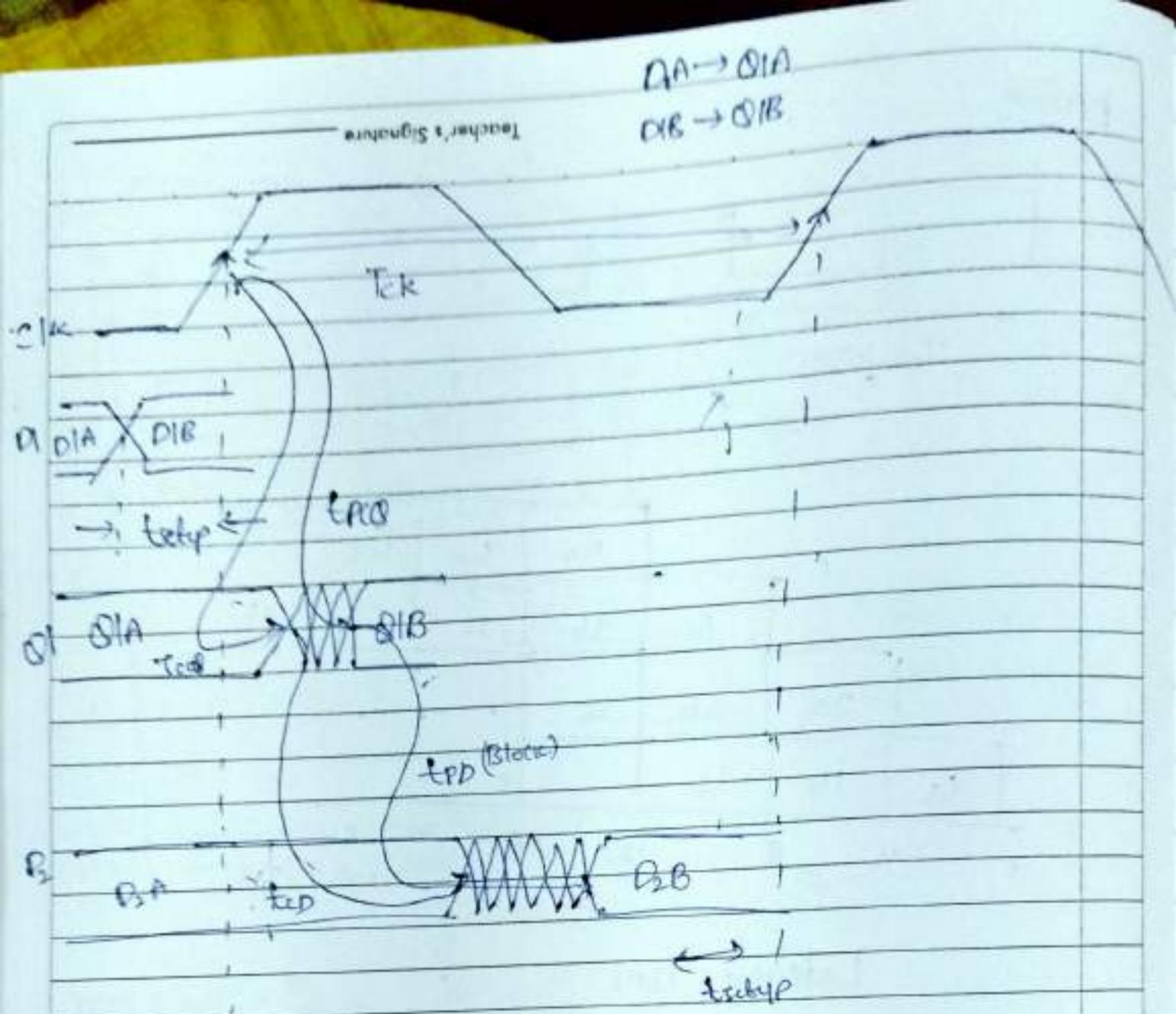
throughput: 1 output/unit



contamination delay (clock to Q) (t_{CO})

propagation delay (clock to Q) t_{PD}

propagation delay to Q



$$TAK \geq t_{PCQ} + t_{PD} + t_{\text{setup}}$$

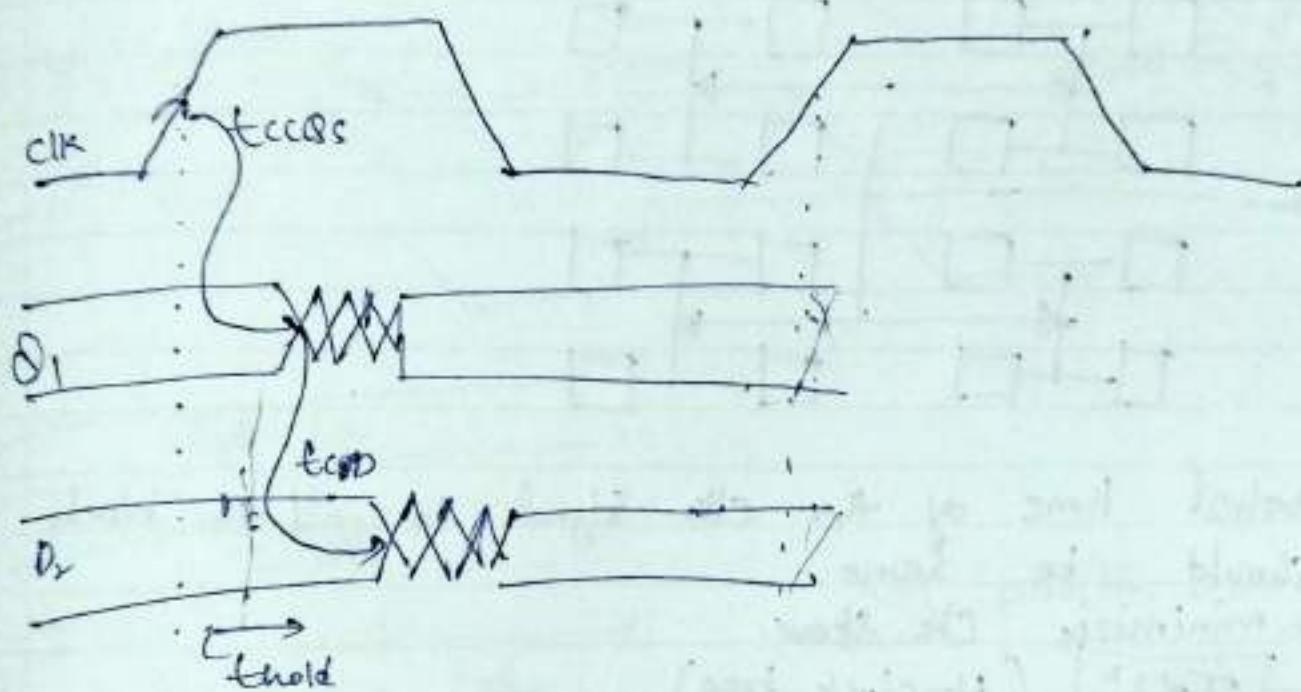
t_{PCQ} \uparrow Variable that is under
specified by manufacturer \rightarrow the control of the
design engineer

Setup time constraint
max delay constraint.

$$t_{PD} \leq T_{ck} - (t_{setup} + t_{PCQ})$$

~ sequencing overhead.

t_{setup} limit the max permissible delay through the comb logic block.



$$\text{to } t_{ccqs} + t_{CD} \geq t_{hold}$$

hold time constraint

$$t_{CD} \geq t_{hold} - t_{ccqs}$$

or minimum delay constraint

Setup time violation (by changing T_{ck})

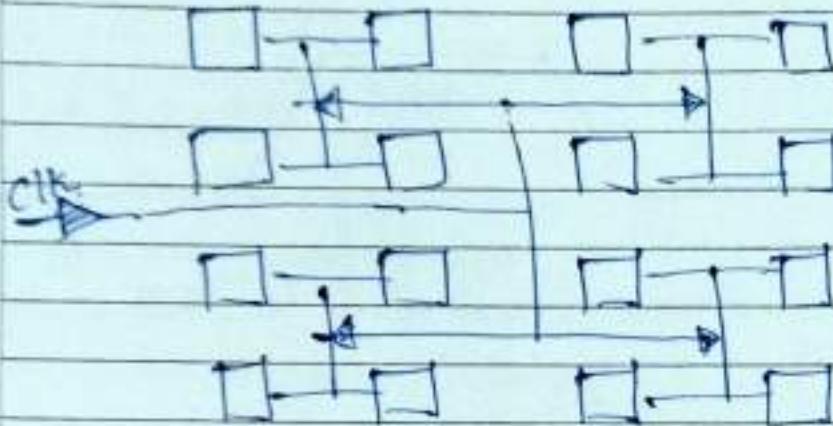
Hold time violation (everything)

(Rabey
Weiste Harris)

Misins.. S(Nov)

S(Nov) 24

Clock Skew: Spatial variation in arrival time of clock transition.

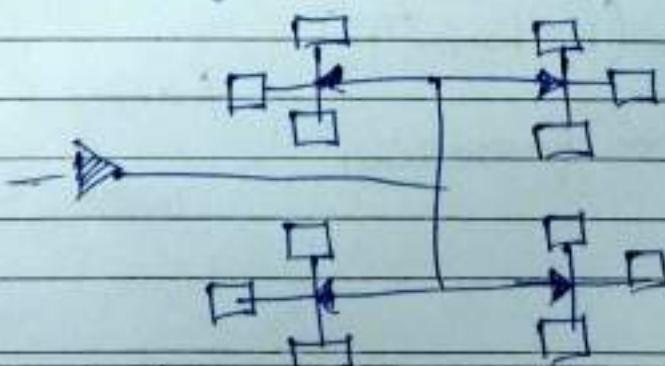


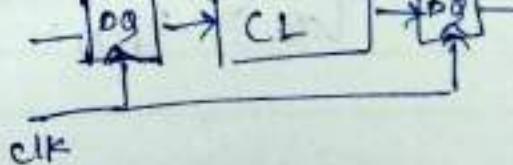
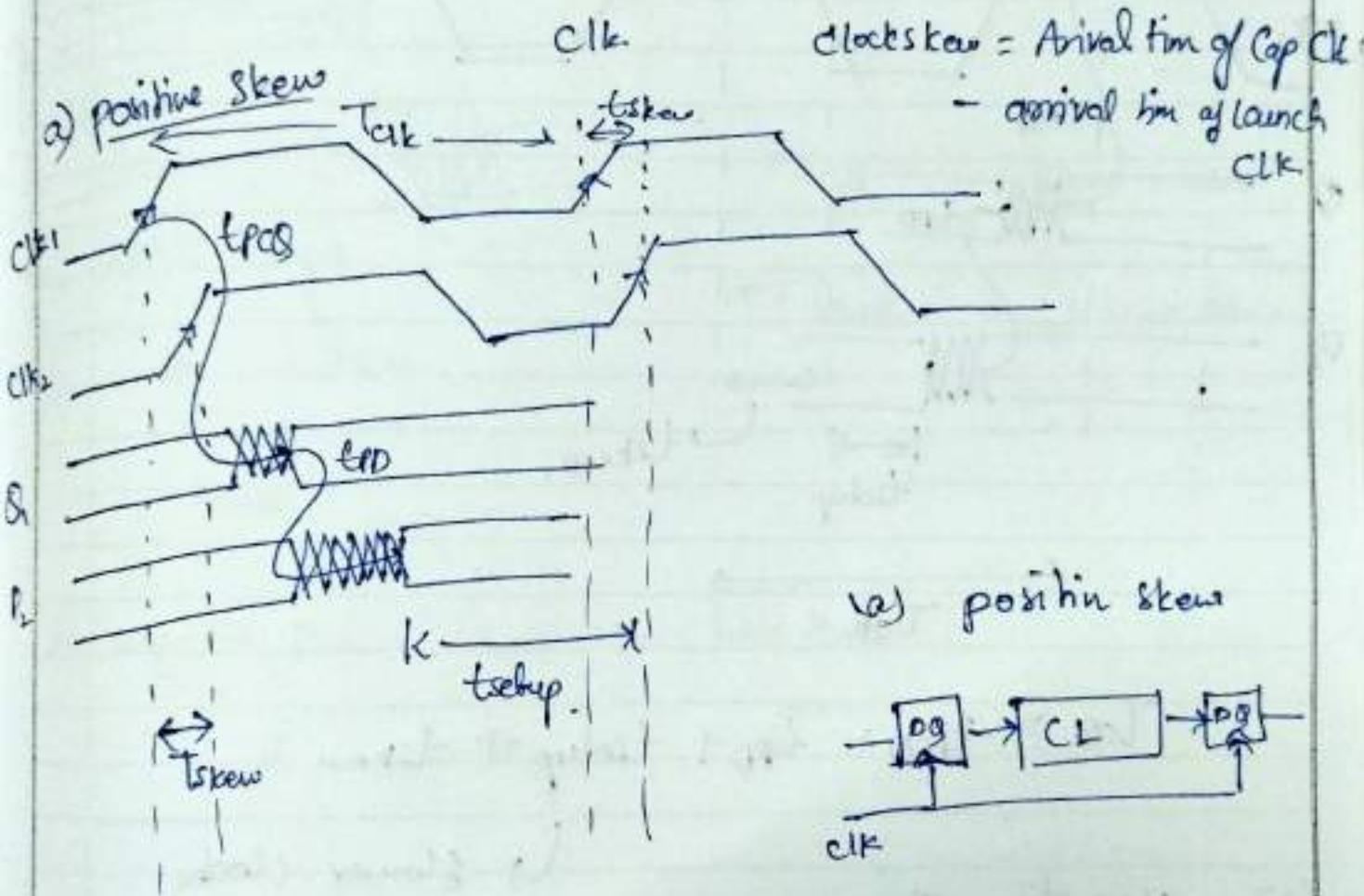
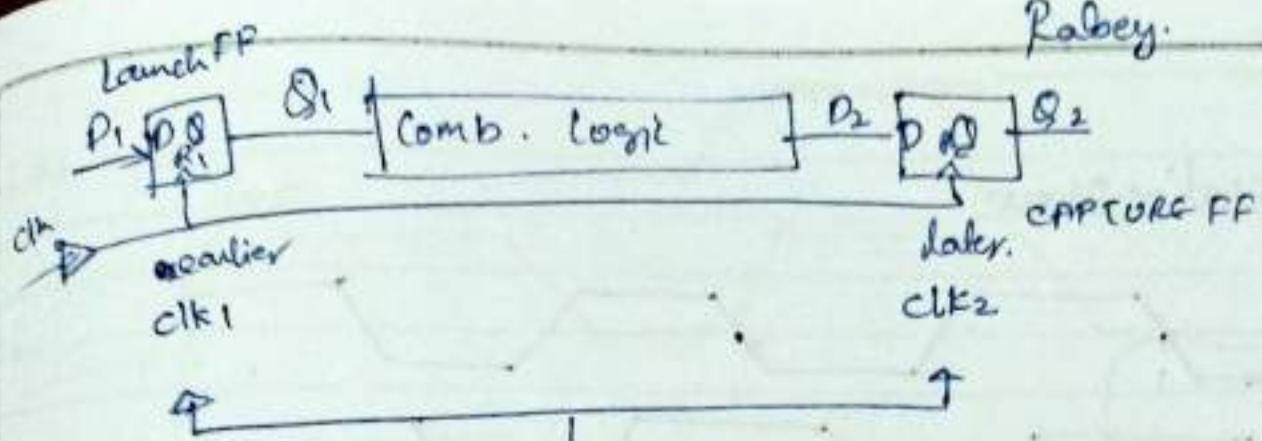
Arrival time of the clk signals to all the blocks
should be same

⇒ minimizing clk skew.

$$T \propto L^2 \quad (\text{H-clock tree})$$

If we need only 12 destination block remove
4 blocks symmetrically w/o load capacitor
w/mish varies





$$T_{CK} + t_{Skew} \geq t_{PCQ} + t_{PD} + t_{Setup}$$

$$T_{CK} \geq (t_{PCQ} + t_{PD} + t_{Setup} - t_{Skew})_B$$

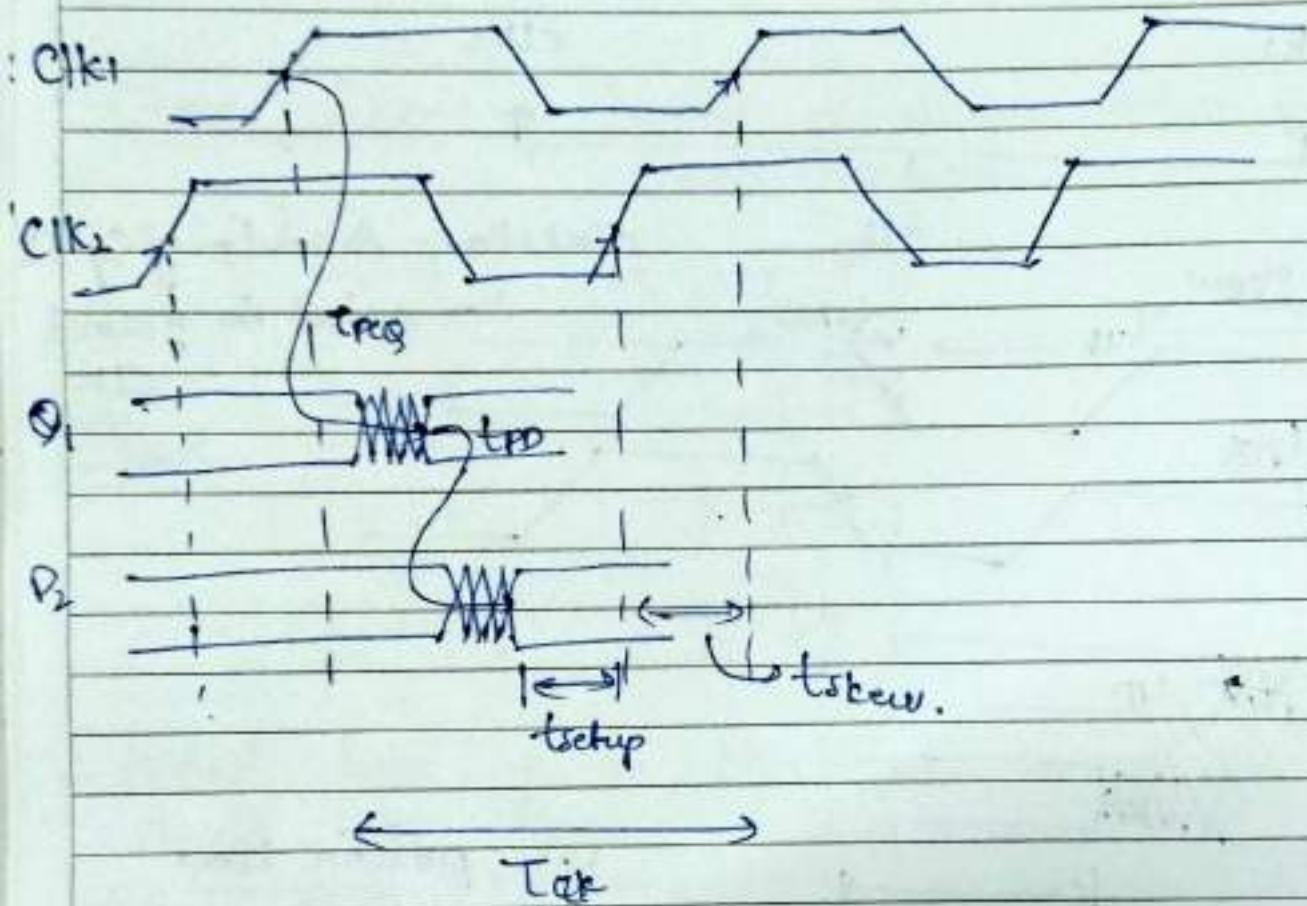
when CLK skew was absent.

$$T_{CK} \geq (t_{PCQ} + t_{PD} + t_{Setup})_A$$

$$A > B$$

$\therefore t_{Skew}$ enables us for faster.

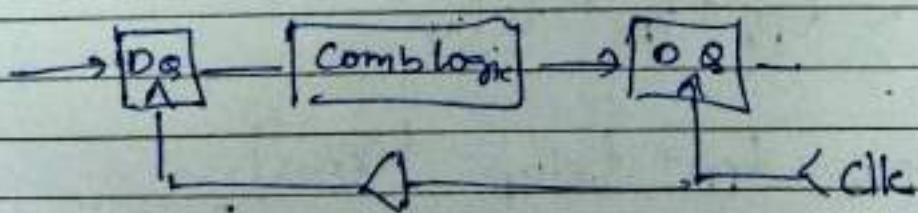
(b) Negative Skew.



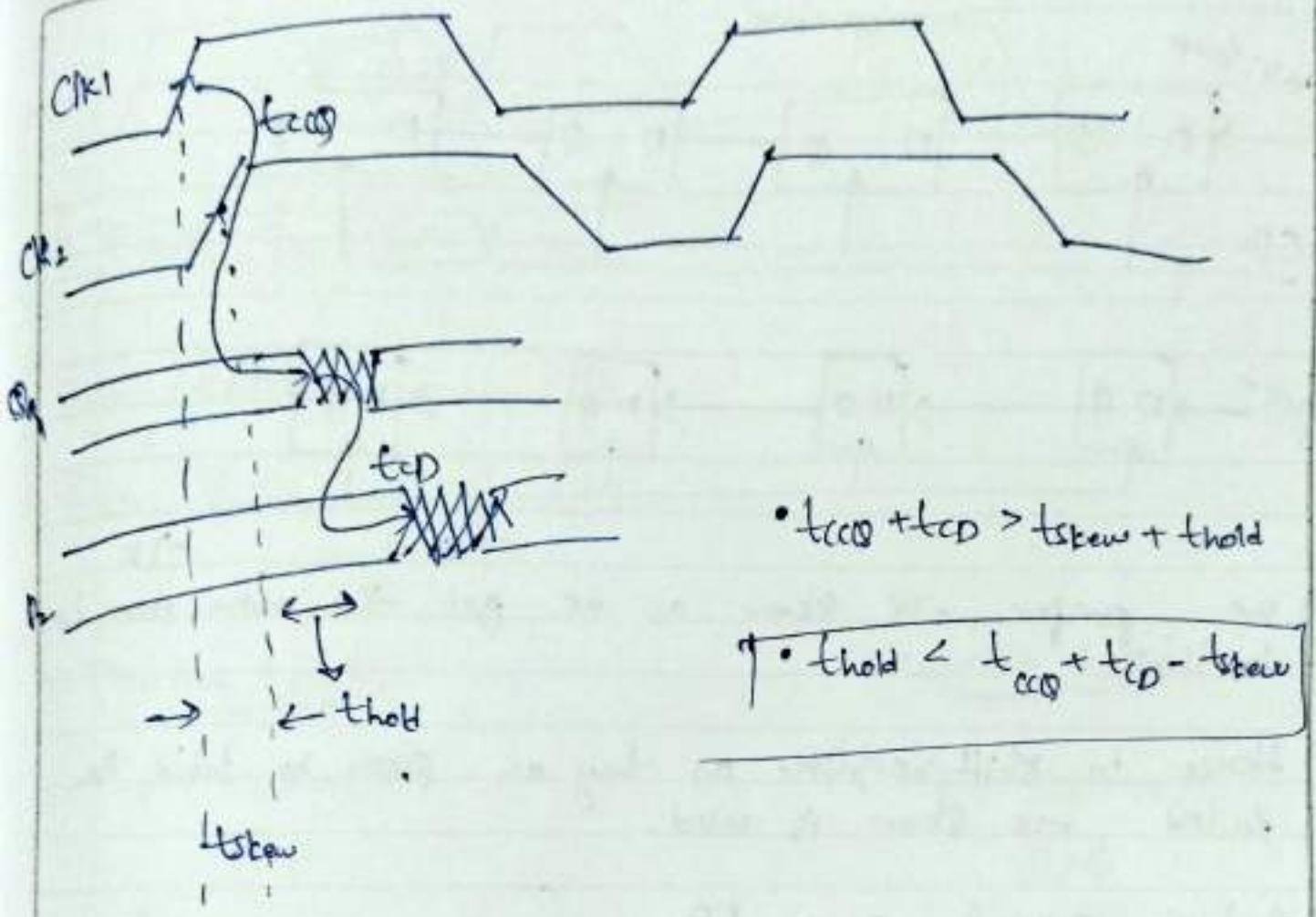
$$T_{clk} \geq t_{pd} + t_{pd} + t_{setup} + t_{skew}$$

↳ slower clock

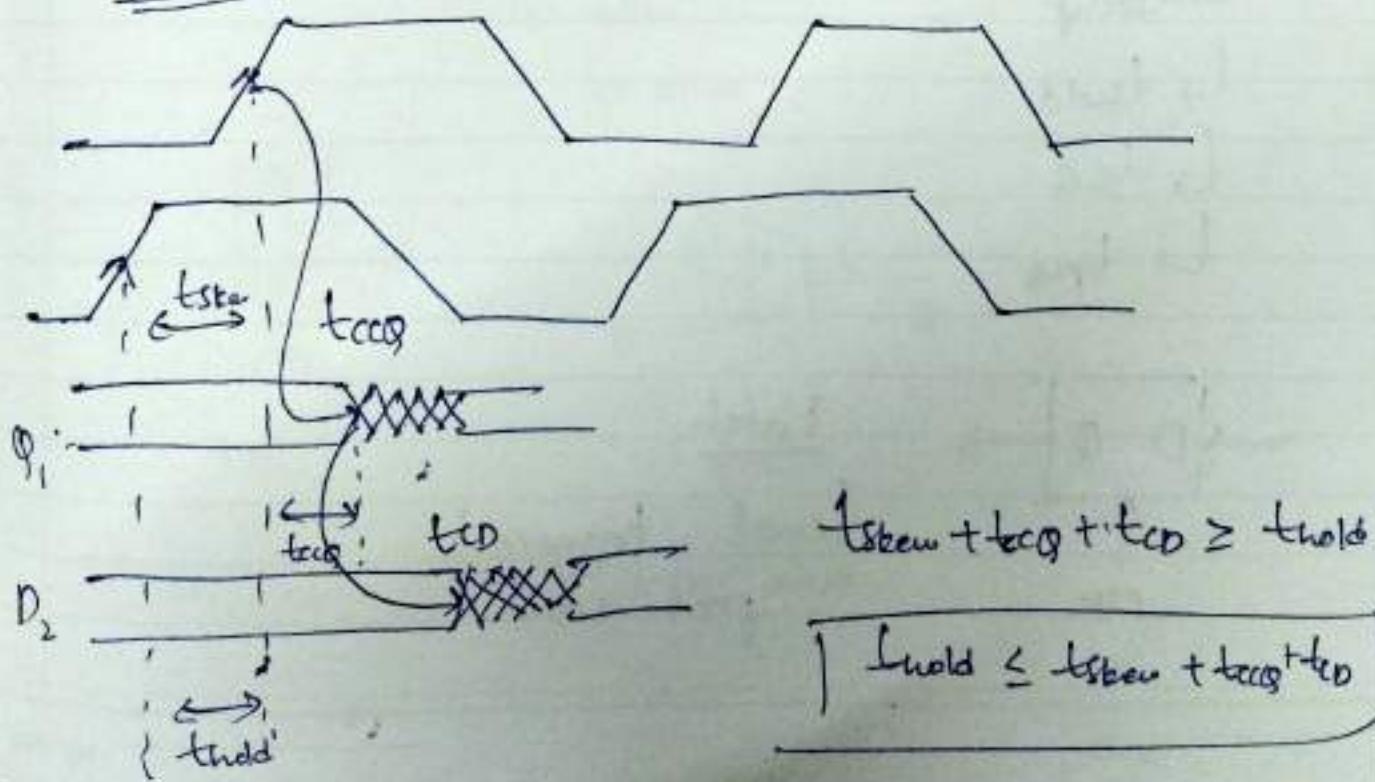
(b) Negative Skew



Data and Clk Signal are opp to each other

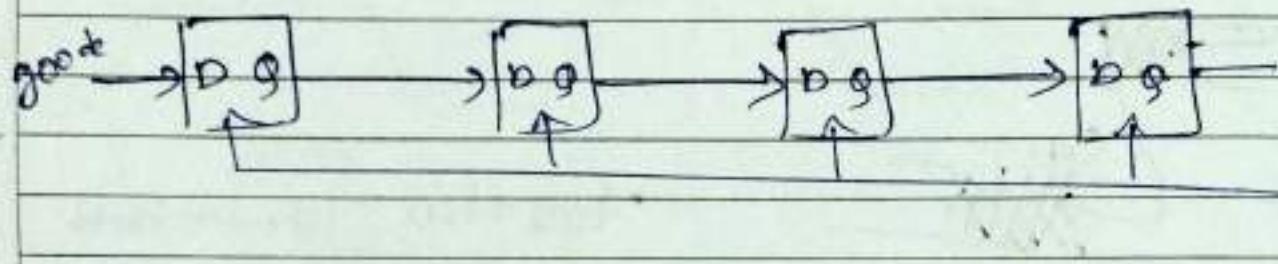
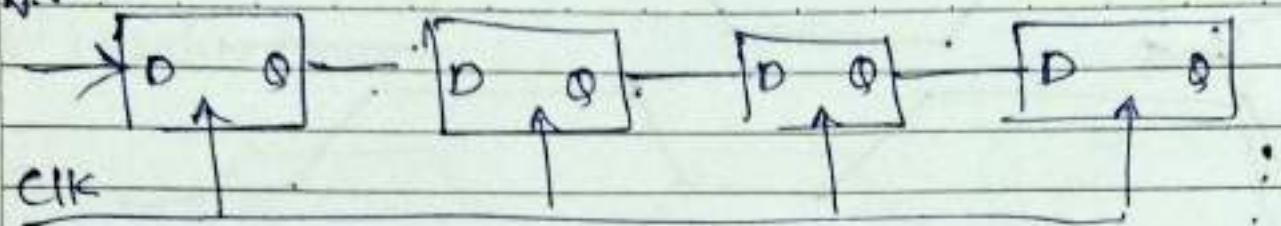


@ negative skew (need for hold time)



N.V. Jimp

Teacher's Signature



'CLK

→ We prefer +ve skew as we get the more room for
to hold

→ Hence in shift register as they are prone to hold time
failures, +ve skew is used.

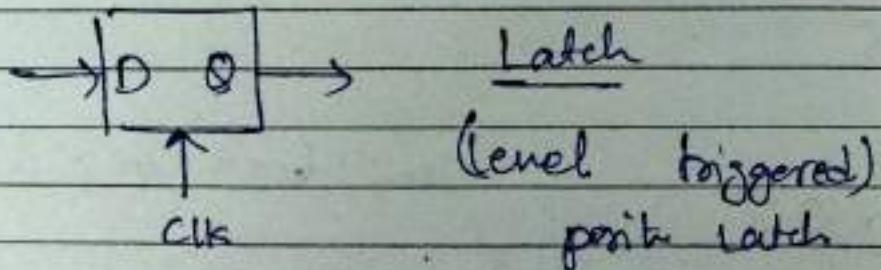
Intrinsic property of a FF.

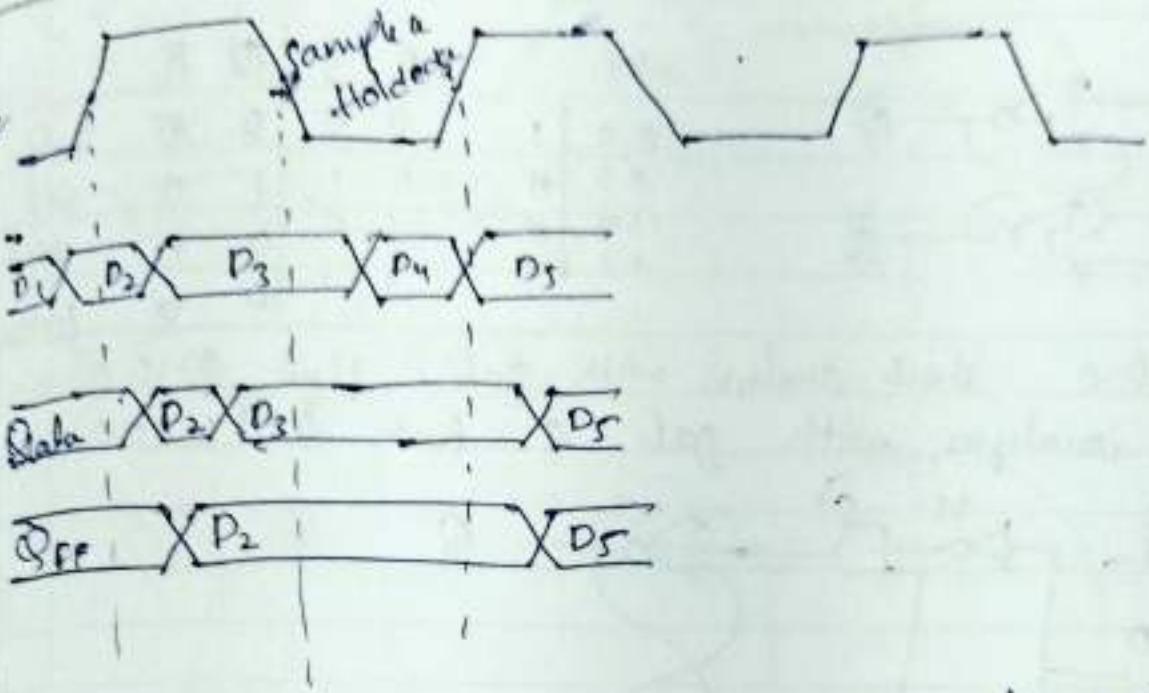
↳ t_{setup}

↳ t_{hold}

↳ t_{aco}

↳ t_{pcq}





positive latch

if ($clk == 1$)

$$Q = D$$

else

$$Q = Q$$

negative latch

if ($clk == 1$)

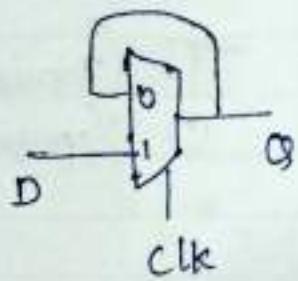
$$Q = Q$$

else

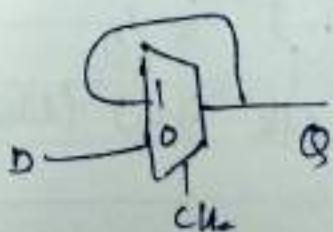
$$Q = D$$

if else

↳ mux.

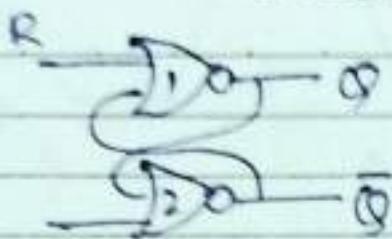


+ve



(-ve)

Latch using mux

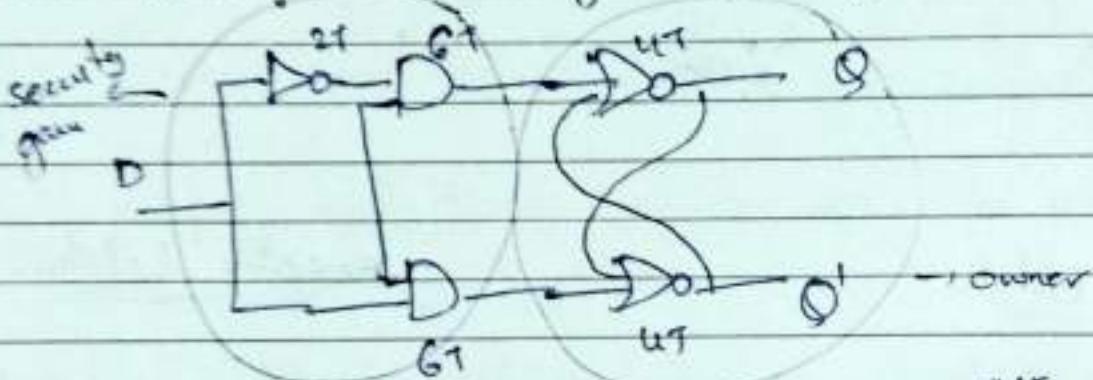


R	S	NOR	R	S	Q	\bar{Q}
0	0	1	0	0	0	1
0	1	0	0	1	1	0
1	0	0	1	0	0	1
1	1	0	1	1	0	0

forbidden

$R=0, S=0$ start analysis with gate 1 first $Q=1; \bar{Q}=0$

start analysis with gate 2 first $\bar{Q}=1; Q=0$

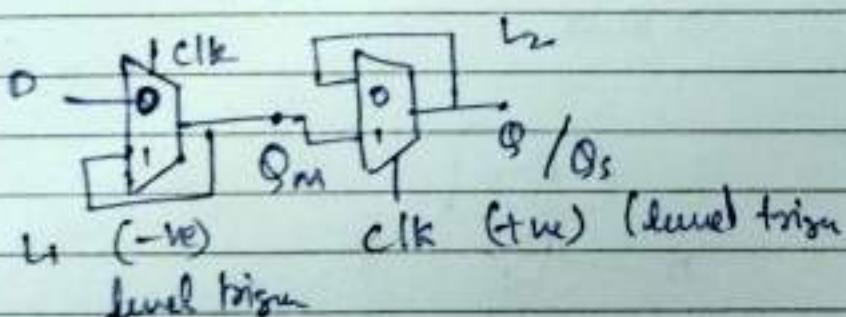


Takes more area on silicon chip bad design ^{VLSI}

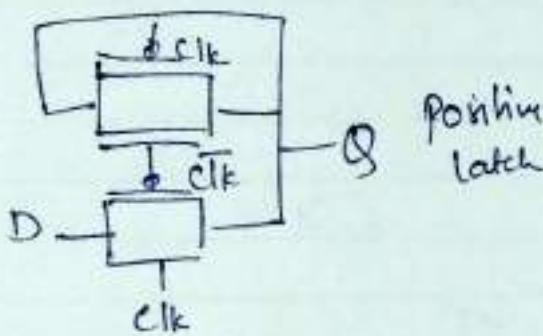
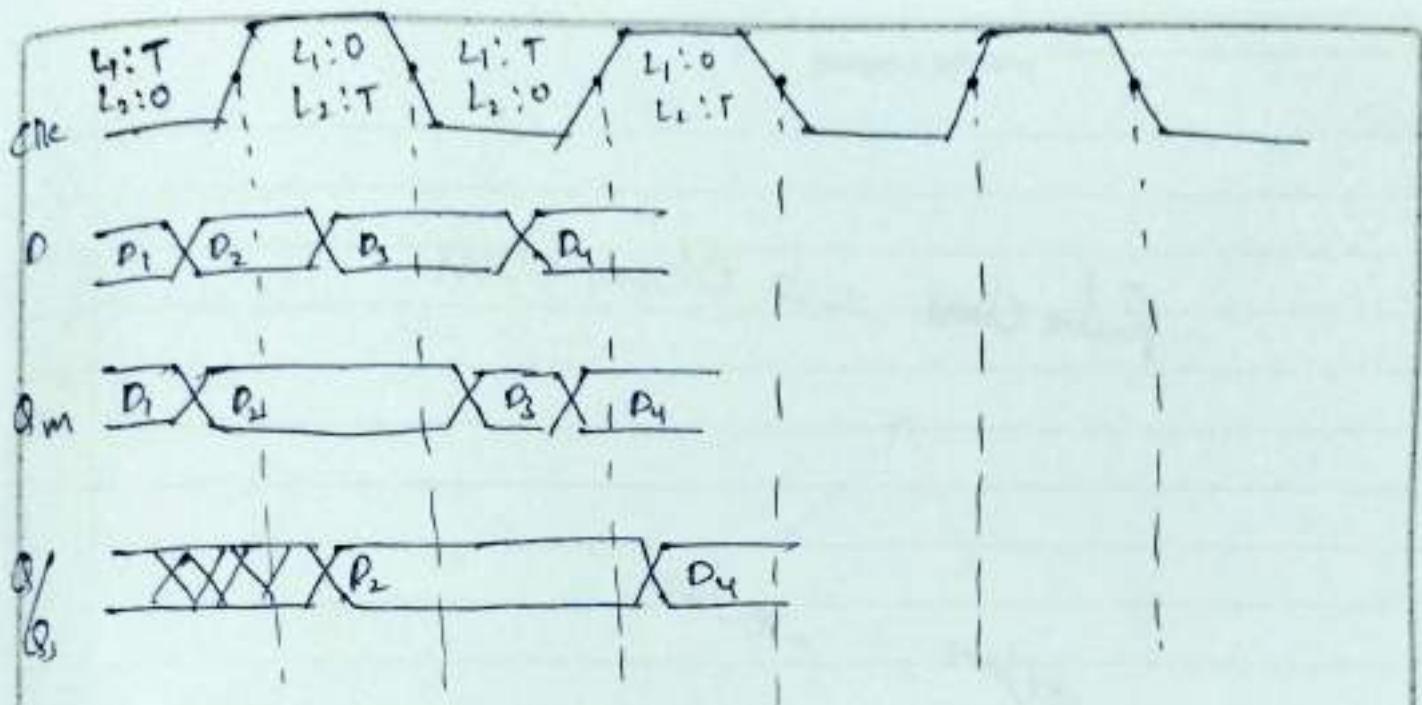
Positive edge triggered FF

Master-slave Configuration

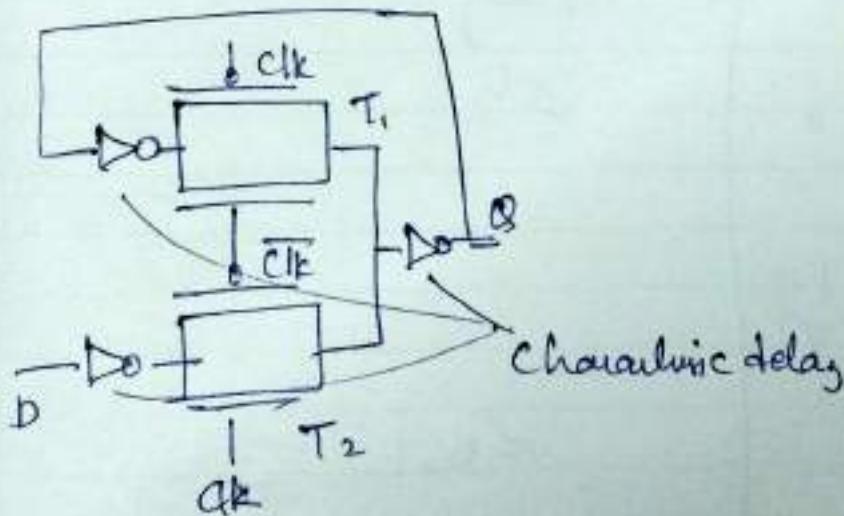
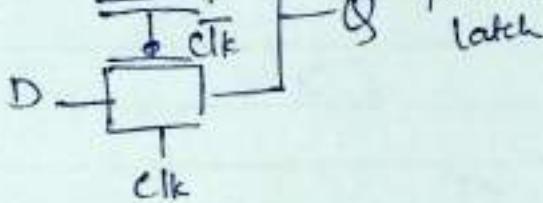
latch latch
low level high level



\square (Transparent)
 \circ (opaque)



Here we don't know V_{dd} or L_{min} to calculate delay

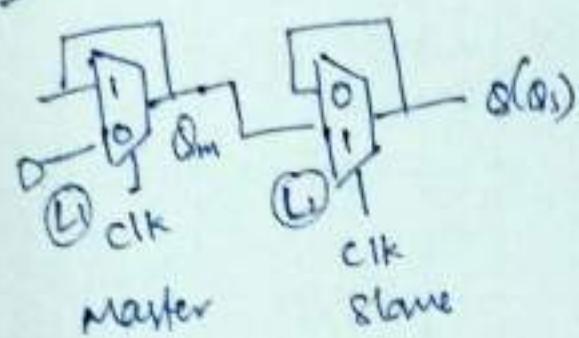


$Clk=1$ T_2 is on
 T_1 is off.

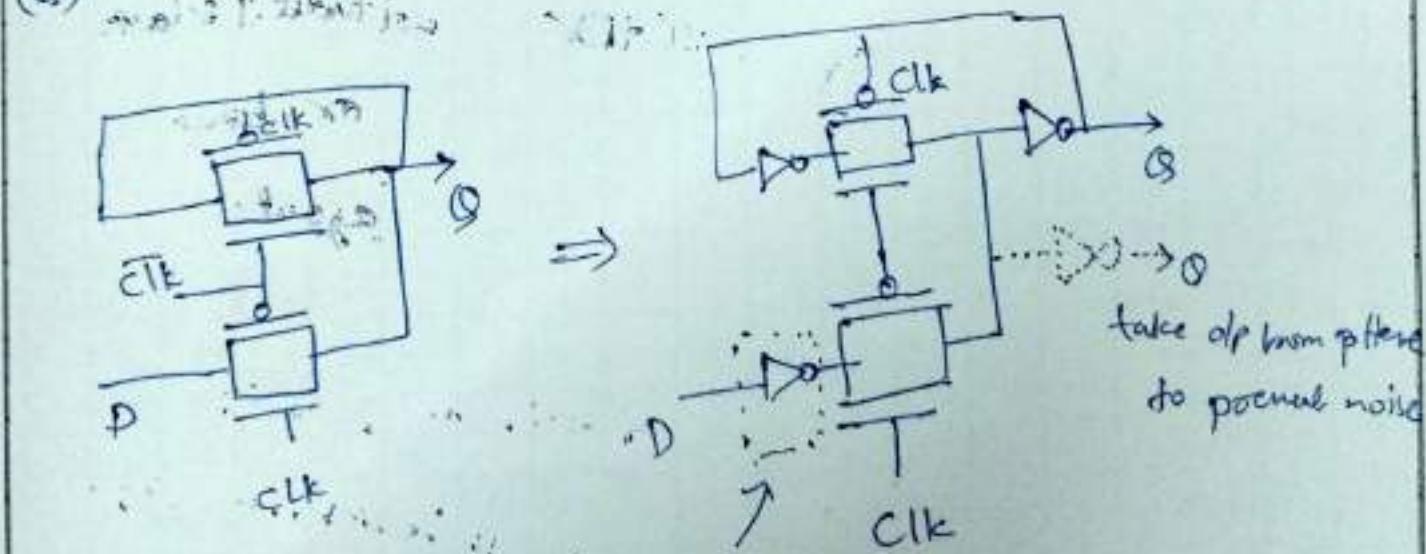
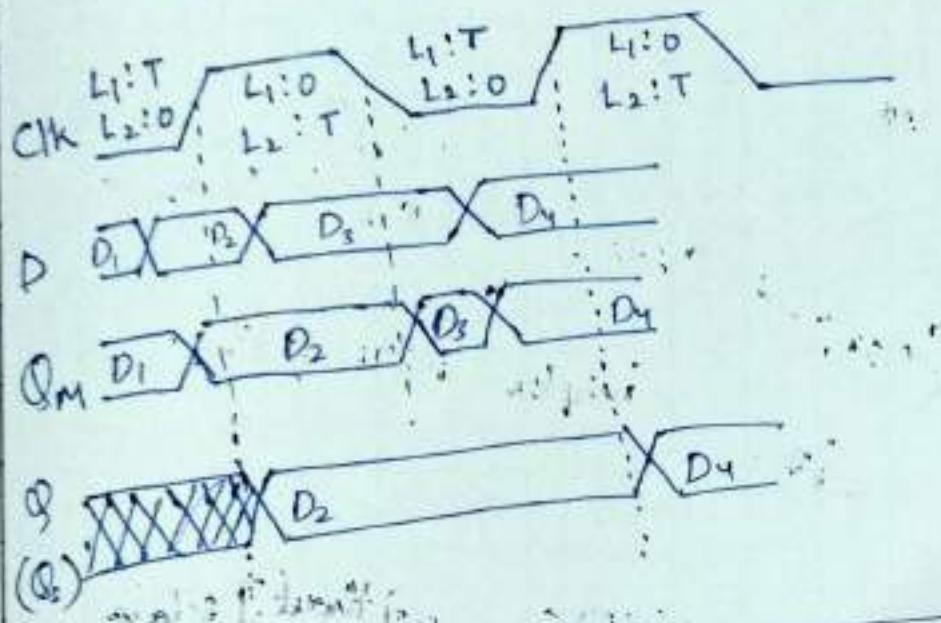
$Clk=0$ T_2 is off
 T_1 is on

9/Nov/24

Reap



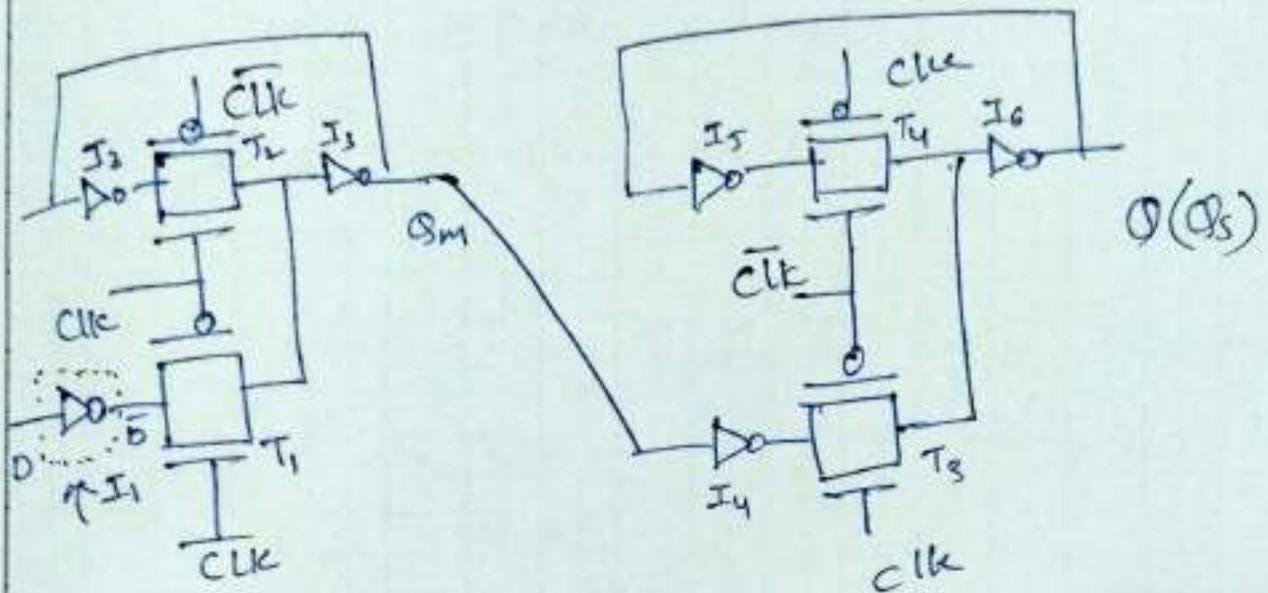
T = transparent
O = opaque



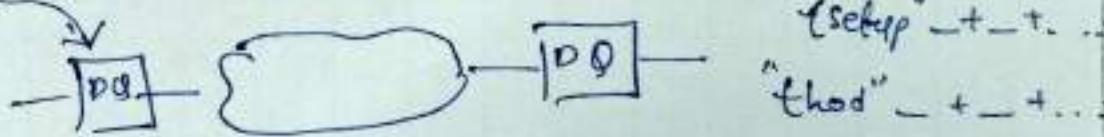
This inverter isolates i/p D from the latch

* provides a constant i/p load for the latch (so that the latch delay can be characterized)

* provides noise immunity to the internal nodes of the latch from i/p.



master-slave "t_{edge}" triggered ckt.



$$\textcircled{1} \quad \bar{\text{CLK}} = 1 / \text{CLK} = 0$$

T_1 is ON, T_2 is OFF

T_3 is OFF, T_4 is ON

$$\Rightarrow Q_M = 0$$

\Rightarrow Cross coupled inverters (I_5, I_6) holds the state of the slave latch.

latch level		edge
-ve	+ve	+ve
+ve	-ve	-ve

② $\text{clk} = 1 / \overline{\text{clk}} = 0$ \Rightarrow crossed coupled inverter
 T_1 is off, T_2 is on (I_2, I_3) holds the state of the
 T_3 is on, T_4 is off master.

$\Rightarrow Q_m$ is copied to the output Q .

③ $\text{clk} = 0 / \overline{\text{clk}} = 1$ $\Rightarrow (I_5, I_6)$ holds the state of the
 T_1 is on, T_2 is off slave latch $(Q_s, \overline{Q}_s) = D$
 T_3 is off, T_4 is on

Setup time

$$T_{\text{setup}} = T_{I_1} + T_{\overline{I}_1} + T_{I_2} + T_{\overline{I}_4}$$

$$T_{C \rightarrow Q} = T_{I_3} + T_{\overline{I}_6}$$

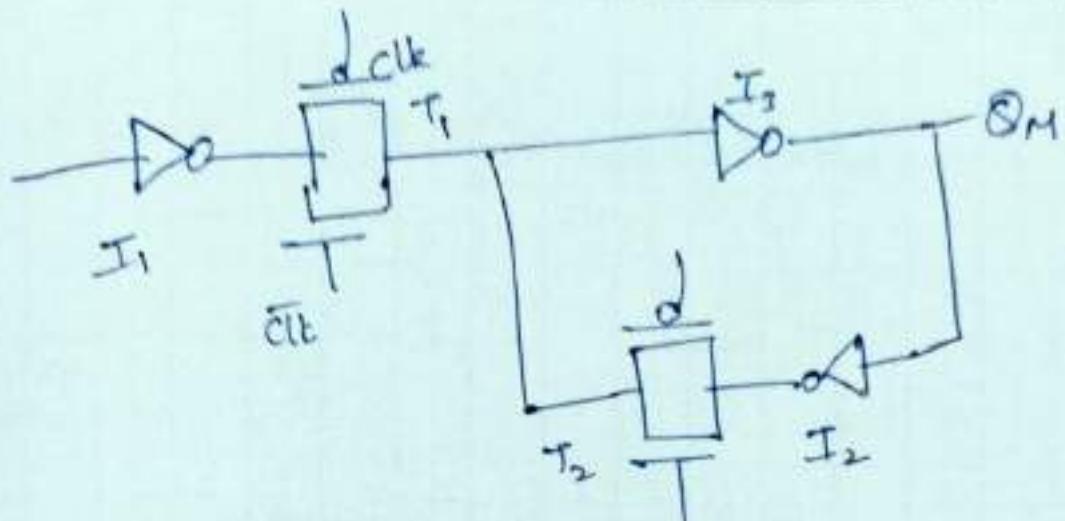
$T_{\text{hold}} = 0$ Because D_s is already settled @
 Q_m and T_1 is off after $T_{S0.1H}$

Disadvantages

Clock load will increase, because FF increases -

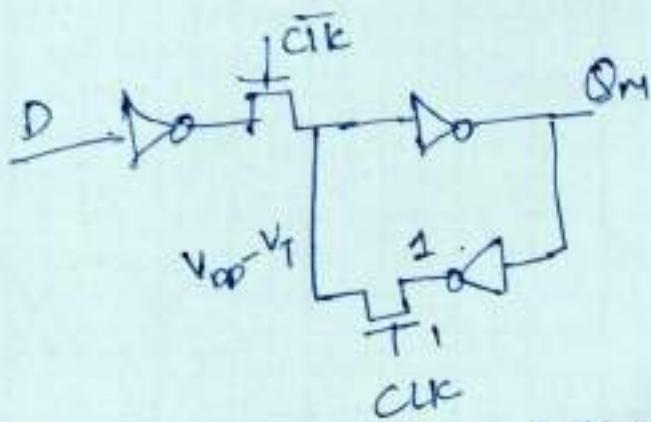
i) Large capacitive load, present to the clk signal

Assumption: $\text{clk} \& \overline{\text{clk}}$ are aligned no clk skew.



(i)

↓ Ratioless

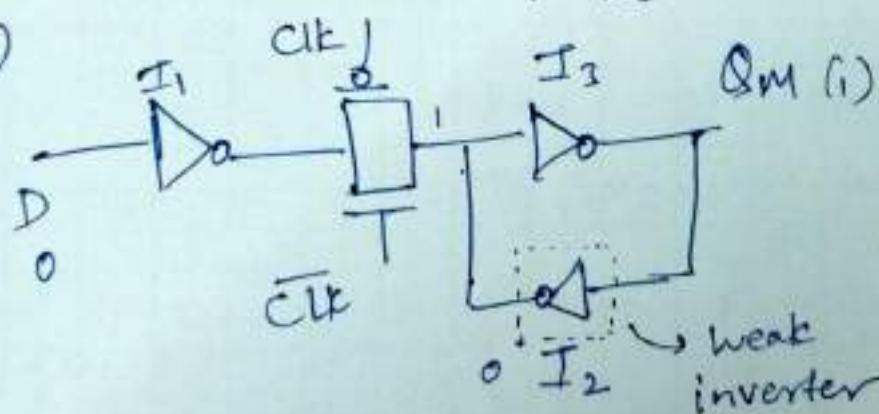


D

Reduce CLK tree network
and also, bulkiness

Ratioless

(ii)



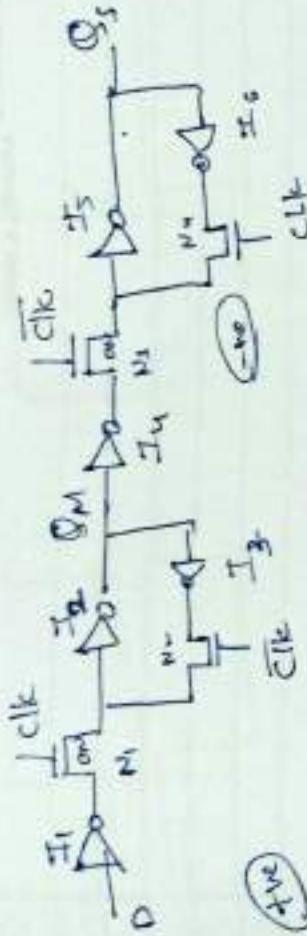
I2, overcomes over 0.

weak inverter

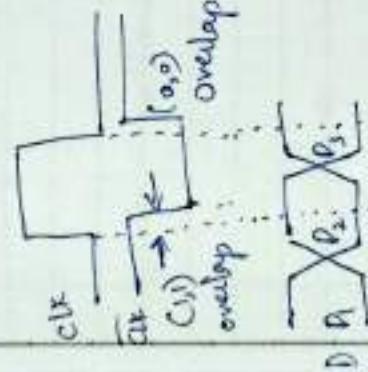
* overpower the feedback network.

→ concerned about size of inverter i.e. why ratio less

Race through



Negative edge triggered FF.



Race through happens due to (0,1) overlap.

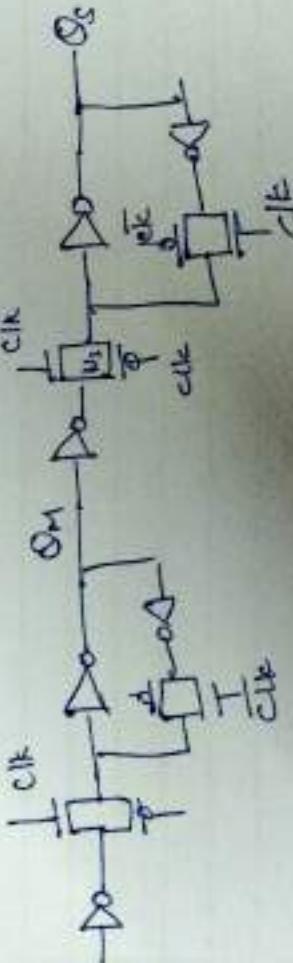


$t_{ov,0} < t_{I_1} + t_{m_1} + t_{I_2} + t_{I_4}$

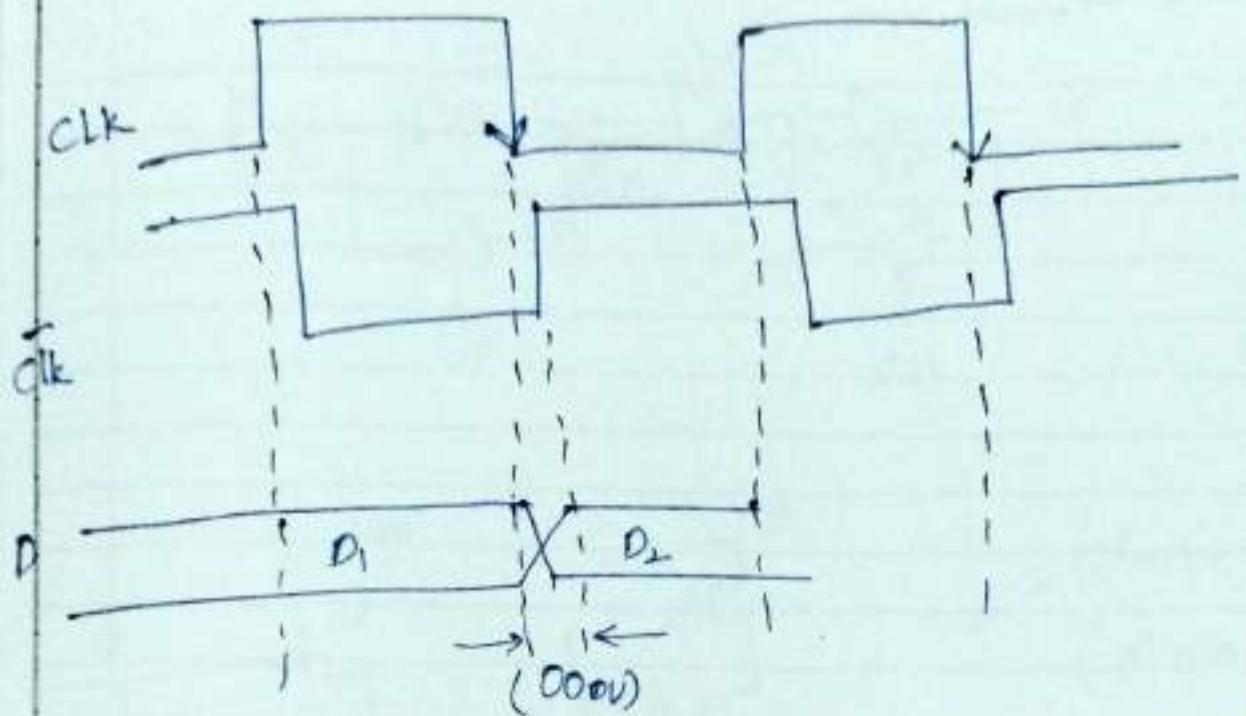
D)

Should not cause Q_3 .

~~Their~~ ~~to~~ $t_{ov,0}$ not following



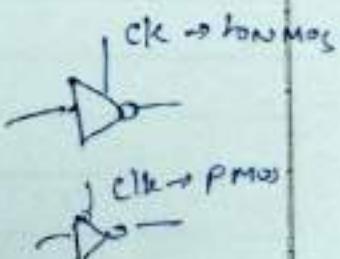
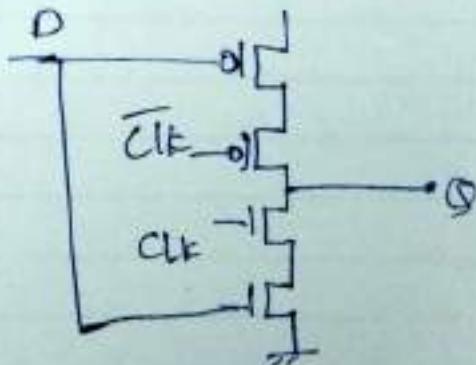
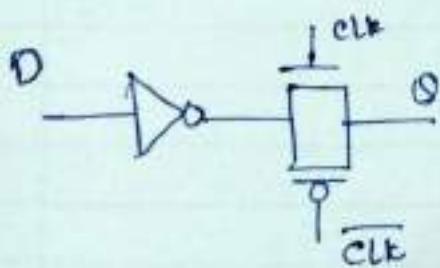
$t_{ov(0-0)} \rightarrow$ Tx. gate shall follow us.

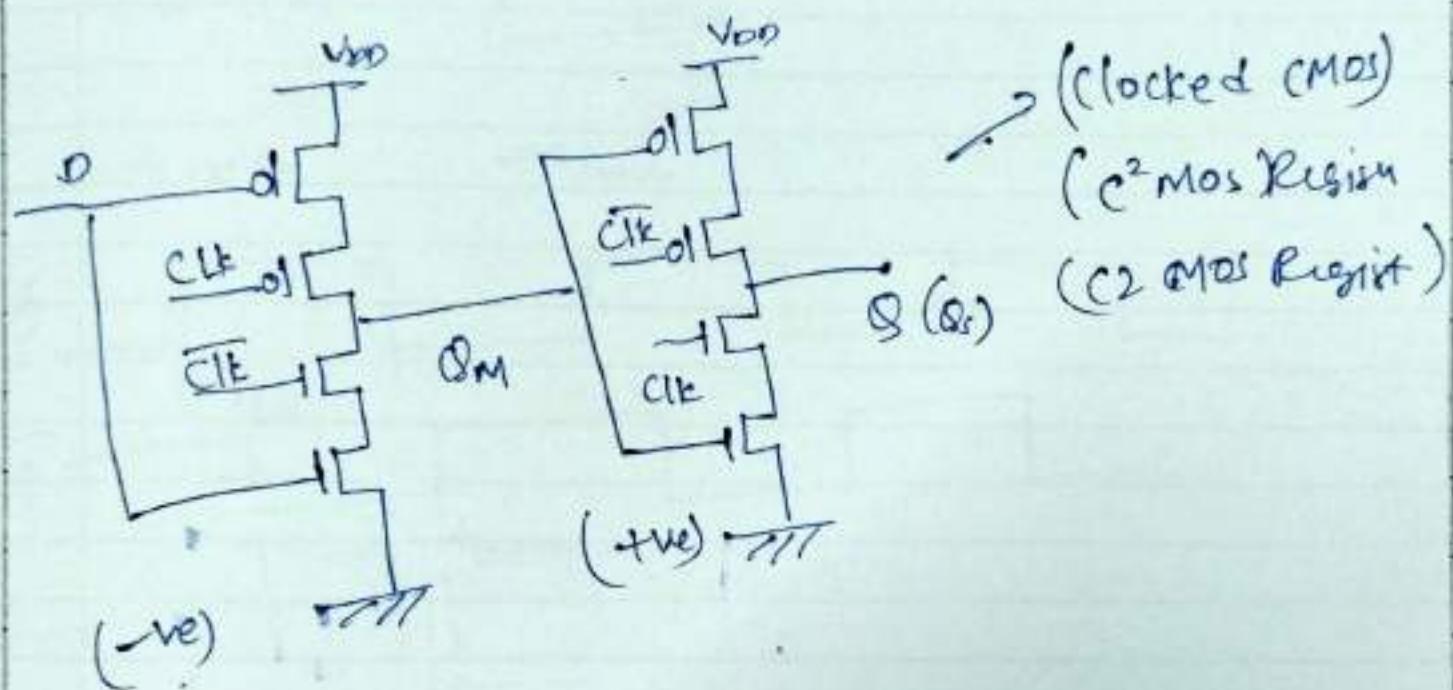
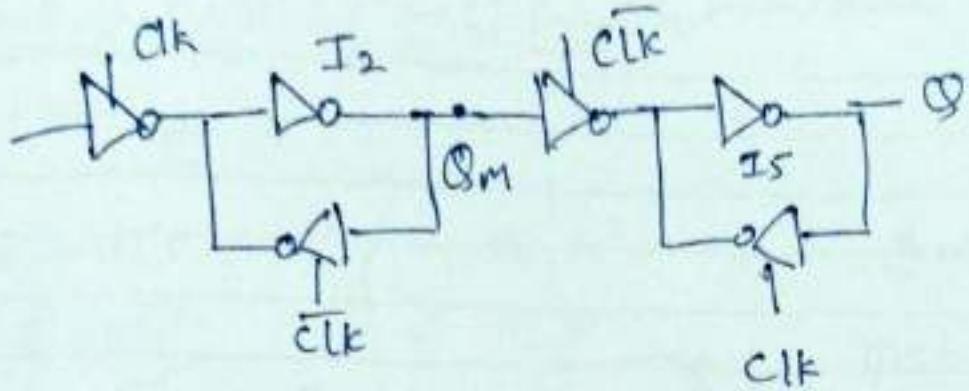


Do not allow changes in D during 0-0 ov.

$$\therefore t_{hold} > t_{ov\ 0-0}$$

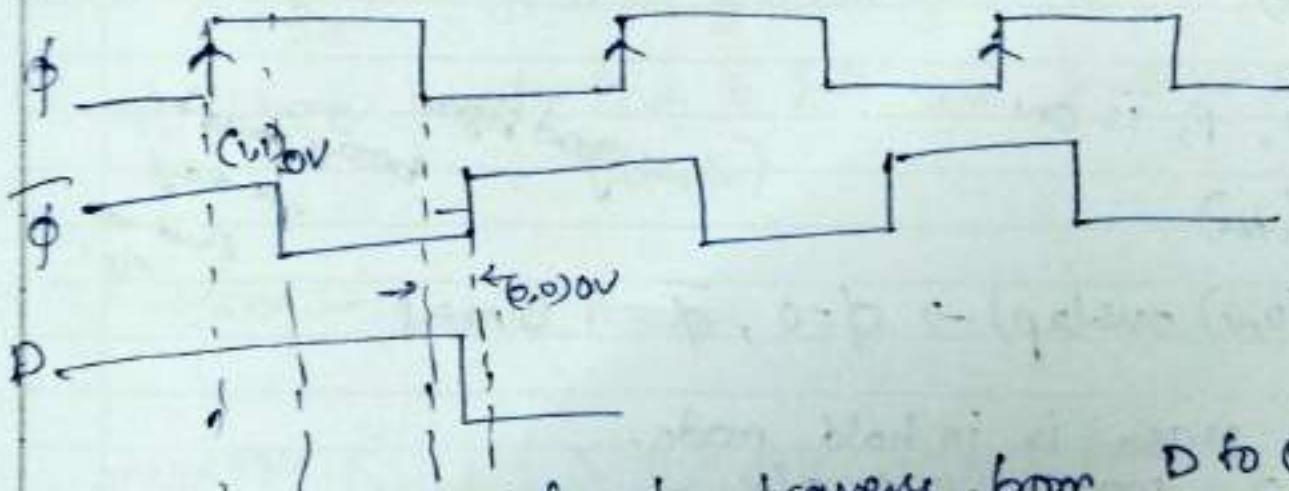
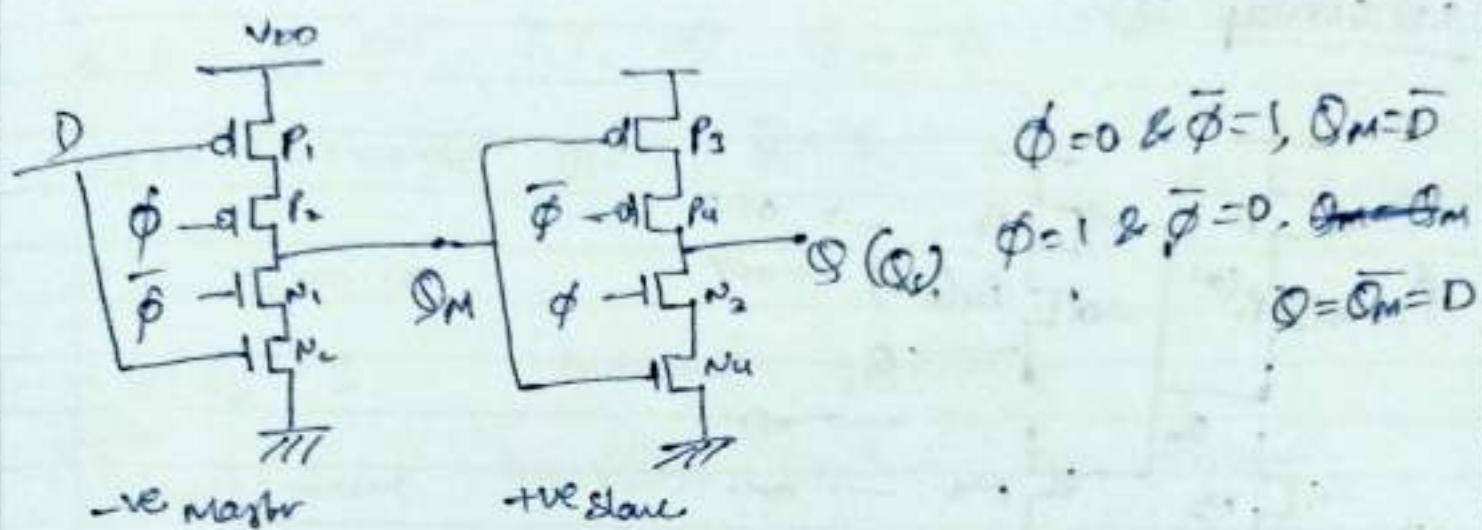
i.e. t_{hold} should be greater than (00) ov.



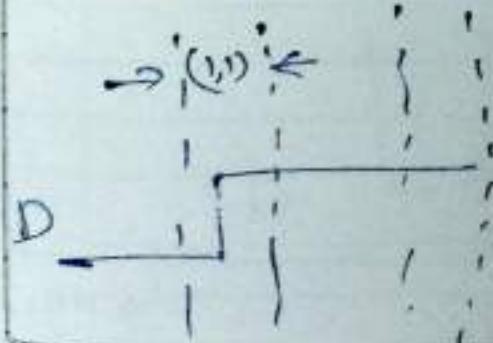


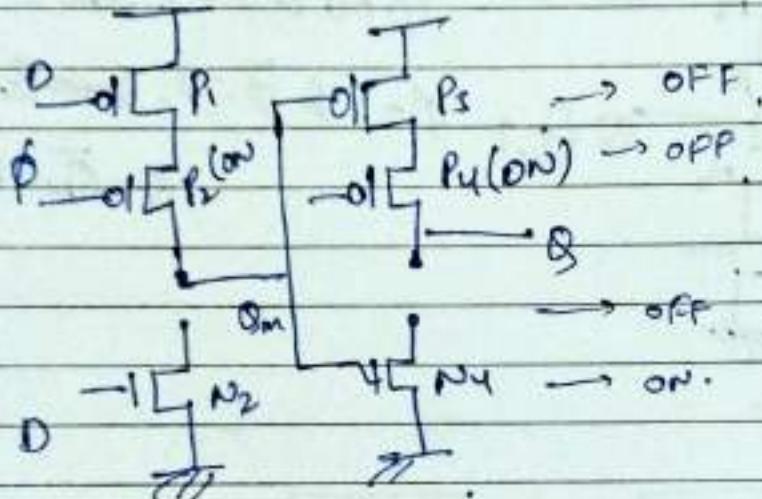
11.100V

Clocked CMOS (C²MOS) Register



* In order for data to traverse from D to Q (i.e. across master and slave), one must pull up and must pull down (or vice versa).



(0,0) overlap case:

$D=0 \rightarrow 0$, P_2 is ON

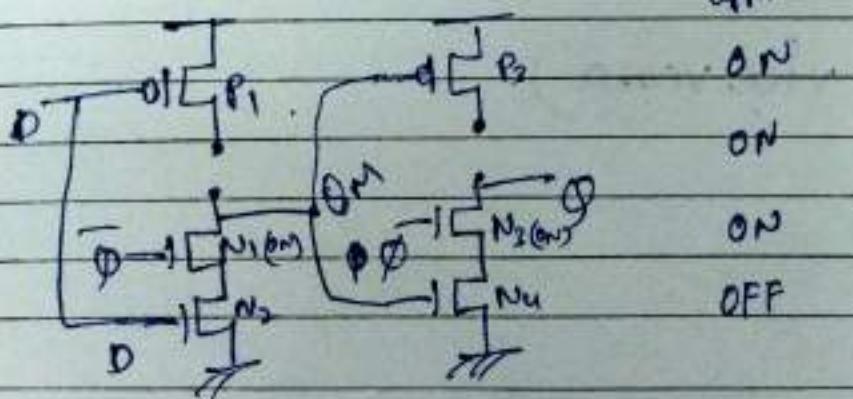
$Q_m = 1$ (V_{DD})

good sign.
decay in at
ve edge
short not
alr1

After (0,0) overlap) $\rightarrow D=0$, $\bar{\phi}=1$ $Q_m=1$

\Rightarrow slave stage is in hold mode.

$\Rightarrow D=1 \rightarrow 0$ doesn't affect O/P.

(1,1) overlap case:

flow rule for -ve edge trigger

$D = 0 \rightarrow 1$ during (1,1) overlap.

N_1, N_2 are ON, P_1, P_2 off. $Q_M = 0$

not good sign.

It shouldn't change after the edge clock

after (1,1) overlap $\phi = 1, \bar{\phi} = 0$

$\Rightarrow P_3, P_4$ are ON

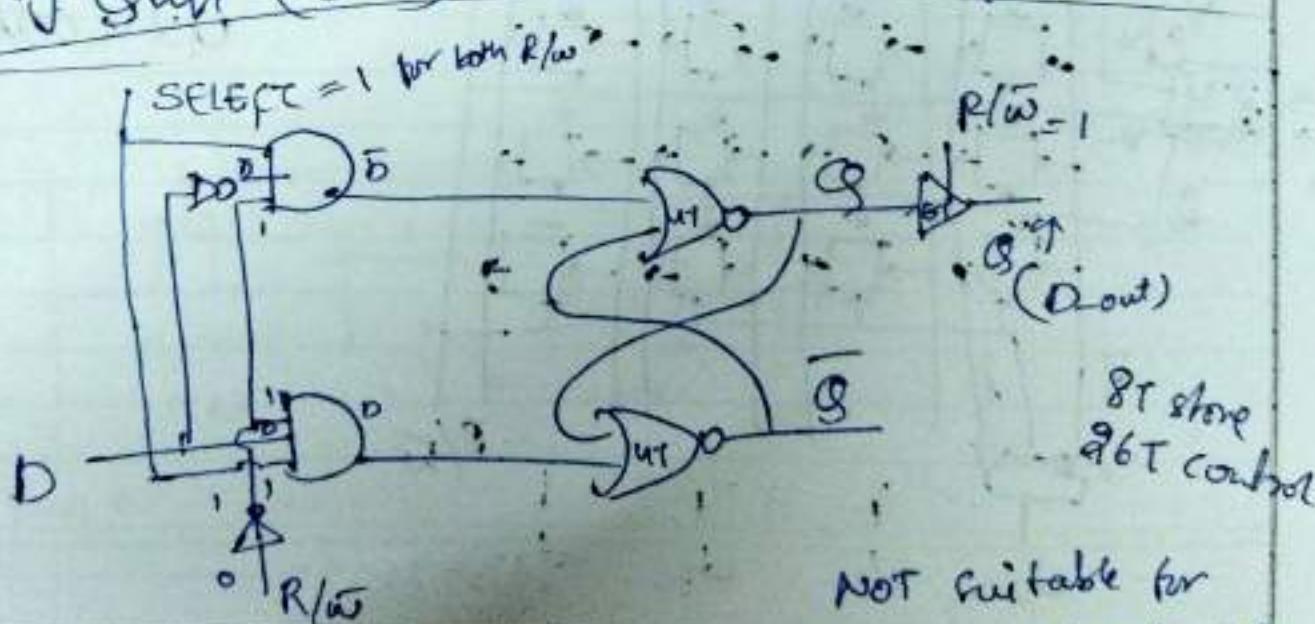
$\Rightarrow Q(Q_s) = 1$ (problematic scenario)

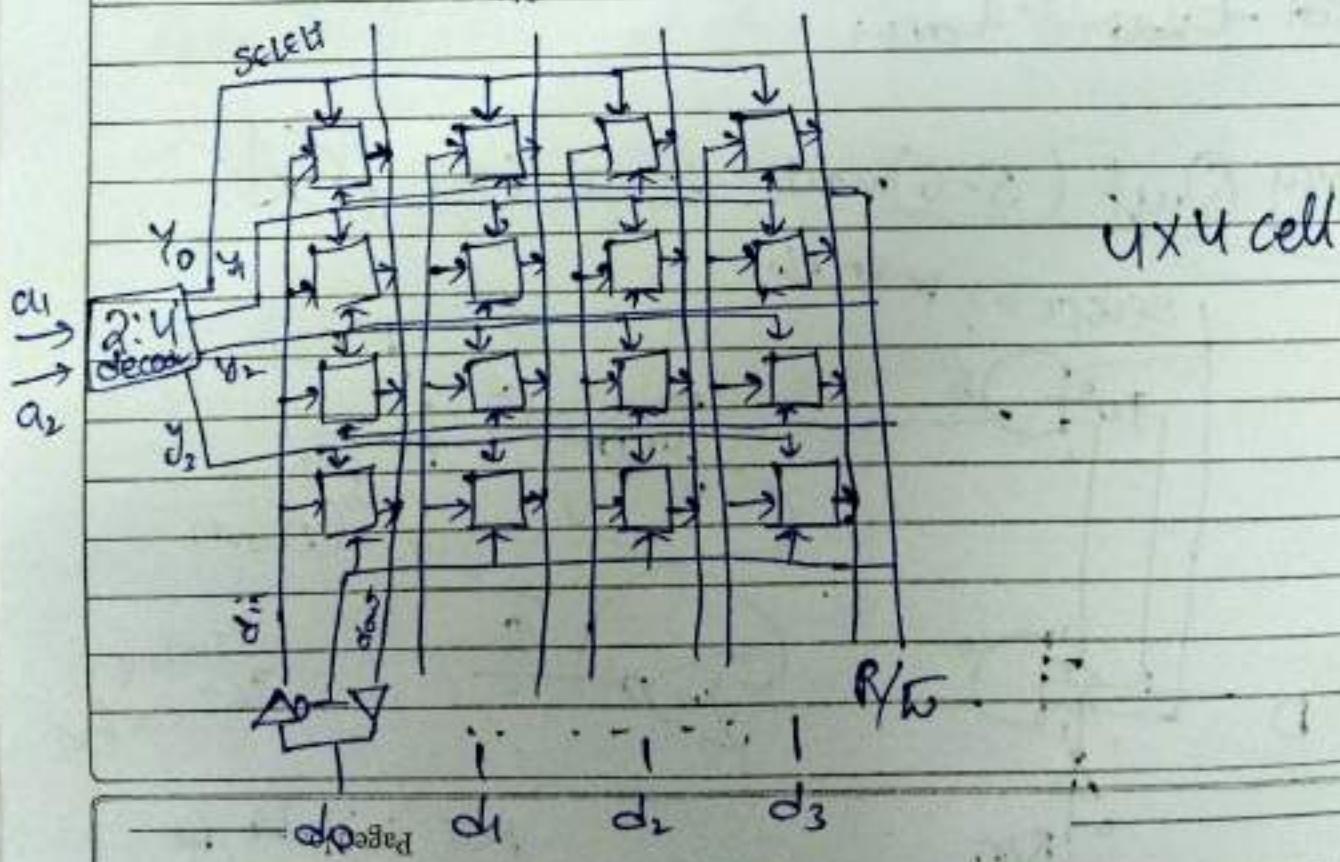
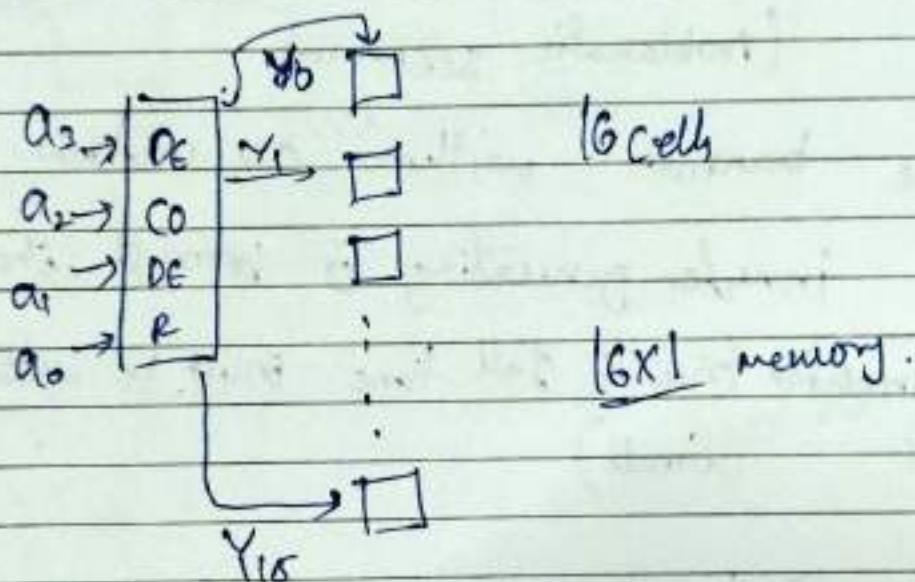
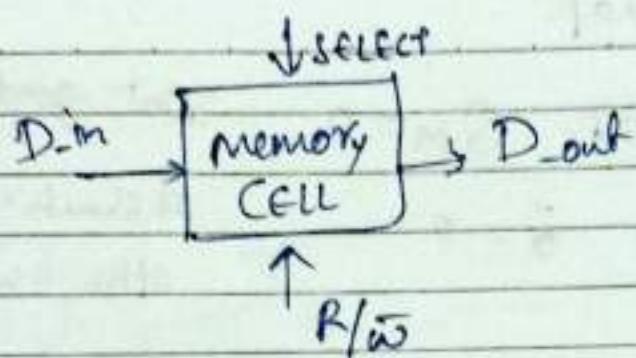
solve: i) don't make transition within OV window.

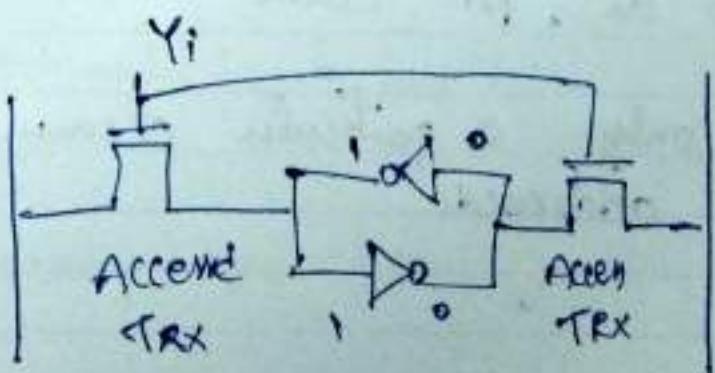
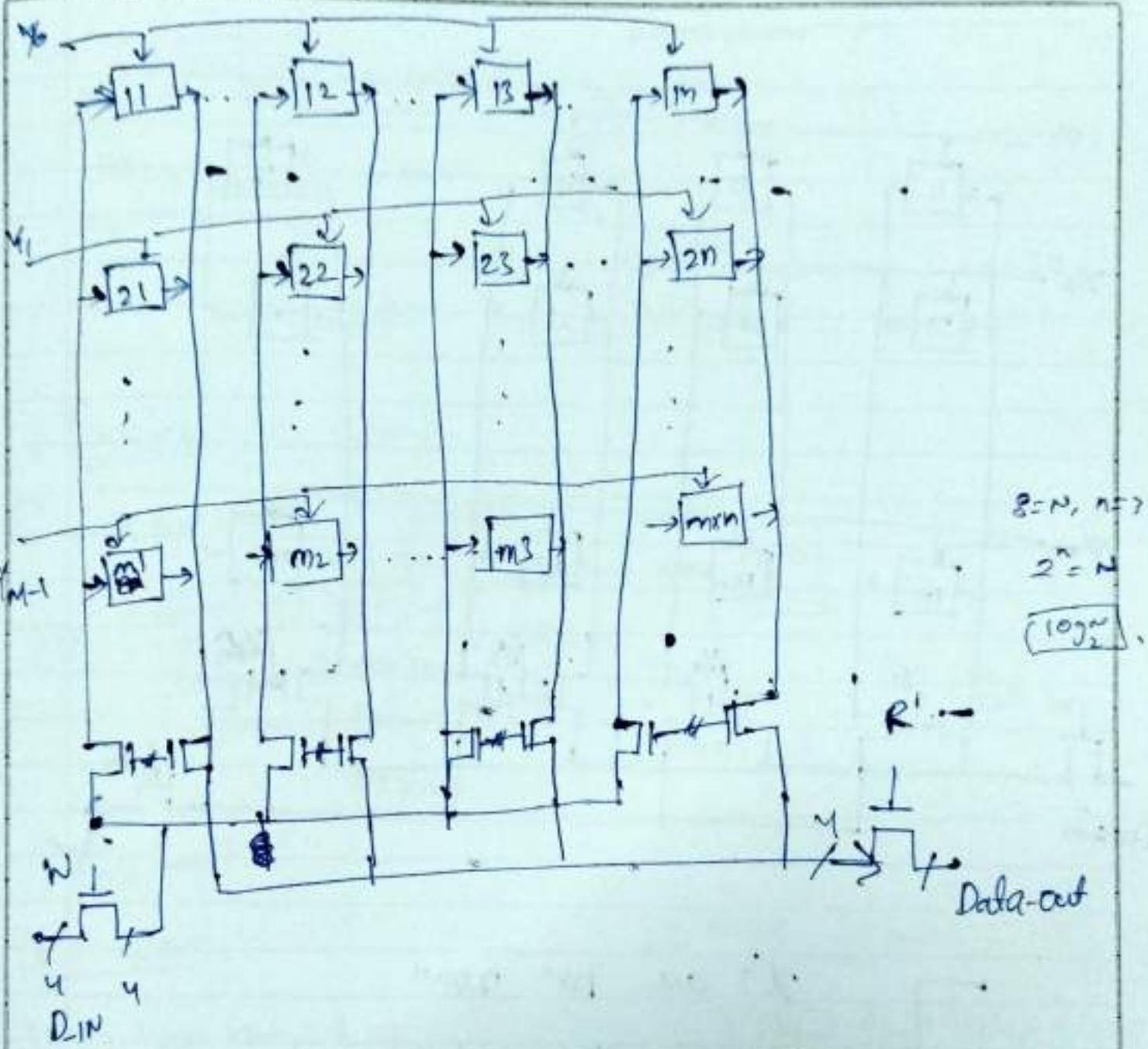
ii) $\phi \rightarrow \bar{\phi}$ inverter generating $\bar{\phi}$ from ϕ should be very strong inverter (rise & fall time must be sufficiently small).

$\Rightarrow t_{\text{hold}} - t_{\text{hold}} > t_{\text{OV},1-1}$

memory Out (5-6) make End semi ~~kit~~







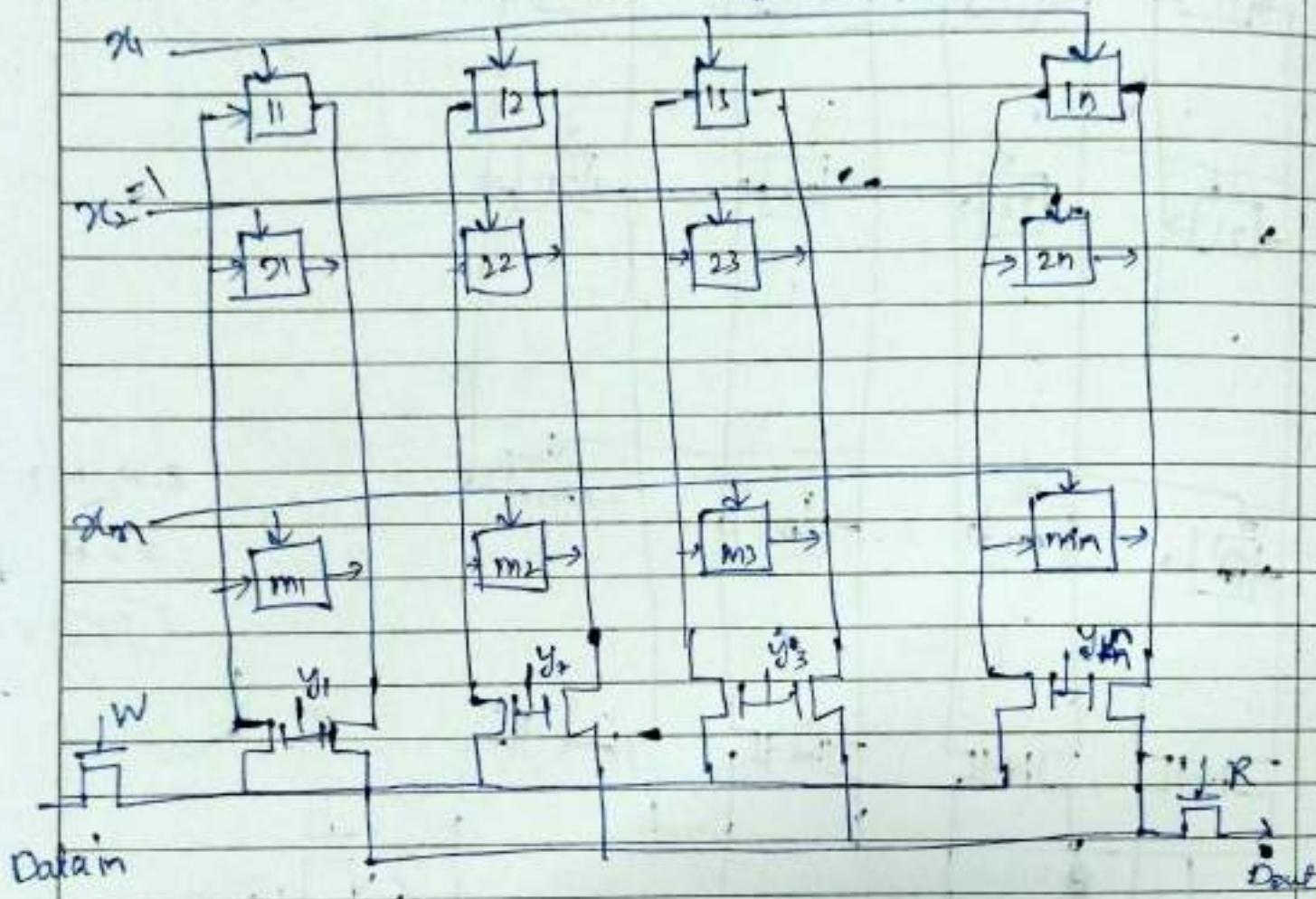
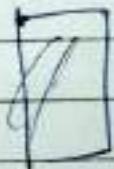
$D_{in} = 0$

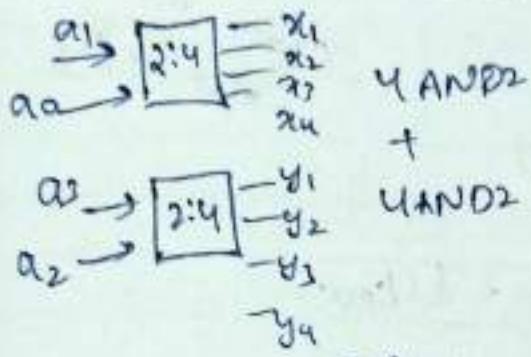
D_{out}

SRAM cell.

12/NOV/24

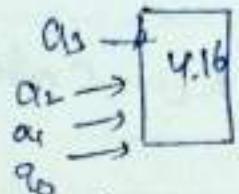
Teacher's Signature

 x 's are for rows y 's are for columnsSo only a particular element will
be addressed.



$4 \text{ AND } 2$
+

Better.



$4 \text{ AND } 2$

$(6 \text{ AND } 4)$

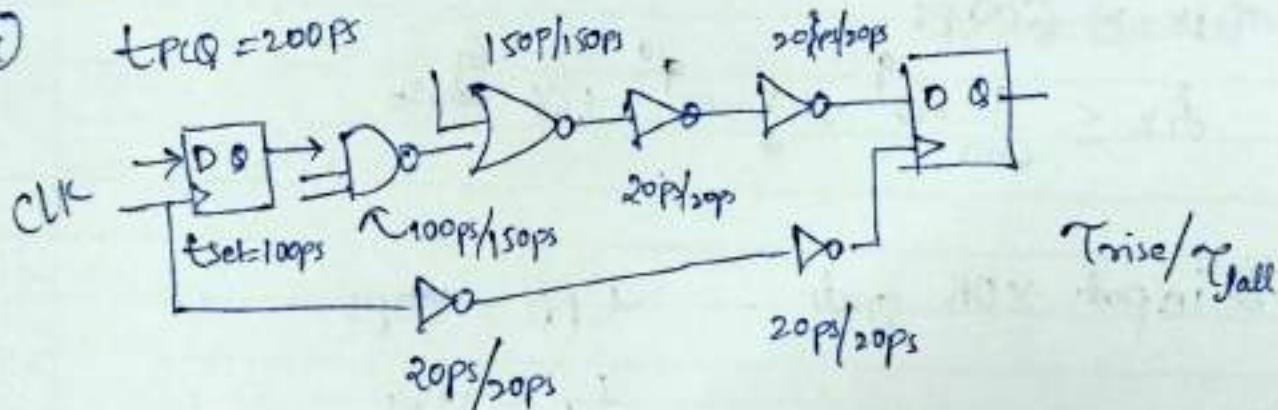
not good

□
T
D
:
□

Problems

Exam

$$t_{PLQ} = 200 \text{ ps}$$



$$f_{CLK(\max)} = ?$$

i) No Skew

$$T_{CLK} \geq t_{PD} + t_{Setup} + t_{PCQ}$$

$$(t_{clock} + t_{CO} \geq t_{hold}) \quad (t_{hold} \leq t_{clock} + t_{CO})$$

ii) Positive Skew

$$T_{CLK} \geq t_{PD} + t_{Setup} + t_{PCQ} - t_{Skew}$$

~~tclock~~

$$t_{hold} \leq t_{clock} + t_{CO} - t_{Skew}$$

iii) Negative Skew

$$T_{CLK} \geq t_{PD} + t_{Setup} + t_{PCQ} + t_{Skew}$$

$$t_{hold} \leq t_{clock} + t_{CO} + t_{Skew}$$

choose max value
between t_{PD} & t_{PCQ}

falls in the skew category

$$T_{CLK} \geq t_{PD} + t_{setup} + t_{PCQ} - t_{skew}$$

$$\Rightarrow \frac{150}{+150} + 100 + 200 - (2 \times 20)$$

$$+20 \\ +20$$

$$T_{CLK} \geq 600 \text{ ps}$$

$$f_{CLK} \leq \frac{1}{600} \text{ GHz} = \frac{1}{6} \times 10^9 \text{ Hz} = 1.66 \text{ GHz}$$

② 2 input XOR gate

$$t_{PD} = 100 \text{ ps}$$

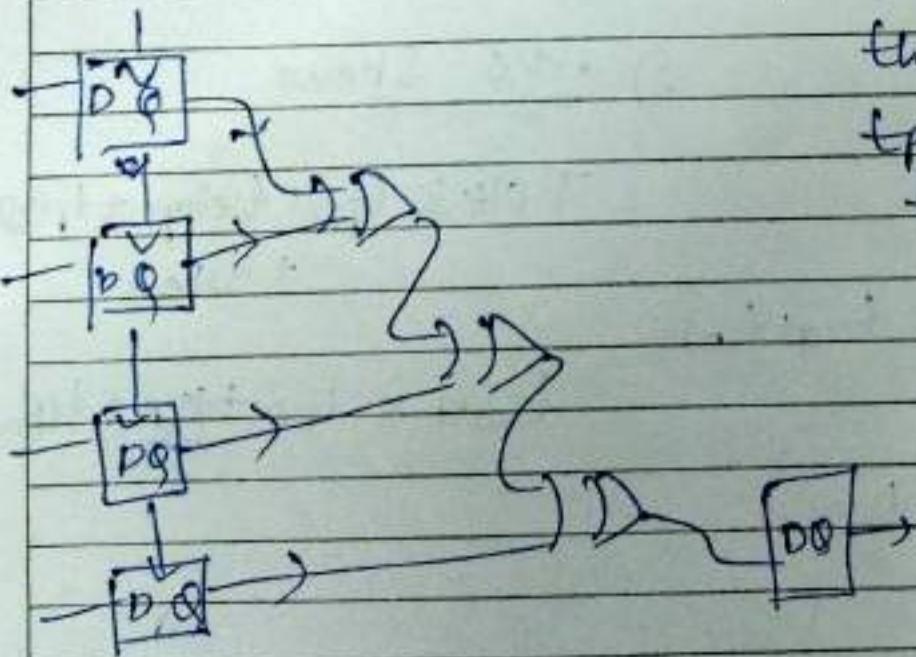
$$t_{PD} = 55 \text{ ps}$$

$$\text{FF: } t_{setup} = 60 \text{ ps}$$

$$t_{hold} = 20 \text{ ps}$$

$$t_{PCQ} = 70 \text{ ps}$$

$$t_{clock} = 50 \text{ ps}$$



a) If there is no clock skew, what is the max op freq of ckt.

∴ NO skew category.

$$T_{CLK} \geq t_{PP} + t_{Setup} + t_{PCQ}$$

$$T_{CLK} \geq 3 \times 100 + 60 + 70 = 430 \text{ ps}$$

$$f_{CLK} \leq 2.325 \text{ GHz}$$

b) How much clock skew can be tolerated if ckt operates @ 2 GHz.

$$f_{CLK} \leq 2 \text{ GHz}$$

$$T_{CK} = 500 \text{ ps}$$

i) Positive Skew

$$T_{CLK} \geq t_{PP} + t_{Setup} + t_{PCQ} - t_{Skew}$$

$$500 \text{ ps} \geq 300 + 60 + 70 - t_{Skew}$$

$$500 \geq 430 - (t_{Skew}) \rightarrow t_{Skew} > 0$$

⇒ No constraint as this inequality is always satisfied.

ii) Negative Skew

$$T_{CLK} \geq t_{PP} + t_{Setup} + t_{PCQ} + t_{Skew}$$

• loops $\geq 430 + t_{skew}$

$t_{skew} \leq 70\text{ps}$ constraint

- Q How much clock skew can the CLK tolerate before it might experience a hold time violation?

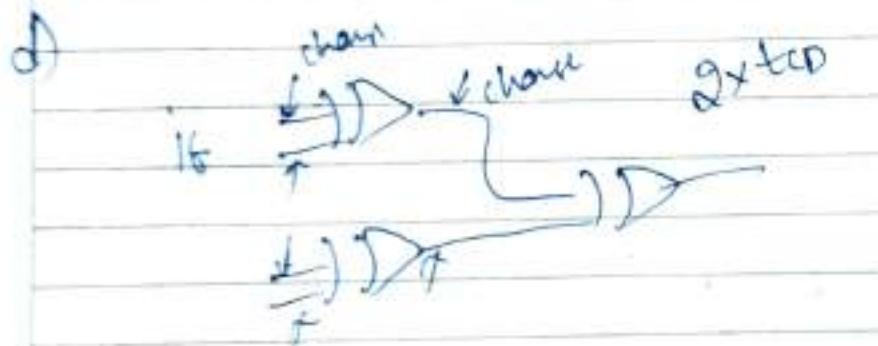
$$t_{hold} \leq t_{CKQ} + t_{PH} - t_{skew}$$

$$A \leq 60 \checkmark \text{ something}$$

$$A \leq 100$$

$$20 \leq 50 + 55 - t_{skew}$$

$$-t_{skew} \leq 85\text{ps}$$



what is the max operating freq of this CLK? (for no clk skew)

$$T_{clk} \geq t_{PH} + t_{setup} + t_{PQ}$$

$$T_{clk} \geq 2 \times 100 + 60 + 70$$

$$T_{clk} \geq 330\text{ps}, f_{clk} \leq 3.03\text{GHz}$$

e) How much clock skew can be tolerated before it might experience hold failure in 2nd ckt.

Ans

$$t_{hold} \leq t_{ao} + t_{CD} - t_{skew}$$

$$20 \leq 80 + 2(55) - t_{skew}$$

$$t_{skew} \leq 87 \text{ ps } 140 \text{ ps}$$

Carry look ahead

Generate

$$\boxed{c_{i+1} = 1}$$

$$\Leftrightarrow a_i = 1$$

$$\Leftrightarrow b_i = 1$$

$$\Rightarrow \boxed{g_i = a_i b_i}$$

propagate

$$\boxed{c_i = c_i}$$

$$\Rightarrow a_i + b_i$$

$$\text{Carry } \boxed{p_i = a_i \oplus b_i}$$

$$c_{i+1} = f(g_i, p_i, c_i)$$

$$c_{i+1} = g_i + p_i c_i$$

Carry kill

$$k_i = \overline{a_i} \overline{b_i}$$

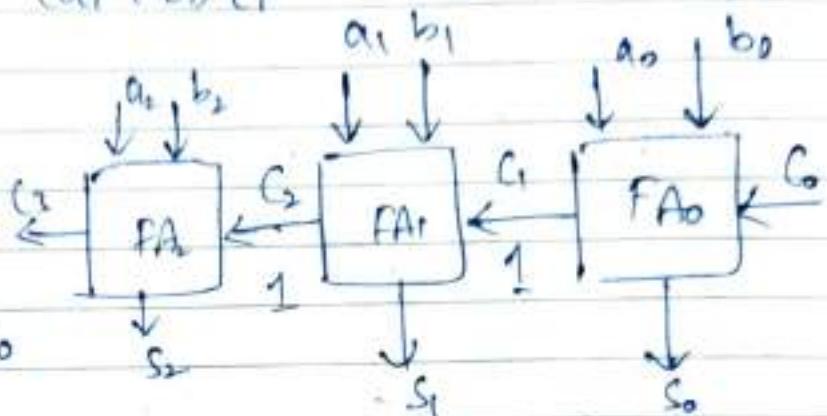
$$c_{i+1} = 0$$

interchangeable.

$$C_{i+1} = a_i b_i + (a_i + b_i) C_i$$

$$C_1 = g_0 + f_0 C_0$$

$$\begin{aligned} C_2 &= g_1 + P_1 C_1 \\ &= g_1 + P_1 g_0 + P_1 P_0 C_0 \end{aligned}$$



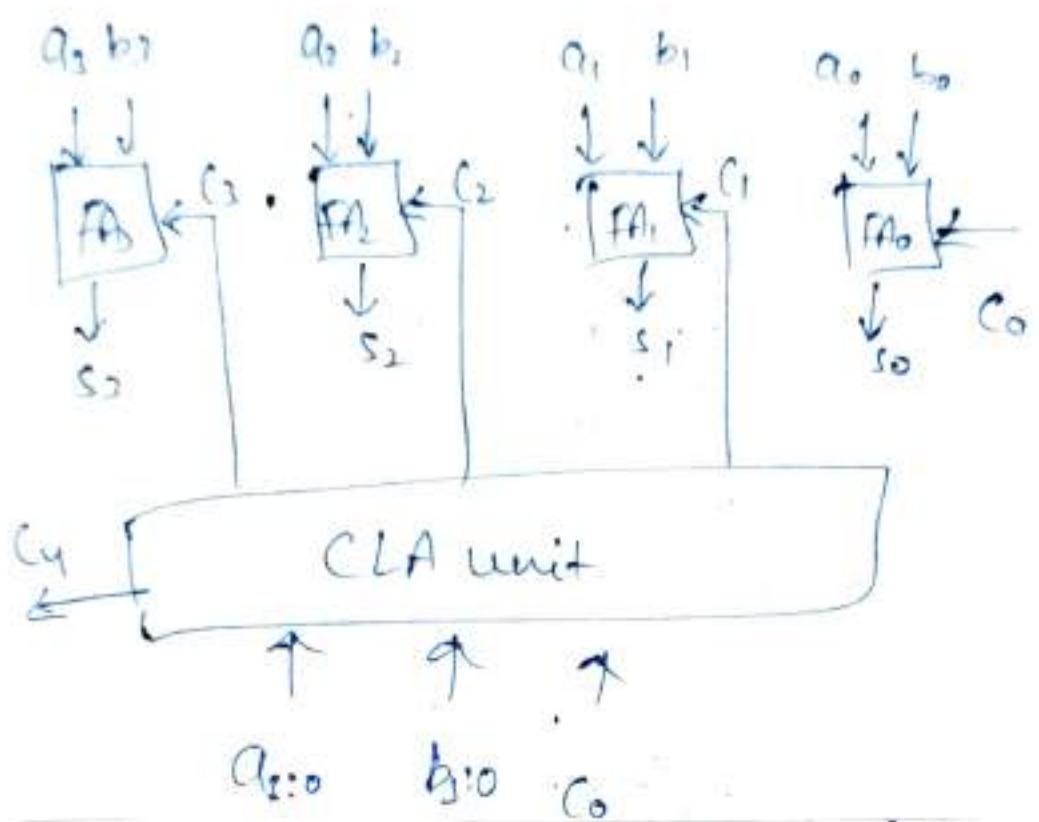
$$P_1 \leftarrow g_0 \leftarrow$$

$$P_2 \leftarrow P_1 \leftarrow P_0 \leftarrow$$

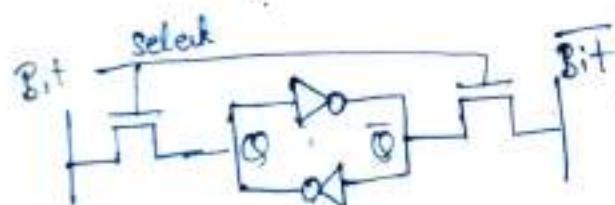
$$C_3 = g_2 + P_2 g_1 + P_2 P_1 g_0 + P_2 P_1 P_0 C_0$$

$$C_4 = g_3 + g_2 P_3 g_1 + g_2 P_2 P_1 g_0 + P_2 P_1 P_0 C_0$$

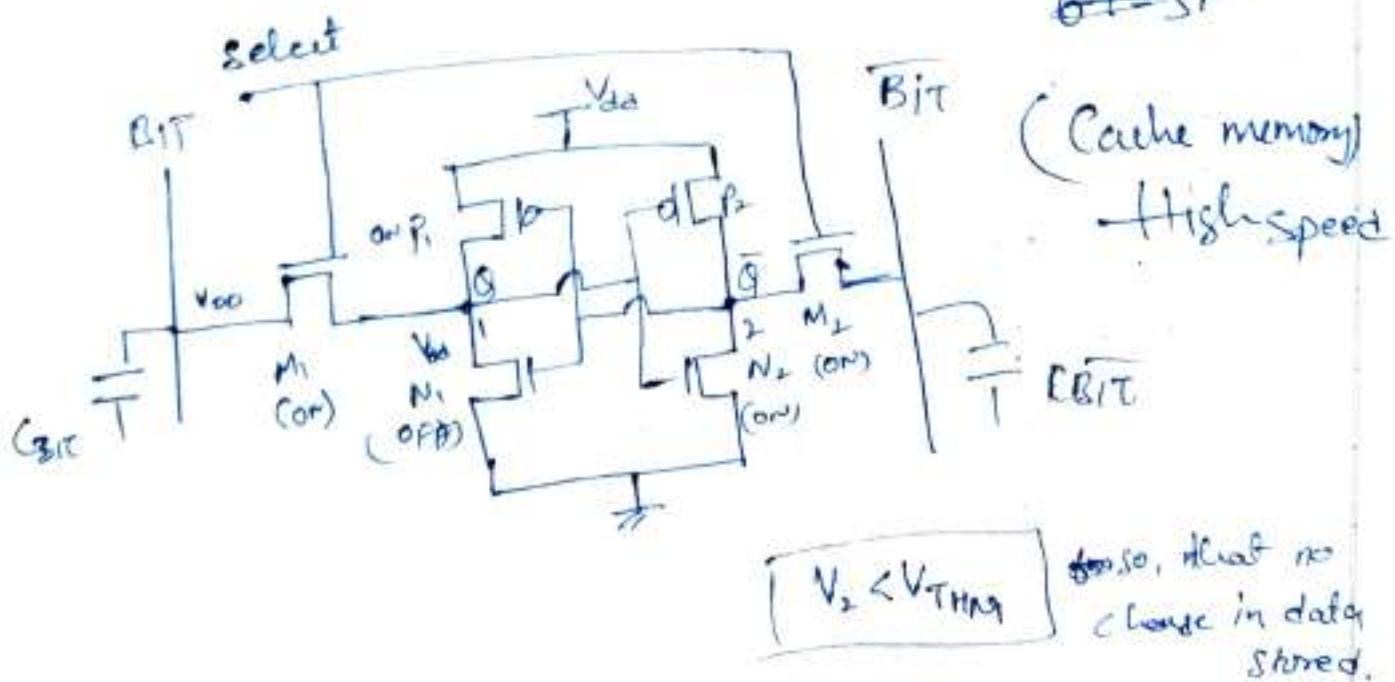
$$= g_3 + P_3 g_2 + P_3 P_2 g_1 + P_3 P_2 P_1 g_0 + P_3 P_2 P_1 P_0 C_0$$



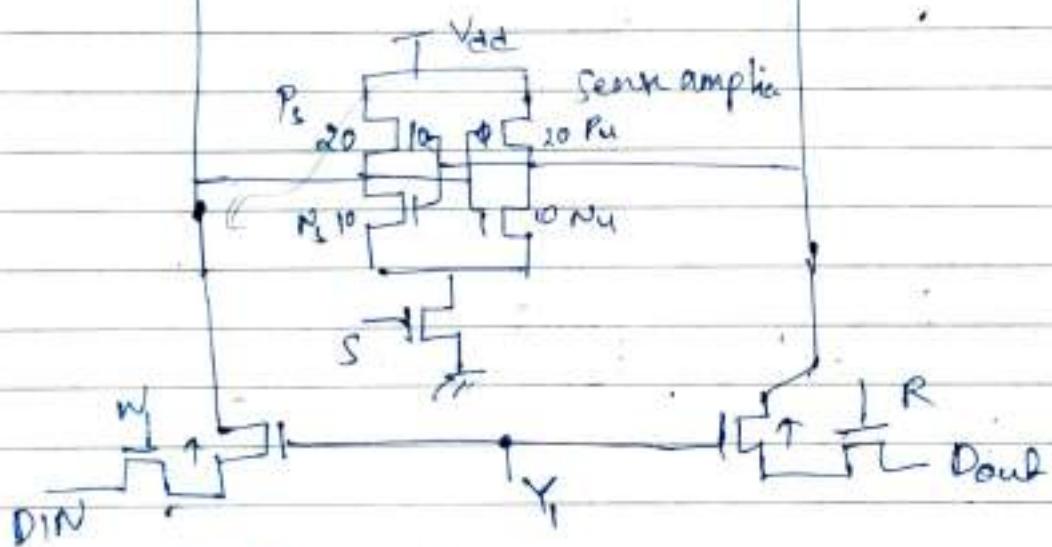
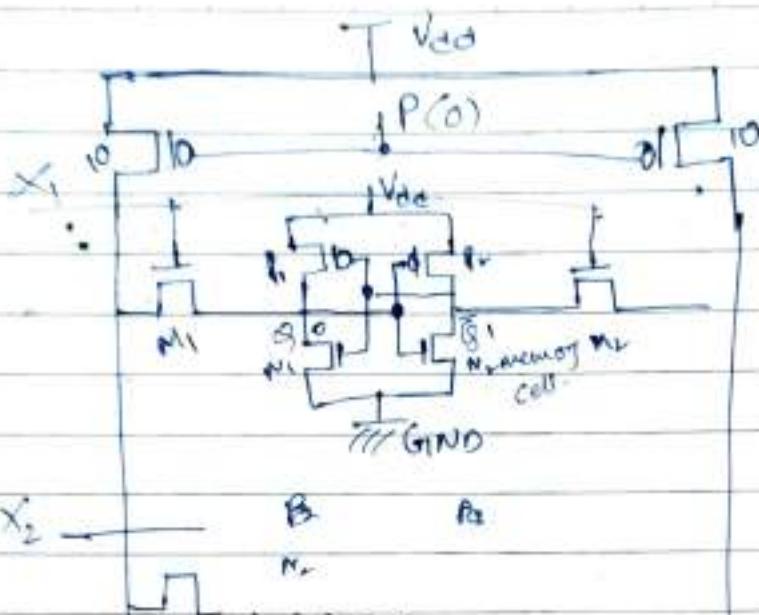
~~Block diagram~~



6T-SRAM Cell



for exam
just class.



Initially let $Q=1$, $\bar{Q}=0$

$\Rightarrow \text{SELECT}=1$

$\Rightarrow M_1, M_2$ are ON.

Initially precharge operation $\Rightarrow P=0$

$\Rightarrow \text{BIT} \& \bar{\text{BIT}}$ are precharged to VDD

Evaluate $\therefore P=1$

$Q=1 \Rightarrow N_2$ is ON

$Q=0 \Rightarrow P_1$ is ON

- $C_{\overline{BIT}}$ discharge slowly
- $V_{\overline{BIT}}$ slows decrease
- $C_{\overline{BIT}}$ remains charged to V_{DD} ($Q=1$)
- $(V_{\overline{BIT}} - V_{BIT})^{> \text{thr}}$ is sensed by a comparator which responds with logic 1 o/p
- Conclusion: Info stored is logic 1
if \neg ve logic 0

Write Operation

$$X_i = Y_i = S = P = 0 \text{ (initially)}$$

precharge operation : $BIT \& \overline{BIT} = 1$.

Assume $Q=0$ & $\bar{Q}=1$ and we want to write the value 1 in the SRAM cell.

Evaluate $P=1$, $X_2=1$, $D_{in}=1$, $Y_i=1$, $W=1$.

⇒ BIT tries to discharge through $N_{10}-N_1$

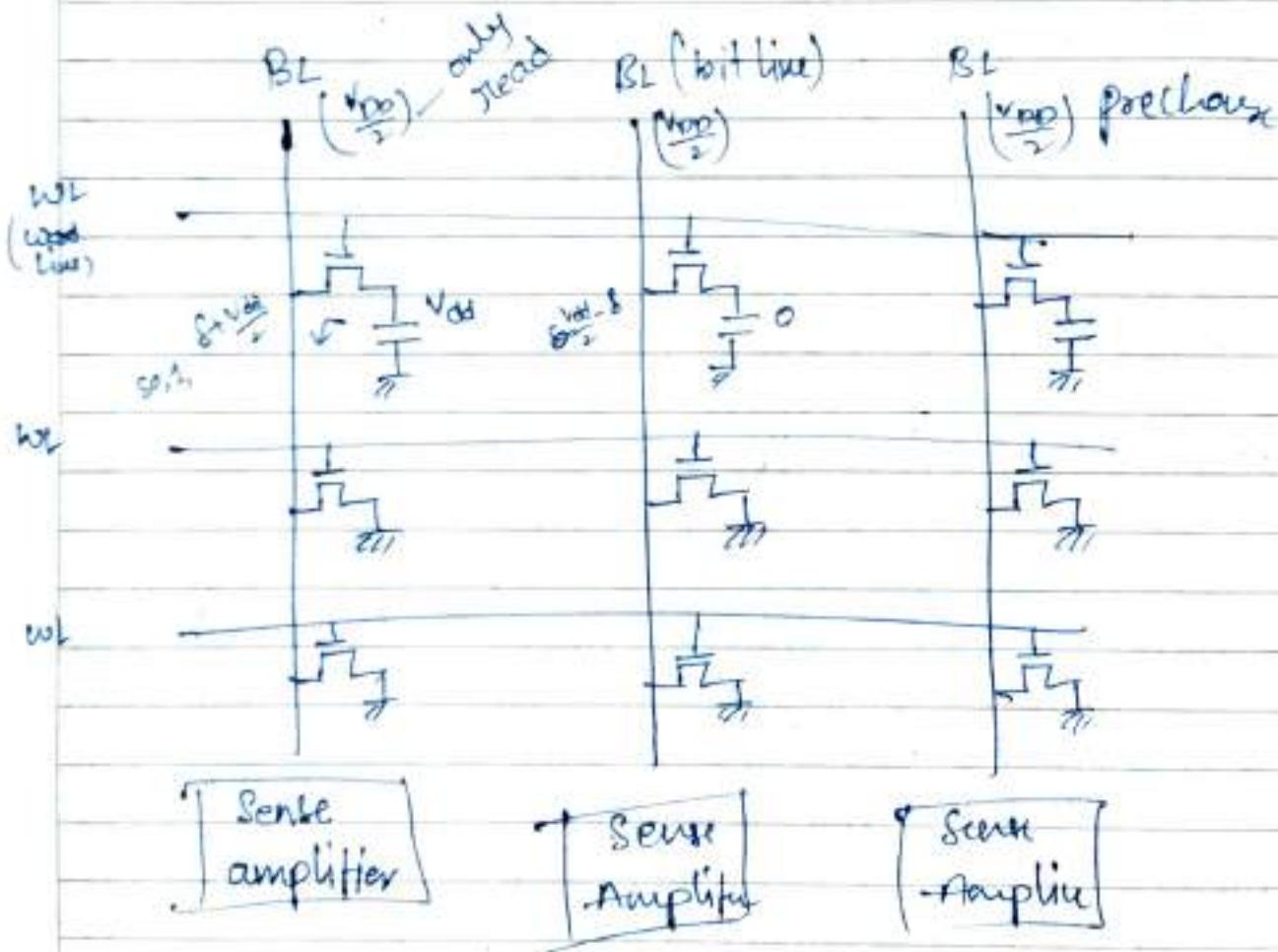
⇒ However, $D_{in}=1$, logic 1 is being sent into BIT line.

⇒ $Q=1$, $\bar{Q}=0$

Now, we make $\delta = 1$

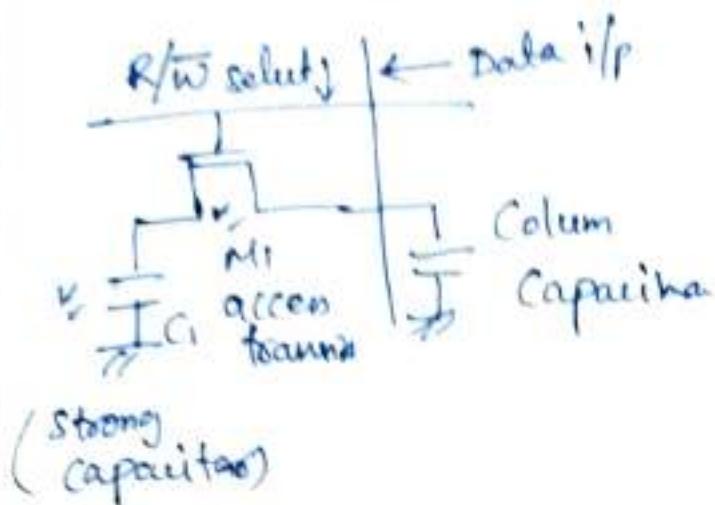
- ⇒ Sense amplifier aids faster charging of BLT as it has larger width transistors.
- ⇒ reading time is lowered as P_1 aids in charging line B.

Dynamic RAM (1T) (main memory)



$$0 \xrightarrow{t_1} \frac{V_{DD}}{2} \xrightarrow{t_2} V_{DD} - V_T$$

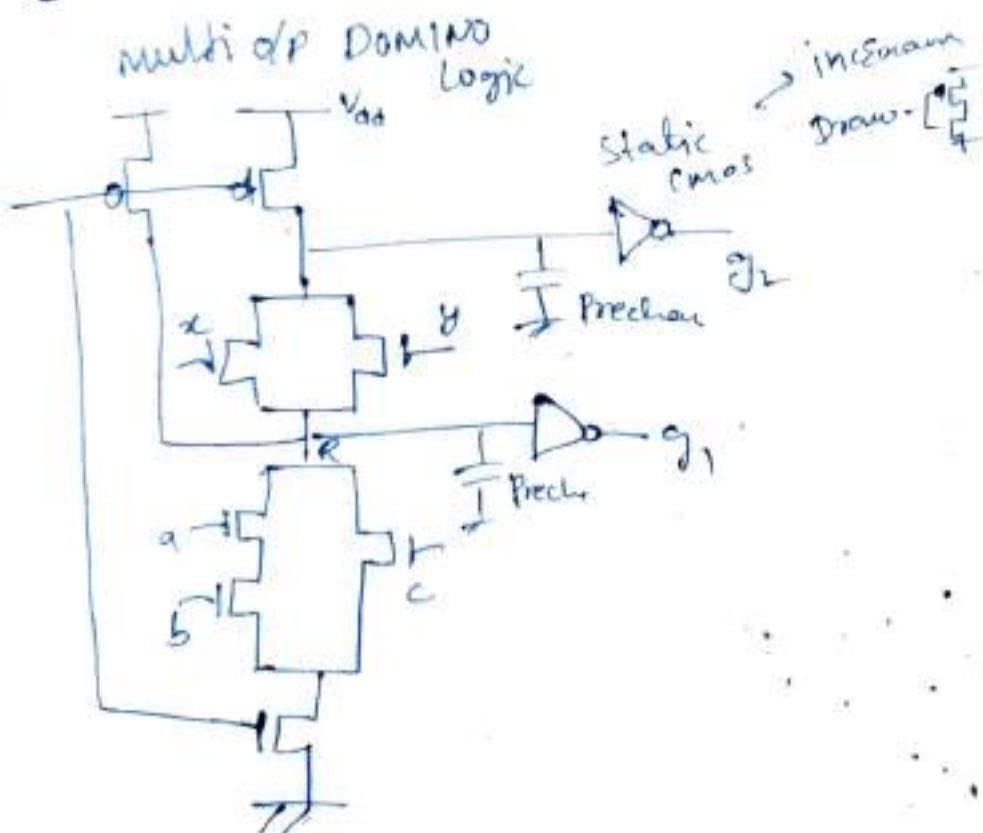
$$t_1 < t_2$$



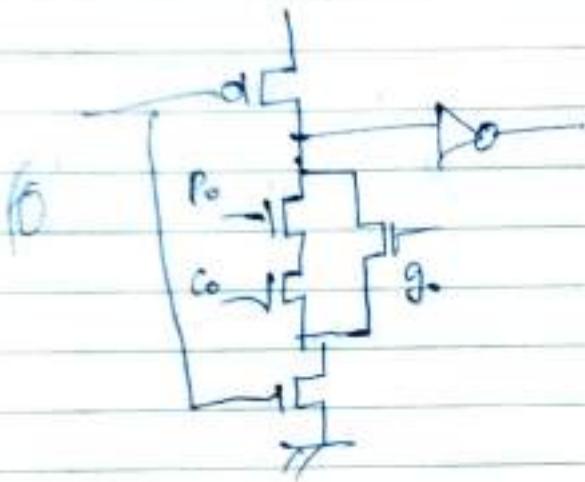
destructive
read operation
↓ after every
read there
must be write operation
to restore the data.

Susbs

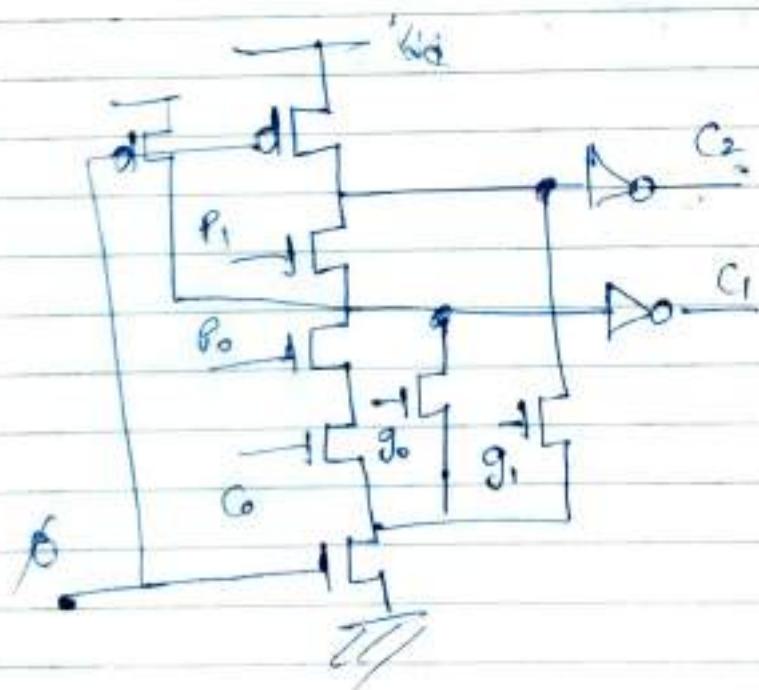
$$g_1 = ab + c \quad g_2 = (x+y)g_1$$



$$C_1 = g_0 + p_0 C_0$$



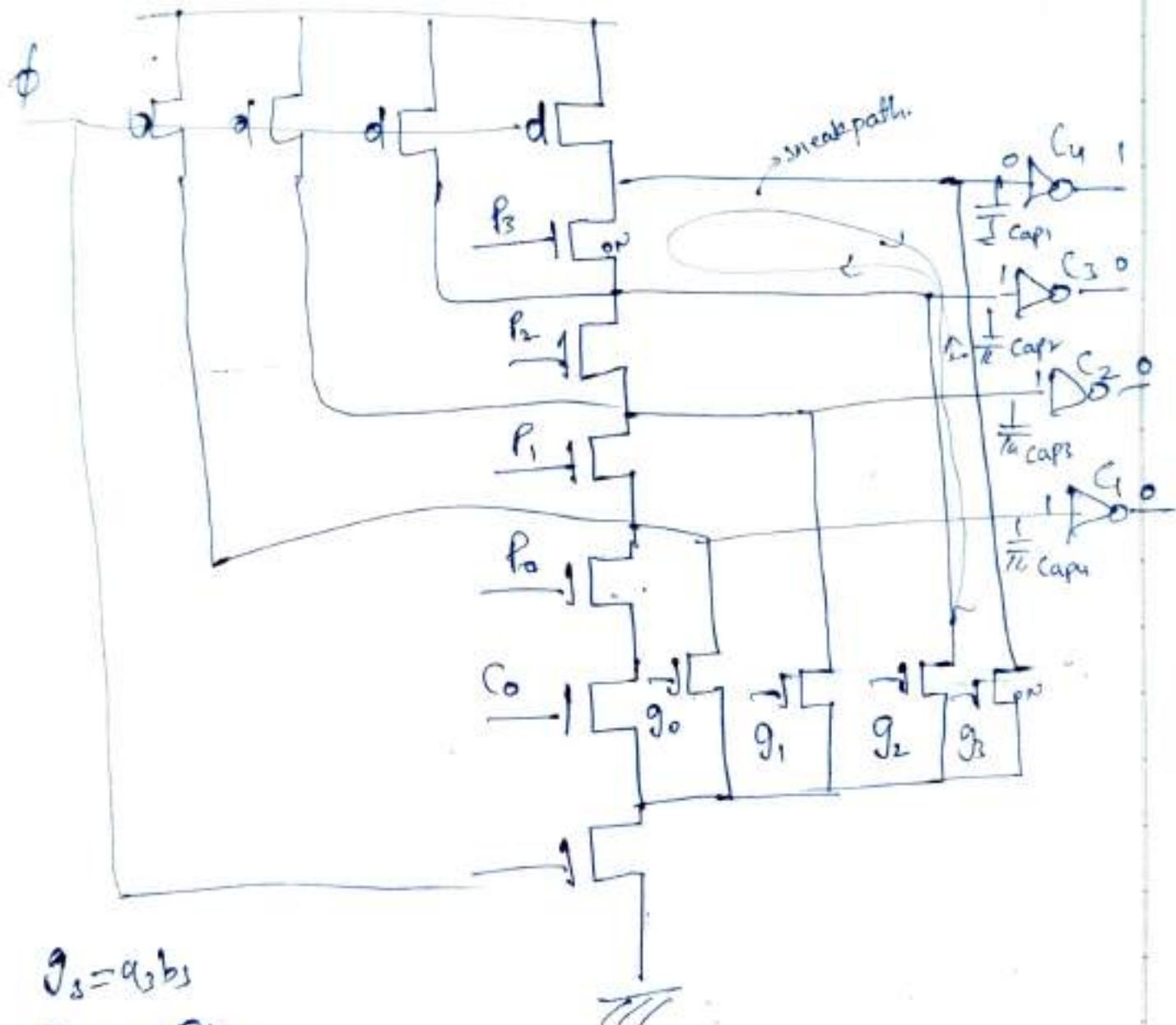
$$C_2 = g_1 + p_1 C_1 \doteq p_1 + p_1(g_0 + p_0 C_0)$$



$$C_3 = g_2 + b_2 C_2 = g_2 + P_2(g_1 + P_1(g_0 + P_0(c_0)))$$

$$C_4 = g_3 + P_3 C_3$$

$$C_4 = g_3 + P_3 [g_2 + P_2(g_1 + P_1(g_0 + P_0(c_0)))]$$



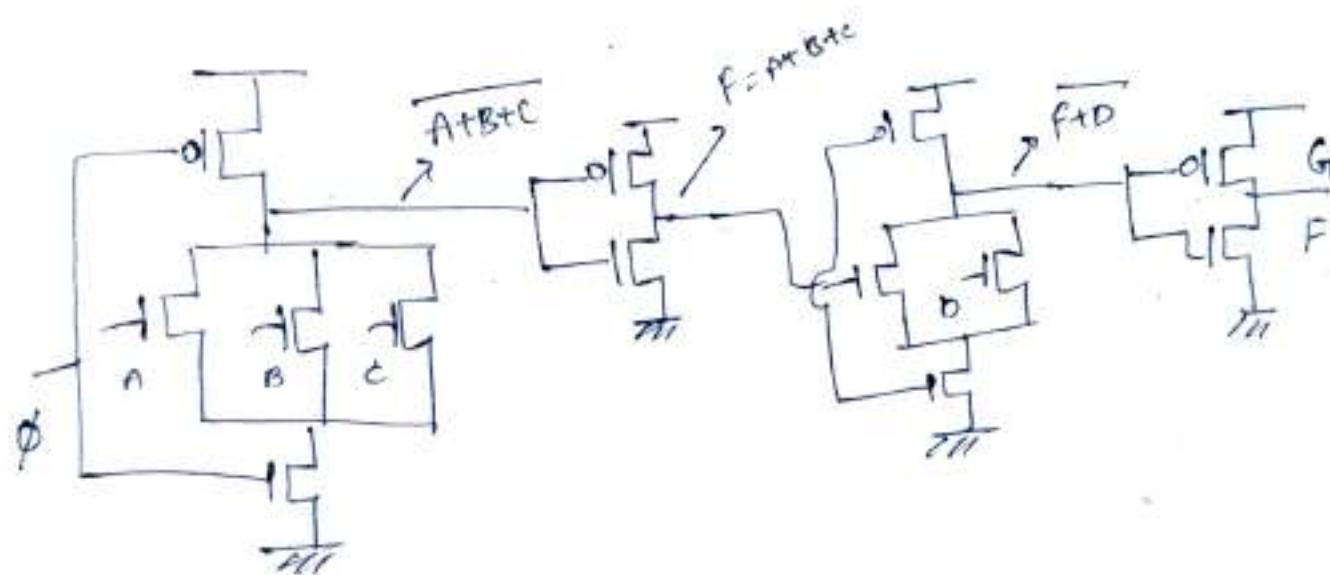
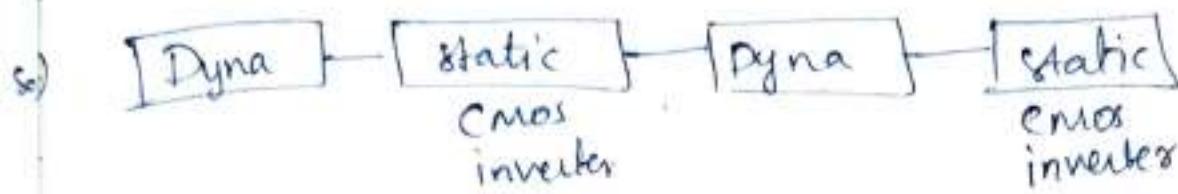
$$g_3 = a_3 b_3$$

$$P_3 = a_3 \oplus b_3$$

$$\begin{matrix} 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{matrix}$$

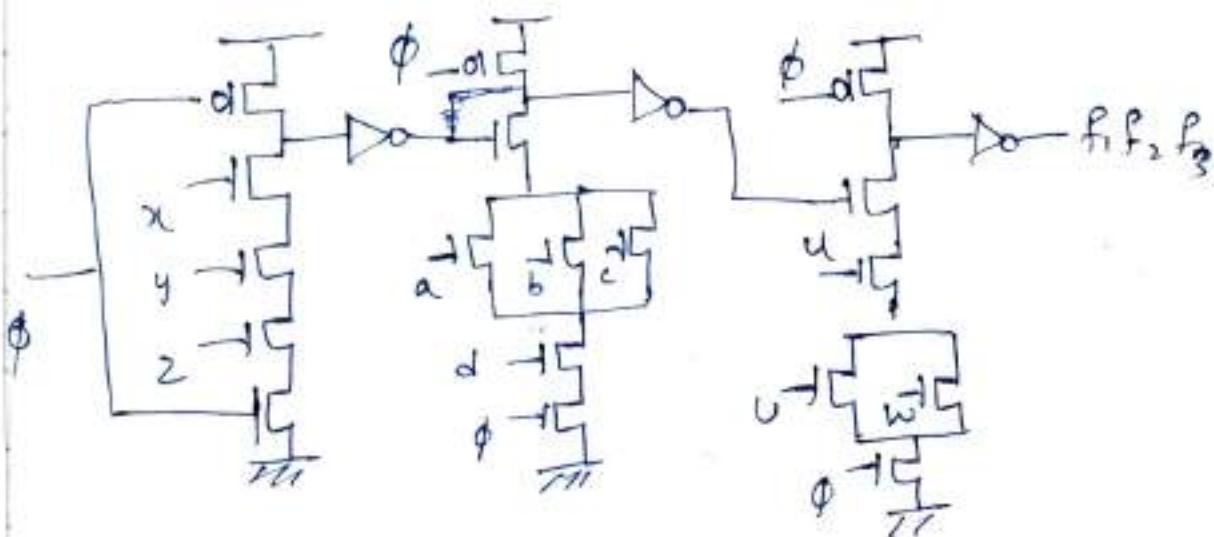
5/11/24

Q1: implement $f = A + B + C$ and $G = A + B + C + D$ using domino logic



Q2: $f_1 = xyz$, $f_2 = (a+b+c)d$, $f_3 = u(v+w)$. $f = f_1 f_2 f_3$

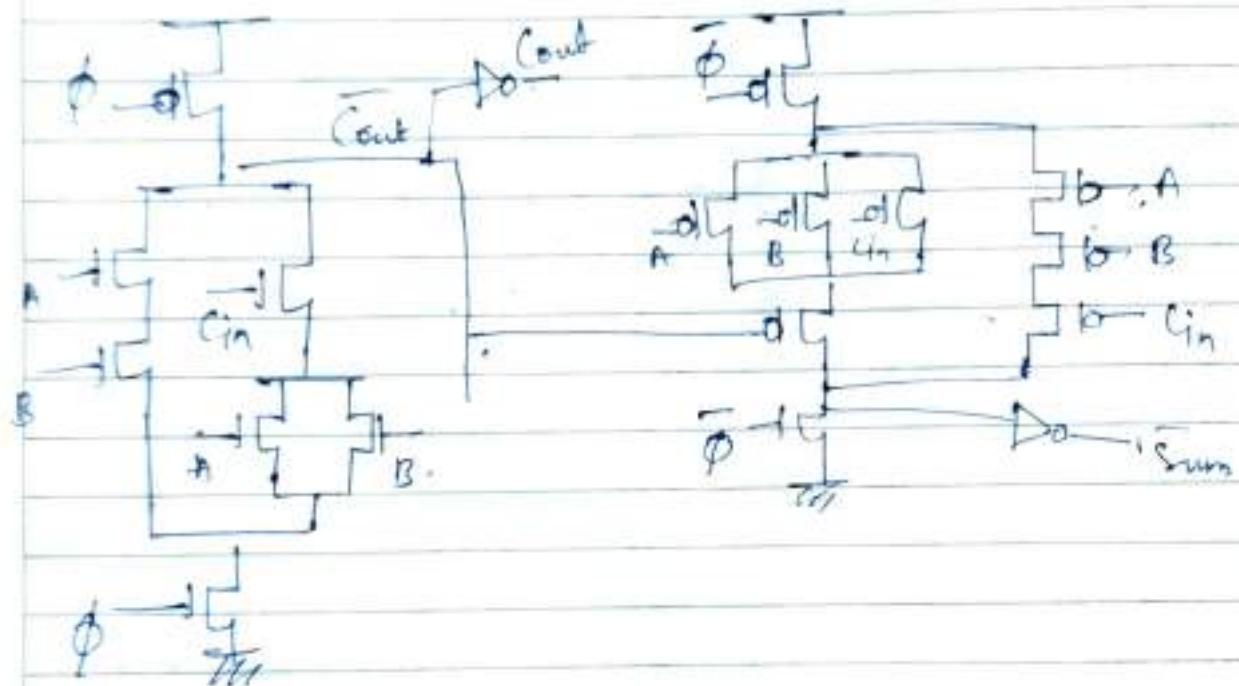
Implement f using domino logic.



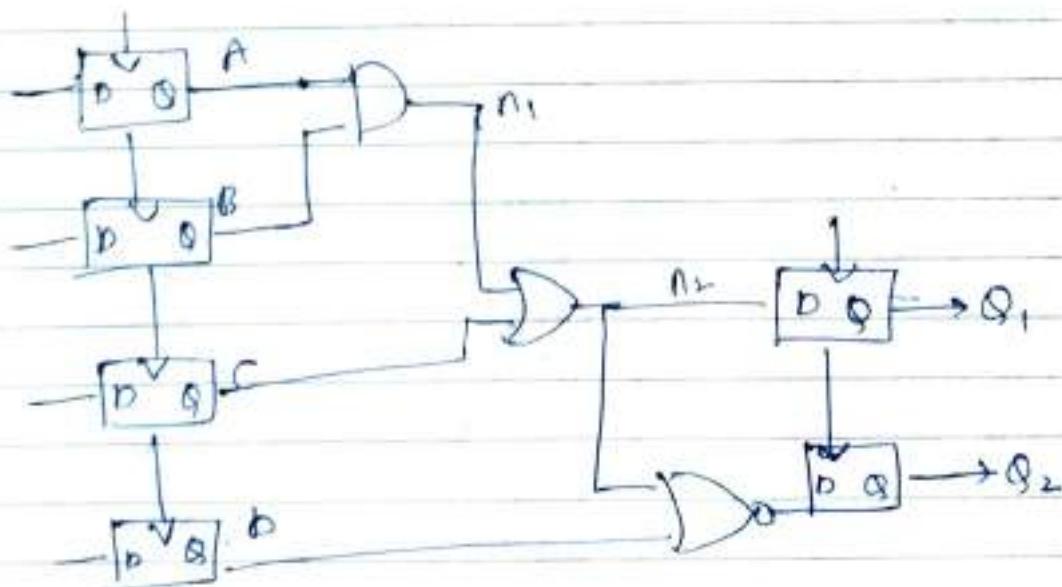
Q) Implement a FA using NOR logic

$$\text{Cout} = \overline{AB} + \text{Cin}(A+B)$$

$$\text{Sum} = ABC\text{cin} + \text{Cout}(A+B+\text{cin})$$



Qb)



all the FF are connected to the same clock.

$$t_{cco} = 30 \text{ ps}$$

gatus

$$t_{pc0} = 80 \text{ ps}$$

$$-t_{PD} = 40 \text{ ps}$$

$$t_{setup} = 50 \text{ ps}$$

$$t_{CD} = 25 \text{ ps}$$

$$t_{hold} = 60 \text{ ps}$$

→ Find the Tclk such that no set up time violation occurs

$$T_{CLK} \geq t_{PC0} + 3t_{PD} + t_{setup}$$

$$T_{CLK} \geq 80 + 3 \cdot 40 + 50$$

$$T_{CLK} \geq 250 \text{ ps}$$

$$f_{CLK} \leq 4 \text{ GHz}$$

b) Does hold time violation occur?

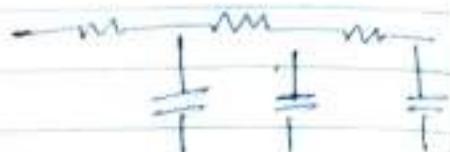
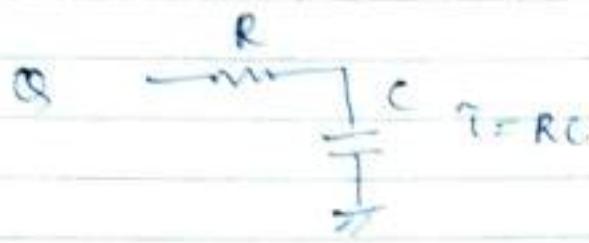
$$t_{cco} + t_{co} \geq t_{hold}$$

$$t_{hold} \leq t_{cco} + t_{co}$$

$$60 \leq 30 + 25$$

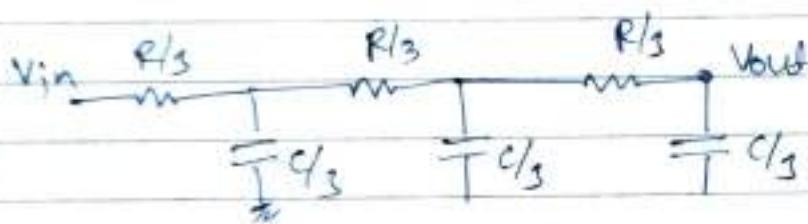
$$\boxed{60 \leq 55}$$

hold time violation occurs



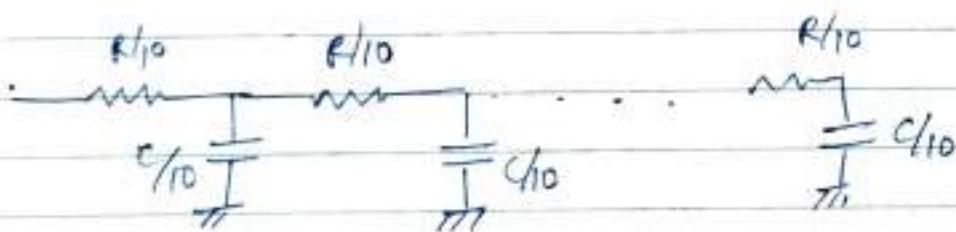
One estimated delay (L-model)

3-section:



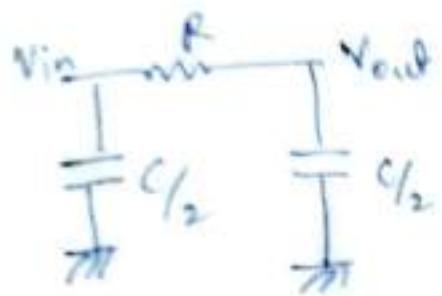
$$\tau = \frac{R}{3}C + \frac{R}{3}\left(\frac{2C}{3}\right) + \frac{R}{3}\left(C\right) = \frac{2RC}{3}$$

10-section

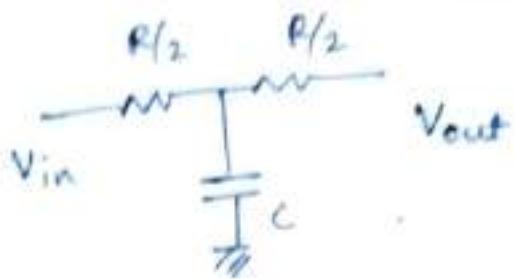


$$\tau = \frac{R}{10}\left(10\frac{C}{10}\right) + \frac{R}{10}\left(9\frac{C}{10}\right) + \frac{R}{10}\left(8\frac{C}{10}\right) + \dots + \frac{R}{10}\left(\frac{C}{10}\right)$$

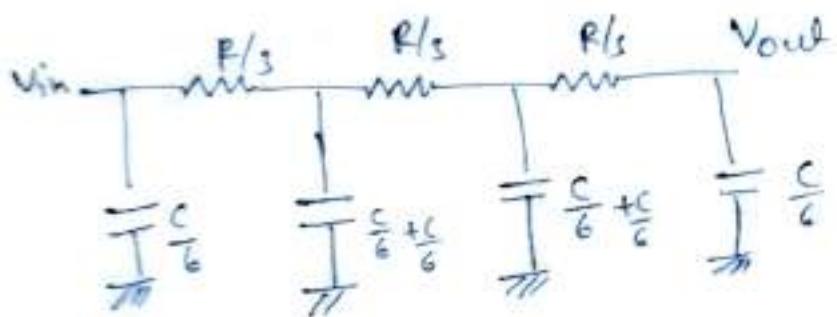
$$= 0.55RC.$$



$$\tilde{\tau} = \frac{RC}{2} \text{ (\pi-model)}$$



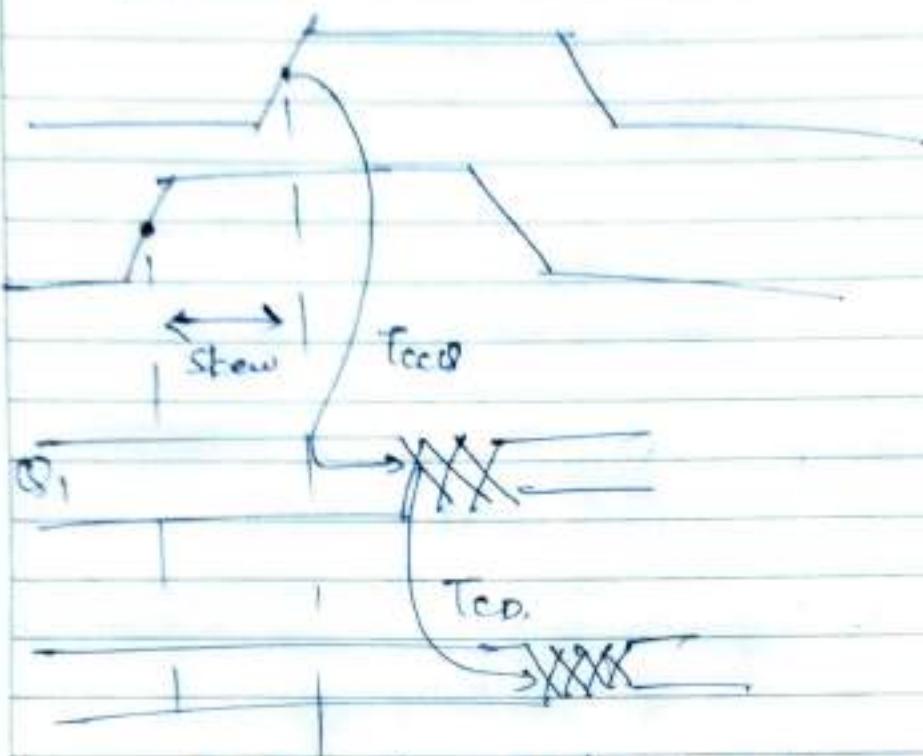
$$\tilde{\tau} = \frac{RC}{2} \text{ (T-model)}$$



$$\tilde{\tau} = \frac{RC}{2}$$

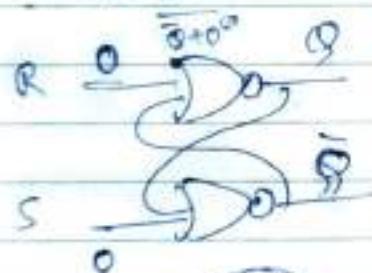
Done

WE Skew



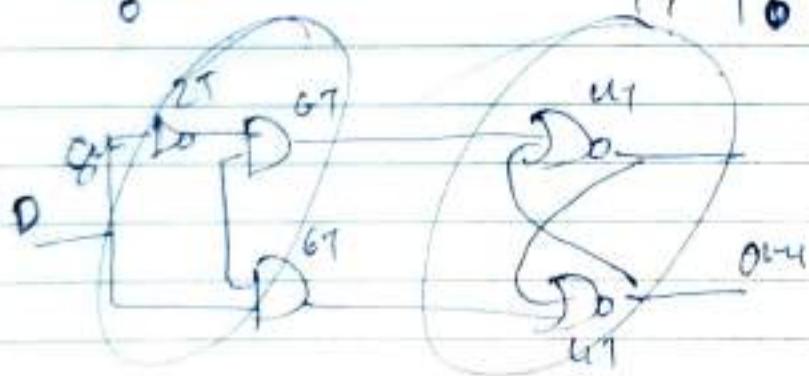
\leftrightarrow Skew & Feed + Tee + Tee

Tead



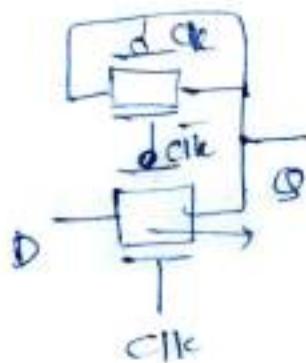
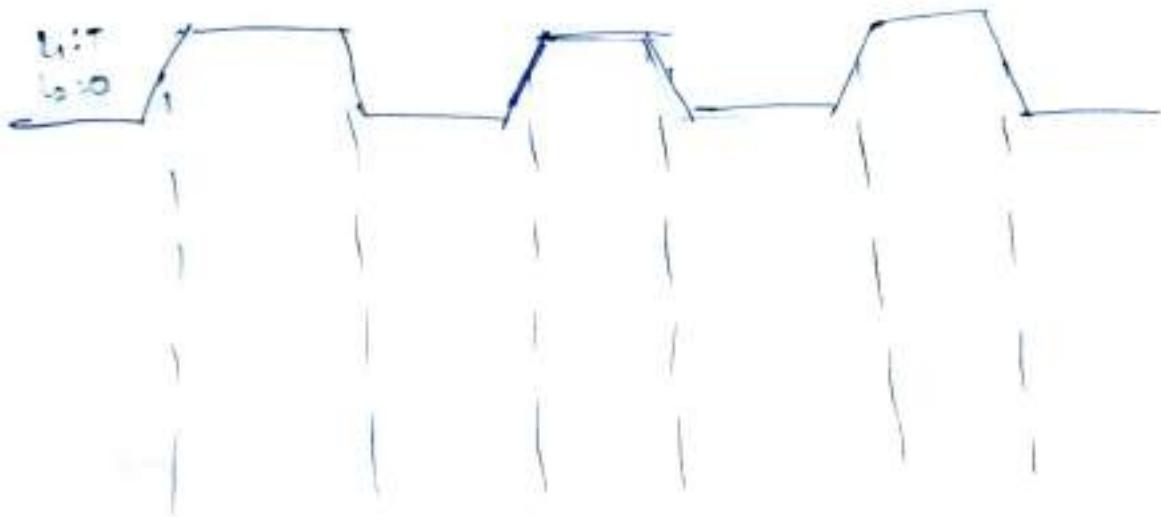
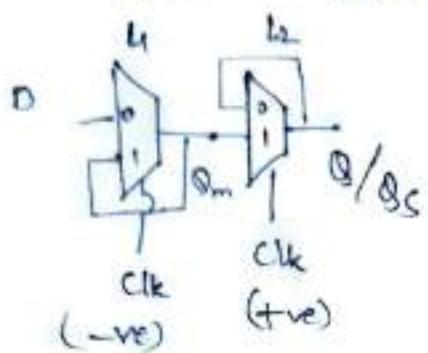
RS	0	0
00	0	0
01	1	0
10	0	1
11	0	0

se



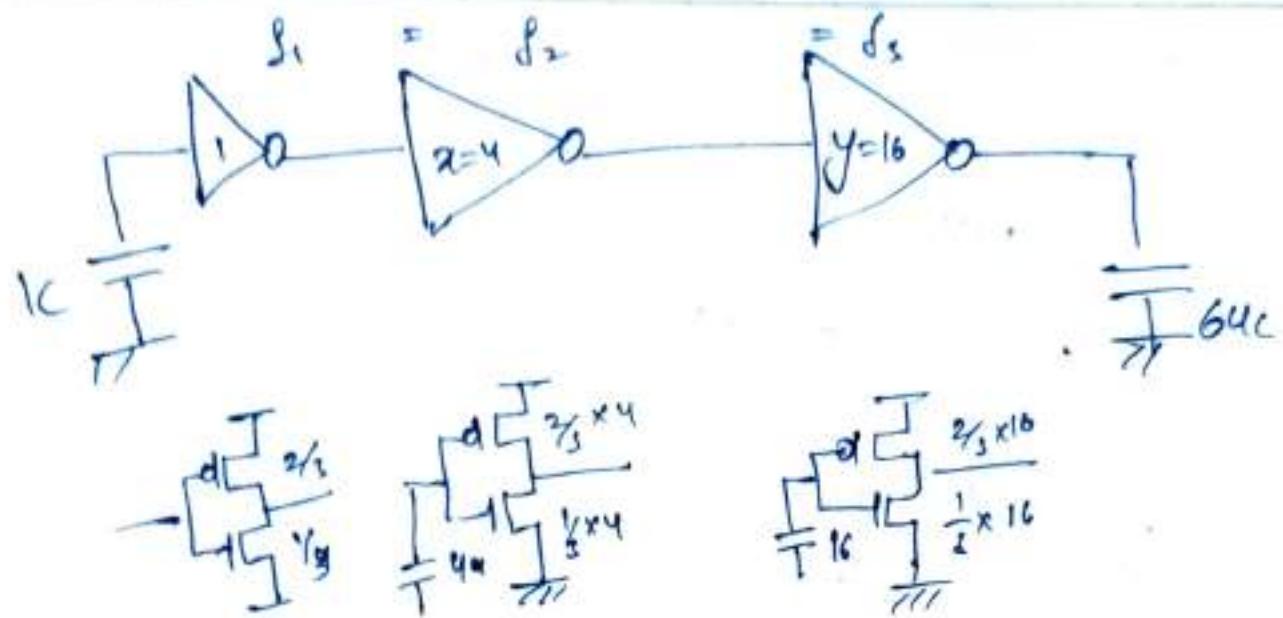
the edge triggered FF

-ve edge triggered Latch +ve edge triggered Latch



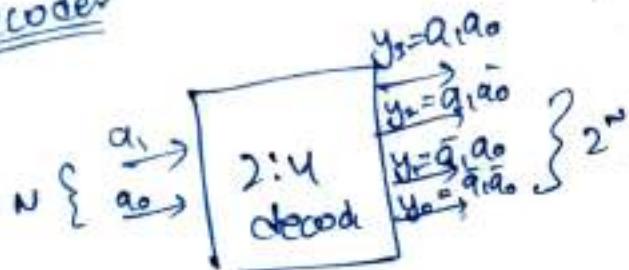
Ck=1

Ck=0



\Rightarrow To have equal stage effort ($f_i = g_i h_i$) input capacitances of successive stages are scaled.

Decoder



a_1	a_0	y_3	y_2	y_1	y_0		$Y = 2^A$
0:	0 0	0	0	0	1	1	
1:	0 1	0	0	1	0	2	
2:	1 0	0	1	0	0	4	
3:	1 1	1	0	0	0	8	