Level-2

FPGAspeaks

August 2023

1 Introduction

In this level you will learn System Design in Verilog. This level is divided into two parts namely **Level-2.A** and **Level-2.B**. In this level Test-Benches are also provided.

2 Pre-requisites

Basic knowledge of Digital System Design. Even if you don't know just learn that particular concept and get started.

3 If Tools are

1. **Linux Ubuntu terminal** : As my laptop also slow downs while using such heavy software, I too have done using terminal. Thus, I have created this Level using terminal.
   Visit my youtube video Click Here
2. **Xilinx Vivado/Xilinx ISE** : If you are using this tools then you have to remove two lines given below in the testbenches provided
   (a) $dumpfile("user-defined-filename.vcd");
   (b) $dumpvars(0,testbenchfilename);

   Also remove $finish in the last
   or else simply watch my video Click Here

4 What you are supposed to do ?

Level-2.A is of basic standard and **Level-2.B** is of medium standard of System Design. In both of this you will find a Order-to-follow.txt file check-out to learn in the sequence.

4.1 Note

Once you are done with this level make Documentation of what you have learnt and upload in your Git-Hub repository in this particular level.