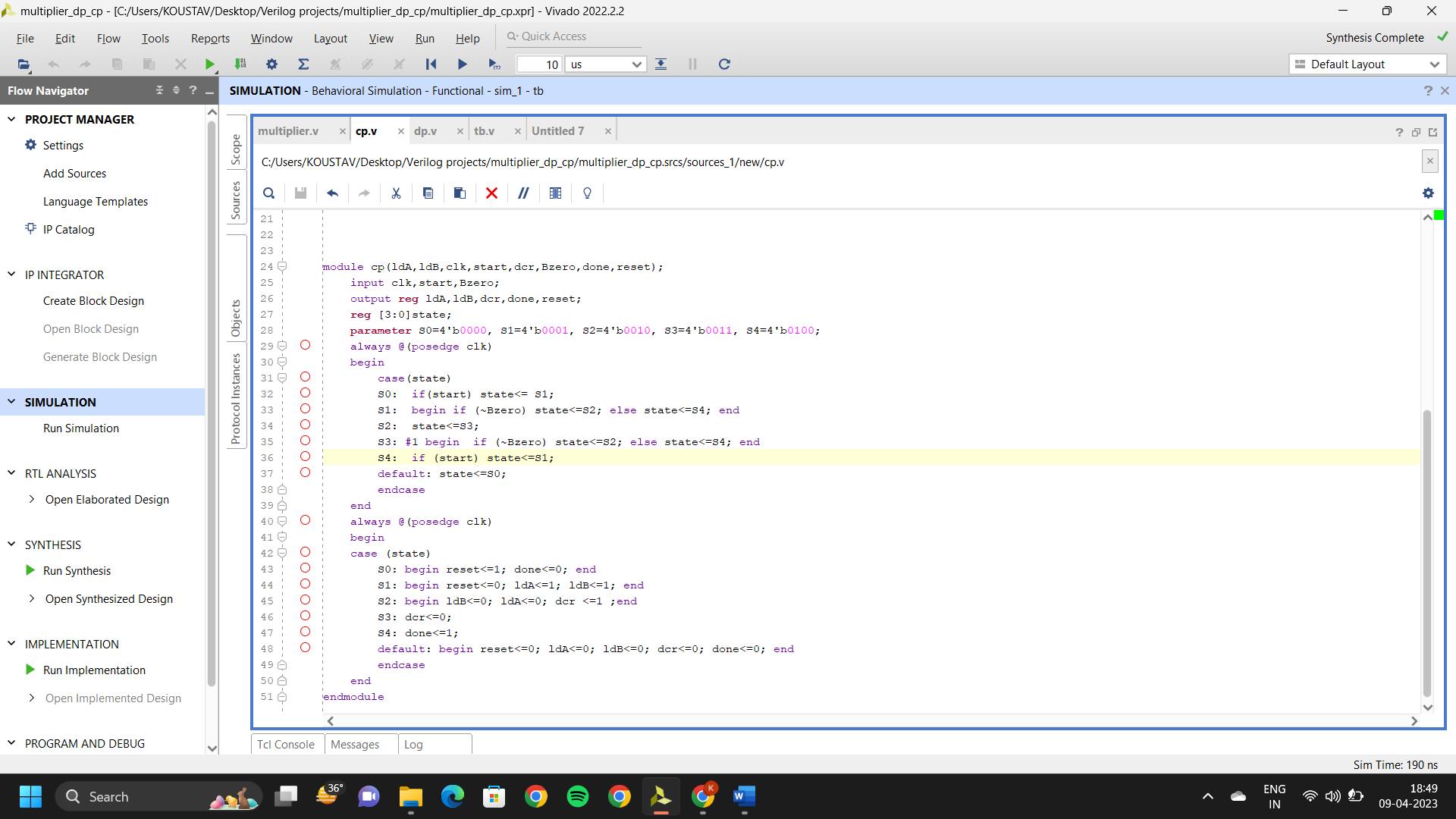
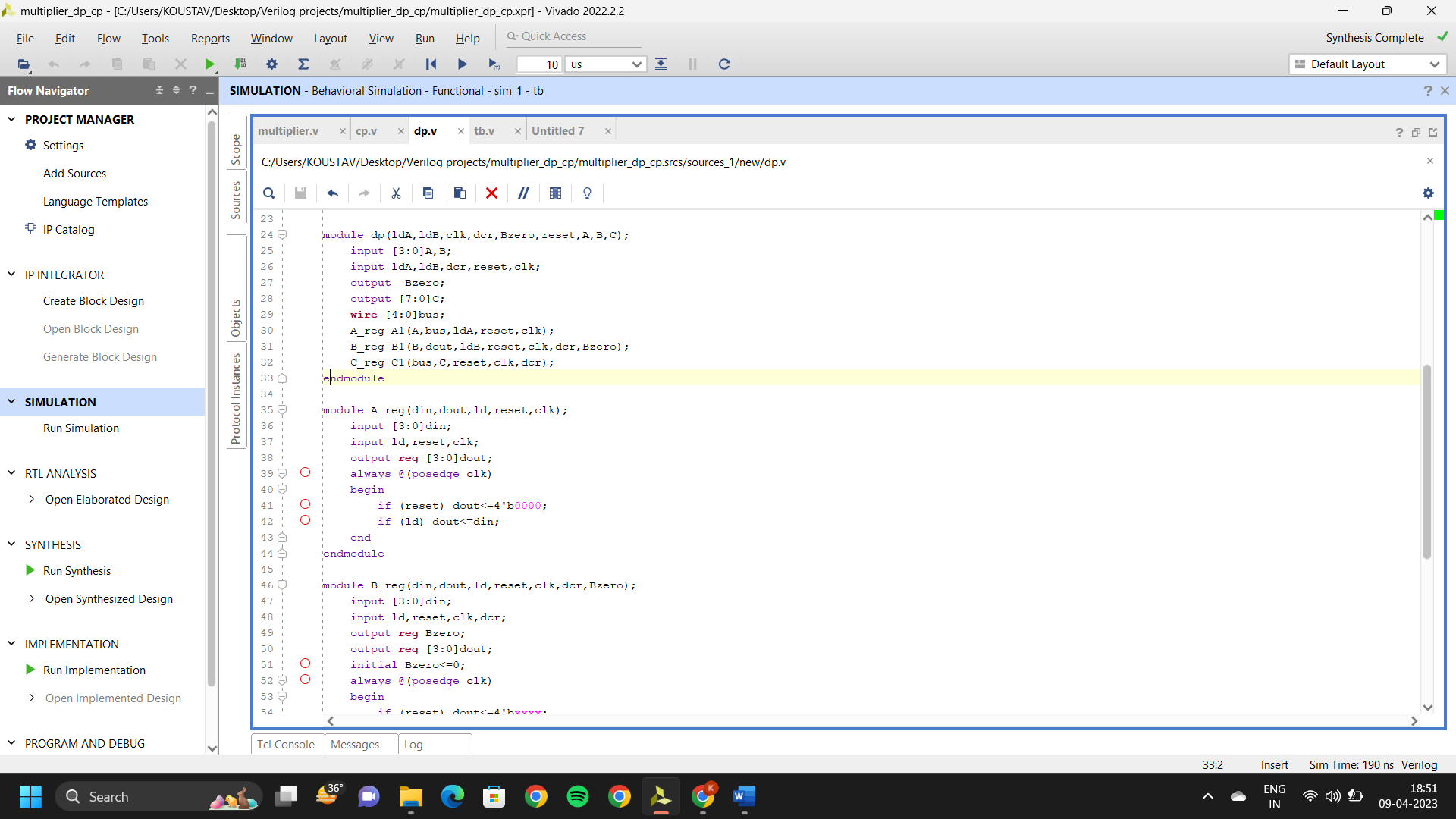
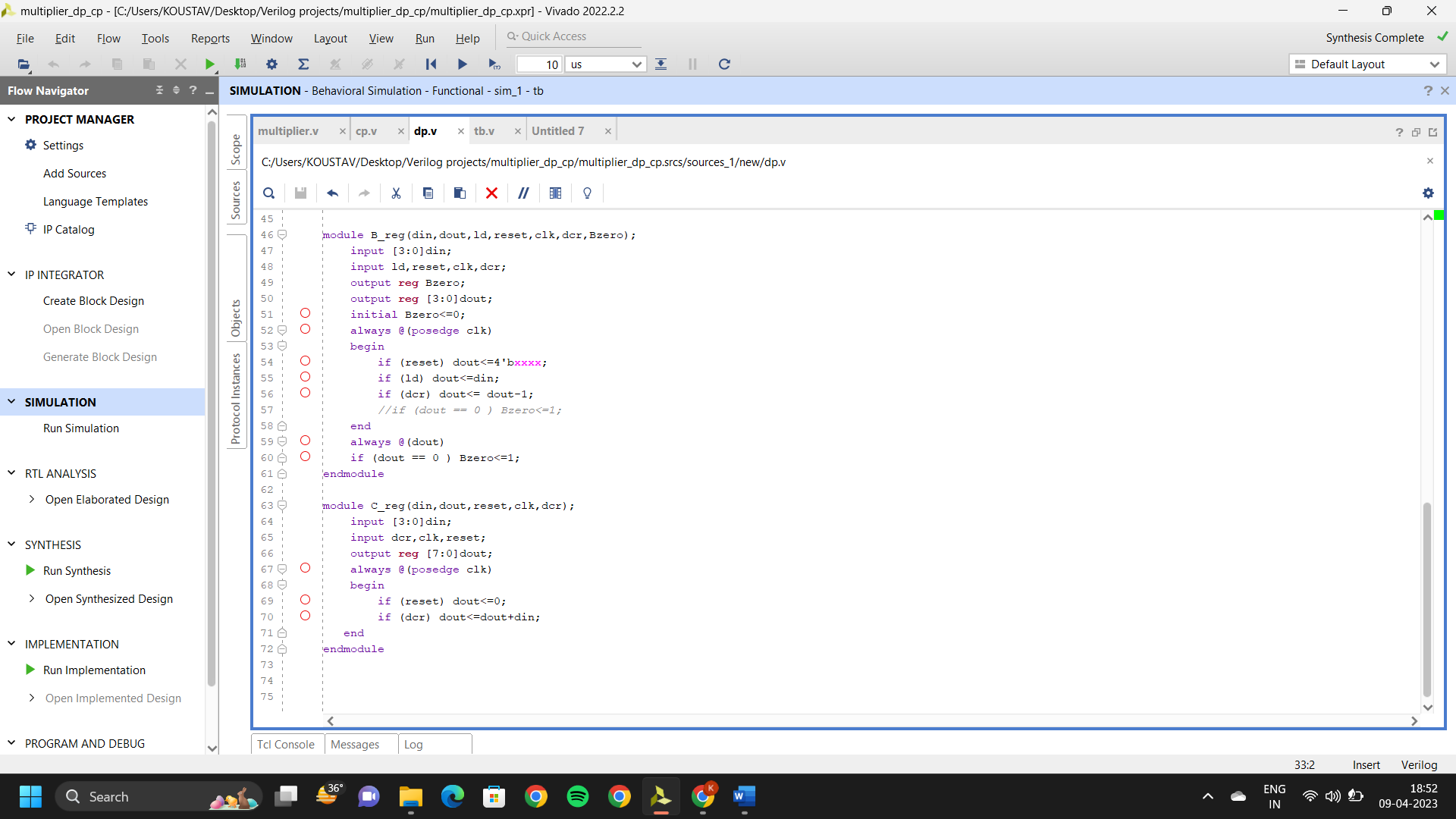
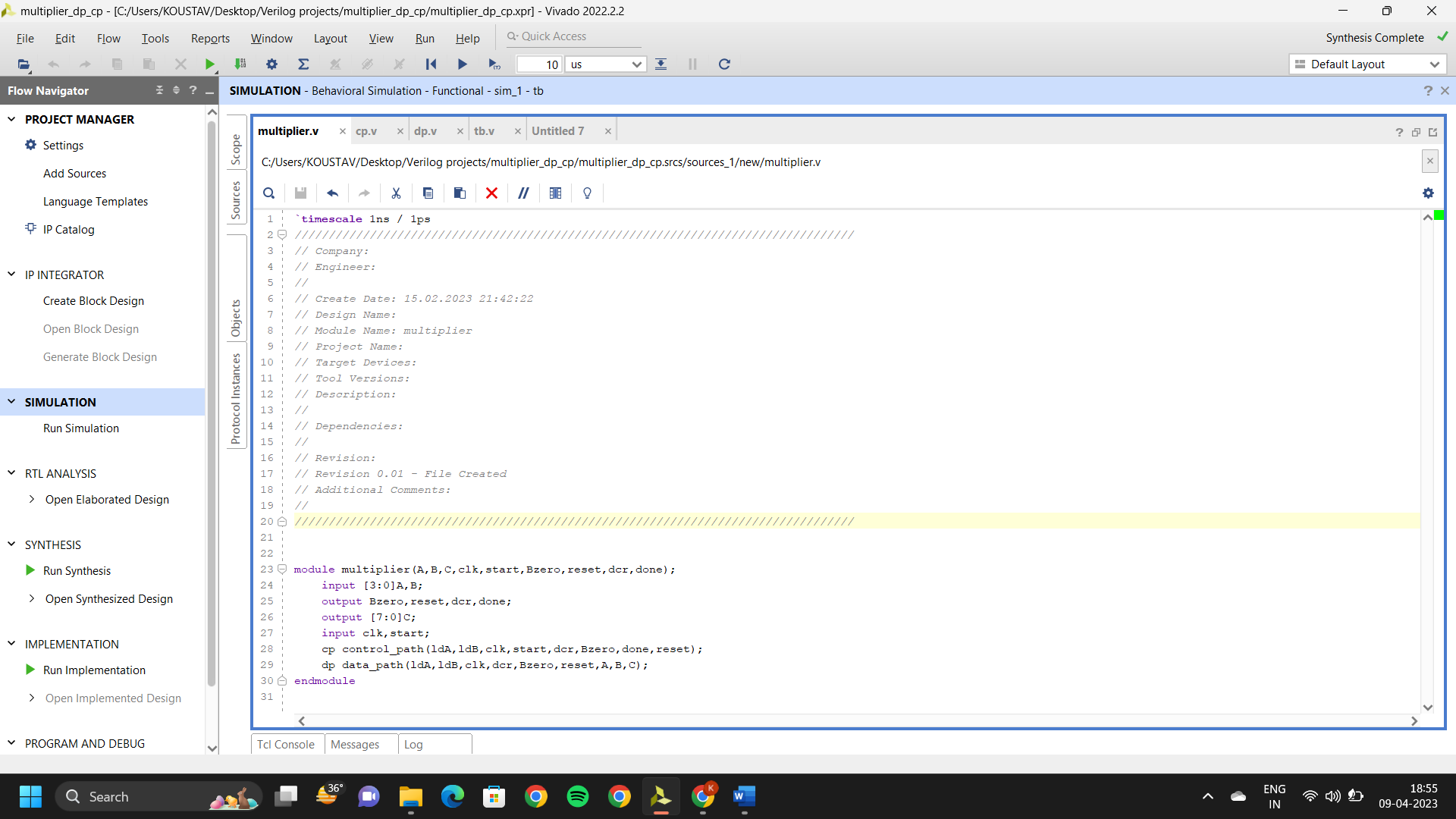
**Multiplier design using controller and data path in Verilog**

**Controller :-**

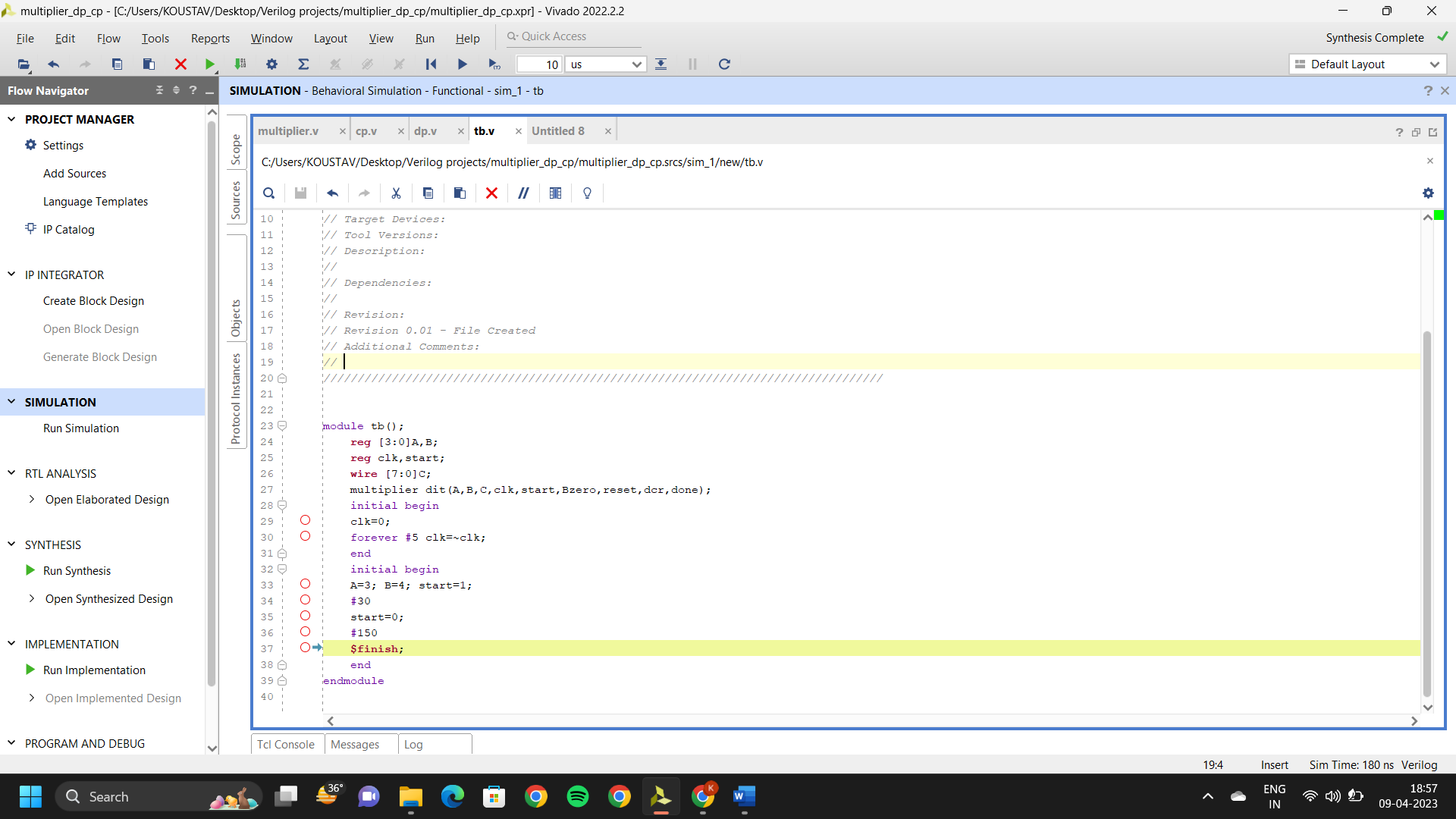
**Data Path :-**

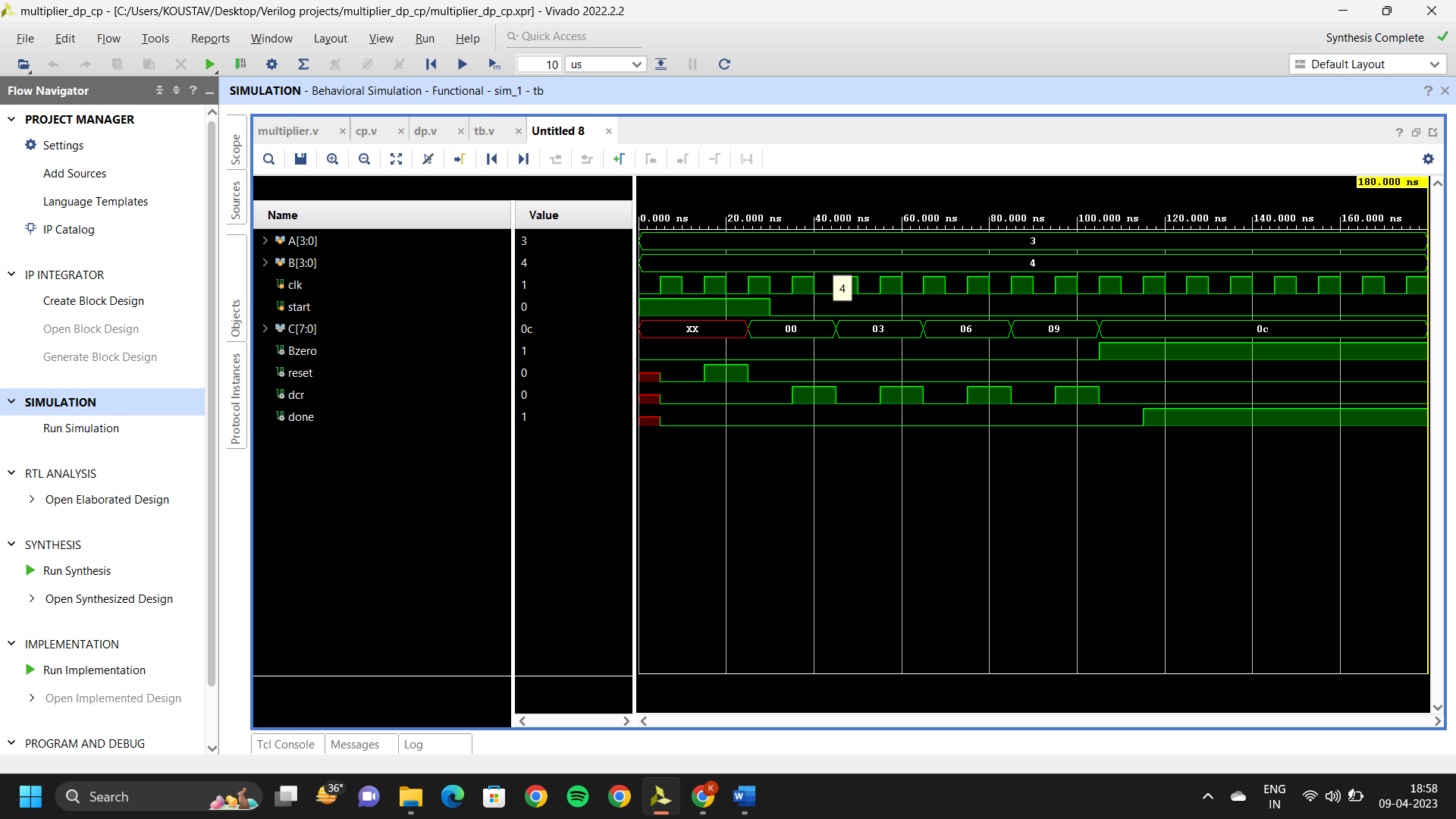


**Top Module :-**



**Test Bench :-**



**Output Waveform :-**