

COMPARISON OF ANTIREFLECTION PROPERTY BETWEEN POROUS Si /Si SURFACE AND POROUS Si ON TEXTURED Si SURFACE

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Abstract: Porous Silicon (PS) layers have been fabricated on p-type crystalline silicon(c-Si) using Reaction Induced Vapour Phase Stain Etching(RIVPSE) and metal induced stain etching on textured surface. The structural and optical properties of porous Silicon on Silicon substrates have been investigated by Optical microscope, Atomic Force Microscope (AFM), photoluminescence (PL) and UV-VIS spectrophotometer. The reflectance spectra has been investigated for three samples (i) PS on Silicon surface(ii)texturing on Pd deposited Si surface(iii) Metal induced Stain etched PS on textured Si surface. The reflectance of simple etched PS layer is 50% lower and the reflectance of simple etching on textured surfaces PS layer is 62.5% lower than the reflectance of pure polished Silicon in wavelength for 300-1200nm. Such low reflectance for both cases can be explained by the roughness of the surface. Porosity and thickness has been studied for different growth condition (different oxidation ratio) using gravimetric method. It has been seen that Porosity and thickness is a function of oxidant ratio. The variation of reflectance is studied with the porosity. It has been seen that the reflectance decreases with increasing porosity .The best antireflection coating is prepared by simple etching by RIVPSE on textured surface.

Keywords: silicon solar cells, photovoltaic, porous silicon, antireflection coating, vapour phase stain etching, texturization

I. INTRODUCTION

Silicon with various structural morphology is widely used for solar cell and other optoelectronics devices. However, flat Si surfaces have a high natural reflectivity. The minimization of reflection loss is of crucial importance for high efficiency solar cell. The reflection loss can reduce by antireflection coatings (AR Coatings).For example, quarter wavelength

transparent layers of SiO_x , TiO_x , ZnO , ITO or Si_3N_4 are regularly used as ARCs on Si. Such coatings perform well only in limited spectral range and for specific angle of incidence. Their typical effect in entire usable spectral range of Si is an average reduction of surface reflection to about 8%-15%. [1] Efficient suppression of reflection in a broad spectral range has been achieved by deep surface texturing.

Several reports concerning use of PS in photovoltaic (PV) devices have been published because of potential advantages of PS. It is already being found that PS as antireflection coating lowers the reflectance in the sensitivity range of solar cell which strongly depends on porosity. The porous silicon (PS) formed by vapour phase stain etching can use as good ARC because this is Si compatible technology, simple and economical than conventional method of porous formation like anodization. Lowering of the reflectance in the sensitivity range of solar cell, which increased the short-circuit current density.

The band gap energy shifts from 1.47 eV for gravimetric density above 40-45% up to 1.8 eV as the density of pores is increased [2]. For this reason the band gap of PS may be optimized for maximum theoretical solar cell efficiency at around 1.5 eV. The last investigation concludes that the electronic band structure show a tendency towards a direct band gap as the porosity increases [3]. PS may be used to convert higher energy solar radiation into the longer wavelength light which is absorbed more efficiently into bulk silicon. While the porosity is changing from 40% to 90% the photoluminescence intensity rises from 10 to 10^6 in arbitrary units [4].It is reported that PS layers have become an attractive material for solar cells because of their band gap broadening, wide optical transmission ranging from 700 to 1000 nm, and surface roughness [5]. The Porous Si (PS) is attractive in solar cell applications due to its efficient ARC and other properties such as band gap broadening, wide absorption spectrum and

optical transmission range (700–1000 nm). It can also be used for surface passivation and texturization[6,7].

The quantum confinement model, a heterojunction can be formed between the Si substrate and porous layers because the latter has a wider band gap (1.8–2.2 eV) compared with crystalline Si (c-Si) [8]. Antireflection Coatings (ARC) could reduce surface reflection, and increase conversion efficiency, extend lifetime and improve the electro-physical and characterization of photovoltaic converters [9]. It is reported that PS layers are an excellent antireflection coating (ARC) for solar cells [10]. The ARC can enhance the efficiency of solar cells by increasing light trapping in the active region [11]. The effect of the porosity of the PS ARC layers on the solar cell efficiency based on the n- and p-type regions with (100) and (111) orientations was investigated[12].

A nanoporous Si layer can be produced in an etching solution with a noble metal catalyst such as Pd, one of the most promising metal with respective low cost. The process can be divided into two steps: (i) deposition of thin noble metal nanoparticles, and (ii) immersion of the sample (silicon wafer) in an KOH solution. The anisotropic etching behavior of crystalline Si in a potassium hydroxide (KOH) solution has been utilized as a tapering process.

In this work, effects of etching time on the nanoporous Si layer (such as surface morphology, etching depth, and the pore diameters) were studied with the developed etching solution. The effect factors of nanoporous silicon on solar cell properties were also studied.

The purpose of the work is to improve the performance of solar cells by incorporating a method by forming a porous silicon (PS) layer as ARC on the top surface of large area p type silicon by comparing of antireflection property of PS-Si surface and PS on textured Si surface. Reflectivity measurements are presented in order to evaluate the effectiveness of PS layer as antireflection coating.

In this paper, the synthesis and characterization of vapour phase stain etched crystalline porous silicon layers is done. In section two, the experimental method for the preparation of porous silicon layer in different methods are presented. Results and discussions are summarized in section third. Finally, section fourth concludes the paper.

II. EXPERIMENTAL

RIVPSE etching

A PS layer was fabricated by RIVPSE process of a P-type c-Si (orientation :100, boron doped, double side

polished surface) wafer with a resistivity of 3-10 Ohm-cm and a thickness of 300 micro meter. Initially, the c-Si wafer was cleaned to remove the oxide layer and contaminants on the surface of wafer using the Radio Corporation of America method. Then, the c-Si samples were dipped in a solution of HF:H₂O (1:10) at 27 °C to remove the native oxide. PS can be formed by electrochemical or chemical etching in HF-based solution. In the first case, applying a positive bias delivers holes to the Si surface, which results in an attack of the Si-H bonds on the Si surface in such a way that the hydrogen is replaced by fluorine coming from the HF solution. The same mechanism of Si dissolution occurs during chemical or stain etching in HF-HNO₃ mixtures. The difference is that the role of current in the chemical method is played by HNO₃. Nitric acid as a strong oxidizing agent injects holes into the Si and then the dissolution reaction occurs in a similar way as in the electrochemical process.

Optimization of growth of porous silicon is done by taking three parameters in RIVPSE, such as oxidant ratio, etching time, height of sample from liquid level. Finally, the samples were rinsed with DI water and subjected to further investigation.

Best bright luminescence come under the UV light from PS substrate which was exposed 4 minute to the acidic vapor with oxidant ratio (HF:HNO₃) 6:1 and 8.4 cm distance between silicon surface and electrolyte solution. Reflectivity measurements were performed using “SHEMADZU UV/VIS Spectrophotometer” (Model: SolidSpec-3700 Series) over the 300 nm to 1200 nm wavelength range. The AFM images are taken using NTEGRA Atomic Force Microscope.

Textured Silicon surface by anisotropic etching

The samples were initially cleaned using RCA Cleaning to remove the oxide layer and contaminants on the surface of Si sample. Thereafter the samples were then thoroughly rinsed with deionized (DI) water. Then the samples were dipped into PdCl₂ and HCL solution for different time (4 min, 6 min) at 75⁰ C temperature to allow the deposition of the Pd nanoparticle layer on the Si substrate. Then the Si surfaces were etched with a KOH solution at nearly 80⁰ C for approximately 20 min. Finally, the samples were rinsed with DI water.

RIVPSE on textured Silicon surface

After dipping into KOH solution to texture the Silicon surface was exposed for 4 minute to the acidic vapor with oxidant ratio (HF:HNO₃) 6:1 and 8.4 cm distance between silicon surface and electrolyte solution(RIVPSE). Finally, the samples were rinsed with DI water.

III. RESULT AND DISCUSSION

Morphology of VE-based Porous Silicon

Optical Microscope picture

Figure 1 and Figure 1a shows the optical microscope image of a Porous silicon surface with oxidant ratio 6:1, etching time 4 minutes and 8.4 cm height. Here Zn as a metal to induce the reaction is added (1.68 gm) for one time only during the RIVPSE. There is a high possibility to form a single etched PS layer by adding Zn for only one time. In Figure 1a the more clear view of pores has been shown. There are some crystallite structures in some places throughout the surface.

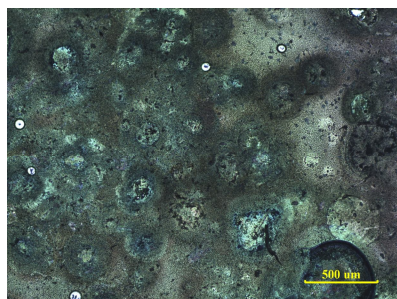


Figure1: Optical microscope picture of RIVPSE on p type Silicon surface

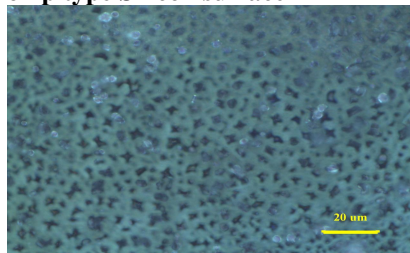


Figure1a: Optical microscope picture of RIVPSE on p type Silicon surface

Figure 2 and Figure 2a shows the optical microscope image of a Porous silicon surface prepared by RIVPSE (with oxidant ratio 6:1, etching time 4 minutes and 8.4 cm height) on textured p type Silicon surface. Here Zn as a metal to induce the reaction is added (1.68gm) for one time only during the RIVPSE. There is a high possibility to form a single etched PS layer by adding Zn for only one time. In Figure 2a the more clear view of pores has been shown. The structure of pores are more uniform and small throughout the surface due to texturing before RIVPSE.

Figure 3 and Figure 3a shows the optical microscope image of a Porous silicon surface prepared by RIVPSE (with oxidant ratio 6:1, etching time 4 minutes and 8.4 cm height) on textured p type Silicon

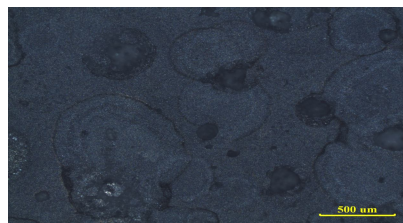


Figure2: Optical microscope picture of RIVPSE on textured p type Silicon surface

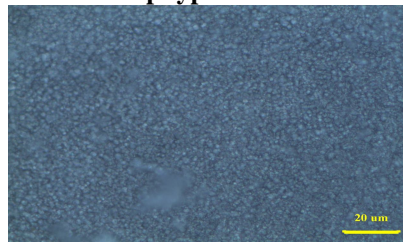


Figure2a: Optical microscope picture of RIVPSE on textured p type Silicon surface

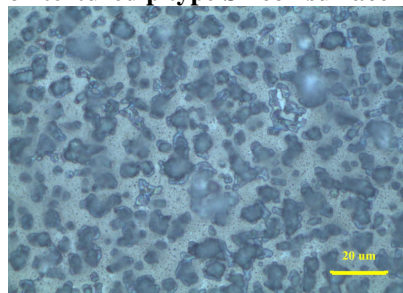


Figure3: Optical microscope picture of RIVPSE on textured p type Silicon (after dipping into PdCl₂ solution)

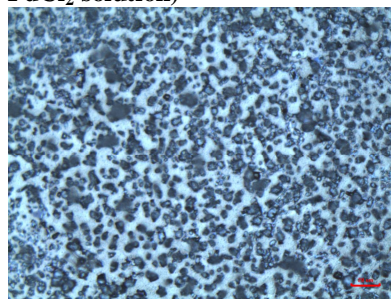


Figure3a: Optical microscope picture of RIVPSE on textured p type Silicon

surface after dipping into PdCl₂ solution. Here Zn as a metal to induce the reaction is added (1.68gm) for one time only during the RIVPSE. There is a high possibility to form a single etched PS layer by adding Zn for only one time. In Figure 3a the more clear view of pores has been shown. The structure of pores may be nano pore and more uniform throughout the surface due to dipping PdCl₂ solution before texturing followed by RIVPSE.

AFM IMAGE

AFM image of textured Silicon surface:

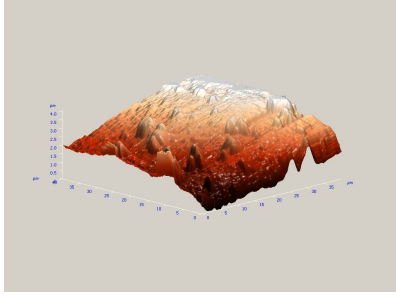


Figure4: 3D AFM image of textured Silicon surface

Figure 4 shows the 3D AFM image of textured Silicon surface. Figure 4a shows the 2D image of the surface and the histogram which shows that the average roughness of the surface is 328.02 nm.

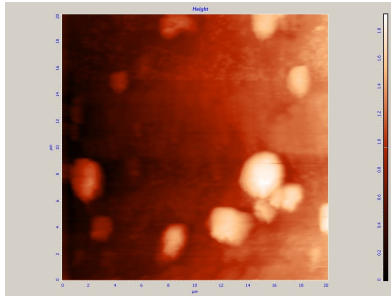


Figure4a:2D AFM image of textured Silicon surface

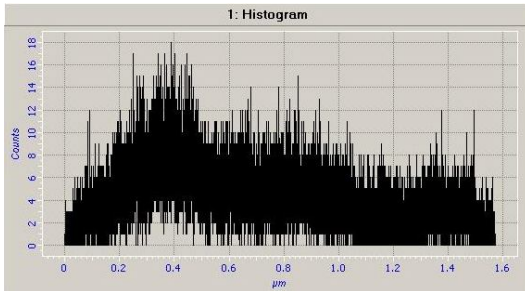


Figure4b: Histogram of average roughness of textured Silicon surface

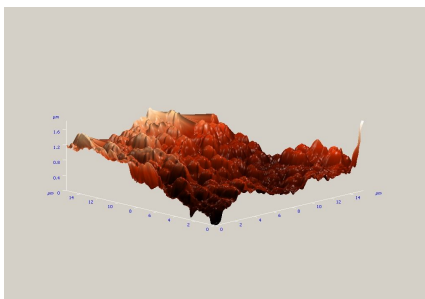


Figure5: 3D AFM picture of RIVPSE on textured Silicon (after dipping into PdCl₂ solution)

Figure 5 shows the three dimensional topographic image of PS etched surfaces with the pyramidal shape distributed over the entire surface. The pyramidal shape indicates that the increase in surface roughness is because of effect of etching parameters on surface characterization. The high degree of roughness of PS surface implies the possibility of using the porous layer as an ARC because the surface texture reduces light reflection. The scattering in PS is possibly because of roughness in relation to the thickness of PS layer.

Rough surfaces with spikes and pyramid like hillocks typical size of several micrometers exhibit a reduced reflectivity due to multiple reflection and absorption.

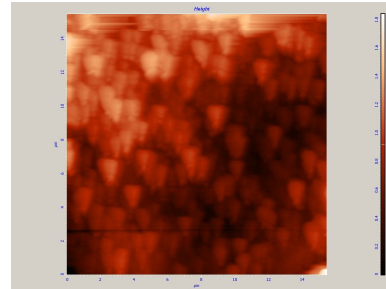


Figure5a: 2D AFM picture of RIVPSE on textured Silicon (after dipping into PdCl₂ solution)

Thickness and Porosity

Thickness and porosity of samples were calculated by gravimetric method. The samples are weighted before etching (m_1), just after etching (m_2) and after dissolution of porous Silicon layer in a molar KOH solution (m_3). The porosity and thickness are given by the following equations (1) and (2), respectively.

$$p(\%) = \frac{m_1 - m_2}{m_1 - m_3} * 100 \quad \dots (1)$$

$$d = \frac{m_1 - m_3}{\rho_s} \quad \dots (2)$$

Where ρ is Si density and S the porous Surface.

The variation of porosity and thickness is shown in Figure6, Figure 7 respectively and the numerical values are presented in Table (1).

Table 1: Porosity and Thickness of PS Samples in different oxidant ratio

oxidant ratio	Time	Porosity	Thickness(μm)
4:1	4 min	44%	1.24
6:1	4 min	50%	2.32
8:1	4 min	67%	3.48

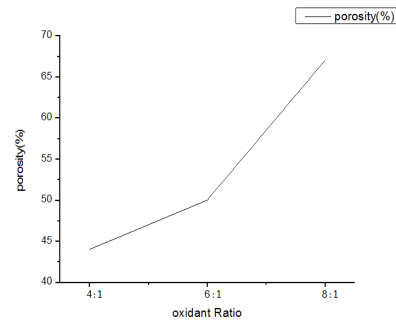


Figure 6: Porosity as a function of oxidant ratio



Figure 7: Thickness as a function of oxidant ratio

It can be noted that the porosity is increased rapidly with increasing of the oxidant ratio. The average thickness of Psi layers grows linearly by increasing the oxidant ratio.

Optical Properties

The optical characteristics of VE-based PS layers were examined by measuring the optical reflectance. The Reflectance measurements were performed using a “SHEMADZU UV/VIS Spectrophotometer” (Model: SolidSpec-3700 Series) over the 300 nm to 1200 nm wavelength range. Figure 8 displays diffused light reflectance values for different porous Si layer. In comparing Figure 8 and Figure 9, one can remark the important decrease of reflectance values when polished Silicon wafers are etched by RIVPSE. The Figure 9 shows that the reflectance values of simple etching on textured surfaces with different condition are much lower than those of their corresponding simple etched PS surface. The reflectance of simple etched PS layer is 50% lower than pure polished Silicon. The reflectance of simple etching on textured surfaces PS layer is 62.5% lower than pure polished Silicon. Such low reflectance for both simple etching by RIVPSE and simple etching on textured surface can be explained by the roughness of the surface

Table 2: Porosity of samples for different oxidation ratio of Figure 8

NAME OF SAMPLE	POROSITY
S1	Plain Si
S2(4:1)	44%
S3(6:1)	50%
S4(8:1)	67%

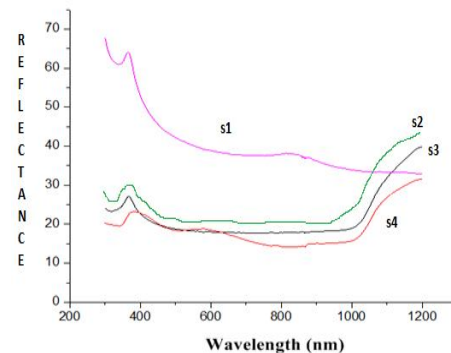


Figure 8: The reflection spectra of PS samples each under different oxidation ratio compared (different porosity) with the c Si sample

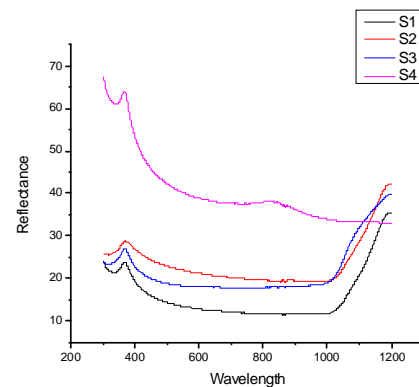


Figure 9: The reflection spectra of different PS samples

Table 3: Sample name and specification of Fig 9

NAME OF SAMPLE	SAMPLE SPECIFICATION
S1	Plain Si
S2	PS on Silicon surface
S3	Metal induced Stain etched PS on textured Si surface (Zn added continuously) RIVPSE (6:1, 4 min)
S4	Metal induced Stain etched PS on textured Si surface (Zn added for one time only) RIVPSE (6:1, 4 min)

PL Measurement

The photoluminescence (PL) measurements in room temperature has been carried out by using HeAg leaser of wavelength 224 nm as the excitation source for all samples. The PL peak corresponding to orange and yellow emission is observed at 612 nm and 584 nm respectively which is due to the nano-scaled size of silicon through quantum confinement effect .The PL intensity is increased in very high value when metal (Zn) is added for only one time in RIVPSE (6:1, 4 min) than continuously adding metal during etching.

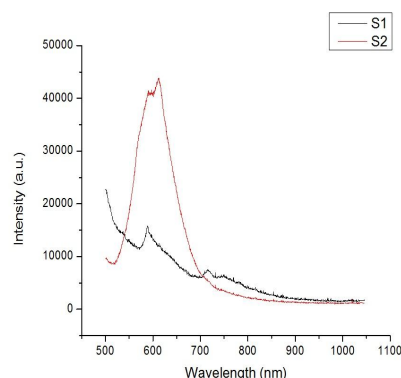


Figure 10: The photoluminescence spectra of different PS samples

Table4:Sample name and specification of Fig 10

NAME OF SAMPLE	SAMPLE SPECIFICATION (RIVPSE-6:1-4min)	Max PL PEAK	
		WAVELENGTH	INTENSITY
S1	Zn added continuously	584.6nm	14020.92 a.u.
S2	Zn added for one time only	612.95 nm	43837.12 a.u.

IV CONCLUSION

It has been shown that metal induced Stain etched PS on textured Si surface has a large potential as ARC in photovoltaics. The reflectance of simple etched PS layer is 50% lower and the reflectance of simple etching on textured surfaces PS layer is 62.5% lower than the reflectance of pure polished Silicon in wavelength for 300-1200nm. It has been seen that Porosity and thickness is a function of oxidant ratio. The reflectance of PS layer decreases with increasing the porosity. A simple etching on textured surfaces leading to PS layer provides reduced reflectance. Performance similar to the conventional ARC and, at the same time substantial simplification of the process may help to improve the conversion

efficiency of Solar cell. The detailed morphological studies of crystallite structures in grown sample(shown in Figure:1a) can be done by using Scanning Electron Microscope in future.

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