Design of Combinational and Sequential Circuits using Threshold Logic

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Abstract— **In this paper we propose the implementation techniques for both combinational and sequential circuits using threshold logic. With the advancement of nano technology threshold-gate based logic design has got a new direction. In this paper capacitive threshold gate based one bit full-adder has been designed first. A two bit synchronous counter has been designed then. Finally threshold gate based four bit ring counter and Johnson counter have been realized in a single circuit. The proposed design has been verified by means of simulation using PSPICE and VHDL.**

Words— Adder, Counter, Threshold Logic(TL) Gates, Very Large Scale Integration(VLSI), Linear threshold gate (LTG)

I. INTRODUCTION

Threshold logic (TL) was introduced over six decades ago. There are many theoretical results showing that TL circuits are more powerful than classical Boolean circuits. However different TL gate realizations are made in recent papers [1] [2] [3] [4] [5]. A number of applications based on TL gates have proved its ability to achieve high operating speed and significantly reduced area compared to conventional logic [6] [16]. Many complex functions can be synthesized in TL with lesser no of gates in a shorter logic depth [7] [8] [9]. The higher the logic depth of Boolean functions, the greater the relative advantage of TL. Also it offers much larger fan-in in comparison with the conventional logic gates. A logical function which is linearly separable can be designed using threshold logic [14]. The design style of latches and flip-flops using threshold logic are already reported [10] [11] [15]. In this paper design of a full adder and different types of counters using threshold logic are presented.

Section II Definition of threshold logic.

Section III Investigates the threshold gate based one bit Full-Adder and its output waveforms.

Section IV Investigates the threshold gate based two bit synchronous counter.

Section V Investigates the threshold gate based four bit Ring Counter and Johnson counter.

Section VI Gives the conclusion of the whole experiment.

II. DEFINITION OF THRESHOLD LOGIC

A linear threshold gate (LTG) is an n binary input and one binary output function.

Threshold Logic Gates are devices that are able to compute any linearly separable Boolean function given by-

$$Y = \text{sgn}\{F(x)\} = \begin{cases} 0, & \text{if } F(x) < 0 \\ 1, & \text{if } F(x) \geq 0 \end{cases} \quad (1)$$

$$F(x) = \sum_{i=1}^{n} w_i x_i - \psi \quad (2)$$

Where x_i is the n Boolean inputs and 'w'_i is the corresponding n integer weights. The TG compares the weighted sum of inputs and the threshold value ψ. If the weighted sum of inputs is greater than or equal to the threshold, the gate produces a logic 1. Otherwise, the output is logic 0. The threshold gate can be implemented using both positive and negative weights. Due to the passive nature of the threshold gate buffers are required for the gates to operate correctly in networks[12]. The basic Boolean logic functions AND,OR,NAND,NOR and NOT can be represented in the form of (1) and (2) as follows

AND(x1, x2) =sgn{ x1+ x2-1.5} (3)
OR(x1, x2) =sgn{ x1+ x2-0.5} (4)
NAND(x1, x2) =sgn{- x1- x2+1.5} (5)
NOR(x1, x2) =sgn{- x1- x2+0.5} (6)
NOT (x1) =sgn{- x1+0.5} (7)

We can implement these basic logic functions with threshold gate as shown in fig. 1. In this diagram AND gate is designed. Other gates can be also designed by changing the weights and threshold values.

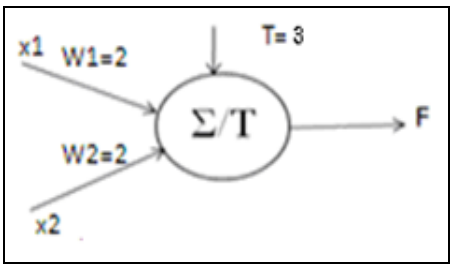

Fig 1: Design of Threshold logic based AND gate

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III. THRESHOLD LOGIC BASED ONE BIT FULL ADDER

The simplest combinational circuit which performs the arithmetic addition of two binary digits is called an *Adder*. A *full-adder* is a combinational circuit that performs the arithmetic sum of three inputs bits and produces a sum output and a carry.

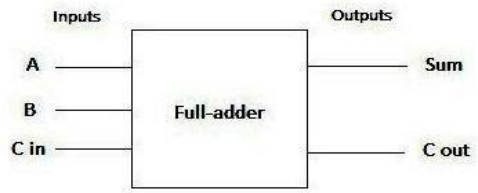

Fig 2: Block diagram of Full Adder

It consists of three inputs and two outputs. The three inputs variables denoted by *A* (Augend bit) and *B* (Addend bit) and the third input C_{in} represents the carry from the previous lower significant position. The outputs are designated by the symbol Sum (for sum) and C_{out} (for carry).

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth table for 1-bit Full Adder

The logic expressions for Cout and Sum are
Cout= AB+BCin+ACin
Sum= A ⊕ B ⊕ C = ABCin + (A+B+Cin)C'out

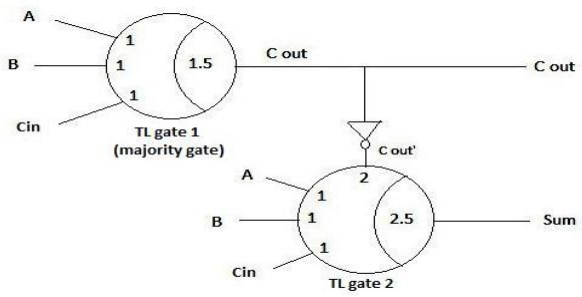

Fig 3: Threshold Logic Gate representation of Sum and Carry

Here the Threshold logic is implemented by capacitors, which determines the weights and the Threshold value (ψ) is determined by the reference voltage (Vref) we have taken.

Where, $\mathbf{Vref = (\psi * V_{dd})/ \sum_{i=1}^{n} wi}$

The basic AND gate operation using Capacitive TL gate has been shown in fig 4[3] .

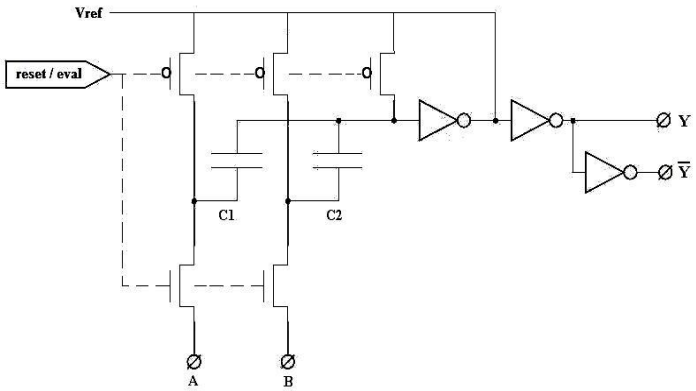

Figure 4: AND gate implementation using Capacitive Threshold Logic.

The threshold gate based one bit Full-Adder is implemented as shown in fig. 5, where the value of V_{dd} and V_{ref} are taken 3.3v and 1.65v respectively and the value of all the capacitors are taken 5fF and C7=10fF.

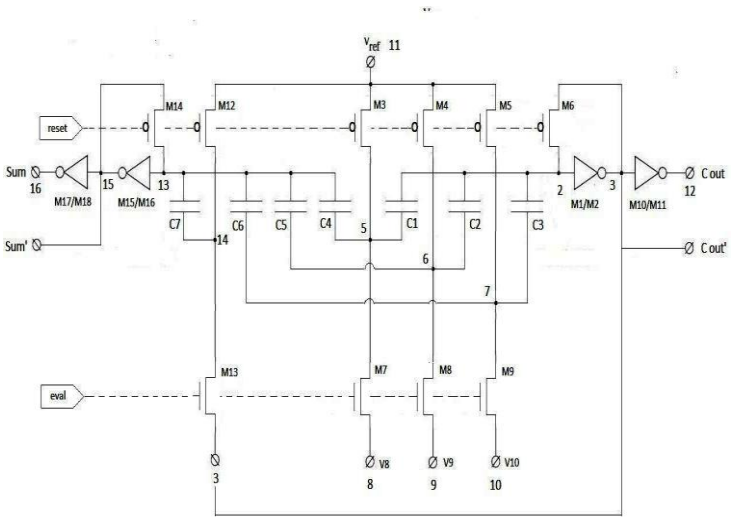

Figure 5: One Bit Full Adder using Capacitive Threshold Logic.

We have verified One Bit Full Adder implementation by using the PSPICE simulator. The Addend, Augend and the input Carry bit is shown in fig. 6, fig. 7 and fig. 8 and the Sum and Carry output results obtained from the simulation is shown in fig. 9 and fig. 10 respectively.

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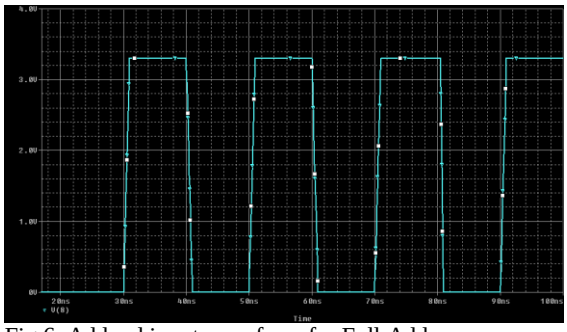

Fig 6: Addend input waveform for Full Adder

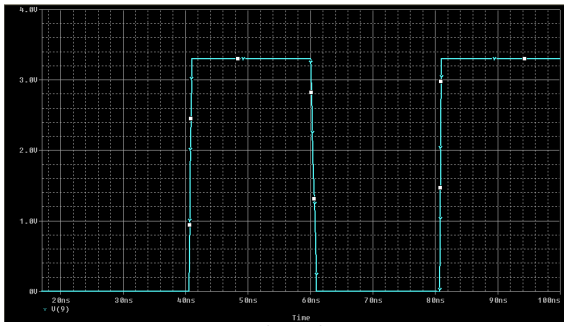

Fig. 7: Augend input waveform for Full Adder

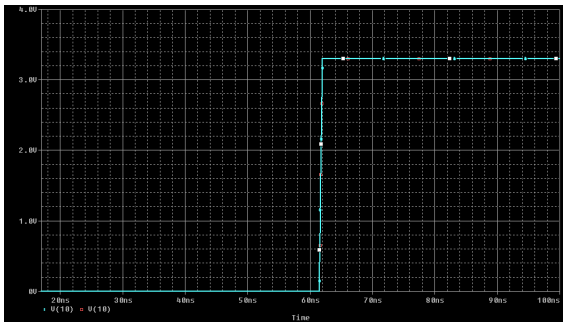

Fig. 8: Carry input waveform for Full Adder

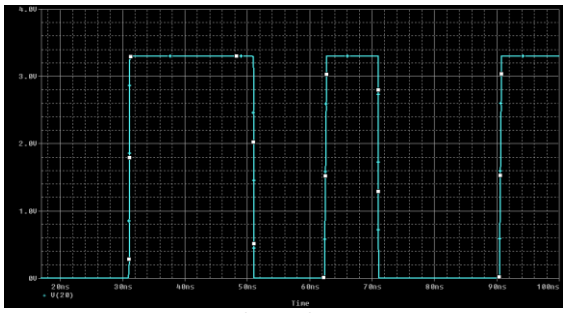

Fig. 9: Sum output waveform of Full Adder.

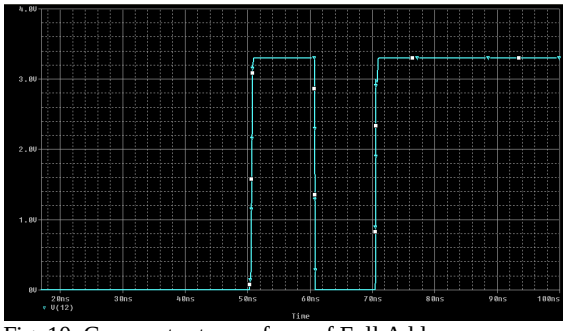

Fig. 10: Carry output waveform of Full Adder.

IV. DESIGN OF TWO BIT SYNCRONOUS COUNTER USING THRESHOLD LOGIC

Synchronous counters have a common clock pulse applied simultaneously to all flip-flops. A two bit binary synchronous counter requires two flip-flops.

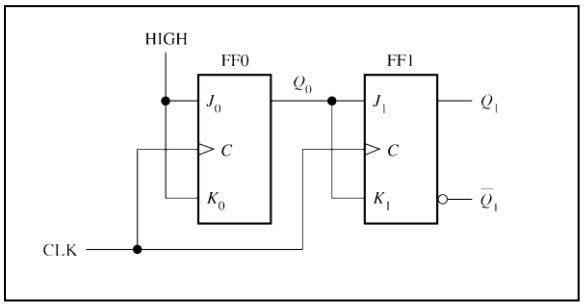

Fig. 11: Two bit binary synchronous counter

Clock	Q0	Q1
1	0	0
0	0	1
1	0	1
0	1	0
1	1	0
0	1	1
1	1	1
0	0	0

Table 2: Truth table of two bit synchronous counter

The threshold gate based equations which are used to make the two bit counter circuit are written below:

A=tlg1=sgn (T-Q-1);
B=tlg2=sgn (Q-T-1);
C=tlg3=sgn (A+B-1);
D=tlg4=sgn (L-C+1);
E=tlg5=sgn (2D-L-Q-1);
F=tlg6=sgn (E-L+1);
G=tlg7=sgn (2F-Q+L-2);
H=tlg8=sgn (Q-H-1);
I=tlg9=sgn (1-q4-H);
J=tlg10=sgn (2I-H-q4-2);

The threshold gate based negative edge triggered two bit synchronous counter is implemented as shown in fig. 12.

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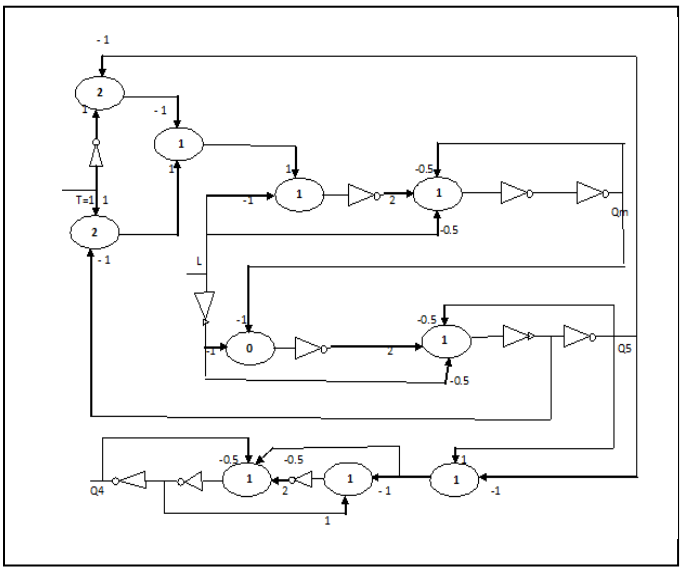

Fig. 12: Two bit synchronous counter using threshold logic

We have verified the proposed counter using the VHDL simulator. The simulation results thus obtained are shown below in figure 13.

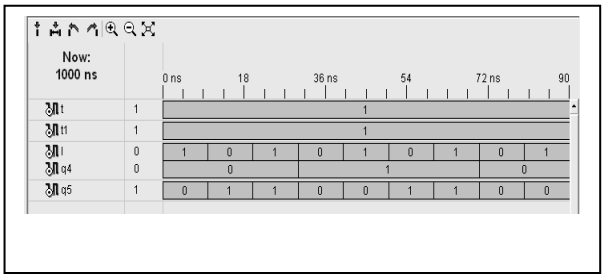

Fig. 13. Two bit synchronous counter output waveform

V. DESIGN OF FOUR BIT RING COUNTER AND JOHNSON COUNTER USING THRESHOLD LOGIC

A ring counter is a counter composed of circular shift register. The output of the last shift register is fed to the input of the first register.

There are two types of ring counters:

A straight ring counter, connects the output of the last shift register to the first shift register input and circulates a single one (or zero) bit around the ring. For example, in a 4 bit ring counter, with initial register values of 1000, the sequences are: 1000, 0100, 0010, 0001, 1000... . One of the registers must be pre-loaded with a 1 in order to operate properly.

A twisted ring counter, also called Johnson counter, connects the complement of the output of the last Flip-Flop to the input of the first Flip-Flop and circulates a stream of ones followed by zeros around the ring. For example, in a 4 bit Johnson counter, with initial register values of 0000,the sequences are: 0000, 1000, 1100, 1110, 1111, 0111, 0011, 0001, 0000... .A counter can be implemented using flip-flops and combinational logic. In this manner, ring counter can be implemented using D-flip-flops and decoder. A four bit ring counter can be implemented using a two bit synchronous counter and a two to four decoder. Similarly a Johnson counter can be implemented using flip-flop and decoder.

Now the ring counter is implemented using a two to four bit decoder. Similarly the Johnson counter is implemented in the same circuit. Both the counter can work together and responds to the same negative edge of the clock pulse. The output of both Ring counter and Johnson counter can be used for any purpose. A,B,C,D are the ring counter outputs and Aj,Bj,Cj,Dj are the Johnson counter outputs. As it is a negative edge triggered, so the output changes when clock goes from logic '1' to logic '0'.

Now the negative edge triggered four bit Ring and Johnson counter truth table have shown in table 3.

	Ring Counter				Johnson Counter			
Clock	A	B	C	D	Aj	Bj	Cj	Dj
1	1	0	0	0	0	0	0	0
0	0	1	0	0	1	0	0	0
1	0	1	0	0	1	0	0	0
0	0	0	1	0	1	1	0	0
1	0	0	1	0	1	1	0	0
0	0	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1	0
0	1	0	0	0	1	1	1	1
1	1	0	0	0	1	1	1	1
0	0	1	0	0	1	1	1	0
1	0	1	0	0	1	1	1	0
0	0	0	1	0	1	1	0	0

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1	0	0	1	0	1	1	0	0
0	0	0	0	1	1	0	0	0
1	0	0	0	1	1	0	0	0
0	1	0	0	0	0	0	0	0

Table 3: Negative edge Triggered Ring and Johnson counter truth table

The threshold gate based equations which are used to make the ring and Johnson counter circuit are written below:
Ring counter equations:
Ar=tlg1=sgn (L-Q1+1);
Br=tlg2=sgn (2Ar-L-Qm-1);
Cr=tlg3=sgn (Br-L+1);
Dr=tlg4=sgn (2Cr-Q1+L-2);
Er=tlg5=sgn (Q1-Dr-1);
Fr=tlg6=sgn (1+Q0-Er);
Gr=tlg7=sgn (2Fr-Er-Q0-2);
A=tlg8=sgn (Dr+Gr-1);
B=tlg9=sgn (Dr-Gr+1);
C=tlg10=sgn (1-Dr+Gr);
D=tlg11=sgn (1-Dr-Gr);

Johnson counter equations:
Aj=tlg12=sgn (1-Dj-L);
Bj=tlg13=sgn (Aj-L);
Cj=tlg14=sgn (Bj-L);
Dj=tlg15=sgn (Cj-L);

The initial value taken for the ring counter is '1000' and the initial value taken for the Johnson counter is '0000'.The threshold gate based negative edge triggered four bit Ring and Johnson counter is implemented as shown in fig. 14

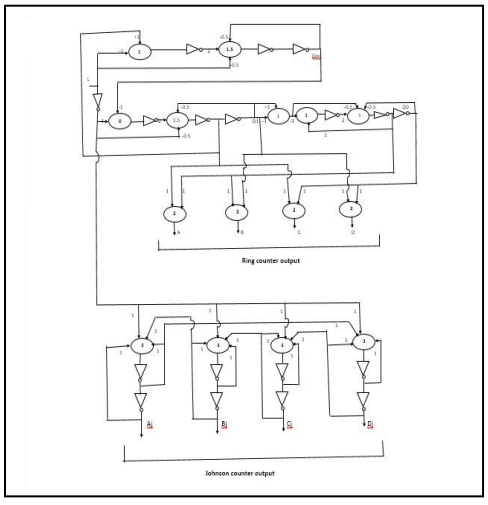

Fig.14 Threshold gate based ring and Johnson counter
We have verified the four bit ring and Johnson counter implementation by using the VHDL simulator. The simulation results obtained is shown in fig. 15.

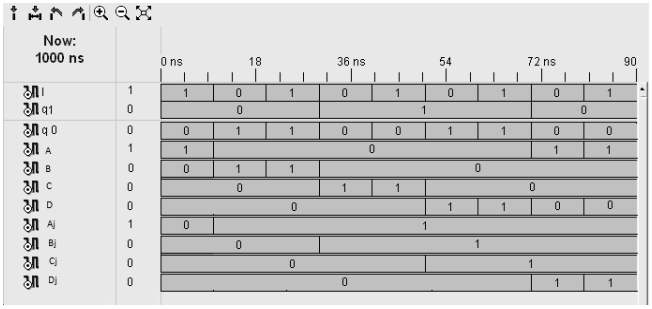

Fig. 15: Four bit Ring and Johnson counter output waveform

In fig. 15, q1 and q0 are the synchronous counter outputs. A,B,C,D are the Ring counter outputs with initial value '1000' and Aj,Bj,Cj,Dj are the Johnson counter outputs with initial value '0000'.

VI. CONCLUSION

In this work, we proposed the threshold gate based implementations of Full Adder, Ring and Johnson counter. The capacitors used in the Full Adder take up very little area so very high integration density is achieved and also due to very high impedance gate inputs, benefit the speed of the circuit. Both the output of Adder, Ring and Johnson counter have required only a single clock pulse to change from one state to another. As the four bit synchronous counter requires four stages or four numbers of flip-flops, the threshold gate based synchronous counter requires two stages only. Similarly the ring and Johnson counter require eight stages altogether to get the four bit output. But use of threshold gates it decreases to two only. So, the delay reduces dramatically in the whole circuit. As the output of both Adder and counters responds to a single negative edge of the clock pulse, the response time of the output to a single input decreases.

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