Optimal Design of Row/Column Decoder Segment of ROM Design in QCA

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***Abstract*—In the current era of a high speed technology, Quantum Dot Cellular Automata (QCA) became a very promising technology in the design of various types of memories. In this modern age, technology goes towards highly dense memory cells where costing trades-off the memory capacity. In this newer field of science, optimization of effective area upon which the design is to be implemented, plays a key role. In the design of Read Only Memory (ROM), the decoding segment helps in deciding which memory block will be chosen for operation. Optimal design of decoder segment signifies the improved memory design. This paper introduces a new design of 4 bit row/column decoder in the Read Only Memory (ROM) design. This decoder shows 74.1% reduction of effective area than the latest design proposed by Rigui Zhou et al. at the cost of only four majority voter blocks.**

Keywords-Majority Voter, Cell Bed Area, Read Only Memory (ROM), Row/Coloumn Decoder

I. INTRODUCTION

QCA dictates engineering towards a new trend which can be considered as "all advantage" technology. The problems of leakage current in Metal Oxide Semiconductor Field Effect Transistor (MOSFET) have been avoided in this new arena of science particularly when the dimensions are shrunk to the level of few nanometers [1]. QCA was first described in 1993 [2] which has several advantages. Proper working of QCA stands upon the negative-edge of the clock owing to no internal power dissipation within the circuit. Secondly the problem of leakage current in MOS technology is completely avoided in QCA technology [3]. The information flows without any voltage supply in the QCA based circuits and this gives QCA an important use in the nanotechnology. The binary information which flows through the quantum cell encoded as a localized charge in the cell.

As the dimensional scaling of CMOS is approaching the fundamental limit, several new alternatives are being explored like SET (Single Electron Tunneling), Spintronics, Ferromagnetic, Molecular and Quantum devices [ITRS report]. The Heat dissipation & Power consumption are next to negligible in the Quantum Cellular Automata which avoids the requirements of heat sink in the electronic circuitry. Also the high density and fast speed is an added advantage. The fundamental nanostructure of Quantum Dot Cellular Automata (QCA) is a cell.

II. BASICS OF QCA

A QCA cell comprises of four interacting quantum dots which are placed in the four corners of a square cell. Each of these dots is coupled together by the means of tunnel junction. The logical cell can contain two free electrons. When two excess electrons are charged, then due to the Coulumbic force of repulsion the two excess electrons occupy diagonal position in a Quantum Cell [2]. The Quantum Cell consists of four quantum dots as shown in Figure 1.

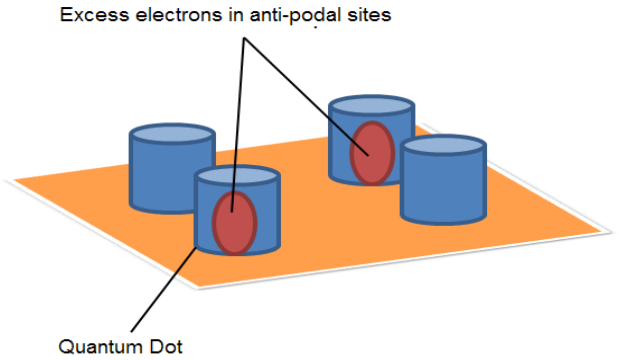

Figure 1. Four quantum dot in a QCA cell

The electrons always take the antipodal sites to be stable. Hence the alignments of the electrons are of two types and

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each of the alignment can be regarded as a polarization. Binary information is encoded by the configuration of this electrical charge. Depending upon the two types of polarization the cell would have steady state polarization of P=+1 and -1. The notion of clocked QCA cell is essential for functional gain and complex operation [3][4] [5]. The clock influences the charge stored in a cell to propagate among the cells. This charge transfers takes place by means of Coulombic Force of attraction and repulsion. Multiplexed clocking mechanism is used in QCA logic. The clocking is provided to the circuit by proper controlling of the potential barriers between the adjacent dots in the quantum cell. With the increase of the potential barrier tunneling potential decreases and electrons in the dots start to localize themselves. When the tunneling potential is high electrons delocalize themselves and cause an indefinite potential. Switch, hold release and relax are the four phases of a clock signal. The polarization of a QCA cell is determined in the switching phase depending upon the polarization of the input of that cell in the present status. The release and relax phase of the input cell does not affect the polarization of the QCA cell. The clock in Quantum Cellular Automata has four phases : (a) Switch, (b) Hold, (c) Release and (d) Relax.

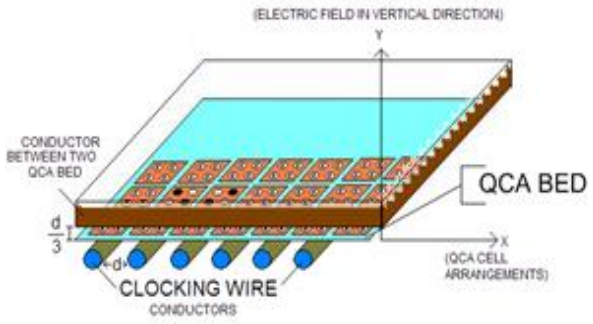

Figure 2. Separation of QCA BED and vertical conductor,x-directiona and y-directional electric field

This clock forces the charge to propagate from the source cell to destination cell. The QCA Cells are instantiated on a bed which can be termed as QCA BED. This QCA BED lies on a surface consisting of several number of clocking wires as shown in Figure 2 [7]. The BED can be of horizontal type or can be of vertical type where each of the QCA BED is separated by a spacing of x (~2-10nm) is showing two components of electric field. One is horizontal component and another is vertical component. X-axis component of electric field is due to the columbic interaction between two neighboring cells. The current carrying conductor is attached with the upper QCA BED interaction with the clocking wire, electric field is directed towards Y-axis. The clocking wires are implemented parallel to the Z-axis. The several states whether +1 or -1 polarization is strictly due to the X-component of the electric field. Y-directional field can have NO preamble to create fixed cell polarization. If clocking wires are separated with each other by a distance of "d", then vertical distance between QCA BED and upper QCA conductor is d divided by 3.The QCA cells can be arranged in different orders to implement logic structures and interconnections. The commonly used QCA logic devices [2] are:

(a) Majority Voter: The five cell logic device whose output takes the decision in favor of majority voter. The majority voter is the median cell. It will show the polarization according to the majority of the logic levels of the three inputs. Depending upon the control input, it acts as either an AND Gate or an OR Gate.

(b) Binary Wire: A linear chain or array of cells functions as a wire, transmitting a 0 or 1 (P = + 1 or P = - 1) from one extremity of the wire to the other. The polarization of one extremity is fixed and the polarization of the other extremity is unconstrained. The self-consistent ground state of the chain is calculated using the Intercellular Hartree Approximation (ICHA) method. It consists of a collection of QCA Cells which provides a "wire-like" connection in QCA Circuits.

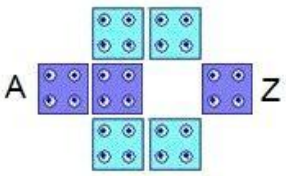

Figure 3. QCA inverter

(c) Inverter: Although several types of inverters are available in QCA but the most popular and noise immune inverter consists of seven cells showing in figure 3. In general by offsetting an array of cells from another, an inverter like structure is constructed.

III. PROPOSED DESIGN OF 2x4 DECODER

The 2 to 4 Decoder claims its importance in the design of memory architecture especially in Read-Only-Memory (ROM) Design. As Quantum Cellular Automata is a promising emerging field of nanotechnology for its extreme high speed and low power dissipation, ROM can also be instantiated in QCA. Memory design comprises of data read-write and data storage techniques. Improved design in Memory designing invokes the optimization of above techniques as it lowers the effective cell-bed area. In this paper, ROM design and it's architecture involves 4-bit data processing. The designing of 4-bit ROM includes of design of channel decoder and data storage units which is shown in Figure 4.

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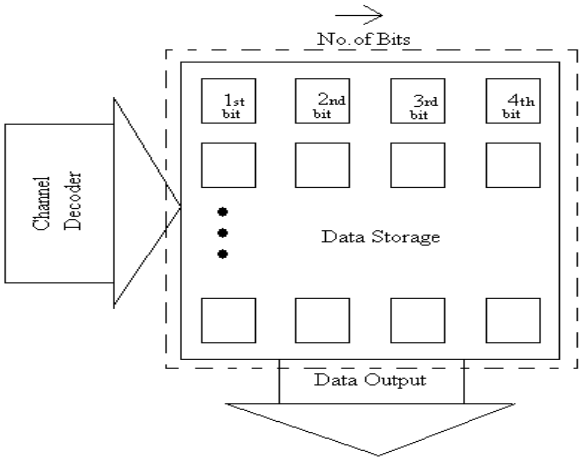

Figure 4. Block Diagram of 4-bit ROM

In this work, we have analyzed and optimized the design of channel decoder which is tested and verified in QCA Designer [6]. The design proposed in [9] to design 2 to 4 decoder, starts from the traditional design. The traditional block diagram for 2 to 4 decoder is shown in Figure 5 whereas the design proposed by Ringui Zhou et al. is shown in Figure 6.

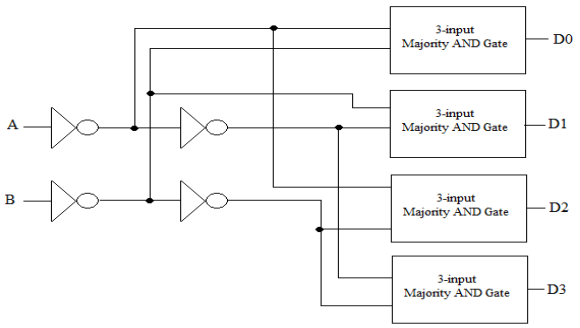

Figure 5. Traditional Block diagram of 2 to4 decoder

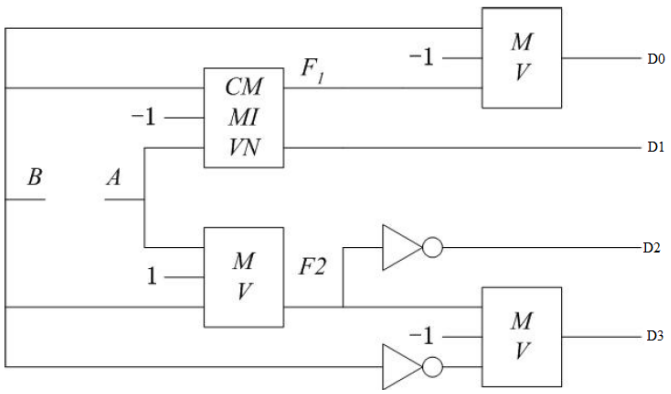

Figure 6. Block diagram of 2 to4 decoder proposed by R.Zhou et al

We propose the 2 to 4 Decoder circuit in Figure 7 and its simulation graph is shown in Figure 8. Proposed circuit improves the designing of memory architecture in terms of cell requirements hence the area as each of the QCA cell requires 324nm^2. Proposed circuit needs two layers and latency equals to 0.75 clock delay. Table 1 compares the statistics for various parameters like gate requirements and cell count.

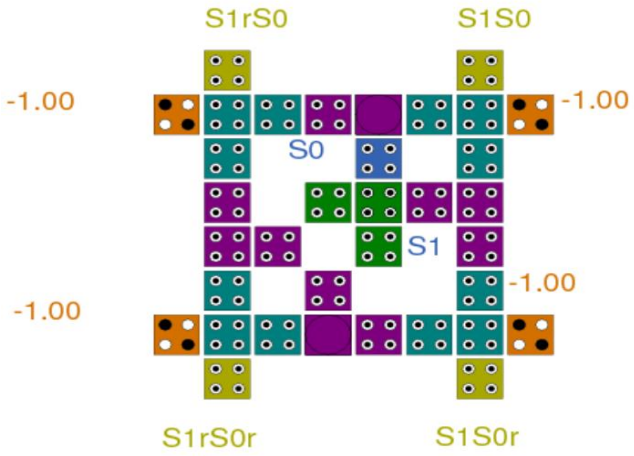

Figure 7. Block diagram of proposed 2x4 decoder

Figure 8. Output Graph of proposed 2 to 4 decoder

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TABLE I. COMPARATIVE ANALYSIS IN TERMS OF CELL COUNT & NO. OF GATE REQUIRED

Design proposed by	Cell Count	No. of Gates required
Traditional Design	168	8
Rigui ZHOU et al.[9]	139	6
A Vettah et al.[10]	154	4
M. Malekpour et al.[11]	302	4
Proposed Design	36	4

IV. CONCLUSION

Proposed decoder design needs (36x18x18) nm^2=11664 nm^2 which has hitherto been the optimal design in terms of effective area. Proposed deign of 2x4 decoder views bi-layer design and minimal latency which fetches only four numbers of gates to get the output. Processor architecture methodology always requires less complexity in design which this design already has. Figure 9 depicts 74.1% improvement can be achieved in this design when compared to the design proposed by [9] which tremendously improves the design-arena for the row/column decoder segment for ROM architecture.

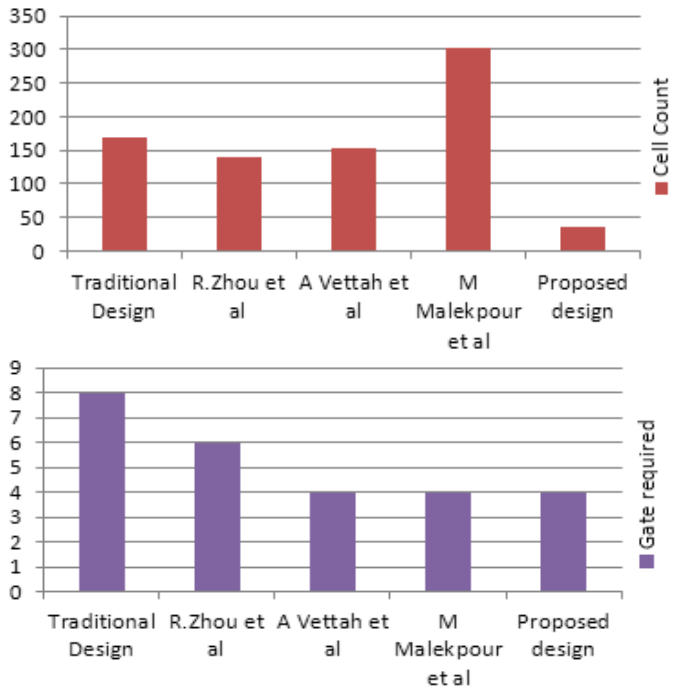

Figure 9. Output Graph of proposed 2 to 4 decoder

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