A simple circuit based approach for GMSK modulation & demodulation

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*Abstract*ð The GMSK Modulation technique is used in GSM. Generally the modulation is performed by GMSK pre-modulation filter or by DSP. But the realization of the filter is difficult. So an alternative way is considered, where the data is at first Manchester coded and this coded form is then passed through band-pass filter to approximate them as Gaussian pulses. These Gaussian pulses are then demodulated by passing them through comparator, then a synchronized PLL circuitry to obtain the data again. The data can be any arbitrary data, so a random sequence of 1 and 0 i.e. the PN sequence is considered as data. The entire circuitry has few limitations but it is a novel approach towards GMSK modulation, and this technique is much cheaper also.

Keywords- GMSK, Manchester code, Gaussian pulses, PLL.

I. INTRODUCTION

GMSK modulation is based on MSK, which is itself a form of phase shift keying. MSK and also GMSK modulation are what is known as a continuous phase scheme. Here there are no phase discontinuities because the frequency changes occur at the carrier zero crossing points. This arises as a result of the unique factor of MSK that the frequency difference between the logical one and logical zero states is always equal to half the data rate. This can be expressed in terms of the modulation index, and it is always equal to 0.5 [1]. The fundamental problem with MSK is that the spectrum is not compact enough to realize data rates approaching the RF channel BW. For wireless data transmission systems which require more efficient use of the RF channel BW, it is necessary to reduce the energy of the MSK upper side-lobes. The advantage of using GMSK modulation for a radio communication system is obviously the improved spectral efficiency when compared to other phase shift keyed modes. Generally the modulation is performed by GMSK pre-modulation filter. The pre-modulation low-pass filter must have a narrow BW with a sharp cutoff frequency and very little overshoot in its impulse response. In MSK we replace the rectangular pulse with a sinusoidal pulse. A Gaussian-shaped impulse response filter generates a signal with low side lobes and narrower main lobe than the rectangular pulse. Since the filterôs impulse response is characterized by a classical Gaussian distribution (bell shaped curve), this modulation is called Gaussian Minimum Shift Keying (GMSK). The relationship between the pre-modulation filter bandwidth, B and the bit period, T defines the bandwidth of the system. GSM designers used a BT = 0.3 with a channel data rate of 270.8 kbps. This compromises between a bit error rate and an out-of-band interference since the narrow filter increases the inter-symbol interference and reduces the signal power. Spectral compactness is the primary trade-off in going from MSK to Gaussian pre-modulation filtered MSK. The channel spacing can be tighter for GMSK when compared to MSK for the same adjacent channel interference.[2],[3],[4].

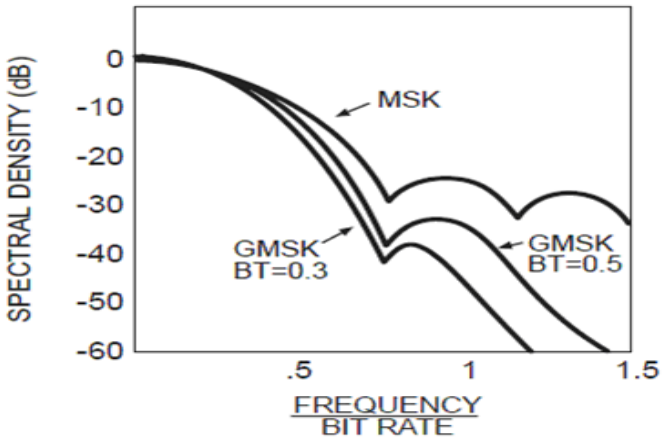

Figure 1: Spectral density of MSK & GMSK [1]

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II. IDEA BEHIND IMPLEMENTATION

In the design, our approach was to avoid the use of DSP (Digital Signal Processing). So instead of using a Filter having the Gaussian impulse function for which DSP technique needs to be used, a simple circuit is used, which approximately generates GMSK modulated data . Here we have made the approximation of Gaussian pulse with Sine pulse. Each of the square pulse train is replaced by a half sine wave. Since we have encoded the original data with Manchester code, we have square pulses of two types of durations: half the clock time period and the clock time period. Since each of the square pulse train is represented with a half sine wave, basically we are allowed to have a waveform with two sine frequencies: the clock frequency and half the clock frequency. So, to have desired waveform, we have passed the Manchester encoded data through a band-pass filter having lower and upper cutoff frequency as half clock frequency and clock frequency respectively. Also since the square wave contains only odd-integer harmonic frequencies (of the form $2´*(2k-1)*f$), by choosing the mentioned cutoff frequencies ideally we should have sine waves of the two aforesaid frequencies i.e. the desired signal.

In the demodulator, by passing the GMSK modulated signal through a comparator with zero reference voltage, we easily get back the Manchester encoded data. It is clear that if Manchester encoded data is sampled at appropriate instant and then the sample is hold for duration of a clock period, we will get the original data. To implement this we need to have the clock synchronized with the data. Since the Manchester code is self clocking i.e. the clock signal can be recovered from it. By using a differentiator circuit it is possible to have pulses at the instances where there is transition from positive to negative or vice versa. And by giving those pulses to i/p of a Phase-Lock-Loop (PLL), a clock of twice frequency synchronized to the data is obtained. Now with the help of the frequency divided by 2 circuit clock frequency signal is obtained. Also a delay of one forth of bit period is introduced to the clock signal with the help of a NOT gate and D flip-flop. This is done to sample the Manchester coded data not at the starting of the data bit, where the waveform has a transition from low to high or high to low and the sample and hold circuit may not get the desired value. So, introducing this delay makes sure that the correct value is sampled. We pass the obtained Manchester coded signal through a positive edge triggered flip-flop, with the delayed clock. Since the flip-flop only responds to the changes in its input as appeared when clock is going from low to high, automatically, the flip-flop holds the sampled valued for a clock period. And hence we obtain the demodulated data.

III. BLOCK LEVEL IMPLEMENTATION

The GMSK Modulation can have a circuit based approach. The block diagram shown can give an insight into the idea.

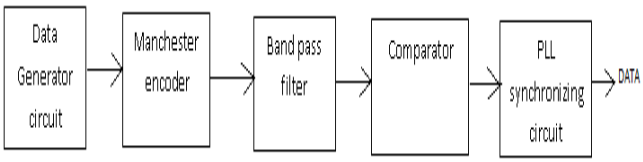

Figure 2: Block level implementation

A. Data Generatotor

The generation of data is the first step for the entire circuit. It consists of two parts- clock generator & data generator. The data is a PN sequence which is generated by a PN sequence generator for digital transmission. The clock is required for controlling the remaining circuit components..

The clock generation circuit has an astable multi-vibrator followed by a D flip-flop. The astable multi-vibrator generates rectangular pulses which are fed to the clock input of a standard D-flip-flop, with the data-input driven by the negated output of the flip-flop. Hence, the flip-flop changes its state ('toggles') on each rising-edge of the flip-flop clock input. The resulting o/p from the D f/f is a square wave (duty cycle=50%) with frequency óFô, where the frequency of rectangular pulse o/p of the multi-vibrator is ó$2*F$ô.

In astable mode, the 555 timer puts out a continuous stream of rectangular pulses having a specified frequency. Resistor R_1 is connected between V_{CC} and the discharge pin (pin 7) and another resistor (R_2) is connected between the discharge pin (pin 7), and the trigger (pin 2) and threshold (pin 6) pins that share a common node. Hence the capacitor is charged through R_1 and R_2, and discharged only through R_2, since pin 7 has low impedance to ground during output low intervals of the cycle, therefore discharging the capacitor.

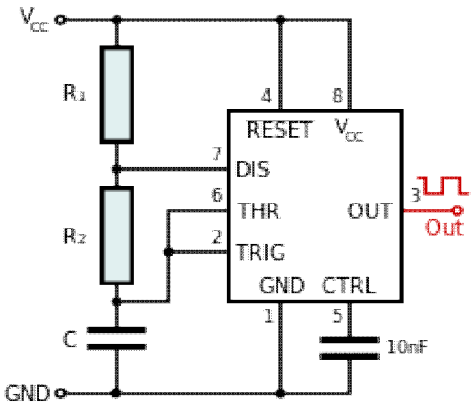

Figure 3: Astable multi-vibrator [7]

The rectangular pulse o/p is fed to a frequency divide by 2 circuit consisting of D f/f to get square wave pulses. Here, the Qô output is connected back to D input, producing square wave pulses at Q output.

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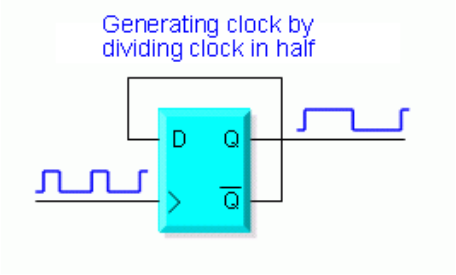

Figure 4: Frequency Divider Circuit [6]

The divide by two circuit employs one D f/f. Simply by giving the rectangular pulse train (from astable multi-vibrator o/p) into the clock i/p, and connecting the Q bar output to the D input, the o/p taken from Q is obtained as a square pulse train having frequency half the clock frequency.

The circuit operates in a simple way. The incoming pulse train acts as a clock for the device, and the data that is on the D input is then clocked through to the output. To see exactly how the circuit works it is worth examining what happens at each stage of the waveforms shown below. Take the situation when the Q output is a level '1'. This means that the Q bar output will be at '0'. This data is clocked through to the output Q on the next positive going edge from the incoming pulse train on the clock input. At this point the output changes from a '1' to a '0'. At the next positive going clock pulse, the data on the Q bar output is again clocked through. As it is now a '1' (opposite to the Q output), this is transferred to the output, & the output again changes state. It can be seen that the output of the circuit only changes state on the positive going edges of the incoming pulse clock stream. Each positive edge occurs once every cycle, but as the output of the D type requires two changes to complete a cycle, it means that the output from the D-type circuit changes at half the rate of the incoming pulse train. In other words frequency has been divided by two. The output Q of the f/f should a perfect square wave with 50% duty cycle and can be used as the clock i/p for the Data generation circuit i.e. the P-N sequence generation circuit.

B. Manchestor Encoder

Since the data sequence is random in nature, so it may contain a continuous sequence of 1 or 0. This problem can be overcome by converting the data sequence into Manchester encoded output where the continuous chain of 1 or 0 can be split into sets of alternate 1 or 0.

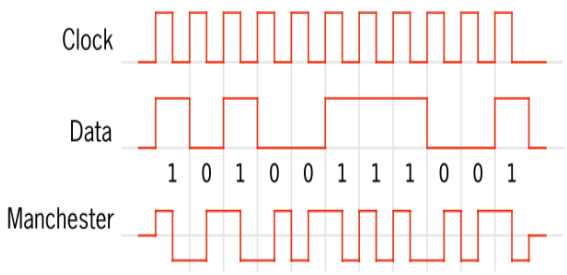

Figure 5: An example of Clock, Data & its Manchester encoded form [7]

C. BandPass Filter

To achieve the Gaussian sine wave for each individual square pulse, the Manchester coded data is sent through a band pass filter with two cut off frequencies. The circuitry is prepared by 1st order active High pass filter in series with 1st order active Low pass filter. The bandwidth of the filter is simply the difference between the upper and lower cutoff frequencies providing a shape similar to the corresponding sine pulse of the square pulse of the data.

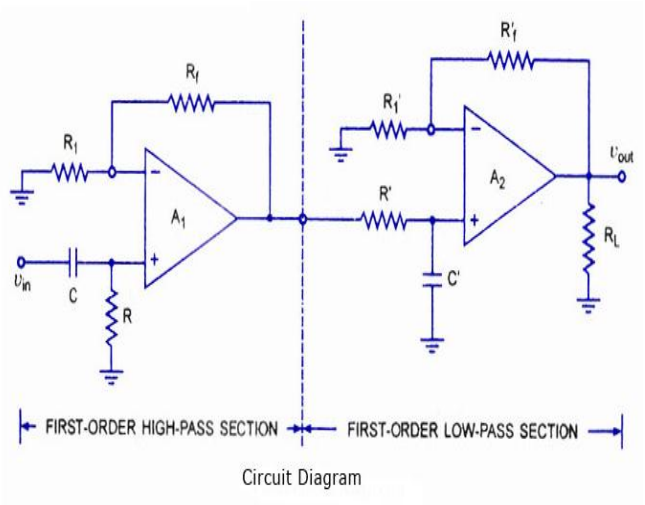

Figure 6: Band-Pass Filter [6]

D. Comparator

This is the demodulation part, where the modulated sine waves are converted back to their square counterparts resulting in the original Manchester encoded data with certain time lag.

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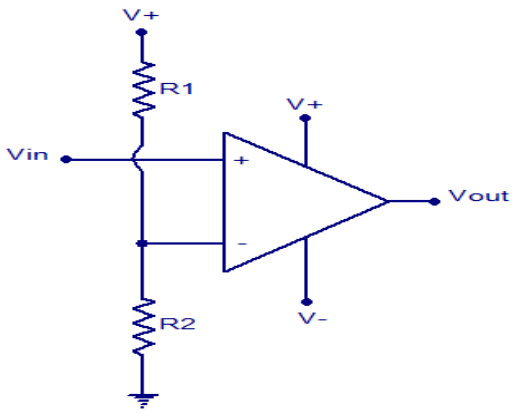

Figure 7: Comparator [6]

E. PLL synchronizing circuit

The PLL synchronizing circuit converts the Manchester data into PN data again. This can be done by extracting the clock from Manchester code, and driving the Manchester code with clock frequency after halving it.

IV LIMITATIONS

We have used band-pass filter for converting the Manchester coded data to GMSK modulated data. Ideally the band-pass filter should allow only the frequencies between the two cutoff frequencies to produce the desired waveform. But practically designing a filter with such sharp cutoff is not possible. The practical band-pass filter cannot suppress the frequencies beyond the pass band completely. As a result the response of the band-pass filter is not exactly the one, we desired. By using the band-pass filter we wanted to get a waveform where each square pulse is replaced with half sine wave. But practically, we donôt get proper half sine wave in the output.

V. OUTPUT WAVEFORMS

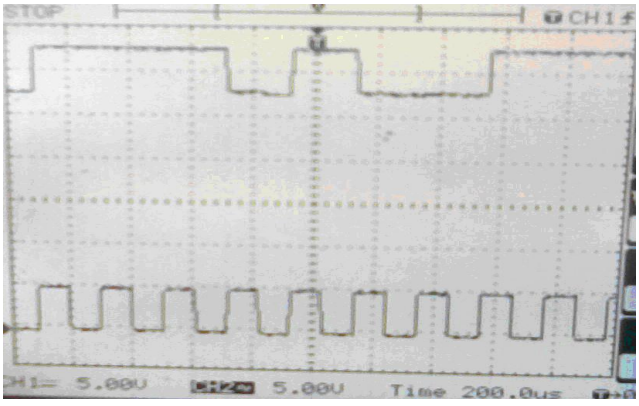

Figure 8: P-N sequence & Clock waveform as observed in DSO

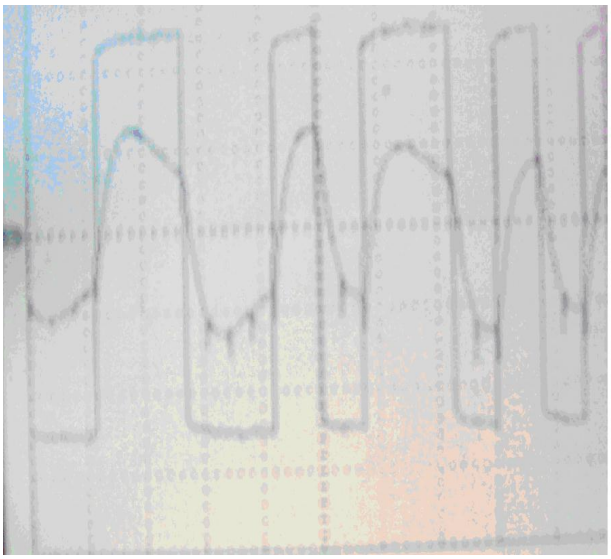

Figure 9: Band-Pass Filter Output & Comparator Output as observed in DSO

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