

Comparative study of electrical properties of vapor phase stain etch and metal assisted stain etch based porous silicon for device applications

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Abstract:-Porous Silicon (PS) is produced by two modified stain etch approaches that are Reaction Induced Vapor Phase Stain Etch (RIVPSE) technique and Metal Assisted Stain Etch (MASE) technique. Various preparation parameters were studied for preparing the PS layer. The PS layer is formed on P-type (100) semiconductor. After that PS dipped into $PdCl_2$ Solution for 5 second and then the contact made on the both surface, i.e. on bulk silicon as well as on PS layer. After that I-V and C-V characteristics are measured, The PL spectra has been observed for photoluminescence, and supported by the results UV ray excitation. AFM and optical microscope images are also observed for surface morphology.

Keywords: Porous Silicon, Electroluminescence, RIVPSE, MASE, LED, doping concentration.

I. INTRODUCTION

Silicon is the basic and most demanding material in present highly developed microelectronics technology. However, it has a drawback that prevents the further development of large-scale fabrication of fully-integrated optoelectronic circuits based on silicon. The drawback is because of the indirect energy band gap of silicon, which leads to very low quantum efficiencies for photoluminescence (PL) and Electroluminescence (EL) in silicon. Furthermore, Si has a small (~1.1 ev) band gap. Hence, the luminescence of bulk Si occurs near the infrared (NIR) part of the spectrum. That is not in the visible spectrum, which makes Si unsuitable for optical applications. Another thing is that GaAs which has a direct band gap and can emit light, but the problem is that it is expensive and unlike Si it is not compatible with the microelectronics technologies, which are based on silicon. In 1990 L.T. Canham [1] reported visible light emission from porous silicon (PS) samples. Since then the interest on PS has greatly

increased, and during the last few years many research has been done on PS. These have been aimed at both understanding the phenomenon from the basic science point of view, and also exploring possible Optoelectronics applications of this material.

PS layer has a very high surface area that is why PS layers are highly reactive and can be oxidized at low temperatures. And also PS has a higher resistivity than a comparable SiO_2 layer. Using these properties, "Silicon-On-Insulator" (SOI) and "Fully-Isolated-Porous-Oxidized-Silicon" (FIPOS) processes have used PSi for device isolation in Si integrated circuits [2]. Porous silicon layer conventionally formed by electrochemical anodisation etching technique using an external current source. But some drawback arises in this technique. Setup cost as the anodisation process need special equipment such as constant current source and anodisation cell. PS layers have been prepared by both RIVPSE and MASE techniques. RIVPSE process is a simple technique which does not require special technical equipment like anodization cell, external current source etc; therefore it significantly reduces the fabrication cost of PS films. RIVPSE technique exposes the substrate to a vapor to obtain uniform PS films.

Another Simple technique to obtain is MASE technique. In this process the crystalline Si is coated with a novel metal and then it is dipped into aqueous HF Solution for very short time. This process is a fast process to grow PS layers, also cost effective than the anodisation technique.

II. EXPERIMENTS

A. RIVPSE Technique

Boron doped P-type c-Si wafers (100) of resistivity 3-10 ohm-cm and thickness 300 micrometer has been taken as the starting material for the formation of Porous Silicon layer. Standard clean procedure is performed for cleaning of wafers. Firstly the c-Si wafer is cleaned by hot acetone treatment in ultrasonic agitation for 5 minutes followed by cleaning Methanol for 10 minutes. Then the Sample is immersed into the piranha etch solution containing concentrated H₂SO₄ and H₂O₂ in 3:1 volume ratio for 15 minutes to remove the organic contaminants present in the wafer. And then the standard RCA cleaning is done. Finally the sample is dipped into hydrofluoric acid (HF) of lower concentration to remove native oxide. PS layer is formed by an innovative RIVPSE method. The silicon substrates are exposed to an etch vapor resulting from the reaction of Industrial Zn dust added continuously to HF:HNO₃ solution (studied for various oxidant ratio and also for various etch time). The sacrificial Zn dust immediately dissolved to generate dense reddish brown vapors which reacted with the Si substrate situated at a specific height on the top of the beaker. An exposure time of 6 min to these acid vapors formed the PS layer.

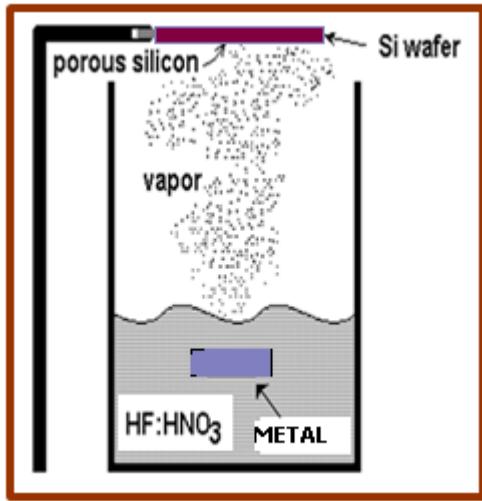


Figure 1. Schematic diagram of vapor phase stain etch apparatus

After that the PS film is modified by immediately dipped into PdCl₂ solution for 5 sec for stable contact [3]. And then annealed in air at 110°C. Here different etch parameters are studied (6:1, 4:1, and 8:1 oxidant ratio with different time variation e.g. 4min, 3min,

5min). In 6:1 oxidant ratio and 4 min etched PS layer has best light emission under UV ray excitation

B. MASE Technique

Boron doped P-type as-cut crystalline silicon wafers having <100> orientation and resistivity 3-10 ohm-cm (double side polished surface) thickness 300 micro meter were taken as starting material for the formation of porous silicon. Firstly, the samples were immersed into PdCl₂:HCl:H₂O₂ solution for 1 min. The molarity of PdCl₂ was taken 0.045M After that, these palladium deposited silicon samples were etched by two different etching solutions and the etchant solutions were HF:H₂O₂:H₂O in the ratio of 5:20:4 for the time period of 1 min.

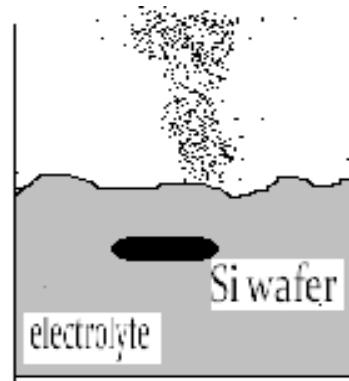


Figure 2. Schematic diagram of Metal Assisted Stain Etch Apparatus

C. Metallization

Both type of PS sample (i.e. RIVPSE and MASE produced) was dipped into PdCl₂ for 5 sec. After that contact has been made on the bulk silicon as well as Porous silicon. The contact is made by both Thermal Evaporation and screen printing. Then the sample is annealed in controlled environment at 500°C.



Figure 3. Structure of M-cSi-PS-M.

III. RESULT AND DISCUSSION

A. RESULT OF C-V MEASUREMENT

The C-V measurements were made using Agilent E4980A and the graph plotted in figure 4 as $1/C^2$ verses volt. During Capacitance measurements, the reverse voltage was varied from 0.5 to -5 volt and the frequency is maintained at 1 KHz.

TABLE-1 C-V Table for MASE based PS

BIAS (VOLTAGE)	C APACITANCE (pF)	
	MASE Based	RIVPSE Based
.5	2.07	3.45
0	1.99	3.18
-1	1.94	2.89
-2	1.89	2.62
-3	1.84	2.47
-4	1.79	2.23
-5	1.96	1.99

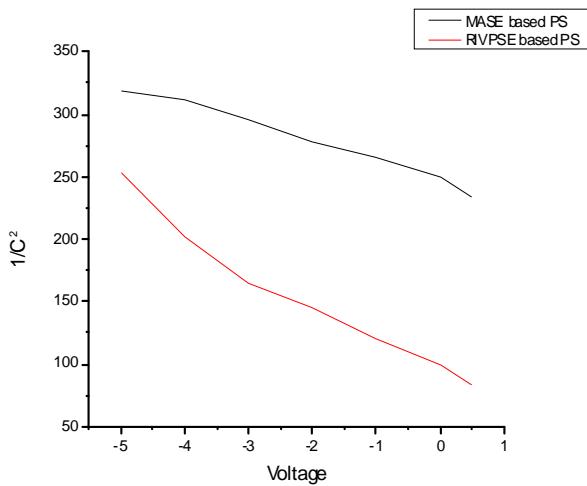


Figure 4. C-V characteristic of RIVPSE and MASE based PS.

B. RESULT OF I-V MEASUREMENT

The I-V measurements were taken using Keithley 2612A source meter. In fig 5 the I-V characteristic of metal/ps/c-si/ metal structure is shown, where PS layer formed based on RIVPSE procedure. Here we applied positive bias on the c-Si metal contact and the PS metal contact is grounded.

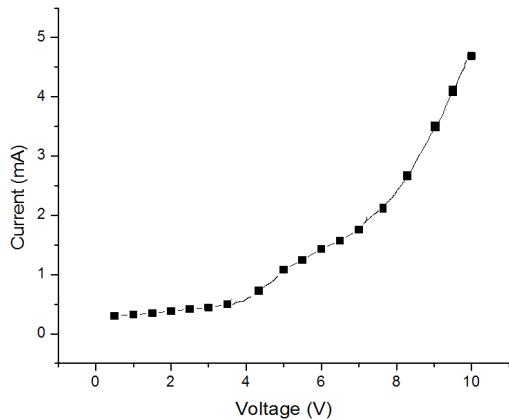


Figure 5. I-V characteristic of M-cSi-PS-M (RIVPSE based PS).

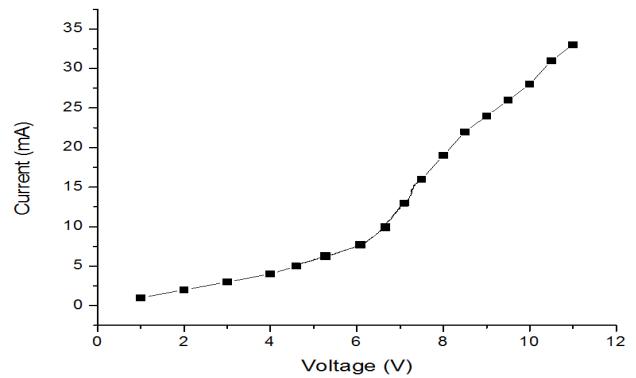


Figure 6. I-V characteristic of M-cSi-PS-M (MASE based PS).

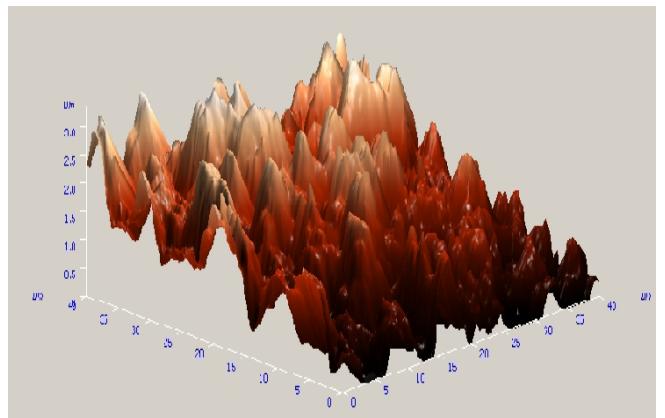


Figure 7. AFM Image of RIVPSE based Porous silicon with Pd modified.

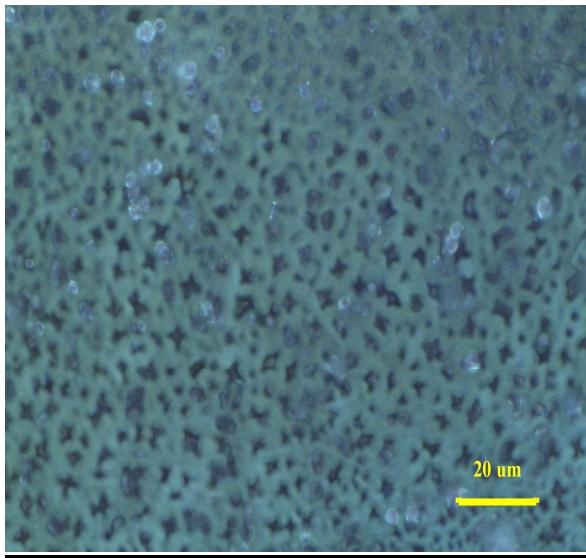


Figure 8. optical microscope image after etching using RIVPSE Technique

Fig 7 shows The morphology of the porous silicon surface after etching the c-Si using RIVPSE and then the PS film dipped into 0.01 (M) PdCl_2 Solution for 5 sec. And Fig 8 shows the optical microscope image of RIVPSE based unmodified PS surface.

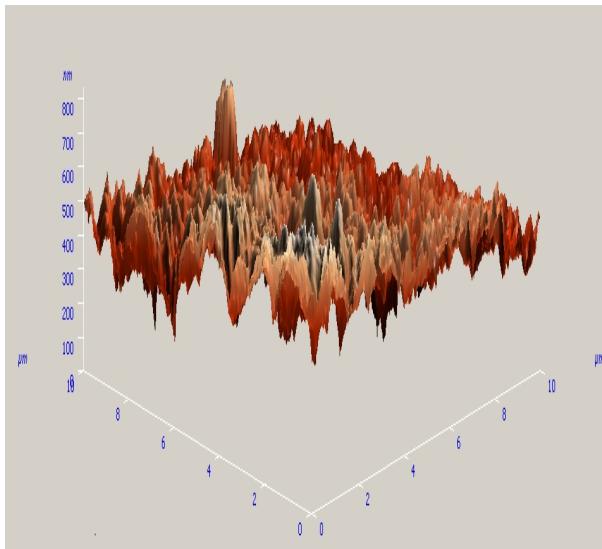


Figure 9. AFM Image of MASE based Porous silicon.

The AFM images are taken using NTEGRA Atomic Force Microscope.

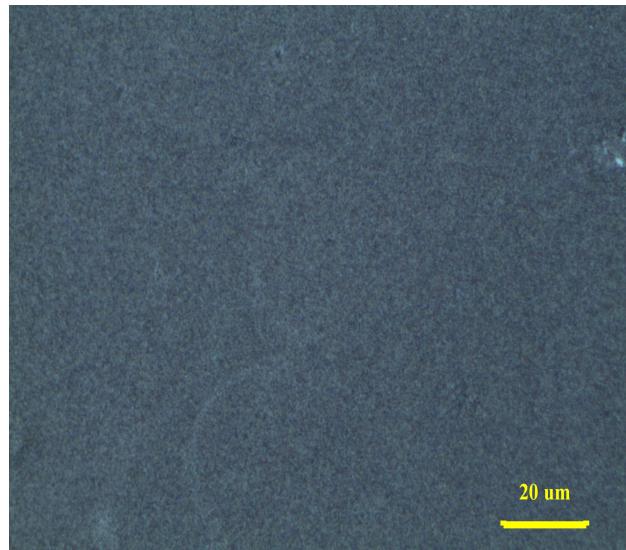


Figure 10. optical microscope image after etching 1 minute in $\text{HF:H}_2\text{O}_2:\text{H}_2\text{O}$ solution

Figure 9 shows The morphology of the porous silicon surface after etching the palladium coated silicon in solution $\text{HF:H}_2\text{O}_2:\text{H}_2\text{O}$ for 1 min, and Fig 10 shows optical microscope image after etching 1 min in $\text{HF:H}_2\text{O}_2:\text{H}_2\text{O}$ solution.

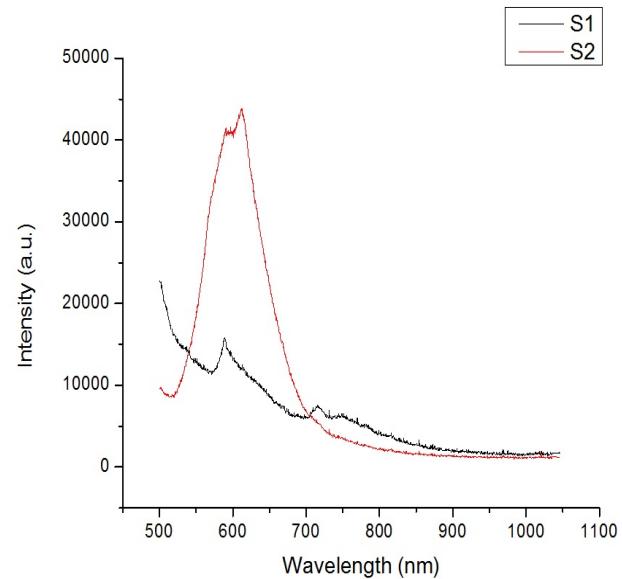


Figure 11. PL spectra for RIVPSE based PS film.

Fig 11 shows the PL spectra for RIVPSE based PS layer. Both the spectrum shown for the PS layer formed in 6:1 oxidant ratio and for etching time 4min, but here for S1 sample Zinc added into the oxidant continuously for 4min. and for sample S2 the

zinc added initially for one time only. The PL measurement has been carried out in room temperature by using HeAg laser of wavelength 224 nm as the excitation source for all the samples.

IV. CONCLUSION

From the Current Voltage characteristics of M-cSi-PS-M structure (for both the MASE and RIVPSE produced PS film), it is concluded that the structure is like Schottky Diode. The current through the structure is in mA range. It confirms that the Pd deposition over the PS layer helps to get a good contact. From the Capacitance-Voltage characteristics, the doping concentration of the material is calculated which is $7.8 \times 10^{13} \text{ cm}^{-3}$. The AFM image shows that for MASE based PS has an average roughness of 83.41nm, and for RIVPSE based PS the average roughness is 504.34nm. As the roughness is increased for the RIVPSE based PS, so the surface to volume ratio is also increased, so the RIVPSE based PS can be used for sensing applications. PL intensity is increased in very high value when Zn is added only for one time. Orange light emission is found in photoluminescence for the one time Zn added material and yellow light emission is found when Zn added continuously throughout the etch time. Hence RIVPSE based PS can be used for optoelectronic applications also.

V. ACKNOWLEDGEMENT

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VI. REFERENCES

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