Study of Surface Potential and Threshold Voltage for non-uniformly doped DHDMG n-Mosfet

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***Abstract*— The paper presents a model for subthreshold surface potential and threshold voltage for a Double halo Dual Material Gate (DHDMG) MOSFET. A pseudo-2D analysis applying Gauss' law along the surface is used to model the subthreshold surface potential. The same model is used to find the threshold voltage for Gaussian profile based DHDMG. The proposed model is derived based on two Gaussian pile-up profiles located at the source and drain ends of a MOSFET. The model is further applied to find the surface potential using high-k gate dielectric materials. The models are verified against 2D device simulator DESSIS. Simulation results show that the model predicts the value of the subthreshold surface potential and threshold voltage fairly accurately for the different device and pocket parameters along with various bias voltages.**

***Keywords*— Halo doping; Pseudo 2D analysis; threshold voltage; Gaussian profile**

I. INTRODUCTION

The dimensions of MOSFETs have reduced considerably in order to achieve higher speed and an improved performance. Nowadays, the power consumption of modem VLSI circuits has become very significant for large scale integration. Scaling down the power supply voltages is an effective method for reducing this potential.

Present day MOSFETs are either vertical non-uniformly doped or lateral non-uniformly doped. The most important factor to model the surface potential and threshold voltage accurately is to model its non-uniform doping profile.

In this paper a quasi-Fermi potential based analytical subthreshold surface potential and threshold voltage model for sub 40 nm DHDMG MOSFET has been derived taking into consideration Gaussian profile based pockets. For finding expression of the characteristic parameters, an average doping profile expression is used. Simulation results from DESSIS show that the model predicts the value of the subthreshold surface potential and the threshold voltage substantially accurately for different device and doping profile parameters along with various bias voltages. The results prove the validity of our model for analog circuits in 30 nm subthreshold regime.

II. MODEL DESCRIPTION

Gaussian doping profile replace other profiles for practical MOSFETs due to the need of many implantation and diffusion steps in the fabrication process. So modeling of characteristic parameters using a Gaussian doping profile as in [1] gives better characteristics for DHDMG MOSFETs.

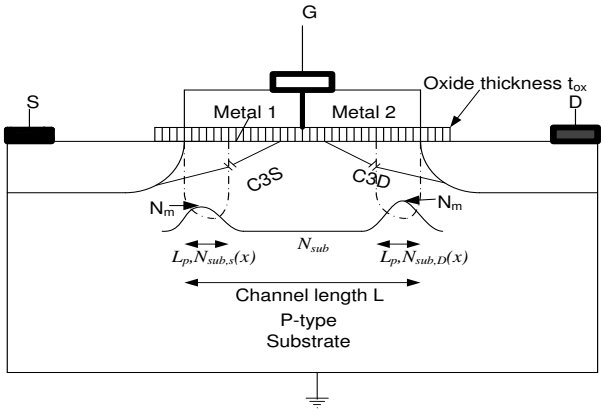

Fig. 1: Structure of n-channel Gaussian doped DHDMG MOSFET

Gaussian profiles at the source and drain ends are considered as in Fig.1. The doping concentration at the source end is

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$$N_{sub,S}(x) = N_m e^{-\{(x/L_p)\}^2} \quad (1)$$

The distance along the channel is considered as x. With the reduction of channel length, the lateral doping increases. This is due to the overlap of the pile-up profiles as channel length decreases as in [1] and [2]. N_m and L_p stands for the maximum concentration of the Gaussian profile and the horizontal length of the Gaussian regions.

The drain side doping concentration is

$$N_{sub,D}(x) = N_m e^{-\{(L-x)/L_p\}^2} \quad (2)$$

The average doping concentration is

$$N_{av,Gauss} = N_{sub} + \frac{L_p}{L} N_m [\int_0^{\frac{L}{L_p}} e^{-p^2} dp - \int_{\frac{L}{L_p}}^{0} e^{-p^2} dp]$$

$$N_{av,Gauss} = N_{sub} + N_m \{\frac{sqrt(\pi) erf(\frac{L}{L_p})}{\frac{L}{L_p}}\} \quad (3)$$

A small Gaussian box is considered at distance x along the channel of length Δx as in [3] and [4].The height of the box is so chosen that it covers the entire depletion depth. Here Y_d=the depletion depth and W=width of the rectangular box and $\Delta x Y_d W$=volume of the box.

Application of Gauss's law leads to

$$\varepsilon \oint \vec{E}.\vec{ds} = -qN_{av} Y_d \Delta x W$$

Here $\vec{E}$ = electric field striking the faces of the box perpendicularly. $\vec{ds}$ = area of the faces.

If ε_{Si} and ε_{ox} stand for permittivity of Silicon and silicon dioxide respectively, the surface potential is given as

$$\varepsilon_{si} \frac{d^2\psi_s}{dx^2} - \frac{C_{ox}}{Y_d}\psi_s = qN_{av,Gauss} - \frac{C_{ox}}{y_d} V_{GS} \quad (4)$$

Where $\frac{\varepsilon_{ox}}{t_{ox}} = C_{ox}$ = oxide capacitance per unit gate area.

The variation of the depletion layer depth is shown in Fig.2:

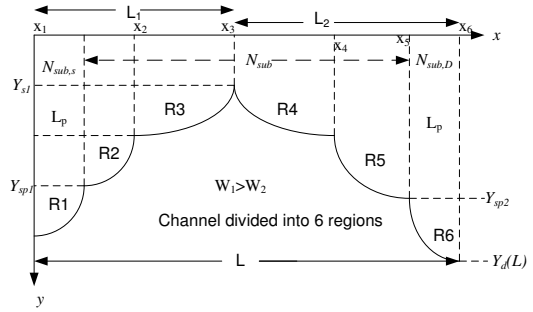

Fig.2:Variation of depletion layer depth.

(4) can be solved for perfect value of the surface potential as in [3],[4],[5].However $Y_d(x)$ need to be modelled for obtaining a perfect solution of the surface potential.

Considering $Y_d(x) = (ax+b)^2$ the source and the drain end values are given by

$$Y_d(0) = X_j + \sqrt{2\varepsilon_{si}(V_1)/(qN_{av,Gauss})} = X_j + X_{rs} \quad (5)$$

and

$$Y_d(0) = X_j + \sqrt{2\varepsilon_{si}(V_7)/(qN_{av,Gauss})} = X_j + X_{rd} \quad (6)$$

respectively where, $V_1 = V_{SB} + V_{bi} + V_{fs}$, $V_7 = V_{DB} + V_{bi} + V_{fd}$, V_{bi} =substrate built-in potential. V_{SB} and V_{DB} = source and drain bias respectively, $N_{av,Gauss}$ is the average concentration,

$$X_{rs} = \sqrt{2\varepsilon_{si}(V_1)/(qN_{av,Gauss})}$$

and $X_{rd} = \sqrt{2\varepsilon_{si}(V_7)/(qN_{av,Gauss})}$

are the depth of penetrations of the depletion layers at the source and the drain ends .

The channel is divided into six regions with known values V_1 and V_7. The unknown voltages are obtained by applying the continuity of the electric field $\frac{d\psi_s}{dx}$ at the junction of the different regions. The following simultaneous equations are obtained which are solved for obtaining the unknown voltages.

$$a_{11}V_2 + a_{12}V_3 + a_{13}V_4 + a_{14}V_5 + a_{15}V_6 = A_1 \quad (7)$$

$$a_{21}V_2 + a_{22}V_3 + a_{23}V_4 + a_{24}V_5 + a_{25}V_6 = A_2 \quad (8)$$

$$a_{31}V_2 + a_{32}V_3 + a_{33}V_4 + a_{34}V_5 + a_{35}V_6 = A_3 \quad (9)$$

$$a_{41}V_2 + a_{42}V_3 + a_{43}V_4 + a_{44}V_5 + a_{45}V_6 = A_4 \quad (10)$$

$$a_{51}V_2 + a_{52}V_3 + a_{53}V_4 + a_{54}V_5 + a_{55}V_6 = A_5 \quad (11)$$

Two fitting parameters $\zeta_s = V_1 / V_{bi}$ for the source end and $\zeta_d = V_7 / V_{bi}$ for the drain end are considered for obtaining a best fit surface potential model profile with ISE TCAD. The same model can give accurate expression of surface potential for SHDMG MOSFET[6].

The threshold voltage is the gate voltage V_{GS} at which the minimum subthreshold surface potential $\psi_{S,\min} = 2*\phi_F + V_{SB} + V_{fs}$ is obtained.

x_{min} corresponding to $\psi_{S,\min}$ is approximated at the junction between regions 2 and 3 or between regions 3 and 4. An iterative method is used to find the threshold voltage.

III. Results

Simulations of MOSFET structures are performed using the 2D-device simulator DESSIS of ISE TCAD [7]. The MOSFET structure shown in Fig. 1 consists of metal gate, n-type source and drain contacts and p-type poly-silicon body contact. Similarly unless mentioned otherwise default values of work functions for the two metals taken are W_1=4.2 eV and W_2=4.1 eV respectively. In the DHDMG MOSFET, the work

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function of Metal 1 is taken greater than that for Metal 2 and hence the threshold voltage corresponding to Metal 1(V_{t1}) is greater than that corresponding to Metal 2(V_{t2}). This has the advantage of improved gate transport efficiency.

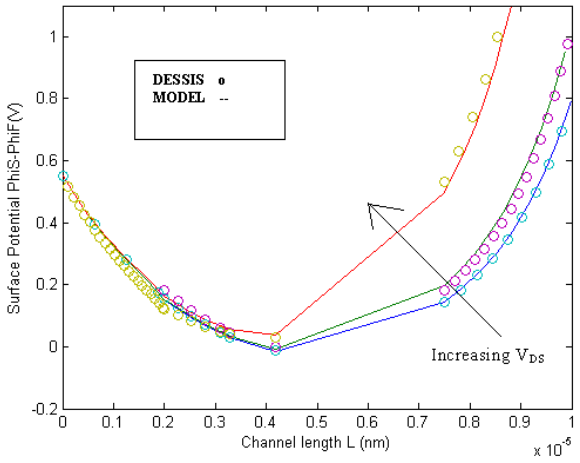

Fig. 3.The plot of surface potential versus channel length of DHDMG MOSFET for three different values of the V_{DS} =0.25,0.5 and 0.75V for L = 100nm and fixed doping of N_{sub}=6*10^{17} cm^{-3} , $N_{av,Gauss}$=6*10^{18} cm^{-3} against the applied voltages V_{GS}=0 V= V_{GB} =V_{SB}

The surface potentials in the channel calculated from our model are illustrated in Fig. 3 for DHDMG MOSFET with the channel length L=100nm at the various drain biases(V_{DS}=0.25,0.5 and 2V).

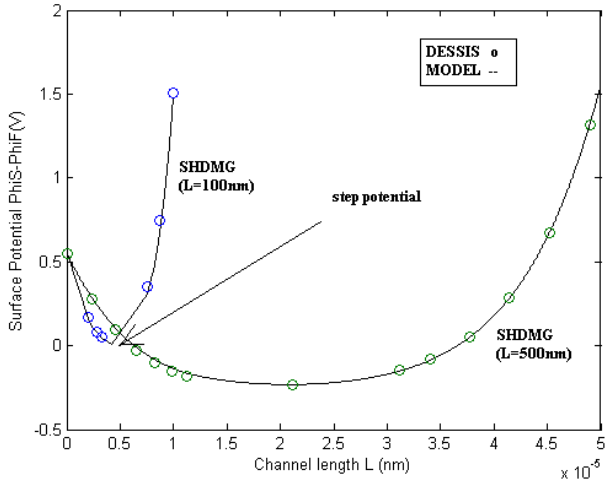

Fig. 4 Surface potential profile of a SHDMG MOSFET for channel length L=100nm and 500nm with potential step profile indicated.

There is no such step profile in the surface potential if the channel length is larger than 100nm as shown in Fig. 4.

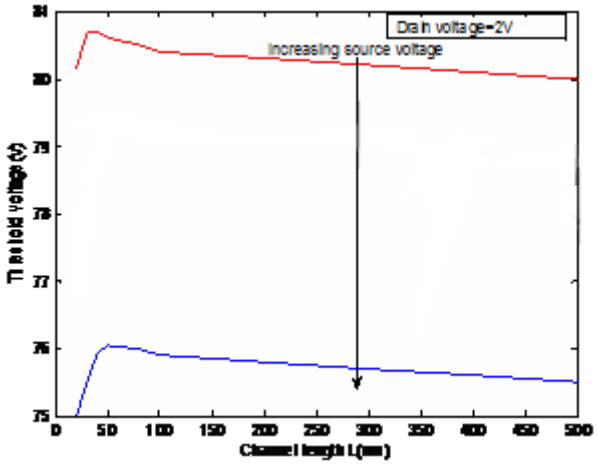

Fig.5: Plot of threshold voltage v/s channel length for Gaussian profile based DHDMG for V_{SB} =0.2 and 0.5 V, V_{DS} = .2 V taking N_{sub}=6*10^{17} cm^{-3} , $N_{av,Gauss}$=6*10^{18} cm^{-3} ,L=40 nm,L_p=8 nm, W_1=4.6 eV and W_2=4.1 eV.

It is found from Fig.5 that as the source bias increases the threshold voltage decreases. It is seen that the roll-off starts around 30 nm.

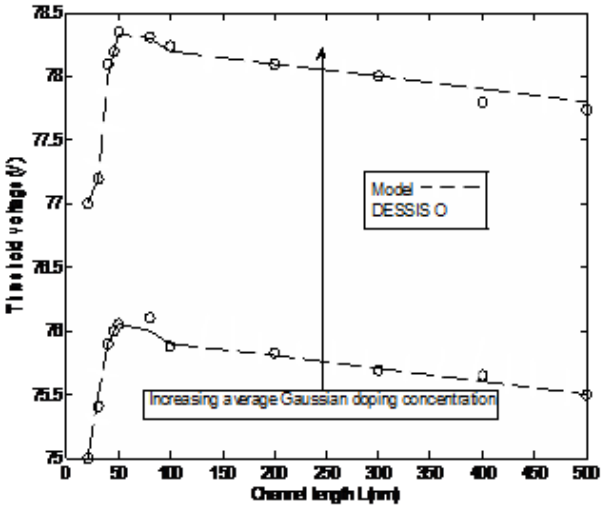

Fig.6: Plot showing threshold voltage roll-off v/s channel length for $N_{av,Gauss}$=2*10^{18} cm^{-3} and 8*10^{18} cm^{-3} taking all other parameters same as in Fig. 5.

It is seen from Fig.6 that as the maximum pocket concentration at the two ends increase the average Gaussian doping concentration increases and the peak of the threshold voltage curves increase.

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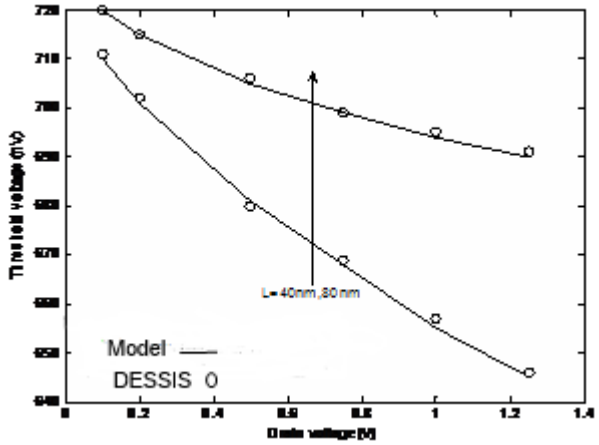

Fig.7: Plot of threshold voltage v/s drain bias for a Gaussian profile based DHDMG n-MOSFET for V_{SB} =0V, V_{DS} =0.5V for two different channel lengths,L=40 and 80 nm,taking N_{sub} =5*10^{17} cm^{-3} , $N_{av,Gauss}$ =5*10^{18} cm^{-3} ,L_p=10 nm.

It is found from Fig.7 that with an increase in the drain bias the threshold voltage is decreased.As the channel length decreases, the effect becomes more prominent.As the channel length increases the lateral electric field becomes less than the transverse electric field.Since the lateral electric field is strong at low drain bias for shorter channel devices,the drift current increases when the drain voltage is low and the deviation in the threshold voltage is high when the drain bias goes from low to high.

High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a device. Replacing the silicon dioxide dielectric with a high-k material allows increased gate capacitance without the leakage effects.

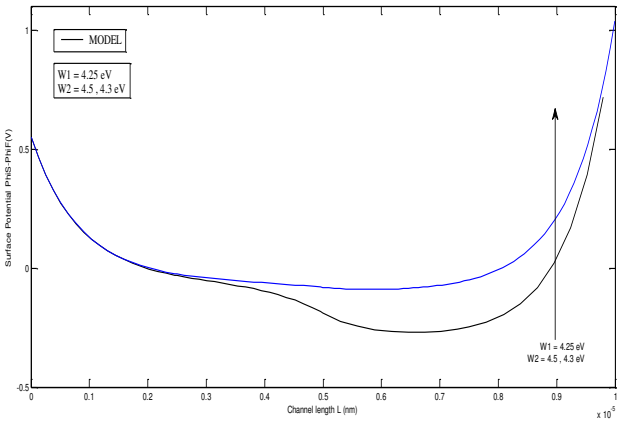

Fig. 8: Plot of surface potential v/s channel length plot for hafnium oxide dielectric obtained by varying work function W_2 = 4.5 eV, 4.3 eV and keeping V_{SB} = 0 V, V_{GS} = 0 V, V_{GB} = 0 V, W_1 = 4.25 eV and W_S = 4.68 eV constant.

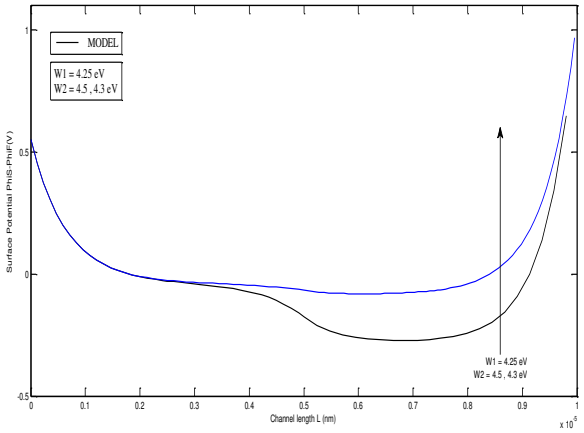

Fig. 9: Plot of surface potential v/s channel length plot for tantalum pentoxide dielectric obtained by varying work function W_2 = 4.5 eV, 4.3 eV and keeping V_{SB} = 0 V, V_{GS} = 0 V, V_{GB} = 0 V, W_1 = 4.25 eV and W_S = 4.68 eV constant.

From Fig 8 and Fig 9 it is seen that as the work function difference is increased the surface potential minima shifts downwards.

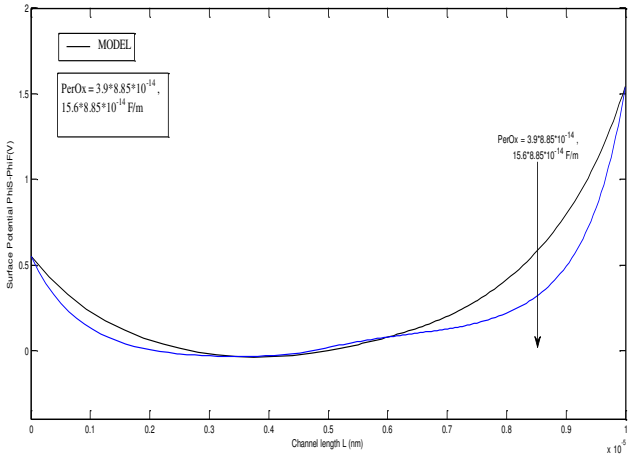

Fig 10: Plot of surface potential v/s channel length for silicon dioxide and hafnium oxide obtained by varying oxide permittivity using SiO_2 permittivity = 3.9*8.85*10^{-14} F/m, HfO_2 permittivity = 15.6*8.85*10^{-14} F/m and keeping V_{SB} = 0 V, V_{GS} = 0 V, V_{GB} = 0 V, W_1 = 4.25 eV, W_2 = 4.1 eV and W_S = 4.68 eV constant.

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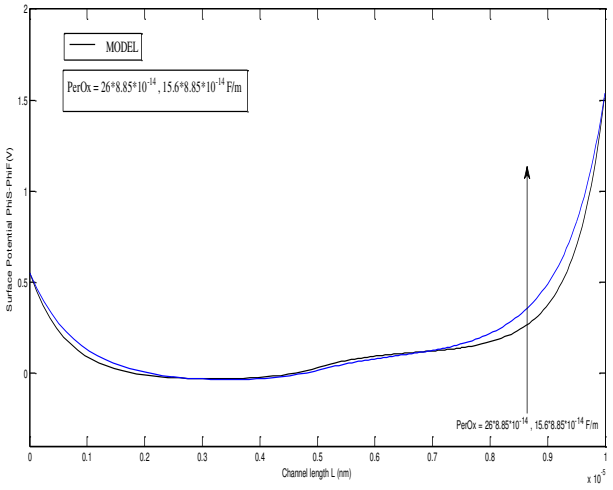

Fig 11: Plot of surface potential v/s channel length for HfO_2 and Ta_2O_5 obtained by varying oxide permittivity using Ta_2O_5 permittivity = $26*8.85*10^{-14}$ F/m, HfO_2 permittivity = $15.6*8.85*10^{-14}$ F/m and keeping $V_{SB} = 0$ V, $V_{GS} = 0$ V, $V_{GB} = 0$ V, $W_1 = 4.25$ eV, $W_2 = 4.1$ eV and $W_S = 4.68$ eV constant.

Fig 10 and Fig 11 shows that as the permittivity of the dielectric material is increased the surface potential decreases at the two ends since the capacitances increases.

IV.CONCLUSION

A two dimensional analytical model for the subthreshold surface potential and threshold voltage of asymmetric DHDMG MOSFETs with vertical Gaussian doping profile in the channel is proposed. The model is obtained using two gradual Gaussian doping profiles at the source and the drain ends and further reduced to a useful compact expression. The effects of doping profile parameters and device parameters on the threshold voltage of the DHDMG devices are also studied. The model results match well with the 2D-device simulator DESSIS for channel lengths above 30 nm. The shrinking of device dimension leads to reduction of gate oxide thickness. In order to overcome this drawback high-k materials are used instead of silicon dioxide, namely Hafnium oxide (HfO_2), Tantalum pentoxide (Ta_2O_5) and so on. In this paper we have demonstrated the results of the model by varying the various device parameters and bias voltages.

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