All-optical Adder with the Help of Terahertz Optical Asymmetric Demultiplexer Based Switch

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***Abstract*— All-optical 4-bit carry skip adder has been designed with the help of terahertz optical asymmetric demultiplexer (TOAD) or Semiconductor Optical Amplifier (SOA) - assisted Sagnac switches. This design promises to meet the present-day ultrafast digital communication which requires high speed and accuracy. We describe all-optical carry skip adder by using a set of all-optical multiplexer and all-optical full adder. This architecture of carry skip adder can be used to form a fast arithmetical processing unit than ripple carry adder and carry look-ahead adder. This theoretical model is proposed and verified through numerical simulation.**

Keywords- Terahertz optical asymmetric demultiplexer; semiconductor optical amplifier; carry skip adder; optical logic.

I. INTRODUCTION

Semiconductor optical amplifiers (SOAs) are among the most important research interest for their applications in all-optical logic and signal processing [1-4]. Their compactness, simplicity, large nonlinearities, and ease of integration make them suitable to perform a large range of functions such as regeneration, time-division demultiplexing, and Boolean logic and arithmetic operations [5-12]. The nonlinearities that enable SOAs to be used in such applications are governed by the dynamics of optically induced carriers. Addition is the most commonly used arithmetic operation and adder performs one of the most crucial functions of any digital processor, so careful optimization must be done to enhance the speed of this operation. This optimization is already being done in gate or circuit level by manipulating transistor sizes and circuit topology and also rearranging the Boolean equations so that faster or smaller even less power consumption circuit is obtained. Several adder configurations such as ripple carry adder, carry lookahead adder, carry select adder, conditional sum and various parallel prefix adders are being made to obtain an optimum area, delay and power requirements. Ripple carry adder is the simplest adder, but has the longest time delay O (n), where n is the operand size in bits. For our circuit the delay is O (n log n) and area is O (n). So far delay is concerns our circuit design gives the better performance. In this paper we use terahertz optical asymmetric demultiplexer (TOAD) based switch as basic unit to design all-optical 4-bit carry skip adder.

II. OPERATION OF TOAD BASED SWITCH

The basic structure of TOAD based switch is shown in Fig. 1 [13, 14].

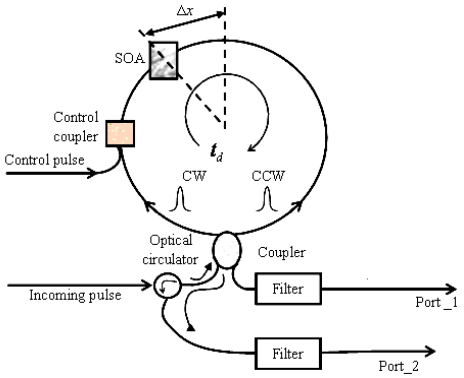

Figure 1. A TOAD based optical switch with single control pulse (CP), where SOA: Semiconductor optical amplifier, CW: Clockwise pulse, CCW: Counterclockwise pulse and Δx: asymmetric distance.

In this paper, we have tried to use the output from both the transmitting and reflecting mode of the device. The output power at port_1 and port_2 can be expressed as [15-17]

$$P_{out\_1}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (1)$$

$$P_{out\_2}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (2)$$

where, $G_{cw}(t), G_{ccw}(t)$ is the power gain. The time-dependent phase difference between clockwise (CW) and counter clockwise (CCW) pulses [15] is

$$\Delta\varphi = -\alpha/2 \cdot \ln\left(G_{cw}(t)/G_{ccw}(t)\right) \quad (3)$$

with α being the line-width enhancement factor. In the absence of a control signal, data signal (incoming signal) enters the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and experience the same unsaturated small amplifier gain G_{ss} , and recombine at the input coupler i.e. $G_{ccw} = G_{cw}$. Then,

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$\Delta\varphi = 0$ and expression for $P_{out\_1}(t) = 0$ and $P_{out\_2}(t) = P_{in}(t) \cdot G_{ss}$. It shows that data is reflected back toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. The gain of SOA decreases rapidly [14-16]. As a result, the two counter-propagation data signal will experience a differential gain saturation profiles i.e. $G_{ccw} \neq G_{cw}$. Therefore they recombine at the input coupler, and then $\Delta\varphi \approx -\pi$ the data will exit from the output port-1 i.e. $P_{out\_1}(t) \neq 0$ and $P_{out\_2}(t) \approx 0$, the corresponding values can be obtained from the equation (2). The energy of the control pulse is ten times greater than that of the incoming pulse. A filter may be used at the output of TOAD based switch to reject the control and pass the incoming pulse.

III. ALL-OPTICAL FULL ADDER

A full-adder adds binary numbers and accounts for values carried in as well as carried out. A one-bit full-adder (FA) adds three one-bit numbers, often written as *A*, *B*, and C_{in}. *A* and *B* are the operands, and C_{in} is a one-bit carried in (in theory, from a past addition). The circuit produces a two-bit output sum typically represented by the signals C_{out} (*carry*) and *S* (*sum*). Block diagram and all-optical circuit of the full-adder is shown in Fig. 2 and 3 respectively. The detail operation is proposed by Gayen and Roy [18].

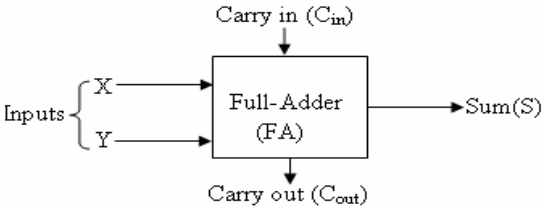

Figure 2. Block diagram of full adder (FA).

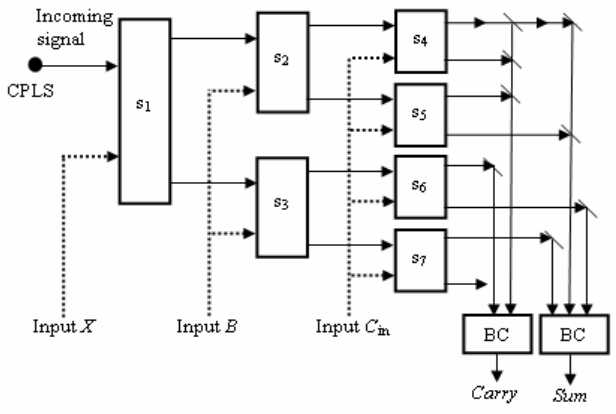

Figure 3. All-optical integrated full-adder [18], where CPLS: Constant pulse light source, *A*, *B*, and C_{in}: Input signals, s_1-s_7: TOAD based switches, BC: Beam combiner, \ : beam splitter, *Carry* and *Sum*: Final outputs.

Depending on the state of input variables (*A*, *B*, C_{in}) [these are also the light signals] the outputs are obtained from *Sum* and *Carry*. The logical expression of these outputs are,

$$S = ABC_{in} + A\bar{B}\bar{C}_{in} + \bar{A}B\bar{C}_{in} + \bar{A}\bar{B}C_{in} = \left(A \oplus B \oplus C_{in}\right) \quad (4)$$

$$C_{out} = ABC_{in} + AB\overline{C_{in}} + A\bar{B}C_{in} + \bar{A}BC_{in} = C\left(A \oplus B\right) + AB \quad (5)$$

IV. ALL-OPTICAL MULTIPLEXER

A multiplexer (MUX) is a combinational circuit that is given a certain number (usually a maximum of power of 2) of data inputs, let us say 2^n, and n address inputs (select inputs) used as a binary number to select one of the data inputs. The MUX has a single output, which has the same value as the selected data input. All-optical operational principle of the 2×1 MUX is explained in Fig. 4. To implement optical 2×1 MUX, we use TOAD based optical switches, namely s_1 through s_3, which have one select input (S_0), and two data inputs (D_0 and D_1). The block diagram of 2×1 multiplexer is shown in Fig. 5.

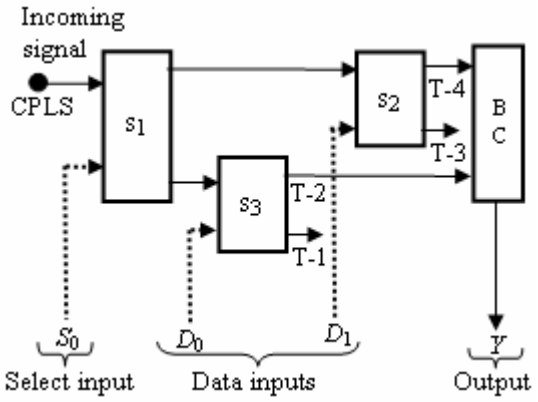

Figure 4. A unit-wise block diagram of all-optical 2×1 multiplexer, where CPLS: Constant pulse light source, S_0: Select input, D_0 and D_1: Data inputs, s_1-s_3: TOAD based switches, T-1 through T-4: Output terminals, BC: Beam combiner, and *Y*: Final output.

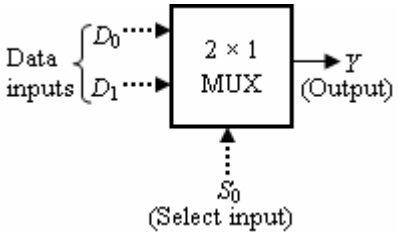

Figure 5. The block diagram of 2×1 multiplexer (MUX).

By applying proper control signal, we can guide the input data signal to one of the required output channels. Here, in the multiplexing scheme, we consider D_0 and D_1 are the input data signals, the control signal S_0 acts as a select input,

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and Y is the output signal. By the proper value of the control signal S_0 a particular input data signal (D_0 or D_1) is selected and this input data signal is then sent to the output Y. Two cases may arise as follows.

When $S_0 = 0$, the light that comes from Constant pulse light source (CPLS) is incident on switch s_1. As the control signal S_0 is absent, the light emerges through the lower channel of s_1 and falls on switch s_3, and no other channel receives the light. In switch s_3 the input data is D_0. Now, if $D_0 = 0$, then T-1 is in 1-state and the other terminals (i.e., T-2, T-3, and T-4) are in 0-state.

The final output is taken after combining the terminals T-2 and T-4 with the help of a beam combiner BC. So, no light is present at the output, i.e., $Y = 0$. Again, if $D_0 = 1$, then T-2 is in 1-state and the other terminals (i.e., T-1, T-3, and T-4) are in 0-state, and the light beam reaches to the beam combiner BC. The light is present at the output, i.e., $Y = 1$. Hence, we conclude that $Y = D_0$, when $S_0 = 0$. That means the input data D_0 can be sent to output Y by setting $S_0 = 0$.

On the other hand, when $S_0 = 1$, the light from CPLS is incident on switch s_1 first. As $S_0 = 1$, the light emerges through the upper channel of s_1 and falls on s_2. In the switch s_2 the input data is D_1. Now, if $D_1 = 0$, then T-3 is at 1-state and the other terminals (i.e., T-1, T-2, and T-4) are in 0-state. So, no light is present at output Y.

Again, if $D_1 = 1$, then T-4 is in 1-state and the other terminals (i.e., T-1, T-2, and T-3) are in 0-state, and the light beam reaches to the beam combiner BC. So, the light is present at the output, i.e., $Y = 1$. Hence, we conclude that $Y = D_1$, when $S_0 = 1$. That means the input data D_1 can be sent to output Y by setting $S_0 = 1$. This is how we realize a multiplexer with the help of TOAD based all-optical switches. The logical expression of multiplexer output is:

$$Y = S_0 D_1 + \overline{S}_0 D_0 \qquad (6)$$

V. Design of All-optical Carry Skip Adder

A ripple-carry adder is a linear dependent on the carry of each block addition, that is the carry bit is "rippled" from one stage to the other, thus the delay through the circuit depends on the number of logic stages that must be traversed and is a function of the applied input signals, so its usage becomes utterly impractical for long word length. So to overcome this, we have designed an adder which simultaneously calculates addition of the next two bits, thus reducing the number of gate delays. A carry-skip adder reduces the carry-propagation time by skipping over groups of consecutive adder stages. This adder simultaneously adds over next two bits by considering two types of carry, 1 or 0, while adding present by least significant bit (LSB). This method is faster than ripple carry adder because it simultaneously adds next two bits without considering the carry from the LSB. A 4-bit carry skip adder with the help of full adders (FA) and 2×1 multiplexers (MUX) is shown in the Fig. 6.

In this circuit first two LSB (A_0, A_1, B_0, and B_1) of each number are added with set of two full adders (FA-1 and FA-2), then next two bits are added simultaneously considering $c_0 = 1$ and $c_0 = 0$ with two sets of two full adders each. Here in this circuit bits A_0 and A_1 are added with B_0 and B_1 respectively using two full adders along with the carry c_{in}. The full adder FA-1 takes the three inputs as A_0, B_0 and C_{in} and produces the output S_0 and carry for the full adder FA-2. Again full adder FA-2 receives the three inputs as A_1, B_1 and carryout from FA-1 and generates the output S_1 and carryout. This carryout acts as select line s for the multiplexers MUX-1, MUX-2 and MUX-3. Simultaneously when this process is going on, full adder FA-3 takes the three inputs as A_2, B_2 and $C_0 = 1$ and produces the output, which acts as a data line D_1 for MUX-1 and carry for the full adder FA-4. Similarly, the output and carry from FA-4 operates as data line D_1 for the multiplexer MUX-2 and MUX-3 respectively. In this similar way, output from FA-5, output and carry from FA-6 act as a data line D_0 for multiplexers MUX-1, MUX-2 and MUX-3, respectively. Depending on the value of the select line s, MUX-1, MUX-2 and MUX-3 produce the output S_2, S_3 and C_{out} respectively. So the final output of this circuit is $C_{out}S_3S_2S_1S_0$.

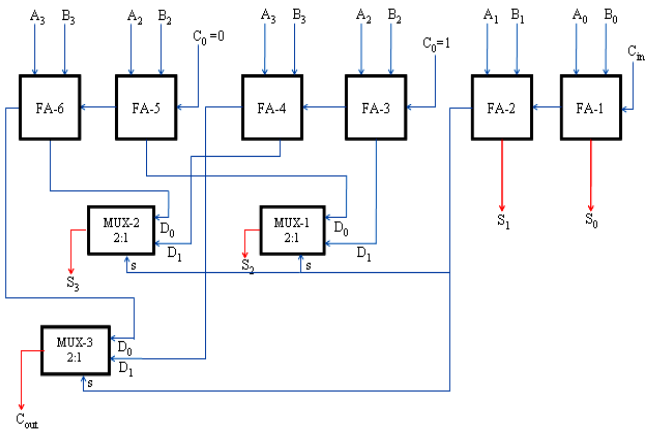

Figure 6. Block diagram of all-optical carry skip adder.FA: full adder, MUX: 2× 1 multiplexer.

Let us consider an example, where A = 1100 ($A_3A_2A_1A_0$), B =1001 ($B_3B_2B_1B_0$) and $C_{in} = 0$. According to the operational principle of full adder $S_0 = 1$ and $S_1 = 0$. In case the value of the select input for three multiplexers is 0, i.e., s = 0. So for all the multiplexers the data line D_0 will be selected. In this case output S_2, S_3 and C_{out} of multiplexes MXU-1, MUX-2 and MUX-3 receives the value 1, 0 and 1, respectively. So the final output is 10101 ($C_{out}S_3S_2S_1S_0$). In this similar way, any two 4-bit numbers are added with the help of carry skip adder.

VI. Simulated Results

The parameters used in this simulation are as follows: unsaturated amplifier gain of the SOA (Gss) = 30 dB, gain recovery time of SOA (τ_e) = 90 ps, saturation energy of the SOA (Esat) = 700 fJ, eccentricity of the loop (T_{asym}) = 30 ps, line-width enhancement factor (α) = 6, full width at half

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maximum of control pulse (σ) = 6 ps, bit period (T_c) = 100 ps, and a control pulse energy (E_{cp}) = 70 fJ so that the operational conditions are satisfied. The simulated input and output waveforms are given in Fig. 7.

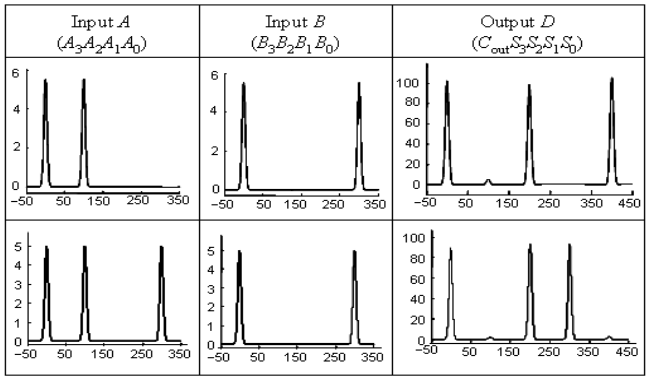

Figure 7. Simulated input and output waveforms, power (mW) is along the y-axis and time is along the x-axis in ps.

VII. CONCLUSION

In this paper, we have reported a novel design of TOAD based carry skip adder. Here, in this proposed scheme, the significant advantage is that the proposed converter circuit can perform addition operations, which are all-optical in nature. This architecture of carry skip adder can be used to form a fast processor unit than ripple carry adder and carry look-ahead adder. This theoretical model has been verified through numerical simulation.

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