Függelék

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **vhdl\_test\_1** **IS**

PORT (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **vhdl\_test\_1**;

**ARCHITECTURE** **Behavioral** **OF** **vhdl\_test\_1** **IS**

**COMPONENT** **vhdl\_test\_1a** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **Add** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**SIGNAL** signal\_a\_0 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_a\_0\_rdy : **BOOLEAN**;

**SIGNAL** signal\_b\_1 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_b\_1\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_3\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_2 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_2\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_4\_rdy : **BOOLEAN**;

**BEGIN**

vhdl\_test\_1a3 : vhdl\_test\_1a

**PORT** **MAP**(rst, loop\_rst, clk, signal\_a\_0, signal\_a\_0\_rdy, signal\_b\_1, signal\_b\_1\_rdy, signal\_out\_2, signal\_out\_2\_rdy);

add4 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_out\_2, signal\_out\_2\_rdy, signal\_b\_1, signal\_b\_1\_rdy, signal\_out\_3, signal\_out\_3\_rdy);

add5 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_out\_3, signal\_out\_3\_rdy, signal\_a\_0, signal\_a\_0\_rdy, signal\_out\_4, signal\_out\_4\_rdy);

signal\_a\_0 <= a;

signal\_a\_0\_rdy <= a\_rdy;

signal\_b\_1 <= b;

signal\_b\_1\_rdy <= b\_rdy;

ret <= signal\_out\_4;

ret\_rdy <= signal\_out\_4\_rdy;

**END** **Behavioral**;

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **vhdl\_test\_1a** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **vhdl\_test\_1a**;

**ARCHITECTURE** **Behavioral** **OF** **vhdl\_test\_1a** **IS**

**COMPONENT** **Init** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **Add** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**CONSTANT** constant\_5 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000000000";

**CONSTANT** constant\_5\_rdy : **BOOLEAN** := true;

**SIGNAL** signal\_out\_9 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_9\_rdy : **BOOLEAN**;

**SIGNAL** signal\_a\_7 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_a\_7\_rdy : **BOOLEAN**;

**SIGNAL** signal\_b\_8 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_b\_8\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_10 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_10\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_6 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_6\_rdy : **BOOLEAN**;

**BEGIN**

init0 : Init

**PORT** **MAP**(rst, loop\_rst, clk, constant\_5, constant\_5\_rdy, signal\_out\_6, signal\_out\_6\_rdy);

add1 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_a\_7, signal\_a\_7\_rdy, signal\_b\_8, signal\_b\_8\_rdy, signal\_out\_9, signal\_out\_9\_rdy);

add2 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_out\_6, signal\_out\_6\_rdy, signal\_out\_9, signal\_out\_9\_rdy, signal\_out\_10, signal\_out\_10\_rdy);

signal\_a\_7 <= a;

signal\_a\_7\_rdy <= a\_rdy;

signal\_b\_8 <= b;

signal\_b\_8\_rdy <= b\_rdy;

ret <= signal\_out\_10;

ret\_rdy <= signal\_out\_10\_rdy;

**END** **Behavioral**;

1. függelék vhdl\_test\_1 VHDL kód

2. függelék vhdl\_test\_1a VHDL kód

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **sim\_vhdl\_test\_1** **IS**

**END** **sim\_vhdl\_test\_1**;

**ARCHITECTURE** **Behavioral** **OF** **sim\_vhdl\_test\_1** **IS**

**COMPONENT** **vhdl\_test\_1**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **sim\_clock** **IS**

**PORT** (clk : **OUT** **std\_logic**);

**END** **COMPONENT**;

**SIGNAL** signal\_clk : **STD\_LOGIC**;

**SIGNAL** signal\_in\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_3\_rdy : **BOOLEAN**;

**SIGNAL** signal\_in\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_rst : **STD\_LOGIC**;

**SIGNAL** signal\_rst\_loop : **STD\_LOGIC**;

**BEGIN**

test\_inst : vhdl\_test\_1

**PORT** **MAP**(

signal\_rst,

signal\_rst\_loop,

signal\_clk,

signal\_in\_3,

signal\_in\_3\_rdy,

signal\_in\_4,

signal\_in\_4\_rdy,

signal\_out\_4,

signal\_out\_4\_rdy

);

clk1 : sim\_clock **PORT** **MAP**(signal\_clk);

proc : **PROCESS**

**BEGIN**

signal\_rst\_loop <= '0';

signal\_rst <= '0';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**0**, **32**));

signal\_in\_3\_rdy <= true;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**0**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **200**ns;

signal\_rst <= '1';

signal\_in\_3\_rdy <= false;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**1**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **10**ns;

signal\_rst <= '0';

**WAIT** **FOR** **100**ns;

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**3**, **32**));

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **200**ns;

signal\_rst <= '1';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**7**, **32**));

signal\_in\_3\_rdy <= false;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**123**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **10**ns;

signal\_rst <= '0';

**WAIT** **FOR** **100**ns;

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **1000**ns;

**END** **PROCESS**;

**END** **Behavioral**;

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **vhdl\_test\_2** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

sum : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

sum\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **vhdl\_test\_2**;

**ARCHITECTURE** **Behavioral** **OF** **vhdl\_test\_2** **IS**

**COMPONENT** **Init** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **Assign** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **loop10** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

d0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

d0\_rdy : **IN** **BOOLEAN**;

d1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

d1\_rdy : **IN** **BOOLEAN**;

x0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

x0\_rdy : **IN** **BOOLEAN**;

z1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

z1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**CONSTANT** constant\_12 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000000000";

**CONSTANT** constant\_12\_rdy : **BOOLEAN** := true;

**CONSTANT** constant\_11 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000010100";

**CONSTANT** constant\_11\_rdy : **BOOLEAN** := true;

**SIGNAL** signal\_out\_14 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_14\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_13 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_13\_rdy : **BOOLEAN**;

**SIGNAL** signal\_sum\_15 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_sum\_15\_rdy : **BOOLEAN**;

**SIGNAL** signal\_z1\_16 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_z1\_16\_rdy : **BOOLEAN**;

**BEGIN**

init7 : Init

**PORT** **MAP**(rst, loop\_rst, clk, constant\_11, constant\_11\_rdy, signal\_out\_13, signal\_out\_13\_rdy);

assign8 : Assign

**PORT** **MAP**(rst, loop\_rst, clk, constant\_12, constant\_12\_rdy, signal\_out\_14, signal\_out\_14\_rdy);

loop10node0 : loop10

**PORT** **MAP**(rst, loop\_rst, clk, signal\_sum\_15, signal\_sum\_15\_rdy, signal\_out\_14, signal\_out\_14\_rdy, signal\_out\_13, signal\_out\_13\_rdy, signal\_z1\_16, signal\_z1\_16\_rdy);

signal\_sum\_15 <= sum;

signal\_sum\_15\_rdy <= sum\_rdy;

ret <= signal\_z1\_16;

ret\_rdy <= signal\_z1\_16\_rdy;

**END** **Behavioral**;

3. függelék vhdl\_test\_1 szimulációjához használt VHDL kód

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **loop10** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

d0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

d0\_rdy : **IN** **BOOLEAN**;

d1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

d1\_rdy : **IN** **BOOLEAN**;

x0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

x0\_rdy : **IN** **BOOLEAN**;

z1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

z1\_rdy : **OUT** **BOOLEAN**

);

**END** **loop10**;

**ARCHITECTURE** **Behavioral** **OF** **loop10** **IS**

**COMPONENT** **hig9** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

f0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

f0\_rdy : **IN** **BOOLEAN**;

f1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

f1\_rdy : **IN** **BOOLEAN**;

X0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

X0\_rdy : **IN** **BOOLEAN**;

c : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c\_rdy : **OUT** **BOOLEAN**;

y0 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

y0\_rdy : **OUT** **BOOLEAN**;

y1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

y1\_rdy : **OUT** **BOOLEAN**;

Z1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

Z1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **Phi** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**SIGNAL** signal\_loop\_rst : **STD\_LOGIC**;

**SIGNAL** signal\_rst : **STD\_LOGIC**;

**SIGNAL** signal\_clk : **STD\_LOGIC**;

**SIGNAL** signal\_c : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_c\_rdy : **BOOLEAN**;

**SIGNAL** signal\_f1\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_f1\_3\_rdy : **BOOLEAN**;

**SIGNAL** signal\_x0\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_x0\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_y0\_5 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_y0\_5\_rdy : **BOOLEAN**;

**SIGNAL** signal\_y1\_6 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_y1\_6\_rdy : **BOOLEAN**;

**SIGNAL** signal\_d1\_2 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_d1\_2\_rdy : **BOOLEAN**;

**SIGNAL** signal\_f0\_1 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_f0\_1\_rdy : **BOOLEAN**;

**SIGNAL** signal\_Z1\_7 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_Z1\_7\_rdy : **BOOLEAN**;

**SIGNAL** signal\_d0\_0 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_d0\_0\_rdy : **BOOLEAN**;

**BEGIN**

signal\_rst <= rst **OR** loop\_rst;

signal\_clk <= clk;

signal\_d0\_0 <= d0;

signal\_d1\_2 <= d1;

signal\_x0\_4 <= x0;

z1 <= signal\_Z1\_7;

signal\_d0\_0\_rdy <= d0\_rdy;

signal\_d1\_2\_rdy <= d1\_rdy;

signal\_x0\_4\_rdy <= x0\_rdy;

loop\_component : hig9

**PORT** **MAP**(

signal\_rst, signal\_loop\_rst, signal\_clk, signal\_f0\_1, signal\_f0\_1\_rdy, signal\_f1\_3, signal\_f1\_3\_rdy, signal\_x0\_4, signal\_x0\_4\_rdy

signal\_c, signal\_c\_rdy, signal\_y0\_5, signal\_y0\_5\_rdy,

signal\_y1\_6, signal\_y1\_6\_rdy, signal\_Z1\_7, signal\_Z1\_7\_rdy

);

phi\_0 : Phi

**PORT** **MAP**(

signal\_rst, signal\_loop\_rst, signal\_clk, signal\_d0\_0, signal\_d0\_0\_rdy,

signal\_y0\_5, signal\_y0\_5\_rdy, signal\_f0\_1, signal\_f0\_1\_rdy

);

phi\_1 : Phi

**PORT** **MAP**(

signal\_rst, signal\_loop\_rst, signal\_clk, signal\_d1\_2, signal\_d1\_2\_rdy,

signal\_y1\_6, signal\_y1\_6\_rdy, signal\_f1\_3, signal\_f1\_3\_rdy

);

loop\_process : **PROCESS** (clk, signal\_rst)

**VARIABLE** is\_loop\_finished : **BOOLEAN** := false;

**VARIABLE** buffer\_z1 : **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**)

;

**BEGIN**

**IF** rising\_edge(signal\_rst) **THEN**

is\_loop\_finished := false;

z1\_rdy <= false;

**ELSIF** falling\_edge(signal\_rst) **THEN**

**ELSIF** signal\_c\_rdy **AND** signal\_y0\_5\_rdy **AND** signal\_y1\_6\_rdy **AND** signal\_Z1\_7\_rdy **THEN**

**IF** signed(signal\_c) > to\_signed(**0**, **32**) **THEN**

z1\_rdy <= false;

signal\_loop\_rst <= '1';

**ELSE**

**IF** **NOT** is\_loop\_finished **THEN**

buffer\_z1 := signal\_Z1\_7;

is\_loop\_finished := true;

**END** **IF**;

z1 <= buffer\_z1;

z1\_rdy <= true;

**END** **IF**;

**ELSE**

signal\_loop\_rst <= '0';

**END** **IF**;

**END** **PROCESS**;

**END** **Behavioral**;

4. függelék vhdl\_test\_2 nevű HIGCompból generált VHDL kód

5. függelék LoopCompból generált VHDL kód

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **hig9** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

f0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

f0\_rdy : **IN** **BOOLEAN**;

f1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

f1\_rdy : **IN** **BOOLEAN**;

X0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

X0\_rdy : **IN** **BOOLEAN**;

c : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c\_rdy : **OUT** **BOOLEAN**;

y0 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

y0\_rdy : **OUT** **BOOLEAN**;

y1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

y1\_rdy : **OUT** **BOOLEAN**;

Z1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

Z1\_rdy : **OUT** **BOOLEAN**

);

**END** **hig9**;

**ARCHITECTURE** **Behavioral** **OF** **hig9** **IS**

**COMPONENT** **LT** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **Add** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**CONSTANT** constant\_17 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000000101";

**CONSTANT** constant\_17\_rdy : **BOOLEAN** := true;

**CONSTANT** constant\_18 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000000001";

**CONSTANT** constant\_18\_rdy : **BOOLEAN** := true;

**SIGNAL** signal\_out\_23 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_23\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_24 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_24\_rdy : **BOOLEAN**;

**SIGNAL** signal\_f1\_19 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_f1\_19\_rdy : **BOOLEAN**;

**SIGNAL** signal\_X0\_22 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_X0\_22\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_20 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_20\_rdy : **BOOLEAN**;

**SIGNAL** signal\_f0\_21 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_f0\_21\_rdy : **BOOLEAN**;

**BEGIN**

lT11 : LT

**PORT** **MAP**(rst, loop\_rst, clk, signal\_f1\_19, signal\_f1\_19\_rdy, constant\_17, constant\_17\_rdy, signal\_out\_20, signal\_out\_20\_rdy);

add12 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_f0\_21, signal\_f0\_21\_rdy, signal\_X0\_22, signal\_X0\_22\_rdy, signal\_out\_23, signal\_out\_23\_rdy);

add13 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_f1\_19, signal\_f1\_19\_rdy, constant\_18, constant\_18\_rdy, signal\_out\_24, signal\_out\_24\_rdy);

signal\_f0\_21 <= f0;

signal\_f0\_21\_rdy <= f0\_rdy;

signal\_f1\_19 <= f1;

signal\_f1\_19\_rdy <= f1\_rdy;

signal\_X0\_22 <= X0;

signal\_X0\_22\_rdy <= X0\_rdy;

c <= signal\_out\_20;

c\_rdy <= signal\_out\_20\_rdy;

y0 <= signal\_out\_23;

y0\_rdy <= signal\_out\_23\_rdy;

y1 <= signal\_out\_24;

y1\_rdy <= signal\_out\_24\_rdy;

Z1 <= signal\_f0\_21;

Z1\_rdy <= signal\_f0\_21\_rdy;

**END** **Behavioral**;

6. függelék A ciklusmag VHDL kódja

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **loop10\_sim** **IS**

**END** **loop10\_sim**;

**ARCHITECTURE** **Behavioral** **OF** **loop10\_sim** **IS**

**COMPONENT** **vhdl\_test\_2** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

sum : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

sum\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **sim\_clock** **IS**

**PORT** (clk : **OUT** **std\_logic**);

**END** **COMPONENT**;

**CONSTANT** constant\_5 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000010100";

**CONSTANT** constant\_5\_rdy : **BOOLEAN** := true;

**SIGNAL** signal\_clk : **STD\_LOGIC**;

**SIGNAL** signal\_in\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_3\_rdy : **BOOLEAN**;

**SIGNAL** signal\_in\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_rst : **STD\_LOGIC**;

**SIGNAL** signal\_rst\_loop : **STD\_LOGIC**;

**BEGIN**

loop1 : vhdl\_test\_2

**PORT** **MAP**(

signal\_rst,

signal\_rst\_loop,

signal\_clk,

signal\_in\_3,

signal\_in\_3\_rdy,

signal\_out\_4,

signal\_out\_4\_rdy

);

clk1 : sim\_clock

**PORT** **MAP**(signal\_clk);

proc : **PROCESS**

**BEGIN**

signal\_rst\_loop <= '0';

signal\_rst <= '0';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**1**, **32**));

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **400**ns;

signal\_rst <= '1';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**30**, **32**));

signal\_in\_3\_rdy <= false;

**WAIT** **FOR** **10**ns;

signal\_rst <= '0';

**WAIT** **FOR** **50**ns;

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **1000**ns;

**END** **PROCESS**;

**END** **Behavioral**;

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **sim\_vhdl\_test\_3** **IS**

**END** **sim\_vhdl\_test\_3**;

**ARCHITECTURE** **Behavioral** **OF** **sim\_vhdl\_test\_3** **IS**

**COMPONENT** **vhdl\_test\_3** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **sim\_clock** **IS**

**PORT** (clk : **OUT** **std\_logic**);

**END** **COMPONENT**;

**SIGNAL** signal\_clk : **STD\_LOGIC**;

**SIGNAL** signal\_in\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_3\_rdy : **BOOLEAN**;

**SIGNAL** signal\_in\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_in\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_rst : **STD\_LOGIC**;

**SIGNAL** signal\_rst\_loop : **STD\_LOGIC**;

**BEGIN**

test\_inst : vhdl\_test\_3

**PORT** **MAP**(

signal\_rst,

signal\_rst\_loop,

signal\_clk,

signal\_in\_3,

signal\_in\_3\_rdy,

signal\_in\_4,

signal\_in\_4\_rdy,

signal\_out\_4,

signal\_out\_4\_rdy

);

clk1 : sim\_clock

**PORT** **MAP**(signal\_clk);

proc : **PROCESS**

**BEGIN**

signal\_rst\_loop <= '0';

signal\_rst <= '0';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**0**, **32**));

signal\_in\_3\_rdy <= true;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**1234**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **200**ns;

signal\_rst <= '1';

signal\_in\_3\_rdy <= false;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**1**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **10**ns;

signal\_rst <= '0';

**WAIT** **FOR** **100**ns;

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**4**, **32**));

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **200**ns;

signal\_rst <= '1';

signal\_in\_3 <= **std\_logic\_vector**(to\_unsigned(**7**, **32**));

signal\_in\_3\_rdy <= false;

signal\_in\_4 <= **std\_logic\_vector**(to\_unsigned(**123**, **32**));

signal\_in\_4\_rdy <= true;

**WAIT** **FOR** **10**ns;

signal\_rst <= '0';

**WAIT** **FOR** **100**ns;

signal\_in\_3\_rdy <= true;

**WAIT** **FOR** **1000**ns;

**END** **PROCESS**;

**END** **Behavioral**;

7. függelék A LoopComp szimulációjához használt VHDL kód

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **vhdl\_test\_3** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

a : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

a\_rdy : **IN** **BOOLEAN**;

b : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

b\_rdy : **IN** **BOOLEAN**;

ret : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

ret\_rdy : **OUT** **BOOLEAN**

);

**END** **vhdl\_test\_3**;

**ARCHITECTURE** **Behavioral** **OF** **vhdl\_test\_3** **IS**

**COMPONENT** **sel15** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

i0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

i0\_rdy : **IN** **BOOLEAN**;

i1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

i1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**SIGNAL** signal\_c4\_27 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_c4\_27\_rdy : **BOOLEAN**;

**SIGNAL** signal\_a\_25 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_a\_25\_rdy : **BOOLEAN**;

**SIGNAL** signal\_b\_26 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_b\_26\_rdy : **BOOLEAN**;

**BEGIN**

sel15node1 : sel15

**PORT** **MAP**(rst, loop\_rst, clk, signal\_a\_25, signal\_a\_25\_rdy, signal\_a\_25, signal\_a\_25\_rdy, signal\_b\_26, signal\_b\_26\_rdy, signal\_c4\_27, signal\_c4\_27\_rdy);

signal\_a\_25 <= a;

signal\_a\_25\_rdy <= a\_rdy;

signal\_b\_26 <= b;

signal\_b\_26\_rdy <= b\_rdy;

ret <= signal\_c4\_27;

ret\_rdy <= signal\_c4\_27\_rdy;

**END** **Behavioral**;

8. függelék vhdl\_test\_3 szimulációjához használt VHDL kód

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **sel15** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

i0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

i0\_rdy : **IN** **BOOLEAN**;

i1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

i1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **sel15**;

**ARCHITECTURE** **Behavioral** **OF** **sel15** **IS**

**COMPONENT** **c20** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input8 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input8\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **c16** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input3 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input3\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**COMPONENT** **c18** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input5 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input5\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**CONSTANT** constant\_0 : signed (**31** **DOWNTO** **0**) := to\_signed(**0**, **32**);

**CONSTANT** constant\_1 : signed (**31** **DOWNTO** **0**) := to\_signed(**4**, **32**);

**SIGNAL** signal\_c4\_2 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_c4\_2\_rdy : **BOOLEAN**;

**SIGNAL** signal\_c4\_4 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_c4\_4\_rdy : **BOOLEAN**;

**SIGNAL** signal\_c4\_3 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_c4\_3\_rdy : **BOOLEAN**;

**BEGIN**

case0 : c16

**PORT** **MAP**(rst, loop\_rst, clk, input2, input2\_rdy, i0, i0\_rdy, i1, i1\_rdy, signal\_c4\_2, signal\_c4\_2\_rdy);

case1 : c18

**PORT** **MAP**(rst, loop\_rst, clk, input2, input2\_rdy, i0, i0\_rdy, i1, i1\_rdy, signal\_c4\_3, signal\_c4\_3\_rdy);

case2 : c20

**PORT** **MAP**(rst, loop\_rst, clk, input2, input2\_rdy, i0, i0\_rdy, i1, i1\_rdy, signal\_c4\_4, signal\_c4\_4\_rdy);

proc : **PROCESS** (clk)

**BEGIN**

**IF** input2\_rdy **THEN**

**IF**

signed(input2) = constant\_0 **THEN**

c4 <= signal\_c4\_2;

c4\_rdy <= signal\_c4\_2\_rdy;

**ELSIF**

signed(input2) = constant\_1 **THEN**

c4 <= signal\_c4\_3;

c4\_rdy <= signal\_c4\_3\_rdy;

**ELSE**

c4 <= signal\_c4\_4;

c4\_rdy <= signal\_c4\_4\_rdy;

**END** **IF**;

**ELSE**

c4\_rdy <= false;

**END** **IF**;

**END** **PROCESS**;

**END** **Behavioral**;

9. függelék vhdl\_test\_3 HIGComp VHDL kódja

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **c16** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input3 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input3\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **c16**;

**ARCHITECTURE** **Behavioral** **OF** **c16** **IS**

**COMPONENT** **Assign** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**SIGNAL** signal\_out\_29 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_29\_rdy : **BOOLEAN**;

**SIGNAL** signal\_I0\_28 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_I0\_28\_rdy : **BOOLEAN**;

**BEGIN**

assign17 : Assign

**PORT** **MAP**(rst, loop\_rst, clk, signal\_I0\_28, signal\_I0\_28\_rdy, signal\_out\_29, signal\_out\_29\_rdy);

signal\_I0\_28 <= I0;

signal\_I0\_28\_rdy <= I0\_rdy;

c4 <= signal\_out\_29;

c4\_rdy <= signal\_out\_29\_rdy;

**END** **Behavioral**;

10. függelék sel15 SelComp VHDL kódja

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **c18** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input5 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input5\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **c18**;

**ARCHITECTURE** **Behavioral** **OF** **c18** **IS**

**COMPONENT** **Add** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**SIGNAL** signal\_I0\_30 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_I0\_30\_rdy : **BOOLEAN**;

**SIGNAL** signal\_I1\_31 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_I1\_31\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_32 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_32\_rdy : **BOOLEAN**;

**BEGIN**

add19 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_I0\_30, signal\_I0\_30\_rdy, signal\_I1\_31, signal\_I1\_31\_rdy, signal\_out\_32, signal\_out\_32\_rdy);

signal\_I0\_30 <= I0;

signal\_I0\_30\_rdy <= I0\_rdy;

signal\_I1\_31 <= I1;

signal\_I1\_31\_rdy <= I1\_rdy;

c4 <= signal\_out\_32;

c4\_rdy <= signal\_out\_32\_rdy;

**END** **Behavioral**;

11. függelék c16 HIGComp VHDL kódja (sel15 case0)

**LIBRARY** **IEEE**;

**USE** **IEEE.STD\_LOGIC\_1164.ALL**;

**USE** **IEEE.Numeric\_STD.ALL**;

**ENTITY** **c20** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input8 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input8\_rdy : **IN** **BOOLEAN**;

I0 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I0\_rdy : **IN** **BOOLEAN**;

I1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

I1\_rdy : **IN** **BOOLEAN**;

c4 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

c4\_rdy : **OUT** **BOOLEAN**

);

**END** **c20**;

**ARCHITECTURE** **Behavioral** **OF** **c20** **IS**

**COMPONENT** **Add** **IS**

**PORT** (

rst : **IN** **STD\_LOGIC**;

loop\_rst : **IN** **STD\_LOGIC**;

clk : **IN** **STD\_LOGIC**;

input1 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input1\_rdy : **IN** **BOOLEAN**;

input2 : **IN** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

input2\_rdy : **IN** **BOOLEAN**;

output1 : **OUT** **STD\_LOGIC\_vector**(**31** **DOWNTO** **0**);

output1\_rdy : **OUT** **BOOLEAN**

);

**END** **COMPONENT**;

**CONSTANT** constant\_33 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**) := "00000000000000000000000000001010";

**CONSTANT** constant\_33\_rdy : **BOOLEAN** := true;

**SIGNAL** signal\_out\_36 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_36\_rdy : **BOOLEAN**;

**SIGNAL** signal\_out\_37 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_out\_37\_rdy : **BOOLEAN**;

**SIGNAL** signal\_I1\_35 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_I1\_35\_rdy : **BOOLEAN**;

**SIGNAL** signal\_I0\_34 : **STD\_LOGIC\_VECTOR** (**31** **DOWNTO** **0**);

**SIGNAL** signal\_I0\_34\_rdy : **BOOLEAN**;

**BEGIN**

add21 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_I0\_34, signal\_I0\_34\_rdy, signal\_I1\_35, signal\_I1\_35\_rdy, signal\_out\_36, signal\_out\_36\_rdy);

add22 : Add

**PORT** **MAP**(rst, loop\_rst, clk, signal\_out\_36, signal\_out\_36\_rdy, constant\_33, constant\_33\_rdy, signal\_out\_37, signal\_out\_37\_rdy);

signal\_I0\_34 <= I0;

signal\_I0\_34\_rdy <= I0\_rdy;

signal\_I1\_35 <= I1;

signal\_I1\_35\_rdy <= I1\_rdy;

c4 <= signal\_out\_37;

c4\_rdy <= signal\_out\_37\_rdy;

**END** **Behavioral**;

12. függelék c18 HIGComp VHDL kódja (sel15 case1)

13. függelék c20 HIGComp VHDL kódja (sel15 case2, default)