

# Kristoffer O. W. Nordström

Neugasse 84  
CH-8005 Zürich

Date of Birth: 1<sup>st</sup> of April 1985

Nationalities: Swiss and Swedish

Mobile: +41 76 566 14 88

kristoffer@nordstroem.ch

github.com/kown7

## Objective

I'm looking forward to tackle your testing and verification challenges at the intersection of FPGA, SW, and embedded systems. Leveraging a decade of experience in space, railways, and communication applications to drive excellence in your projects. I want to contribute in a collaborative environment that provides growth opportunities.

---

## Practical Experience

### Development Engineer

2017-12 – current

Super Computing Systems AG, Zürich

Test Engineer for an interlocking system's subsystems. These subsystems were directly or over ethernet connected FPGA modules whose firmwares were developed according to EN50128: either SIL0 or SIL4.

- I derived and written the test specifications from the requirements for the various subsystems according to their safety requirements.
- I designed and implemented the test harness (FPGA boards with custom VHDL code) and the test cases.
  - Connected through PCIe to host computer with custom *Linux* drivers
  - DUT connected through Ethernet or GPIO pins
  - Test cases have been written in *Python* and the test scripts orchestrated through *pytest*.
- I was working on verification tasks for various application specific documentation
- Writing design documents for the application generating software

Proof-of-concept to connect multiple ADC through a FPGA with DMA to an NXP iMX8 SoM. The task included requirements facing various units at the customer, adapting kernel modules and user-space software to show the data transfers.

I was assigned the role of *Technology Ambassador*. Supporting the management team with strategic decisions concerning our technology stacks. Amongst others:

- supporting technology roadmap, e.g., high-level synthesis, test-automation with *vu-nit*
- organizing the annual internal *Hackday*

### Maintainer sltoo.dev

2018-02 – current

Added traceability features to *rmtoo*. Improvements with package managing lead to the fork *sltoo*. Accepted speaker at SWISSED21.

### FPGA Development Engineer

2015-06 – 2017-11

nanoTronic GmbH, Lyss

Software Engineer in a customer project. Upgrading an ethernet and STM32 based legacy application to a wireless solution on a ESP32 chip. Mainly responsible for refactoring the C/C++ code-base and requirements engineering with the customer.

FPGA firmware verification engineer on an ESM/Orion sub-system, see Artemis I. I was responsible for ensuring the firmware conformed to the specifications (ECSS) written by the customer and derived in-house works.

**Software Engineer** 2015-04 – 2015-06  
Helveting Engineering AG, Neuenhof

**FPGA Development Engineer** 2014-01 – 2014-12  
Super Computing Systems, Zürich

For an application in biochemical analysis:

- Development and verification of data and control paths for a high-speed digital receiver in VHDL
- Porting Existing code to a 7 Series Xilinx FPGA

**Education** **MSc ETH** in Electrical Engineering and Information Technology 2011-09 – 2013-01  
ETH Zürich, grade average: 5.18  
Focus Microelectronics and Communication

Master's thesis: *Tuneable Operational Transconductance Amplifier in Deep Submicron CMOS*. A tunable OTA for a LTE+ baseband filter has been successfully designed in a 28 nm node. Grade: 5.5.

Semester thesis: *Turbo Decoder Implementation for Evolved EDGE*. Group-project for a stand-alone turbo decoder ASIC for EEDGE. Chip was manufactured with UMC 0.18 µm node and successfully tested. See C. Benkeser et al., “*Turbo decoder design for high code rates*”, 2012. Grade: 5.25.

**BSc ETH** in Electrical Engineering and Information Technology 2006-09 – 2011-08  
ETH Zürich, Major: Micro- and Optoelectronics, grade average: 4.57.  
Erasmus exchange year at Lund University (LTH), 2008/2009.

**Coursework** iDesign Architect's (2018) and Project Design Master Class (2020), DDC (2023)  
Black Box Testing Software Testing Foundations (2024)  
Systems Architecting, SE Training (2023)

---

**Technology & Tooling** Languages  
VHDL, Python including pytest, poetry  
C/C++, PSL, Bash  
Web-Stacks Astro, HTML/JS, MySQL  
SystemVerilog, SystemC/HLS, P-org *first contact*  
German, Swedish *native*, English *highly proficient*

Tools  
Codebeamer ALM, Docker, git  
Systems (Ubuntu, CentOS), various build tools (Jenkins, github, SCons, ...)

---

**References** On demand.