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VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(AUTONOMOUS)

B.Tech. II Year II Semester Regular Examinations, July 2024

COMPUTER ORGANIZATION

(Common to CSE, IT and CSE-CyS)

Time: 3 hours **Max. Marks: 60**

Answer ALL questions in PART-A.
Answer any ONE question from each unit in PART-B.

PART-A

5X2=10M

a)	How data is transferred between registers? Discuss with an example.	2M	CO-1	BL-1
b)	What are instruction formats and why are they critical in CPU design?	2M	CO-2	BL-2
c)	How does the placement of the binary point affect the precision and range of fixed point numbers?	2M	CO-3	BL-1
d)	What are the different types of I/O interfaces and their characteristics?	2M	CO-4	BL-2
e)	What is a RISC pipeline?	2M	CO-5	BL-1

PART-B

5X10=50M

UNIT-I

1.	a)	Explain the applications of various logic micro operations using below registers. A=101101, B=110010.	5M	CO-1	BL-2
	b)	Explain instruction cycle with the help of flow chart?	5M	CO-1	BL-3
		OR			
2.	a)	Differentiate between logical, arithmetic, and circular shifts.	4 M	CO-1	BL-2
	b)	Explain the significance of multiplexers in the design of an Arithmetic Logic & Shift Unit.	6 M	CO-1	BL-3

UNIT-II

3.	a)	Explain the role of the control address register (CAR) and control buffer register (CBR) in address sequencing.	4M	CO-2	BL-2
	b)	Discuss various addressing modes with examples.	6M	CO-2	BL-2
		OR			
4.	a)	Describe the challenges involved in designing an efficient control unit and how they can be addressed.	7M	CO-2	BL-2
	b)	Provide examples of data manipulation instructions with mnemonics.	3M	CO-2	BL-2

UNIT-III

5.	a)	How do you represent fixed point numbers? Explain with example.	4M	CO-3	BL-2
	b)	Describe the steps involved in multiplication of below numbers -13 X -15. Draw the flow chart.	6M	CO-3	BL-3
		OR			
6.		Explain the non-restoring division algorithm for the example 10/3? How it differs from the restoring method. Describe a situation where restoring division might be preferred over non-restoring division.	10M	CO- 3	BL-3

UNIT-IV

7.	a)	Define cache memory ? Explain various mapping techniques of cache memory with relevant diagrams.	7M	CO-4	BL-2
	b)	How does the operating system enforce the distinction between privileged and non-privileged instructions?	3M	CO-4	BL-2
		OR			
8.	a)	Explain Direct Memory Access (DMA) with relevant diagrams.	7M	CO-4	BL-3
	b)	Provide examples of scenarios where asynchronous data transfer is preferred.	3M	CO-4	BL-2

UNIT-V

9.	a)	How do branch prediction and speculative execution enhance the performance of an instruction pipeline?	5M	CO-5	BL-3
	b)	Discuss various types of array processors in handling large-scale computations.	5M	CO-5	BL-2
		OR			
10.	a)	Describe the stages involved in an arithmetic pipeline for floating-point operations.	5M	CO-5	BL-2
	b)	Discuss Flynn's classification of parallel computer architectures.	5M	CO-5	BL-3

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