Subject Code
22PC1CS203

R22

**VNR VIGNANA JYOTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY**
**(AUTONOMOUS)**
**B.Tech. II Year II Semester Sessional Examination-II, July 2024**
**Computer Organization**
(Common to CSE, IT, CyS)

**Time: 2 Hours** **DoE: 04-07-2024** **Max. Marks: 30M**

## PART-A

**5X 2M=10 M**

***All Questions are compulsory.***

| | | | |
|---|---|---|---|
| a) | Differentiate Privileged instructions from non-privileged instructions. | CO-4 | BL-2 |
| b) | Give the logic between Non-Restoring Division method. | CO-3 | BL-2 |
| c) | State the write policies. | CO-4 | BL-2 |
| d) | Define pipelining. | CO-5 | BL-1 |
| e) | Draw Memory Hierarchy. | CO-4 | BL-2 |

## PART-B

***Answer any ONE question from each Unit***

**2X8=16M**
**1X4=4M**

### UNIT-III

| | | | | |
|---|---|---|---|---|
| 1. | Multiply 10111 with 10011 with Booth's algorithm. Show all the registers content for each step. | 4M | CO-3 | BL-3 |
| | OR | | | |
| 2. | Write an algorithm to multiply binary numbers represented in normalized floating-point mode. | 4M | CO-3 | BL-3 |

### UNIT-IV

| | | | | |
|---|---|---|---|---|
| 3. | Analyse the operation of DMA controller with block diagram. | 8M | CO-4 | BL-4 |
| | OR | | | |
| 4. | What are the different types of mapping techniques used in the usage of cache memory? Explain. | 8M | CO-4 | BL-2 |

### UNIT-V

| | | | | |
|---|---|---|---|---|
| 5. | Explain pipeline for floating point addition and subtraction. | 8M | CO-5 | BL-2 |
| | OR | | | |
| 6. | Examine the Flynn's Classification in detail. | 8M | CO-5 | BL-4 |

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