Module 5

Carrier Modulation

Lesson 32

Timing Synchronization

After reading this lesson, you will learn about:

- ***Bit Error Rate (BER) calculation for BPSK;***
- ***Error Performance of coherent QPSK;***
- ***Approx BER for QPSK;***
- ***Performance Requirements;***

All digital communication systems require various timing control measures for specific purposes. For example, timing information is needed to identify the rate at which bits are transmitted. It is also needed to identify the start and end instants of an information-bearing symbol or a sequence of symbols. Note that all the demodulation schemes that we have discussed are based on the principle of symbol-by-symbol detection scheme and we assumed that precise symbol-timing information is always available at the receiver.

Further, information, when available in binary digits, is often treated in groups called blocks. A block is a small segment of data that is treated together for the purpose of transmission and reception. Each block is added with time stamps marking the beginning and end of the block and these time stamps should also be recovered properly at the receiving end to ensure proper sequence of blocks at the user end. In the context of radio transmission and reception, such as for communication through a satellite or in wireless LAN, a block of binary digits called 'frame', along with necessary overhead bits, needs synchronization.

For reliable data communication at moderate and high rates, timing information about the transmitter clock is obtained in the receiver directly or indirectly from the received signal. Such a transmission mode is known as synchronous. In this lesson, we will discuss about synchronous mode of digital transmission, primarily applicable for wireless communications. Though an additional channel may be used in a communication system to transmit the timing information, it is wastage of bandwidth. For baseband transmission schemes, it is a popular practice to insert the timing signal within the transmitted data stream by use of suitable line encoding technique.

A straight forward approach to insert the timing signal in a binary data stream is to encode the binary signal in some way to ensure a high-low (or low-high) transition with each bit. Such a transition in each bit can be used easily to recover the time reference (e.g. the clock) at the receiver.

Non-Return to Zero (NRZ) Encoding

In this encoding scheme, logic '1' is sent as a high value and logic '0' is sent as a low value (or vice versa). This is simple but not an elegant technique. A long run of '0' or '1' will have no transition for a fairly long duration of time and this may cause drift in the timing recovery circuit at the receiver.

Return to Zero (RZ) Encoding:

This is a three level encoding scheme where logic '1' is encoded as a high positive value for a portion (typically 50 %) of the bit duration while nothing is transmitted over the remaining duration. Similarly, logic '0' is encoded as a negative value for a portion (typically 50 %) of the bit duration while nothing is transmitted over the remaining duration. So, a long run of '1' or '0' will have level transitions.

Manchester Encoding:

In Manchester encoding the actual binary data to be transmitted are not sent as a sequence of logic 1's and 0's. The bits are translated into a different format which offers several advantages over NRZ coding. A logic '0' is indicated by a transition from '0' to '1' at the middle of the duration of the bit while logic '1' is indicated by a transition from '1' to '0' at the middle of the duration of the bit. So, there is always a transition at the centre of each bit. The Manchester code is also known as a Biphase Code as a bit is encoded by $\pm$ 90^0 phase transition. As a Manchester coded signal has frequent level transitions, the receiver can comfortably extract the clock signal using a phase locked loop. However, a Manchester coded signal needs more bandwidth than the NRZ coded signal. Thus this line coding scheme finds more use in optical fiber communications systems where additional bandwidth is available.

Symbol Synchronization

We will now discuss about time synchronization techniques, specifically necessary for demodulating narrowband carrier modulated signals. Such techniques are also known as 'symbol synchronization' techniques.

Let us recollect from our discussion on matched filtering that if a signal pulse s(t), $0 \leq t \leq T$, is passed through a filter, matched to it, the output of the filter is maximum at $t = T$.

Example 5.32.1: Consider a rectangular pulse s(t) as shown in **Fig. 5.32.1(a).** The corresponding matched filter output is sketched in **Fig. 5.32.1(b).** It may be observed that, if we sample the filter output early, i.e., at $t = T - \delta$ or late, at $t = T + \delta$, the sampled values are not maximum. In presence of noise (AWGN), it implies that the average sampled value may result in wrong symbol decision. A symbol synchronization scheme attempts to ensure that even in presence of noise, the time offset 'δ' is acceptably small.

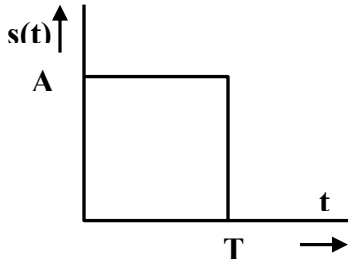

Fig. 5.32.1(a): *A rectangular pulse s(t) of duration T*

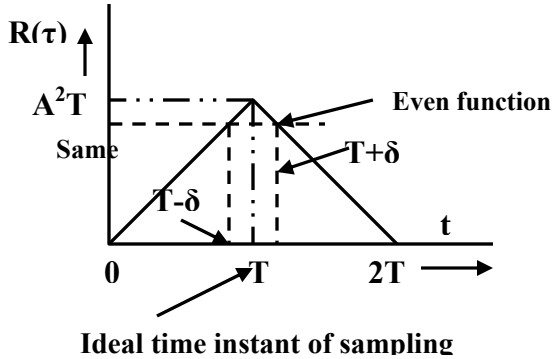

Fig. 5.32.1(b): *Autocorrelation of a rectangular pulse s(t)*

Now, note that the auto correlation function R (τ) is an even function & its values for t = T ± δ are the same. So, the aim of a symbol synchronization scheme is to ensure small 'δ' first and then declare the ideal time instant of sampling as the mid-point of 'T-δ' and 'T+ δ'. This is also the basic approach of a symbol synchronizer popularly known as *'Early-Late gate Synchronizer'* **[Fig. 5.32.2(a)]**. The received IF signal is multiplied by the recovered carrier $\cos(\omega_c t + \hat{\varphi})$ and the resultant signal is treated in two parallel paths. In the upper branch, the signal is correlated with a little advanced version of the expected ideal symbol pulse while it is correlated with a little delayed version of the symbol pulse. Outputs of the two correlators are then sampled at the same time instant which gets corrected depending on the difference of the two squaring circuit outputs. If the present time instant of sampling is very close to the ideal sampling instant, the two squaring circuits, following the two correlators, produce very similar outputs and hence the low frequency component at the output of the difference unit is almost zero. The VCO in this situation is locked to the desired clock frequency with correct phase. So, In essence, the VCO output is the desired symbol clock which can be used for the purpose of demodulation. Another way of implementing the same concept of early-late-gate synchronizer, which is sometimes easier for practical implementation, is shown in **Fig. 5.32.2(b)**.

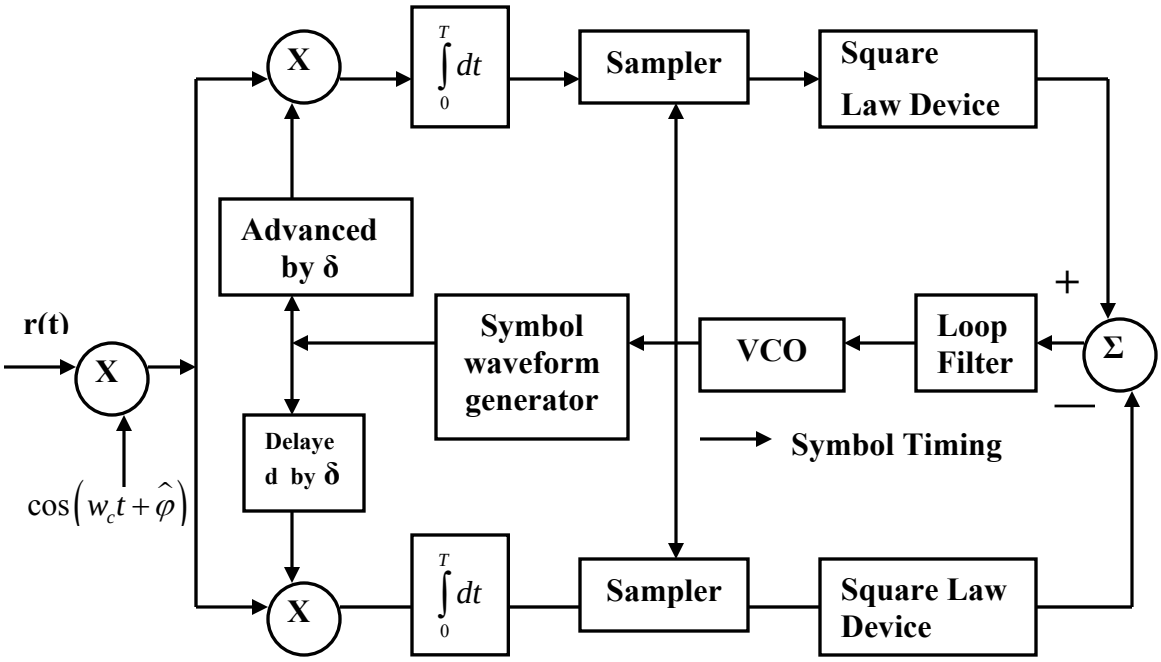

Fig. 5.32.2 (a): *Schematic diagram of an Early-Late-Gate synchronizer*

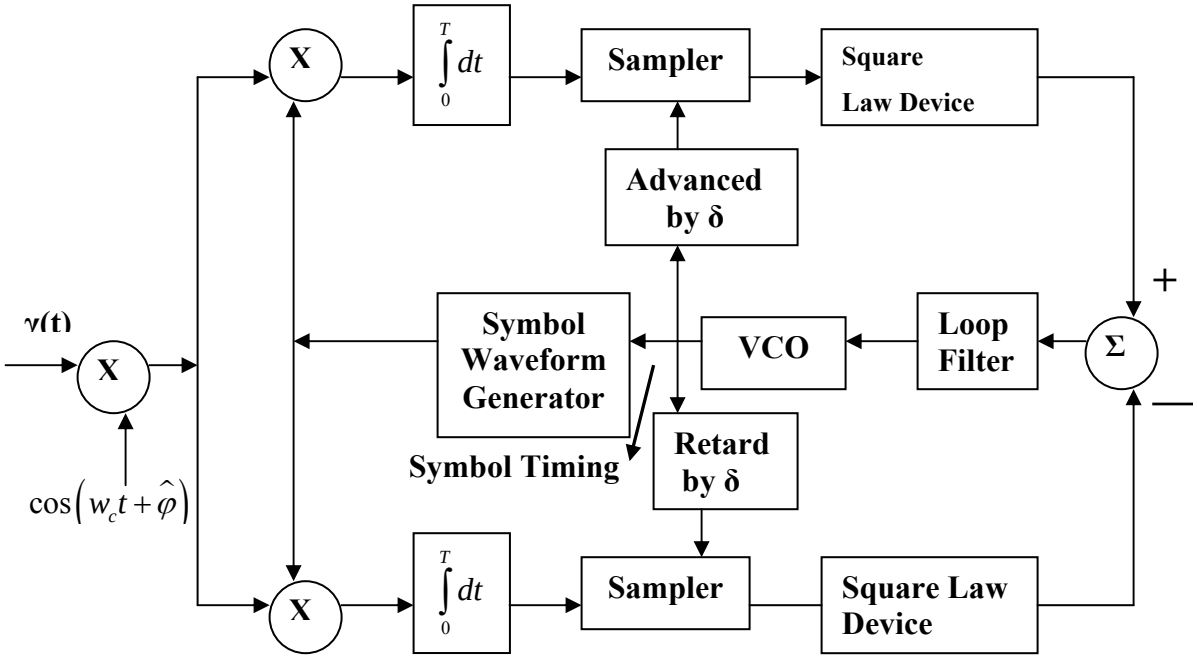

Fig. 5.32.2 (b): *An alternative scheme for Early-Late-Gate synchronizer*