

CS2011 Foundations of Computing Systems, Test 1

September 11, 2025

Q1: For an n sized bit vector $\mathbf{x} = (x_1, x_2, \dots, x_n)$, the parity is defined to be 1 if and only if there are odd number of x_i 's that are 1's.

- (a) (5 points) Give the truth table for the parity of 3 bits.
- (b) (5 points) Give the OR of ANDs representation of the 3-bit parity function.
- (c) (5 points) In data storage (or transmission), one often *encodes* the data \mathbf{x} by padding an *additional parity bit* before storage (or transmission). In the HDL that you learned in the course develop the chip **ENCODE**, that takes as input a bit vector of length 3 and gives out a bit vector of length 4 where the first 3-bits are the data bits and the last bit is the parity. You may use the builtin XOR chip for this chip.

Q2: (5 points) Using a 16-bit adder circuit and a 16-bit register as a basic block, give a *sequential circuit* **SUM** that keeps the running sum of a stream of 4-bit input data data . The output of the chip is the sum of all the input it has seen so far. You should describe the **SUM** chip using the HDL that we did in the class.