EE214 - Digital Circuits Lab

Logic Function Design using NAND gate

Thrusday Batch

04/08/2022

Instructions:

1. NAND is a universal gate.
2. For writing VHDL description use the NAND gate provided in Gates.vhdl .
3. For the design part do pen-paper design and get it verified by your TA.
4. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
5. Perform RTL simulation using the provided testbench and tracefile.
6. Demonstrate the simulations and RTL view to your TA.

Problem Statement

1. Design XOR gate using NAND gate. [3 Marks]
2. Describe XOR gate using NAND gate in VHDL using Structural modeling. [5 Marks]
3. Design Full Adder using NAND gate. [3 Marks]
4. Describe Full Adder using NAND gate in VHDL using Structural modeling. [5 Marks]
5. Verify working of your design by performing RTL simulation. Show the results of XOR [2 Marks] and Full Adder[2 Marks] to your TA.
6. Simulate the above designs in Modelsim and validate its functionality using the given Tracefile.
   NOTE: TRACEFILE format for XOR gate
   Input{X1 X0} Output{Y0} MASK{1}

   TRACEFILE format for Full Adder
   Input{X2 X1 X0} Output{Sum Carry} MASK{1 1}

   Click on XOR to get the tracefile of XOR gate.

   Click on Full Adder to get the tracefile of Full Adder.