EE214 - Digital Circuits Lab

Logic Function Design using NAND gate

Friday Batch

05/08/2022

Instructions:

1. NAND is a universal gate.
2. For writing VHDL description use the NAND gate provided in Gates.vhdl .
3. For the design part do pen-paper design and get it verified by your TA.
4. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
5. Perform RTL simulation using the provided testbench and tracefile.
6. Demonstrate the simulations and RTL view to your TA.

Problem Statement

1. Design XNOR gate using NAND gate. [3 Marks]
2. Describe XNOR gate using NAND gate in VHDL using Structural modeling. [5 Marks]
3. Design Full Subtractor using NAND gate. [3 Marks]
4. Describe Full Subtractor using NAND gate in VHDL using Structural modeling. [5 Marks]
5. Verify working of your design by performing RTL simulation. Show the results of XNOR [2 Marks] and Full Subtractor[2 Marks] to your TA.
6. Simulate the above designs in Modelsim and validate its functionality using the given Tracefile.
   NOTE: TRACEFILE format for XNOR gate
   Input{X1 X0} Output{Y0} MASK{1}

   TRACEFILE format for Full Subtractor
   Input{A B Borrow_in} Output{Diff Borrow} MASK{1 1}

   Click on XNOR to get the tracefile of XNOR gate.

   Click on Full Subtractor to get the tracefile of Full Subtractor.