EE214 - Digital Circuits Lab

Prime Detector
Thursday Batch

18/08/2022

Instructions

1. Use structural modelling for this experiment i.e. instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.
5. Demonstrate the experiment to your TA.
6. Submit the entire project files in .zip format in Moodle.

Design [5 Marks]

Design a system that detects a prime number. Any number between 0 to 15 will be given as input to the system which will be represented in binary form such as $0 \rightarrow 0000$, $1 \rightarrow 0001$ and so on. The output of the system will be '1' only when the given input is a prime number. Show the pen-paper design using K-Maps to the corresponding evaluating TAs.

VHDL Description [5 Marks]

Write a VHDL description for the given problem statement.

Inputs(4-bit): $x_3x_2x_1x_0$
Output(1-bit): y
Tracefile format: $< x_3x_2x_1x_0 >$ $< y >$ 1

Design Verification [10 Marks]

- Perform RTL Level Simulation of the prime detector using the generic testbench to confirm the correctness of your description using the TRACEFILE [5 Marks]
- Pin plan switches S4 to S1 as input and LED 8 as output and show the correctness of the design on board. [5 Marks]

NOTE: Once you finish this experiment, perform the previous lab experiments on board.