EE214 - Digital Circuits Lab

Multiplier

Thursday Batch

01/09/2022

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the given testbench and tracefile.
5. Perform scan-chain evaluation on board using the given tracefile.
6. Demonstrate the RTL simulations and board scanchain output to your TA
7. Submit the entire project files in .zip format in Moodle.

Problem Statement:

1. **Design** [5 Marks]

   Design a multiplier circuit with one 4-bit input and one 3-bit input.

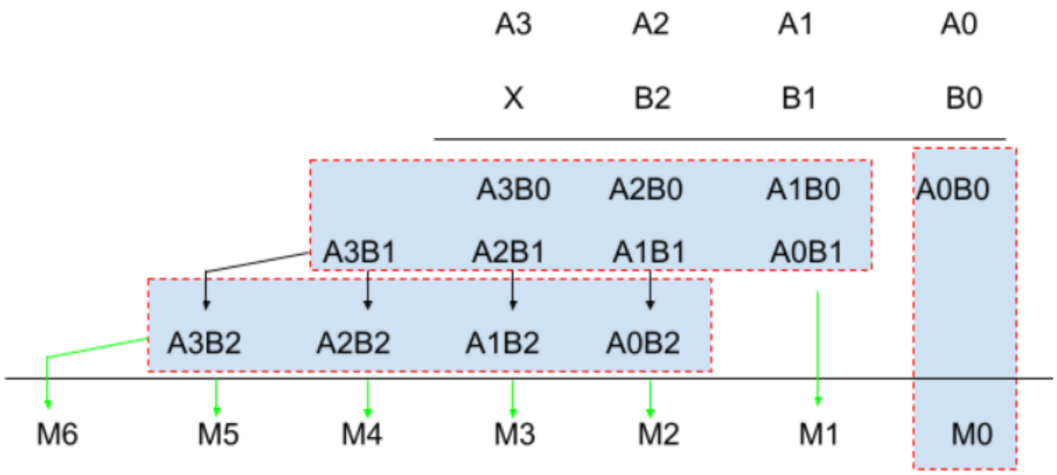

Figure 1: Block diagram

2. **VHDL description** [5 Marks]

   Describe your designed circuit in VHDL.

3. **Simulation** [5 Marks]
   Simulate your design using the generic testbench to confirm the correctness of your description.
   To do this, use the tracefile given below and modify the testbench given to you appropriately.

   Tracefile format: ($< A3\ A2\ A1\ A0\ B2\ B1\ B0 >\ \ < M6\ M5\ M4\ M3\ M2\ M1\ M0 >\ \ 1111111$) Tracefile

4. **Scanchain** [5 Marks]
   Test the correctness of your design using scanchain