EE214 - Digital Circuits Lab

Demux

Friday Batch

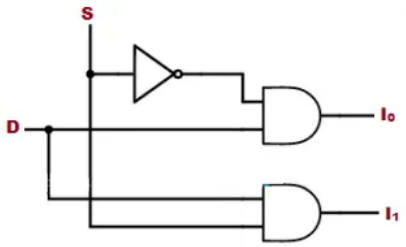
12/08/2022

Instructions:

1. Use structural modelling for this experiment; means instantiate components and use port map to connect those components.
2. For the design part do pen-paper design and get it verified by your TA.
3. In pen paper design use proper labeling for each wire. And use same labels for the VHDL code.
4. Perform RTL simulation using the provided testbench and tracefile.
5. Demonstrate the simulations to your TA.
6. Submit the entire project files in .zip format in Moodle.

Problem Statement:

1. **Part-A: 1x2 Demux**
   (a) VHDL description: Write the VHDL description of a 1x2 demultiplexer as shown in figure below. The unselected line should output '0'. [5 Marks]
   INFO: Demultiplexer is a combinational circuit that has single input line, maximum of 2^n output lines and 'n' selection lines.



   (b) Write Truth table and boolean expression for output Y. [3 Marks]

   (c) Simulation: Simulate the 1x2 demultiplexer using the generic testbench to confirm the correctness of your description. [5 Marks]
   NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.
   Tracefile format: ($< S\ D >\ \ < Y1\ Y0 >\ \ 1\ 1$) Tracefile

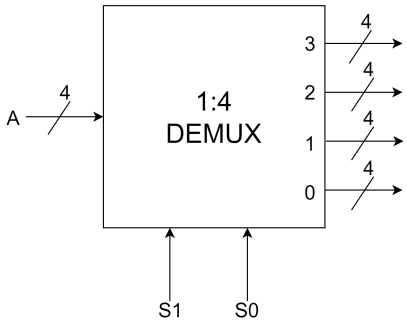
2. **Part-B: 1X4 Demux**
   (a) Design: Design 1x4 Demux using only 1x2 Demux. [3 Marks]
   INFO: $2^2 = 4$ outputs, 2 select lines, 1 data input line

   (b) VHDL description: Write the VHDL description of a 1x4 demultiplexer designed using 1x2 demultiplexer. The unselected lines should output '0'. [5 Marks]

   (c) Simulation: Simulate the 1x4 demultiplexer using the generic testbench to confirm the correctness of your description. [3 Marks]
   NOTE: To do this, use the given tracefile and modify the testbench given to you appropriately.
   Tracefile format: ($< S2\ S1\ In0 >\ \ < Y3\ Y2\ Y1\ Y0 >\ \ < 1\ 1\ 1\ 1 >$) Tracefile

3. **Part-C: 4-bit 1x4 Demux**

(a) Design: Design 4-bit wide 1x4 demux using only 1x4 demux designed in part B. [3 Marks]



(b) VHDL description: Write the VHDL description of a 4-bit wide 1x4 demux, designed using 1bit 1x4 demux. The unselected lines should output '0'. [5 Marks]

(c) Simulation: Simulate the 4-bit 1x4 demultiplexer using the generic testbench to confirm the correctness of your description. [5 Marks]
NOTE: To do this, use the tracefile given below and modify the testbench given to you appropriately.
Tracefile format:
(A3 A2 A1 A0 S1 S0) (Y15 Y14 Y13 Y12 Y11 Y10 Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0) (1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1)
Tracefile