How to connect an Ethernet PHY to SAM3X

AT91SAM
ARM-based
Flash MCU

Application Note

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1. SAM3X, MII and RMII

The Atmel® SAM3X ARM® Cortex™-M3 Flash-based microcontroller integrates an EMAC module to implement a 10/100 Ethernet MAC compatible with the IEEE 802.3 standard. It can connect to an external Physical layer transceiver (Ethernet PHY) by Media Independent Interface (MII) or Reduced Media Independent Interface (RMII). Due to different packages, some devices support both MII and RMII interface, other supports only RMII interface.

1.1 MII vs. RMII

- IO

Table 1-1. SAM3X pins configuration for MII and RMII interface

SAM3X Pin Name	PHY MII	PHY RMII
ETXCK_EREFCK	ETXCK: Transmit Clock	EREFCK: Reference Clock
ECRS	ECRS: Carrier Sense	
ECOL	ECOL: Collision Detect	
ERXDV	ERXDV: Data Valid	ECRSDV: Carrier Sense/Data Valid
ERX0 – ERX3	ERX0 – ERX3: 4-bit Receive Data	ERX0 – ERX1: 2-bit Receive Data
ERXER	ERXER: Receive Error	ERXER: Receive Error
ERXCK	ERXCK: Receive Clock	
ETXEN	ETXEN: Transmit Enable	ETXEN: Transmit Enable
ETX0 – ETX3	ETX0 – ETX3: 4-bit Transmit Data	ETX0 – ETX1: 2-bit Transmit Data
ETXER	ETXER: Transmit Error	

As shown in Table 1-1 RMII reduces the number of pins used to connect to an external PHY. Choosing RMII will save several pins, ease the PCB routing and leave IOs for other purposes.

- EMI

Generally, MII frequency is 25 MHz and RMII is 50 MHz. So, when EMI is a critical aspect of a system, opting for the MII interface instead of RMII is likely to be the best choice.

- Cost

The difference between costs for choosing MII or RMII mainly depends on the PHY chip and the crystal/oscillator needed. Normally, a MII PHY is more expensive than a RMII PHY. A 50MHz oscillator needed by RMII cost more than a 25MHz crystal needed by MII.

2. Supported PHY list and Code

Market is always evolving and there are a lot of manufacturers providing their own PHY products. Table 2-1 lists some products for your reference. You can contact your supplier for more options.

Table 2-1. Devices for reference

Manufacturers	Website link	RMII	MII
Broadcom Corporation	http://www.broadcom.com/products/Physical-Layer/Fast-Ethernet-PHYs	BCM5221	BCM5241
Davicom Semiconductor Inc.	http://www.davicom.com.tw/page1.aspx?no=143760	DM9161	DM9161
Micrel Semiconductor	http://www.micrel.com/page.do?page=product-info/fastether_trans.jsp	KSZ8001,KSZ8051MNL	KSZ8001,KSZ8051RNL
Realtek Semiconductor Corp.	http://www.realtek.com.tw/products/productsView.aspx?Langid=1&PNid=17&PFid=13&Level=5&Conn=4	RTL8201F/FN/FL	RTL8201F/FN/FL

Due to standardization, the connection between a MAC controller and a PHY is straightforward and simple. Even, any PHY can work with any MAC.

Currently, SAM3X-EK is using a PHY DM9161 from DAVICOM. Atmel Corporation provides a Software Package for SAM3X on its website. In this Software Package, there is a basic project (support for IAR EWARM, KEIL and GNU GCC tool chain) to show how to initialize MAC and PHY.

3. PHY Initialization

3.1 Default operation mode

For a PHY chip, its default operation mode is determined by its pins state during power on/reset as well as its default resistor values. The pins definition of PHY may differ among different manufacturers. It is suggested for hardware designers to guarantee the PHY chip is in a known state after power on/reset. Including:

- PHY address (0b00000~0b11111): Most PHY support a unique address from 0b00001 to 0b11111, and broadcast address 0b00000. It means a PHY will responds to two addresses. If there are two or more PHY devices connected on the same management interface, their unique address must be different. Normally, the unique address is latched into and stored at PHY register depending on some pins input during power on/reset. Normally during power on/reset the unique address is latched and stored in a PHY register, this functionallty depends on the state of some pins during the power on/reset.

- RESET pin: hardware designers must pay attention to this pin because special reset timing may be required to reset the PHY device. For example, the reset pulse can not be too narrow.

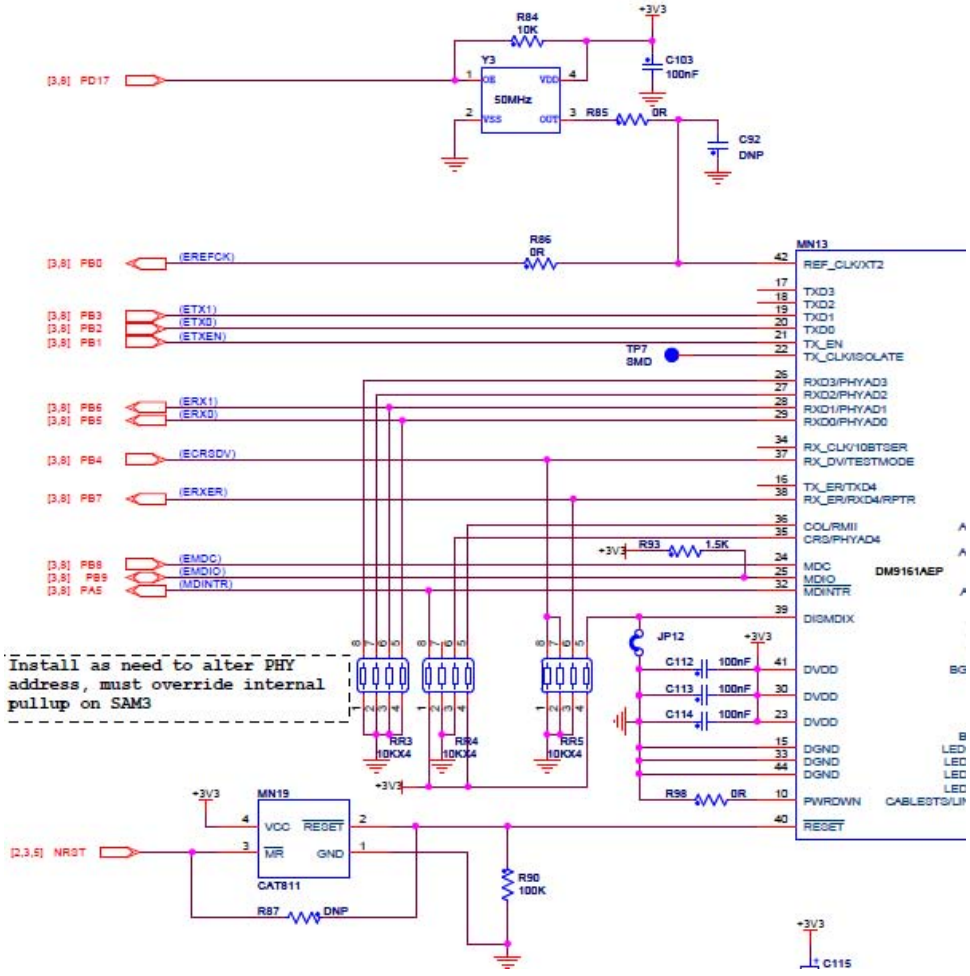
- Other pins: the input state on other pins of a PHY may configure more options. For example, MDI/MDIX (Ethernet cable connection type, straight through/cross over), DUPLEX mode (Half/Full), Speed mode (10/100Mbps), LEDs mode (to indicate link activity status, speed or other status) and so on.

By setting up a default operation mode with proper hardware consideration, the PHY device will go to this mode directly and no software initialization is needed. Software developers just needs to read and check the status of the PHY device, afterwards higher level functions at MAC side can be initialized.

3.2 PHY connection on SAM3X-EK

The connection between SAM3X and DM9161 on SAM3X-EK is shown in Figure 3-1. The DM9161 was set in RMII mode with a 50MHZ crystal oscillator.

Figure 3-1. Connection for Reference



- PHY address driven to 0b00000

PHYAD[4:0] of DM9161 have internal pull-down(50~100 kΩ) while SAM3X I/Os, which are input by default, are designed with embedded pull-up resistor(50~100 kΩ). It is difficult to say which are stronger, pull-downs or pull-ups. Because of the latter, external pull-downs (e.g. 10K) are used between DM9161 and SAM3X on PHYAD[4:0] to guarantee the PHY address is driven to 0b00000 (unique PHY address is the same with broadcast address).

Note that the unique PHY address can be driven to any values from 0b00001 to 0b11111.

- RESET

SAM3X NRST negative pulse during power on is too narrow to reset the PHY correctly. Using a power supply supervisor, CAT811, the negative pulse was expanded from about 60us to longer than 10ms.

- Other pins

RX_ER/TESTMODE: external pull-down to guarantee the PHY in normal mode.

COL/RMII: external pull-up to guarantee the PHY in RMII mode.

DISMDIX: use a Jumper to enable/disable auto MDI/MDIX mode.

3.3 Software solution

To reduce cost and simplify PCB layout, the external pull-ups/downs between SAM3X, the PHY device and the special reset circuit can be omitted.

For example, on SAM3X-EK, the pull-downs on PHYAD[4:0] can be omitted and the RESET pin of DM9161 can then connect to NRST of SAM3X directly. By doing this, the PHY may go into an unwanted mode and the address of PHY is unknown. To solve these problems, a warm reset and auto negotiation routine is needed after power-on in application software.

- Set SAM3X IOs which are connected to PHY address lines, PHYAD[4:0], to output and drive them to 0 or 1 to config PHY address.
- Thanks to the SAM3X Reset Controller, a negative pulse on NRST can be generated and its length is adjustable to reset external devices, e.g. PHY.
- After reset, switch SAM3X IOs back to MII/RMII use.

4. Links and OS

After PHY initialization as described in the previous chapter, the next step for designers is to implement MAC initialization and network protocols. Here are some website resources for reference:

uIP and lwIP are two popular TCP/IP stack for embedded design.

uIP is a small TCP/IP stack ; lwIP is a light-weight implementation of the TCP/IP protocol

Both can be found on Adam Dunkel's homepage: http://www.sics.se/~adam/

There are some example projects, supporting IAR workbench, ARM MDK and GCC toolchain, in the SAM3X software package on ATMEL website.

Both uIP and lwIP have been ported to ATMEL products on FreeRTOS: http://www.freertos.org/

SAM3X-EK BeRTOS HTTP Demo.

This demo is based on the Open Source RTOS named BeRTOS. This RTOS provides micro kernel and software layers (drivers, services) which make it easier the kick off of any new development.

See SAM3X-EK Page: http://www.atmel.com/tools/SAM3X-EK.aspx

Revision History

Doc. Rev	Date	Comments	Change Request Ref.
11153A	25-Jun-12	First issue	

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