KPK 8 BIT PROGRAMMABLE COMPUTER INSTRUCTION SET ARCHITECTURE (ADD/SUB)					
Operation	**Memory Address**	**Decimal Value**	**CPU Op.Code/ Memory Address/ Value (Binary)**		**Decimal Value**
INSTRUCTIONS			**CPU Op.Code**	**Memory Address/ Value**	
LOAD-A	0000	0	0001	1011	NA
LOAD-B & ADD (X+Y)	0001	1	0010	1100	NA
LOAD-B & SUB (X-Z)	0010	2	0011	1101	NA
		…			
VARIABLES		…			
X	1011	11	0101	0000	80
Y	1100	12	0001	0100	20
Z	1101	13	0001	1110	30

CLOCK	**LOAD-A**	**LOAD-B & ADD (X+Y)**	**LOAD-B & SUB (X-Z)**
CLK-1	CO-E, CO-O, MA-I RST	CO-E, CO-O, MA-I RST	CO-E, CO-O, MA-I RST
CLK-2	RM-O, IR-I RST	RM-O, IR-I RST	RM-O, IR-I RST
CLK-3	IR-O, MA-I RST	IR-O, MA-I RST	IR-O, MA-I RST
CLK-4	RM-O, R(A)-I RST	RM-O, *R(B)-I* RST	RM-O, R(B)-I RST
CLK-5		*∑-O, DI-I* RST	*SU-E* , ∑-O, DI-I RST