

KPK 8 BIT PROGRAMMABLE COMPUTER INSTRUCTION SET ARCHITECTURE (MULTIPLY - MICROCODE)								
CPU Op.Code	CPU Op.Code	CPU Function		CPU Instruction Set				
				CLK-1	CLK-2	CLK-3	CLK-4	CLK-5
0000	0	No Operation		CO-E, RA-O, IR-I	MA-I, CO-O			
0001	1	LOAD-A		CO-E, RA-O, IR-I	IR-O, MA-I			
0010	2	LOAD-B & ADD		CO-E, RA-O, IR-I	RA-O, IR-I, CO-E	RA-O, R(B)-I	R(A)-I, $\Sigma$ -O, F-I	
0011	3	LOAD-B & SUB		CO-E, RA-O, IR-I	RA-O, IR-I, CO-E	RA-O, R(B)-I	R(A)-I, SU-E, $\Sigma$ -O, F-I	
0100	4	STORE-A		CO-E, RA-O, IR-I	RA-I, R(A)-O			
0101	5	LOAD IMMEDIATE		CO-E, RA-O, IR-I	IR-O, R(A)-I			
0110	6	JUMP		CO-E, RA-O, IR-I	IR-O, J-E	RA-O, IR-I, CO-E		
0111	7	JUMP-CARRY		CO-E, RA-O, IR-I	IR-O, J-E	RA-O, IR-I, CO-E		
1000	8	JUMP-ZERO		CO-E, RA-O, IR-I	IR-O, J-E	RA-O, IR-I, CO-E		
1001	9	-						
1010	10	-						
1011	11	-						
1100	12	-						
1101	13	-						
1110	14	OUTPUT		CO-E, RA-O, IR-I	R(A)-O, OP-I			
1111	15	HALT		CO-E, RA-O, IR-I	CLK-I			

**Legends:**

CO-E : Program Counter ENABLE	RA-I : RAM IN	IR-I : Instruction REG. IN	MA-I : Memory Address REG. IN
CO-O : Program Counter OUT	RA-O : RAM OUT	IR-O : Instruction REG. OUT	MA-O : Memory Address REG. OUT
R(A)-I : Register -A IN	R(B)-I : Register -B IN	J-E : Jump ENABLE	OP-I : Output REG. IN
R(A)-O : Register -A OUT	R(B)-O : Register -B OUT	$\Sigma$ -O : ALU SUM OUT	ZF : Zero Flag
F-I : Flags REG. IN		SU-E : ALU Subtract ENABLE	CF : Clear Flag

PROJECT NAME :	8BIT PROGRAMMABLE COMPUTER	DRAWING :	INSTRUCTION SET ARCHITECTURE (MULTIPLY - MICROCODE)
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