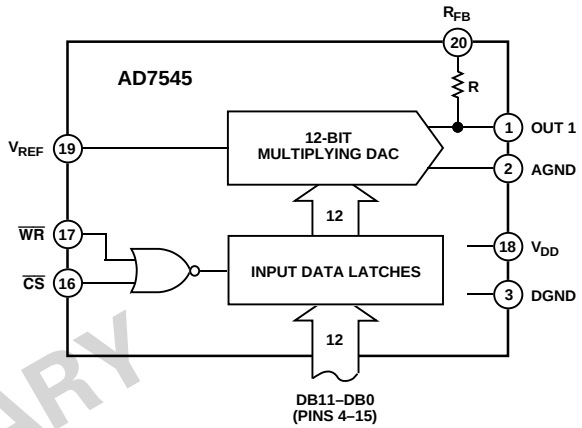
CMOS 12-Bit Buffered Multiplying DAC

AD7545

FEATURES

- 12-Bit Resolution
- Low Gain TC: 2 ppm/°C typ
- Fast TTL Compatible Data Latches
- Single +5 V to +15 V Supply
- Small 20-Lead 0.3" DIP and 20-Terminal Surface Mount Packages
- Latch Free (Schottky Protection Diode Not Required)
- Low Cost
- Ideal for Battery Operated Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

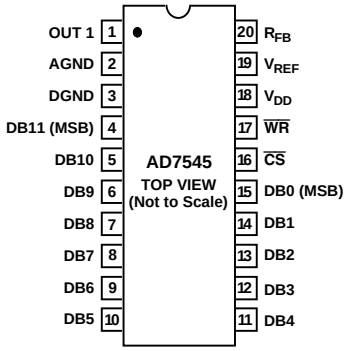
The AD7545 is a monolithic 12-bit CMOS multiplying DAC with onboard data latches. It is loaded by a single 12-bit wide word and directly interfaces to most 12- and 16-bit bus systems. Data is loaded into the input latches under the control of the $\overline{CS}$ and $\overline{WR}$ inputs; tying these control inputs low makes the input latches transparent, allowing direct unbuffered operation of the DAC.

The AD7545 is particularly suitable for single supply operation and applications with wide temperature variations.

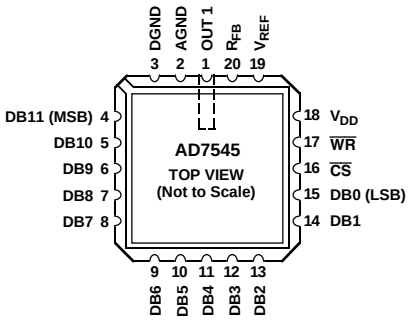
The AD7545 can be used with any supply voltage from +5 V to +15 V. With CMOS logic levels at the inputs the device dissipates less than 0.5 mW for V_{DD} = +5 V.

PIN CONFIGURATIONS

DIP



LCCC



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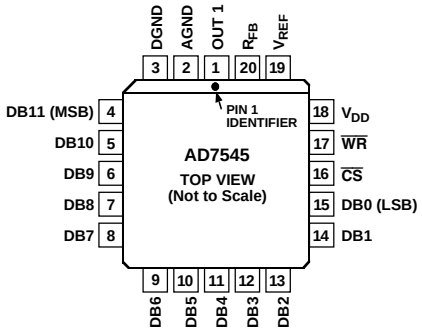


REV. A

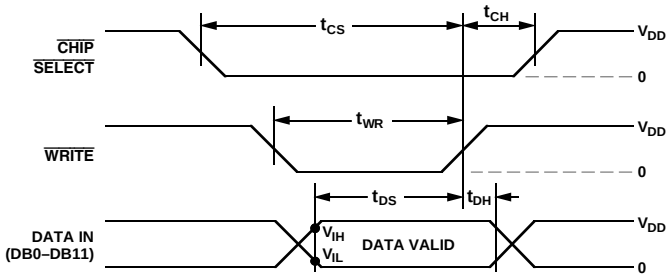
One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 World Wide Web Site: http://www.analog.com
Fax: 617/326-8703

AD7545–SPECIFICATIONS (V_{REF} = +10 V, V_{OUT1} = 0 V, AGND = DGND unless otherwise noted)

Parameter	Version	V_{DD} = +5 V Limits T_A = + 25°C	V_{DD} = +5 V Limits T_{MIN}, T_{MAX}[1]	V_{DD} = +15 V Limits T_A = + 25°C	V_{DD} = +15 V Limits T_{MIN}, T_{MAX}[1]	Units	Test Conditions/Comments
STATIC PERFORMANCE							
Resolution	All	12	12	12	12	Bits	
	J, A, S	±2	±2	±2	±2	LSB max	
	K, B, T	±1	±1	±1	±1	LSB max	
	L, C, U	±1/2	±1/2	±1/2	±1/2	LSB max	
	GL, GC, GU	±1/2	±1/2	±1/2	±1/2	LSB max	
Differential Nonlinearity	J, A, S	±4	±4	±4	±4	LSB max	10-Bit Monotonic T_{MIN} to T_{MAX}
	K, B, T	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{MIN} to T_{MAX}
	L, C, U	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{MIN} to T_{MAX}
	GL, GC, GU	±1	±1	±1	±1	LSB max	12-Bit Monotonic T_{MIN} to T_{MAX}
Gain Error (Using Internal RFB)[2]	J, A, S	±20	±20	±25	±25	LSB max	DAC Register Loaded with
	K, B, T	±10	±10	±15	±15	LSB max	1111 1111 1111
	L, C, U	±5	±6	±10	±10	LSB max	Gain Error Is Adjustable Using
	GL, GC, GU	±1	±2	±6	±7	LSB max	the Circuits of Figures 4, 5, and 6
Gain Temperature Coefficient[3]							
ΔGain/ΔTemperature	All	±5	±5	±10	±10	ppm/°C max	Typical Value is 2 ppm/°C for V_{DD} = +5 V
DC Supply Rejection[3]							
ΔGain/ΔV_{DD}	All	0.015	0.03	0.01	0.02	% per % max	ΔV_{DD} = ±5%
Output Leakage Current at OUT1	J, K, L, GL	10	50	10	50	nA max	DB0–DB11 = 0 V; $\overline{WR}$, $\overline{CS}$ = 0 V
	A, B, C, GC	10	50	10	50	nA max	
	S, T, U, GU	10	200	10	200	nA max	
DYNAMIC PERFORMANCE							
Current Settling Time[3]	All	2	2	2	2	μs max	To 1/2 LSB. OUT1 Load = 100 Ω. DAC Output Measured from Falling Edge of $\overline{WR}$, $\overline{CS}$ = 0.
Propagation Delay[3] (from Digital Input Change to 90% of Final Analog Output)	All	300	–	250	–	ns max	OUT1 Load = 100 Ω, C_{EXT} = 13 pF[4]
Digital-to-Analog Glitch Inpulse	All	400	–	250	–	nV sec typ	V_{REF} = AGND
AC Feedthrough[5]							
At OUT1	All	5	5	5	5	mV p-p typ	V_{REF} = ±10 V, 10 kHz Sinewave
REFERENCE INPUT							
Input Resistance	All	7	7	7	7	kΩ min	Input Resistance TC = –300 ppm/°C typ
(Pin 19 to GND)		25	25	25	25	kΩ max	Typical Input Resistance = 11 kΩ
ANALOG OUTPUT							
Output Capacitance[3]							
C_{OUT1}	All	70	70	70	70	pF max	DB0–DB11 = 0 V, $\overline{WR}$, $\overline{CS}$ = 0 V
C_{OUT1}		200	200	200	200	pF max	DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0 V
DIGITAL INPUTS							
Input High Voltage							
V_{IH}	All	2.4	2.4	13.5	13.5	V min	
Input Low Voltage							
V_{IL}	All	0.8	0.8	1.5	1.5	V max	
Input Current[6]							
I_{IN}	All	±1	±10	±1	±10	μA max	V_{IN} = 0 or V_{DD}
Input Capacitance[3]							
DB0–DB11	All	5	5	5	5	pF max	V_{IN} = 0
$\overline{WR}$, $\overline{CS}$	All	20	20	20	20	pF max	V_{IN} = 0
SWITCHING CHARACTERISTICS[7]							
Chip Select to Write Setup Time	All	280	380	180	200	ns min	See Timing Diagram
t_{CS}		200	270	120	150	ns typ	
Chip Select to Write Hold Time							
t_{CH}	All	0	0	0	0	ns min	
Write Pulse Width							
t_{WR}	All	250	400	160	240	ns min	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$
		175	280	100	170	ns typ	
Data Setup Time	All	140	210	90	120	ns min	
t_{DS}		100	150	60	80	ns typ	
Data Hold Time							
t_{DH}	All	10	10	10	10	ns min	
POWER SUPPLY							
I_{DD}	All	2	2	2	2	mA max	All Digital Inputs V_{IL} or V_{IH}
		100	500	100	500	μA max	All Digital Inputs 0 V to V_{DD}
		10	10	10	10	μA typ	All Digital Inputs 0 V to V_{DD}

NOTES
[1]Temperature range as follows: J, K, L, GL versions, 0°C to +70°C; A, B, C, GC versions, –25°C to +85°C; S, T, U GU versions, –55°C to +125°C.
[2]This includes the effect of 5 ppm max gain TC.
[3]Guaranteed but not tested.
[4]DB0–DB11 = 0 V to V_{DD} or V_{DD} to 0 V.
[5]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (Suffix D) to DGND.
[6]Logic inputs are MOS gates. Typical input current (+25°C) is less than 1 nA.
[7]Sample tested at +25°C to ensure compliance.

Specifications subject to change without notice.



Write Cycle Timing Diagram

MODE SELECTION

WRITE MODE:	HOLD MODE:
$\overline{CS}$ AND $\overline{WR}$ LOW, DAC RESPONDS TO DATA BUS (DB0–DB11) INPUTS.	EITHER $\overline{CS}$ OR $\overline{WR}$ HIGH, DATA BUS (DB0–DB11) IS LOCKED OUT; DAC HOLDS LAST DATA PRESENT WHEN $\overline{WR}$ OR $\overline{CS}$ ASSUMED HIGH STATE.

NOTES:
V_{DD} = +5V; $t_r = t_f$ = 20ns
V_{DD} = +15V; $t_r = t_f$ = 40ns
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}.
TIMING MEASUREMENT REFERENCE LEVEL IS $V_{IH} + V_{IL}/2$.

ABSOLUTE MAXIMUM RATINGS*

(T_A = + 25°C unless otherwise noted)

V_{DD} to DGND ..... –0.3, +17 V
Digital Input Voltage to DGND ..... –0.3 V, V_{DD} +0.3 V
V_{RFB}, V_{REF} to DGND ..... ±25 V
V_{PIN1} to DGND ..... –0.3 V, V_{DD} +0.3 V
AGND to DGND ..... –0.3 V, V_{DD} + 0.3 V
Power Dissipation (Any Package) to +75°C ..... 450 mW
Derates above +75°C ..... 6 mW/°C
Operating Temperature
Commercial (J, K, L, GL) Grades ..... 0°C to +70°C
Industrial (A, B, C, GC) Grades ..... –25°C to +85°C
Extended (S, T, U, GU) Grades ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 secs) ..... +300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7545 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

RELATIVE ACCURACY

The amount by which the D/A converter transfer function differs from the ideal transfer function after the zero and full-scale points have been adjusted. This is an endpoint linearity measurement.

DIFFERENTIAL NONLINEARITY

The difference between the measured change and the ideal change between any two adjacent codes. If a device has a differential nonlinearity of less than 1 LSB it will be monotonic, i.e., the output will always increase for an increase in digital code applied to the D/A converter.

PROPAGATION DELAY

This is a measure of the internal delay of the circuit and is measured from the time a digital input changes to the point at which the analog output at OUT1 reaches 90% of its final value.

DIGITAL-TO-ANALOG GLITCH IMPULSE

This is a measure of the amount of charge injected from the digital inputs to the analog outputs when the inputs change state. It is usually specified as the area of the glitch in nV secs and is measured with V_{REF} = AGND and an ADLH0032CG as the output op amp, C1 (phase compensation) = 33 pF.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Relative Accuracy	Maximum Gain Error T_A = +25°C V_{DD} = +5 V	Package Options[3]
AD7545JN	0°C to +70°C	±2 LSB	±20 LSB	N-20
AD7545AQ	–25°C to +85°C	±2 LSB	±20 LSB	Q-20
AD7545SQ	–55°C to +125°C	±2 LSB	±20 LSB	Q-20
AD7545KN	0°C to +70°C	±1 LSB	±10 LSB	N-20
AD7545BQ	–25°C to +85°C	±1 LSB	±10 LSB	Q-20
AD7545TQ	–55°C to +125°C	±1 LSB	±10 LSB	Q-20
AD7545LN	0°C to +70°C	±1/2 LSB	±5 LSB	N-20
AD7545CQ	–25°C to +85°C	±1/2 LSB	±5 LSB	Q-20
AD7545UQ	–55°C to +125°C	±1/2 LSB	±5 LSB	Q-20
AD7545GLN	0°C to +70°C	±1/2 LSB	±1 LSB	N-20
AD7545GCQ	–25°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7545GUQ	–55°C to +125°C	±1/2 LSB	±1 LSB	Q-20
AD7545JP	0°C to +70°C	±2 LSB	±20 LSB	P-20A
AD7545SE	–55°C to +125°C	±2 LSB	±20 LSB	E-20A
AD7545KP	0°C to +70°C	±1 LSB	±10 LSB	P-20A
AD7545TE	–55°C to +125°C	±1 LSB	±10 LSB	E-20A
AD7545LP	0°C to +70°C	±1/2 LSB	±5 LSB	P-20A
AD7545UE	–55°C to +125°C	±1/2 LSB	±5 LSB	E-20A
AD7545GLP	0°C to +70°C	±1/2 LSB	±1 LSB	P-20A
AD7545GUE	–55°C to +125°C	±1/2 LSB	±1 LSB	E-20A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-20) in lieu of cerdip packages (Q-20).
[2]To order MIL-STD-883, Class B process parts, add /883B to part number. Contact local sales office for military data sheet. For U.S. Standard Military DRAWING (SMD) see DESC drawing 5962-87702.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip.