

Nondissipative Clamping Benefits DC-DC Converters

By **Viktor D. Vogman**, Senior Power Supply Engineer,
Enterprise Power Conversion, Intel Corp., DuPont, Wash.

Even if small, a transformer's leakage inductance reduces the efficiency of some isolated dc-dc converter topologies. However, the technique of lossless voltage clamping helps restore most of the lost energy.

The leakage inductance of the power transformer of an isolated dc-dc converter may significantly affect its efficiency and cost. Using lossless recovery circuits improves efficiency and avoids problems arising from transformer leakage-inductance spikes.

In the dual-transistor forward (full-bridge and half-bridge) converters, where the switching transistors are connected in series, energy stored in the transformer leakage inductance may be recycled through the clamping diodes that are an integral part of this architecture. However, in the

"single-ended" topologies, such as forward, flyback, push-pull and current-fed, in which the switching transistors are connected to electrical ground, the energy stored in the leakage inductance may significantly affect a converter's performance.

If no measures are taken to recover the energy stored in this inductance, the energy will be dissipated either in the converter components or in the snubber circuits, absorbing voltage spikes caused by the leakage inductance. Energy stored in the leakage inductance of the power transformer during each switching cycle may be represented by this equation:

$$E_{LS} = \frac{L_s \times I_M^2}{2} \quad \text{Eq. 1}$$

where L_s is the leakage inductance between primary and secondary windings, and I_M is the peak current in the primary transformer winding.

Power loss (P_{LS}) associated with the leakage is proportional to the switching frequency (f_{sw}):

$$P_{LS} = \frac{L_s \times I_M^2 \times f_{sw}}{2} \quad \text{Eq. 2}$$

The efficiency loss associated with P_{LS} may be determined as a ratio of the power dissipation caused by the leakage inductance to the power drawn from the primary source (V_{CC}). For a single transistor topology, the drawn power is:

$$P_{IN} = V_{CC} \times I_M \times D \quad \text{Eq. 3}$$

where D is the switching transistor duty cycle.

Taking the ratio of Eq. 2-to-Eq. 3 and making simple transforms gives a simple equation quantifying the efficiency loss associated with the leakage inductance effect:

$$\text{Efficiency Loss} = \frac{P_{LS}}{P_{IN}} = \frac{1 - K_C}{2 \times \hat{I}_\mu} \quad \text{Eq. 4}$$

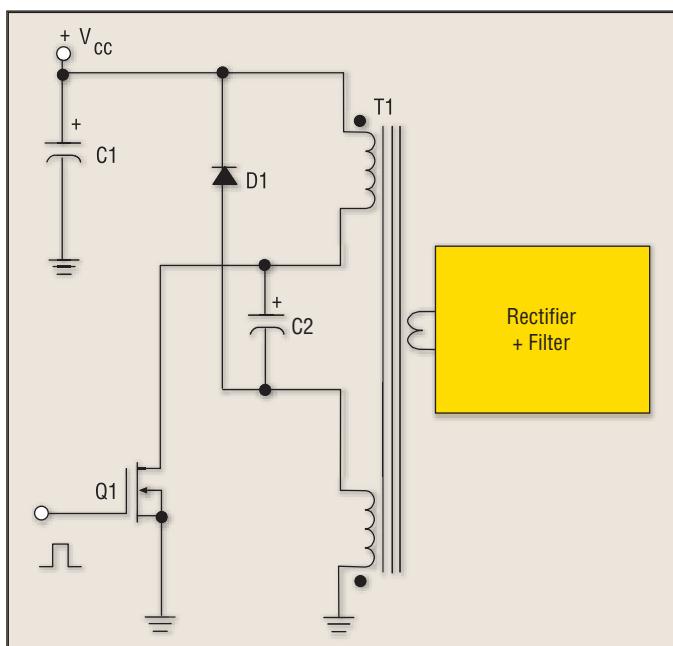


Fig. 1. Clamping circuit for transistor forward and flyback converters. A capacitor (C_2), coupling similar leads of the two identical primary windings, and a diode (D_1) provide lossless voltage clamping in forward and flyback converters at a level $V_{DSMAX}=2V_{cc}$.

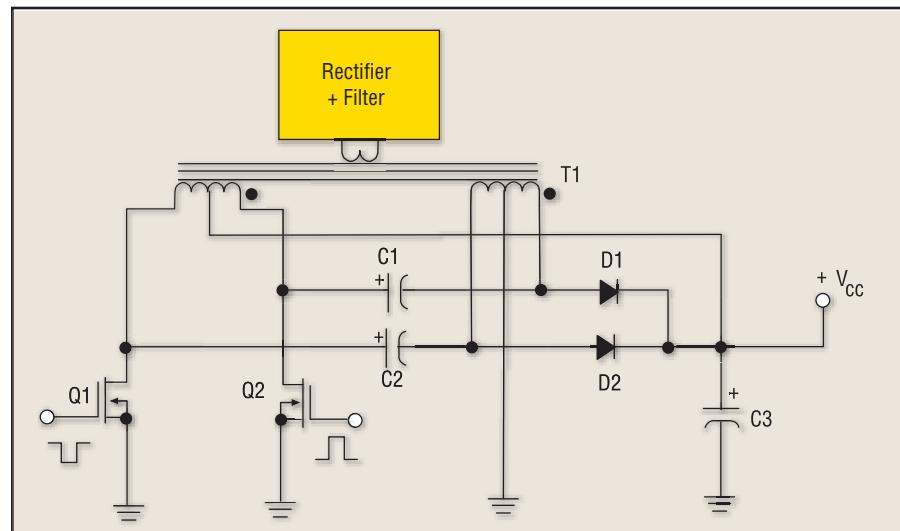


Fig. 2. Lossless clamping circuit in a push-pull converter. Combining two of the clamping circuits shown in Fig. 1 provides clamping of voltage spikes in the push-pull converter.

where K_C is the transformer coupling factor $K_C = 1 - L_s / L_\mu$, L_μ is the magnetizing inductance, and I_μ is the magnetizing current magnitude normalized to the peak current:

$$\hat{I}_\mu = \frac{I_\mu}{I_M} = \frac{V_{CC} \times D}{(L_\mu \times f_{SW} \times I_M)}$$

Assume that the magnetizing current of a typical transformer doesn't exceed (0.1 to 0.2) I_M . Then according to Eq. 4, even with a power transformer having a comparatively low leakage inductance ($K_C = 0.99$), the efficiency loss associated with L_s reaches 2.5% to 5%.

Conventional ways of alleviating this issue—providing better winding coupling or using active clamps—usually affect the cost and dynamic performance of a converter.

At the same time, the efficiency loss associated with leakage inductance may be recovered while maintaining low cost and high reliability in a dynamic load environment. This can be achieved if energy stored in the leakage inductance could be recovered back to the primary source. This function may be provided with the help of the lossless clamping circuits described next.

Basic Lossless Clamping

The simplest lossless clamping circuit suitable for a single transistor forward and for flyback converters is shown in Fig. 1. The circuit incorporates the recovery reset winding (W2), with its number of turns equal to the primary winding (W1), a blocking capacitor C2, coupling identical leads of the two windings and a clamping diode D1. Since there is no dc voltage drop across transformer windings, C2 represents a floating dc source with a voltage equal to V_{CC} . Once the switching transistor Q1 turns off and voltage across it exceeds $2 V_{CC}$, D1 starts conducting and recovers energy stored in the magnetic field of the transformer T1 and its leakage inductance back to the primary source.

Minimum capacitance required for effective clamping can be determined as:

$$C_2 \text{MIN} = \frac{L_s \times I_M^2}{\Delta V \times 2 \times V_{CC}} \quad \text{Eq. 5}$$

where ΔV is a normalized ripple voltage on C2 predetermined by design:

$$\Delta V = \frac{\Delta V}{V_{CC}} \quad \text{Eq. 6}$$

Let us assume the converter operates from the power-factor correction (PFC) stage with output voltage $V_{CC} = 400$ V; the transformer leakage inductance between primary and secondary windings $L_s = 20 \mu\text{H}$; maximum switching transistor current $I_M = 10$ A; and we would like to limit peak voltage across the switching transistor at $V_{DSMAX} = 2.01 V_{CC}$ (i.e. $\Delta V = 0.01$). Plugging these numbers in Eq. 5 gives $C_2 \text{MIN} = 0.625 \mu\text{F}$. This is the minimum capacitor value that allows clamping of the voltage across the switching transistor at a level $V_{DSMAX} = 804$ V. This value is obtained on the assumption that capacitor ESR is negligible as compared to its reactance at a frequency:

$$f = \frac{1}{2} \times \pi \sqrt{L_s \times C_2} \quad \text{Eq. 7}$$

KEEP YOUR COOL

INTRODUCING...

T_J=150°C TRIACS

Visit us at the
POWER ELECTRONICS
EXHIBITION & CONFERENCE
Booth 915

Based on SanRex's new diffusion technology, the NEW T_J=150°C Triacs, TMG-Q series, increases T_J (max) from 125°C to 150°C, and offers this extremely cool advantage: Typically reduce the heat sink size by 66% or eliminate it completely for high efficiency and reliability, at a lower cost.

0.8 amp up to 25 amp
Environmentally friendly
Lead-free plating finish as per EU's RoHS
Variety of packages available

SanRex®
SanRex Corp. Semiconductor Division
50 Seaview Blvd., Port Washington, NY 11050-4616
Tel (516) 625-1313 Fax (516) 625-8845
www.sanrex.com

CIRCLE 218 on Reader Service Card or freeproductinfo.net/pet

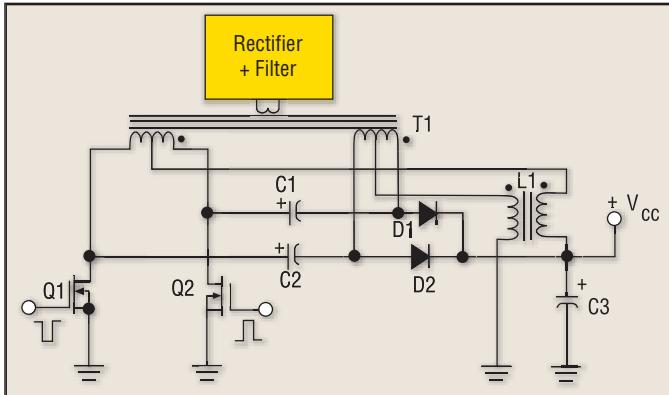


Fig. 3. Lossless clamping circuit in a current-fed push-pull converter operating in nonoverlapping conduction mode. Use of the clamping circuit in Fig. 2 for a current-fed push-pull converter operating in nonoverlapping conduction mode requires one more identical winding on the feeding inductor (L1).

If that is not the case, an additional voltage drop across the capacitor ($ESR \times I_M$) should be taken into account. It is also important to note that during the transistor turn-off time period, a current in a series resonant circuit consisting of a clamping capacitor and leakage inductance between two primary windings may add copper losses on the primary side. To prevent this from happening, the resonant frequency of this circuit should be made lower than the switching frequency:

$$f_R = \frac{1}{2} \times \pi \sqrt{L_{sp} \times C_2} \ll f_{sw} \quad \text{Eq. 8}$$

where L_{sp} is leakage inductance between primary transformer windings.

This could be provided by increasing capacitor C_2 's value and using an electrolytic capacitor. In several cases, using a larger-value electrolytic capacitor rated to withstand V_{cc} could also be more cost-effective than using minimum-value ceramic caps. The diode D_1 should be able to withstand a reverse voltage $V_R = 2 V_{cc}$. In conventional applications, it conducts only the reset current of the primary transformer winding. In this case, it should have a peak current rating exceeding I_M . Average current flowing through this diode depends on magnetizing current and the primary/secondary winding leakage inductance. Normally, it is quite low and doesn't exceed a small percentage of the average current drawn from the primary source.

One of the advantages of using a large-value electrolytic capacitor is that current drawn from the primary source never drops to zero. When the switching MOSFET turns off, the snubber circuit continues to draw current flowing through the primary windings and charges the clamping capacitor C_2 . This results in significant (2x) reduction of the current step in the primary source and the associated EMI. Another advantage related to the lossless snubber is the opportunity to relax the transformer coupling requirements and allow

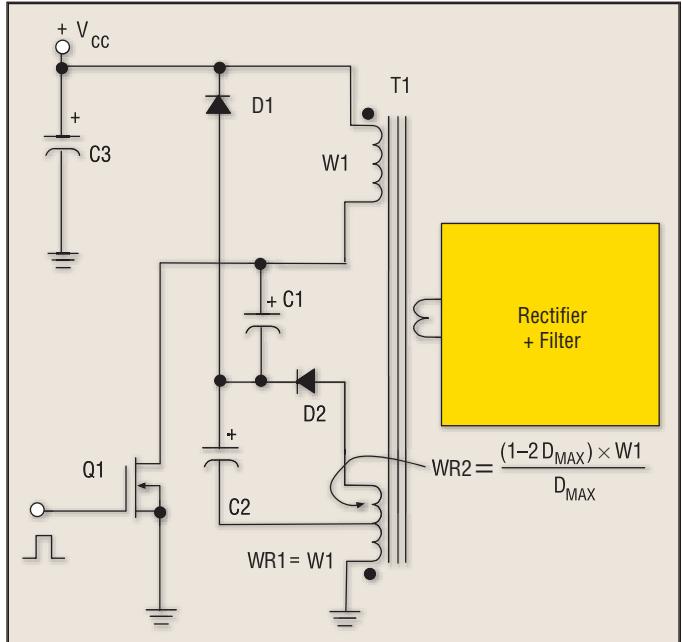


Fig. 4. Lossless clamping circuit for converters with small duty-cycle limits. A tapped recovery winding with two capacitors and two diodes is capable of providing stiff lossless voltage clamping at a level $V_{cc} < V_{dsmax} < 2 V_{cc}$.

converter operation with increased leakage inductance. In turn, this helps to reduce current ramp rates and peak current magnitudes as well as the generated noise level.

While the dc component of the switching transistor current flows exclusively through the main primary winding (W1) connected to the positive terminal of the primary source, the ac component of the switching transistor current is split evenly between both primary windings. Assuming,

One of the advantages of using a large-value electrolytic capacitor is that current drawn from the primary source never drops to zero.

for simplicity, that transistor current waveform has a flat top, RMS current of the primary winding can be determined by this equation:

$$I_{RMS-W1} = \frac{I_M}{2} \times \sqrt{D \times (1 + 3 \times D)} \quad \text{Eq. 9}$$

where D is duty cycle, which is the fraction of the switching cycle corresponding to the transistor's on state.

The RMS current of the recovery winding (W2) can be determined by this equation:

$$I_{RMS-W2} = \frac{I_M}{2} \times \sqrt{D \times (1 - D)} \quad \text{Eq. 10}$$

All other equations describing converter operation do not differ from the traditional topologies.

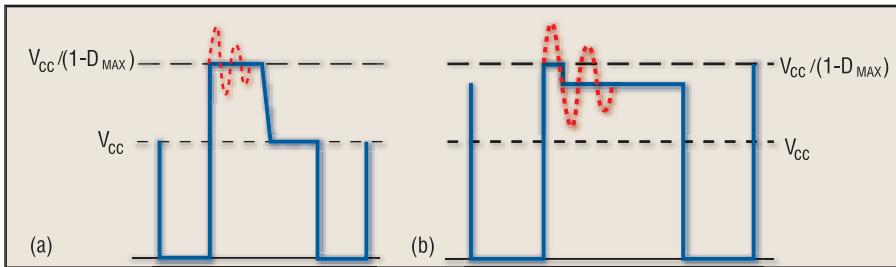


Fig. 5. Typical timing diagrams of a MOSFET's V_{DS} voltage in forward (a) and flyback (b) converters. Using lossless clamping helps to eliminate leakage voltage spikes, improve efficiency and obtain classic waveform shapes characteristic of ideal cases.

The maximum duty cycle (D_{MAX}) that can be achieved in this topology is 0.5. It is important that this limit not be exceeded. If the duty cycle exceeds 50%, the transformer may saturate. The circuits providing stiff lossless clamping at larger duty cycles are described next.

Higher-Order Lossless Clamping

The circuit of Fig. 1 may be used as a basic building block for lossless clamping of the leakage-voltage spikes in push-pull and current-fed push-pull converters operating in nonoverlapping conduction mode. These topologies are shown in Figs. 2 and 3, respectively. In Fig. 3, an additional winding with an equal number of turns on the feeding

inductor L1 core is also required.

In practice, the transformer core in the push-pull converter operating in a voltage mode may drift off the center of the origin of its B-H curve. This occurs because of pulse duration differences caused by tolerances of the driver circuits and switching transistors. To prevent this from happening, a current-mode control is normally required for this topology. If for some reason a single current sensor, being an integral part of this control, has

to be placed on the primary side in the lossless clamping topology, it is reasonable to position this sensor between the sources (which will be tied together) of the transistors Q1 and Q2 and the ground (negative terminal of the primary source). In this case, one sensor will monitor true currents flowing through each of the switching MOSFETs, which include current components that are provided by the clamping capacitors C1 and C2 (Fig. 2).

For forward and flyback converters with $D_{MAX} < 0.5$, where voltage spikes need to be clamped at a level below $2V_{CC}$, the clamping circuit shown in Fig. 4 is recommended. In this circuit, the recovery winding is split into two sections: WR1 (WR1=W1) and WR2. The number of turns

SURFACE MOUNT RESISTORS

Control the Power

Our engineers have developed a complete range of SURFACE MOUNT RESISTORS for the power electronics world, from current sense to high voltage in various styles. For your next application choose an Ohmite solution and design-in excellence.

EXCELLENCE

1600 Golf Road, Suite 850
Rolling Meadows, IL 60008
Phone: 866-964-6483 Fax: 847-574-7522
www.ohmite.com email: sales@ohmite.com



Visit us at the
POWER ELECTRONICS
TECHNOLOGY
EXHIBITION & CONFERENCE
Booth 1132

OHMITE®

CIRCLE 220 on Reader Service Card or freeproductinfo.net/pet

NONDISSIPATIVE CLAMPING

of WR2 depends on the maximum duty cycle required in the converter and may be determined by this equation:

$$WR2 = \frac{(1 - 2D_{MAX}) \times W1}{D_{MAX}} \quad \text{Eq. 11}$$

Voltages across blocking capacitors C1 and C2 in steady state are equal to:

$$\frac{V_{CC} \times D_{MAX}}{(1 - D_{MAX})} \text{ and } \frac{V_{CC} \times (1 - 2 D_{MAX})}{1 - D_{MAX}}, \text{ respectively.}$$

Typical timing diagrams showing voltages across the switching transistor in forward and flyback converters using lossless clamping are shown in **Fig. 5**. Using stiff voltage clamping in these topologies eliminates voltage spikes and provides classic waveform shapes that are characteristic of ideal cases.

For converter topologies with $D_{MAX} > 0.5$, the clamping circuit shown in **Fig. 6** may be used. This circuit clamps the transistor peak voltage to the level of $3 V_{CC}$ and allows operation with duty cycles up to 0.66. It is also recommended for the current-fed push-pull converter operating in overlapping conduction mode.

Splitting the recovery winding into two not-directly coupled halves allows for rearranging the topology shown in **Fig. 6** into a clamping circuit for a dual-transistor forward/flyback converter, allowing expansion of its duty cycle to 0.66 and getting stiff clamping to the level of $1.5 V_{CC}$ for each of its switching MOSFETs. This circuit is shown in **Fig. 7**.

Similar clamping circuits may be proposed for converters operating at duty cycles exceeding 0.66; however, because

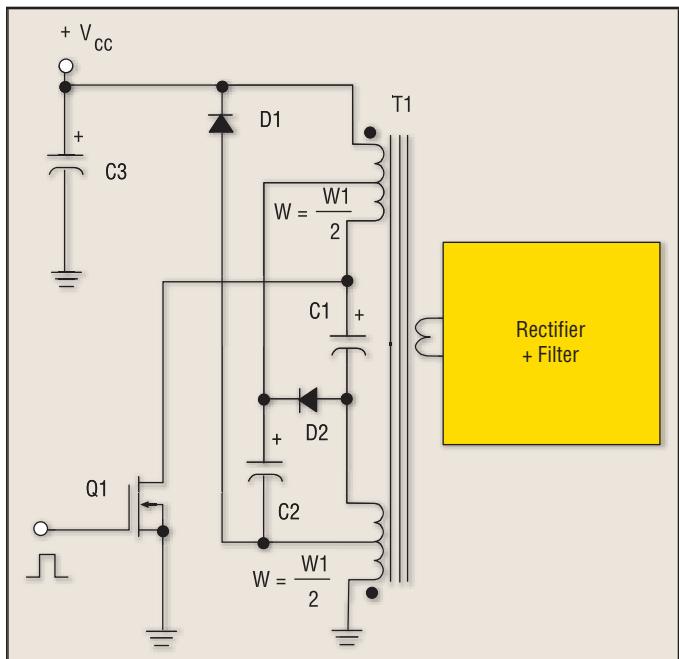


Fig. 6. Lossless clamping circuit for forward and flyback converters operating at a duty cycle exceeding 0.5. Two taps divide the primary windings in half, and two capacitors and two diodes provide stiff lossless voltage clamping at a level of $3 V_{CC}$.

of their complexity and increased discrete part count, their usage may be considered impractical.

Design Tips

There are a few key points to bear in mind when designing with lossless voltage-clamping components. One is that the current flowing through the recovery windings does not include the dc content of the switching transistor current. Therefore, a small gage wire can be used. Another consideration is that the clamping capacitors connect the winding taps with equal numbers of turns. To prevent capacitor-charging currents from flowing through the switching transistor, it is recommended that designers avoid errors in the numbers of turns.

Also note that stiff clamping provides an opportunity for relaxing the transformer coupling requirement. This option allows operating with increased leakage inductance, which in turn helps reduce current ramp rates and generated noise level. And finally, observe that clamping capacitors are essentially connected in parallel with the main V_{CC} decoupling capacitor. Therefore, the main V_{CC} decoupling function can usually be shared among several capacitors, including those that provide stiff voltage clamping. **PETech**

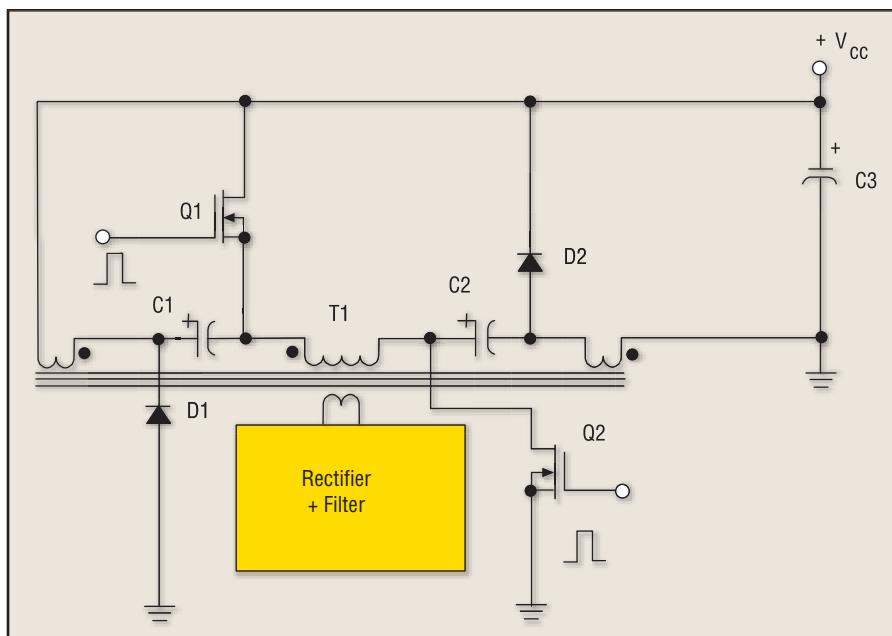


Fig. 7. Lossless clamping circuit for dual-transistor forward/flyback converters. This circuit allows expanding the converter duty cycle to 0.66 and clamps voltage spikes at a level of $1.5 V_{CC}$ for each of the switching MOSFETs Q1 and Q2.