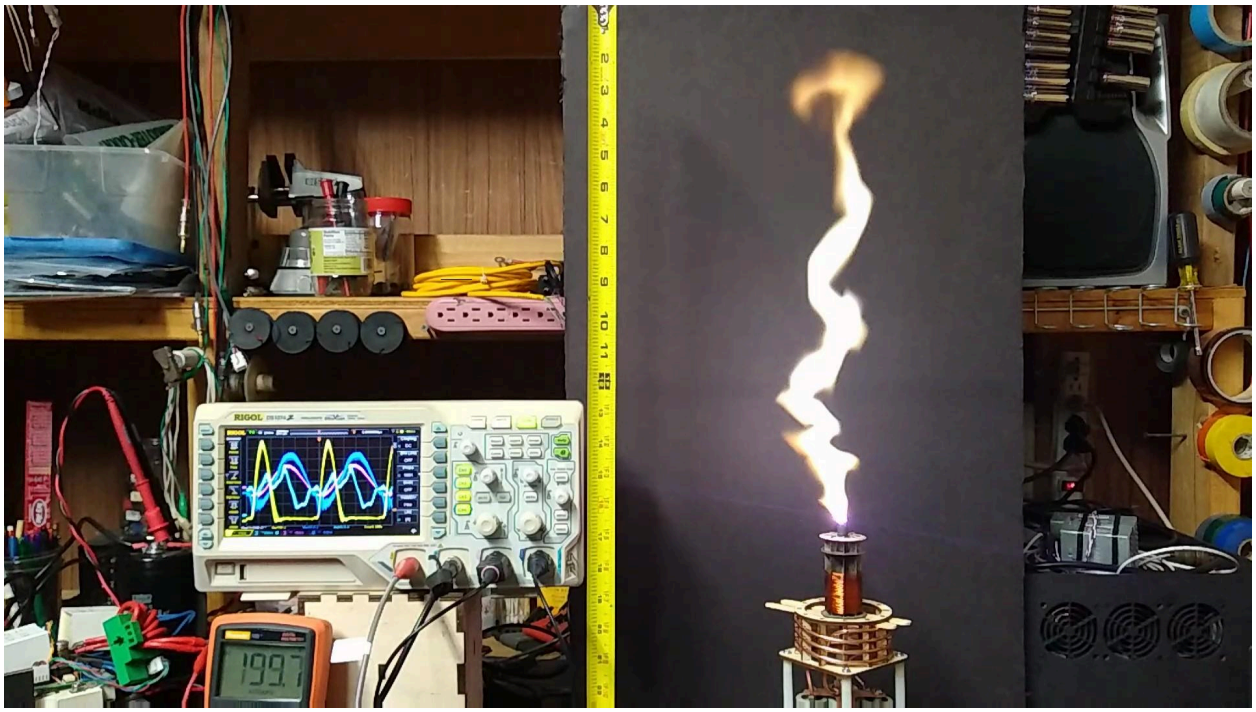
HFSSTC - The Classy Self Oscillator Steve Ward, Feb 2021

I'm not sure who "originated" this deceptively “simple” circuit, but my original exposure was from this excellent website:

https://www.vn-experimenty.eu/teslov-transformator/hf-sstc/hf-sstc-1.html

After seeing how clever this circuit is and the size of flame produced from an IRFP460, I knew I wanted to try it with some newer parts. With some LTspice study-time (the best way to suppress the plasma habit is the spice/femm/matlab simulation habit), I quickly discovered that control of gate bias, phase, amplitude, were of great importance to the efficient operation of this circuit. An explanation of critical circuit fundamentals of operation is often lacking in any published information, so I’m gonna take a swing at explaining it!



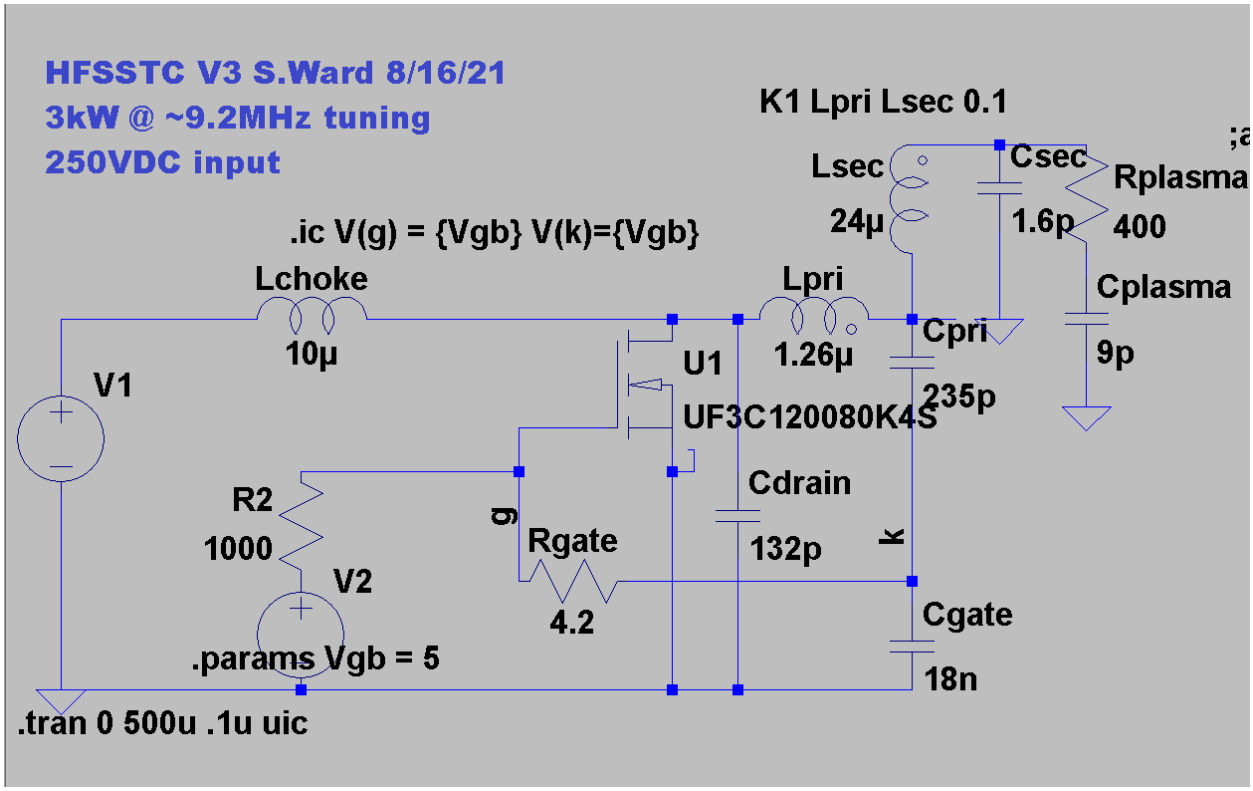
The HFSSTC Class E Power Oscillator works at ~9.3MHz processing up to ~3000W of input power with flaming arc bridging a 15” gap. Who doesn’t want such a desk toy?!

SERIOUS SAFETY ALERT, NOT A TOY: it produces toxic fumes, probably a fair bit of UV, and obviously will catch things on fire, and the plasma will burn you if the DC doesn’t shock, so no touchy! I operate this machine directly under forced exhaust ventilation to keep the nasties out of my lungs. Safety glasses of some form to block UV would probably be wise. Fortunately, the voltages produced are relatively low (<10kV), so capacitively coupled RF discharges don't seem to be an issue with reasonable distance. Also, do NOT use tungsten, brass, or zinc-plated breakout points as they all produce harmful oxides when burned. Carbon (like “gouging rod” or inside certain dry-cell batteries) is probably the best bet for least toxic breakout electrode.

Theory of Operation:

Intro:

Below is a schematic (needs update) of the LTspice model of a “simple” HFSSTC.

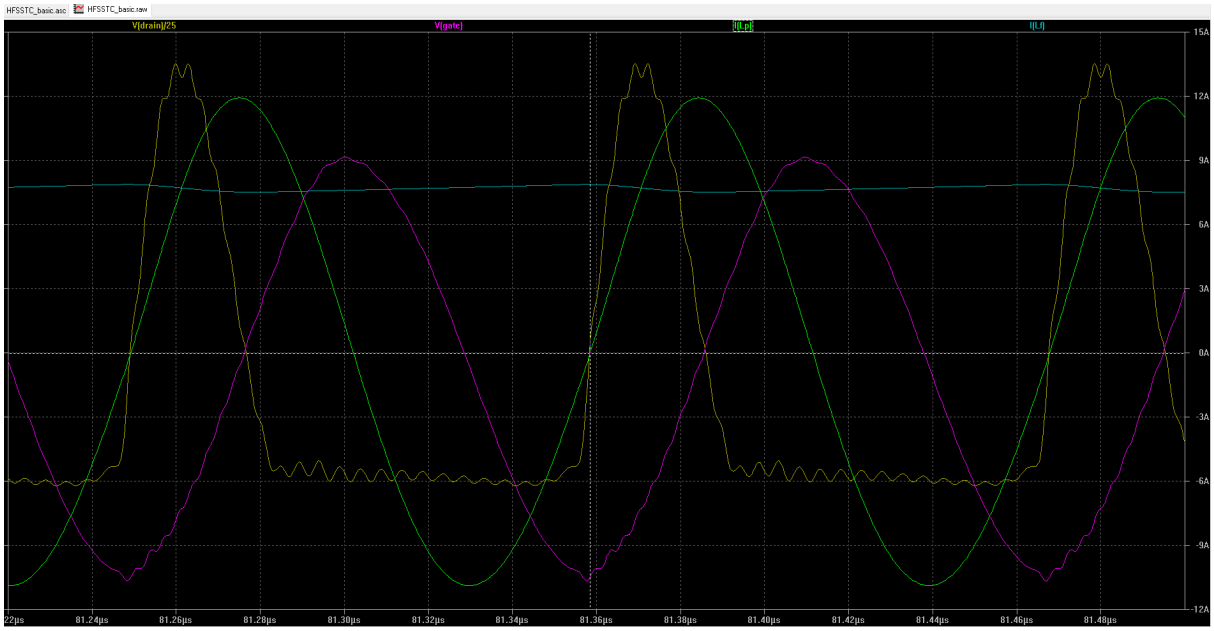


This circuit is a class E power oscillator, relying on the gain of a transistor being far greater than unity, and the fact that there is a phase shift in the voltage signal delivered to the MOSFET gate relative to the voltage at the drain. Roughly speaking, the gate voltage should be “inverted” with respect to the drain voltage to make an oscillator, but practically speaking there are reasons this 180 degree phase shift isn’t an exact enough answer. The circuit comes into oscillation as any disturbance in drain voltage will induce a current through the tank circuit, preferentially, as its impedance at RF is small. This tank current produces a lagging voltage across the tank capacitor, and a fraction of that voltage is fed to the gate with a “voltage divider” type tank capacitor arrangement of Cp and Cg.

Overview:

So, without getting too detailed yet, let’s identify the circuit components. Starting with the input inductor, Lf, its function is to provide steady input current to the oscillator and allow the drain voltage to take on a pulsed waveform. Lp and Cp+Cg form a series-resonant “tank” circuit along with providing a feedback voltage as Cp and Cg form a capacitive voltage divider. Note that the Tesla coil secondary is connected to the primary voltage (auto-transformer style), taking advantage of this extra voltage boost reduces the total voltage that the secondary must generate, which is helpful for efficiency reasons as it minimizes the conductor length required and so resistance is less. Of course, the remaining crucial component is the MOSFET which while conducting, will cause input current through Lf to increase and also discharge Cp+Cg

("Ctank") through Lp, and likewise when blocking will decrease current through Lf and charge Ctank through Lp.



Seen above are typical waveforms of a "robustly" operating machine. Yellow is drain voltage (divided by 25), purple is gate voltage (measured externally, so the true gate voltage is lagging due to inductance/resistance feeding gate junction capacitance), the green is the primary current through Lp, and the light blue is input current through Lf.

Input Filter, Lf:

One way to think about a filter inductor, Lf, is as a "constant current" source as the current ripples should be smaller than the average current. The current will increase through this filter inductance if drain voltage is less than the supply voltage, at a rate dI/dt = (Vsupply-Vdrain)/Lf. In steady state, the average drain voltage (plus the resistive losses in the inductor, we can ignore for now) must then equal the supply voltage for the input current to hold a steady average value. Therefore, if the drain voltage is zero for some portion (and input current increases) of the oscillation period, it must then exceed the supply voltage (and input current decreases) for some other portion to achieve the same average value. Since it's the average values that must be conserved in steady state, the narrower the drain voltage pulse width is, the higher magnitude it must have, so an optimum voltage profile should exist that minimizes drain voltage while delivering maximum power.

Drain Voltage "Shape":

It's important to see why the drain voltage takes on the shape that it does. When the MOSFET switches from ON to OFF, and there is current flowing into the drain from Lf and Lp, that current begins to charge the parasitic capacitance between drain and source nodes of the mosfet (plus any external snubber C). It is this "output capacitance" (Coss) of the MOSFET plus Cd that serves to limit the voltage rise over time. I've explained why the voltage will INCREASE across the MOSFET, because Lp and Lp charging Coss, but why does the voltage ever stop increasing? And why does it actually return back to zero? There must be a current that

DISCHARGES Coss, and that is the role of the resonant primary current, which has a peak value that exceeds the input current and sucks the energy back out of Coss before the MOSFET turns back on again. Given that the primary current oscillates around zero (its AC only), the duration of time for which the primary current exceeds the supply current must be long enough to discharge Coss so that there is zero drain voltage when the MOSFET turns on. This means, roughly, that the tank must maintain enough "stored" energy to reflect back into the driver, or basically, the Q factor must be high enough.

Power Factor, Dot-Product, "real" power:

If my explanation for how the oscillations go was satisfactory, let's go one step further to understand how to not just make an oscillator, but make sure it processes the maximum useful "real" power possible. Considering the concept of "power factor", it would make sense then that the drain voltage would pulsate "in phase" with the primary current as much as possible to maximize the power factor of the converter. Another way to look at it is, the "real" power is the dot product of the drain (driving) voltage and the primary (load) current. The dot product is zero when 2 sine waves have a 90 degree phase shift and the same frequency, and conversely, the dot product is maximum when there is zero phase shift between voltage and current sines.

The drain voltage is not a simple sine wave, instead it is sort of a half-sine pulse with a frequency higher than the oscillation period (the exact shape isn't really critical to understand the concept). The voltage pulse seen at the drain is dependent on the timing of the gate signal, combined with the input current (through Lf) and primary current (from Lp) to determine what happens to the voltage across Coss (mosfet drain-source cap) and Cd. Crudely speaking, the voltage pulse is about ¼ to ⅓ of the total cycle period. For power factor reasons, it would seem the ideal timing for the voltage pulse is to start at the primary current zero crossing so that the entire voltage pulse lies within the positive portion of primary current. This ensures that every volt-amp-second (aka, watt-second, or Joule) contributes to output power rather than some of it canceling out as reactive power. Practical tuning shows the drain voltage pulse takes off just a bit before the primary current zero crossing, otherwise the risk of losing ZVS goes up significantly. So a trade-off is power factor for safety margin. This circuit will happily oscillate, with plenty of safety margin, at a very poor power factor if the gate voltage phase is not tuned.

Low power factor shows up, essentially, as a higher drain voltage for a given primary current and output power, as any drain voltage applied while the primary current is negative, effectively cancels the same volt-amp-seconds while the primary current is positive. Since voltage margin is limited, it makes sense to optimize the switch-off timing and external Cd to reduce drain voltage as much as possible for a given operating current.

Class-E characteristics and Zero Volt Switching (ZVS):

In typical "hard" switching converters (not class E), when the semiconductor transitions between conducting and non conducting states (and vice versa), there is a brief time where the device sees both high voltage and current, and the power lost to the chip can be kilowatts, although for only some nano or microseconds duration, so the average power is reasonable and

power semiconductors can tolerate this if the localized heat isn't too great to be dispersed. Considering switching at 10MHz, this kind of "transition" loss must be mitigated for all practical implementations. Class E is a type of "Zero Voltage Switching" (ZVS) condition which allows the switching transition to happen with essentially zero voltage across drain to source. Since power is voltage potential multiplied by current, if the voltage is zero, the power is zero even if the current is non-zero. In this way, the efficiency of any ZVS converter can be quite high, especially at high frequencies where the switching losses dominate. ZVS can apply to both the "turn on" and "turn off" transitions. Of course, the truth is there is still some switching loss, though usually quite small compared to the conduction losses due to Rds.

ZVS Turn ON:

ZVS is applied at turn on due to some external circuit current that discharges the Coss (effective drain-source "output" capacitance of the mosfet) and brings the drain voltage to zero before the MOSFET is due to conduct. The gate voltage must be applied quickly after drain voltage is brought to zero, or else there is risk that the external oscillatory circuit current could reverse and "re-charge" Coss. It is the "self-discharging" of Coss that is to be explicitly avoided for it will cause immediate failure at high operating power levels. So with this point in mind, turning on, even with zero current, but a voltage across Coss, will produce "switching loss" that is very real! Hence the reason that the "external" circuit discharges Coss, rather than the mosfet turn-on short circuiting Coss when it's charged.

ZVS Turn OFF:

ZVS is applied at turn off by considering that the Coss can act as a voltage limiter at the critical time that the mosfet junction is transitioning from conducting to non conducting. Coss, initially, is discharged, and so the current that was once flowing through the mosfet channel is now effectively bypassed by Coss during the turn off transition. In some cases, extra capacitors are added from drain to source to further limit the rise in drain voltage during the transition time, further reducing switch off loss. ZVS turn off is potentially not quite zero loss, for this reason that Vds is indeed rising as the device is still conducting some finite "pinch off" current.

Zero Current Switching?

One last note, there is a misconception by some that class E is "zero current switching" (ZCS), and this is not the case. While it turns out that proper operation does have simultaneous MOSFET turn-off with the load zero current crossing, the MOSFET's drain current is definitely not zero at turn-off when working efficiently, and this is OK because ZVS is also an effective means to "zero" switching loss.

Also, on the topic of ZCS, it is important to realize that even if the mosfet is conducting zero current, but is switched from off to on, it can still dissipate appreciable energy if it discharges Coss, the drain-source capacitance of the mosfet. Therefore, ZCS condition does not necessitate ZVS condition, and switching losses can still be large! This is why "phase-lead" for bridge driven resonant loads can significantly improve switching losses, and is critical for QCW and CW machines at high frequency operation. By switching off the bridge leg before the load current reverses, the load current will serve to "gracefully" charge/discharge the Coss of

both transistors, avoiding this “self-discharge” loss. If the bridge leg does not switch before the current reverses, not only will the load current will try to maintain the voltage state on Coss, forcing self-discharge of Coss plus “reverse recovery” of the freewheeling or body diode, which causes ringing and even way more losses. This principle is the basis for “resonant charging” of capacitors being nearly perfectly efficient, while “resistive charging” of capacitors is 50% efficient, half the energy is lost in the resistance that limits the charging current. Don't let that last bit about “50% charging efficiency through resistance” confuse the issue on self-discharging Coss through the mosfet, in this case, the whole energy stored in Coss will be lost to heat as it short circuits.

Coss is Lossy!

One detail to mention with regards to Coss is that like any capacitor technology, it is not perfect, meaning there is some energy lost to heat when charging or discharging, no matter the method. This energy loss is just now being studied in more detail in the last 10 years, despite ZVS being commonly thought of as “lossless” switching for decades now! It is almost impossible to predict which Si MOSFET will have, say, 50% of the energy stored in Coss, known as Eoss, lost to dissipation, versus say 10% lost. With Eoss being ~10-20uJ, repeated at ~10MHz with 50% efficiency, this would represent 50-100W of extra switching losses that were supposed to not exist!! Compare that loss with the conduction loss, which would be on the order of 10Arms^2*0.1ohm = 10W. SiC and GaN devices seem to have much better Coss efficiency, and so I chose to focus efforts on SiC devices even though they have less power dissipation capability and cost more for specified Rds.

https://superlab.stanford.edu/poster/TPEL2019_paper_Grayson.pdf

Gate Bias, Phase, Amplitude:

As explained in the previous section on power factor, the gate voltage signal plays a crucial role in determining the starting time of the drain voltage pulse, which ideally coincides with the primary current zero crossing. The gate drive voltage is essentially a sine wave due to the high Q factor of the resonant tank circuit. If you think about the mosfet in simple terms, if the gate voltage is above the threshold voltage, the device is conducting, and when the gate voltage is less than threshold, it is blocking. You can then see how raising and lowering this sine wave would change the duty cycle of the MOSFET conduction as more or less of the sine wave is above/below the threshold voltage. This sine wave is lifted with the gate bias voltage, as there is no other source for DC current flow into the gate node. Also notice that, when increasing the bias voltage for example, the mosfet turn off timing will be delayed, and the turn on time will be advanced, the “on-time” duty cycle is increased. So bias can affect the phase and duty cycle of the gate control.

Temperature Effect on Gate Bias:

It is important to realize that all MOSFET technologies show a decrease in Vgs-threshold voltage with increasing junction temperature, so the effective bias voltage will increase as the temperature increases, which can be hazardous as it can cause loss of ZVS. This is one factor

among many that requires constant attention, via the oscilloscope, to see that the converter operates properly over the full range of power and temperature. This Vgs drop with increasing temp is a reason for less than ideal class-E conditions.

Gate drive "feedback network":

In order to control the gate phase/timing separately from the duty cycle, a gate resistance can be added. In academia, this resistor would be one type of "feedback network". Feedback networks are designed to provide the desired phase adjustment, sometimes it must add phase "lead" but in this case we want "lag" or delay. It turns out that this circuit structure, as previously seen on other websites, has too much phase lead built into it by letting Vgate = V(Cg). However most old-school silicon mosfets have enough inductance and resistance internally to the gate connection to delay the turn off/on sufficiently for good power factor (talk about lucky), so extra gate resistance is not always required. However even a small amount of phase shift can have a profound effect on performance, so tuning Rg can make a significant difference in performance as the power factor is optimized. If much gate resistance is required for good power factor, the value of Cg can be reduced to boost the gate drive voltage so that even with significant voltage drop on Rg, the gate voltage is sufficient to drive the mosfet efficiently (generally about 10V on the gate is fully ON for Si fet, some SiC fets want more).

Selecting the amplitude of the gate drive voltage is a trade-off between heat generated by internal gate resistance to the mosfet (this is often specified in the datasheet as internal Rg) and meeting ZVS conditions and reducing Rds_on by achieving sufficient gate voltage, and by staying within breakdown voltage limits on the gate I often aim for ~15V peak gate voltage, as measured externally to the device. As mentioned, there is internal resistance that will further reduce the gate voltage, so devices with a large gate charge, and large gate internal resistance will want some extra gate drive voltage to compensate. The SiC mosfet has relatively small gate charge, and requires substantial external gate resistance for good power factor. The internal gate resistance is ~5ohms, with external gate resistance set to ~15 ohms. We can infer the internal gate voltage based on the voltage drop across the 15 ohm resistor, and assume an additional voltage drop and phase shift being about ⅓ as much internal to the device. In this manner, external gate resistance can be helpful to infer what the voltage signal at the mosfet die might be, as we can never truly probe there.

Because we cannot directly probe the gate at the mosfet die, we are left to do some guesswork about what the "actual" gate voltage is. Fortunately, the drain voltage gives fairly clear evidence about when turn off and turn on is taking place. Generally, the gate voltage probed externally will have reached a significant negative voltage (5-10V below threshold) before the drain voltage shows signs of rising (indicating turn-off achieved). We can infer there must be similar lag when observing the gate turn-on timing. When gate turn-on is premature it will discharge Coss in a lossy way, and this must be avoided. With that in mind, the drain voltage waveform should show a smooth trajectory back to zero volts, any premature discharging of Coss is often evident as a "knee" in the drain voltage pulse with the voltage being pulled down at higher dv/dt along with extra ringing on the gate voltage at the time of turn-on. Note, that there is often some ringing on the gate voltage, even when operating efficiently, this is

just consequence of discontinuous mosfet current (so, a large dI/dt) which produces a voltage transient across the source inductance of the fet, which causes the voltage as the source node to ring, and thus measuring from gate-source, will show ringing.

With these concepts in mind, an experimenter can tune Cg for reasonable amplitude, tune Rg and bias for good power output and to maintain ZVS. Generally speaking:

Adjustment	Pro	Con
Increase Gate Bias	May delay drain voltage (switch-off) to improve power factor, will tend to enforce oscillation to persist. May advance turn-on, which might be good (or bad). Gives higher gate voltage, so lower On resistance, possibly.	If total loop delay is too big, may cause loss of ZVS! Increasing junction temp can lower Vgsth, effectively raising gate bias and causing loss of ZVS and MOSFET destruction. Reduces negative gate bias, which can make fet more prone to destructive self-oscillation at turn-off.
Decrease Gate Bias	Causes earlier switch-off which gives safer ZVS “robustness” (at the cost of worse power factor, usually).	Might reduce power factor if reduced too far. May suddenly fail to oscillate. May reduce duty cycle too far which can cause loss of ZVS as Coss “recharges” before turn-on due to excessive “off-time”. May increase Rds.
Increase Gate Amp. (less Cg)	Increases gate voltage to reduce Rds_on, easier to get oscillations started.	Causes extra loss on internal Rg, can destroy the gate, pushes the duty cycle closer to 50% instead of a more ideal 60-65%, can lose ZVS.
Decrease Gate Amp (more Cg)	Reduces internal/external Rg losses, less stress on gate oxide.	May become difficult to start oscillations, duty cycle may become too great causing loss of ZVS with turn-on event discharging Coss. Rds_on might be large due to low Vgs.
Increase Rg	May delay drain voltage pulse to be in phase with primary current, boosting power factor	Too much Rg will delay turn-off too much, loss of ZVS despite improved power factor. Power may be high,

		but losses will be huge.
Decrease Rg	Generally “safer” as gives earlier switch-off, so more robust ZVS	but consequently poor power factor can result from too low Rg from too much phase lead on gate voltage

Si Vs SiC:

There are a few key differences between silicon and silicon carbide mosfets, the most important being that SiC has much lower capacitance between gate, drain, and source. It is important to study the datasheet, which will always contain a plot of the 3 capacitors versus drain voltage. The drain-source capacitance, Coss, will play a big role in shaping the drain voltage, and this capacitance is essentially sized to match the power level and operating frequency of the oscillator. Higher power and lower freq will require more Coss+Cd. Some Si mosfets, especially higher current ones, may have too much Coss to even function properly in this circuit if the frequency is high, so it is not a simple matter of picking the biggest mosfet you can find.

The other 2 capacitances are from gate-source (often called the “input capacitance”, Ciss) and drain-gate (often called the “reverse transfer capacitance”, Crss). Ciss is representative of how much capacitance the gate presents to the circuit, a bigger Ciss will require more gate current to charge to the same voltage at a given frequency. Again, too big of Ciss will lead to difficulty in driving the gate, and it might function poorly at high freq. Crss works as a negative feedback as it couples the drain voltage back to the gate. During turn-off of the mosfet, the drain voltage will rise rapidly, and here Crss will try to “pull up” on the gate, which if successful, could lead to disastrous “self oscillation” of the mosfet. Likewise, when turn-on happens, the drain voltage is quickly returning to zero, which tries to “pull down” on the gate, hindering the turn-on process. SiC reduces the Crss and Coss capacitances by a greater amount than the Ciss, and this means SiC mosfets are easier to control, leading to greater efficiency when switching.

Tips for Si:

As mentioned, Si has larger internal capacitances, especially the gate-source (Ciss). This will lead to very low external gate resistance being required to tune for best power factor.

Bigger isn’t always better: since the conduction (Rds*Id^2) loss is relatively modest with a well-designed coil (the primary current is a decent indicator of the mosfet RMS current, while the input current is in fact the mosfet’s average current), sometimes the penalty of large fet capacitance can outweigh the benefit of lower ON resistance. It seems best to operate the fet at about ½ of the rated drain current in most cases.

There are different types of Si mosfets, in particular it is noted that “super junction” type, while they do reduce the magnitude of Coss, they also tend to have worse lossy factor for the Coss, which can become an appreciable amount of power dissipation. There’s no telling which fet will have better or worse Coss dissipation, as this characteristic is not normally published in spec sheets.

Tips for SiC:

SiC has its own list of shortcomings, namely reduced thermal dissipation capability (because the chips are much much smaller for a given Rds), and secondly, limited negative gate voltage tolerance and thirdly, lower “gain” (drain amps per gate volt) around the threshold, so higher gate amplitude would be helpful, but limited -Vgs rating might be problematic.

The thermal dissipation for a SiC fet will be substantially less than a Si part with the same current rating, this is because the SiC part is indeed more efficient and thus when used correctly, will have less heat to remove. However, generally speaking, the more potential for efficiency that SiC brings, also brings along more potential for disaster if the efficient mode of operation is compromised. The difference between SiC and Si on this point might be trivial, as any device would easily be overloaded by loss of ZVS or other malfunction.

As to the limited negative gate voltage tolerance and lower gain: enter, the SiC JFET cascode. Apparently SiC JFET makes for a pretty good switching device, but with the shortcoming that it's a normally-ON device and requires negative gate bias of ~5-10V to turn off. The cascode uses a low voltage Si MOSFET in series with the JFET source so that when the MOSFET is off, the required negative bias voltage will develop across the MOSFET and the JFET will turn off. Alternatively, when the MOSFET turns on, the JFET gate will have the same potential as source, and will turn ON. It’s important to note that low voltage Si MOSFETs are actually pretty outstanding compared to high voltage mosfets. The low voltage part adds negligible resistance and has a smaller gate charge than the SiC JFET that it’s controlling, and also, the main benefit, is that its gate is very rugged and can handle large negative voltage as well as positive.

RF Coil design optimization:

It’s generally true that coils which are as wide as they are long will have higher quality factor than long skinny coils due to the shape of the magnetic field produced by a solenoid. The trouble with any coil is that the field it produces interacts with the conductor, especially at the ends of the coil, which increases the apparent resistance of the wire itself. Longer coils will have greater increase in resistance due to it’s own field, while very short coils on the other hand will suffer more from too little inductance for a given length of wire. Since Q is defined as the ratio of inductive reactance (Xl) to effective resistance (ESR), the goal is to maximize Xl and minimize ESR.

Space winding can be an effective means of increasing Q factor of a coil as it allows the magnetic field of the coil to more easily penetrate the winding without inducing eddy currents in itself. In some cases, for a given winding pitch, resistance can actually increase with a bigger conductor, as the conductor surface area increases to capture more coil flux and raise the ESR.

The primary coil design uses both of these general ideas as inspiration, with its diameter being greater than its length, and by space winding a practical wire size.

The last tradeoff that I want to highlight is the self-capacitance of the coil, especially the secondary coil which has to produce the highest voltages. Self-capacitance is generally used to an advantage with Tesla coils, where some stored up energy in the secondary coil may aid the growth of sparks, and most tesla coils add extra toroid capacitance, even. However, in the case of very high frequency coils, the self-capacitance seems to be mostly a drawback. The reason it is undesired is mainly because for a given voltage required to generate the plasma, more self-C is just extra current demand for the secondary coil, and the plasma does not seem to benefit from the energy stored. Also, the design of my HFSSTC does not rely on secondary resonance, so in fact minimizing the capacitance seems to directly improve performance. The tradeoff, perhaps obvious, is that the smaller the secondary becomes, the finer the wire must be to achieve desired inductance, and so the resistance must be greater and at the same time, its smaller size means it can dissipate less heat. However, magnet wire with 200*C insulation is easy to come by, and coil forms capable of handling high temps are not hard to find for small coils, so in this case, smaller can be better.

Ceramic Capacitors:

Ceramic capacitors are pretty ideal for this application, especially the low loss types with stable dielectric constant properties, commonly “C0G” or “NP0”, but maybe more. Whether leaded or SMD, these parts have exceptionally low ESR, meaning even something like a 1nF 0805 C0G can handle at least an amp of RF current.

The tank cap Cp is constructed with a 6x6 array of 100pF, 3kVDC, 1808 case size, C0G SMD “chip” capacitors, and has been proven to handle ~12A RMS current at ~10MHz with a little air flow, maintaining temps <100*C, for parts rated to 130*C operation (the other nice part about ceramic, high operating temp). I did have trouble, however, with carbon tracking of my FR4 PCB on the first iteration of the cap assembly. However, my earlier iteration faced much higher tank voltages than the current state of the design, so FR4 PCB is probably OK, especially if the board can have slots cut where the caps mount, so there is no FR4 to track on under the cap.

The lower Cg is made up of ~12 parallel 1nF, 450V, 0805, C0Gs. Both caps were made by TDK and feature “soft terminations” which give them added robustness to flexing or soldering them with an iron.

The input filter cap, Cf, is a 1uF 630V, 3630 case, “X7R” type dielectric. I happened to have some leftovers, otherwise a film capacitor would be a lower cost option, as there is no need for ceramic here. Also no real need to use extra voltage rating here, it’s just filtering the 10MHz ripple.

Soldering Ceramic Capacitors:

I’d feel bad about suggesting SMD ceramic caps without including a warning about soldering them. While some MLCC’s may tolerate a soldering iron, others may crack due to the thermal shock, and you may not know it till the cap fails catastrophically later on. The safer method to soldering these parts is hot-air reflow, avoiding any big differential in heat across the

chip, and avoiding rapid heating/cooling. I've experienced SMD ceramic failures in a variety of voltage ranges (from 12V to 600V), all cases had been subjected to soldering iron at some point, before coming to understand what the cause was. Now, as much as possible, I try to use hot air methods, however, the soft termination caps from TDK have been quite resilient towards my impatient "just use the iron this one time" method.