Sachin Kumar

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Leetcode: leetcode.com/u /Sachuu 23/

GitHub: kr-sachin12/

Medium: /@sachinmizo1223/

Education

• Sharda University (SU)

UP, India

Bachelor of Technology - ECE; GPA: 7.0 2022 - 2026

• K.P.S Memorial High School Bihar, India

Class XII - CBSE; Percentage: 62% 2022

• St. Jhon's Higher Secondary School Mizoram, India

Class X - MBSE; Percentage: 72%

Skills

• Languages: C, C++, Java, Python, JavaScript, HTML, CSS, MySQL, Typescript

• Frameworks: ReactJS, Tailwind CSS, NodeJS, ExpressJS

• Database: PostgreSQL, MongoDB

• Others: Git, Github, Matlab, VScode, Vim, Cursor, System Design(HLD)

• **Soft Skills**: Leadership, Emotional Intelligence(EQ), Communication Skills, Teamwork, Adaptibility, Problem-Solving Mindest

Experience

• WebExpert Software (Certificate 1&2) May'25 - July'25

Built REST APIs with Node.js & Express (routing, middleware, request handling).

Integrated databases (MySQL/MongoDB) with focus on queries & authentication.

Created secure user auth & profile management module.

Improved API response time by 25% using query optimization & caching

Technologies Used: JavaScript (Node.js), Express.js, Redis, JWT, MongoDB

Projects

• Low-Latency, Hardware-Efficient SVD Algorithm for Real-Time Applications Research Paper 1

Designed an SVD algorithm using the CORDIC approach to minimize time delay and optimize hardware resource usage for real-time applications

Research paper published in IEEE Xplore

Technologies Used: C Programming, VLSI Design

• Smart AI Health Assistant

Built AI-powered health assistant with live monitoring, symptom analysis, and risk prediction

Developed secure backend using NodeJS, ExpressJS, MongoDB, JWT, and real-time APIs

Integrated Google Maps API for nearby hospital/doctor recommendations

Patent published in Patent Office Journal

• FPGA-Accelerated ANN for Efficient Arrhythmia Multi-Classification

Research Paper 2

Patent Office Journal

Email: sachinmizo1223@gmail.com

Implemented ANN-based ECG Classification on FPGA for biomedical applications

Enhanced accuracy and optimized hardware utilization.

Research paper published in IEEE Xplore

Tools: C, VLSI, PYNQ-Z2, Vitis HLS, Vivado

Achievements

- Patent published in Patent Office Journal
- Contributed a full chapter on Functional Verification of ASICs for Performance Optimization in Front-End VLSI Design in a
 recently published book <u>Exploring the Intricacies of Digital and Analog VLSI</u>, edited by <u>Koushik Guha</u>, <u>Jyoti Kandpal</u>, and
 <u>Swagata Devi</u> (IGI Global, 2025).
- Solved 900+ questions on all platform and 400+ on Leetcode
- 2 Research paper published in IEEE Xplore
- Qualified JEE Mains 2022S