CSIT\_230 HW-4, Module 4

1.

Design a digital logic circuit as a Read Only Memory (ROM) [Decoder plus OR

gates]. A ROM accepts a three–bit number and generates an output binary number

equal to four times the input number.

**(a)** What is the size (number of bits) of the initial (unsimplified) ROM ?

2^n x m

2^3 \* 5

One 3-8 decoder and 5 or gates are needed

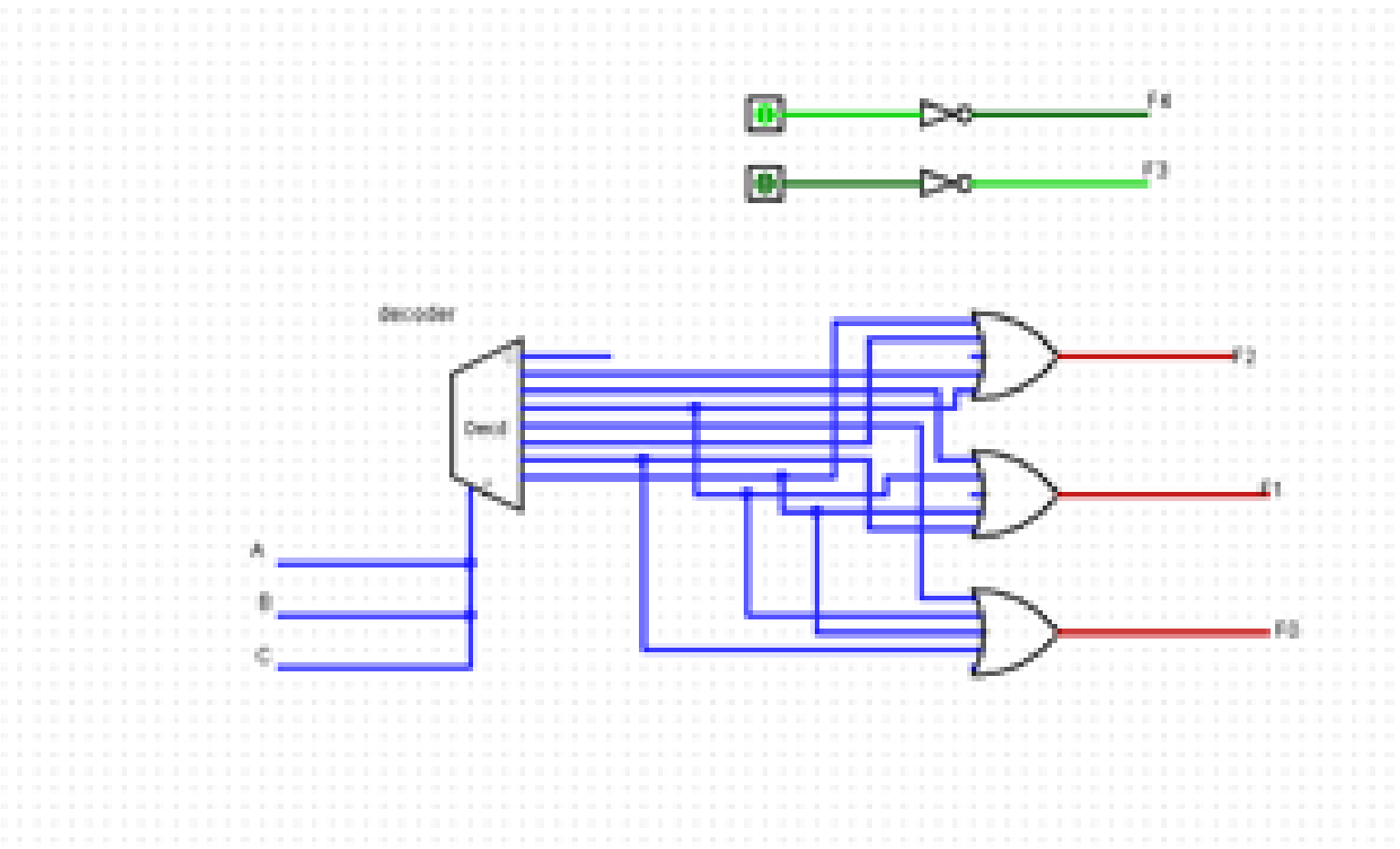
**(b)** What is the size (number of bits) of the final (simplified) ROM ? (c)

Show in detail the final memory layout.

N= 3 M=5

Since 3 is the input the output is 12

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A | B | C | F0 | F1 | F2 | F3 | F4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |



2.

Design a digital logic circuit as a Read Only Memory (ROM) [Decoder plus OR

gates]: Three light–emitting diodes (LEDs) [one Red, one Green, one Blue] turn on

when a number 0–7 is passed through. Red turns on with even numbers, green

turns on with odd numbers, blue turns on with multiples of 3. Zero means they are

all off, seven means they are all on.

(a) What is the size (number of bits) of the initial (unsimplified) ROM ? (b) What is

the size (number of bits) of the final (simplified/smallest size) ROM ? (c) Show in

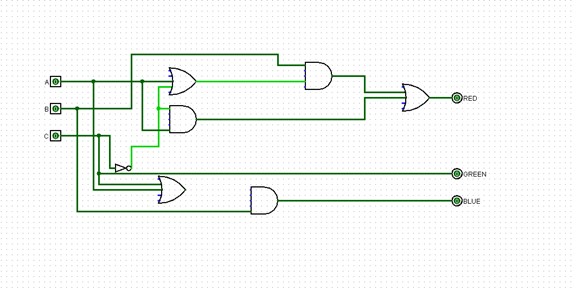
detail the final memory layout.

**a**. There are 3 inputs so there will be 8 combinations... there are 3 outputs 2^3\*3 =

24 bits

**b**. Red = BnotC + SnotC Green = C Blue = AB+ BC 5\*3 = 15 bits

**c**.



3.

Design (step–by–step) and implement (using LogiSim) a 1–bit Arithmetic Logic Unit

(ALU) that will perform the following logical (a) and arithmetic (b) operations:

(a) Logical operations

• NOT b

• a AND b

• a OR b

• a NAND b

• a NOR b

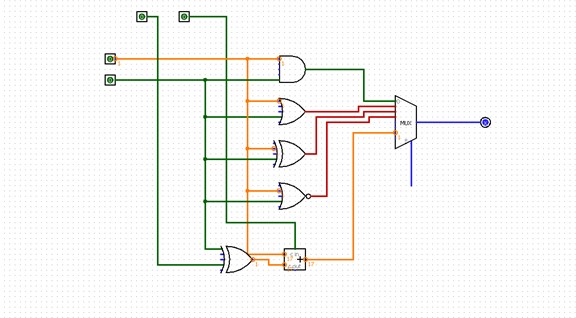
• a XOR b

• a XNOR b

(b) Arithmetic operations

• a + b

• a – b



Only one adder should be used for both Add (+) and Sub (–) operations. (a) Test

the final design with one set of data. (The LogiSim circuit should be active)

4.

Design a 8K × 8 RAM (memory) system, using 1K × 8 RAM chips.

1. Number of Data Bus lines?

There are 8 bus lines.

(b) Number of Address Bus lines?

2N= 1024\*8

n=2^13

13

(c) Draw and briefly explain the overall memory architecture layout.

There are 8 address lines represented by 3 bits as followed

000,001,010,011,100,101,110,111

|  |
| --- |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |
| 1K\*8 |