

**Problem 1:**

**Information Technology**

Instructor: Dr. G.E. Antoniou

Day, Month, Year

Day

CSIT\_230, 03SP

Department of CSIT

Assessment

Module-4

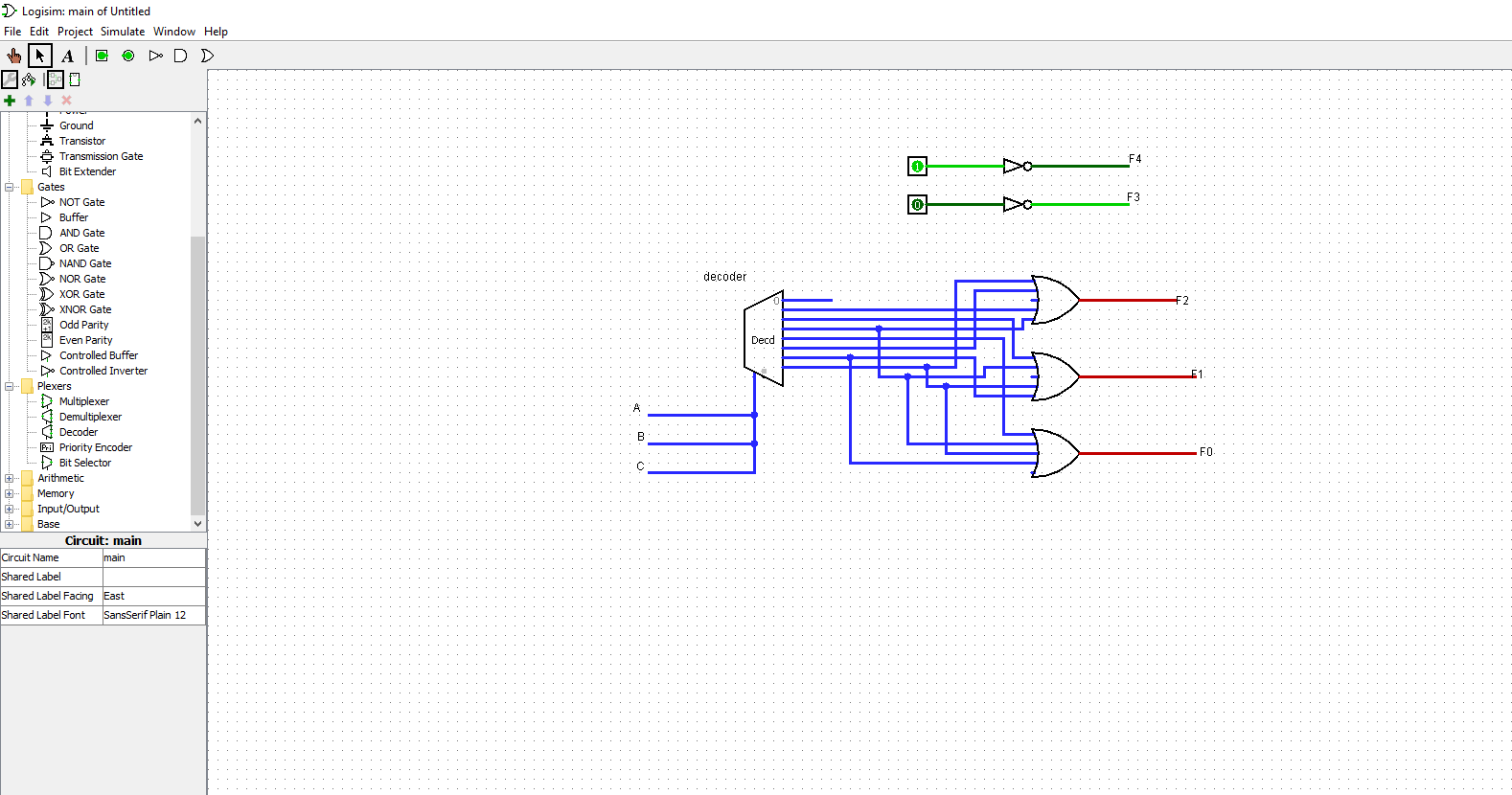
Rana, Karan (name)

Design a digital logic circuit as a Read Only Memory (ROM) [Decoder plus OR gates].

A ROM accepts a three–bit number and generates an output binary number equal to

four times the input number.

1. What is the size (number of bits) of the initial (unsimplified) ROM ?
2. What is the size (number of bits) of the final (simplified) ROM ?
3. Show in detail the final memory layout.

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**Problem 2:**

Design a digital logic circuit as a Read Only Memory (ROM) [Decoder plus OR gates]:

Three light–emitting diodes (LEDs) [one Red, one Green, one Blue] turn on when a

number 0–7 is passed through. Red turns on with even numbers, green turns on with

odd numbers, blue turns on with multiples of 3. Zero means they are all off, seven

means they are all on.

1. What is the size (number of bits) of the initial (unsimplified) ROM ?

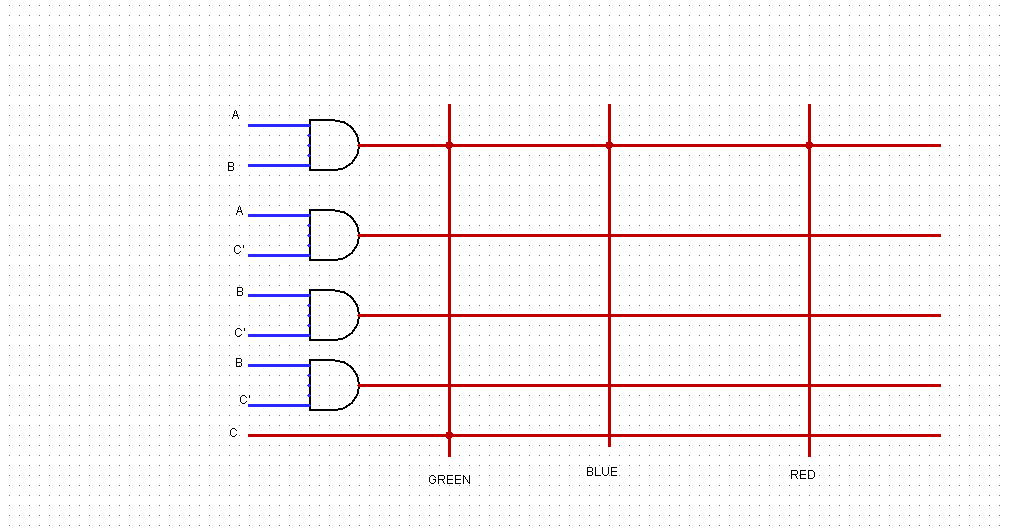
3 inputs so the combination will be 23 = 8

Because there are 3 inputs there will be 3 outputs

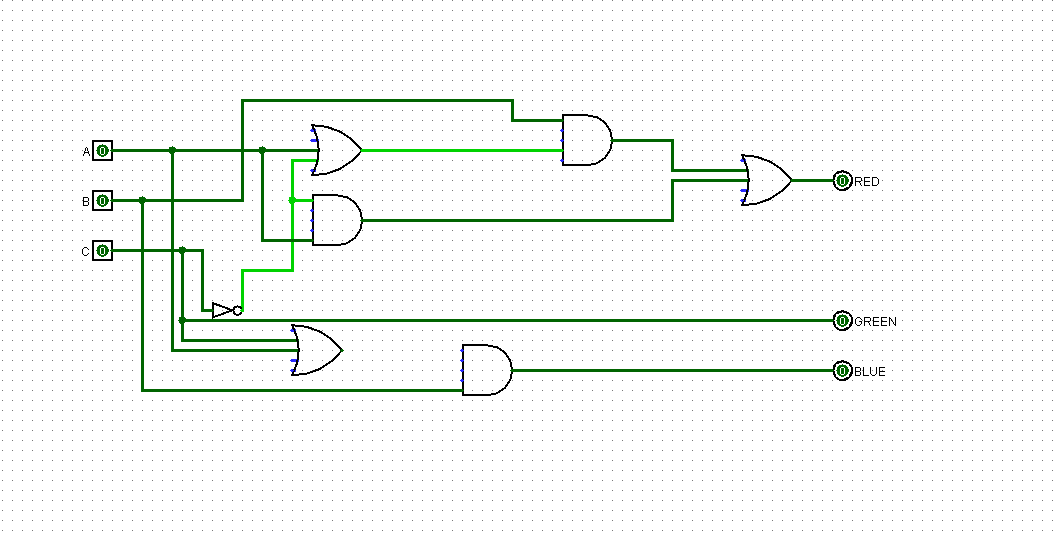
23 \* 3 = 24

1. What is the size (number of bits) of the final (simplified/smallest size) ROM ?

5\*3 =15



(c) Show in detail the final memory layout.



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**Problem 3:**

Design (step–by–step) and implement (using LogiSim) a 1–bit Arithmetic Logic Unit

(ALU) that will perform the following logical (a) and arithmetic (b) operations:

(a) Logical operations

• NOT b

• a AND b

• a OR b

• a NAND b

• a NOR b

• a XOR b

• a XNOR b

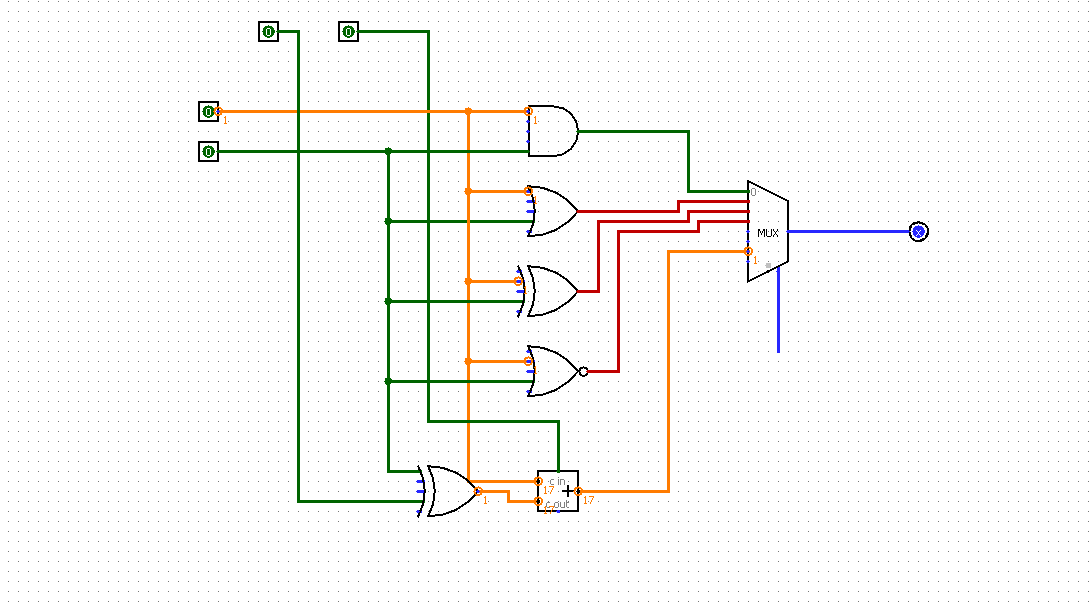
(b) Arithmetic operations

• a + b

• a - b

Only one adder should be used for both Add (+) and Sub (–) operations.

(a) Test the final design with one set of data. (The LogiSim circuit should be active)

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**Problem 4:**

Design a 8K × 8 RAM (memory) system, using 1K × 8 RAM chips.

1. Number of Data Bus lines?

We know that there are 8 RAM chips.

1. Number of Address Bus lines?

1k = 1024

1024\*8

213

There are 13 bus lines

(c) Draw and briefly explain the overall memory architecture layout.

|  |
| --- |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |
| 1k\*8 |