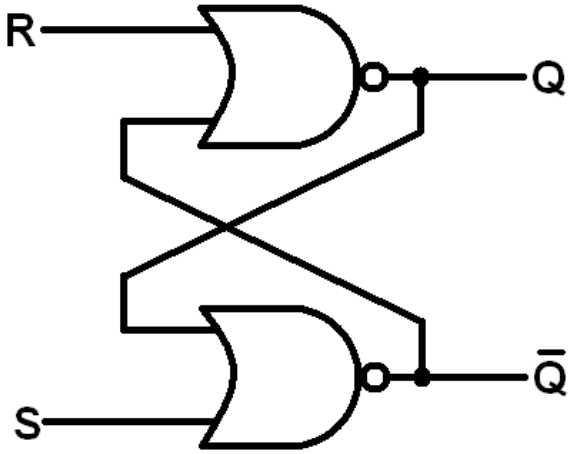
## 6. 1-Bit Memory Element

The memory element uses D-flip flop to store 1 bit data in memory.

**RS Latch:**

Block Diagram:

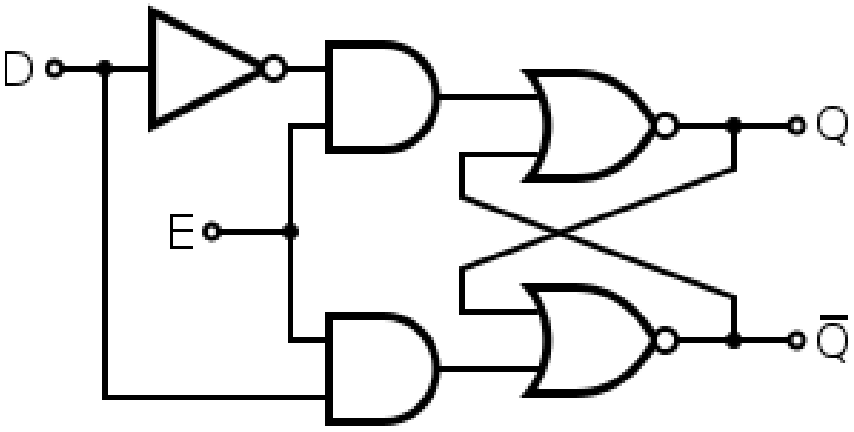



Verilog Code:

```
module SR (output reg q, output reg qn, input r, input s);     //SR-latch
        always @(q, qn, r, s) begin
                q <= ~ (qn | r);        //NOR gate SR-latch
                qn <= ~ (q | s);
        end
endmodule
```

**D-FF using RS Latch:**

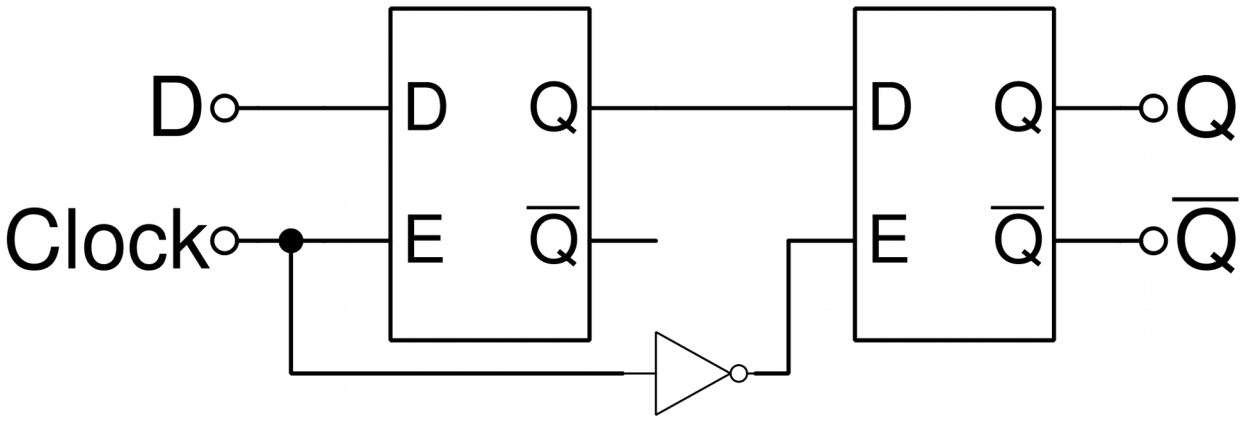
Block Diagram:



Verilog Code:

```
module D (output q, output qn, input d, input clk);            //D-latch
       reg r, s;
       SR SR1 (q, qn, r, s);
       always @ (r, s, d, clk) begin
                r <= (~ d) & clk;
                s <= d & clk;
       end
endmodule
```

**D flip-flop using master slave D Latch:**




Verilog Code:

File: **Dff.v**

```
/*
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       15 October 2018
*/

module Dff (output q, output  qn, input d, input clk, input res);
       reg clkn;
       wire qi, qni;
       wire new_d;
       assign new_d = d & res;
       D inst1 (qi, qni, new_d, clkn);          // D-latch 1
       D inst2 (q, qn, qi, clk);                // D-latch 2
       // complement of clock
       always @ (clk) begin
                clkn <= ~clk;
       end
endmodule
```

Explanation:

Using the above block diagrams each module is coded and used as blocks in other modules. It helps to store 1 bit data in memory along with an active low reset signal. The master slave configuration allows the sequential circuit to be positive edge triggered.

Output: