2-b. Encoder

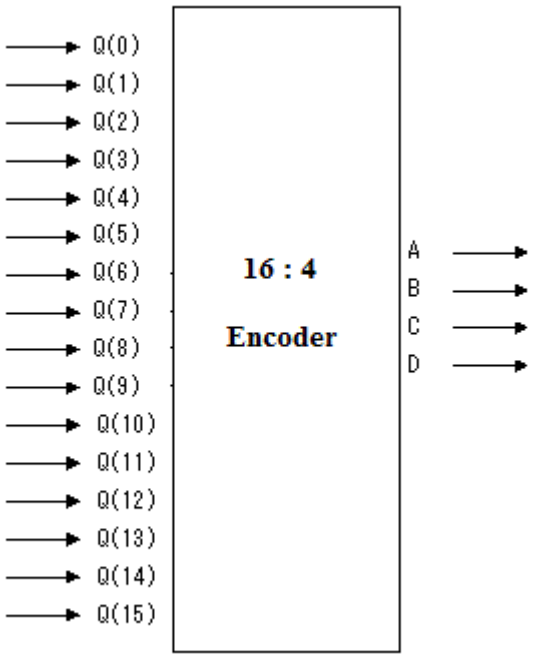
16-bit input indicating decimal value is encoded to give corresponding 4 bit binary value

Truth table:

OUTPUTS				INPUTS															
A	B	C	D	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}	X_{13}	X_{14}	X_{15}
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The subscript of the input variables give the corresponding decimal values of the input.

Block Diagram:



Verilog Code :

File: encoder.v

```
/*
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        15 October 2018
*/

module encoder (output reg [0:3] out, input [0:15] in);
        always @ (in) begin
                case (in)       //switch to give 4-bit output corresponding to 16-bit input
                        16'b0000000000000001    : out = 4'b0000;
                        16'b0000000000000010    : out = 4'b0001;
                        16'b0000000000000100    : out = 4'b0010;
                        16'b0000000000001000    : out = 4'b0011;
                        16'b0000000000010000    : out = 4'b0100;
                        16'b0000000000100000    : out = 4'b0101;
                        16'b0000000001000000    : out = 4'b0110;
                        16'b0000000010000000    : out = 4'b0111;
                        16'b0000000100000000    : out = 4'b1000;
                        16'b0000001000000000    : out = 4'b1001;
                        16'b0000010000000000    : out = 4'b1010;
                        16'b0000100000000000    : out = 4'b1011;
                        16'b0001000000000000    : out = 4'b1100;
                        16'b0010000000000000    : out = 4'b1101;
                        16'b0100000000000000    : out = 4'b1110;
                        16'b1000000000000000    : out = 4'b1111;
                        default                 : out = 4'bxxxx;
                endcase
        end
endmodule
```

Explanation:

Using behavioral modelling for the encoder unit, the behaviour of the circuit is coded using switch cases for all possible input variable combinations, giving corresponding output variable values.

Output:

```
VCD info: dumpfile tb_encoder.vcd opened for output.
                   0: input: 0000000000000001 output: 0000
                  10: input: 0000000000000010 output: 0001
                  20: input: 0000000000000100 output: 0010
                  30: input: 0000000000001000 output: 0011
                  40: input: 0000000000010000 output: 0100
                  50: input: 0000000000100000 output: 0101
                  60: input: 0000000001000000 output: 0110
                  70: input: 0000000010000000 output: 0111
                  80: input: 0000000100000000 output: 1000
                  90: input: 0000001000000000 output: 1001
                 100: input: 0000010000000000 output: 1010
                 110: input: 0000100000000000 output: 1011
                 120: input: 0001000000000000 output: 1100
                 130: input: 0010000000000000 output: 1101
                 140: input: 0100000000000000 output: 1110
                 150: input: 1000000000000000 output: 1111
```