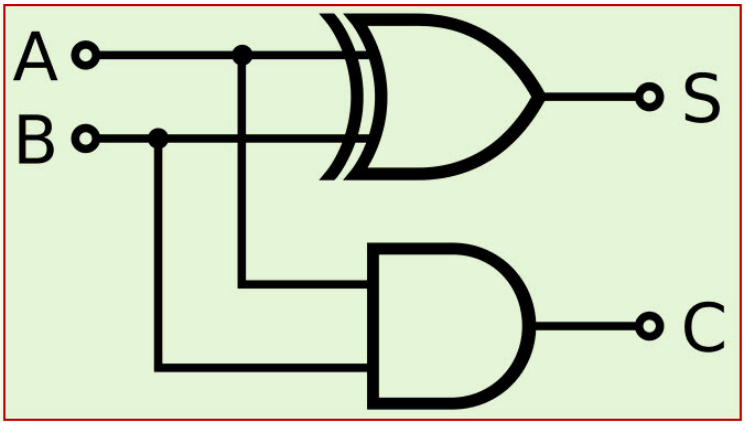
3. Half Adder

The circuit is used to add two 1-bit values to give corresponding 1-bit sum and carry outputs.

Truth table:

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Block Diagram:



Verilog Code:

File: **halfAdder.v**

```
/*
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       15 October 2018
*/


module halfAdder (output reg sum, output reg carry, input op1, input op2);
       always @ (op1 or op2) begin            //if inputs are 0 and 0, thread is not executed
              sum = op1 ^ op2;                // sum bit of two operands
              carry = op1 & op2;              // carry bit of two operands
       end
endmodule
```

Explanation:

The above block diagram is coded in the module using data flow modelling.

Output:

```
VCD info: dumpfile tb_halfAdder.vcd opened for output.
Sum of 1 and 1
Sum = 0
Carry = 1

Sum of 1 and 0
Sum = 1
Carry = 0

Sum of 0 and 1
Sum = 1
Carry = 0

Sum of 0 and 0
Sum = 0
Carry = 0
```