2-a. Decoder

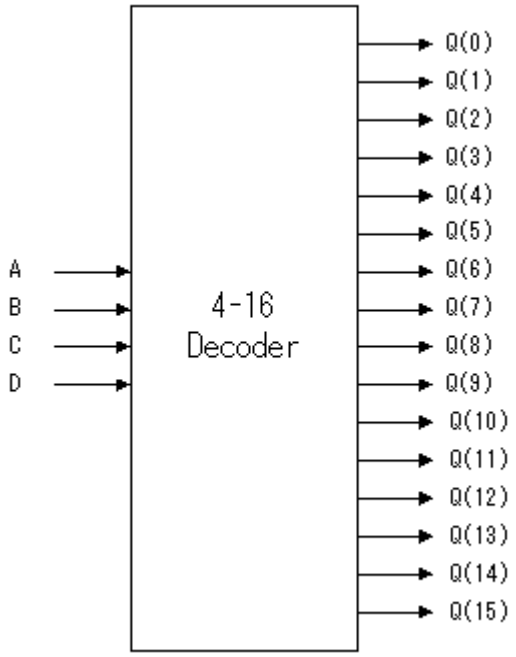
A 4-bit binary input is decoded to give corresponding decimal values.

Truth table:

INPUTS				OUTPUTS															
A	B	C	D	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}	X_{13}	X_{14}	X_{15}
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

The subscript of the output variables give the corresponding decimal values of the input.

Block Diagram:



Verilog Code :

File: **decoder.v**

```
/*
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*/

module decoder (output reg [0:15] out, input [0:3] in);
       always @ (in) begin                    //if not used case is read as module
                case (in)                     //switch to match 4-bit input to 16-bit output
                        4'b0000 : out = 16'b0000000000000001;
                        4'b0001 : out = 16'b0000000000000010;
                        4'b0010 : out = 16'b0000000000000100;
                        4'b0011 : out = 16'b0000000000001000;
                        4'b0100 : out = 16'b0000000000010000;
                        4'b0101 : out = 16'b0000000000100000;
                        4'b0110 : out = 16'b0000000001000000;
                        4'b0111 : out = 16'b0000000010000000;
                        4'b1000 : out = 16'b0000000100000000;
                        4'b1001 : out = 16'b0000001000000000;
                        4'b1010 : out = 16'b0000010000000000;
                        4'b1011 : out = 16'b0000100000000000;
                        4'b1100 : out = 16'b0001000000000000;
                        4'b1101 : out = 16'b0010000000000000;
                        4'b1110 : out = 16'b0100000000000000;
                        4'b1111 : out = 16'b1000000000000000;
                        default : out = 16'b0000000000000000;
                endcase
       end
endmodule
```

Explanation:

Using behavioral modelling for the decoder unit, the behaviour of the circuit is coded using switch cases for all possible input variable combinations giving corresponding output variable values.

Output:

```
VCD info: dumpfile tb_decoder.vcd opened for output.
input: 0000 output: 0000000000000001
input: 0001 output: 0000000000000010
input: 0010 output: 0000000000000100
input: 0011 output: 0000000000001000
input: 0100 output: 0000000000010000
input: 0101 output: 0000000000100000
input: 0110 output: 0000000001000000
input: 0111 output: 0000000010000000
input: 1000 output: 0000000100000000
input: 1001 output: 0000001000000000
input: 1010 output: 0000010000000000
input: 1011 output: 0000100000000000
input: 1100 output: 0001000000000000
input: 1101 output: 0010000000000000
input: 1110 output: 0100000000000000
input: 1111 output: 1000000000000000
```