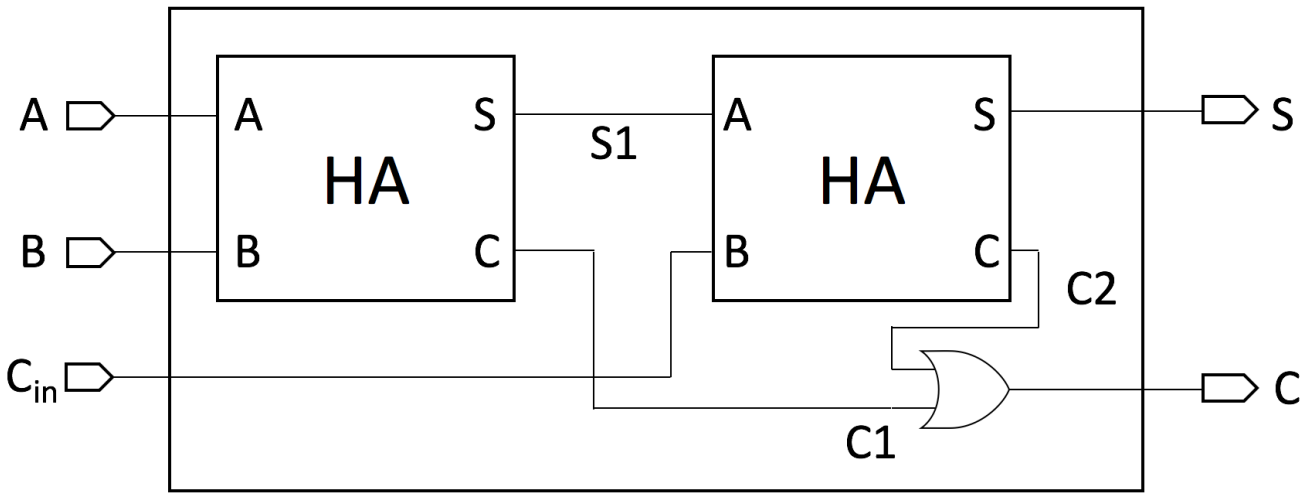
4. Full Adder

The circuit is used to add three 1-bit values to give corresponding 1-bit sum and carry outputs.

Truth table:

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Block Diagram:



Verilog Code:

File: **fullAdder.v**

```
/*
       K Rahul Reddy   17CO119
       Sushruth V      17CO148
       15 October 2018
*/

`include "halfAdder.v"

module fullAdder (output sum, output carry, input op1, input op2,input op3);
       wire tempSum,t1carry,t2carry;
       halfAdder inst1 (tempSum,t1carry,op1,op2);      // sum of first two bits
       halfAdder inst2 (sum,t2carry,tempSum,op3);      // calculating the sum
       assign carry = t1carry|t2carry;                 // calculating the carry
endmodule
```

Explanation:
The above block diagram is coded in the module using data flow modelling. The module simulates a full-adder implemented using two half-adders.

Output:

```
VCD info: dumpfile tb_fullAdder.vcd opened for output.
Sum of 1, 1 and 0
Sum=0
Carry=1

Sum of 1, 0 and 0
Sum=1
Carry=0

Sum of 0, 1 and 0
Sum=1
Carry=0

Sum of 0, 0 and 0
Sum=0
Carry=0

Sum of 1, 1 and 1
Sum=1
Carry=1

Sum of 1, 0 and 1
Sum=0
Carry=1

Sum of 0, 1 and 1
Sum=0
Carry=1

Sum of 0, 0 and 1
Sum=1
Carry=0
```