64-bit Integer ALU Design.

Extending the 1-bit ALU to support the same tasks on 64-bits. One change done is the passing the carry bit generated during addition/subtraction to the next 1-bit ALU cycle.

OP Codes:

4-bits

bit 1 : neg_A bit 2 : neg_B

bit 3,4 : indicate component

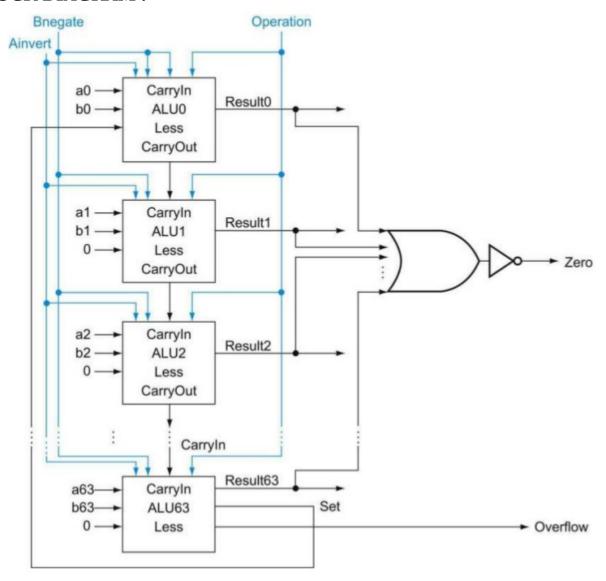
 $00 \Rightarrow and$

01 => or

 $10 \Rightarrow add$

The main module accepts 4 inputs from the user. The input 1, input 2, carry_in and the opcode.

BLOCK DIAGRAM:



VERILOG CODE:

SAMPLE OUTPUT:

```
Time =
                       Carry In =
Op Code = 0100
Result = 000000<u>000000000</u>3
                                       Zero = 0
                                                               Carry Out = 0
Time = 9
                       Carry In =
Op Code = 0100
Result = 00000000000000001
                                       Zero =
                                                               Carry Out = 0
Time = 10
                       Carry In =
Op Code = 0101
Result = 00000000000000001
                                       Zero =
                                                               Carry Out = 0
Time = 11
Op Code = 0101
                       Carry In =
Result = fffffffffffffd
                                       Zero =
                                               0
                                                               Carry Out = 0
Time = 12
                       B =
Carry In =
Op Code = 0110
Result = fffffffffffffd
                                       Zero =
                                                               Carry Out = 0
Time = 13
Op Code = 0110
                       Carry In =
Result = fffffffffffffff
                                       Zero =
                                                               Carry Out = 0
Time = 14
                       B =
Carry In =
Op Code = 0111
Result = ffffffffffffff
                                       Zero = 0
                                                               Carry Out = 0
```