Lab 09 (All Sections) Prelab: Single Cycle Processor and Control Unit

Name:

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Sign the following statement:

On my honor, as an Aggie, I have neither given nor received unauthorized aid on this academic work

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1 Objective

In this lab, you will implement the main *control unit* of the MIPS processor. You should know the details of the MIPS single cycle processor and control unit from the textbook.

2 Introduction

If the data path is the "brawn" of a processor, then the control unit is the "brain" of a processor. It generates signals that control the components in the data path, such as multiplexers, ALU, register file, memory units, etc.

3 Questions

1. Add the control unit for the given MIPS data path that supports R-type, load/store and branch instructions only to Figure 1 (not for submission).
2. **Signal stuck-at-0-fault**: A *stuck-at-0-fault* is a hardware fault where the signal is always 0, regardless of what it should be. Describe the effect of the following

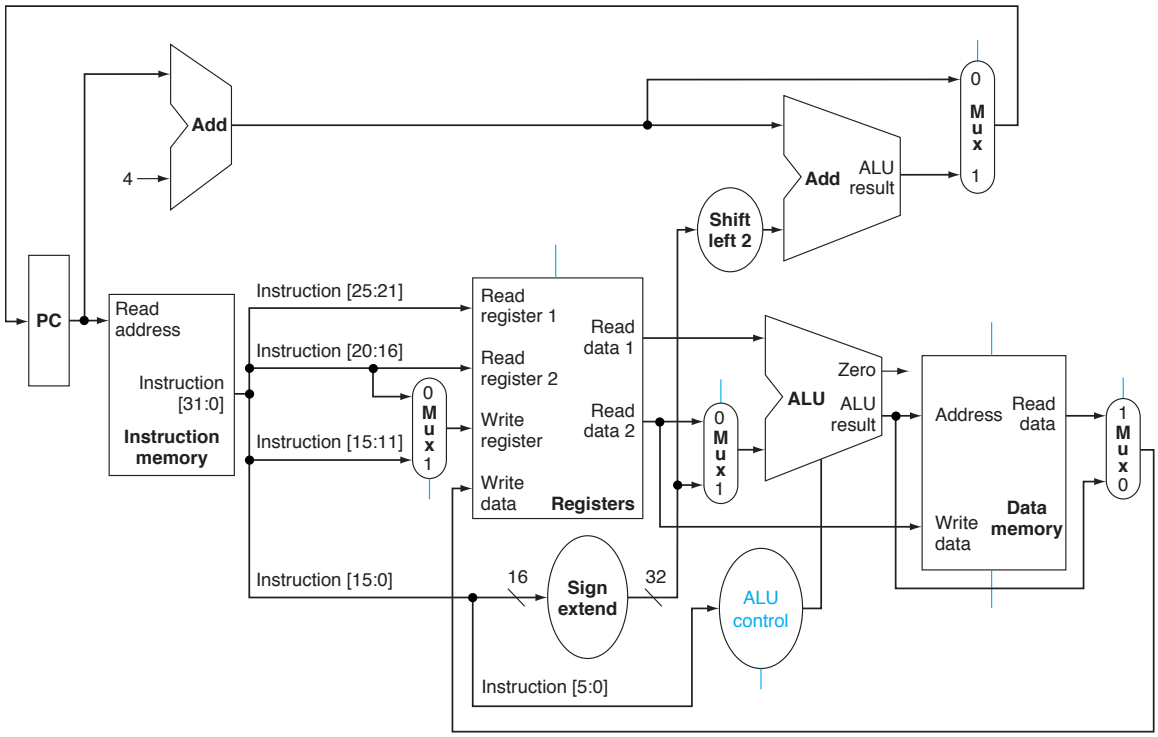

Fig. 1: Single Cycle Datapath that supports R-type, load/store word and branch instructions only.

signal *stuck-at-0-fault* in the single cycle data path that supports R-type, lw/sw and branch instructions only. (Figure 1). Which instructions, if any, will not work correctly? Explain why.

(a) RegWrite = 0

All R-type instructions won't work because that can't write results to a register file. lw wouldn't be able to operate either.

(b) Branch = 0

beq won't work, because even if the condition is satisfied the jump can't occur.

(c) MemRead = 0

lw wouldn't work. Data couldn't be read from memory.

(d) MemWrite = 0

contrary to the previous question, sw wouldn't work, because data would not be able to be written to memory.

(e) ALUop[3:0] = 0000

r format instructions wouldn't work with the exception of subtract. beq might not work because the ALU might make the jump go to the wrong branch.

3. **Signal stuck-at-1-fault**: A *stuck-at-1-fault* is a hardware fault where the signal is always 1, regardless of what it should be. Describe the effect of the following signal *stuck-at-1-fault* in the single cycle data path that supports R-type, lw/sw and branch instructions only (Figure 1). Which instructions, if any, will not work correctly? Explain why.

(a) RegWrite = 1

sw and beq wouldn't be able to write register file. They would overwrite a random register with random data or a target address.

(b) Branch = 1

beq is the only instruction that could still work. If an r-type instruction produces 0 output, it will be branched to the target address.

(c) MemRead = 1

sw will not work correctly because memread and memwrite could simultaneously be 1.

(d) MemWrite = 1

contrary to the last question, only sw could work correctly, because the rest of the instructions would continually store data into memory.

(e) ALUop[3:0] = 1111

no instructions would work correctly.

4. As you know the Control unit takes the 6-bit opcode as input and generates the control signals as in Figure 2.

   Fill in the following truth table:

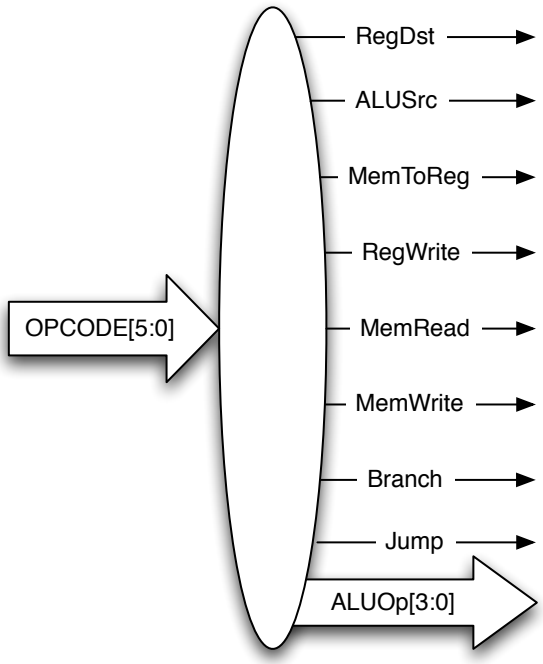

Fig. 2: Opcode Control

Instruction class	OPCODE[5:0]	RegDst	ALUSrc	MemToReg	RegWrite	MemRead	MemWrite	Branch	Jump	ALUOp[3:0]
R-format	000000	1	0	0	1	0	0	0		1111
Load Word	100011	0	0	1	1	1	0	0	0	0010
Store Word	101011	X	1	X	0	0	1	0	0	0010
Branch (BEQ)	000100	X	1	X	0	0	0	1	0	0010
Jump	000010	X	X	X	0	0	0	X	1	XX
ADDI	001000		1	0	1	0	0	0	0	0010
ADDIU	001001		1	0	1	0	0	0	0	1000
ANDI	001100		1	0	1	0	0	0	0	0000
LUI	001111		1	0	1	0	0	0	0	1110
ORI	001101		1	0	1	0	0	0	0	0001
SLTI	001010		1	0	1	0	0	0	0	0111
SLTIU	001011		1	0	1	0	0	0	0	1011
XORI	001110		1	0	1	0	0	0	0	1010