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REVIEWS

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A review on performance comparison of advanced MOSFET structures below 45 nm technology node

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Abstract: CMOS technology is one of the most frequently used technologies in the semiconductor industry as it can be successfully integrated with ICs. Every two years the number of MOS transistors doubles because the size of the MOSFET is reduced. Reducing the size of the MOSFET reduces the size of the channel length which causes short channel effects and it increases the leakage current. To reduce the short channel effects new designs and technologies are implemented. Double gate MOSFET design has shown improvement in performance as amplifiers over a single MOSFET. Silicon-based MOSFET design can be used in a harsh environment. It has been used in various applications such as in detecting biomolecules. The increase in number of gates increases the current drive capability of transistors. GAA MOSFET is an example of a quadruple gate around the four sides of channel that increases gate control over the channel region. It also increases effective channel width that improves drain current and reduces leakage current keeping short channel effects under limit. Junctionless MOSFET operates faster and uses less power with increase in ON-state current leading to a good value of I_{ON}/I_{OFF} ratio. In this paper, several gate and channel engineered MOSFET structures are analyzed and compared for sub 45 nm technology node. A comparison among different MOSFET structures has been made for subthreshold performance parameters in terms of I_{OFF}, subthreshold slope and DIBL values. The analog/RF performance is analyzed for transconductance, effective transistor capacitances, stability factor and critical frequency. The paper also covers different applications of advance MOSFET structures in analog/digital or IoT/ biomedical applications.

Key words: MOSFET; junctionless; RF; biosensor; DIBL; double gate

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1. Introduction

A conventional MOSFET maintains its performance beyond 100 nm. Several adverse effects arise due to reduction in channel length reduction depending on scaling trends[1]. Due to the scaling of microelectronic technologies, the electrical performance of the device and effects of short channels should be reduced[2]. New structures are designed such as double-gate MOSFET[3], tri-gate MOSFET, multi-gate MOSFET to compensate the effects of short channel lengths. These MOSFETs were proposed as an alternative to bulk MOSFET beyond 45 nm. Double gate MOSFET has many advantages over the bulk MOSFET[1, 2]. It reduces the short channel effects, junction capacitance and provides dielectric isolation SOI (silicon on insulator) is also used in CMOS technology due to its high-speed performance and low power consumption[4]. Surround gates used in MOSFET allow more channel width which increases the drive current[5]. Capacitance model of material engineered CGT has also been proposed for improvement of short channel effects[6]. Square GAA MOSFET was proposed to be used in the device simulator and can easily be incorporated in compact models[7]. The gate all around junctionless MOSFET has been designed for high RF performance[8]. A TM-DG SOI MOSFET improves RF performance, linearity and analog performance[9]. A thermal model is proposed to predict the transfer of phonon in tri-gate SOI MOSFET and 3D MOSFET[10]. DG MOSFET has been used to design amplifier for better control of short channel effects[11]. JLDG MOSFET was proposed which reduces the short channel effects significantly[12]. A CSDG MOSFET was designed to store more energy and increase the current flow between source to drain[13].

In this paper, a comparison is made among different advance MOSFET structures on the basis of their ON and OFF-state performance. The ON and OFF-state performance are the deciding factor in future scaling trends of new transistor structures. The design of MOSFET structures also depends on different applications such as digital circuit, memory, analog/RF and biomedical applications. The paper describes application based MOSFET designs by exploring DC and AC performance parameters. Several MOSFET designs are implemented to check their circuit performance using circuit simulators available in TCAD tool. Such a prefabrication transistor structure and circuit design analysis plays an important role in achieving the desired performance and also to reduce failure or defect in the fabricated sample.

2. Performance parameter

In general, the MOSFET structures are evaluated on the basis of their subthreshold performance and analog/RF performance. The important MOSFET parameters are needed to be discussed before any comparison among different MOSFET structures.

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2.1. Subthreshold performance parameters

The region of operation before MOSFET channel inversion is known as the subthreshold region. The subthreshold parameters are a deciding factor to obtain a desired and reliable MOSFET performance.

2.1.1. Threshold voltage

The minimum amount of gate to source voltage required for channel inversion is known as MOSFET threshold voltage (V_T). The value of threshold voltage depends mainly on surface potential which is the voltage of MOSFET capacitor surface (top layer of polysilicon or metal above the oxide) and voltage in the bulk of MOSFET.

2.1.2. OFF-state current

When the voltage of the gate is less than the threshold voltage the MOSFET is considered to be in OFF-state. However, in OFF-state there is a flow of current due to minority charge carriers between the drain and source. This current is known as subthreshold current.

2.1.3. ON-state current

When the voltage of the gate is more than the threshold voltage of the MOSFET. The MOSFET is said to be in ON-state. The flow of current in this state is known as ON current denoted by Ion. The movement of electrons takes place from source to drain.

2.1.4. DIBL (drain induced barrier lowering)

It is a short channel effect in which threshold voltage reduces originally at high drain voltage. When the length of the channel is short drain it is close enough to the gate, at high drain voltage the bottleneck opens and the transistor turns on prematurely. The value of DIBL should be as low as possible to obtain ideal output characteristic of MOS transistors reducing threshold voltage variations due to drain field effect on channel potential.

$$\mathrm{DIBL} = \frac{V_{\mathrm{Th}}^{\mathrm{DD}} - V_{\mathrm{Th}}^{\mathrm{low}}}{V_{\mathrm{DD}} - V_{\mathrm{D}}^{\mathrm{low}}}. \tag{1}$$

2.1.5. Subthreshold slope (SS)

In the subthreshold region, the gate terminal controls the drain current and the current is exponentially decreased. The slope of the drain current plot and gate voltage with drain, bulk and source voltages fixed gives subthreshold slope. A suitable value of subthreshold slope (~60 mV/decade) is required to limit the heating effect in short channel devices. The subthreshold slope can be expressed as:

$$\mathrm{SS_{th}} = \ln(10)\frac{kT}{q}\left(1 + \frac{C_{\mathrm{d}}}{C_{\mathrm{ox}}}\right). \tag{2}$$

2.2. Analog/RF performance parameters

The analog and RF performance mainly depends on transconductance, transistor capacitances, stability factor and cutoff frequency, etc.

2.2.1. Transconductance

Transconductance is the ratio of drain current variation with respect to the gate voltage of transistor over a small interval of time in the drain current versus gate voltage curve. It is represented as g_m[10]. The higher value of transconductance is required to obtain a suitable range of amplifier gain.

$$g_{\mathrm{m}} = \frac{2I_{\mathrm{DS}}}{|V_{\mathrm{P}}|}\left(1 - \frac{V_{\mathrm{GS}}}{V_{\mathrm{P}}}\right). \tag{3}$$

2.2.2. Junction capacitance

Due to the depletion of charge between the source/drain and substrate the junction capacitances in MOSFET is formed. The charged depletion is changed according to the source/drain voltage. When the voltage of the gate exceeds the threshold voltage there is a formation of the channel at the surface. The junction capacitances are deciding factors for small signal analysis of transistor in RF range of frequencies.

2.2.3. Stability factor

The stability factor (K) mainly depends on two-port equivalent circuit parameters of MOS transistors. It decides the conditional or unconditional stability of transistors in RF range of frequencies. The stability factor can be expressed as[14]:

$$K = \frac{2\mathrm{Re}[Y_{11}]\mathrm{Re}[Y_{22}] + \mathrm{Re}[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|}. \tag{4}$$

Here, Y_{11} and Y_{22} are input and output admittance parameters at port 1 and 2 respectively. The Y_{12} and Y_{21} are called as transfer admittances.

2.2.4. Critical frequency

The critical frequency (f_k) is essential for a small signal transistor model and also important to maintain a suitable AC transistor gain and frequency bandwidth. The critical frequency can be calculated at stability factor $K = 1$. The critical frequency mainly depends on MOSFET capacitance (C_{gs}, C_{gd}, and C_{ds} etc.) and other parasitic capacitances. The critical frequency can be expressed as[15]:

$$f_{\mathrm{k}} \cong \frac{f_{\mathrm{T}}N}{\sqrt{g_{\mathrm{ds}}g_{\mathrm{m}}R_{\mathrm{gs}}M^2 + NM\left(g_{\mathrm{m}}R_{\mathrm{gd}} + 1\right)}}. \tag{5}$$

Here, f_T, g_{ds}, R_{ds} and R_{gs} are the frequency at unity gain, output conductance, drain to source and gate to source resistances respectively. Also, the M and N values are calculated in terms of C_{gs} and C_{gd} respectively.

3. Device structure and dimensions

Sarkar *et al.*[6] presented a paper on the effect of engineering on DG MOSFET (Fig. 1). In this paper, a fully depleted tri material double gate MOSFET is used. Improvement in the RF performance, linearity and analog performance compared to the DM DG MOSFET and single material DG MOSFET. The structure is designed in 35 nm CMOS technology. In n-MOSFET, three different gate materials of different work functions are chosen. The work function of the materials are Φ_{M1} = 5.0 eV, Φ_{M2} = 4.75 eV, Φ_{M3} = 4.5 eV.

The material of the gate having the larger work function in place close to the source and the material which is having the lesser work function is placed close to the drain. Polysilicon gates have depletion width of polysilicon and penetration effect of dopant so metal gates are used. The thickness of the Si film is 10 nm and SiO_2 is 2 nm. The concentration of dopant of the source and drain is considered to be 10^{20} cm^{-3}. The ratio of the length of the three material is taken as (L_1 : L_2 : L_3 = 1 : 1 : 0). The doping concentration of the p substrate is taken as 10^{16} cm^{-3}. Djeffal *et al.*[3] presented a paper

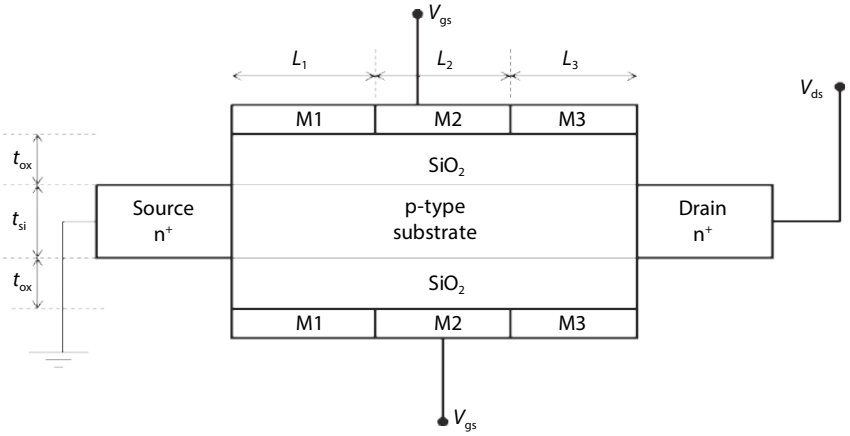

Fig. 1. TM-DG MOSFET structure.

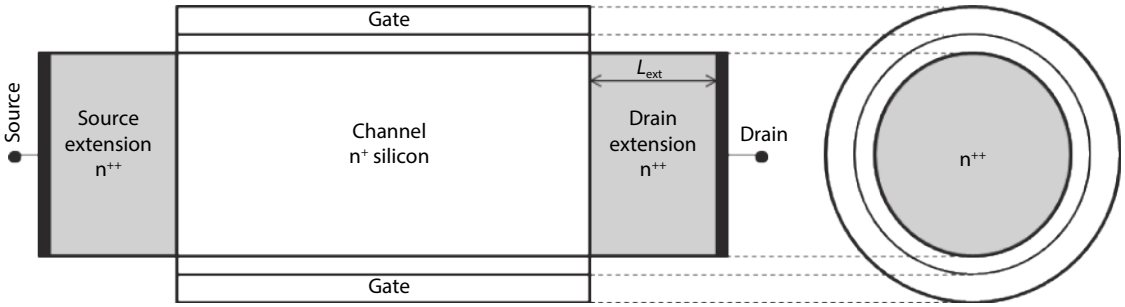

Fig. 2. GAAJ MOSFET with S/D extensions regions.

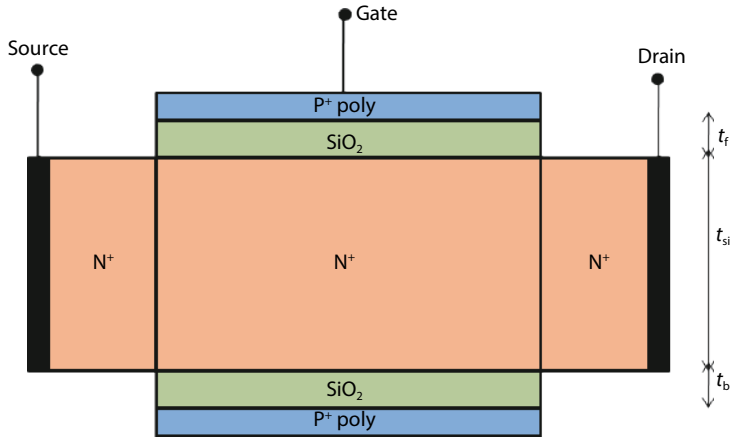

Fig. 3. (Color online) n-type JLDG MOSFET structure.

on gate all around junctionless MOSFET (Fig. 2) with source and drain extension to improve analog and RF performances. In this structure, the source and drain extensions are heavily doped compared to the channel doping. The doping concentration is given as $n^{++}/n^+/n^{++}$. A long channel structure is considered with film thickness of silicon less than 5 nm. The doping concentration $N_d = 10^{18}$ cm^{-3}, the concentration of the extension is taken as $N_{ext} = 10^{19}$ cm^{-3}, $R = 5$ nm, $L = 100$ nm, $t_{ox} = 5$ nm.

By including the heavily doped extensions the drain current improves. The GAAJ MOSFET having extensions has high current when compared to conventional GAAJ. The highly doped regions have increased ion current magnitude by 70%. Abhinav *et al.*[9] have discussed the reliability issues concerning junctionless double gate (JLDG) MOSFET (Fig. 3). In this paper, the gate misalignment and thermal stability between 200 to 500 K have been studied. The gate misalignment in this structure reduces the current which in turn reduces JLDG MOSFET's performance. The front and the back gate alignment effects the performance of the MOSFET. The effect of misalignment occurs due to the shifting of the back gate towards the source or drain side. The misalignment of gate produces non-ideal effects.

The dimensions of device parameters and gate work function is 5.2 eV, the thickness of front gate oxide is 1 nm, the thickness of back gate is 1 nm, the thickness of silicon substrate 5 nm, doping concentration N_D is 3×10^{19} cm^{-3}, length of the channel L is 20 nm. Ouruji *et al.*[16] proposed a double step buried oxide (DSBO) SOI MOSFET (Fig. 4). This structure has both the advantages of bulk MOSFET and SOI structure.

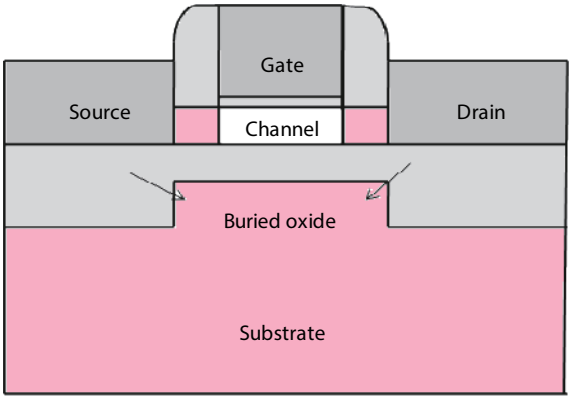

Fig. 4. (Color online) Structure of DSBO-SOI MOSFET.

This structure is designed to reduce the self-heating by changing the shape of buried oxide into a double step shape for reducing the thickness of silicon dioxide. Heat exchange is easily done between the channel to substrate. In this structure there is increase in drain current irrespective of the self-heating effects. The parameter of the device are N^+ source/drain doping is 10^{20} cm^{-3}, N^+ source/ drain extension doping is 10^{19} cm^{-3}, P-type silicon film doping is 10^{15} cm^{-3}, thin-film thickness is 10 nm, raised source/drain thickness is 50 nm, oxide thickness under the source/drain is 100 nm, oxide thickness under the channel is 20 nm, channel length is 30 nm, thickness of gate oxide is 1.5 nm.

Ajay *et al.*[12] presented a paper on two types of gate underlap junctionless double-gate MOSFET (JL DG MOSFET). In this paper, two cases are taken. The first case includes the gate underlap region present at the end portion of source of the JL DG MOSFET's (Fig. 5) channel region. The second case consists of the underlapped gate region is present at the end portion of the drain of the JL DG MOSFET (Fig. 6) channel region. Both types of structure are used to detect biomolecules using dielectric modulation techniques. The charged biomolecules produce an effect on the potential of the surface of JL DG MOSFET. When the biomolecules are positively charged the surface potential move upwards and when the biomolecules are negatively charged the surface potential move downwards. The parameters of the device are, gate length 50 nm, length of the cavity 50 nm, the thickness of cavity 19 nm, thickness of channel of 20 nm, thickness of gate oxide of 10 nm, the doping in source/drain and channel is 1×10^{24} m^{-3}, the thickness of oxide layer in open cavity region is 1 nm.

Kwon *et al.*[17] proposed a paper on silicon-based MOSFET (Fig. 7) for the improvement of operation at high temperatures. The MOSFET is designed for harsh environmental applications[18]. Wide bandgap material is inserted locally between the regions of source and channel for high-temperature operation. The proposed SOI MOSFET structure has buried oxide (BOX) that prevents the leakage of current flowing in the substrate.

The device parameters are the length of gate given as 100 nm, thickness gate oxide is 3 nm, bottom oxide thickness is 10 nm, width of barrier is 10 nm, depth of barrier 75 nm, drain and source doping and substrate are 1×10^{20} and 1×10^{17} cm^{-3}, respectively. Kumar *et al.*[19, 20] proposed a black phosphorus junctionless recessed channel MOSFET (Fig. 8) for RF application using 45 nm technology. Black phosphorus is integrated with the junctionless recessed MOSFET. In this structure drain current increases up to 0.3 mA. The OFF current reduces and there is improvement in subthreshold slope. The black phosphorus material has high ON current and low OFF current. The device parameters are length of gate is 20 nm, length of channel is 44 nm, length of drain and source region is 30 nm, device width is 200 nm, depth of groove is 38 nm, negative junction depth (NJD) is 10 nm, substrate doping is 5×10^{16} cm^{-3}, doping of drain and source is 5×10^{16} cm^{-3}, thickness of physical oxide is 2 nm, work function of metal is 5.16 eV, voltage of gate to source is 1.5 V, voltage of source to drain is 0.2 V.

Djeffal *et al.*[21] proposed a dual material surrounded gate MOSFET of 10 nm for digital applications. The advantages of DMSG MOSFET's (Fig. 9) of 50 nm and multi-objective genetic algorithms (MOGAs) optimization technique has been combined. The MOGAs approach optimizes and improves the electrical behavior of 10 nm DMSG MOSFET. This provides low power consumption and nanoscale high speed digital applications. The formula for DIBL is given as

$$\mathrm{DIBL} = \frac{V_{\mathrm{th}}\,(V_{\mathrm{ds2}} = 0.4\ \mathrm{V}) - V_{\mathrm{th}}\,(V_{\mathrm{ds1}} = 0.1\ \mathrm{V})}{V_{\mathrm{ds2}} - V_{\mathrm{ds1}}}. \quad (6)$$

The device parameters are N_A is 10^{15} cm^{-3}, drain and source doping is 10^{20} cm^{-3}, the length L is 10 nm, the thickness of oxide is 2 nm, silicon thickness is 10 nm, L_1 and L_2 is $L/2$.

Pathak *et al.*[22] proposed a GC-DMGJL MOSFET (graded channel, dual material gate junctionless MOSFET) shown in Fig. 10 for applications in the analog domain. In this paper GC-DMGJL performance is compared with uniform channel dual material gate junctionless (UC-DMGJL) MOSFET. The GC-DMGJL MOSFET gives high drain current and transconductance and also reduces short channel effects. The device consists of high doping area $N_{gd} = 2.5 \times 10^{19}$ cm^{-3} near drain region of the channel, rest of the regions are uniformly doped with $N_d = 2 \times 10^{19}$ cm^{-3}. The ratio of length of the metal L_{M1} : L_{M2} (nm) = 15 : 15. The work function of the metal is given as W_{M1} : W_{M2} (eV) = 5.353 : 4.8. The thickness of oxide is given as 2 nm. Length of the spacer is W_{sp} = 10 nm .The thickness of silicon is T_{si} = 10 nm.

Ajay *et al.*[23] proposed a junctionless metal oxide semiconductor field effective transistor structure (Fig. 11) which is capable of detecting biomolecules such as DNA, enzymes, cells, etc., using dielectric modulation technique. Formation of a nanogap cavity by using the process of gate oxide etching in the channel from both the sides of source and drain. The biomolecules affect the potential of the surface in the channel beneath the nanocavity that bind the SiO_2 layer present in the cavity.

The dimensions of the device are t_{bio} = 9 nm, t_{ox1} = 1 nm, t_{Si} = 10 nm, doping of the source, drain and channel is 1×10^{25} m^{-3}. Length of the cavity is L_1 and L_3 is 25 nm, and L_3 length of the oxide Al_2O_3 is 50 nm. Pang *et al.*[24] proposed a structure of 0.1 μm pocket of n-MOSFETs (Fig. 12) for applications of low voltage. In this structure a pocket region is constructed close to the drain and source region and is heavily doped and at the center of the structure center region is constructed which is lightly doped. This design provides good immunity from short channel effects and is able to meet the spe-

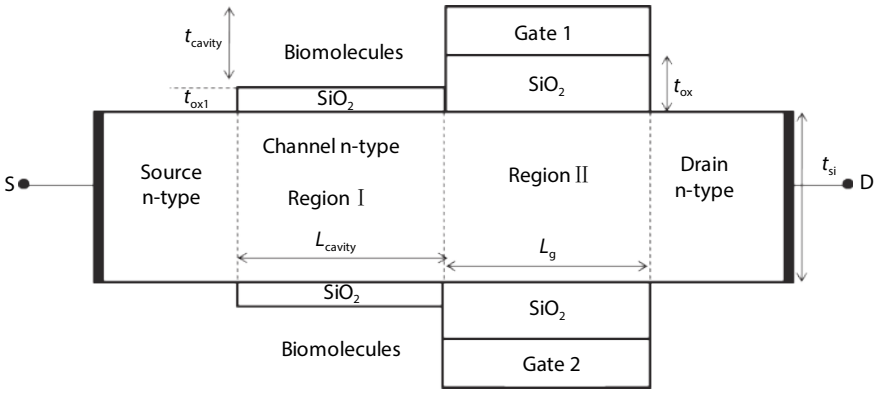

Fig. 5. JL DG MOSFET for underlapping at the source end of the channel region.

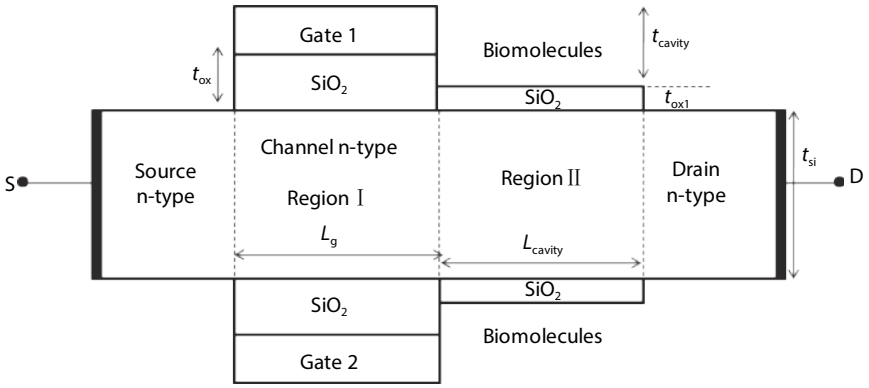

Fig. 6. JL DG MOSFET for underlapping at the drain end of the channel region.

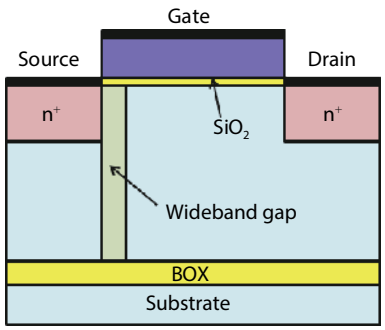

Fig. 7. (Color online) Structure of silicon-based MOSFET.

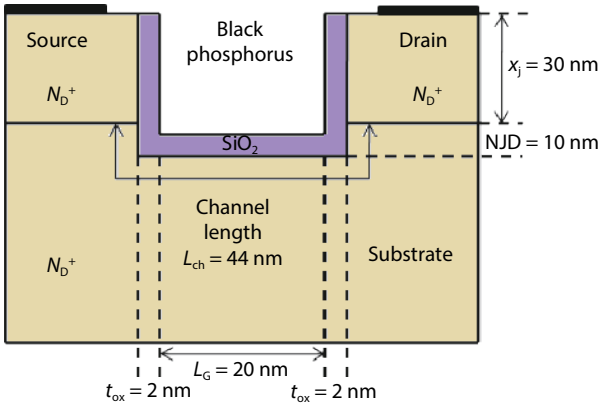

Fig. 8. (Color online) Design of BP JL RC MOSFET.

cifications of OFF current and ON current.

The device parameters are channel length which is 0.1 μm, the thickness of oxide is 4 nm, the junction depth (r_j) is 0.06 μm, the doping concentration of the pocket (N_P) is 1.906×10^{18} cm^{-3} and doping concentration in the center region (N_c) is 2.175×10^{17} cm^{-3}, length of the pocket (L_P) is 0.024 μm. Orouji *et al.*[25] proposed a structure of nanoscale SOI MOSFET which has electrically induced source and drain extensions for suppressing short channel effects length of channel less than 50 nm and also suppresses hot electron effects. The formation of shallow drain and source by fabrication is very difficult but EJ SOI MOSFET (Fig. 13) is able to form virtual drain and source electrically. This structure consists of triple gate, one main gate with two side gates. The biasing of side gates are independent of the main gate. These side gates form inversion layers which further forms virtual drain and source.

The device parameters given are doping of silicon thin layer is 6×10^{16} cm^{-3}, source and drain doping is 5×10^{19} cm^{-3}, the side gates work function is 4.7 eV, the main gate work function is 4.9 eV, thickness of silicon thin layer is 50 nm, thickness of buried oxide is 500 nm, thickness of gate oxide is 2 nm, thickness of barrier diffusion layer is 2 nm, length of main gate is 50 nm and length of total side gate is 50 nm. Pal *et al.*[26] presented a paper on the study of the surrounding gate MOSFET with dual material (Fig. 14) to overcome short-channel effects. The parameters like threshold voltage, potential of the surface, and distribution of electric field are analytically modeled using parabolic approximation method. The comparison between DMSG and SMSG device structures having equal dimensions is taken out in terms of SCE's. The result shows that DMSG MOSFET suppresses (SCEs) more efficiently in comparison with SMSG MOSFET. The formula for DIBL calcu-

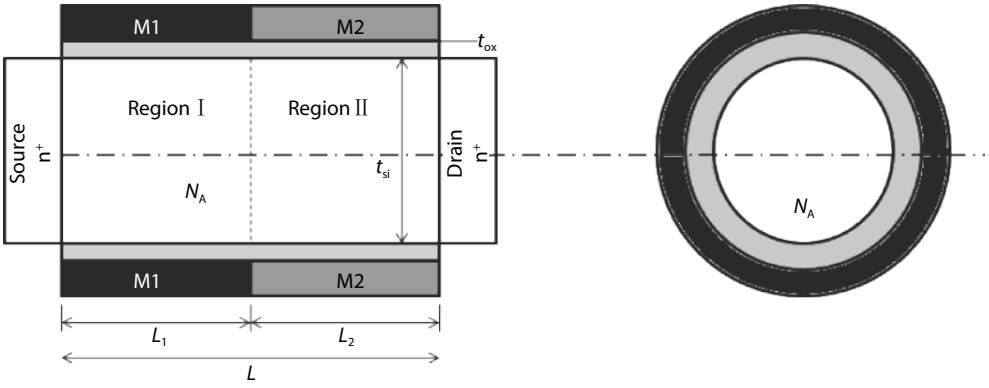

Fig. 9. Structure of DMSG MOSFET.

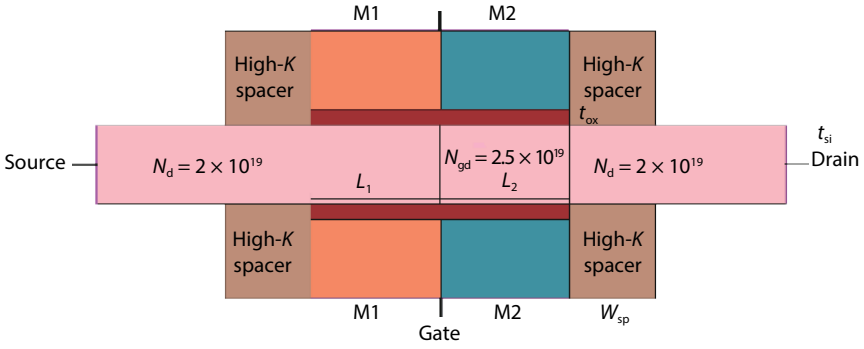

Fig. 10. (Color online) Structure of an n-type GC-DMGJLT.

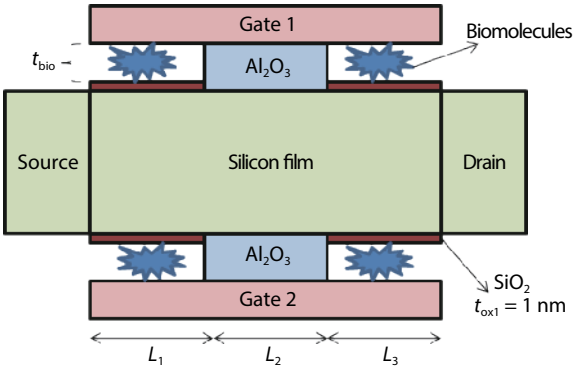

Fig. 11. (Color online) Junctionless MOSFET with a cavity for detecting biomolecules.

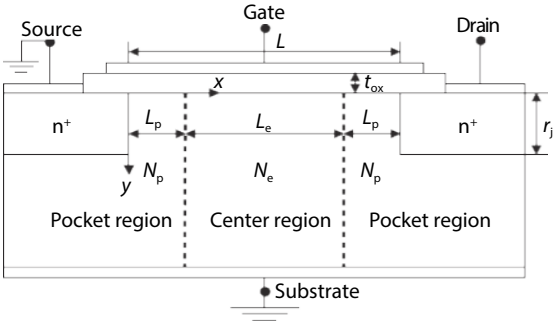

Fig. 12. Structure of a pocket n-MOSFET.

lation is given as

$$\mathrm{DIBL} = \frac{\Delta V_{\mathrm{TH}}}{\Delta V_{\mathrm{DS}}} = \frac{V_{\mathrm{TH1}} - V_{\mathrm{TH2}}}{V_{\mathrm{DS1}} - V_{\mathrm{DS2}}}. \quad (7)$$

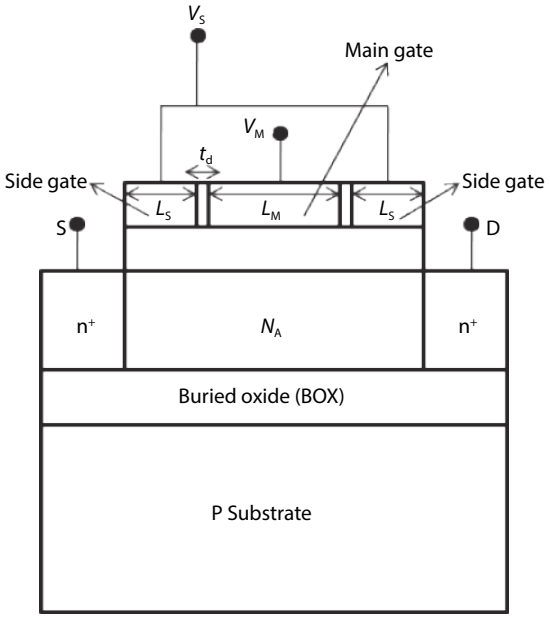

Fig. 13. Structure of EJ-SOI MOSFET.

The work function of gold (Au Φ_{M1} 4.8 eV), work function of cadmium (Cd) is 4.0 eV. The channel doping of p-type is 6×10^{16} cm^{-3}, n^+ source and drain doping region is 5×10^{19} cm^{-3}. Chebaki *et al.*[27] proposed a paper on double-gate junctionless MOSFET (Fig. 15) using engineered gate material and source/drain extensions. This structure is able to produce high drain current and improves RF and analog performance. The figure of merit is also increased compared to the conventional double gate junctionless MOSFET.

The parameters of the devices are doping concentration

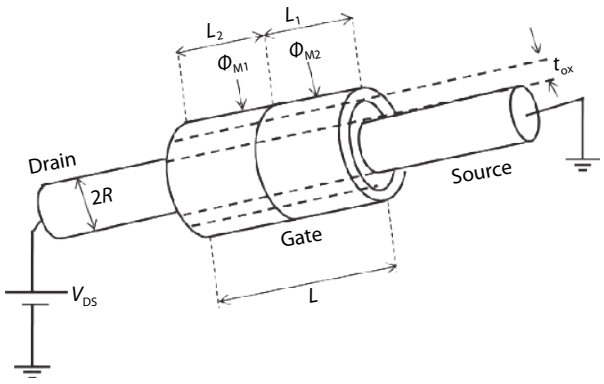

Fig. 14. Design of cylindrical surrounding gate MOSFET using dual material.

N_d is 5×10^{18} cm^{-3}, doping of the extension is 5×10^{19} cm^{-3}, thickness of silicon t_{Si} is 10 nm, L is 100 nm, L_1 and L_2 is $L/2$, the metal (M_1) work function is 5.1 eV, metal (M_2) work function is 4.5 eV. Wang *et al.*[28] proposed a junctionless MOSFET with asymmetrical gate (Fig. 16) to improve the functioning of the device. The device has two gates with a lateral offset[29] between them. In this structure the channel length depends upon the ON and OFF state of the MOSFET. The channel length of the MOSFET during the ON state is equal to the overlap length of the gate, and the channel length during the OFF state is combined length of the two gates minus the overlap length of the gate. This structure increases the I_{ON} to I_{OFF} ratio and decreases the sub-threshold slope and DIBL.

The structure parameters are an oxide (HfO_2) with EOT 1 nm, channel doping is 1×10^{19} cm^{-3}, length of gate is 20 nm, thickness of silicon is 6 nm. Kumar *et al.*[30] proposed a paper on RF performance of the recessed channel with a transparent gate (Fig. 17). The values of transconductance, cut-off frequency, DIBL, and maximum oscillator frequency have been calculated. The outcomes of the structure are compared with the conventional recessed channel MOSFET. The MOSFET gate is made up of indium tin oxide which is a transparent material. The results show that there is increase of cut-off frequency by 42% and oscillator frequency is increased by 132%. Due to the improvement in the gate control the short channel effects are reduced by using the transparent gate material.

The length of the channel (L_G) is 30 nm, width of the device is 200 nm, depth of the groove is 38 nm, junction depth of source and drain is 30 nm, Negative junction depth (NJD) is 10 nm, doping of the substrate (N_A) is 1×10^{16} cm^{-3}, doping of source and drain (N_D) is 1×10^{19} cm^{-3}, thickness of physical oxide (t_{ox}) is 2 nm. SiO_2 permittivity ε_{ox} is 3.9, gate to source voltage (V_{GS}) is 0.7 V, drain to source voltage (V_{DS}) 0.5 V, TGRC-MOSFET work function for (Φ_{ITO}) is 4.7 eV, CRC-MOSFET work function (Φ_M) is 4.2 eV. Mishra *et al.*[31] proposed a structure of junctionless transistor-based 6-T SRAM cell (Fig. 18) using silicon on inductor. This structure reduces the area of the devices and increases performance. There is increase in the I_{ON} current and decrease in I_{OFF} compared to double-gate junctionless. This structure occupies only half the area of the conventional structure. Read and write operation is also improved using the proposed structure. The ratio of I_{ON}/I_{OFF} is 10^6. The area of the of junctionless transistor-based 6-T SRAM cell using silicon on inductor is 6.9 μm^2 and that of conventional structure is 11.3 μm^2.

The dimensions of the structure is gate length 18 nm, T_{ox} 1 nm, T_{Si} channel thickness 10 nm, substrate thickness 10 nm, doping density in substrate regions 1×10^{18} cm^{-3}, doping density channel 1×10^{18} cm^{-3}, work function of gate material 4.9 eV.

Roy *et al.*[32] proposed a short channel junctionless double-gate MOSFET (Fig. 19). This structure does not contain any p-n junction because the doping of the channel is same as that of the drain and source. The RF and analog performance of the structure has been investigated. The voltage of the front and back gate provided are same. The DIBL value obtained is 75.98 mV/V, the sub-threshold slope is 62.32 mV/decade and the I_{ON} and I_{OFF} ratio obtained is 4.86×10^9. From the result it is observed that sub-threshold slope is decreased by 1.61%, the I_{ON} and I_{OFF} ratio is increased by 17.08% and DIBL is decreased by 4.52%. The dimensions of the device are gate work function is 5.2 eV, front gate oxide thickness is 1 nm, back gate thickness is 1 nm, silicon substrate thickness 5 nm, doping concentration N_D is 10^{19} to 4×10^{19} cm^{-3}, channel length L is 20 nm.

Saramekala *et al.*[33] proposed a dual metal gate with a short channel having recessed source and drain silicon on insulator MOSFET (Fig. 20). This device provides high ON current, low DIBL value. The channel region is lightly doped and the drain and source region is heavily doped.

Work-function of control gate (Φ_{M1}) is 4.8 eV (gold), work-function of screen gate (Φ_{M2}) is 4.6 eV (molybdenum), doping of the channel (N_a) is 10^{15} cm^{-3}, doping of source and drain (N_d) is 10^{20} cm^{-3}, doping of substrate (N_{sub}) is 10^{15} cm^{-3}, oxide thickness of channel (t_{ox}) is 1.5–4 nm, thickness of buried (t_{box}) is 100–300 nm, thickness of recessed is (t_{rsd}) 30–100 nm, length of recessed (d_{box}) is 3 nm, length of the channel (L) is 30–300 nm.

4. Performance comparison and discussion

The performance comparison of different double gate MOSFET has been shown in Table 1 for sub 20 nm technology node including their applications. Since multiple gate MOSFETs have more control of gate over the channel, therefore different DG MOSFET have been considered for performance comparison. Metal gates with high work function are suitable for low OFF-state leakage. The underlap asymmetrical gate increases fringing electric field and leads to better ON-state transistor performance. The absence of depletion region between source/channel and drain in junction-less transistor, improves transistor current drive capability by increasing ON-state current. The high-K dielectric material is preferred as oxide region under gate to improve subthreshold performance parameters and improved switching behavior of transistor. The comparison 20 nm junctionless double gate (JLDG) MOSFET[32] provides the lowest subthreshold slope and maximum I_{ON}/I_{OFF} ratio. The lowest DIBL obtained from graded channel dual material gate junctionless (GC-DMGJL) with channel length 15 nm[22]. Therefore, multi-gate juntionless transistors with low leakage and good I_{ON}/I_{OFF} ratio can be preferred as low power digital and memory applications. Several researchers have explored bio-sensing ability of double gate MOSFET by including nano-gap cavity region. The dielectric constant of these cavity regions depends on changes occurred in bio-species that adds to a very interesting feature to the biomedic-

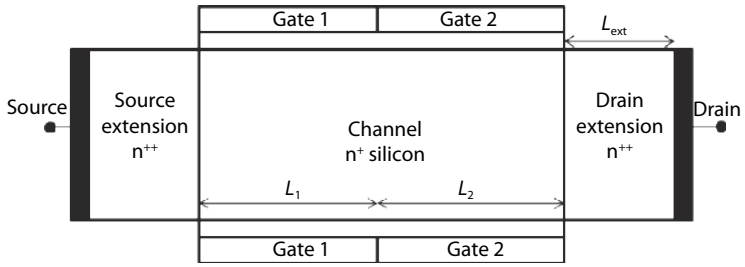

Fig. 15. Double Gate junctionless MOSFET with extensions and engineering of gate material.

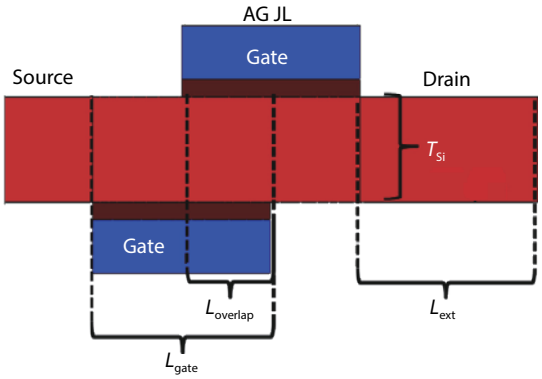

Fig. 16. (Color online) Junctionless MOSFET with asymmetric gate (AG-JL MOSFET).

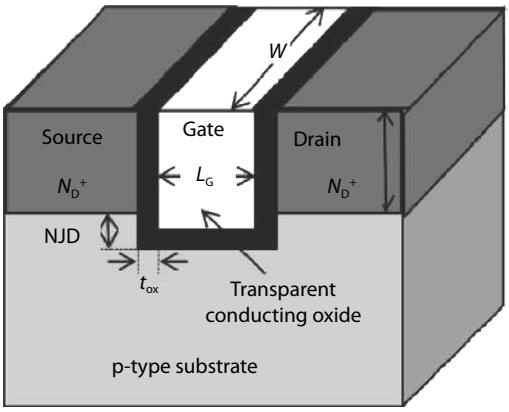

Fig. 17. Structure of recessed channel MOSFET with transparent gate.

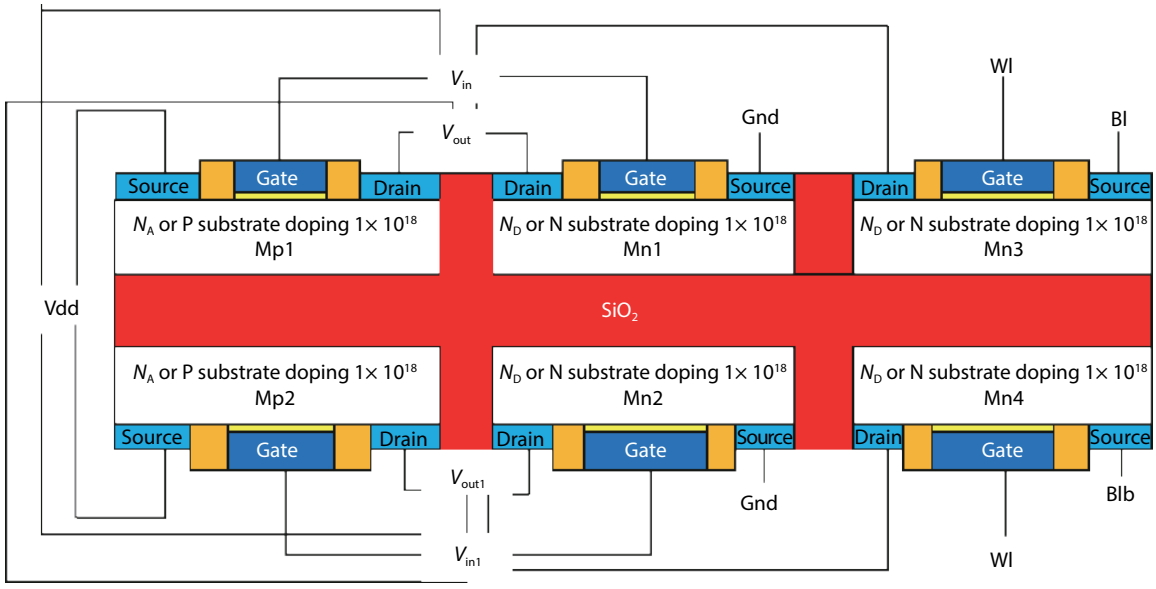

Fig. 18. (Color online) Proposed 6-T SRAM cell using junctionless SOI transistor with the connection.

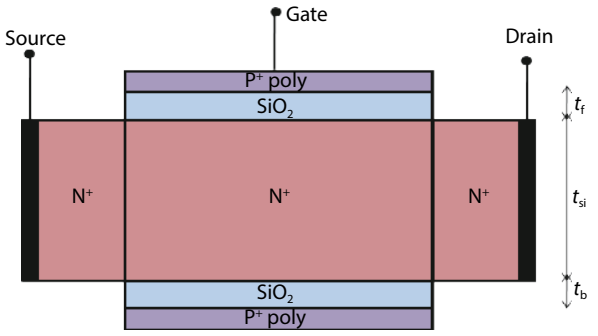

Fig. 19. (Color online) Structure of n-type junctionless double gate MOSFET.

al applications of these devices[12, 23, 34].

5. Conclusion

Various structures of MOSFET have been explored with their structural details and dimensions including applications. Modification in the structure of MOSFET has been done mainly to reduce the short channel effects that include DIBL and SS values. The main motive of these structures is to increase the ON-state current and reduce the OFF-state current. The MOSFET structures are also analyzed for suitable analog/RF performance parameters to obtain a desired range of transconductance, transistor gain, stability factor and critical frequencies. The comparisons between different structures

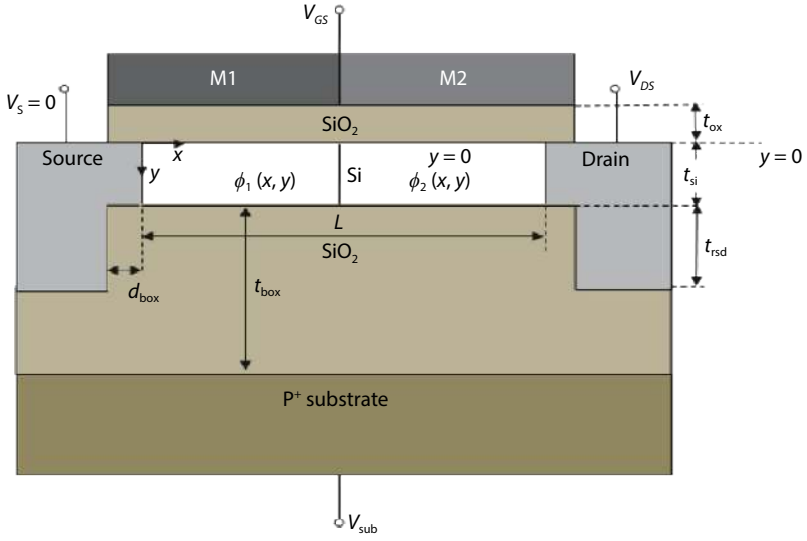

Fig. 20. (Color online) Dual metal gate (DMG) with recessed source and drain UTB SOI MOSFET.

Table 1. Comparison of performance parameters of different MOSFET structures.

Parameter	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	Channel length (nm)	Application
(GC-DMGJL) MOSFET[22]	7.695×10^{-4}	3.741×10^{-10}	2.057×10^{6}	73.42	21	15	Analog circuit
AG-JL MOSFET[28]	127×10^{-4}	1×10^{-15}	1.27×10^{5}	68	65	20	Digital circuit
(DMSG) MOSFET[21]	–	1.053×10^{-16}	–	64.7978	–	10	Digital circuit
JLDG[32]	–	–	4.86×10^{9}	62.32	75.98	20	Analog/RF
DGJL MOSFET[27]	–	–	4.03×10^{9}	63.34	79.58	20	Analog/RF

are done on the basis of subthreshold and analog/RF performance parameters. As per comparison made, the junctionless double gate (JLDG) MOSFET provides the lowest subthreshold slope and maximum I_{ON}/I_{OFF} ratio for channel length 20 nm. The lowest DIBL obtained from graded channel dual material gate junctionless with channel length 15 nm. Gate engineered transistors of high work function metal contact with various high-K dielectric regions are found suitable to obtain improved subthreshold performance. This shows that gate-engineered multi-gate juntionless MOSFET has good potential to meet future scaling trends with increased compatibility in CMOS technology for any digital/analog and portable IoT or biomedical applications.

References

[1] Radamson H H. CMOS past, present and future. Woodhead Publishing Series in Electronic and Optical Materials, 2018

[2] Buvaneswari B, Balamurugan N B. 2D analytical modeling and simulation of dual material DG MOSFET for biosensing application. Int J Electron Commun, 2019, 99, 193

[3] Srivastava V M, Yadav K S, Singh G. Design and performance analysis of double-gate MOSFET over single-gate MOSFET for RF switch. Microelectron J, 2012, 43(9), 873

[4] Colinge J P. Multi-gate SOI MOSFETs. Microelectron Eng, 2007, 84, 2071

[5] Gili E, Kunz V D, Groot C H D, et al. Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance. Solid-State Electron, 2004, 48, 511

[6] Verma J H K, Pratap Y, Haldar S, et al. Capacitance modeling of gate material engineered cylindrical/surrounded gate MOSFETs for sensor applications. Superlattices Microstruct, 2015, 88, 271

[7] Tienda-Luna I M, Roldan J B, Ruiz F G, et al. An analytical mobility model for square gate-all-around MOSFETs. Solid-State Electron, 2013, 90, 18

[8] Djeffal F, Ferhati H, Bentrcia T. Improved analog and RF performances of gate-all-around junctionless MOSFET with drain and source extensions. Superlattices Microstruct, 2016, 90, 193

[9] Sarkar A, Das A K, De S, et al. Effect of gate engineering in double-gate MOSFETs for analog/RF applications. Microelectron J, 2012, 43, 873

[10] Nasri F, Aissa M F B, Gazzah M H, et al. 3D thermal conduction in ananoscale tri-Gate MOSFET based on single-phase-lag model. Appl Therm Eng, 2015, 91(5), 647

[11] Pakaree J E, Srivastava V M. Realization with fabrication of double-gate MOSFET based differential amplifier. Microelectron J, 2019, 91, 70

[12] Abhinav, Rai S. Reliability analysis of junction-less double gate (JLDG) MOSFET for analog/RF circuits for high linearity applications. Microelectron J, 2017, 64, 60

[13] Srivastava V M, Yadav K S, Singh G. Design and performance analysis of cylindrical surrounding double-gate MOSFET for RF switch. Microelectron J, 2011, 42, 1124

[14] Ku W H. Unilateral gain and stability criterion of active two-ports in terms of scattering parameters. Proc IEEE, 1966, 54(11), 1617

[15] Sivasankaran K, Kannadassan D, Seetaram K, et al. Bias and geometry optimization of silicon nanowire transistor: radio frequency stability perspective. Micro Optic Technol Lett, 2012, 54(9), 2114

[16] Orouji A A, Heydari S, Fathipour M. Double step buried oxide (DSBO) SOI-MOSFET: A proposed structure for improving self-heating effects. Physica E, 2009, 41, 1665

[17] Kwona I, Kwonb H I, Cho H I. Development of high temperatureoperation silicon based MOSFET for harsh environment application. Results Phys, 2018, 11, 475

[18] Tahirparveen. Operational transconductance amplifier and analog integrated circuits. I K International Publishing House, 2009

[19] Narang R, Saxena M, Gupta M. Modeling of gate underlap junction-

less double gate MOSFET as bio-sensor. Mater Sci Semicond Process, 2017, 71, 240

[20] Kumar A, Tripathi M M, Chaujar R. Comprehensive analysis of sub-20 nm black phosphorus based junctionless-recessed channel MOSFET for analog/RF applications. Superlattices Microstruct, 2018, 116, 171

[21] Djeffal F, Lakhdar N, Yousfi A. An optimized design of 10-nm-scale dual-material surrounded gate MOSFETs for digital circuit applications. Physica E, 2011, 44, 339

[22] Pathak V, Saini G. A Graded channel dual-material gate junctionless MOSFET for analog applications. Proced Comput Sci, 2018, 125, 825

[23] Narang R, Saxena M, Gupta M. Investigation of dielectric modulated (DM) double gate (DG) junctionless MOSFETs for application as a biosensors. Superlattices Microstruct, 2015, 85, 557

[24] Pang Y S, Brews J R. Design of 0.1-μm pocket n-MOSFETs for low-voltage applications. Solid-State Electron, 2002, 46, 2315

[25] Orouji A A, Kumar M J. Nanoscale SOI MOSFETs with electrically induced source/drain extension: Novel attributes and design considerations for suppressed short-channel effects. Superlattices Microstruct, 2006, 39, 395

[26] Pal A, Sarkar A. Analytical study of dual material surrounding gate MOSFET to suppress short-channel effects (SCEs). Eng Sci Technol, 2014, 17, 205

[27] Chebaki E, Djeffal F, Ferhati H, et al. Improved analog/RF performance of double gate junctionless MOSFET using both gate material engineering and drain/source extensions. Superlattices Microstruct, 2016, 92, 80

[28] Wang Y, Tang Y, Sun L L, et al. High performance of junctionless MOSFET with asymmetric gate. Superlattices Microstruct, 2016, 97, 2016

[29] Awadhiya B, Kondekar P N, Meshram A D. Understanding negative differential resistance and region of operation in undoped HfO_2-based negative capacitance field effect transistor. Appl Phys A, 2019, 125, 427

[30] Kumar A, Gupta N, Chaujar R. TCAD RF performance investigation of transparent gate recessed channel MOSFET. Microelectron J, 2016, 49, 36

[31] Mishra V K, Chauhan R K. Efficient layout design of junctionless transistor based 6-T SRAM cell using SOI technology. ECS J Solid State Sci Technol, 2018, 9, 456

[32] Roy N C, Gupta A, Rai S. Analytical surface potential modeling and simulation of junction-less double gate (JLDG) MOSFET for ultra-low power analog/RF circuits. Microelectron J, 2015, 46, 916

[33] Saramekala G K, Santra A, Dubey S, et al. An analytical threshold voltage model for a short-channel dual-metal-gate (DMG) recessed-source/drain (Re-S/D) SOI MOSFET. Superlattices Microstruct, 2013, 60, 580

[34] Tripathi S L, Patel R, Agrawal V K. Low leakage pocket junctionless DGTFET with bio sensing cavity region. Turk J Electr Eng Comput Sci, 2019, 27(4), 2466