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Research advances on III–V MOSFET electronics beyond Si CMOS

J. Kwo [a,*], M. Hong [b]

[a] Department of Physics, National Tsing Hua University, Hsinchu 30012, Taiwan
[b] Department of Materials Science and Engineering, National Tsing Hua University, Hsinchu 30012, Taiwan

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ABSTRACT

An overview is given on recent advances of science and devices of III–V based and Si MOS and MOSFET. Firstly, we have integrated molecular beam epitaxy (MBE) with atomic layer deposition (ALD) for the growth of excellent high-κ dielectrics with abrupt interfaces, critical for further complementary metal-oxide-semiconductor (CMOS) scaling beyond the 45 nm node. Secondly, we showed that epitaxial yttrium-doped HfO_2 films on GaAs(1 0 0) have stabilized the cubic phase, and led to enhancement of κ over 30. Thirdly, inelastic electron tunneling spectroscopy (IETS) was applied to probe the phonon modes and charge trappings within the high-κ dielectrics. Fourthly, scaling of the high-κ oxides approaching 1.0 nm capacitance equivalent thickness (CET) is achieved in a $Ga_2O_3(Gd_2O_3)$[GGO]/$In_{0.2}Ga_{0.8}As$ (InGaAs) gate stack that has undergone 850 °C rapid thermal annealing, and which has unpinned the surface Fermi level of the III–V semiconductor. Finally, we have demonstrated a self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs made of Al_2O_3(2 nm)/GGO(7 nm) gate oxide and TiN metal gate at 1-μm gate length, reaching a *world record* of drain current and transconductance.

1. Introduction

The success of silicon-based integrated electronic technology over last four decades relies, to a large extent, on the excellent properties of SiO_2 and the SiO_2/Si(1 0 0) interface such as low-defect densities, superb uniformity over large area, thermal stability, etc. Currently, the SiO_2 thickness in *state-of-the-art* devices is approaching 1.2 nm, and quantum tunneling of electrons through such thin insulating layer gives rise to unacceptably large electric leakage. The revolutionary replacements of the long-standing, reliable SiO_2/polysilicon in the gate of transistors by HfO_2-based high-κ dielectric plus metal gates were announced in 2007, and are now in production for the 45 nm Si complementary metal-oxide-semiconductor (CMOS) by the leading integrated circuits (ICs) manufacturers. The monolithic dimensional scaling, which in the past has provided simultaneously high-density/low-cost and high-performance ICs in Si-based system, may not work any more, as further scaling in devices does not guarantee performance benefits. Driven by continual demands of enhanced transport in channels and reducing power dissipation beyond the 16–22 nm node, the current consensus is that the integration of III–V semiconductors and Ge as high-mobility channels with high-κ gate dielectrics and metal gates is urgently needed in order to build a viable CMOS technology ready by year 2015.

Electron mobility in III–V is known to be much higher than those in Si and Ge. A mature III–V MOS technology with electron mobility at least 10 times higher than that in Si and with dielectrics having several times higher than that of SiO_2 would certainly enable the electronic industry to continue pushing its new frontiers for a few more decades. Furthermore, bandgap engineering and direct bandgaps in III–V, not available in Si- and Ge-based systems, has provided great opportunities of novel device architectures, thus leading to high-performance integrated optoelectronic circuits in combining both electronics and photonic devices on a single chip.

The basic III–V MOS material properties have to be fully understood to allow process integration and full-scale manufacturing. Besides thermal stability, compatibility, and electronic transport properties, the III–V surface passivation and interface properties with the high-κ dielectric are enormous challenges, and will have to be thoroughly investigated in depth.

2. Major research results on III–V and Si MOS devices

Since early 1960s there have been intensive efforts in seeking electrically and thermodynamically stable insulators on GaAs with Fermi-level unpinning and a low-interfacial density of states (D_{it}) as required for the GaAs MOSFET [1]. This drive has been answered by our discovery of MBE-deposited mixed oxide $Ga_2O_3(Gd_2O_3)$ [GGO] [2,3] and pure Gd_2O_3 [4] dielectric films on GaAs surfaces during the 1990s in Bell Labs. Subsequent

*Corresponding author. Tel.: +886 3 574 2800; fax: +886 3 572 3052.
E-mail address: raynien@phys.nthu.edu.tw (J. Kwo).

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employment of GGO as a gate dielectric led to the *first* inversion-channel GaAs MOSFETs in both n- and p-configurations [5], and InGaAs MOSFET in n-configuration [6]. Depletion-mode GaAs MOSFETs were shown to exhibit negligible drain current drift and hysteresis [7–9], the first achievement in this class of transistors and an important technological advance for the manufacturing consideration. With these achievements, the problem puzzling the researchers for the past 35 years has finally been solved. Moreover, the discovery has opened up an entirely new field for the IC industry; i.e., III–V MOSFET, giving a timely needed innovative technology beyond Si CMOS at 16 nm node.

Molecular beam epitaxy (MBE) with its unique and superior atomic layer-by-layer growth has been widely used in tailoring the interface of high-κ dielectrics and semiconductors. The long-sought III–V MOS and MOSFET have been realized with the MBE growth. Moreover, the thin gate dielectrics required for the 22–16 nm node Si CMOS may demand the usage of the MBE approach for further reducing interfacial layer thickness.

In recent years we have successfully established the high-κ dielectric growth using both MBE and atomic layer deposition (ALD) methods on the III–V, Si, and Ge, including the high-κ enhancement. The surface Fermi-level unpinning in InGaAs and the understanding for its mechanism have been studied. Furthermore, we have demonstrated world-record device performance in inversion-channel InGaAs MOSFET, superior to Si in the same gate length. Recent major achievements are summarized below:

2.1. *Si MOS devices based on high-κ dielectrics fabricated by a novel MBE template approach followed by ALD*

With our advanced molecular beam epitaxial growth, we have demonstrated atomically abrupt high-κ dielectrics HfO_2/Si(1 0 0) interface free of interfacial layer formation [10]. Such nano-thick high-κ dielectric films were employed as a template to suppress the formation of unwanted oxide/Si interfacial layer during subsequent ALD, as illustrated in Fig. 1(a–c) [11]. The attainment of high κ and very small frequency dispersion in capacitance–voltage (C–V) curves suggests the absence of low κ capacitors in series near the oxide/Si interface. A composite film consisting of ALD-Al_2O_3(3.0 nm)/MBE-HfO_2(2.0 nm) showed an overall κ value of 11.5, a capacitance equivalent thickness (CET) of 1.7 nm, a D_{it} of $2\times10^{11}\,cm^{-2}\,eV^{-1}$, and a leakage current density of $1.1\times10^{-4}\,A/cm^2$ at V_{fb}+1 V as in Fig. 1(d) [11]. Here a CET is defined as κ_{SiO_2}*(thickness of high-κ dielectrics)/($\kappa_{high\ \kappa}$). More recently, another composite film made of ALD-HfO_2(1.4 nm)/MBE-HfO_2(1.5 nm) showed an overall κ value of 16.2 and a CET as low as 0.7 nm with a leakage current density of $5.3\times10^{-1}\,A/cm^2$ at $V_{fb}-1$ V [12]. The D_{it} value at midgap is $3.6\times10^{11}\,cm^{-2}\,eV^{-1}$ calculated by the conductance method. The attainment of low-CET value suggests an oxide/Si interface that is nearly free of low κ capacitor in series with it. Furthermore, MOSFETs based on the MBE–ALD HfO_2 composites were fabricated, showing excellent device performance with a drain current (I_D) of 240 mA/mm and transconductance (G_m) of 120 mS/mm, superior to those of the MOSFETs using either solely ALD-grown (55 mA/mm, 60 mS/mm), or MBE-grown (80 mA/mm, 35 mS/mm) gate dielectrics [13]. We are currently implementing an ALD reactor chamber directly into our MBE system to perform better analysis and control of the interface formation, thus achieving an even lower CET value.

2.2. *Single crystalline epitaxial growth of high-κ dielectric oxide films on GaAs(1 0 0), with enhanced dielectric constant*

HfO_2 has three known crystallographic structures, monoclinic, cubic, and tetragonal phases, with respective predicted κ ~20, 30, and 70 according to the density function theory calculations [14]. The monoclinic phase is the most stable phase below 1750 °C, while the tetragonal and cubic phases can be transformed thermodynamically at approximately 1720 and 2600 °C, respectively. The HfO_2–Y_2O_3 phase diagram suggests a possible cubic or tetragonal phase formation at relatively lower temperatures with Y_2O_3 doping to HfO_2.

Recently, pure MBE-HfO_2 films were obtained on GaAs(0 0 1) in the monoclinic crystal structure (α=γ=90° and β~99°) with their a and b axes aligned with the in-plane {1 0 0} axes of GaAs, and formed four equivalent in-plane domains rotated 90° about surface normal [15]. Furthermore, doping the HfO_2 films with Y_2O_3 (denoted as YDH) at an atomic percentage of Y about 19.2 ± 0.5 altered the crystal structure of the epitaxial film from the common monoclinic phase of a κ~17 to the cubic phase of a κ over 30. The attainment of the cubic YDH has effectively eliminated the number of azimuthal domains as shown by HR-TEM image, thus significantly improved electrical leakage shown in Fig. 2(a and b) [16].

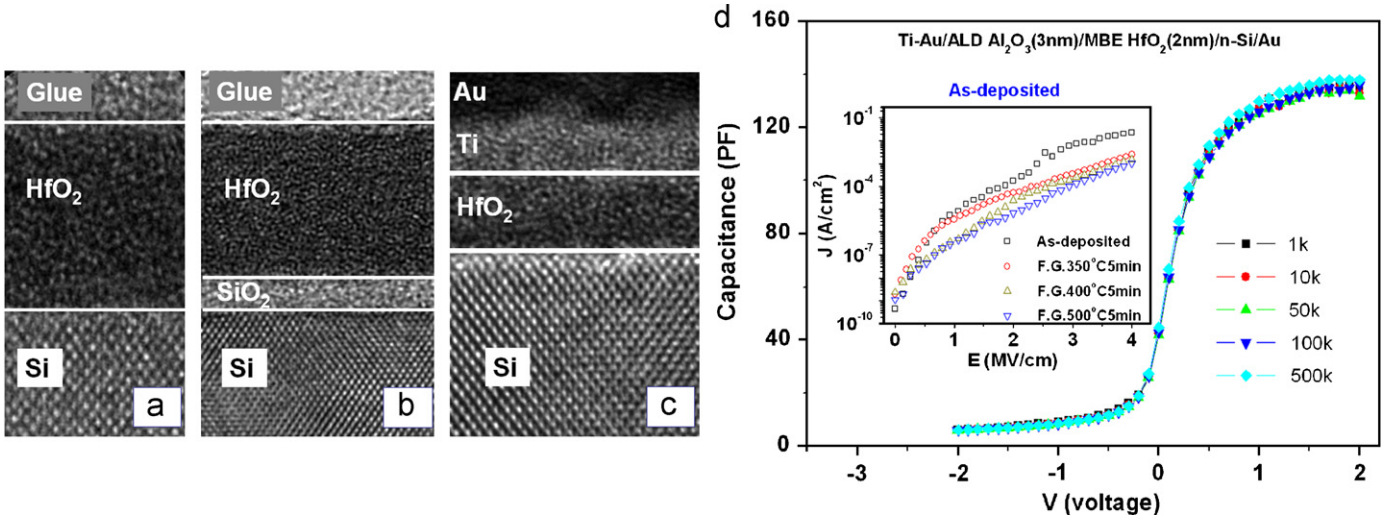

Fig. 1. HR-TEM pictures showing the HfO_2/Si interface comparison of three different oxide growth techniques, including (a) MBE HfO_2 (6.7 nm); (b) ALD HfO_2 (8.1 nm) with SiO_2 (1.4 nm); (c) ALD (1.4 nm)/MBE (1.5 nm) composite HfO_2; (d) C–V characteristics of an Al_2O_3 (ALD)/HfO_2 (MBE) composite film. The inset shows the J–E curves after forming gas anneals at various temperatures.

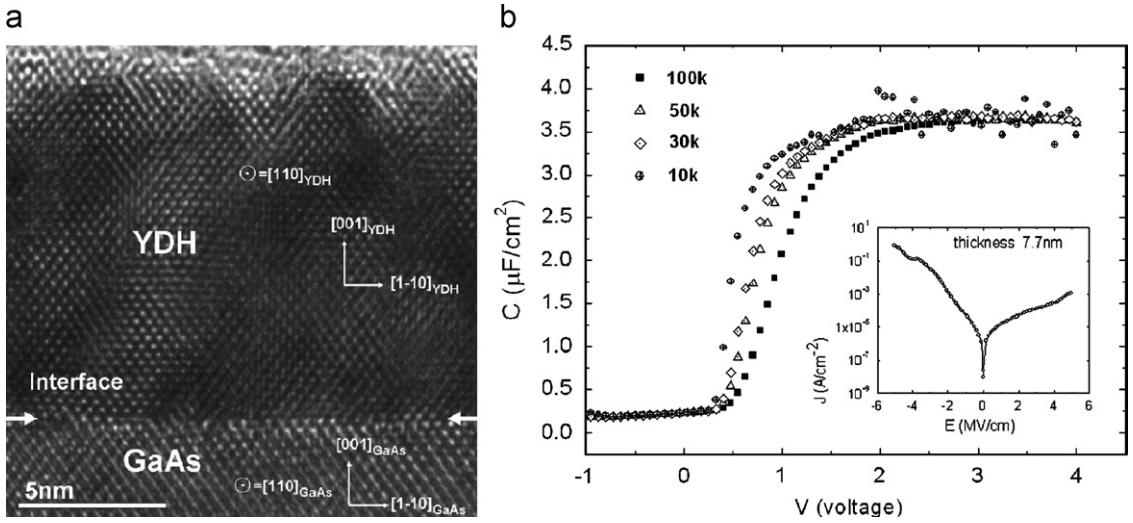

Fig. 2. Cross-sectional HR-TEM images of (a) cubic phase yttrium-doped HfO_2 (1 0 0) epitaxially grown on GaAs(1 0 0) in the [1 1 0] projection. The image clearly shows the atomically sharp interface and free of interfacial layer; (b) *C–V* curves of a MOS capacitor of an YDH layer 7.7 nm thick measured at frequencies between 10 and 100 kHz. The inset is a *J–E* curve of the same sample.

The incorporation of cations with lower valence into HfO_2 is known to be one approach to achieve the stabilization of the meta-stable high-temperature phase at room temperature [17]. When the tetravalent cations of Hf^{4+} are replaced with the trivalent cations such as Y^{3+}, oxygen vacancies are formed for charge compensation. The creation of oxygen vacancies leads to a change in cation-oxygen coordination since the ionic positions are displaced away from the stoichiometric form, followed by a phase transition from the amorphous to the meta-stable high-temperature tetragonal or cubic phases, but not to the equilibrium low-temperature monoclinic phase. Furthermore, according to the *Clausius-Mosotti* relation, the dielectric constant κ is closely related to the polarizability α_m and the molecular volume V_m. The enhancement of κ may be understood from the reduction of the molecular volume V_m that often occurred in the high-temperature phase.

2.3. Inelastic electron tunneling spectroscopy (IETS) and charge pumping studies of MOS diodes of high-κ gate dielectrics

Charge trappings are largely responsible for mobility degradations found in high-κ dielectrics. In addition, scatterings of the electrons by low-frequency phonons were proposed as another probable source responsible for mobility degradation [18]. We have recently carried out IETS on Si-based MOS devices made of high-κ dielectrics like HfO_2, Y_2O_3, and stacked HfO_2/Y_2O_3 to extract the energies of vibrational modes in monoclinic HfO_2 and cubic Y_2O_3 with good reproducibility, and to further characterize the interfacial structure and chemical bonding unique of the MBE and ALD processes (Fig. 3(a)) [19]. By analyzing the pronounced features of charge trapping in IETS spectra of stacked HfO_2/Y_2O_3, we infer that these traps are located mostly near the interface between HfO_2 and Y_2O_3, likely caused by dissimilar charge distributions of two ionic oxides of different cation valences, and the presence of interfacial strains at dissimilar structures. (Fig. 3(b)) Our work thus has raised an important possibility of tailoring the trap locations in a gate dielectric stack through the novel scheme of multi-layering a number of dielectric materials of dissimilar cation valences.

Both interface traps and bulk traps in high-κ dielectrics are major sources for charge trapping. To evaluate the surface states near the semiconductor–high-κ interface of the MOSFET device, the charge pumping method is well known as a powerful measurement [20]. Our recent charge pumping experiment on the Si- and GaAs-MOS diodes showed that energy distribution of $D_{it,}$ occurs in higher half of the bandgap due to severe Coulomb scatterings from interface-trapped and oxide-trapped charges. In addition, notable accumulations of traps were observed near the interface of the HfO_2/Y_2O_3 bi-layer, consistent with the IETS observations [21].

2.4. Investigation of Fermi-level unpinning mechanism on InGaAs surface

$In_{0.53}Ga_{0.47}As$, with its lattice matched to InP, has been used as a backbone for nearly all high-speed electronic devices [22]. Recently we have employed ALD-HfO_2 to effectively passivate $In_{0.53}Ga_{0.47}As$, and to determine the energy-band parameters [23]. The key for the passivation is the removal of arsenic oxides from the ALD-HfO_2/$In_{0.53}Ga_{0.47}As$ interface during the ALD growth according to detailed XPS analysis, thus ensuring the Fermi-level unpinning as evidenced from the *C–V* characteristics [24].

However, residual native oxides of Ga_2O_3 and In_2O_3 still remained at the interface. The quality of the high-κ dielectrics/substrate interface critically affects the equivalent oxide thickness (EOT) scaling. To minimize the formation of native oxides on the $In_{0.53}Ga_{0.47}As$/InP surface upon air exposure, we deliberately shortened the exposure time under 10 min of the MBE-grown $In_{0.53}Ga_{0.47}As$/InP surface prior to the ALD HfO_2 deposition [25]. The amount of "residual" native oxides at the HfO_2/InGaAs interface was drastically reduced to minimal formation of the interfacial layer thickness (on the order of 0.2 nm), as confirmed from X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy. A CET of 0.95–1.06 nm was achieved without any surface pretreated process. After quantum-mechanical corrections, the EOT will be even lower than the CET [26].

2.5. GGO thickness scalability study

Scaling high-κ oxides to nanometer range as well as unpinning surface Fermi level of the III–V semiconductors has been one main focus of recent high-κ research on high-mobility channel materials. Among all the dielectrics passivating GaAs (InGaAs)

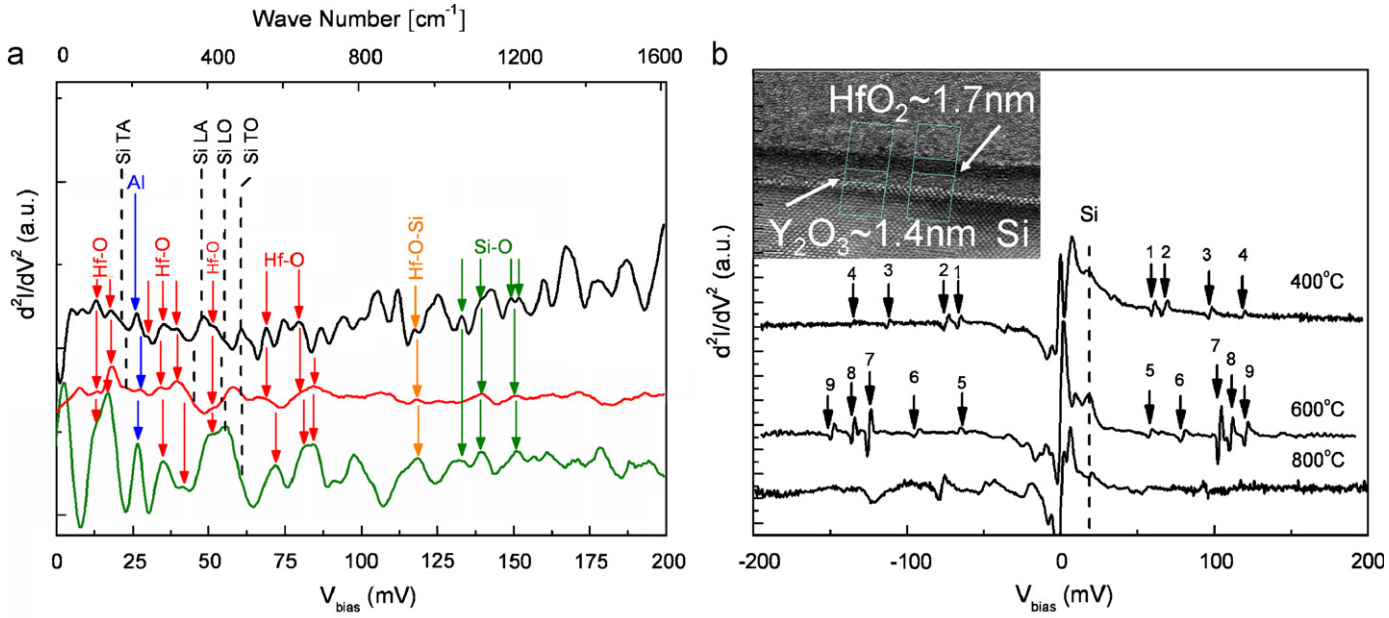

Fig. 3. (a) Gate injection IETS spectra of 600 °C N_2 annealed ALD-grown HfO_2 film (black line), 600 °C UHV annealed MBE-grown HfO_2 film (red line), and 600 °C N_2 annealed MBE-grown HfO_2 films (green line). The Si phonons appeared at 19 (TA), 44 (LA), 53 (LO), and 58 (TO) mV are denoted by black dotted lines, and the peaks for Hf–O bonds at 105, 146, 278, 319, 416, 555, 645, and 680 mV are denoted by red arrows. The peaks associated with Al, Hf–O–Si, and Si–O are denoted by blue, orange, and green dotted lines, respectively. (b) The IETS spectra of stacked HfO_2/Y_2O_3/Si MOS diodes which were annealed at 400, 600, and 800 °C. Series of symmetric charge trapping features with strong intensity were revealed in these two spectra. The inset shows the cross-sectional TEM view of the stacked HfO_2/Y_2O_3/Si MOS sample. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

[2–4,23–25,27,28], GGO was found to give the lowest interfacial densities of states [3]. Therefore, the essential issue of the thickness scalability of the GGO oxide on InGaAs was addressed, and a CET approaching 1 nm was demonstrated [29,30]. The GGO/$In_{0.2}Ga_{0.8}As$ (InGaAs) gate stacks were fabricated with the oxide thickness systematically reduced from 33 to 4.5 nm. With the aid of an *in situ* capping layer Al_2O_3 3 nm thick as a protection layer against moisture due to its thermal and chemical stabilities, MOS capacitors with the dual-dielectric layer on InGaAs have withstood rapid-thermal-anneals (RTA) to 800–850 °C. Excellent *C–V* characteristics in terms of small flat-band voltage, a small frequency dispersion of measured capacitances at accumulation, D_{it}'s in the low 10^{11} cm^{-2} eV^{-1}, the κ values of GGO remaining ~14–16, were achieved for all GGO film thicknesses. The smallest CET achieved is 1.1 nm, and linearly scales with the GGO physical film thickness as in Fig. 4. The systematic variations of the device performance with the GGO film thickness are summarized in Table 1. Hence the *in situ* Al_2O_3 cap plays a vital role in extending our earlier success of unpinning surface Fermi level in the III–V to an aggressive scaling $Ga_2O_3(Gd_2O_3)$ thickness to a CET~1 nm, greatly enhancing the prospect for realistic device applications.

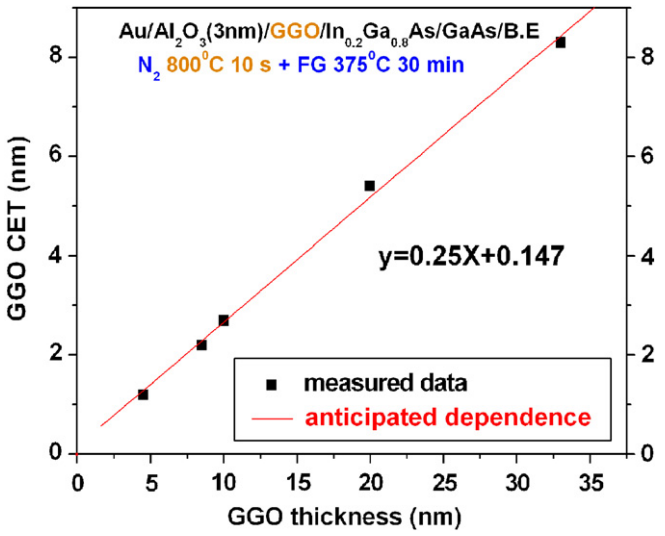

Fig. 4. Oxide scalability studies: the CET value of $Ga_2O_3(Gd_2O_3)$ linearly scales with the GGO physical film thickness.

2.6. *Attainment of high-performance inversion-channel GGO/InGaAs MOSFET*

In 1990s, employment of MBE-GGO enabled the demonstration of the first non-self-aligned inversion-channel GaAs and $In_{0.53}Ga_{0.47}As$ MOSFETs [5,6]. $In_{0.53}Ga_{0.47}As$ MOSFETs with GGO 40 nm thick as the gate dielectric exhibited a maximum drain current of 375 mA/mm (1-μm gate length) and a transconductance of 190 mS/mm (0.75-μm gate length) [6]. Recently, other non-self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs using ALD-Al_2O_3 as a gate dielectric were also demonstrated [31], in that an 0.5-μm gate length $In_{0.53}Ga_{0.47}As$ MOSFET with an ALD-Al_2O_3 gate oxide 8 nm thick gave a maximum drain current of 367 mA/mm, and a transconductance of 130 mS/mm [32]. More recently, a 0.4-μm gate-length inversion-channel $In_{0.65}Ga_{0.35}As$ MOSFET with an even higher In content and an ALD-Al_2O_3 gate oxide 10 nm thick showed a maximum drain current of 1.05 A/mm, and a transconductance of 350 mS/mm [33].

Nonetheless, the non-self-aligned process is impractical for device integration, due to the complexity of mask alignment as well as the unavoidable parasitic resistance. Recently, we have succeeded in attaining self-aligned inversion-channel $In_{0.53}Ga_{0.47}As$ MOSFETs of 1-μm gate length by employing a MBE-deposited gate dielectric stack of Al_2O_3 (2 nm)/GGO(7 nm) and TiN metal gate [33]. *In situ* deposited Al_2O_3 was used to protect GGO from absorbing moisture during fabrication of devices, and TiN

Table 1
Summary of GGO scalability and relevant electrical properties, including GGO dielectric constant (κ), flat-band voltage (V_{fb}), frequency dispersion of capacitance at accumulation, leakage current density at V_g=V_{fb}+1 V, interfacial density of states (D_{it}) near the mid-gap, and GGO EOT values.

GGO thickness (nm)	GGO κ value	V_{fb} (V)	Dispersion (10 k–500 kHz)(%)	$J@V_{fb}$+1 V (A/cm^2)	D_{it} (10^{11} cm^{-2} eV^{-1})	GGO EOT (nm)
Au gate metal (RTA 800 °C 10 s)						
33	15–16	3.5	2.8	1.18×10^{-9}	1.3	8.6–8.0
20	14–15	1.3	1.5	1.62×10^{-9}	1	5.6–5.2
10	14–15	1.1	2.2	1.46×10^{-9}	1.4	2.8–2.6
8.5	14–16	1.1	4.7	1.78×10^{-9}	2.6	2.4–2.1
4.5	14–16	1.1	5.4	3.1×10^{-5}	1.3	1.3–1.1
Al gate metal (RTA 850 °C 10 s)						
8.5	14–16	0.1	2.6	2.5×10^{-9}	2.5	2.4–2.1

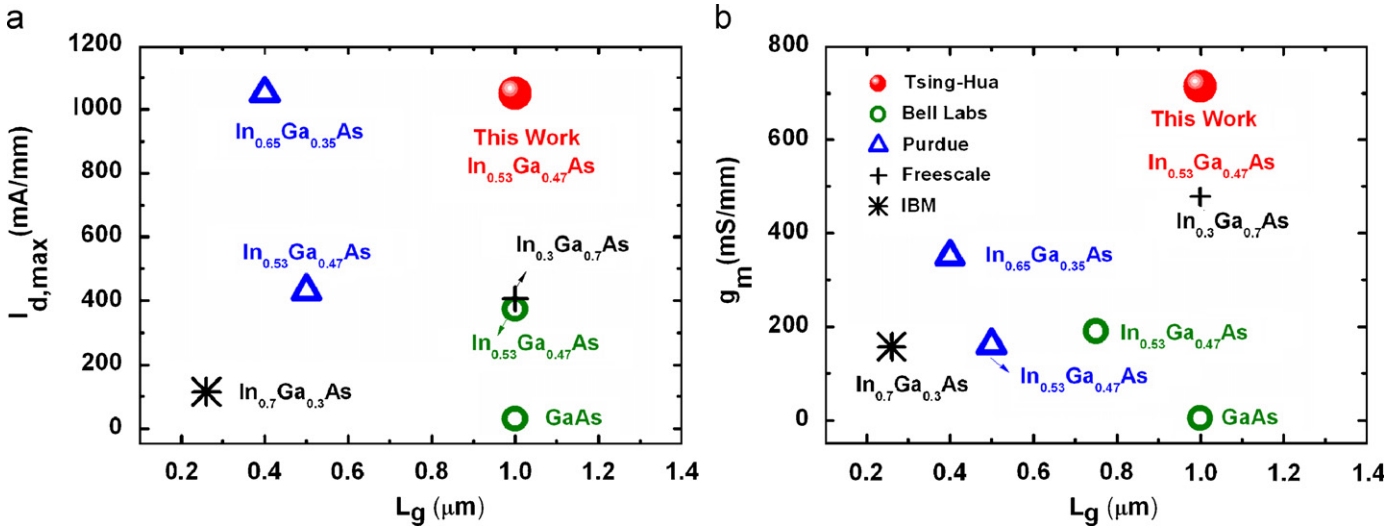

Fig. 5. Summary of (a) the maximum drain current I_d and (b) transconductance g_m representative work on III–V enhancement mode nMOSFETs reported in the last decade. Devices with gate length longer than 1 μm are excluded. The self-aligned processed inversion channel device (our work) is denoted with a solid circular symbol, and the data of non-self-aligned processed inversion-channel devices are denoted with hollow circular symbol.

was chosen due to its suitable work function and thermal stability. The MOSFET of TiN/Al_2O_3/GGO/$In_{0.53}Ga_{0.47}As$, with high-thermal intactness as subjected to RTA to 700 °C for dopant activation, has demonstrated *world record* performance of a maximum drain current of 1.05 A/mm, a transconductance of 714 mS/mm, and a peak mobility of 1300 cm^2/V s, the highest ever reported for III–V inversion-channel devices of 1-μm gate length. The maximum drain current I_d and transconductance g_m of representative III–V enhancement mode nMOSFETs reported in the last decade are summarized in Fig. 5a and b, respectively, for comparison [33].

Acknowledgments

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