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ORIGINAL PAPER

Temperature Dependent Performance Evaluation and Linearity Analysis of Double Gate-all-around (DGAA) MOSFET: an Advance Multigate Structure

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Abstract
Multi-gate devices such as double gate, FinFET and Gate-All-Around (GAA) are potential candidates to achieve the performance expected by semiconductor association. This paper presents an analog/RF performance and linearity distortion analysis for an advance multigate structure named Double Gate-All-Around (DGAA) MOSFET. Temperature dependent characteristics of the DGAA MOSFET have also been investigated in detail from 200 K to 400 K. A comparative analysis between Gate-All-Around (GAA) and DGAA MOSFETs with impact of silicon film thickness is analyzed by using 3-D ATLAS TCAD device simulator. It is demonstrated that depending on gate voltage, DGAA MOSFET has larger value of drain current (I_{ds}), transconductance (g_m) and gain. Results demonstrate that drain current, transconductance, device gain and transconductance to drain current ratio (g_m/I_{ds}) improves when temperature is decreased. DGAA MOSFET shows improvement in analog/RF performance, suppressed Short Channel Effects (SCEs) and harmonics distortions due to more gate controllability on the channel charge.

Keywords Double gate-all-around (DGAA) MOSFET · Inner and outer gate · Harmonic distortion · Linearity1

1 Introduction

The improved performance and higher packing density of semiconductor devices in Integrated Circuits (ICs) continuously motivate the device scientists to reduce the feature size of single transistor into nanoscale regime. According to ITRS, the technology node will reach atomic level (below 5 nm) by 2020 [1, 2]. This can be achieved by reducing the short channel effects (SCEs) with scaling the device for more controllability over the channel. For this, the multiple gate structures such as double gate (DG) [3, 4], Fin-FET [5] and Gate-All-Around (GAA) [6, 7] are becoming cornerstone for sub-32 nm technologies having enhanced channel charge controllability by the gate. Although these multiple gate structures exhibit better short channel immunity but their performance degrades with the decrease in gate length. Therefore it is the need of hour to refine the device fundamental techniques for the survival of nano-electron device technology.

For gate-all-around nanowire FETs, the charge is centroid and the maximum leakage point in the sub-threshold regime is the center of the nanowire [8]. In the sub-threshold regime, if charge can move towards centroid and the maximum leakage point to the outer channel region and thus, get closer to the gate, it may lead to improved gate control over the nanowire channel and thus, lead to better control of short-channel effects. Therefore, presence of cylindrical gate electrode on semiconductor channel for more than one side similarly to double gate structure will effectively increase the electrostatic control, improve the device gain and will decreases the short-channel effects [9]. Then the nano-scaling can further be increased with innovative MOSFET design. This new structure is called as Double Gate-All-Around (DGAA) MOSFET. Thus it is essential to realize the high performance in terms of transconductance and linearity distortion. Recently proposed a similar MOS structure has shown the possibility to fulfill the requirements [10].

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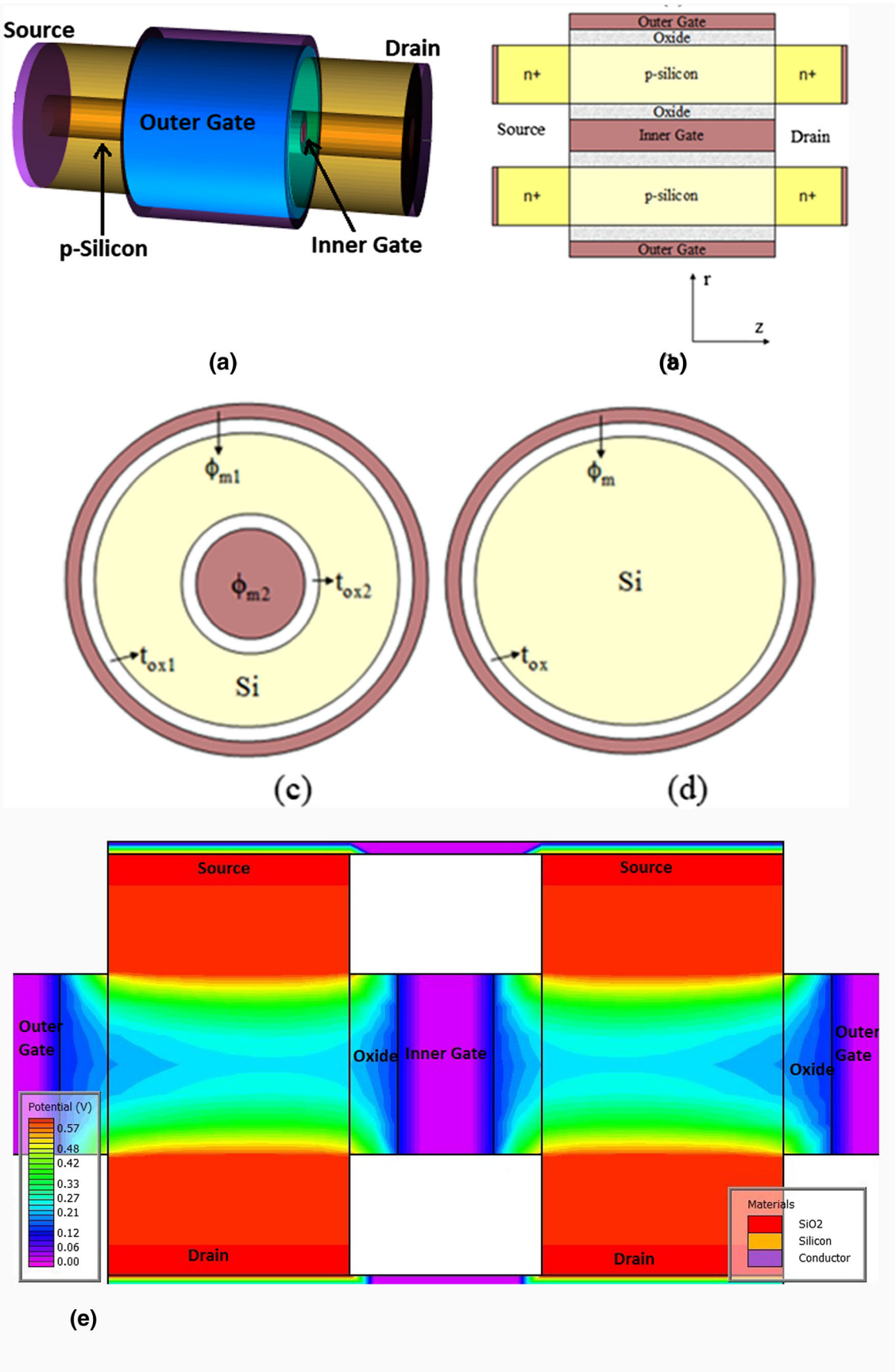
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n+
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Outer Gate
r
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(b)
ϕ_{m1}
ϕ_{m2}
t_{ox2}
t_{ox1}
Si
(c)
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Si
t_{ox}
(d)
Source
Source
Outer Gate
Oxide
Inner Gate
Oxide
Outer Gate
Potential (V)
0.57
0.48
0.42
0.33
0.27
0.21
0.12
0.06
0.00
Drain
Drain
Materials
SiO2
Silicon
Conductor
(e)

◀ **Fig. 1** **(a)** 3-D view of DGAA MOSFET **(b)** Vertical cross-sectional view of Double Gate–All-Around (DGAA) MOSFET **(c)** Circular cross-sectional of DGAA MOSFET and **(d)** Circular cross-sectional of GAA MOSFET (e) Contour plot of potential of DGAA MOSGET

DGAA MOSFET can be classified as double gate in cylindrical version which consists of two gates; outer gate and inner gate. These gates control the channel charge independently. The role of outer gate is quite similar as conventional gate-all-around structure and the inner core gate acts as the second gate which enhances the charge controllability. This novel device structure is expected to exhibit exceptional charge control allowing scaling roadmap to extend beyond GAA. The performance of the device enhances with the decrease in the radius of the silicon thickness like silicon nanotube [11] and the volume inversion will take place below 4 nm thickness between two gates which leads to an improvement in mobility [12]. Analytical modeling for DGAA MOSFET has been done in term of surface potential, electric field and drain current [13, 14]. Low-k dielectric as vacuum gate has also been used over silicon substrate instead of native oxide to reduce hot carrier reliability [15]. Chen et al. explored manufacturing challenges of similar device by experimental study and shown that such type of structure can be easily fabricated [16]. Therefore it is necessary to investigate analog RF performance for new device with linearity analysis. The linearity analysis is also very important for device higher reliability. High reliability insures the device stability and workability for long time. Linear device insure the minimal distortion and others higher order harmonics should be minimum at device output [17]. In Radio Frequency and wireless communication systems, device should be maintained linear operation even receiving a weak signal in the presence of a strong interference. In addition to the linearity and harmonic distortion the impact of temperature over the crucial RF performance such as (cut-off frequency, trans-conductance, and g_m/I_{ds}) for DGAA and GAA MOSFET architecture has also been studied.

2 Device Structure and Simulation Details

Figure 1 (a) shows the 3-D view and (b) illustrates the vertical cross-sectional view of DGAA MOSFET. Figure 1 (c) is circular cross-sectional picture of DGAA MOSFET with both the gates i.e. outer metal gate with work function (ϕ_{m1}) and inner metal gate with work function (ϕ_{m2}) and (d) are the circular cross-sectional view for GAA MOSFET. Figure 1(e) shows the potential distribution in the silicon film in form of contour plot.

DGAA MOSFET works in two modes – first one is separate inversion and second one is volume inversion. In first mode two channel regions are formed i.e. first at the Si/SiO_2 interface closely under the upper gate and second one at SiO_2/Si interface closed to inner gate. Both the inversion layers almost occupy the complete silicon region. Both the gates can control the channel more efficiently. This particular mode enhances the number of charge carriers and channel mobility which result in improved performance compared to non-classical structures. Parameters used in the TCAD simulation are illustrated in Table 1.

ATLAS–3D TCAD device simulator is used to simulate DGAA structure. CVT mobility model is used to account the mobility of channel charge due to various scattering and operating temperature. Concentration and temperature dependent analytical model is used keeping in view that the analysis has been carried out in the temperature range 77–450 K. Shockley-Read-Hall (SRH) recombination model has been used with fixed carrier life time (1×10^{-7} s) along with carrier density dependence of auger recombination [18].

3 Linearity Distortion Analysis

Higher order transconductance derivatives are the main cause of linearity distortion. Important linearity performance matrices such as Second and third Order Voltage Intercept Point VIP2 and VIP3 and higher Order Inter-Modulation Distortion (IMD3) are functions of higher order transconductance derivatives. These metrics are used for the evaluation of device linearity performances and inter-modulation distortion [19, 20]. The trans-conductance derivatives are given as:

$$g_{mn} = \frac{d^n I_{ds}}{dV_{gs}^n}, \quad \text{where } n = 1, 2, 3 \tag{1}$$

The device Figures of Merit is mathematically described as

$$VIP_2 = 4\frac{g_{m1}}{g_{m1}} \tag{2}$$

Table 1 Parameters values used in DGAA and GAA

Symbol	Parameter	Value	
		DGAA	GAA
L	Channel length	30 nm	30 nm
R_1	Outer radius	14 nm	10 nm
R_2	Inner radius	4 nm	–
N_a	Channel doping	10^{17} cm^{-3}	10^{17} cm^{-3}
t_{ox1}, t_{ox2}	Oxide thickness	2 nm (each)	2 nm(t_{ox})
ϕ_{m1}, ϕ_{m2}	Work function	4.8 eV	4.8 eV(ϕ_m)

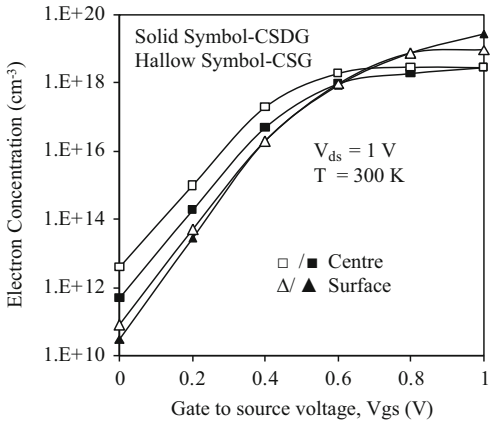

Fig. 2 Electron concentration at z = L/2 at 1 nm below the surface and centre of the channel of DGAA and GAA MOSFET

$$VIP_3 = \sqrt{24\frac{g_{m1}}{g_{m3}}} \tag{3}$$

$$IMD_3 = \left[\frac{9}{2}(VIP_3)^3 g_{m3}\right]^2 R_s \tag{4}$$

In this work, value of internal resistance R_S is 50 Ω for RF applications [20, 21]. VIP2 and VIP3 represent the extrapolated gate voltage at which the second order and third order harmonics become equal to fundamental tone in the device drain current respectively. VIP2 peak refers to cancellation of the second order derivatives. It is the ratio of first order to second order transconductance.

4 Results and Discussion

Figures 2 and 3 shows the effect of gate voltage extracted electron concentration and electron mobility at the surface and centre of the silicon film for DGAA and GAA MOSFET at V_{ds} = 1.0 V. At low gate voltage, mobile carriers spread out across the semiconductor substrate, which indicates

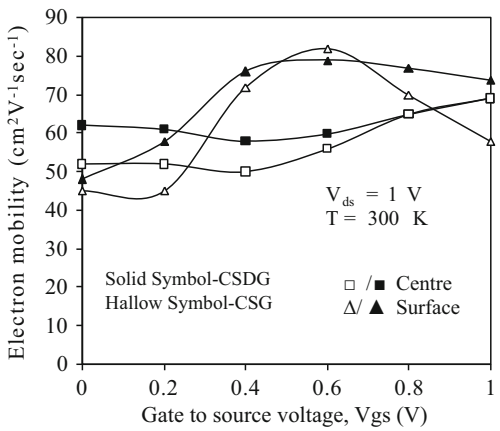

Fig. 3 Electron mobility at z = L/2 at 1 nm below the surface and centre of the channel of DGAA and GAA MOSFET

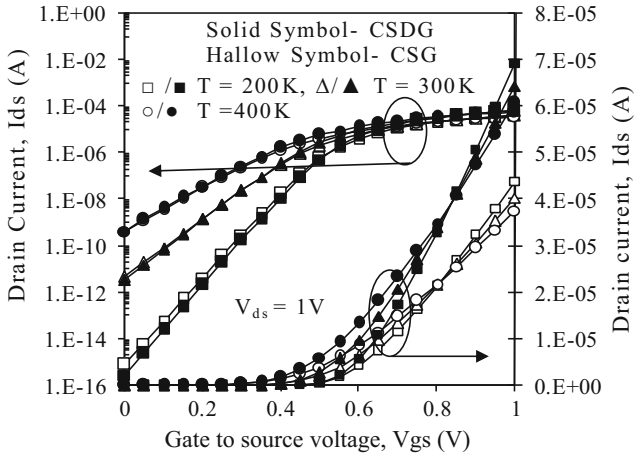

Fig. 4 Drain current versus gate voltage at different temperatures of DGAA and GAA MOSFET (Linear and logarithmic region)

the presence of volume inversion. Electron concentration is larger than doping level at the surface and centre of the substrate. As voltage increases, surface carriers have screening effect on the carrier at centre of the substrate. As a result potential at the centre of the substrate saturates and surface potential get increased. Thus the potential at the surface increases and is more than the centre of the substrate. DGAA MOSFET shows higher electron concentration at higher gate voltage and low concentration at the lower gate voltage than the GAA MOSFET which is required for high Ion/Ioff current ratio. Electron mobility in DGAA MOSFET shows higher value at the surface as well as at centre at lower gate voltage than the GAA MOSFET. As gate voltage increases, the mobility at centre is becoming equal with GAA but surface mobility decreases more rapidly than the DGAA MOSFET.

Figures 4 and 5 show the transfer characteristics and output characteristics for DGAA MOSFET at various temperatures and the results are compared with that of GAA MOSFET. As evident from the figures, the drain current when $V_{gs} = V_{ds}$ = 1 V is much higher in case of DGAA MOSFET. The presence of two cylindrical gates in specified DGAA MOSFET leads to

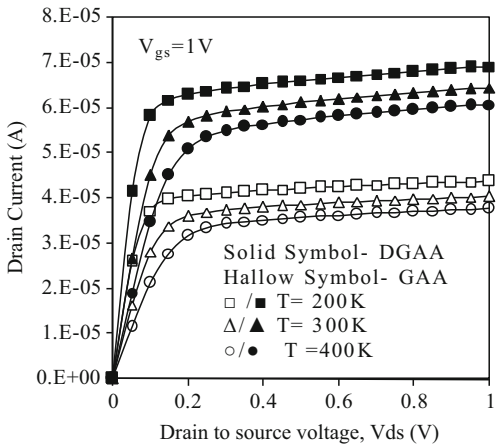

Fig. 5 Drain current as a function of Vds at different temperatures of DGAA and GAA MOSFET

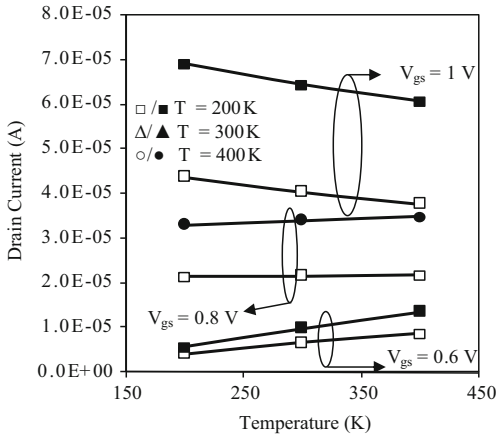

Fig. 6 Drain current versus drain to source voltage at different temperatures. (Solid Symbol: DGAA and Hollow Symbol: GAA)

increase in surface area of the conducting channel. Also the gate controllability over the channel increases which eventually increases the total drain current compared to GAA MOSFET.

In Fig. 4, the drain current in sub-threshold region for DGAA MOSFET is less than GAA MOSFET as shown in log scale. It shows that there is cross-over of the drain current at $V_{gs} = 0.8$ V for various temperatures Fig. 5. At lower gate voltage i.e. below 0.8 V, output current (Ids) increases with the increase of temperature but above that decreases in current is seen with the increase of temperature in term of mobility degradation due to enhanced scattering. Figure 6 shows the variation of drain current with temperature at cross-over gate voltages at $V_{ds} = 1$ V. It is seen that at gate voltage, $V_{gs} = 0.8$ V I_{ds} does not change with temperature. At gate voltage higher than 0.8 V, the drain current decrease with increase in temperature, whereas gate voltage smaller than 0.8 V, the drain current increase with an increase in temperature.

Figure 7 shows the variation of trans-conductance with gate to source voltage at various values of temperatures. The results are compared with GAA MOSFET. The trans-

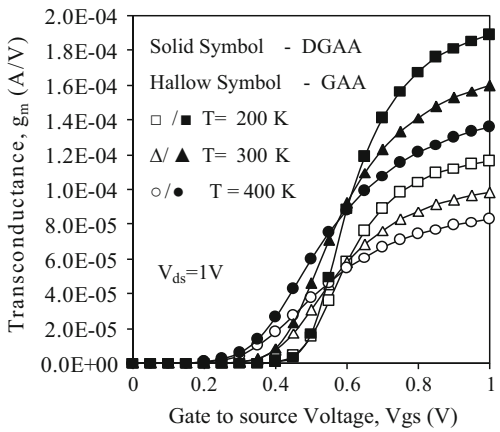

Fig. 7 Trans-conductance as a function of gate to source voltage at different temperatures

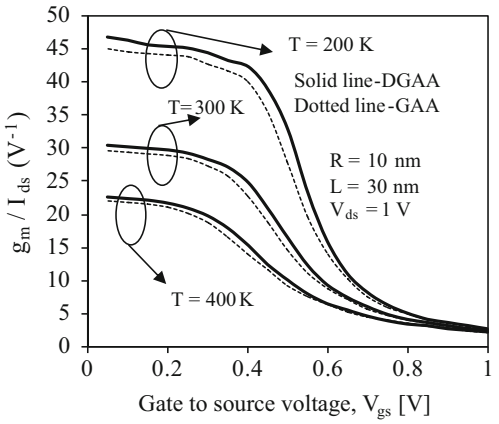

Fig. 8 g_m/I_{ds} as a function of gate voltage with temperature as a parameter

conductance is not only important for analog/RF application, it also important to choose optimum bias point. For any device, the cut-off frequency is maximum at optimum bias point. The increased current drivability and large drain current leads to high value of transconductance in DGAA MOSFET.

Figure 8 shows the variation of transconductance generation efficiency (g_m/I_{ds}). Slope of g_m/I_{ds} ratio reflects the steepness of sub-threshold slope. The excellent g_m/I_{ds} value is near in weak inversion region related to near ideal value of sub-threshold 60 mV/decade. For g_m/I_{ds} between 10 V^{-1} and 5 V^{-1} corresponds to a gate voltage from 500 mV to 700 mV typically used for analog/RF bias [22]. Usually the limiting value of sub-threshold slope is 60 mV/decade at g_m/I_{ds} value of 40 V^{-1}. From the figure it is evident that as temperature decreases to 200 K, g_m/I_{ds} increases beyond 40 V^{-1} ($\approx$ 45 V^{-1}) thus reducing the sub-threshold slope below 60 mV/decade. From the figure it is also evident that g_m/I_{ds} is higher in case of DGAA MOSFET [23].

Figure 9 shows the variation of gate capacitance with gate to source voltage of DGAA MOSFET and GAA MOSFET. DGAA MOSFET has inner gate capacitance and outer gate capacitance. When both the channel starts conducting, the

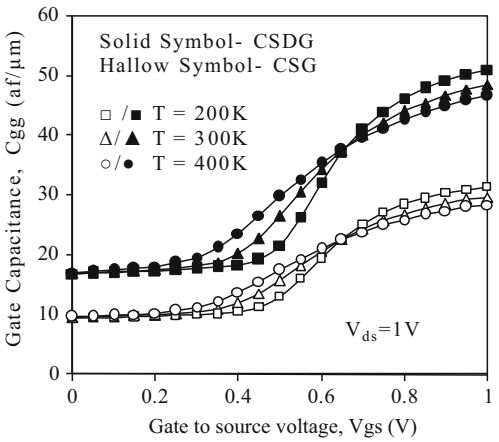

Fig. 9 shows the gate capacitances of GAA and DGAA MOSFET with respect to gate to source voltage for different temperature

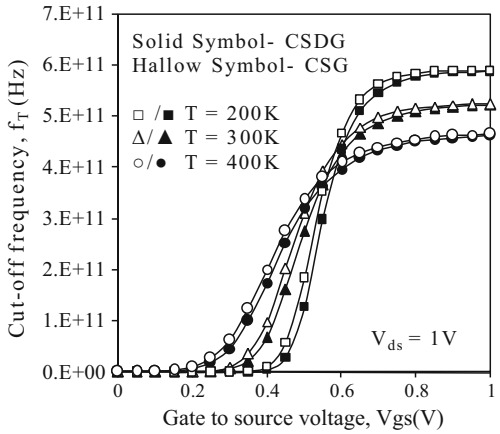

Fig. 10 Cut-off frequency of GAA and DGAA MOSFET with respect to gate to source voltage for different temperature

inner gate capacitance and outer gate capacitance comes in parallel as in DG MOSFET, which increasing the total gate capacitance of DGAA MOSFET. Gate capacitance of DGAA MOSFET is higher than the GAA MOSFET. When the total gate capacitance of the DGAA MOSFET is taken in account, the cut-off frequency becomes comparable to GAA MOSFET as shown in Fig. 10. Table 2 shows the impact of variation in temperature on analog/RF FOMs of GAA and DGAA MOSFET at V_{ds} = 1 V. g_m/g_d is the intrinsic gain of the device and it is higher in case of DGAA MOSFET and decreases with the increase in temperature. Thus the gain of the device can be retained higher at low temperatures. For digital applications I_{on}/I_{off} should be as high as possible. In DGAA MOSFET, it can be seen that trans-conductance, drain on current and I_{on}/I_{off} are higher compared to GAA MOSFET. Table 3 shows the impact of thickness variation on I_{on}/I_{off}, Sub-threshold Slope (SS) and I_{off} current. From the table it is clearly evident that Sub-threshold Slope and I_{off} current increases, while I_{on}/I_{off} decreases with the increase of silicon pillar radius. This is due to decrease in controllability with increase in silicon pillar thickness so off state current increases.

Although DGAA device shows excellent analog performance and it needs to be analyzed for reliability particularly in terms of linearity performance for radio frequency integrated circuit (RFIC) design. VIP2, VIP3 and IMD3 are the important figure of merits which reflects the nonlinear behavior

Table 2 Impact of temperature variation on analog/RF FOMs of GAA and DGAA MOSFET at Vds = 1 V

Temperature(K)	T = 200		T = 300		T = 400	
Devices	GAA	DGAA	GAA	DGAA	GAA	DGAA
g_m(mA/μV)	1.85	3.0	1.56	2.54	1.32	2.16
g_m/g_d	36	42	29	33	25	28
I_{on}(μA/μm)	698	1100	643	1030	600	968
I_{on}/I_{off} (× 10^6)	5.86E4	2.48E5	8.67	18.6	0.09	0.14

Table 3 Impact of thickness variations on analog/RF FOMs of GAA and DGAA MOSFETs at temperature 300 K

V_{ds}	Linear region = 0.1 V				Saturation region = 1 V			
Device	DGAA		GAA		DGAA		GAA	
Radius (nm)	8	10	8	10	8	10	8	10
SS(mV/dec)	65	74	69	75	66	76	70	78
I_{off} (pA/μm)	0.8	4.5	0.7	5.2	2.6	55.5	3.8	74.5
$I_{on}/I_{off} \times 10^7$	9	1.6	5.9	0.8	2.3	1.9	1.6	0.87

and inter-modulation distortion of the device. In order to maintain linearity at high frequency and to minimize the inter-modulation distortion, it is desirable to have high VIP2, VIP3 and low IMD3. The variation of VIP2 with gate to source voltage V_{gs} is shown in Fig. 11.

The higher VIP2 value results in reduced harmonics distortions in the case of DGAA MOSFET as compared to GAA MOSFET. The VIP3 peak signifies the cancellation of third order nonlinearity derivative by device internal feedback around second order nonlinearity [24]. It can be clearly seen from Fig. 11 that the DGAA MOSFET has higher peak value of VIP3 than the GAA MOSFET.

Figure 12 shows the variation in the third order inter-modulation distortion IMD3 as a function of gate bias for GAA and DGAA MOSFET at 300 K temperature. IMD3 originates from the nonlinearity behaviour of transistor in static characteristics, which causes degeneracy in the signals in wireless communication system [20]. From the figure it is seen that, at room temperature below threshold voltage DGAA MOSFET shows a little lower value of IMD3 in comparison to GAA MOSFET and above threshold voltage higher value of kink point. Low value of IMD3 and higher value of kink point signifies the cancellation of harmonics distortions [17, 24].

Figure 13 illustrates the comparison of maximum transducer power gain of GAA and DGAA MOSFET architecture at a wide range of temperature. Maximum Transducer Power Gain

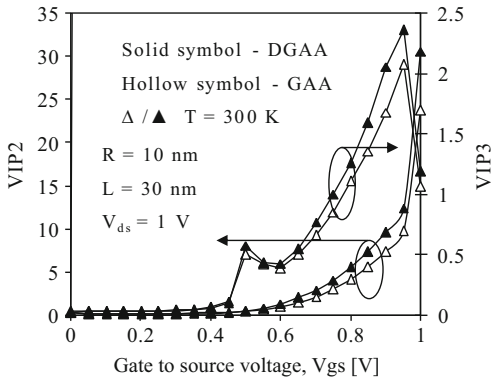

Fig. 11 VIP2 as a function of gate voltage for GAA and DGAA MOSFET

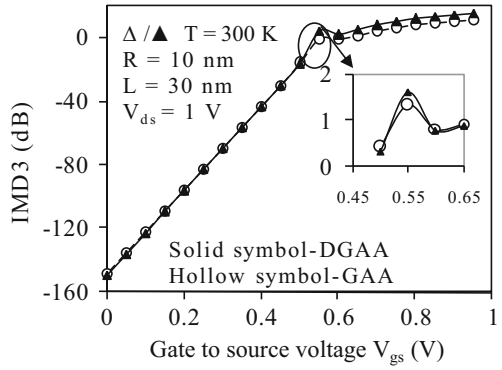

Fig. 12 IMD3 as a function of gate to source voltage for GAA and DGAA MOSFET

can be calculated at any frequency. But form from Fig. 10 in the manuscript, it is evident that the both the devices i.e. GAA and DGAA have cut-off frequency more than 100 GHz. Therefore F = 100 GHz is considered for calculating the power gain. For microwave applications, the maximum transducer power gain should be as high as possible. As is evident from the figure, DGAA MOSFET shows much higher gain than the GAA MOSFET.

5 Conclusion

In this work, a dual gate-all-around (DGAA) MOSFET is analyzed for suppressed harmonic distortions and SCEs. The analog performance and linearity investigation of the device is carried out and DGAA MOSFET shows the merit for good analog performance. A comprehensive comparative study has been carried out for the GAA and DGAA MOSFET at different temperatures. Due to excellent gate controllability on the channel and more channel area in the specified region in DGAA design, a tremendous enhancement in drain on current and trans-conductance is achieved. Electron concentration and mobility shows excellent behaviour for DGAA MOSFET. Linearity FOMs i.e. VIP2, VIP3, IMD3 insures suppressed harmonic distortions in DGAA MOSFET. Thus, DGAA MOSFET may be a good reliable candidate for future switching applications.

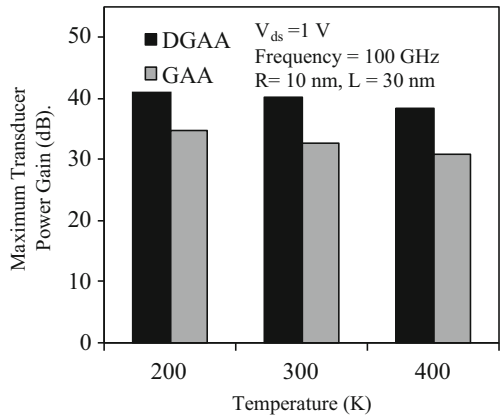

Fig. 13 Maximum Transducer Power Gain of the DGAA and GAA MOSFET at various temperatures

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