

Trench Gate Power MOSFET: Recent Advances and Innovations

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Chapter 1

Trench Gate Power MOSFET: Recent Advances and Innovations

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The trench gate MOSFET has established itself as the most suitable power device for **low to medium voltage power** applications by offering the **lowest possible ON resistance** among all MOS devices. The evolution of the trench gate power MOSFET has been discussed in this chapter, starting right from its beginnings to the recent trends. The innovations in the structural improvements to meet the requirements for an efficient operation, the progress in the fabrication process technology, the characterization methods and various reliability issues have been emphasized.

I. INTRODUCTION

From the very beginning in the history of mankind, there have been continuous and systematic scientific efforts to make our lives easy and comfortable. The development of power electronic devices is one of the steps towards that goal as these devices provide the means to control heavy electro-mechanical loads, industrial machines etc. to perform difficult tasks that would have been impossible otherwise. In these applications, a huge amount of electrical energy is required, which is acquired from an electrical source and stored in various elements and finally released in a controlled manner for our intended use of driving various devices and systems. The basic goal of controlling the flow of energy from its source to the load in an efficient manner with high reliability is accomplished by using the design concepts of electrical engineering with sophisticated analytical tools and efficient power electronic devices of small size, light weight and most importantly the low cost.

We have entered the age of limited energy resources amidst an emerging energy crisis. Therefore, highly efficient, rugged and reliable power electronic devices are required so that without consuming much energy, a variety of our needs may be fulfilled within the economical and manufacturing constraints. To meet the energy efficiency demand, there is a need for efficient power MOSFETs, capable of delivering high power without consuming a significant part of it. Out of a variety of possible options, trench gate architecture of power MOSFET provides the most efficient performance as a discrete power device for relatively low

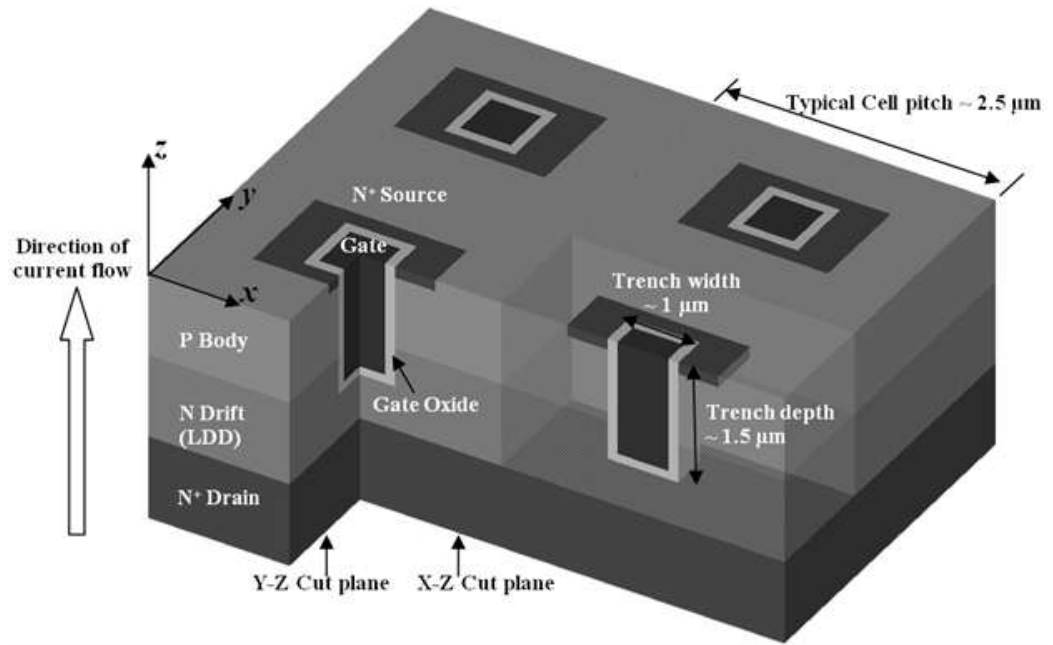


Fig. 1: Schematic 3D view of a trench gate power MOSFET showing typical dimensions.

voltage applications due to their lowest achievable ON-state resistance (R_{ON}) than any other structure of otherwise similar specifications.

A trench gate MOSFET is basically an attempt to make a complete chip conduct the current vertically from one surface to the other so as to achieve a high drive capability. It is realized by packing millions of trenches on a chip, deep enough to cross the oppositely doped 'body' region below the top surface. Each trench houses a gate dielectric and gate electrode to control the current conduction in its vicinity by the virtue of field effect. The schematic 3D view of a part of a trench gate MOSFET, with its cut sections along two vertical cut planes, is shown in Fig. 1 indicating four adjacent cells (each containing a trench). Similar to any other MOSFET, a trench MOSFET cell contains the drain, gate, source, body and the channel regions but exhibits a vertical direction of current flow. All the cells are connected to work in parallel in order to reduce the value of R_{ON} . In addition, it has a lightly doped drain (LDD) region between the channel and the drain to make it capable of sustaining large voltage in OFF-state condition. In the ON-state condition, the charge carriers are simply drifted through the LDD region towards the drain due to the potential difference across it. Therefore, the LDD region is also known as the 'drift region'.

The major design considerations of a trench gate power MOSFET are lowering of R_{ON} , enhancement of breakdown voltage (V_{BD}), reduction in switching delays, enhancement in transconductance, enhancement in dV/dt capability, high damage immunity while switching large current in inductive loads and minimization of energy losses. In a given structure, all the parameters are



technologically linked with each other and none of these can be adjusted independently. For example, thickness and doping concentrations of the drift and the body regions decide the VBD and RON. Similarly, the gate oxide thickness decides the threshold voltage (V_{Th}), transconductance and gate capacitance. Therefore, the design of a trench gate MOSFET for a specific application is a tradeoff among its performance parameters. With the passage of time, various improvements have been suggested, analyzed and implemented to modify the basic device structure for improving these tradeoffs.

As far as energy efficiency is concerned, there are two types of energy losses in a power MOSFET that need to be suppressed. The first and foremost is the conduction loss arising from the non-zero RON and the other one is the switching loss caused by charging and discharging of the gate electrode while switching the device ON and OFF. This charge is known as gate charge (QG). These two losses are also interlinked. Any attempt to reduce the RON in a conventional structure results in an increased QG, and vice versa. Therefore, a real improvement in device performance is considered only if the product of RON and QG is reduced. Therefore, $RON \cdot QG$ is called figure of merit (FOM).

II. EVOLUTION OF TRENCH POWER MOSFETS: A BRIEF HISTORY

The semiconductor power devices have evolved in the second half of the 20th century [1-4], when the first significant device was demonstrated by Hall in 1952 using germanium mesa alloy junction [5]. This was the first step towards getting rid of the bulky, large and less reliable vacuum tube devices and therefore it attracted a lot of research interest in semiconductor electronic devices, resulting in a rapid development in the semiconductor technology. Soon after its first commercial launch in 1954 by Texas Instruments [6], Silicon based Bipolar Junction Transistor (BJT) has taken over the majority of the power device market by replacing the vacuum tube devices. However, later on it was realized that the BJT was also not suitable for various emerging power applications due to many problems associated with it [7, 8], e.g., its positive temperature coefficient of current that makes it susceptible to thermal runaway, the charge storage problem in the base that makes it a slow switch, secondary breakdown and the low input resistance that necessitates a large controlling current consumption. These shortcomings of BJTs motivated intense research for their improvements as well as search for a new and better device. In this direction, the metal oxide semiconductor (MOS) based insulated gate devices have been investigated and found to be the most promising from various perspectives. A MOSFET, due to its insulated gate, puts a very little load to the input circuitry and being a majority carrier device, it does not suffer from the charge storage problem. Furthermore, the negative temperature coefficient of current not only makes MOSFETs better from the thermal runaway point of view but also makes them suitable for parallel conduction. With all these advantages, people started exploring the suitability of the MOSFETs in the power electronic applications. The only difficulty found in

the MOSFET as a power device was **its large ON-resistance** that results in conduction losses. It was quite attractive to overcome this difficulty in an otherwise near ideal power device, i.e., MOSFET that had the potential to replace the bipolar transistors. The main structures that have been proposed in early 1970's to implement the insulated gate controlled devices were LDMOS, VDMOS, and VMOS [9].

Around early 1980's the power MOS transistors had started competing bipolar power devices in power-handling capability when the technological improvements made it possible to successfully realize very short active channels and incorporation of a lightly doped region between the channel and the drain for improving both ON and OFF state device performance [9]. This structure was double diffused MOSFET (DMOSFET). Later on the V-grooved MOSFET (VMOSFET) had been developed as a potential candidate to meet the upcoming power requirements with lower conduction losses, but they were suited only for low voltage applications [10-21]. Development of VMOSFET was the first attempt of making a vertical MOSFET and is considered to be the major breakthrough in the power electronics because their large scale integration capability and the absence of parasitic JFET made them able to provide the lowest ON-resistance compared to other possible structures. However, the VMOSFET had a problem of low breakdown voltage due to the crowding of electric field lines at its sharp bottom. This problem was solved partially by smoothing the V-shaped bottom that resulted in the UMOSFET structure. By 1985, the advancements in the etching technology has enabled opening of rectangular grooves that resulted in the fabrication of a new vertical power MOSFET structure called rectangular grooved MOSFET (RMOS), in which the vertical channels along the sidewalls of the rectangular grooves were formed by a reactive ion-beam etching (RIBE) technique [22]. This is how the UMOSFET structure has further changed into its improved successor, the trench gate MOSFET. This structure was another major milestone of the progress of low ON-resistance and high packing density MOSFET structures and was demonstrated experimentally to have lower ON-resistance per unit area than other VMOS and DMOS structures [23-29].

III. STRUCTURAL ADVANCEMENTS AND INNOVATIONS

Although the ON-resistance offered by the trench gate MOSFET has been the lowest among various possible structures, the applications keep demanding **further reduction** in ON-resistance with sufficiently high breakdown voltage and reliability. To meet this ever persistent demand, various modifications in the basic trench gate structure with improved fabrication technology have been incorporated. Such important milestones are discussed in subsequent subsections.

A. Trench Optimization

The problems associated with the trench have motivated the development of improved and optimized trench structures. The major considerations at the

initial phase of their development were the **depth of trenches and the sharp corners**. In 1986, D. Ueda et. al. have realized the deep trench gate MOSFET having three times **smaller RON** than that of the best achievable structure with a shallow trench and have shown that the use of deep trenches had two additional advantages, i.e., **low spreading resistance due to the increased accumulation layer area** and complete **elimination of parasitic JFET**, reducing the RON [30]. Later on, the deep trenches have been further investigated experimentally as well as theoretically and found to have superior characteristics [31-34]. The deep trenches were also found to have better **immunity for the repetitive inductive switching** [35]. Another initial technological **limitation** was related to the sharp corners at the trench bottom having a **very strong corner effect**, i.e., crowding of electric field lines that exist even with the low fixed oxide charge density (Q_f). It was **investigated** that the doping concentration of **higher than 10^{17} cm^{-3}** was necessary for the case of $Q_f = 10^{11} \text{ cm}^{-2}$ to minimize the inversion at the corners that, on the other hand, can adversely affect the leakage currents along the trench [36]. The **thicker gate oxide** has also been tried as an **approach** to control the corner effect, but was found not very effective. **Finally, corner rounding** was found to be the only effective way to get rid of the corner effect. In its implementation, the area loss due to corner rounding is minimized by properly adjusting some of the parameters like substrate doping concentration, oxide thickness and corner curvature. To overcome the technological problems associated with the trench corner shaping, a novel fabrication process technique of pull-back has been suggested that uses hydrogen annealed trench surface [37-41]. Due to the virtue of silicon migration, it results in highly reliable thin gate oxide along with corner rounding [38].

The deep trenches with round corners were found suitable for lowering RON and increasing the breakdown voltage. However, as they extend deep into the drift region, the gate capacitances are enhanced affecting the **switching delays**. In a power MOSFET, the switching delay is a very important performance parameter and is mainly governed by the gate capacitance, especially the **gate-to-drain capacitance, CGD** that acts as miller capacitance in usual circuit configurations. Therefore, **CGD has to be minimized** to make the ON and OFF transitions fast. The WMOSFET is an attractive design that **reduces CGD by using higher gate oxide thickness at the trench bottom** and is realized using LOCOS and sub atmospheric CVD (SACVD) processes [42-45]. The structure was named as WMOSFET due to the 'W' like shape of its trench. The WMOSFET has been demonstrated experimentally to have a significant reduction in gate-drain charge QGD, a low RON and a good production process margin [43-45].

B. Body/Channel Profile Engineering

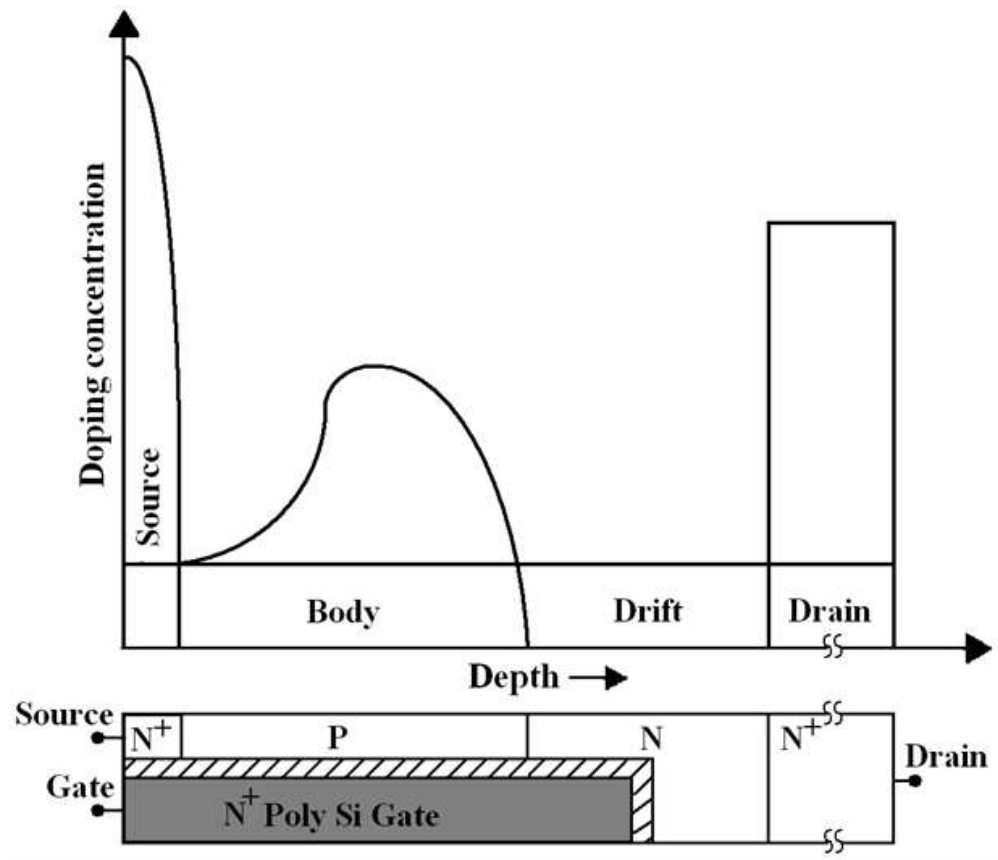


Fig. 2: Schematic doping profile of retrograde body trench MOSFET [46].

In order to achieve a low specific ON-resistance and low gate capacitance, a simple method of **retrograde body profile** has been suggested [46-48]. The retrograde body MOSFET (RBMOS) was realized by high energy implantation for body formation as shown in Fig. 2. In this structure, basically the doping concentration in the channel is adjusted in such a way that its drain-side gets highest concentration. This reduces the depletion width at the drain-side, resulting in the screening of drain voltage at the source-side and, therefore, allows a significant reduction in channel length without degrading the punch-through voltage. Low thermal budget and easy trench gate process are its additional benefits. Comparing with the conventional device, the specific ON-resistance and the figure-of-merit have been reported to improve by 38% and 70%, respectively, in the RBMOS device [46].

Another type of channel engineering that reduces the channel resistance is the **use of hetero-epitaxy**. SiGe epitaxial layer in the body region has been demonstrated to provide lower RON, **but at the cost of a little degradation in**

thermal performance [49]. This degradation can be retrieved by incorporating carbon to realize the SiGeC body/channel [50]. A device with the SiGeC body shows significantly smaller temperature sensitivity of the drain current as compared to the Si and SiGe devices, while the higher drain current advantage of SiGe channel is still preserved in the SiGeC device.

C. Drift Region Engineering

The drift region is designed to sustain a large drain to source voltage in OFF condition and, therefore, is doped lightly. However, due to the low doping concentration, its resistance becomes large resulting in higher ON-resistance of the device. The difficulty behind simultaneously meeting the requirement of low ON-resistance and high breakdown voltage becomes severe as these two parameters are found to be related by about 2.5th power relation [51-63]. Various novel structures like floating island, super junction and RESURF (reduced surface field) effect have been worked out to improve the trade-off between specific ON-resistance and breakdown voltage, such as oppositely doped floating island devices (FLIMOSFET and FITMOSFET) [51-59], super-junction/COOLMOS devices [60, 61], Opposite Doped Buried Regions (ODBR) MOSFET [62], and P-buried layer Schottky barrier diodes [63]. Incorporation of the floating islands inside the drift region of the device modifies the electric field distribution in the bulk in such a way that there exist several (depending on the number of buried islands) small peaks in electric field profile. This results in a significant lowering of the highest peak [56]. The formation of multiple peaks allows increasing the doping concentration up to the level at which the highest peak of electric field is just less than the breakdown field, thereby improving the relation between RON and VBD as well as reducing the FOM [59]. Additionally, the reverse recovery of the body diode becomes faster in these devices, reducing the switch OFF delays. On the other hand, there is a drawback of floating islands that the JFET effect is enhanced, resulting in the enhancement of RON under AC mode of operation. This issue was solved by the passive hole gates to control the minority carriers during AC operation that resulted in the RON equivalent under both AC and DC operations [59]. The trade-off between VBD and RON is also improved by using floating islands in elliptical forms [57-59].

Many efforts have been made for incorporating super junction or RESURF structure in trench gate MOSFETs, which is not straight forward in such non-planar devices. The first SJ trench structure was realized by T. Nitta et. al. by making the P and N stripe structure in alternating fashion fabricated by angled implantation in very deep trenches [64]. Though the structure was not actually the trench gated MOSFET, it was an important contribution as it confirmed the field relaxation possibility in vertical trench structures and motivated further research in this direction. Soon after this attempt, Y. Hattori et. al. have realized the first real SJ trench gate MOSFET [34], wherein an accurate control of the impurity concentration of N drift region was achieved by As- ion implantation at 10o angle

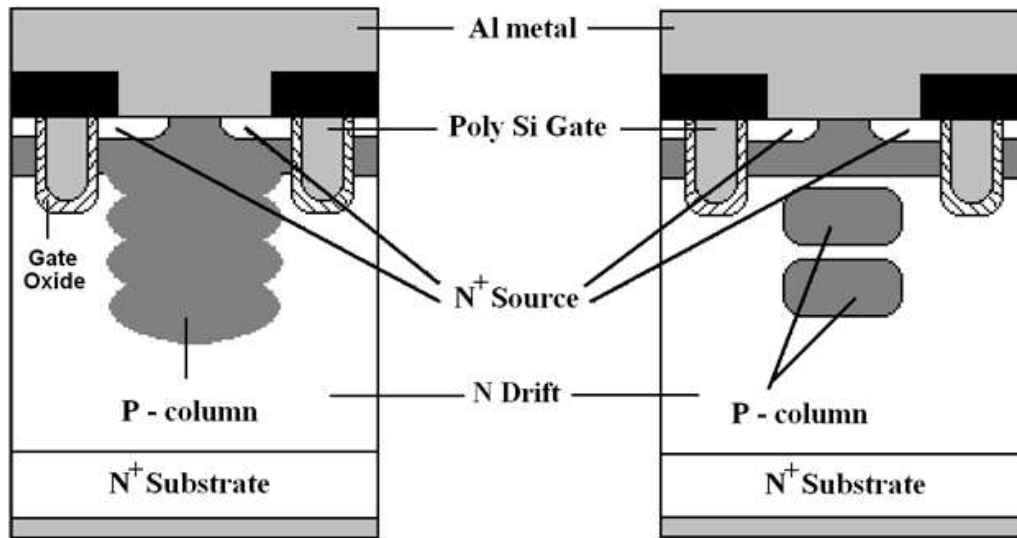


Fig. 4: A SJ trench MOSFET realized by implanting P-column base using multiple implants of boron in N-drift region, having (a) continuous P-base [66], (b) split P-base [67].

and chlorine source gases simultaneously [74]. A further improvement in this structure has been suggested, wherein the trench gates were made orthogonal to the P/N columns, allowing independent control of trench gate pitch and p/n column pitch [75]. This structure has shown 36% lower figure of merit. Moreover, the unclamped inductive switching endurance of this SJMOSFET was found to be 30% larger than the conventional trench MOSFET.

A new split gate, stepped oxide RESURF trench MOSFET is recently attracting a lot of research interest as it promises lower FOM. The structure has been examined experimentally [76] as well as through TCAD simulations [77] to have better switching characteristics due to lower gate charge. The use of double epi-layer drift region [78, 79] and asymmetric wing cell [80] are the other RESURF techniques proposed for improving the breakdown performance.

D. Use of Metal Substrate

The major efforts made for reducing RON are usually based on the lateral scaling or pitch reduction. This approach is effective in reducing the channel resistance [81], but at the same time it causes gate charge to increase, which deteriorates the switching performance. Also, aggressively reducing the cell pitch causes the resistance contribution of silicon substrate to the total RON quite significant [82]. It has been shown that the 30 V n-channel trench gate MOSFETs, with a pitch of 4.0 μm , have 25% contribution of the specific RON from the silicon substrate having a resistivity of 3.5 $\text{m}\Omega\cdot\text{cm}$ and thicknesses in the range of 200 μm [83]. Suppressing the substrate resistance contribution by using metal substrate, instead of silicon, may allow a significant reduction in the ON-

resistance, without compromising gate charge. The incorporation of metal substrate is actually realized by transferring the silicon device layers to the metal substrate at the end of the device fabrication. This technology is known as silicon-on-metal (SOM) technology [84]. The trench MOSFET, fabricated using SOM technology on copper substrate, has demonstrated significant improvement in RON, energy efficiency and thermal conductance [84, 85]. The transient thermal resistance of the SOM device was also found to be much smaller than the silicon substrate devices. The increased biaxial compressive thermal stress in silicon, perpendicular to the channel was investigated by a 3D piezo-resistance model [85]. This stress results in an enhanced carrier mobility that in turn reduces the total device resistance. Additionally, an improved transient thermal conductance improves the ruggedness and reliability of the device.

IV. ADVANCEMENTS IN FABRICATION TECHNOLOGY

Being a device of commercial importance, the fabrication cost is the governing aspect of the trench gate MOSFET fabrication. Therefore, numerous attempts have been concentrated to cut down the fabrication cost while maintaining the high performance. A wide variety of methods for fabrication of trench devices have been inherited from the advanced semiconductor processing technology, but none of those has been found to be as superior in all respects as to displace all others. The fabrication usually involves a number of processing steps, such as, epilayer growth for drift region on a low resistivity silicon substrate and the growth of the body region over the substrate, trench creation by reactive ion beam etching, gate definition and contact-hole opening etc. All unit processes need special attention and online monitoring for consistently getting high yield. Out of various process steps, **lithography and trench etching** are the most important processes because a little deviation in these may largely degrade the performance and the overall yield. The impact of lithographic limitations on the device performance, as studied experimentally on 0.6 μm pitch devices [86, 87], indicates that scaling down the trench and contact width is achievable **by DUV lithography**.

To meet the requirement of low RON, a very high channel density is necessary that can be achieved by the self aligned fabrication process because otherwise the alignment tolerances between two lithography steps may become a bottleneck. Entire technological improvement efforts can be categorized in two: trench etching technology and self aligned process technology, because other process steps are not at all critical. The development of technologies and their issues are discussed in following subsection.

A. Trench Etching Technology

Opening **high aspect ratio** trenches reliably with controlled depth is the most important process step in realizing a high performance trench gate MOSFET. For reducing the RON, it is necessary to thin down the epitaxial layer and

minimize the cell size which requires exact control of trench depth in order to maintain the desired drain-to-source breakdown voltage. Another important issue is the capacitive coupling between the gate and drain regions that governs the switching speed. The best switching performance can be achieved with a narrow trench that extends just beyond the P-N interface. The trench width is governed by the photolithographic capabilities and the compatibility with subsequent processing steps. The P-N junction depth can also be controlled accurately by ion implantation. Therefore, trench depth becomes the most critical parameter to control during the etching of silicon trenches. The smoothness of the trench sidewall that minimizes the gate leakage current, the sidewall profile that is required for its proper filling with poly Si, and trench bottom rounding to avoid the pre-matured device breakdown due to electric field crowding at sharp corners are the other parameters which need to be considered for making a high performance, reliable trench device. The importance of trench etching process can be realized by the fact that the first successful realization of trench MOSFET, to an acceptable level, could be achieved only by an improved silicon trench processing technology [88, 89] and using a novel trench fabrication process only, the channel electron mobility approaching 87% of its bulk value could be obtained [90]. The control on trench etching process led to a narrow trench formation process and the double trench (one additional trench for contact) structure that enabled the 3rd generation, high performance trench gate MOSFET [91].

The trenches in a power MOSFET are usually etched using the SF₆/O₂ plasma. The balancing of bi-directional etching reactions between F atoms and the silicon substrate forms SiF₄ by-products. On the other hand, the oxygen in the plasma reacts with the etched silicon sidewalls to produce SiO₂ and thus provides the sidewall passivation. When an additional sidewall passivation is required, for example in case of deep trench opening, the CF₄ or SiF₄ is added into the process gas mix [92].

Since repeatability and yield have become the major governing forces for the power electronic devices, it is important to have a rugged and reliable fabrication process for the trench MOSFETs. The trench depth control during etching process, in a trench power MOSFET, is more difficult than that in many other dry etching applications because of the absence of stop layer where etching is to be terminated. Thus, the conventional etch stop technique of optical emission spectroscopy (OES) cannot be utilized for trench depth control and controlling that by adjusting the etching rate and time is also not a reliable method as it is subjected to many inconsistencies, affecting the repeatability and yield. Therefore, trench etching requires a sophisticated Reactive Ion Beam Etching (RIE) machine with in-situ depth monitoring system. To achieve the trench depth repeatability and yield up to the desired level, it is necessary to integrate a real time depth-monitoring and analysis tool embedded with the etching chamber itself. One of such techniques is the Interferometric End Point Detection (IEPD) which is also

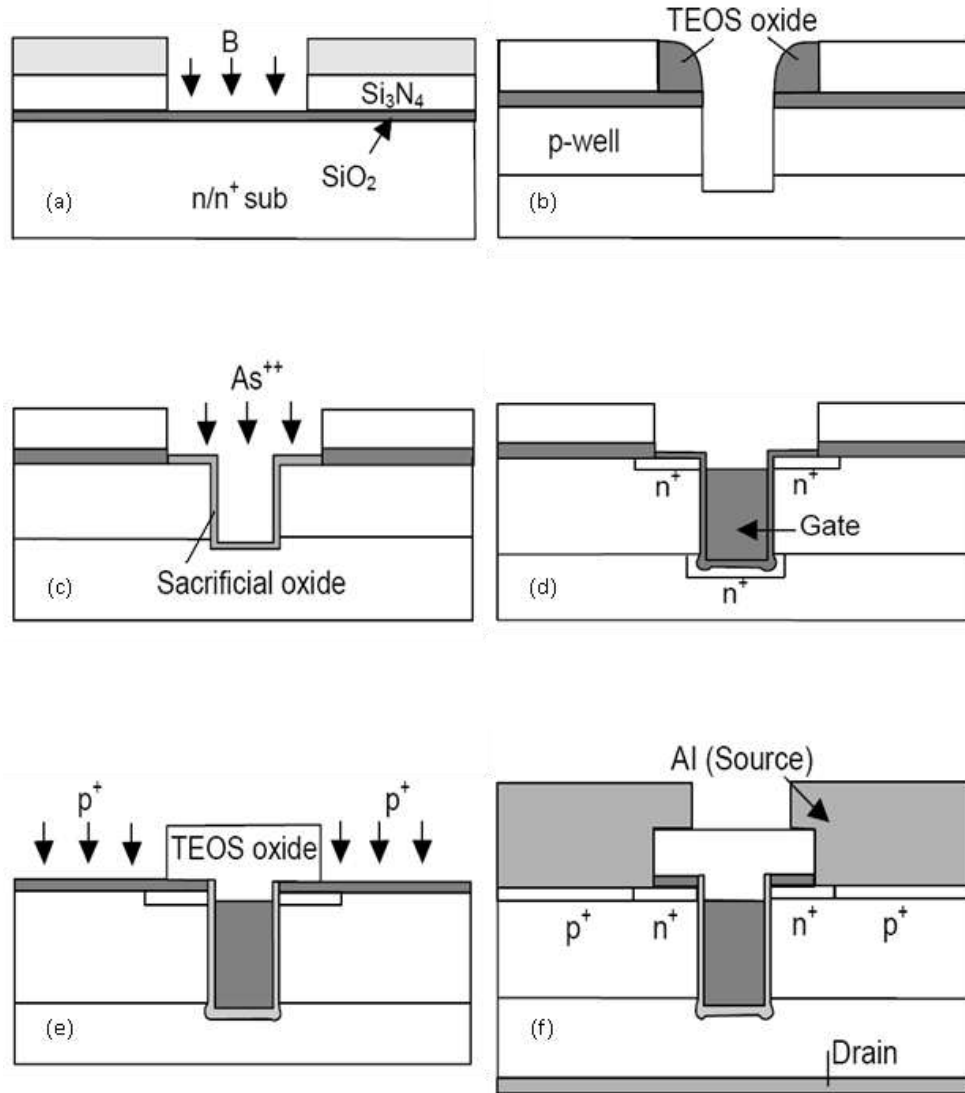


Fig. 5: Self aligned process sequence of fabricating trench MOSFET, using oxide spacer technique [102].

suited for high aspect ratio trenches. Implementation of this technique has been demonstrated successfully for trench device applications [93].

B. Self Aligned Fabrication Process

The techniques of trench filling with Poly Si and etching it back along with selective etching of doped and undoped poly Si have been employed initially for realization of most of the processing steps, such as channel formation, gate definition, and contact-hole opening, through a single masking step [94, 95]. This has permitted a remarkable increase in packing density and therefore attracted a lot of attention and sincere efforts for further simplification and advancement in the self aligned process techniques. Shenai has suggested the use of poly Si pillar (formed while trench filling and removal of RIE mask) for spacer formation that gives self aligned contacts for source [39]. In another technique, local oxidation of

poly Si pillar [96, 97] enabled self aligned contact holes for source/body connection. A well studied and implemented method of forming self aligned source was the use of oxide spacer [98-100] by deposition and RIE etching of TEOS oxide to expose surface areas of the N-epi where the trenches are to be formed. Then the exposed N-epi silicon and underlying P-body and N-drift region are etched away to define trenches [98, 101]. This approach was further modified by performing N⁺ ion implantation after removal of oxide spacer and also by making it more reliable by smoothing of trench corners using H₂ annealing [37, 102-104]. A typical self aligned process sequence is shown in Fig. 5. Silicidation [105] and triple trench etching [106] were the other methods tried for making self aligned source/body contact.

A different approach of fabricating very high density trenches was demonstrated by J. Zeng, et. al. [107], wherein the poly Si gate is recessed into the trench, leaving a region to be filled by the BPSG the next step. The depth of the recess region determines the final thickness of BPSG, which is a design parameter for getting desired gate-source voltage rating. The BPSG layer is re-flown and is then etched back using the flat silicon surface as the end point. BPSG then serves as the isolation regions. In next step the BPSG isolation is planarized and the space occupied by BPSG at the surface is completely removed. This results in very closely spaced trenches. The finer process details are explained in [107]. A few more similar approaches of self aligned trench gate formation are discussed in [108, 109].

C. Other Technological Innovations

The thicker gate oxide is preferred at the drain side to reduce the capacitive coupling of gate and drain regions that needs realization of larger bottom oxide thickness. The oxide bypassed structure utilizes the oxide thickness control in fabrication instead of the doping concentration control and has been shown to obtain RON versus VBD tradeoff limit beyond the conventional unipolar silicon limit [110, 111]. The structure also provides the option to utilize an additional bias voltage to compensate possible process variations in order to enhance the VBD. The structure, fabrication process and the laboratory results on the tunable oxide-bypassed trench gate power MOSFET have shown that this technology is feasible in making super junction MOSFET devices. Another innovative technique is the LOCOS process at the trench bottom that results in a W-shaped trench structure [42, 81, 112, 113] which promises 40% reduction in QG and about 58% improvement in RON.QG figure-of-merit [114, 115].

V. CHARACTERIZATION TECHNIQUES

Characterization is an unavoidable and essential step in any semiconductor device manufacturing process because only using this step one can predict the final behavior of the device in its intended application before its actual deployment, saving a lot of time, money and efforts. Additionally, it provides

feedbacks to the process engineers to avoid/minimize all the systematic and random errors in the device fabrication by fine tuning and controlling the process parameters to readjust the desired device parameters, if required, for yield improvement. Various standard techniques are used for material, process and device characterization [116] for this purpose.

Since in a trench MOSFET, majority of active parts are located deep in the silicon, the extraction of important device parameters like defect density in the epi-layer, doping-concentration variations in epi-layer (due to drive-in anneals and dopant out-diffusion), p-well doping concentration, and SiO₂/Si interface quality is a challenging task. To overcome this problem, gate-controlled diode (GCD) current has been suggested to be used as the process control monitor [117]. Due to very high packing density, the effective transistor width becomes several meters. Therefore, W/L ratio becomes very large as the transistor channel length remains in the sub-micrometer range. The increased W/L ratio makes the total GCD current large enough for its reliable measurement. The GCD current has been shown to have signatures of the process conditions, such as silicon doping concentration in the epi-layer and effect of thermal cycles on it. The high-frequency and quasi-static CVs have also been used to extract the critical device parameters, like epi-doping-concentration, defect density in the epi, p-well doping concentration, and SiO₂/Si interface quality [117].

The terminal current-voltage characteristics and gate charge transients are the usual methods to extract the performance parameters like ON-resistance, breakdown voltage, transconductance, gate charge and most importantly the FOM. Since, the total gate charge QG mainly depends on the gate to drain charge QGD, the figure-of-merit (FOM) is also defined as the product of RON and QGD that is commonly used to quantify the performance of the power MOSFETs for a specified off-state breakdown voltage. Additionally, measurement of carrier mobility in the channel, transient capability and energy handling capability are the other suggested and employed techniques to characterize the trench MOSFET.

A. *Gate Charge*

When the gate of a power MOSFET is connected to the supply voltage to turn it ON, first the capacitances associated with the gate are charged. The charging of these input capacitances decides the switching speed. The amount of charge supplied to the gate for charging these capacitances is defined as the total gate charge. Estimating the gate charge not only allows us to get an idea about the switching delays and losses, it also provides a comparison among the switching performances of two devices from different manufacturers. Thus, gate charge is a more useful parameter from the circuit design point of view as compared to the gate capacitance. Using experimental and analytical gate charge transient analysis [118, 119], it has been shown that QGD itself is composed of accumulation, depletion, and inversion charges. The inversion charge is located mainly

underneath the trench bottom. The accumulation and depletion charge contribute each about 45% in conventional trench MOSFETs and can be reduced by using thick bottom oxide in a shallow trench device.

Another technique of analyzing gate charge utilizes a curve tracer. A curve tracer not only allows testing of the static parameters using DC characteristics, but can also show AC characteristics of the device. Due to the charging and discharging of capacitances of the device under AC signal, a phase difference exists between current and voltage. Therefore, the AC waveform of the power MOSFET generated on the curve tracer, serves to quantify its capacitance effect clearly and a qualitative idea about the various other capacitances may also be obtained, as discussed in [120].

B. Carrier mobility extraction

Extraction of carrier mobility in the channel is not straight forward. Various methods have been proposed to accurately estimate the value of carrier mobility in the channel of a trench MOSFET device. A method using fitting of experimental ON-resistance into an appropriate model has been proposed for extracting both the inversion and accumulation layer mobilities of electrons in n-channel trench MOSFET as a function of a wide range of effective electric field [121]. The split C-V method has been reported to be more accurate in evaluating the mobilities for the trench MOSFET which might have high interface states [122, 123].

C. Energy capability estimation

When a power MOSFET is switched ON or OFF, momentarily it is subjected to a very high current and high voltage simultaneously and therefore, may lead to excessive heat dissipation that may cause permanent device failure. The electrical or thermal instabilities within the device govern the Safe Operating Area (SOA) limits at the time of switching. Thus, designing of an optimum power device requires proper consideration for the SOA and its trade off with RON and VBD. The total energy that a device can safely handle is known as its energy capability (EC). The EC of a power MOSFET decides its energy switching capability and therefore is a very important parameter. The EC is measured by applying the controlled pulse train. The amplitude of the pulses and the duty cycle is increased continuously until the device fails. This measurement is applied in two different ways. In the first approach, an inductive load is switched OFF by the saw-tooth type power pulses, known as Unclamped Inductive Switching (UIS) [124]. In the second approach, the drain is clamped by a Zener diode to protect the device from avalanche operation, known as Clamped Inductive Switching (CIS) [125]. A theoretical and experimental comparison has been made between the two methods and it was found that in the CIS method, the measurement conditions are difficult to control independently and the results are dependent on the circuit parameters [126, 127] and therefore, a modified technique has been suggested wherein rectangular power pulses are applied to the device for excitation thereby

directly forcing constant current or voltage [128]. This method provides the most straightforward control over the device excitation.

D. Fabrication process control and monitoring

The process steps used to fabricate a trench gate power MOSFET are critical and need to be monitored and controlled for maintaining the desired performance and yield of the resulting device. The most critical step in the fabrication of trench gate power MOSFET is opening of trenches. Therefore careful monitoring of the trench depth, bottom, sidewalls and its subsequent filling with poly Si is very important for reliable device fabrication. The process characterization and monitoring need to be robust and should be applicable in the manufacturing environment. A conventional approach for process control in VLSI circuits is the use of MOS capacitor as a diagnostic tool. Similarly, the trench MOS capacitor may be analyzed using standard capacitance-voltage (CV) analysis and deep level transient spectroscopy (DLTS) to study dielectric/Si interface and bulk Si carrier traps in a trench gate MOSFET as reported in [129-131].

Model-Based Infrared Reflectometry (MBIR) is another useful technique for trench structure characterization [132]. It is used routinely for process control of deep trench DRAM devices and therefore can be employed in trench gate MOSFETs also for their process control. The technique is useful for measuring etch depth and monitoring the trench bottom at the time of trench opening. Furthermore, MBIR is also useful for detecting the voids in filled trenches and measuring poly Si fill depth after recess etch [133].

Various other techniques have also been employed for monitoring the trench gate MOSFET fabrication and control. The atomic force microscopy (AFM) has been shown to be effective for evaluating depth and resolving surface topological issues [134]. Use of secondary ion mass spectrometry (SIMS) has been demonstrated to be an effective approach for extraction of doping profiles in trenched regions within the MOSFET cells [135]. Scanning electron microscopy (SEM) has been suggested as an effective characterization tool for high-aspect-ratio three-dimensional structures with submicron dimensions [136] suitable for trenches. Angle-resolved X-ray photoelectron spectroscopy has been demonstrated to be very useful for monitoring of the surface composition of etched Si samples and depth profile in trenches [137]. The technique allows a full depth profile analysis of trenched structures by analyzing the exposed Si area, which is accessed in the trenches also, by using angled X-ray spectra.

VI. TECHNIQUES OF RELIABILITY ESTIMATION AND ASSURANCE

Reliability is a very important issue for a device like trench power MOSFET that has commercial importance and need proper investigation and assurance for consistent yield. Usually, local defects due to electrical over stresses (EOS) occur during the backend processes like source metallization and the wire bonding [138] that can be avoided by proper care. However, there exist varieties

of uncontrolled random mechanisms that may cause an early failure of a trench device. Some of the important concerns for early failure are the heavy ion radiation especially in the devices fabricated for space application, trench corners, oxide interface and hot electron degradation in addition to the usual process induced device failures, such as the poor interconnect of the poly gate and the metal, the bonding wire, and the etch process [118]. The aging failure is examined mainly through acoustic, electron and ion microscopy under extreme electro-thermal fatigue conditions. The de-lamination at the die attach is found to be one of the main aging modes related to the drastic increase in the drain resistance [138]. The avalanche behavior was investigated by measurements as well as electro-thermal simulations and found to be related to either of two mechanism, i.e., high energy consumption in the device and the high current being driven by it [139].

To make the trench MOSFET suitable for space applications, radiation hardness is another important issue as it may result in large shifts in I-V characteristics. Even a very small, micro-dose of the heavy ions may result in the parasitic transistor formation in the gate oxide and may have significant implications on the MOS devices for use in space. It is shown that they can lead to off-state leakage currents greater than 1.0 A [140, 141].

Other usual reliability concerns are related to the trench processing that primarily influence the device immunity to electrical stress, i.e., trench etching, trench cleaning and subsequent gate-oxide growth. Since the thermal-growth of gate oxide layer on the sidewall and base of a reactive-ion etched silicon surface is a three dimensional process, its interface with the Si at the bottom corners of the trench becomes the weakest region in the MOS structure and may cause serious reliability problems [39, 40, 129-132, 142-145]. Also, the thickness variations of the oxide layer at the sidewalls may result in the formation of voids while filling the trenches with poly Si. The oxide edge adjacent to the drain and the oxide/silicon interface are the most susceptible regions to damage [145].

The P-channel trench gate MOSFETs suffer from a peculiar reliability problem related to the Boron penetration from heavily boron-doped P+ poly-Si gate into the gate dielectric/Si-sidewall interface and into bulk Si [142], due to high diffusivity of Boron. The oxide-nitride complex gate structure is reported to overcome most of such reliability problems. It is shown that by optimizing this structure, high gate reliability same as that of a planar MOSFET can be obtained in trench gate MOSFETs [142]. The Boron doped (for body formation), n-channel trench MOSFETs have been examined using charge pumping technique [146] and it has been found that the hot electron effect is governed by the channel doping. The measurement of bulk current is a usual and conventional technique of estimating the hot carrier effect. However, recently the bulk current has been found to reach at its maximum at intermediate drain voltage [147]. This behavior

has important consequences for the hot carrier reliability evaluation of the transistors and need a careful further investigation.

The hot free carriers, with sufficiently high energy, cross over the Si–SiO₂ barrier and get trapped at the interface of the gate dielectric and the bulk. These trapped charges can induce large threshold voltage shifts due to the bias and temperature stress, resulting in the problems, known as negative and positive bias temperature instability (NTBI and PTBI). Even if the effect can partially be recovered or compensated externally during its standard operation, the large V_{Th} shift can still affect the proper functionality of the device [148, 149] and therefore should not be underestimated. Moreover, the input and feedback capacitances are also affected by trapped charges. To analyze this, the device is stressed with gate voltage along with precise temperature steps and the gate-charge characteristics, before and after stress, is used to estimate shifts in capacitances (CGD and CGS). This indicates the amount of the degradation of physical properties under different stress time and stress temperature conditions [149].

VII. CONCLUSIONS

We have presented a brief summary of the work done for the development of trench gate power MOSFETs. We have shown that starting from its evolution as the best power device in low to medium power applications; the trench gate power MOSFET has undergone several structural and technological changes, though its basic structure and operating concept remained unchanged. These modifications have made the present form of a trench MOSFET a reliable and better device. Since the ultimate goal of these improvements is to achieve the ideal specifications, the trench power MOSFET continues to evolve making it an even better device in future [150-153].

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