Materials Science in Semiconductor Processing 78 (2018) 22–31

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

# Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review

Maria Cabello*, Victor Soler, Gemma Rius, Josep Montserrat, José Rebollo, Philippe Godignon

*Centro Nacional de Microelectrónica (CNM-CSIC) Campus UAB, 08193 Cerdanyola, Barcelona, Spain*

ARTICLE INFO

*Keywords:*
Silicon carbide
SiC MOSFETs
Field effect mobility
Interface traps
Power devices

ABSTRACT

This paper reviews advanced gate dielectric processes for SiC MOSFETs. The poor quality of the $SiO_2$/SiC interface severely limits the value of the channel field-effect mobility, especially in 4H-SiC MOSFETs. Several strategies have been addressed to overcome this issue. Nitridation methods are effective in increasing the channel mobility and have been adopted by manufacturers for the first generations of commercial power devices. Gate oxide doping techniques have also been successfully implemented to further increase the channel mobility, although device stability is compromised. The use of high-k dielectrics is also analyzed, together with the impact of different crystal orientations on the channel mobility. Finally, the performance of SiC MOSFETs in harsh environments is also reviewed with special emphasis on high temperature operation.

## 1. Introduction

It is today widely recognized that new generations of power devices based on Wide Band Gap (WBG) semiconductor materials with superior material properties for power operation are required for a higher efficiency of power converters, as profusely covered in this special issue. Their critical field is more than one order of magnitude higher than Si, which allows using a thinner and higher conductive epitaxial layer. Consequently, the on-state current losses are drastically reduced. Within the WBG family, SiC is one of the most promising semiconductor materials for power devices fabrication, and indeed several commercial devices are already offered on high volume production.

Specifically, MOSFET device is a key element in modern microelectronics, with applications spanning from highly integrated CMOS to high power devices. As a device, it has really boosted the development of all kind of microelectronic technologies since the 1970's. In power electronics, a technology initially based on Si bipolar devices (BJTs and thyristors), MOSFETs and MOS gate-controlled devices (mainly IGBTs), completely monopolize today's market. Therefore, it seemed logical to endeavor a new generation of SiC power devices based on the development of MOSFET architecture. Indeed, since its demonstration in 1993 [1], SiC MOSFET has been the focus of numerous investigations.

However, the development of low resistance SiC power MOSFETs has been slower than other SiC power switches, like JFETs or BJTs, due to its very low inversion channel mobility values and threshold voltage ($V_{th}$) high instability. These limitations are mainly caused by a poor quality of the MOS interface, which is affected by large oxide charges and interface trap density ($D_{it}$) values. However, improvements in the MOS interface quality allowed the realization of commercial SiC MOSFETs operative up to 1.2 kV–1.7 kV, yet, SiC high voltage capability is not fully exploited. The current roadmap for SiC semiconductor industry tentatively predicts the introduction of 3.3 kV–6.5 kV SiC devices in the market in the medium term to compete with their Si-based counterparts.

This review compiles several technological solutions focused to improve the SiC MOS interface toward a main target, to increase the channel carrier mobility. Indeed, regarding mobility in the MOSFET channel, we have to consider two ranges of operation, one at relatively low electric field, just above the $V_{th}$ (typically 5 V), and a second regime at higher field, for MOS gate voltages of 15–25 V. The latter is especially relevant for power electronics converters as it corresponds to the gate operation voltage of the devices. There are several ways to extract the channel mobility, coming from Si technology: a) effective channel mobility ($\mu_{eff}$) is extracted from output curves ($dI_{DS}/dV_{DS}$), b) field effect mobility ($\mu_{fe}$) is extracted from transfer curves ($dI_{DS}/dV_{GS}$) and c) hall mobility ($\mu_{hall}$) is extracted under magnetic field using Hall laws. However, in SiC, the electrons generated in the inversion layer are trapped by the high density of interface traps and near interface oxide charges, and it strongly affects the extraction of an accurate mobility value [2]. Accordingly, the concept of apparent channel mobility would better reflect the mobility extracted from the measurements. In the literature, most of the reported mobility values for SiC MOSFET test structures are specifically field effect mobilities. Experimentally, the $\mu_{fe}$ versus gate voltage (or electric field) curve typically shows a peak

* Correspondence to: CNM-CSIC, C/ dels Tillers, Campus UAB, 08193 Cerdanyola del Valles, Barcelona, Spain.
*E-mail address:* maria.cabello@imb-cnm.csic.es (M. Cabello).

http://dx.doi.org/10.1016/j.mssp.2017.10.030
Received 1 August 2017; Received in revised form 18 October 2017; Accepted 20 October 2017
Available online 02 November 2017

**Table 1**
Properties of SiC polytypes as compared to Si.

| Material | $E_g$ (eV) @300k | $\mu_n$ ($cm^2/V\cdot s$) | $\mu_p$ ($cm^2/V\,s$) | $\mu_{fe}$* ($cm^2/V\,s$) | Ratio $\mu_n/\mu_{fe}$ | $E_c$ (MV/cm) | $\varepsilon_r$ |
|---|---|---|---|---|---|---|---|
| **Si** | 1.11 | 1350 | 450 | 500 | 2.7 | 0.3 | 11.8 |
| **3C-SiC** | 2.3 | 750 | 40 | 150 | 5 | 1.6 | 9.6 |
| **6H-SiC** | 3.05 | 415 | 90 | 45 | 9.2 | 2.6 | 9.7 |
| **4H-SiC** | 3.2 | 950 | 120 | 7 | 135 | 2.5 | 9.7 |
| **15R-SiC** | 2.98 | 600 | – | 60 | 10 | 2.5 | 9.7 |

* Average value for either dry or wet oxidation [5].

maximum just after the $V_{th}$ is reached. Then, $\mu_{fe}$ decreases upon increasing gate voltage (increasing vertical electric field), as it will be carefully discussed latter in this paper. Eventually, the $\mu_{fe}$ peak value can be much higher than the $\mu_{fe}$ values at high fields. When considering a possible technological solution for MOSFET improvement, this behaviour must be also taken into account. While in Si technology the $\mu_{eff}$ is usually a factor 2.5 lower than the bulk mobility, in SiC, this difference is larger and it depends on the crystallographic structure, i.e. SiC polytype (see Table 1).

It is understood that the decrease of the channel carrier mobility is mainly caused by structural imperfections of the dielectric layer as well as in the interface. All the root causes for traps formation are not known today, but interstitial carbon clusters, Si and C vacancies in the SiC surface, oxygen vacancies in the oxide, and most probably a high strain of interface atomic layers are responsible for the creation of electrically active traps. The presence of electrically active charges in the oxide bulk or at the interface strongly influences the flow of the charge carriers in the conduction channel. The different types of charges [3] and their arrangement are schematically represented in Fig. 1. A modelling of channel mobility as a function of the applied gate voltage is reported in [4] for several types of physical scattering effects. Their relevant results include that $D_{it}$ and fixed charges ($Q_{ox}$) strongly impact the $\mu_{fe}$ peak value at low fields, while surface roughness and Near Interface Oxide Traps (NIOTs) are the main parameters affecting $\mu_{fe}$ at high fields. However, if the interface traps are reduced, below $4 \times 10^{11}$ $cm^{-2}eV^{-1}$, the phonon scattering is a $\mu_{fe}$ major limiting effect at low fields. The mobile charges and NIOTs are mainly responsible for the $V_{th}$ instability.

This review is structured as follows. We will first recap some results obtained on the different SiC polytypes. Then, the rest of the paper will be focused on 4H-SiC. We will review the various solutions proposed to increase the poor mobility obtained by standard oxidation (wet/dry) of Si face < 0001 > 4H-SiC. Particularly, we will start presenting nitridation treatments, as well as phosphorus, boron and alkaline earth element doping. Other crystallographic orientation of 4H-SiC will then be considered. Finally, we will apply our knowledge on SiC MOS interfaces to discuss device operation in harsh environment, such as performance at high temperature and radiation hardness.

The review is focused on the n-channel mobility improvement. It is important, when comparing results in different papers of the literature to take into account that reported mobility and $D_{it}$ values strongly depend on method and on the test structure used for parameter extraction. Extracted $\mu_{fe}$ decreases when the channel length decreases, when the p-type doping is done by implantation instead of epilayer, and when the surface doping is increased.

## 2. MOS interface for different SiC polytypes

Among the more than 200 possibilities of SiC crystallographic structures, the so-called polytypes, the most commonly used for device fabrication have traditionally been the 3 C (cubic), 6 H and 4 H (hexagonal) polytypes. Table 1 summarizes main fundamental properties of each polytype, together with Si characteristics for reference. Yet, in most present applications, devices are produced on 4H-SiC polytype, due to its superior and more isotropic bulk carrier mobility. Although most of the results reviewed in this paper concern 4H-SiC, it is also interesting to collect the insights on 3C-SiC and 6H-SiC MOSFETs properties reported in literature.

**3C-SiC**. If compared to 4H-SiC and 6H-SiC based MOSFETs, the few examples of 3C-SiC MOSFETs reported in the literature systematically exhibit higher $\mu_{fe}$ values. This behaviour is corroborated by lower $D_{it}$ ($7 \times 10^{10}$ $cm^{-2}eV^{-1}$at 0.2 eV from electric field ($E_C$)) and active NIOTs values obtained from their experimental measurements. The fact is that as the 3C-SiC bandgap is smaller than the hexagonal polytypes, the NIOTs that trap electrons from the channel, causing the $\mu_{fe}$ degradation, are located within the conduction band, but they do not affect electrons trapping [6].

Different from the rest of SiC polytypes, the lower active $D_{it}$ values obtained in 3C-SiC have allowed the integration of MOSFETs with $\mu_{fe}$ values between 75 and 260 $cm^2/Vs$ using a standard dry oxide gate process [7], i.e. without extra nitridation or specific Post Oxidation Annealing (POA) treatment. Accordingly, from the point of view of channel efficiency, 3C-SiC would be the ideal polytype for the fabrication of SiC-based power MOSFET. However, the 3C-SiC polytype has important limitations. Drawbacks include its lower critical field strength or lower thermal conductivity, which limit its application to MOSFET high voltage applications. Moreover, the main issue concerning the use of 3C-SiC is the starting material fabrication and quality. Since 3C–SiC polytype is a metastable crystal phase, it cannot be grown in large wafer size by the sublimation method. Despite original growth methods have been proposed by Hoya, like Chemical Vapor Deposition (CVD) on Si [6,7] or Switch Back Epitaxy (SBE) method, a large density of defects and especially Si-terminated stacking faults (SF) are still present in the available material, which limits 3C-SiC

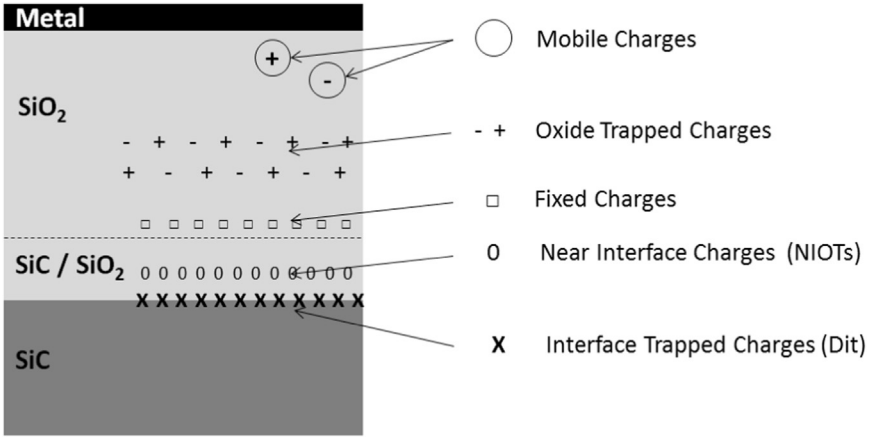


**Fig. 1.** Schematic representation of the charges present in the SiC MOS interface.

use for real commercial devices.

**6H-SiC.** Similar to 3C-SiC, the quality of the $SiO_2$/6H-SiC interface, and consequently $\mu_{fe}$ values, is inherently higher than that of the 4H-SiC polytype due to its smaller bandgap. 6H-SiC MOSFET's with $\mu_{fe}$ values up to 72 $cm^2$/Vs have been reported when standard dry oxidation treatment is combined with low temperature wet re-oxidation annealing, without the need for nitridation or incorporation of other element atoms [8]. In addition, nitridation was also proven effective in improving the interface quality of 6H-SiC MOSFET [9]. However, despite high quality 6H-SiC crystal can actually be obtained, unlike 3C-SiC, its low bulk mobility along the c-axis, due to its large crystal anisotropy, makes this polytype unattractive for power devices fabrication [10].

**15R-SiC**. This polytype behaves similarly to 6H-SiC polytype, but with slightly higher $\mu_{fe}$ values due to its higher bulk mobility. However, 15R-SiC material is very difficult to synthetize, so growth process results always contain large amount of other polytypes inclusions.

## 3. Effect of nitridation on mobility

As mentioned in the introduction, the $D_{it}$ and NIOTs large values and at the $SiO_2$/SiC interface limits $\mu_{fe}$ in 4H-SiC MOSFETs processed with dry or wet oxidation [11,12]. Hence, strategies for reducing $D_{it}$ and NIOTs values are needed for developing high performance SiC MOSFETs. One of the approaches involves the application of a nitridation process which consists in complete or partial growth of the gate oxide in the presence of N-containing gas. N promotes the generation of strong Si-N bonds that act as a passivation of the interface traps. Interface traps are linked to dangling and strained bonds, as well as from missing atomic C or other complex Si-CO compounds from the oxide and $SiO_2$/SiC interface [11]. Effectively, the introduction of N at the $SiO_2$/SiC interface reduces $D_{it}$ and increases $\mu_{fe}$.

First studies reported on nitridation showed the positive effect of NO annealing at $SiO_2$/6H-SiC interface [9]. Additional results of NO annealing in $SiO_2$/4H-SiC [12,13] found that N is incorporated only at the interface, therefore being very efficient in reducing $D_{it}$ by a factor of 10. Based on this NO annealing, $\mu_{fe}$ could be increased up to 25–35 $cm^2$/Vs. To implement the nitridation process, the oxide can be directly grown in NO ambient at 1150–1175 °C, or a dry thermal oxide can be submitted to a NO POA. The effect of $N_2O$ annealing on the $SiO_2$/4H-SiC interface was investigated later [14], obtaining $\mu_{fe}$ values of up to 26 $cm^2$/Vs. At high temperature, $N_2O$ decomposes into a small percentage of NO and a large percentage of $N_2$ and $O_2$. These become undesired byproducts as they lead to competing reactions which hinder the N incorporation process into the $SiO_2$/4H-SiC interface. In consequence, NO treatment is more efficient than $N_2O$ treatment. On the other hand, drawback of NO is its high toxicity.

Recent studies on POA in $N_2$ gas at high temperatures (> 1350 ºC) [15] has shown effectiveness in passivating dominant slow traps at the interface on thin $SiO_2$ layers (< 15 nm) in 4H-SiC MOS devices. Other alternative nitridation methods have also been tested, such as ammonia ($NH_3$) nitridation [16,17] or the N-plasma nitridation [18–20]. Despite little improvement on $SiO_2$/4H-SiC interfaces is reported by $NH_3$ annealing, the leakage current increases due to a reduction of the dielectric strength. On the other hand, even though N-plasma nitridation results in substantially greater N coverage at the $SiO_2$/4H-SiC interface, $\mu_{fe}$ is not further increased. This fact suggests that plasma method is effective in reducing $D_{it}$, but NIOTs, which also play a dominant role in limiting $\mu_{fe}$ [11,12], are not decreased as much as with the standard NO annealing. Summarizing, mentioned nitridation methods have allowed a $\mu_{fe}$ increase in SiC MOSFETs, keeping a good $V_{th}$ stability level [21]. The evolution of transfer curves $I_{DS} = f(V_{GS})$ during bias stress instability (BSI) test are shown in Fig. 2(a)[22], for samples with different surface preparation before the $N_2O$ gate oxidation; Fig. 2(a) shows the evolution of the transfer curve of n-MOSFETs pre-treated by $O_2$ plasma, while Fig. 2(b) shows the results obtained when doing a pre-annealing under $H_2$ at 800 °C.

Concerning the oxide reliability, Time-Dependent Dielectric Breakdown (TDDB) measurements have been done in SiC MOS capacitors. For instance, promising results were obtained on 6H-SiC [23,24]. Failure meantime at 3 MV/cm is 100 years at 240 °C and 10 years at 305 °C on wet oxide [23], while it is about 5.6 h at 350 °C on dry oxide [24]. However, several studies performed on nitrided 4H-SiC MOSFETs [25,26] have also shown the improvement of high temperature gate oxide reliability (e.g. 100 years operating at a gate oxide electric field of 4 MV/cm at 250 °C). Actually, recently obtained oxide lifetimes are comparable to those reported on Si devices [27].

Nitridation process is commonly used in the production of commercial power MOSFETs. In spite of the $\mu_{fe}$ increase obtained by nitridation, the mobility values are still rather low (less than 5% of the bulk mobility) and it is thought that the limit of the improvements provided by nitridation has been reached. Consequently, alternative strategies for a further $\mu_{fe}$ enhancement have been addressed as reviewed in the next paragraphs.

## 4. Doped gate oxides

As an alternative to nitridation, several approaches consisting in doping the gate oxide by the introduction of different ions have been considered for effectively passivating the $SiO_2$/SiC interface and increasing $\mu_{fe}$. Firstly, accidental addition of Na actually resulted in $\mu_{fe}$ peak high values of about 170 $cm^2$/Vs [28], although resulting devices were highly unstable due to mobile ions effects. However, other chemical elements such as P or B, which have been used more recently, have shown better results as follows.

### 4.1. Phosphorus

P incorporation via the annealing of thermal $SiO_2$ in $POCl_3$ ambient, as compared to NO annealing, has allowed obtaining high $\mu_{fe}$ values (89 $cm^2$/Vs) and lowering $D_{it}$ on Si-face 4H-SiC [29]. Similar results were obtained by Phosphosilicate Glass (PSG) annealing from solid diffusion sources [30]. Besides, P incorporation by ion implantation in the SiC prior to an oxidation step has also proven effective in reducing $D_{it}$ [31,32]. However, the introduction of atomic P converts $SiO_2$ into a PSG layer, which can lead to $V_{th}$ instability. Explicitly, $V_{th}$ instability was analyzed and compared to that of nitride-gate dielectrics [33]. The results show that the oxide traps in phosphorus-doped oxides are the main cause of $V_{th}$ instability via the capture of electrons. The $V_{th}$ stability has been improved by using a stacked gate oxide structure consisting of a thin PSG interfacial layer and a CVD oxide deposited on top [34,35], importantly, while maintaining $\mu_{fe}$ high values.

In addition, recent studies [36] have proved that the P inclusion into the gate oxide layer also accounts for SiC surface doping, which also has an effect in the $\mu_{fe}$ value. Known as counter doping, this effect is linked to the group V elements, i.e. they act as donors when they accumulate at the $SiO_2$/SiC interface substituting Si or C atoms. As a result, the inversion channel of the MOS structure is displaced deeper inside the SiC crystal, therefore, reducing interface effects such as Coulomb scattering. In consequence, counter-doping increases $\mu_{fe}$ especially at low gate voltages, i.e. near the threshold voltage, where the Coulomb scattering and $D_{it}$ are the mobility main limiting factors.

Differently, at high transverse electric fields, surface roughness scattering is the main limiting factor, and counter-doping has a lower effect on improving $\mu_{fe}$. As seen in Fig. 3, typical channel mobility versus gate voltage curve exhibits a strong peak maximum followed by a marked decrease of the mobility. Counter-doping via N ion implantation was firstly discussed by Ueno et al. [37]. They showed an increase of the $\mu_{fe}$ peak and a $V_{th}$ decrease as compared to the values of a standard oxide. More recent achievements of counter-doping have also been reported for phosphorus [38], as well as using other group V elements such as antimony [39,40] and arsenic [40]. Quantitatively,

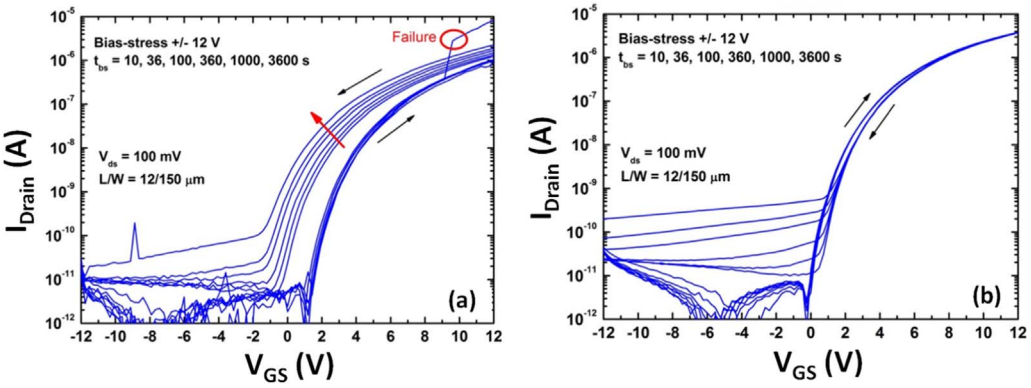


**Fig. 2.** Evolution of the transfer curve for (a) $O_2$ plasma pre-treatment and (b) $H_2$ at 800 °C pre-treatment on $N_2O$ grown oxide during stability BSI test. $V_g$ sweeps from − 12 V to + 12 V, and reverse, are applied for increasing step-time durations, up to 1 h [22].

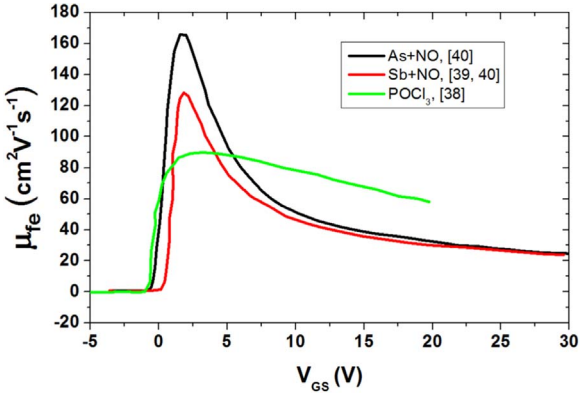


**Fig. 3.** Field effect mobility versus gate voltage curves obtained on MOSFETs. Their oxides have been treated with different group V element doping profiles.

reported $\mu_{fe}$ peak values are 89 $cm^2$/Vs, 100–120 $cm^2$/Vs, and 160 $cm^2$/Vs, respectively. Their mobility curves are shown in Fig. 3. As clearly observed, both Sb and As exhibit very pronounced $\mu_{fe}$ peaks at low electric fields, which maxima are significantly higher than in the P case. Yet, mobilities at high electric fields (e.g. > 10 V) are significantly lower for Sb and As and, consequently, As or Sb counter-doping seems to be of limited effectiveness in real-device applications.

### 4.2. Boron

In 4H-SiC MOSFETs, B diffusion in a previously grown dry thermal oxide has allowed a reduction of their $D_{it}$ so that high $\mu_{fe}$ peak values (100 $cm^2$/Vs) could be obtained [41]. The mobility improvement is attributed to a structural change of $SiO_2$/SiC interface. As reported in previous works on $POCl_3$ [36], the stress at the interface can be reduced by the incorporation of network formers. Specifically, it is believed that B atoms occupy Si sites, instead of C sites, in accordance with Si lower electronegativity [42]. As a result, the oxygen bond strength is reduced, which promotes stress relaxation in the oxide [43]. B incorporation by diffusion has also proven effective in reducing NIOTs, and therefore, accounted for the $\mu_{fe}$ increase. These results are in agreement with some earlier studies on the $SiO_2$/Si interface by Fourier transform infrared absorption and X-ray photoelectron spectroscopy that showed how B incorporation relaxes the built-in compressive stress in the oxide network near the interface [44]. On the other hand, boron is smaller than other group V atoms, and it does not always counter dope the SiC surface.

Actually B doping process has been improved more recently, particularly, as a combination of $N_2O$ oxynitridation plus B diffusion [45,46]. Further $\mu_{fe}$ increase even at high electric fields is reported. Given that C clusters and NIOTs constitute the dominant fraction of interface traps [47], the combination of B diffusion with oxynitridation can contribute also to improve the $SiO_2$/4H-SiC interface quality. Precisely, an oxide stacked structure has been prepared by a sequential processing which consists in: a) rapid thermal oxidation (RTO) in $N_2O$ environment to grow a thin $SiO_2$ which limits the C interstitials, b) B diffusion into the $SiO_2$ from BN solid source, and c) deposition of a Plasma Enhanced CVD tetraethyl orthosilicate (PECVD TEOS) oxide on top. With this approach, average $\mu_{fe}$ peak values of 160 $cm^2$/Vs at low electric fields (7.5 V) have been reached, with a relatively low attenuation up to a gate voltage of 30 V (120 $cm^2$/Vs). Indeed, the study also shows that the higher the B concentration, the higher the $\mu_{fe}$, with peak values above 200 $cm^2$/Vs. Alternatively, other groups have been able to reach high values of $\mu_{fe}$ peak (> 160 $cm^2$/Vs) at low electric field by combining a B treatment with superficial Sb doping [48,49]. In Fig. 4, we compare the B, B + $N_2O$ and Sb + B $\mu_{fe}$ curves, showing a maximum of the mobility at low electric field and the mobility decrease at high fields. Importantly, $V_{th}$ of B-doped oxide remains positive and the maximum oxide critical field is not reduced.

When analyzing the oxide layer with SIMS and X-ray diffraction, we detect the presence of BN. Accordingly the nitrogen help fixing the boron atoms. Interestingly, MOSFETs fabricated with $NO_2$ + B gate dielectric have shown a reasonable $V_{th}$ stability at room temperature (Fig. 5). However, $V_{th}$ stability is not maintained when temperature is increased. Experimental data in Fig. 5 correspond to stress testing on 4.5 kV power MOSFETs in a BSI test, for up to 1 h duration at both; room temperature and 150 °C. Our results indicate that boron doped gate oxide is unsuitable for high temperature operation. A possible explanation is boron activation for instance as a mobile ion above certain temperatures. Structurally, germanium, similar to boron, could also be a potential element to relax interface stress, so that MOS device performances could be improved [50].

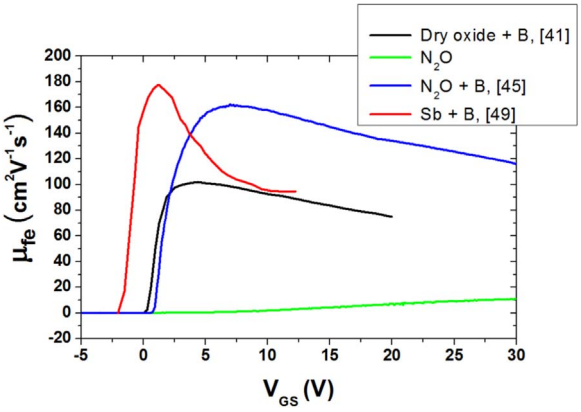


**Fig. 4.** $\mu f_e$ versus gate voltage curves for MOSFET devices having different configurations of B-doped oxides. Results on bare $N_2O$ thermal oxide are included for reference.

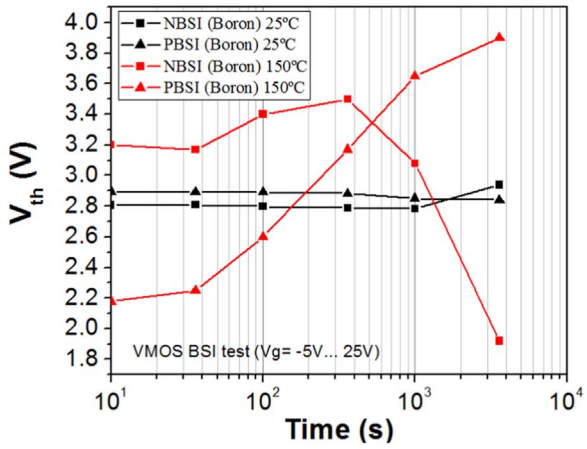


**Fig. 5.** $V_{th}$ drift of in boron-treated 4.5 kV power MOSFETs. BSI stress tests are performed at room temperature and 150 °C.

### 4.3. Alkali and alkaline earth elements

The use of alkali and alkaline earth elements for passivating the $SiO_2$/4H-SiC interface has also been investigated. The passivation process mainly consists of a very thin interface layer of alkali or alkaline earth materials deposition, followed by a CVD $SiO_2$ layer and a subsequent high temperature POA. Experimentally, thin layers of Rb and Cs increase $\mu_{fe}$ values only up to 25 $cm^2$/Vs (see Fig. 6). Contrarily, alkaline earth elements such as Sr and Ba provided $SiO_2$/SiC interface conditions suitable for obtaining high channel mobility MOSFETs on the Si-face (0001) of 4H-SiC without the need of employing the standard nitric oxide (NO) annealing. Precisely, it is understood that Sr and Ba atoms located at the interface provide $\mu_{fe}$ values as high as 65 and 110 $cm^2$/Vs, respectively (Fig. 6) [51]. It has been also shown that Ba allows obtaining stable $V_{th}$ under stress testing at 175 °C and 2 MV/cm gate bias. More recently, Ba interface passivation combined with post-deposition anneal of up to 10 h in an $O_2/N_2$ ambient has provided $\mu_{fe}$ values two times higher than that obtained by standard NO passivation annealing [52,53]. It is reported that Ba catalyzes an increase of the oxidation rate and its efficiency, including the formation of $BaSiO_X$.

## 5. High-k dielectrics

In addition to the poor quality of the SiC/$SiO_2$ interface, a drawback of $SiO_2$ for power MOSFETs is its low dielectric constant (k). As $SiO_2$ k is approximately 2.5 times lower than SiC k value, proportionally larger electric field is obtained in the dielectric medium as compared to the semiconductor layer. This is the reason why a new class of dielectric materials with k values equal or larger than the SiC one is sought.

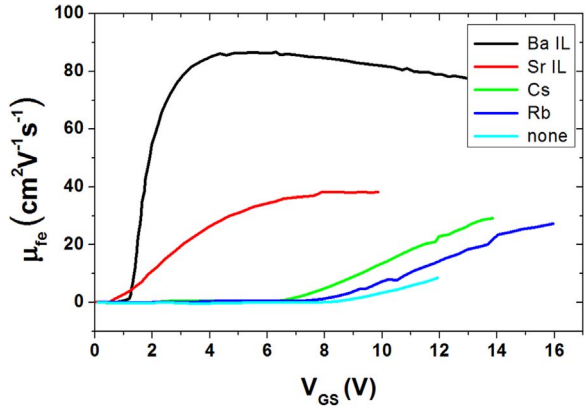


**Fig. 6.** $\mu f_e$ versus gate voltage curves for MOSFET devices.
Oxides have been treated with various alkaline earth elements (adapted from [51]).

High-k gate dielectric materials reduce significantly the electric field value for a given gate dielectric thickness, and hence the total gate current density is also reduced. Additionally, high-k gate dielectrics further reduce $V_{th}$ shifts with varying dielectric thicknesses, thus leading to a better processing margin and a more stable performance in operating devices. Several high-k gate dielectrics have been studied for both Si and SiC MOS technologies as they would provide a $D_{it}$ reduction. However, gate leakage increase is expected due to their reduced bandgap. Fig. 7a shows k vs bandgap energies for several relevant high-k oxides [54]. It can be seen that $Al_2O_3$, MgO and $ZrO_2$ exhibit larger bandgaps and $ZrO_2$ also offers a high k value.

Indeed, not only the bandgap value but also the band alignment with SiC bandgap must be taken into account to avoid excessive leakage currents through the interface. Examples of band alignment for $Al_2O_3$ and $HfO_2$ are shown in Fig. 7b. Then, a thin $SiO_2$ layer stacked between SiC and the high-k layer is a typical configuration for implementing high k gates. The use of a high-k layer instead of a thick $SiO_2$ allows reducing the thickness of the thermal oxide at the SiC interface for a given maximum electric field, as schematically illustrated in Fig. 8. Specifically, it impacts the $\mu_{fe}$ value as less C clusters and Si vacancies are created during oxidation. $SiO_2$ acts as an interface barrier [54,55] able to mitigate the gate leakage effect. In addition, the thin $SiO_2$ layer also acts as a barrier layer to avoid eventual chemical reactions in the high-k/SiC interface.

Many studies involving different dielectrics with high relative permittivity values have been reported, e.g. $Al_2O_3$ ($\varepsilon_r$ = 8–11) also interposing a thin $SiO_2$ layer ranging from 1 up to 6 nm thick [56–59], $HfO_2$ ($\varepsilon_r$ = 15–25) were the optimal reported $SiO_2$ layer thickness is about 6 nm [60–63], $Ta_2O_5$ ($\varepsilon_r$ = 10–20) [64,65] or $La_2O_3$ ($\varepsilon_r$ = 20–30) with which some works are also using a 6 nm layer of $SiO_2$ [66–68]. Additionally, our studies on $Ta_2Si$, [64,65] show reasonably high $\mu_{fe}$ values (~ 45 $cm^2$/Vs) which are totally modulated by the effect of the carrier Coulomb scattering on interface trapped charges. The processing key consisted in firstly $Ta_2Si$ deposition followed by a dry oxidation. As a result, Si atoms in $Ta_2Si$ become oxidized and SiC surface oxidation is reduced, which results in a lower amount of C clusters. A commonly used high-k dielectric in SiC MOSFETs is $Al_2O_3$, due to an excellent lattice matching with SiC crystal, together with a good thermal stability and large dielectric bandgap [56]. Indeed, high $\mu_{fe}$ peak values have been obtained with $Al_2O_3$ gate dielectric, 64 $cm^2$/Vs – 300 $cm^2$/Vs [57,58]. However, again, the reported mobility values correspond to the maximum peak mobility, whereas field effect mobility under high fields drastically decreases. Recently, studies on $La_2O_3$ [67,68] have achieved remarkable $\mu_{fe}$ values of 133 $cm^2$/Vs and relatively stable $V_{th}$. $La_2O_3$ is deposited at the interface, covered by a $SiO_2$ layer. A significant reduction in leakage current density has been also observed in high-k $La_2O_3$ based MOSFETs. Summarizing, high-k $La_2O_3$ looks promising.

The main drawback of most high-k dielectrics is their recrystallization at medium temperature values (400–700 °C) which reveals as an increase of leakage currents. In the power MOSFET fabrication process, the gate dielectric is typically deposited before the polysilicon deposition and ohmic contacts formation. Polysilicon electrode and ohmic contacts formation in SiC technologies involve thermal processes at temperatures higher than 900 °C. Consequently, the structure of the deposited high-k dielectric layer would be likely modified during post-processing.

## 6. Impact of crystal orientation

In Si technology, the MOS interface properties can significantly change depending on whether < 100 > or < 111 > crystal orientation is used. Similarly, SiC MOS properties depend on crystal orientation. For instance, as SiC is a polar material, oxide growth kinetics of the Si face differs from C face. As another example, for hexagonal SiC material

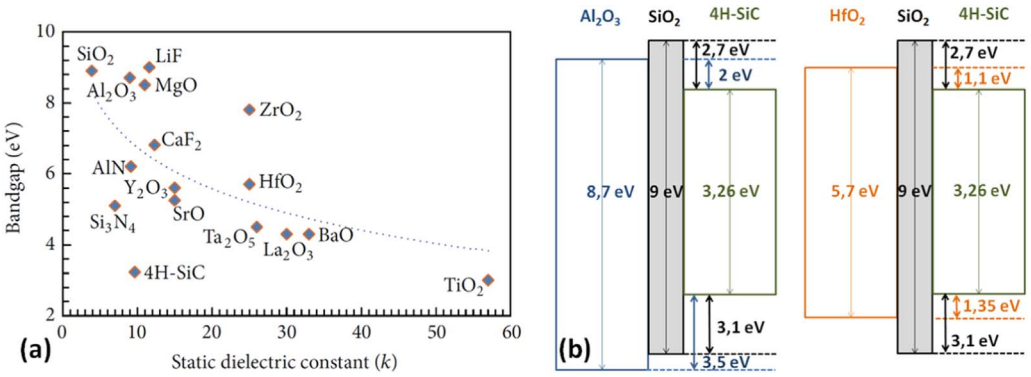


**Fig. 7.** (a) Bandgap energy as a function of dielectric constant for different dielectric and oxide materials [54], (b) Representation of energy band alignment for $Al_2O_3/SiO_2$/4H-SiC and $HfO_2/SiO_2$/4H-SiC heterostructures.

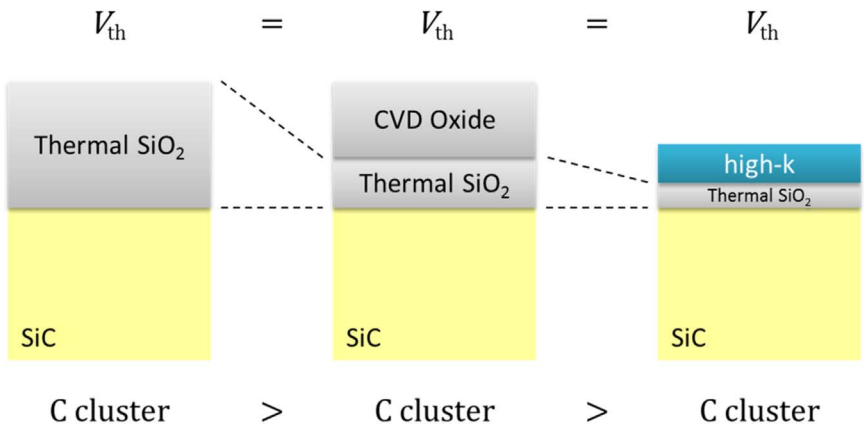


**Fig. 8.** Concept scheme for thermal oxide thickness reduction using high-k to reduce generation of C clusters at the MOS interface.

epilayers must be grown on off-axis substrates to limit the amount of defects as well as 3 C or 15 R inclusions. Today, most of the processed SiC material corresponds to 4° off-axis cut Si face 4H-SiC wafers. This type of SiC substrate is the best quality substrate for high voltage device fabrication. Differently, it is the worst substrate in terms of MOS performances.

The strong impact of crystal orientation on MOS properties was firstly observed on the < 11–20 > crystal orientation, also known as α-face. As early as 2000, Yano *et al.* [5] reported $\mu_{fe}$ peak values of nearly 100 $cm^2/Vs$ on < 11–20 > 4H-SiC MOS based on wet oxidation at 1100 °C plus Ar annealing at the same temperature. Instead, mobility values as low as 6 $cm^2/Vs$ with the same MOS processing on < 0001 > 4H-SiC are obtained. It must be mentioned that the thermal oxide growth rate is faster on the < 11–20 > face by a factor of 3–5. Other technical aspects include using wet oxidation instead of dry oxidation in the case of < 11–20 > orientation, while dry oxidation is preferred on the < 0001 > face. Importantly, the $\mu_{fe}$ values on < 11–20 > 4H-SiC are reproducible and have even been improved later on [69,70]. For instance, in [70] we reported 160 $cm^2/Vs$ average channel mobility in 4H-SiC MOSFETs, which were fabricated on < 11–20 > p-type epitaxial layers using a two-step procedure for gate oxide formation. The first step consists in the thermal growth of a thin dry $SiO_2$ at 1050 °C. The second step aims at a thick (50 nm) layer of complementary oxide deposited by PECVD using TEOS as precursor gas.

More recently, alternative crystal orientations, such as the < 0–33-8 > or < 03–38 > , have also been studied [71]. These orientations form an angle of 54.7° with respect to the < 0001 > Si face. This orientation is equivalent to the Si < 001 > face in cubic structure (3C-SiC). Similarly to < 11–20 > , higher $\mu_{fe}$ peak values can be obtained as compared to Si face [72,73]. In this case, the gate oxide was initially thermally grown in dry ambient, followed by post-annealing in first NO and then in Ar. Using this MOS configuration, $\mu_{fe}$ peak values of 80 $cm^2/Vs$ and low subthreshold slope of 110 mV/decade have been obtained. For comparison, 15–25 $cm^2/Vs$ and 200–400 mV/decade are typically obtained on < 0001 > face with the same oxidation applied on the implanted surface. Moreover, similar to Si MOS technology the channel mobility decreases as temperature increases. These results can be obtained thanks to the low $D_{it}$ value at the interface ($3 \times 10^{11}$ $cm^{-2}eV^{-1}$ near $E_c$).

Currently, there is no debate about the strong advantage of building the MOS channel on a non-polar SiC face. Specifically, it allows using a natural thermal oxide at the interface, without the need for incorporating foreign impurities. As a result, a more stable and reliable MOS structure should be achieved. The best way to implement the MOS channel on such crystal orientation is to build trench devices, and to avoid drawbacks such as lower breakdown capability. For instance, the following solution was proposed by Infineon on their new CoolSiC MOSFET [74]. The MOS channel is implemented on the side wall of a trench oriented 4° with respect to the surface, so that the < 11–20 > orientation is reached only on one side of the trench (Fig. 9a). As another example, Sumitomo implement a V-groove MOSFET, i.e. a trench etched with a sidewall angle corresponding to the < 0–33-8 > orientation [75] (Fig. 9b). The main drawback of both trench and V-groove transistor structures is the presence of a high electric field at the trench bottom in the blocking mode, which limits the breakdown voltage capability. While trench devices for operational voltages up to 1.7 kV are realistic, higher voltage class MOSFETs based on trench structures are complex to be implemented [74]. Fortunately, when the power MOSFET breakdown voltage capability increases (thicker epilayer), the weight of the channel resistance on the total device resistance is reduced. Accordingly, for a breakdown range higher than 3.3 kV, a planar structure can be used, even if any improvement of the < 0001 > mobility would always be welcome.

If we now consider the SiC polarity, we first observe that the growth kinetics of the thermal oxide is one order of magnitude faster on the C face than in the Si face. In the case of SiC MOSFETs fabricated by conventional dry gate oxidation of the C face, the $\mu_{fe}$ peak value is relatively low. However, it has been found [76] that pyrogenic gate

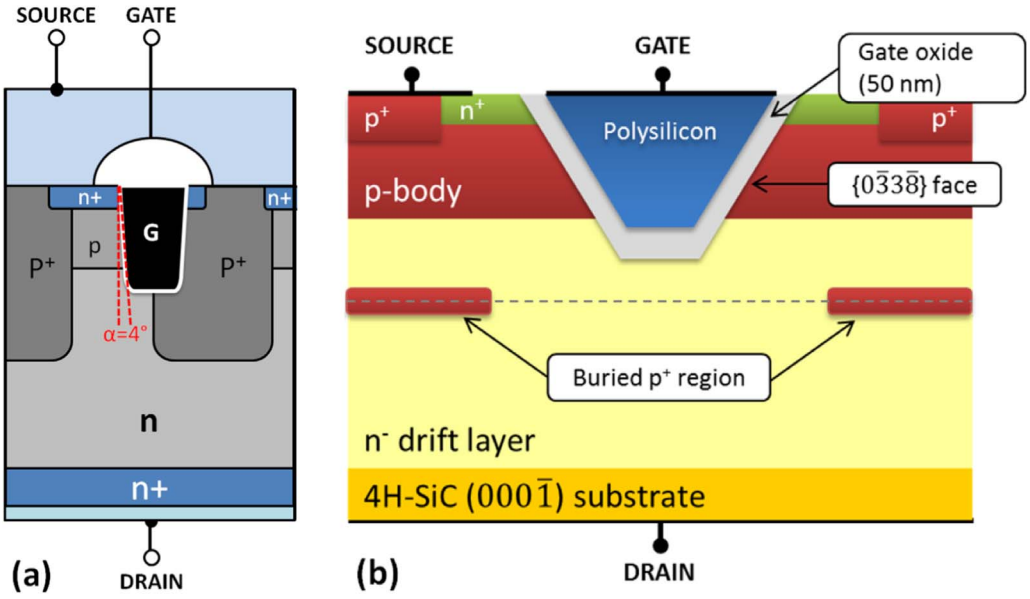


**Fig. 9.** Sketch of novel trench/groove MOSFET (a) the CoolSiC™ Trench MOSFET cell [70] and (b) the V-groove MOSFET from Sumitomo [75].

oxidation, as well as pyrogenic gate oxidation followed by $H_2$ POA, considerably decreased $D_{it}$. As a result, an increase $\mu_{fe}$ up to 111 $cm^2/Vs$ is obtained, which is much higher than the values obtained on similar MOSFETs fabricated on the Si face. These results have been confirmed by Okamoto's group who used wet oxidation and $H_2$ POA and reached $\mu_{fe}$ values of 90 $cm^2/Vs$ [77]. Remarkably, those values correspond to peak mobilities at low electric fields, just above the $V_{th}$. Similarly to counter doped MOSFETs, the mobility on C face strongly decreases at high electric fields. It is considered that the $D_{it}$ reduction might be caused by the passivation of interface states by –H or –OH. However, it is known from Si technology that H dangling bonds passivation is not stable and actually can be removed applying temperatures above 200 °C. It is also important to mention that wet or $H_2$ treatments do not work efficiently upon the Si face. Inversely, NO annealing cannot be applied on C face. As a final remark, the leakage through the oxide under high electric fields (attributed to Fowler-Nordheim tunneling) usually starts at lower electric fields in the C face due to earlier band alignment [78].

Another remark regarding crystal orientation was to check the impact of the characteristic off-cut angle of commercial wafers. As mentioned earlier, off-axis cut substrates are required to minimize the amount of 3 C inclusions [79,80]. Originally, in the 90's, 8° off-axis cut wafers were used to get maximum epilayer quality, but more recently, 4° off-axis cut substrates became the standard for SiC devices fabrication thanks to improvements of the growth processes. The impact of the off-axis nature of the interface on MOSFET performances was not extensively studied in the past, due to the lack of on-axis epitaxied material. However, our experiments, as well as other literature papers, indicated that the lower the off-axis angle, the better the MOS' channel properties. For example, Fukuda et al. [76] concluded that an off-axis epitaxial angle below 1° could highly contribute to reduce $D_{it}$ on C face SiC, since it eases the reduction of surface roughness. In [81] we demonstrated the advantages and disadvantages based on studying on-axis MOSFETs. When comparing on-axis with 8° off-axis implanted wafers, we observed a 50% $\mu_{fe}$ peak value increase for $N_2O$ MOSFETs. We again attributed this performance increase to an improved surface roughness in on-axis substrates. In addition, better $V_{th}$ stability, as compared to the other orientations, has been observed at both room and high temperatures on on-axis samples. The physical and electrical properties of $SiO_2$/4H-SiC interfaces on 2° off-axis epilayers were also reported by Vivona *et al.* [82]. Specifically, they reported improvements in surface flatness, $D_{it}$ and oxide reliability. Their MOS capacitors exhibit reasonable low $D_{it}$ values, in the order of $1 \times 10^{12}\ eV^{-1}cm^{-2}$, close to $E_c$, and of the oxide breakdown electric field (9.5 MV/cm). Importantly, the reduction of the off-cut angle implies a decrease of the wafer cost while not degrading the MOSFET electrical properties.

## 7. High temperature oxidation

Increasing the temperature of the SiC oxidation process is potentially beneficial for several aspects. Firstly, the oxidation rate would increase [83], what allows reducing oxidation time for a given thickness. More interestingly, Kurimoto *et al.* [84] reported that thermal oxidation temperature and rate can be used to tune $D_{it}$ of the SiC MOS interface. In particular, increasing the oxidation rate promotes C desorption during oxide growth. Therefore, C clusters present at the interface, which are partially responsible of trapping effects, are reduced. More recently, the presence of O vacancies in thermal oxides produced at standard processing temperatures has been also measured. It has been shown that promoting O diffusion by increasing oxidation-process temperature would reduce O vacancies. For example, Naik *et al.* [85] reported a significant $D_{it}$ decrease by performing wet oxidation at 1400 °C. In this case negative charges are reduced, while typically positive charges are affected in nitrous oxides. However, these MOSFET devices based on the 1400 °C oxidation process showed very low $\mu_{fe}$ values (2 $cm^2/Vs$). Yet, in another study, Thomas *et al.* [86] obtained $\mu_{fe}$ values of 40 $cm^2/Vs$ using a dry oxidation temperature of 1500 °C. They suggest reducing O content down to 7% to optimize the oxidation process. In this case, they obtained normally-on devices with a significant negative $V_{th}$. Actually, a common feature of all oxide treatments methods improving $\mu_{fe}$ is that a $V_{th}$ reduction is systematically observed. More recently, in [87] the authors compared dry oxides grown from 1150 °C up to 1600 °C. They observe minimum $D_{it}$ for an optimal oxidation temperature of 1450 °C. However, no large differences in $D_{it}$ values are found for the whole range of tested temperatures.

In summary, improvement of dry/wet oxide interface quality by increasing growth temperature is still not clearly understood. This means that others factors such as temperature ramp-down or the presence of ozone during the oxidation process are important aspects. Concerning ozone, a recent publication [87] demonstrates that its use during growth increases the growth rate. However, no electrical results are provided in this study.

## 8. SiC MOSFET for harsh environment

Two of the typically claimed advantages of SiC versus Si are its

capability for high temperature operation and its superior radiation hardness. These statements are undeniable when based on SiC crystal intrinsic properties, i.e. when considering SiC as a standalone bulk semiconductor, but it is not as simple when in view of operative SiC MOSFETs.

Considering its band gap and its intrinsic doping concentration, 4H-SiC is supposed to be able to operate at temperatures even higher than 750 °C. For reference, Si operation is limited to 250 °C, or even lower for the low doped epilayers used in power devices. Practically, high temperature operation in SiC diodes, JFETs and bipolar transistors has been demonstrated at up to 500 °C. At such high temperatures, the main limitations actually come from degradation of deposited metals and reliability of the interconnections. However, in SiC MOSFETs, a strong degradation is usually observed at the gate level at temperatures as low as just-above 200 °C. Explained in detail, it is observed that gate oxide starts to electrically leak and physically degrade, which causes devices failure after few minutes of operation. Despite some companies claimed for a CMOS technology operating at 300 °C, no long term stress or reliability data have been reported so far. Therefore, claiming its robust operation only up to a 200 °C seems more realistic based on current technology-development.

As another aspect for discussion, in Si technology the $\mu_{fe}$ peak value systematically decreases when the operation temperature is increased. Contrarily, in our first generation of SiC MOSFETs, device mobility increased up to a maximum value obtained for a given temperature which was typically around 200 °C, depending on the oxide type. This behaviour can be understood as due to the high density of charges and traps at the interface, which are able to capture electrons flowing through the channel. Instead, on newly-improved MOSFETs where $D_{it}$ values are lower than $4{\cdot}10^{11}$ $cm^{-2}eV^{-1}$, $\mu_{fe}$ presents a Si-like behaviour with increasing temperature. Specifically, this feature is observed when nitrous oxides are used, and also in P- or B-treated oxides. In [88], we evaluated the $V_{th}$ stability of nitrous oxide ($N_2O$ RTA grown) up to 450 °C. A very stable behaviour of these oxides up to 300 °C was demonstrated. Peculiarly, the $V_{th}$ stability is higher at 300 °C than at 200 °C, which is attributed to electron-hole capture balance at the higher temperature. Differently, $V_{th}$ stability of P or B doped oxides starts to degrade at temperatures > 150 °C, as mentioned previously.

Regarding power MOSFET technology, the device operation at higher temperature is dictated by an interest to reduce the cooling systems requirements for power applications. However, when temperature is increased, the current capability of the power MOSFET strongly decreases. As an example, in Fig. 10 we present the output characteristics of two 4.5 kV power MOSFETs, one providing high $\mu_{fe}$ value (B treatment, in Fig. 10(b)) and another with a lower one (dry oxidation, in Fig. 10(a)) [89]. There is a large difference in output current ($I_{DS}$) at 25 °C between the two transistors. However, at 300 °C the I-V curves are almost equivalent. It is therefore understood that $\mu_{fe}$ value has little influence on the static performance of the transistors at 300 °C. Indeed, at 300 °C the lower-mobility dry oxide seems more stable than the B-doped oxide. Therefore, the belief that room temperature $\mu_{fe}$ should be improved in devices designed for high temperature operation may not actually be a strict requisite.

Concerning radiation hardness, similar evaluation for SiC MOSFET behaviour versus SiC bulk fundamental properties can be done. Due to the $SiO_2$ sensitivity to ionizing effects, MOSFETs are the most accurate devices in radiation-rich environments. Detrimentally, electrical performances of Si MOSFETs in radiation-rich environments are typically degraded by the generation of positive oxide trapped charges and $D_{it}$ increase at the $Si/SiO_2$ interface. Their degradation is mainly caused by the increase of the electron-hole pairs generated in the gate dielectric layer, based on a charge build-up mechanism [90]. As gate oxides of SiC MOSFETs also consist in $SiO_2$, similar effects could be expected. However, observation upon both electron and proton irradiation in SiC MOSFETs reveal a special behaviour, which again is attributed to the presence of higher density of charges and traps [91,92]. In particular, we can somehow state that we have been able to improve the actual performances of certain MOSFETs after controlled irradiation. Our results indicate that under certain conditions, the irradiation could be used to stabilise $V_{th}$ drift, yet further studies are needed (Table 2).

## 9. Conclusions

Since the pioneering studies on SiC MOSFETs in the early 90 s, many technology developments and testing experiments have been performed to improve the initially poor results in $\mu_{fe}$. Since 2000, Si-face off-axis cut 4H-SiC turned to be the material of choice for fabricating power devices. Most efforts on material growth have been done toward this polytype, particularly, aiming at defect reduction and an increase of wafer size. However, in this review paper 4H-SiC Si face has been profusely demonstrated as the worst configuration to get MOSFET high $\mu_{fe}$ values.

A solution based on nitridation is today considered the standard in commercial MOSFET devices. However, nitridation mobilities are still low, reaching the limits of acceptable values. Moreover, with the availability of first pre-commercial power MOSFET devices, new issues such as $V_{th}$ instabilities appeared. New solutions such as Na or P doping have shown to be very efficient to increase $\mu_{fe}$. Yet, they strongly suffer from $V_{th}$ instability and reliability problems. Other alternative solutions, like oxide counter-doping with As and Sb or deposition of $Al_2O_3$ dielectric layer for 4H-SiC MOS, would have also provided very high low field $\mu_{fe}$ values, but actually show a strong $\mu_{fe}$ decrease at higher fields, in the operation range of the devices. The B incorporation in the oxide also allows a strong $\mu_{fe}$ increase, up to values of 200 $cm^2/Vs$. When combined with nitridation, devices show good stability at room temperature, but start to drift significantly above 100 °C. More efforts

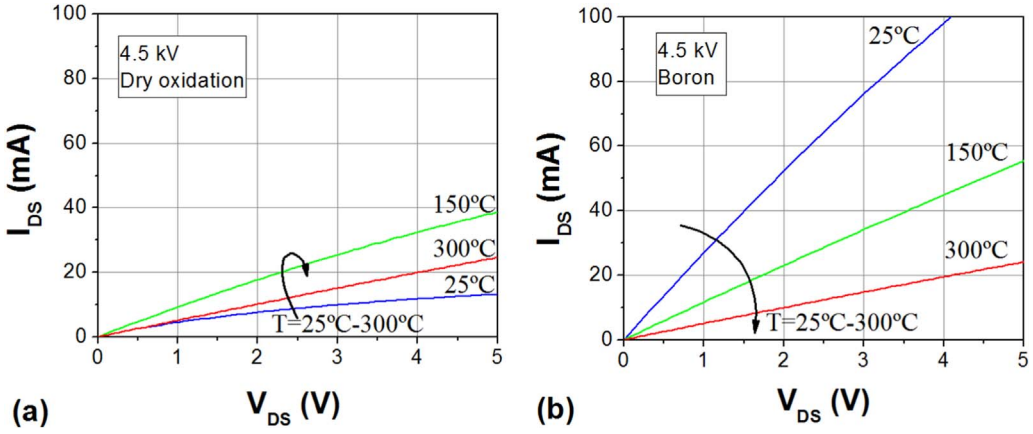


**Fig. 10.** Impact of temperature on the output characteristics of 0.8 $mm^2$ 4.5 kV power MOSFETs (a) without B treatment, and (b) with B treatment. $V_{GS}$ = 20 V.

**Table 2**
Summary of best oxidation process and corresponding parameters ranges, for different SiC crystal polytypes and orientations. $D_{it}$ is determined by the high-low method.

| Substrate material | Optimal oxidation type | $D_{it}$ at Ec-E ($cm^{-2}eV^{-1}$) | Subthreshold slope (mV/decades) | Peak channel mobility range ($cm^2/Vs$) |
|---|---|---|---|---|
| Silicon | Wet oxide | 2e10@0.1 eV | 65 | 450–550 |
| 4H off axis | Dry oxide | 2e12 @0.2 eV<br>1e13@0.1 eV | 200–400 | 2–7 |
| 4H off axis | Dry oxide, 1500 °C 7% $O_2$ | 2e12@0.13 eV | – | 40 |
| NO | Dry oxide, 1175 °C | 5e11@0.2 eV | 160 | 35 |
| $N_2O$ | Post oxidation or oxidation, > 1200 °C | 8e11@0.2 eV | 180 | 25 |
| Phosphorus | Dry oxide | 2e11@0.2 eV | – | 90–110 |
| Boron | $N_2O$ oxide | 2e11@0.2 eV | 140 | 100–180 |
| Barium | NO oxidation + 10 h 20% $O_2$ POA | 2e11@0.2 eV | – | 80 |
| 11–20 | Wet oxide or wet + $H_2$ POA | 1.5e11@0.2 eV<br>2e12@0.1 eV | 85 | 100–160 |
| 0–338 | Wet oxide | 3e11@0.2 eV<br>1e12@0.1 eV | 110 | 80 |
| C-face | Wet or dry oxide + $H_2$ POA | 5e11 @0.2 eV | – | 90–110 |

are needed to solve this problem, so that B doping can be validated as a future solution for SiC MOSFETs. A general tendency on 4H-SiC Si-face seems to be that a $\mu_{fe}$ increase is counter-balanced by degradation in both stability and reliability.

Today, one of the most promising solutions to combine high $\mu_{fe}$ values and good stability seems to be to use a Ba interface layer on Si face for planar MOS channels, while the use of trench or groove gates to build (only) the channel on other crystallographic orientation prevails. Yet, novel issues appear for this configuration, such as a poor breakdown voltage capability. As a final important remark, at high voltage and high temperature operation, a high $\mu_{fe}$ value is not necessary as the on-state losses are driven by the drift layer, and not anymore by the channel.

## Acknowledgments

This work was partially supported by the European Commission through the SPEED FP7 Large Project (NMP3-LA-2013–604057) and by the HiVolt-Tech project funded by the Spanish Government (TEC2014-54357-C2-1-R) cofounded by the EU-ERDF (FEDER).

## References

[1] J.W. Palmour, J.A. Edmond, H.S. Kong, C.H. Carter Jr., Proceedings of the 28th Intersoc. Energy Conversion Energy Conference, 1993., pp. 1249–1254.
[2] T. Kimoto, J.A. Cooper, Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices and Applications, John Wiley & Sons-IEEE, 2014.
[3] M. Krieger, S. Beljakowa, et al., Mater. Sci. Forum 645–648 (2010) 463–468.
[4] A. Pérez-Tomás, P. Godignon, N. Mestres, J. Millán, Microelectron. Eng. 83 (2006) 440–445.
[5] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, Jpn. J. Appl. Phys. 30 (2000) 2008–2011.
[6] A. Schoner, M. Krieger, G. Pensl, M. Abe, H. Nagasawa, Chem. Vap. Depos. 12 (2006) 523–526.
[7] M. Kobayashi, H. Uchida, A. Minami, T. Sakata, R. Esteve, A. Schoner, Mater. Sci. Forum 679–680 (2011) 645–648.
[8] L.A. Lipkin, J.W. Palmour, J. Electron. Mater. 25 (5) (1996) 909–915.
[9] H. Li, S. Dimitrijev, H. Barry Harrison, D. Sweatman, Appl. Phys. Lett. 70 (1997) 2028–2030.
[10] W. Schaffer, G. Negley, K. Irvine, J. Palmour Proc. Mater. Res. Soc. 339 (1994).
[11] V.V. Afanas'ev, M. Bassler, G. Pensk, M. Schulz, Phys. Status Solidi (A) 162 (1997) 321–337.
[12] H.A. Moghadam, S. Dimitrijev, J. Han, D. Haasmann, Microelectron. Reliab. 60 (2016) 1–9.
[13] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, M. Di Ventra, S.T. Pantelides, L.C. Feldman, R.A. Weller, Appl. Phys. Lett. 76 (13) (2000) 1713–1715.
[14] G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R.K. Chanana, R.A. Welles, IEEE Electr. Device Lett. 22 (4) (2001) 176–178.
[15] T. Kimoto, Y. Kanzaki, M. Noborio, H. Kawano, H. Matsunami, Mater. Sci. Forum 338 (2004) 737–740.
[16] A. Chanthaphan, T. Hosoi, T. Shimura, H. Watanabe, AIP Adv. 5 (9) (2015).
[17] G. Chung, C.C. Tin, J.R. Williams, K. McDonald, M. Di Ventra, R.K. Chanana, S.T. Pantelides, L.C. Feldman, R.A. Weller, Appl. Phys. Lett. 77 (22) (2000) 3601–3603.
[18] E. Pitthan, A.L. Gobbi, H.I. Boudinov, F.C. Stedile, J. Electron. Mat. 44 (8) (2015).
[19] A. Modic, Y.K. Sharma, Y. Xu, G. Liu, A.C. Ahyi, J.R. Williams, L.C. Feldman, S. Dhar, J. Electron. Mat. 43 (4) (2014).
[20] X. Zhu, A.C. Ahyi, M. Li, Z. Chen, J. Rozen, L.C. Feldman, J.R. Williams, Solid-State Electron. 57 (1) (2011) 76–79.
[21] M.J. Tadjer, A. Constant, P. Godignon, S. Martin-Horcajo, A. Boscá, F. Calle, M. Berthou, J. Millán, Mater. Sci. Forum 740–742 (2013) 553–556.
[22] A. Constant, N. Camara, J. Montserrat, E. Pausas, J. Camassel, P. Godignon, Mater. Sci. Forum 679–680 (2011) 500–503.
[23] M. Maranowski, J.A. Cooper Jr., IEEE Trans. Electron Devices 46 (3) (1999) 520–524.
[24] L.A. Lipkin, J.W. Palmour, IEEE Trans. Electron Devices 46 (3) (1999) 525–532.
[25] K. Matocha, G. Dunne, S. Soloviev, R. Beaupre, IEEE T. Electron Dev. 55 (8) (2008) 1830–1834.
[26] K. Matocha, P. Losee, A. Gowda, E. Delgado, G. Dunne, R. Beaupre, L. Stevanovic, Mater. Sci. Forum 645–648 (2010) 1123–1126.
[27] Z. Chbili, K.P. Cheung, J.P. Campbell, J. Chbili, M. Lahbabi, D.E. loannou, K. Matocha, Mater. Sci. Forum 858 (2016) 615–618.
[28] E.Ö. Sveinbjörnsson, F. Allerstam, H.Ö. Ólafsson, G. Gudjónsson, D. Dochev, T. Rödle, R. Jos, Mater. Sci. Forum 556–557 (2007) 487–492.
[29] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, IEEE Electron Devices Lett. 31 (7) (2010) 710–712.
[30] Y.K. Sharma, A.C. Ahyi, T. Issacs-Smith, X. Shen, S.T. Pantelides, X. Zhu, L.C. Feldman, J. Rozen, J.R. Williams, Solid-State Electron. 68 (2012) 103–107.
[31] T. Sledziewski, M. Weber, H.B. Krieger, Mater. Sci. Forum 858 (2016) 697–700.
[32] A. Schoner, M. Krieger, H.B. Weber, A. Mikhaylov, S. Reshanov, T. Sledziewski, Mater. Sci. Forum 778 (2014) 575–578.
[33] H. Yano, Natsuko Kanafuji, A. Osawa, T. Hatayama, T. Fuyuki, IEEE Trans. Electron Devices 62 (2) (2015) 324–332.
[34] Y.K. Sharma, A.C. Ahyi, T. Isaacs-Smith, A. Modic, M. Park, Y. Xu, E.L. Garfunkel, S. Dha, L.C. Feldman, J.R. Williams, IEEE Electron Device Lett. 34 (2) (2013) 175–177.
[35] T. Akagi, H. Yano, T. Hatayama, T. Fuyuki, Mater. Sci. Forum 740–742 (2012) 695–698.
[36] P. Fiorenza, F. Giannazzo, M. Vivona, A. La Magna, F. Roccaforte, Appl. Phys. Lett. 103 (15) (2013) 153508.
[37] K. Ueno, T. Oikawa, IEEE Electron Device Lett. 20 (12) (1999) 624–626.
[38] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, T. Fuyuki, IEEE Electron Devices Lett. 31 (7) (2010) 710–712.
[39] A. Modic, G. Liu, A.C. Ahyi, Y. Zhou, P. Xu, M.C. Hamilton, J.R. Williams, L.C. Feldman, S. Dhar, IEEE Electron Device Lett. 35 (9) (2014) 894–896.
[40] A.C. Ahyi, A. Modic, C. Jiao, Y. Zheng, G. Liu, L.C. Feldman, S. Dhar, Mater. Sci. Forum vols. 821–823, (2015) 693–696.
[41] D. Okamoto, M. Sometani, S. Harada, R. Kosugi, Y. Yonezawa, H. Yano, IEEE Electron Device Lett. 35 (12) (2014) 1176–1178.
[42] X. Shen, S. Pantelides, Proceedings of the 11th annual SiC MOS workshop meeting, UMD College Park, August 15, 2016.
[43] D. Okamoto, M. Sometami, S. Harada, R. Kosugi, Y. Yonezawa, H. Yano, Appl. Phys. A (2017) 123–133.
[44] S. Miyazaki, K. Morino, M. Hirose, Solid State Phenom. 76–77 (2001) 149–152.
[45] M. Cabello, V. Soler, N. Mestres, J. Montserrat, J. Rebollo, J. Millán, P. Godignon, Mater. Sci. Forum 897 (2017) 352–355.
[46] M. Cabello, V. Soler, J. Montserrat, J. Rebollo, J.M. Rafí, P. Godignon, Appl. Phys. Lett. 111 (2017) 042104.
[47] V.V. Afanas'ev, A. Stesmans, Appl. Phys. Lett. 82 (2003) 568.
[48] T. Isaacs-Smith, Y. Zheng, C. Jiao, C. Ahyi, S. Dhar, Proceedings of the Mater. Research Society Spring Meeting & Exhibit, Phoenix Arizona, 4, 2016.
[49] Y. Zheng, T. Isaacs-Smith, A.C. Ahyi, S. Dhar, Proceedings of the 11th European Conference on Silicon Carbide and Related Materials, Mater. Sci. Forum, 2016.
[50] T. Sledziewski, M. Vivona, K. Alassaad, P. Kwasnicki, R. Arvinte, S. Beljakowa, H.B. Weber, F. Giannazzo, H. Peyre, V. Souliere, T. Chassagne, M. Zielinski, S. Juillaguet, G. Ferro, F. Roccaforte, M. Krieger, J. Appl. Phys. 120 (20) (2016) 205701.
[51] D.J. Lichtenwalner, L. Cheng, S. Dhar, A. Agarwal, J.W. Palmour, Appl. Phys. Lett. 105 (18) (2014) 182107.

[52] D.J. Lichtenwalner, Mater. Sci. Forum 858 (2016) 671–676.
[53] D.J. Lichtenwalner, Mater. Sci. Forum 897 (2017) 163–166.
[54] S.K. Gupta, J. Singh, J. Akhtar, Physics and Technology of Silicon Carbide Devices (Chapter 8), InTech Publications, 2016, pp. 208–234.
[55] M. Nawaz, Active and passive electronic components, 2015 (2015) (id. 651527).
[56] E. Schilirò, P. Fiorenza, S. Di Franco, C. Bongiorno, M. Saggio, F. Roccaforte, R. Lo Nigro, Phys. Status Solidi A 214 (4) (2017) (id. 1600365).
[57] S. Hino, T. Hatayama, J. Kato, E. Tokumitsu, N. Miura, T. Oomori, Appl. Phys. Lett. 92 (18) (2008) (Id. 183503).
[58] T. Hatayama, S. Hino, N. Miura, T. Oomori, E. Tokumitsu, IEEE Trans. Electron Devices 55 (8) (2008) 2041–2045.
[59] K.Y. Cheong, J.H. Moon, D. Eom, H.J. Kim, W. Bahng, N.-K. Kim, Electrochemical and solid-state letters, 10 (2) (2007) 69–71.
[60] K.Y. Cheong, J.M. Moon, T.-J. Park, et al., IEEE Trans. Electron Devices 54 (12) (2007) 3409–3413.
[61] K.Y. Cheong, J.H. Moon, H.J. Kim, W. Bahng, N.-K. Kim, J. Appl. Phys. 103 (8) (2008).
[62] R. Mahapatra, A.K. Chakraborty, A.B. Hoesfall, N.G. Wright, G. Beamson, K.S. Coleman, Appl. Phys. Lett. 92 (4) (2008).
[63] A. Taube, S. Gierałtowska, T. Gutt, et al., Acta Phys. Pol. A 119 (5) (2011) 696–698.
[64] A. Pérez-Tomás, M.R. Jennings, P.M. Gammon, et al., Microelectron. Eng. 85 (4) (2008) 704–709.
[65] A. Pérez-Tomás, P. Godignon, J. Montserrat, J. Millán, N. Mestres, P. Vennegues, J. Stoemenos, J. Electrochem, Society 152 (4) (2005) G259–G265.
[66] X. Yang, B. Lee, V. Misra, IEEE Electron Device Lett. 36 (4) (2015) 312–314.
[67] X. Yang, B. Lee, V. Misra, IEEE Trans. Electron Devices 62 (11) (2015) 3781–3785.
[68] J.H. Moon, K.Y. Cheong, D. Eom, H.K. Song, J.H. Yim, J.H. Lee, H.J. Na, W. Bahng, N.-K. Kim, H.J. Kim, Mater. Sci. Forum 556–557 (2007) 643–646.
[69] J. Senzaki, K. Fukuda, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, T. Suzuki, K. Arai, Mater. Sci. Forum 389–393 (2002) 1061–1064.
[70] C. Blanc, D. Tournier, P. Godignon, D.J. Bring, V. Souliere, J. Camassel, Mater. Sci. Forum 527–529 (2006) 1051–1054.
[71] T. Hiyoshi, T. Masuda, K. Wada, S. Harada, Y. Namikawa, Mater. Sci. Forum 740–742 (2013) 506–509.
[72] S. Nakazawa, T. Okuda, J. Suda, T. Nakamura, T. Kimoto, IEEE Trans. Electron Devices 62 (2) (2015) 309–315.
[73] T. Kobayashi, S. Nakazawa, T. Okuda, J. Suda, T. Kimoto, Appl. Phys. Lett. 108 (15) (2016) (id. 152108).
[74] D. Peters, T. Basler, B. Zippelius, T. Aichinger, W. Bergner, R. Esteve, D. Kueck, R. Siemieniec, Power Electron. Eur. 3 (2017) 25–27.
[75] K. Ushida et als., Proceedings of the IEEE 27th International Symp. Power Semicond. Devices & IC's, Hong-Kong, 2015, pp. 85–88.
[76] K. Fukuda, M. Kato, S. Harada, et al., Mater. Sci. Forum 527–529 (2006) 1043.
[77] M. Okamoto, M. Iijima, K. Fukuda, H. Okumura, Jpn. J. Appl. Phys. 51 (4R) (2012) (id. 046504).
[78] H. Watanabe, T. Kirino, Y. Kagei, et al., Mater. Sci. Forum 679–680 (2011) 386–389.
[79] W. Si, M. Dudley, H.S. Kong, C. Carter, J. Electron. Mater. 26 (3) (1997) 151–159.
[80] S. Leone, H. Pedersen, A. Henry, et al., J. Cryst. Growth 311 (12) (2009) 3265–3272.
[81] M. Florentin, M. Cabello, J. Rebollo, J. Montserrat, P. Brosselard, A. Henry, P. Godignon, Semicond. Sci. Tech. 32 (2017) (id. 035006).
[82] M. Vivona, P. Fiorenza, T. Sledziewski, M. Krieger, T. Chassagne, M. Zielinski, F. Roccaforte, Appl. Surf. Sci. 364 (2016) 892–895.
[83] Y. Hijikata, H. Yaguchi, S. Yoshida, Appl. Phys. Express 2 (2) (2009) (id. 021203).
[84] H. Kurimoto, K. Shibata, C. Kimura, H. Aoki, T. Sugino, Appl. Surf. Sci. 253 (5) (2006) 2416–2420.
[85] T.P. Chow, H. Naik, Mater. Sci. Forum 778 (2014) 607–610.
[86] S.M. Thomas, Y.K. Sharma, M.A. Crouch, C.A. Fisher, A. Perez-Tomas, M.R. Jennings, P.A. Mawby, IEEE J. Electron Devices Soc. 2 (5) (2014) 114–117.
[87] T. Hosoi, et al., Mater. Sci. Forum 897 (2017) 323–326.
[88] M.J. Tadjer, A. Constant, P. Godignon, S. Martin-Horcajo, A. Boscá, F. Calle, M. Berthou, J. Millán, Mater. Sci. Forum 740–742 (2013) 553–556.
[89] V. Soler, M. Cabello, J. Montserrat, J. Rebollo, J. Millan, P. Godignon, M. Berthou, E. Bianda, A. Mihaila, Proceedings of the International Symp. Power Semicond. Devices and ICs, 2016, pp. 283–286, id. 7520833.
[90] R. Oldham, F.B, IEEE Trans. Nucl. Sci. 50 (3) (2003).
[91] M. Florentin, M. Alexandru, A. Constant, P. Michel, J. Montserrat, J. Millan, P. Godignon, Mater. Sci. Forum 821–823 (2015) 667–672.
[92] M. Florentin, J. Millán, P. Godignon, M. Alexandru, A. Constant, B. Schmidt, Proceedings of the European Solid-State Device Research Conference, id. 6948780, 2014, pp. 150–153.