Trends in Power Semiconductor Devices

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(Invited Paper)

***Abstract*—This paper reviews recent trends in power semiconductor device technology that are leading to improvements in power losses for power electronic systems. In the case of low voltage (<100 V) power rectifiers, the silicon P-i-N rectifier has been displaced by the silicon Schottky rectifier, and it is projected that the silicon TMBS rectifier will be the preferred choice in the future. In the case of high voltage (>100 V) power rectifiers, the silicon P-i-N rectifier continues to dominate but significant improvements are expected by the introduction of the silicon MPS rectifier followed by the GaAs and SiC based Schottky rectifiers.**

Equally important developments are occurring in power switch technology. The silicon bipolar power transistor has been displaced by silicon power MOSFET's in low voltage (<100 V) systems and by the silicon IGBT's in high voltage (>100 V) systems. The process technology for these MOS-gated devices has shifted from V-MOS in the early 1970's to DMOS in the 1980's, with more recent introduction of the UMOS technology in the 1990's. For the very high power systems, the thyristor and GTO continue to dominate, but significant effort is underway to develop MOS-gated thyristors (MCT's, EST's, DG-BRT's) to replace them before the turn of the century. Beyond that time frame, it is projected that silicon carbide based switches will begin to displace these silicon devices.

I. Introduction

POWER semiconductor devices play a crucial role in the regulation and distribution of power and energy in the world. By some estimates, more than 60 percent of all the power utilized in the United States flows through at least one power device and more often through multiple devices. Consequently, the performance of power rectifiers and switches has a significant impact on the efficient use of electricity. In the power electronics community, it is well recognized that the improvements in system performance in terms of efficiency, size, and weight are driven by enhancements made in semiconductor device characteristics.

Some of the prominent applications for power semiconductor devices are shown in Fig. 1, where the boxes indicate the device voltage and current ratings required to meet the system needs. It is obvious that the device ratings span a very broad range of voltages and currents. At relatively low voltages (< 100 V), two important applications are in power supplies for computers, telecommunications or office equipment, and for automotive electronics. With the proliferation of personal computers, an improvement in the efficiency of the power supply is essential to reduce wastage of electricity. This will also lead to a reduction in the size and weight of the computer

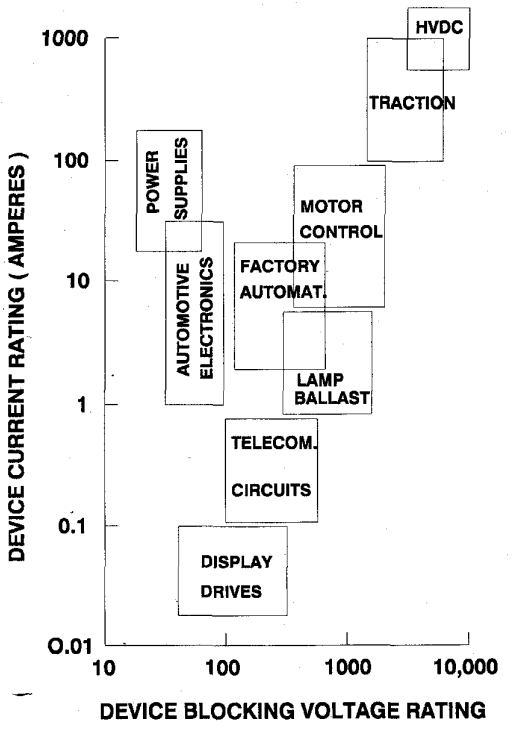

Fig. 1. Applications for power semiconductor devices.

which is attractive to consumers. The growth in power device applications in automotive electronics is occurring due to the introduction of the multiplex bus architecture to replace point-by-point wiring in order to enhance manufacturability and reduce the weight of the wiring harness. This trend, which has already been implemented in luxury cars, is expected to spill over to all automobiles in the future. Such a multiplex bus architecture can only be implemented by using smart power control at each of the large number of loads (lamps, motors, etc.) that are distributed throughout the car. These loads demand currents in the range of 1 to 10 A which need to be controlled by power switches that must withstand up to 100 V due to spikes in the nominally 12 V power bus.

As indicated in Fig. 1, there are applications, such as displays and telecommunication circuits, for power devices operating at relatively low currents (< 1 A) and high voltages (> 100 V). Due to large number of high voltage transistors required in these systems, it is advantageous and cost effective to satisfy the needs of these applications by using monolithic power integrated circuits, which have been developed using

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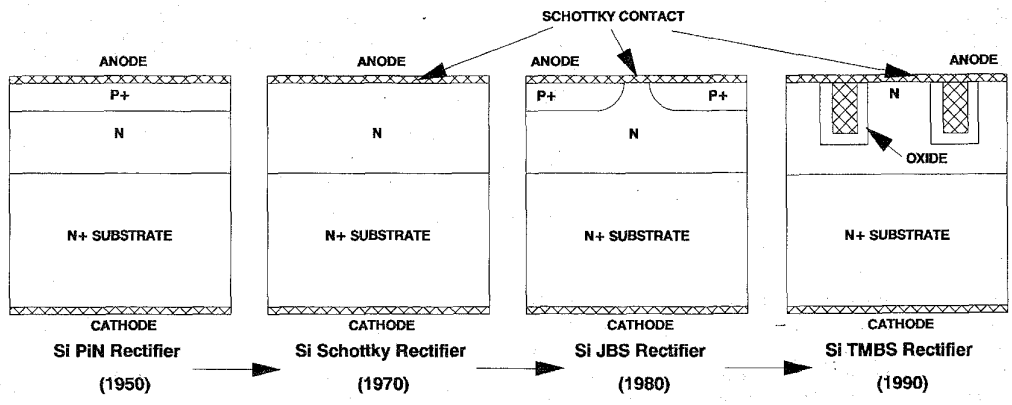

Fig. 2. Evolution of low voltage (<100 V) power rectifiers.

both junction isolation (JI) and dielectric isolation (DI) technologies. The DI technology based on direct wafer bonding is finding favor for power applications with the most recent work aimed at extending the current handling capability by implementing lateral IGBT's with 500 V blocking capability. The reader should refer to a prior review [1] of this technology for more details. For the medium power applications that span 10 to 100 A and 300 to 1200 V, multi-chip modules are the preferred cost effective implementation today. These modules contain rectifiers, power switches, and the control circuit within a single package. The more advanced intelligent power modules [2] allow local diagnostics for protection against adverse operating environments. The preferred devices for these modules are insulated gate bipolar transistors (IGBT's).

Turning to the high power end of the applications spectrum, devices are needed for traction (electric street-cars and locomotives), and for power distribution networks. The traction applications at present utilize gate turn-off thyristors (GTO's), which are current controlled devices with low current gain (typically less than three). This has motivated development of MOS-gated thyristors which will be reviewed in this paper. In the case of high voltage dc transmission (HVDC) systems, the preferred devices are light triggered thyristors, which are unlikely to be replaced by any alternate technology in the future.

In this review paper, the trends in power rectifiers will be first considered followed by those for power switches. On the basis of the above discussion regarding applications for power devices, it is obvious that the demands on power devices span a huge range of voltages and currents. The current rating of power devices can be scaled by increasing the area. However, no single device structure has yet been conceived that performs optimally over the entire range of voltages from 50 to 10 000 V. Consequently, these sections will be partitioned into devices relevant for low voltage (< 100 V) applications and those relevant for high voltage (> 100 V) applications.

II. Power Rectifiers

Power rectifiers are needed for all the applications shown in Fig. 1. During the 1950's, the P-i-N rectifier was commercially introduced for power electronics applications. Since then there have been continuous improvement in the ratings of these devices based upon the demand for them in higher power applications. In addition, new device structures have been introduced in order to improve their switching performance. The silicon device structure that has been found to be the most suitable for each application depends upon the voltage rating of the rectifier. For this reason, the developments in low voltage (<100 V) rectifiers will be discussed first followed by those that impact high voltage systems.

A. Low Voltage Power Rectifiers

Power rectifiers with reverse blocking capability of less than 100 V are required for applications such as switch mode power supplies and automotive electronics. The first devices available for these applications were germanium rectifiers. However, the high leakage currents in germanium devices associated with its small energy bandgap (0.66 eV) led to its replacement by silicon P-i-N rectifiers.

The basic P-i-N rectifier structure is shown in Fig. 2. The doping concentration and thickness of the i-region is designed to support the required reverse blocking voltage [3]. During on-state current flow, the P^+ and N^+ regions inject a high concentration of holes and electrons into the i-region, when the applied bias exceeds the junction built-in potential, leading to an increase in its conductivity. This is responsible for the on-state voltage drop of the P-i-N rectifier being close to 1 V for these low breakdown voltage structures. When the voltage across the device reverses polarity, the injected electron-hole population (called stored charge) must be removed before the formation of a depletion region can occur to support the reverse blocking voltage. This leads to a reverse recovery current that is typically equal in magnitude to the on-state current. The presence of a reverse recovery transient leads to power dissipation that limits the maximum switching frequency for P-i-N rectifiers.

In order to eliminate the reverse recovery problems associated with P-i-N rectifiers, the Schottky barrier diode (SBD) was developed in the 1970's [3]. As shown in Fig. 2, its structure consists of a metal-semiconductor rectifying contact with a N-drift region which is designed to support the required reverse blocking voltage. Forward conduction in the

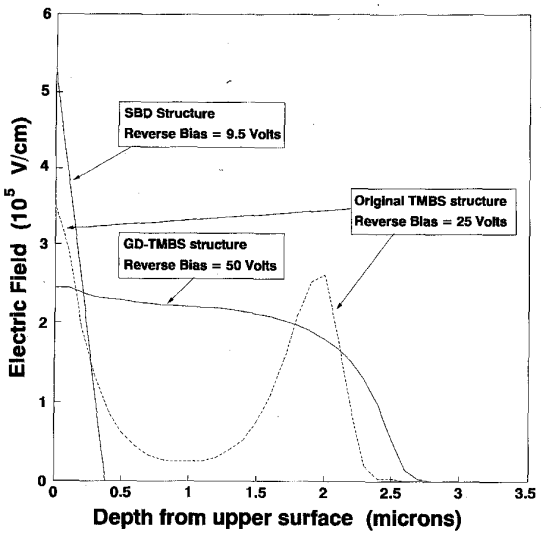

Fig. 3. Comparison of electric field distribution in Schottky (SBD) rectifier, original TMBS rectifier, and TMBS rectifier with graded doping profile (GD-TMPS). Note that the device are operating at different reverse blocking voltages.

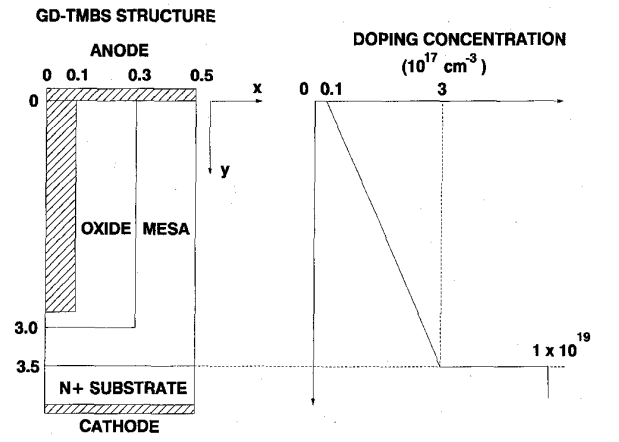

Fig. 4. Structure and doping profile for the TMBS rectifier with a graded doping concentration.

SBD occurs by the transport of electrons across the metal-semiconductor barrier. The on-state voltage drop of the SBD consists of the sum of the voltage drop across this barrier and the ohmic voltage drop across the N-drift region. For low breakdown voltages (<100 V), the doping concentration of the N-drift region can lie between 5×10^{15} and 1×10^{16} cm^{-3} and its thickness can be made less than 10 μm. This leads to a relatively modest voltage drop in the drift region resulting in a net on-state voltage drop of about 0.55 V for state-of-the-art devices. By replacing the P-i-N rectifier with the SBD, it is possible to obtain a reduction in on-state power loss by a factor of two. In addition, a significant advantage of SBD's is their faster switching speed because of the absence of the reverse recovery current transient observed in P-i-N rectifiers, thus, allowing the operation of switch mode power supplies at higher frequencies. It has been found that operation at higher frequencies results in a more compact power supply due to a shrink in the size of the magnetic components (inductors and transformers).

The efficiency of switch mode power supplies has been found to be strongly dependent upon the voltage drop across the output rectifiers in relation to the output voltage [4]. A 10 percent loss in efficiency occurs in the case of a 5 V power supply with a conventional SBD having an on-state voltage drop of 0.55 V. The loss in efficiency will become much worse when the output voltage of the power supply is reduced to 3.3 and 1.6 V in the future as demanded by the voltage scaling required for future generations of VLSI chips. It is therefore imperative that rectifiers be developed with lower on-state voltage drop. One of these approaches is the junction barrier controlled Schottky (JBS) rectifier shown in Fig. 2 [3]. This structure consists of a SBD with a junction grid integrated under the metal-semiconductor contact. The junction grid serves to prevent Schottky barrier lowering, a phenomenon that produces poor reverse blocking characteristics with high leakage currents. JBS rectifiers have been fabricated with on-state voltage drops of 0.35 V [5], [6] by using VLSI technology. Further reduction in on-state voltage drop was not possible due to the area taken up by the junction regions.

An even superior low voltage power rectifier was conceived and experimentally demonstrated recently based upon incorporation of a trench MOS structure below the metal-semiconductor contact [7]. The cross-section of the TMBS rectifier is shown in Fig. 2. The charge coupling between the donors in the mesa region and the metal on the trench sidewalls produces a redistribution of the electric field under the metal-semiconductor contact. In the case of the SBD, the electric field reduces linearly with distance as predicted by Poisson's equation for a parallel plane junction. For a doping concentration of 1×10^{17} cm^{-3}, this results in a breakdown voltage of 9.5 V. In contrast with this, the electric field in the TMBS structure takes the form shown in Fig. 3 with two peaks—one located at the metal-semiconductor interface and a second at the bottom of the trench. It has been demonstrated that this field redistribution allows supporting a much higher voltage (25 V) than predicted by parallel-plane theory. Further, the peak electric field at the metal-semiconductor interface is small leading to less leakage current. Due to the high doping concentration in the mesa region, the TMBS rectifiers also exhibit a very low on-state voltage drop of 0.2 V.

Based upon two-dimensional numerical simulations of the original TMBS rectifier structure, it was concluded that the maximum reverse blocking voltage of the device was limited to 25 V [7]. This was due to the high electric field at the bottom of the trenches. However, an improvement in the reverse blocking voltage can be achieved without significant increase in the on-state voltage drop by changing the doping profile in the mesa region. The proposed doping profile and device cross-section is shown in Fig. 4. In the TMBS structure with graded doping concentration (GD-TMBS), the doping concentration increases linearly from 1×10^{16} cm^{-3} at the metal-semiconductor interface to 3×10^{17} cm^{-3} at the boundary between the epitaxial layer and the N^+ substrate. In

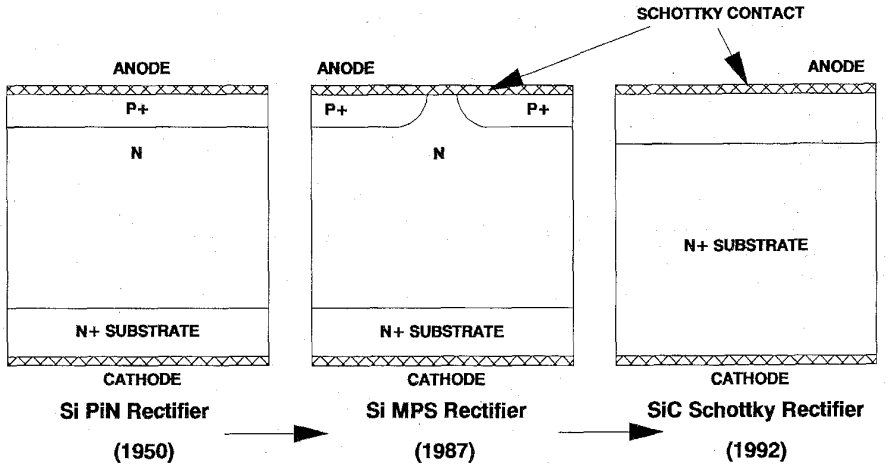

Fig. 5. Evolution of high voltage (>300 V) power rectifiers.

addition, the oxide thickness in the trench region is increased from 500 Å for the conventional TMBS structure to 2000 Å to alleviate high electric fields at the bottom of the trench. It has been found by two-dimensional numerical simulations that this combination of structural changes alters the electric field distribution in the mesa region to a relatively constant electric field with depth as shown in Fig. 3. Note that electric field at the metal-semiconductor interface is even lower than for the conventional TMBS rectifier even though the GD-TMBS rectifier has twice the reverse blocking voltage applied to it. Consequently, it has been found that the GD-TMBS rectifier can support 60 V for a trench depth of 2 μm. Further, the on-state voltage drop in the GD-TMBS rectifier has been found to be only 10 mV higher than for the conventional TMBS structure. Thus, the GD-TMBS rectifier allows extension of the concept to higher blocking voltages with little penalty on the on-state voltage drop. The linearly graded doping profile proposed for the GD-TMBS structure can be easily obtained during epitaxial growth of the N drift layer on the N^+ substrates with computer controlled epitaxial growth processes that are in production today. The commercialization of the TMBS structure offers great benefits for improving the efficiency of power supplies with output voltages ranging from 5 V (used at present) down to 1.6 V (as needed in the future).

B. High Voltage Power Rectifiers

High voltage power rectifiers are needed for many applications such as motor control. Most commercial systems utilize the P-i-N rectifier structure shown in Fig. 5 which is essentially identical to the low voltage P-i-N rectifier shown in Fig. 2 with a wider i-region to increase its reverse blocking capability. These devices are available with blocking voltages in excess of 5000 V. Their primary drawback has been the large reverse recovery current flow during switching from the on-state to the reverse blocking state due to the large amount of stored charge in the drift region. Many methods of lifetime control have been developed to reduce the lifetime in the drift region to decrease the turn-off time but they all lead to an increase in the on-state voltage drop [3]. It is therefore customary to perform a trade-off between on-state and turn-off losses when designing these devices.

A superior trade-off curve can be obtained by using the merged P-i-N/Schottky (MPS) rectifier structure shown in Fig. 5 and the Static Shielded Diode (SSD) structure [8], [9]. As the charge in the P-region under the metal of the SSD structure becomes smaller, its performance begins to resemble that for the MPS rectifier. Although the MPS structure appears to be similar to the JBS structure shown in Fig. 2, its physics of operation is different because of injection of minority carriers from the junction (a phenomenon that is absent for the JBS device). In the JBS rectifier, the on-state voltage drop is less than 0.5 V making the junction potential insufficient for the injection of carriers. In the MPS rectifier, the on-state voltage drop is about 1 V leading to the injection of minority carriers into the drift region. This injection leads to a reduction in the resistance of the drift region below the Schottky contact allowing a large proportion of the on-state current to flow thorough the metal-semiconductor contact in the MPS rectifier. The resulting forward I-V characteristic for the MPS rectifier is shown in Fig. 6, which includes the characteristics of the Schottky diode and the P-i-N rectifier for comparison. It can be seen that the MPS rectifier behaves like the SBD at on-state voltage drops of less than about 0.6 V. However, unlike the SBD whose on-state current becomes limited by the large series resistance of the drift region, the on-state voltage drop of the MPS rectifier remains low due to the injection of carriers from the P-N junction at voltages above 0.7 V. It has been found by two-dimensional numerical simulations that the carrier distribution profile in the MPS rectifier results in a lower stored charge by a factor of upto eight times when compared with the P-i-N rectifier [8]. This produces a greatly reduced ($4\times$ smaller) reverse recovery current.

Due to the process compatibility of the MPS rectifier with the P-i-N rectifier, it is anticipated that the MPS rectifiers will become widely available for commercial applications. However, these devices cannot be considered as ideal for power switching because they still exhibit substantial reverse recovery transients. A much superior power rectifier can be

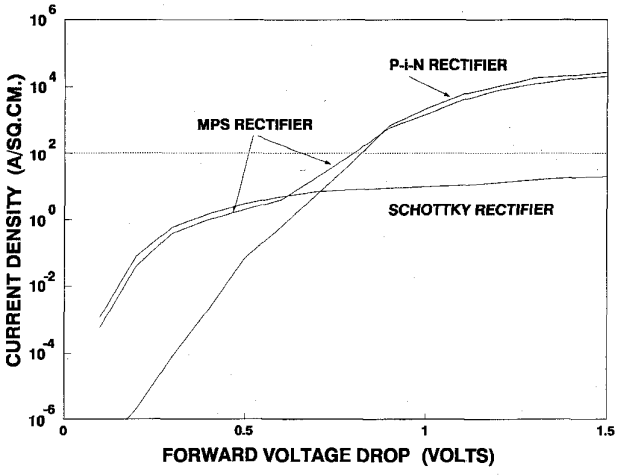

Fig. 6. Comparison of the forward I-V characteristics of the MPS rectifier with that for the P-i-N and Schottky rectifiers.

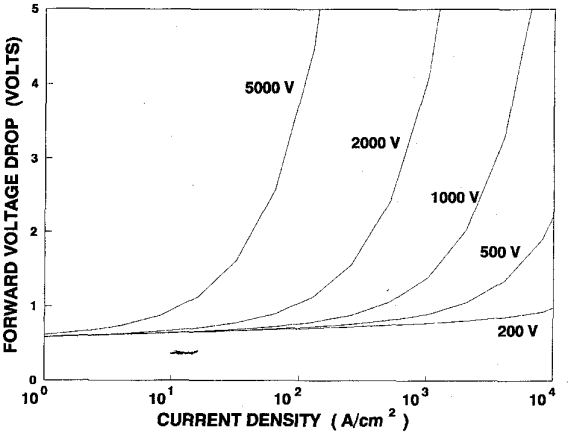

Fig. 7. Calculated on-state characteristics of silicon carbide Schottky rectifiers with breakdown voltages ranging from 200 to 5000 V. A Schottky barrier height of 1.0 eV was used for these calculations.

created by using the metal-semiconductor rectifying contact if the resistance of the drift region can be reduced while preserving the high blocking voltage capability. An approach for achieving this was first proposed in 1982 [10] by replacing silicon with a wide bandgap semiconductor. Based upon this fundamental analysis, it was demonstrated that SBD's made from gallium arsenide would have good on-state voltage drop for blocking voltages upto 500 V. This was experimentally verified by fabrication of devices using aluminum and titanium Schottky barrier contacts [11], [12]. These devices have now become commercially available.

An even greater reduction in the resistance of the drift region can be projected for silicon carbide [13]. The predicted on-state characteristics for silicon carbide SBD's are shown in Fig. 7 for various reverse blocking voltages. From these plots, it can be concluded that rectifiers with blocking voltages in excess of 3000 V will have attractive on-state characteristics. The first high voltage silicon carbide SBD's with breakdown voltages of 400 V were reported in 1992 [14] followed by reports on 1000 V devices [15]–[17]. These devices have excellent switching behavior as expected with an on-state voltage drop of only 1 volt, thus, verifying the theoretical predictions. Although the cost of silicon carbide wafers is too high and the size of the wafers too small for commercial production of power SBD's at this time, it is anticipated that all the silicon P-i-N rectifiers will be replaced by silicon carbide SBD's in the twenty-first century.

III. Power Switches

Power switches are an essential component of all power electronic systems for the regulation of loads. The first power semiconductor switches were thyristors and bipolar transistors developed in the 1950's. Thyristors were used in higher power systems because their ratings were scaled at a faster pace than bipolar transistors. Thyristors are now available with ratings of 6500 V and 1000 A. These devices are manufactured from single 10 to 12.5 cm diameter wafers using a mature deep diffusion process technology with gallium and aluminum as dopants. In order to ensure good control over the breakdown voltage and uniform current distribution within the devices, it is essential that the background doping and the minority carrier lifetime are very uniform in the initial starting material. This has been achieved by using neutron transmutation doping [18] to produce a very uniform phosphorus concentration distribution, and by using electron irradiation to control the lifetime [19]. Light triggered thyristors have also become commercially available for high voltage dc (HVDC) transmission systems [20]. It is unlikely that these devices will be displaced unless the proposed change occurs from HVDC power transmission to Flexible AC transmission (FACT) in the future [21]. The FACT system requires the development of cost effective technology for rapid control of reactive elements which is expected to provide motivation for commercialization of MOS-gated thyristors that are under development as discussed later in this section of the paper.

Ever since their introduction in the 1950's, bipolar transistors were favored for low and medium power applications because of their faster switching capability. The ratings for these devices grew steadily until the late 1970's. Since the bipolar transistor is fundamentally a current controlled device, with the magnitude of the collector current determined by the base drive current, one of the most critical design goals has been to improve the current gain in order to reduce the complexity, size, and weight of the gate control circuit. Unfortunately, achieving a high current gain has been found to be in conflict with the achievement of high breakdown voltages. Further, the fall-off in current gain at typical operating current densities due to high level injection effects [22] leads to a gain of less than 10. The current gain can be improved by using the *Darlington configuration* [23] at the disadvantage of a considerable increase in the on-state voltage drop. For these reasons, the bipolar transistor has been displaced by the power MOSFET's for low voltage/power applications in the 1980's, and for medium voltage/power applications by the IGBT's in the 1990's. The evolution and status of these MOS-gated power devices is discussed in more detail in this section of the paper.

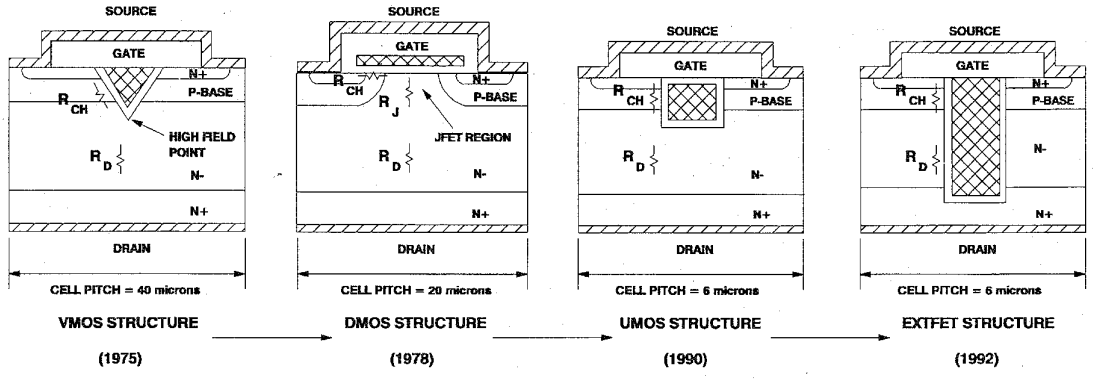

Fig. 8. Evolution of power MOSFET structures.

A. Low Voltage Power Switches

Power switches designed to operate at blocking voltages below 100 V are needed in power supplies, peripheral drives, and automotive electronic multiplex bus systems. The silicon MOSFET has become the dominant device technology for these applications for many reasons. Firstly, it has an excellent low on-state voltage drop due to the low resistance of the drift region that supports these modest voltages. Structural improvements that have enabled obtaining low on-state voltage drop are discussed in the next paragraph. Secondly, the power MOSFET has a very high input impedance in steady-state due to its metal-oxide-semiconductor (MOS) gate structure. It is classified as a voltage controlled device that can be controlled using integrated circuits because of the small gate currents that are required to charge and discharge the input gate capacitance. When the operating frequency becomes high (>100 kHz), this capacitive current can become significant but it is still possible to integrate the control circuit due to the low gate bias voltages (typically 5 to 15 V) required to drive the device into its to low state voltage drop regime of operation. Thirdly, in comparison with bipolar transistors, the MOSFET has a very fast inherent switching speed due to the absence of minority carrier injection. The switching time for the MOSFET is dictated by the ability to charge and discharge the input capacitance rapidly. Fourthly, the MOSFET has superior ruggedness and forward biased safe operating area (FBSOA) when compared with bipolar transistors which allows elimination of snubber circuits for protection of the switch during operation in typical hard-switching PWM circuits used for motor control.

Due to its many attractive features, there has been a concerted effort to optimize its structure, design, and process technology. The first power MOSFET's were developed in the 1970's based upon the VMOS structure shown in Fig. 8. The V-groove in the structure was created by using preferential etching with potassium hydroxide based solutions. This led to instabilities in the threshold voltage. In addition, the sharp tip at the bottom of the V-groove created a high electric field which degraded its breakdown voltage [24]. Consequently, the VMOS structure was displaced by the DMOS structure [25] shown in Fig. 8 which was based upon the diffusion of the P-base and N^+ source regions using the edge of the polysilicon as a masking boundary. This process enabled fabrication of sub-micron channel lengths without resorting to high resolution lithography by utilizing the difference in the junction depth of the two diffusions. Although the first 60 V DMOSFET's had a specific on-resistance (on-resistance per cm^2) of about 7 $m\Omega$-cm^2 based upon using a design rule of 10 μm in the 1970's, state-of-the-art devices that are manufactured in the 1990's have a specific on-resistance of 1 $m\Omega$-cm^2 by utilizing design rules of less than 2 μm. It has been demonstrated that the specific on-resistance can be reduced to 0.75 $m\Omega$-cm^2 by using VLSI design rules (1.25 μm) [26].

The resistance of the drift region required to support the blocking voltage with current transport under uniform distribution conditions is defined as the ideal specific on-resistance of the device [3]. In the case of a silicon FET with 60 V blocking capability, the ideal specific on-resistance can be calculated to be 0.165 $m\Omega$-cm^2. Thus, there is considerable opportunity to improve the performance of silicon power MOSFET's beyond the capability achieved with the DMOS structure. An effective method for achieving this goal is the UMOS structure shown in Fig. 8. The UMOS gate region can be fabricated by using trench etching processes originally developed for memory cells in DRAM's. With this process, the UMOS cell size can be made relatively small (6 μm) when compared with the DMOS cell (typically 20 μm) for the same design rules. This results in an increase in the channel density (channel width per sq. cm. of device area) and an elimination of the JFET component of the resistance inherent within the DMOS cell. Specific on-resistance for the 60 V UMOSFET of 0.58 $m\Omega$-cm^2 has been reported [27].

Even greater reduction in the specific on-resistance has been achieved by utilizing deep trench structures where the trench extends all the way down to the N^+ substrate as shown in Fig. 8 [28]. In this structure, the resistance contribution from the drift region is reduced by the parallel current flow path created by the formation of an accumulation layer on the sidewalls of the trench. It is theoretically possible to obtain a specific on-resistance even lower than the ideal limit for silicon with this structure if the cell pitch is reduced to below 2 μm. However, it must be noted that the blocking voltage of this structure is limited to 30 V by the high electric field created in the gate oxide by the extension of the trench into the N+ substrate. The specific on-resistance of experimentally

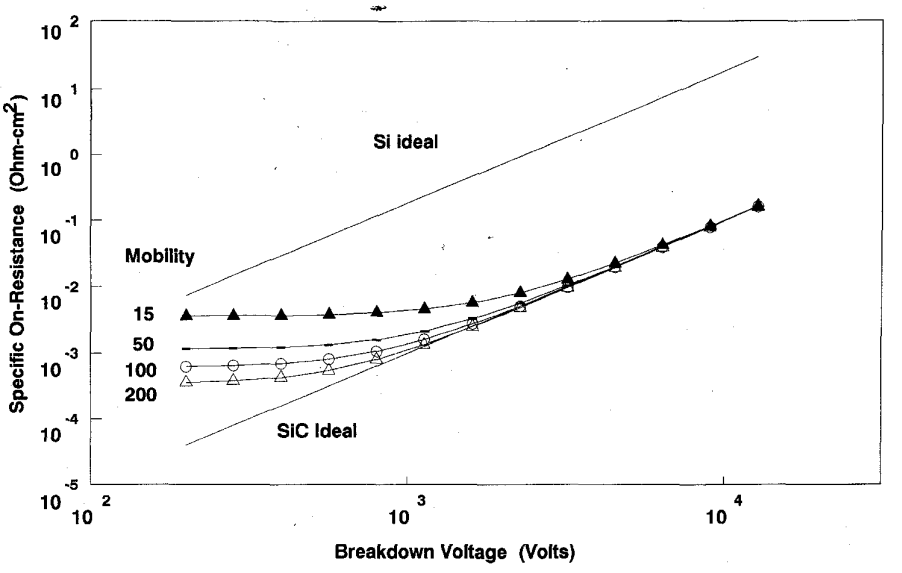

Fig. 9. Calculated specific on-resistance of silicon carbide power UMOSFET's using inversion layer mobilities ranging from 15 to 200 cm^2/V s.

fabricated devices with blocking voltage of 25 V was under 0.2 mΩ-cm^2 at a gate bias of 15 V. Based upon these results, it can be concluded that the advent of the UMOS technology has allowed fabrication of low voltage silicon devices that are approaching the limits for silicon FET performance.

Due to the very low specific on-resistance of the low voltage power MOSFET's, it has been proposed that these devices be used in place of rectifiers to reduce the on-state power losses. In this application, the device blocks voltage in the first quadrant of operation if the gate voltage is zero and conducts current in the third quadrant of operation if a positive bias is applied to the gate. Since it is necessary to synchronize the gate bias with the AC voltage applied across the device, these MOSFET's are called *synchronous rectifiers* [4]. The on-state power losses of the synchronous rectifier can be reduced by increasing the size (area) of the device to reduce its resistance. However, this is accompanied by an increase in its input capacitance. At the high (>200 kHz) operating frequencies of power supplies, a large gate drive power loss occurs due to the need to charge and discharge this input capacitance. It has been shown that the power loss exhibits a minimum value at an optimum device size [13]. When these considerations are taken into account, the power losses obtained with the synchronous rectifier have been found to be only slightly lower than those of conventional Schottky rectifiers and much higher than those for the TMBS rectifiers. Further, it is difficult to synchronize the gate drive voltage precisely at higher operating frequencies leading to unstable operation. In addition, the cost of the power MOSFET and its high frequency gate drive circuit is substantially higher than that of the rectifier it is expected to replace. These factors have hindered its widespread use.

B. High Voltage Power Switches

Due to its excellent electrical characteristics, it would be desirable to utilize power MOSFET's for high voltage power electronics applications. Unfortunately, the specific on-resistance of the drift region increases very rapidly with increasing breakdown voltage (as shown in Fig. 9) because of the need to reduce its doping concentration and increase its thickness. Thus, inspite of the ability to obtain nearly ideal specific on-resistance with silicon UMOSFET structures, they are not satisfactory for applications that require breakdown voltages above 300 V due to their high on-state power dissipation.

Insulated Gate Bipolar Transistor: This problem was resolved in the 1980's by the introduction of the Insulated Gate Bipolar Transistor (IGBT) in which bipolar current conduction is controlled by using an MOS-gate structure [29]. A cross-section of the DMOS-technology based IGBT structure introduced in the early 1980's is shown in Fig. 10. The equivalent circuit for this device consists of a wide-base P-N-P bipolar transistor driven by a short channel MOSFET [3]. Due to the injection of a high concentration of holes from the P^+ substrate into the N-drift region, the IGBT exhibits a P-i-N diode-like on-state characteristics with a forward voltage drop of less than 2 V at relatively high on-state current density (typically 100 A/cm^2). Since the input signal for the IGBT is a voltage applied to the MOS-gate, the IGBT shares the high input impedance advantages of the power MOSFET and can be classified as a voltage controlled device. However, unlike the MOSFET, the switching speed of the IGBT is limited by the time taken for removal of the stored charge in the drift region due to injection of holes during on-state current conduction. The turn-off time for the IGBT is dictated by the minority carrier lifetime which can be controlled by electron irradiation [30]. Although the electron irradiation process was successful in reducing the turn-off time, it was found that the on-state voltage drop of the IGBT increases after lifetime reduction as observed for all bipolar power devices.

The trade-off curve between the on-state voltage drop and the turn-off time for the nonpunch-through (NPT) epitaxial IGBT structure that was initially fabricated in the early 1980's

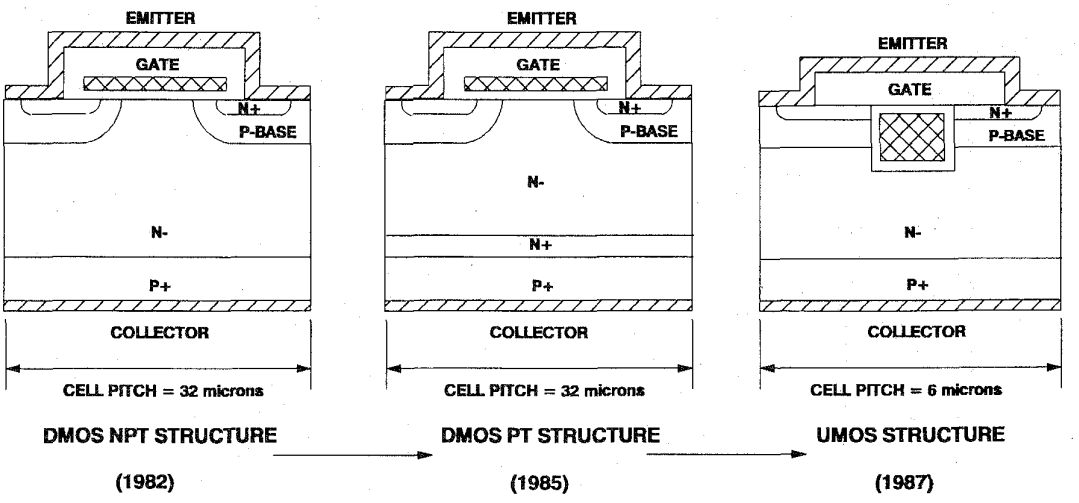

Fig. 10. Evolution of IGBT structures.

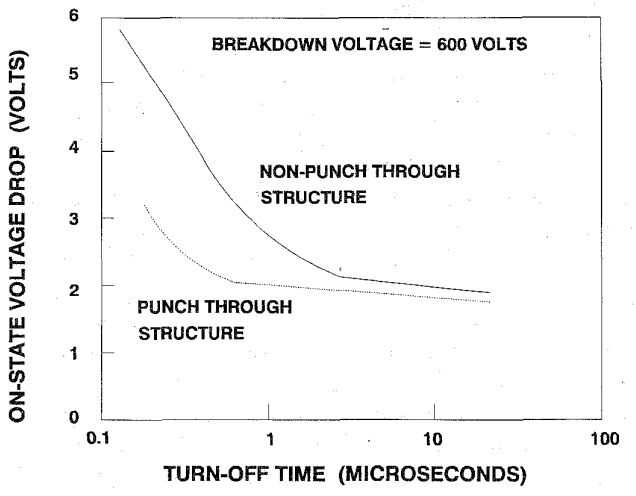

Fig. 11. Comparison of the trade-off curve between on-state voltage drop and turn-off time for the punch-through (PT) and nonpunch-through (NPT) IGBT structures.

is shown in Fig. 11 [3]. A significant increase in on-state voltage drop was observed for turn-off times of less than 1 microsecond. A significant improvement in the trade-off curve was subsequently obtained by using the punch-through (PT) epitaxial structure shown in Fig. 10. The PT structure allows supporting the same forward blocking voltage with about half the thickness of the N-base region of the P-N-P transistor resulting a greatly improved trade-off curve as shown in Fig. 11. Thus, the PT structure is preferred for IGBT's with forward blocking capability of upto 1200 V. For higher blocking voltages, the thickness of the drift region becomes too large for cost effective epitaxial growth. Consequently, the NPT structure fabricated using bulk starting material is preferred for IGBT's that must support more than 1500 V [31].

A more significant improvement in the trade-off between on-state voltage drop and turn-off time has been achieved by using the UMOS-gate structure for the IGBT [32] shown in Fig. 10. With the UMOS structure, the channel density is greatly increased and the JFET region is eliminated. In addition, it has been found that the electron-hole concentration is enhanced under the bottom of the trench due to the formation of the accumulation layer [33]. This creates a catenary type carrier distribution profile in the IGBT which resembles that obtained in thyristors. These improvements lead to a large reduction in the on-state voltage drop until it approaches that of a P-i-N diode [34]. Since the safe-operating-area of the UMOS structure has been shown to be superior to that for the DMOS structure, it can be anticipated that trench gate IGBT's will replace the DMOS IGBT structures in the future.

MOS-gated Thyristors: In spite of the on-going refinement of the IGBT structure to improve the trade-off curve between on-state voltage drop and turn-off time, its on-state power dissipation becomes large when designed for operation at higher frequencies and at high voltages. For this reason, considerable research has been performed on MOS-gated thyristors as alternative devices for power switching applications because the on-state voltage drop of thyristors is known to be lower than for IGBT's. The ability to turn-on a vertical thyristor structure with an integrated MOS-gate region was first reported in 1979 [35]. This approach is now used in all MOS-gated thyristors. The ability to turn-off current flowing in a thyristor has been found to be much more challenging because of the internal regenerative action and the negative temperature coefficient for the on-state voltage drop within thyristors. These effects easily lead to the formation of current filaments that can destroy the devices.

The first reported MOS-gated thyristor structure with current turn-off capability is the MOS-controlled thyristor (MCT) [36], [37]. In this device structure, whose cross-section is shown in Fig. 12, the regenerative action of the thyristor is interrupted by short-circuiting the N^+ emitter to the P-base region by using a MOSFET integrated within the P-base region. The ability to successfully turn-off the thyristor can only be achieved if the hole current flowing in the P-base region is shunted away from the emitter/base junction via the MOSFET without raising the potential of the P-base region above 0.7 V (the junction potential). If the resistance of the

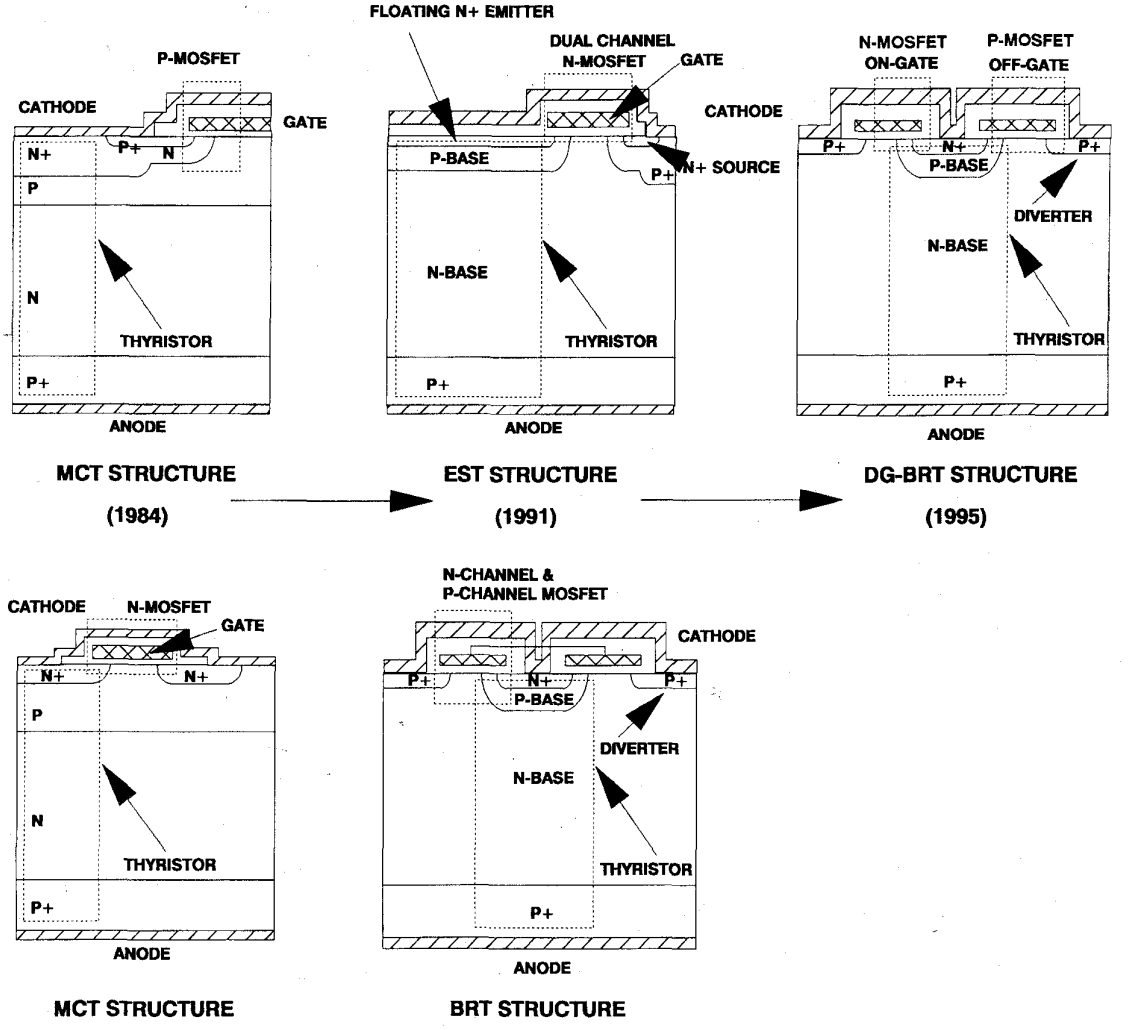

Fig. 12. Evolution of MOS-gated thyristor structures.

turn-off path is sufficiently low, the current flowing via the junction in the on-state can be fully diverted, suppressing injection of carriers from the N^+ emitter. This then results in a cessation of the regenerative action resulting in turn-off. Significant effort has been performed to optimize the MCT structure to improve its turn-off performance [38]–[42]. In order to prevent current filamentation, an MCT structure with an emitter ballast using a polysilicon resistor has also been demonstrated [43]. However, this was found to result in a significant increase in the on-state voltage drop which greatly diminishes the benefits of the MCT in comparison with the IGBT. Further, the MCT lacks the ability to saturate the anode current level making it a fundamentally different device than the IGBT from an applications viewpoint. The current saturation capability in IGBT's is routinely used to provide gate controlled turn-on for regulation of the reverse recovery in the associated rectifiers, and for providing short-circuit protection. With the MCT, it is necessary to change either the circuit topology or to introduce new snubber elements to the PWM circuits to account for lack of current saturation. This factor has been a major hinderance in making the MCT attractive for applications in spite of its lower on-state voltage drop than the IGBT.

In terms of device evolution, the next MOS-gated thyristor that has been reported is the base resistance controlled thyristor (BRT) shown in Fig. 12 [44]. In this case, the regenerative action of the thyristor is interrupted by short-circuiting the N^+ emitter to the P-base region by using a MOSFET integrated within the N-base region. The BRT has similar on-state characteristics to the MCT but has been found to have higher maximum controllable current capability [45]. Perhaps, its greater advantage is that it can be fabricated using the basic DMOS (IGBT-like) process while the MCT requires a triple-diffused process that is more difficult to master during the manufacturing of devices. However, the lack of current saturation capability makes the device unattractive when compared with the IGBT for power electronic applications.

The first MOS-gated thyristor structure with current saturation capability was the emitter switched thyristor (EST) shown in Fig. 12 [46]. This capability was achieved by forcing the thyristor current to flow via a lateral MOSFET integrated within the P-base region. The thyristor current could then

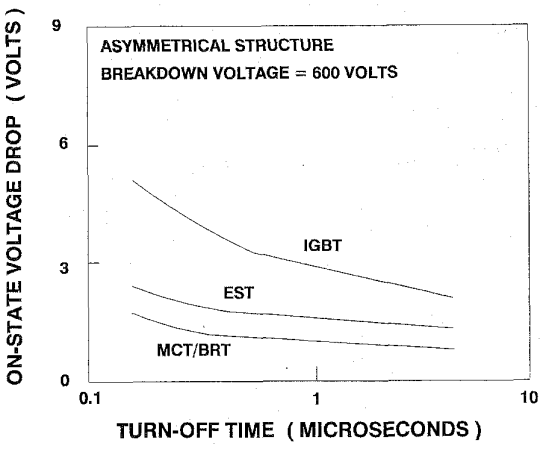

Fig. 13. Comparison of the trade-off curve between on-state voltage drop and turn-off time for the MOS-gated thyristors with the IGBT.

be controlled via the gate bias enabling current saturation. Although the first devices had only a small FBSOA, improved dual-channel structures with high voltage current saturation were subsequently developed [47]. The on-state voltage drop of the EST is larger than that of the thyristor, due to the additional voltage drop across the MOSFET, by about 0.5 V. This makes its trade-off curve superior to that for the IGBT but inferior to that for the MCT/BRT as shown in Fig. 13. However, the MOSFET serves as an emitter ballast for the thyristor within each EST cell resulting in a net positive temperature coefficient for the on-state voltage drop. This ensures uniform current distribution within multicellular devices and prevents current filamentation during turn-off.

During the selection of devices for power electronic applications, it is becoming increasingly common to perform a trade-off not only between on-state voltage drop and turn-off time, but also between these parameters and the FBSOA. An innovative technique for improving this three-fold trade-off is by creating dual-gate devices. The first dual-gate MOS-gated thyristor specifically designed for improving this three-fold trade-off was the Dual-Gate (DG) BRT [49] whose cross-section is also shown in Fig. 12. This structure is similar in appearance to the BRT but the two gates can be used to operate this structure in both the BRT mode and the IGBT mode. When both gates are biased at a positive potential, the thyristor is turned-on resulting in a low on-state voltage drop. If both gates are simultaneously switched to a negative value, the thyristor is turned-off as in the BRT. However, if only one of the gates is biased at -15 V, the P-channel MOSFET shunts the holes collected by the P-base region preventing latch-up of the thyristor. The device can now operate in the IGBT-mode, if a positive bias is applied to the other gate, with high voltage current saturation. Thus, this structure has all the attributes of the BRT while providing a good FBSOA to perform controlled turn-on and short-circuit protection functions as well. A closely related Dual MOS-Gate thyristor structure has also been reported [50] for enhancing the switching behavior but its FBSOA was not reported.

For applications operating at up to 2500 V, the IGBT has become widely accepted as the best device. However, its ratings have not yet been extended to higher voltages due to the reasons already discussed. For applications in traction (electric street cars and locomotives), the gate Turn-Off (GTO) thyristor is the only commercially available device with the ability to block 4500 V and control over 500 A. The basic structure of the GTO is shown in Fig. 14. In the on-state, the current flows via the thyristor. The turn-off is achieved in this structure by the application of a negative bias to the gate electrode to extract the stored charge within the P-base region [3], [51]. When this charge has been removed, the N^+ emitter/P-base junction becomes reverse biased leading to turn-off. In the GTO, the removal of the stored charge via the gate electrode requires substantial current flow in the gate circuit. It is therefore classified as a current controlled device. The turn-off current gain of the GTO has been analyzed using the storage time for removal of carriers in the P-base region [52]. In order to achieve a higher current gain and maximum controllable current, a variety of structural changes have been reported. The current gain can be improved by reducing the width of the P-base region but this can have an adverse effect on the blocking voltage. The introduction of the P^+ buried region as shown in Fig. 14 is aimed at reducing the resistance of the P-base region during charge extraction so as to enhance the maximum controllable current. In addition, the anode shorted structure with buffer layer has been introduced to reduce the current tail that occurs after turn-off. Unfortunately, this greatly reduces the current gain of the P-N-P transistor which causes an increase in the on-state voltage drop and a reduction in the turn-off gain. After optimization of the GTO structure, it has been found that the maximum turn-off gain is reduced to less than 5.

Due to the limitations in the performance of GTO's, there is considerable interest in the development of high voltage (>2500 V) and high current (>200 A) MOS-gated thyristor structures. The basic structures for these devices was already discussed in context with Fig. 12. The blocking voltage rating for these devices can be increased by using higher resistivity, bulk, neutron transmutation doped silicon as the starting material as commonly used for high power thyristors and GTO's. One of initial concerns with these MOS-gated device structures was that relatively shallow junctions ($<3\,\mu$m deep) are needed to build the DMOS gate structure in contrast with the very deep (100 μm) junctions that are used to obtain high blocking voltages in thyristors and GTO's. Fortunately, it has been proven that the cell structure for the MOS-gated devices is capable of supporting high voltages [53] inspite of the relatively shallow junctions. The essential technological roadblocks that must then be overcome are ensuring a high maximum controllable current density within the device cells and the ability to scale the device to handle the large current levels encountered in the applications. Recent work on MOS-gated thyristors has allowed optimization of the cells to obtain high maximum controllable current densities for devices capable of operating at 600 V [3] but this needs to be scaled to cells capable of high voltage operation.

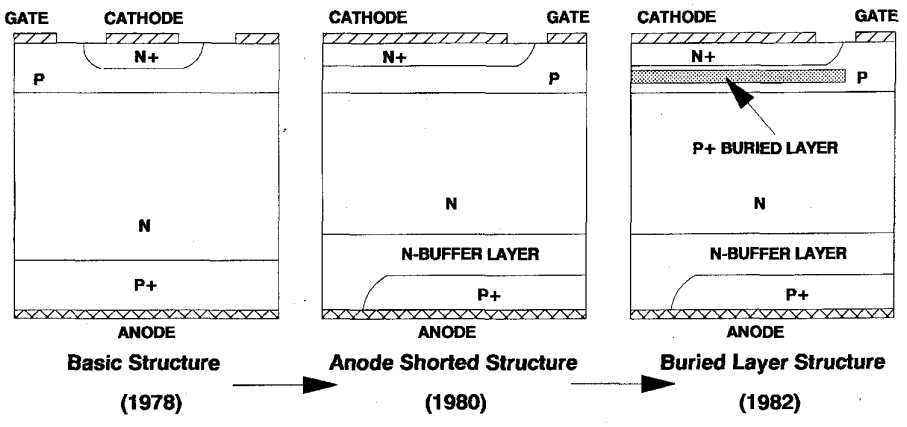

Fig. 14. Evolution of Gate Turn-Off thyristor structures.

The difficulty is scaling the current handling capability is related to the yield limitations of MOS technology. At present, the largest device active area that can be manufactured is about 1 cm^2. Since the on-state current density is limited to less than 100 A/cm^2 from thermal considerations, the yield limits the maximum current handling capability of single devices to less than 100 A. An obvious solution to obtaining higher currents is by paralleling of packaged devices. However, this has been found to be expensive and raises new issues related to uniform current sharing between devices during both steady-state and dynamic operation. For these reasons, wafer repair approaches have been investigated [35], [54], [55] to produce devices with high current ratings. The basic concept consists of partitioning the device into segments with high yield, isolating the defective segments, and utilizing the remaining area for current transport. The first attempt at wafer repair required extensive testing followed by cathode metal definition using a custom mask for each device [35]. This was not considered a cost effective manufacturable technology. In the more recent wafer repair approaches, a fusible link is used to isolate the defective segments without the need for custom masks [54], [55]. These approaches are more cost effective but have not yet been commercially implemented.

IV. Silicon Carbide Power Switches

More than 15 years ago, a fundamental analysis was first performed relating the specific on-resistance of the drift region in semiconductor devices to the breakdown voltage and the basic transport properties [10]. Based upon the electric field profile within the drift region with a uniform doping concentration, it was shown that the specific on-resistance is given by:

$$R_{\text{on,sp(ideal)}} = \frac{4BV^2}{\epsilon_s \mu E_c^3} \tag{1}$$

where BV is the breakdown voltage, ϵ_s is the dielectric constant, μ is the carrier mobility, and E_c is the critical electric field for breakdown. The denominator $(\epsilon_s \mu E_c^3)$ has been referred to as *Baliga's Figure of Merit (BFOM)* which can be used to compare the relative performance of various semiconductor materials for power device fabrication [56], [57]. Using this figure of merit, it has been predicted that GaAs based devices will have 13 fold lower specific resistance for the drift region [10]. On the basis of these projections, vertical channel JFET's and MESFET's were fabricated with breakdown voltages upto 200 V [58], [59].

With the commercial availability of high quality silicon carbide wafers with lightly doped epitaxial layers [60], the fabrication of power devices has become viable. For all three polytypes, a 200 fold smaller specific on-resistance is projected [61]. The first SiC power devices were high voltage Schottky rectifiers as already discussed. The fabrication of power MOSFET's has also been undertaken [62]. Due to the very small diffusion rates for dopants in SiC, it is not practical to fabricate the DMOS structure. The most suitable structure is the UMOSFET in which the P-base region is epitaxial grown on the N-drift layer. The UMOSFET structure also provides a high channel density which is essential to allow taking full advantage of the very low specific on-resistance for the drift region predicted for SiC. It was found that the breakdown voltage of these UMOSFET's was limited to under 100 V due to rupture of the gate oxide. Careful analysis of the electric field distribution within the UMOSFET indicates a high electric field at the corners of the trenches [63]. Further, since the critical electric field for breakdown in SiC is about 2×10^6 V/cm and the electric field in the oxide is about three times that in the underlying semiconductor, the electric field in the oxide can approach its breakdown strength of about 1×10^7 V/cm at the trench corners leading to its rupture. Another problem with the MOSFET structure is that the very low inversion layer mobilities (15 cm^2/V s) reported for this material lead to a severe degradation in the specific on-resistance [65]. This is illustrated in Fig. 9, where the calculated specific on-resistance is given as a function of the breakdown voltage for various inversion layer mobility values. From these plots, it is obvious that SiC UMOSFET's with breakdown voltages below 200 V will not be able to outperform silicon devices. Even in the case of higher breakdown voltages, the performance of SiC MOSFET's is severely degraded by the poor inversion layer mobility. Methods for improving this parameter must be developed to resolve this problem.

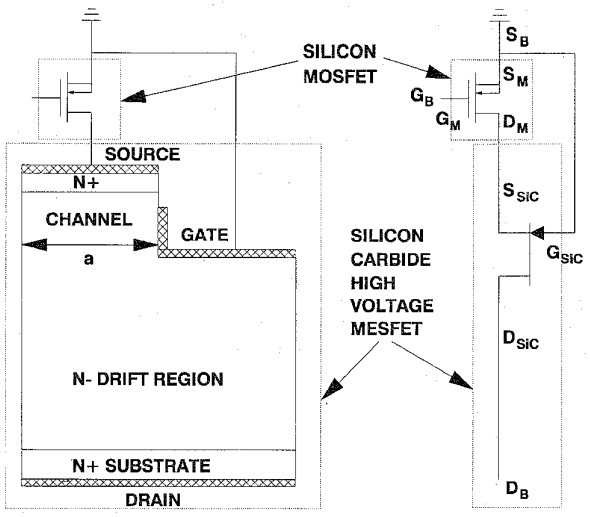

Fig. 15. The *Baliga-Pair device configuration* consisting of a silicon MOSFET and silicon carbide MESFET.

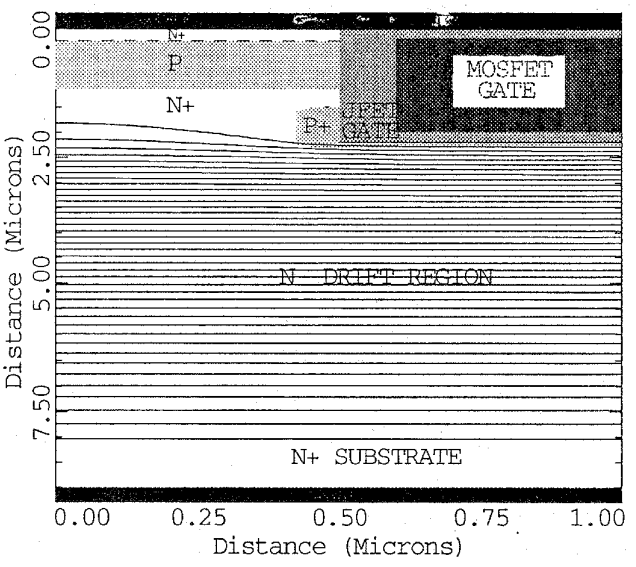

Fig. 16. Potential contours obtained by two-dimensional numerical simulation using a concatenated structure to demonstrate that the applied drain voltage is support mainly by the JFET device. The potential contours are given at every 25 V for a drain bias of 1000 V.

Due to the above problems associated with SiC UMOSFET's, an alternate strategy to take advantage of the low specific resistance of the drift region has been suggested by using a combination of a low breakdown voltage, normally-off, silicon MOSFET and a high breakdown voltage, normally-on SiC MESFET or JFET structure. This approach rivals that used to create the *Darlington bipolar transistor configuration* to enhance the current gain [64]. This configuration of devices, called the *Baliga-Pair* circuit configuration [65,66] is shown in Fig. 15. It consists of a Si power MOSFET connected in series with the source region of a SiC high voltage power MESFET or JFET. Either vertical channel or lateral SiC FET structures can be utilized. It is important to note that the gate region of the SiC MESFET is connected to the reference terminal (or source region of the silicon power MOSFET) and the composite switch is controlled by a signal applied only to the gate of the silicon power MOSFET. The basic operating principles of this switch are discussed below. In order to clarify the various modes of operation, two-dimensional numerical simulations of this configuration were performed by concatenation of a MOSFET with a JFET structure. Although such an integrated structure is desirable, the goal here is to illustrate the modes of operation of the combination and not to suggest that this integration is necessary.

If the half-width "a" of the MESFET channel is designed to be larger than the zero bias depletion width of the MESFET gate structure, the MESFET behaves as a depletion-mode (or normally-on) device structure. When an increasing positive bias is applied to the drain (D_B) of the Baliga-pair with gate (G_B) shorted to the source (S_B), the voltage is initially supported by the silicon MOSFET because the MESFET channel is not depleted. This results in an increase in the potential of the source region S_{SiC} of the SiC MESFET. Since the gate G_{SiC} of the silicon carbide MESFET is at zero potential, this produces a reverse bias across the gate-source junction of the MESFET. As the voltage applied to the drain D_B is increased, this reverse bias produces pinch-off of the MESFET channel by the extension of a depletion region from the gate contact. Once the MESFET channel pinches-off, any further increase in the voltage applied to the drain D_B is supported by the extension of a depletion region in the drift region of the SiC MESFET. The two-dimensional numerical simulations showed that, once the channel is pinched-off, the potential at the drain D_M of the MOSFET remains relatively constant and independent of the voltage applied to the drain D_B of the composite switch. Most of the voltage is then sustained by the drift region of the JFET. This can be clearly seen in Fig. 16, where the potential contours are plotted at a drain D_B bias of 1000 V for intervals of 25 V demonstrating that all the potential contours are within the drift region of the JFET. From this figure, it can also be concluded that the potential supported by the MOSFET is less than 25 V because the JFET channel pinch-off voltage is less than this value. This implies that a silicon power MOSFET with relatively low breakdown voltage (<50 V) can be used in conjunction with a high voltage silicon carbide MESFET to form the Baliga-pair. This is important from the point of view of obtaining a low total on-state voltage drop for the composite switch.

In order to turn-on the Baliga-pair, a positive gate bias is applied to the gate G_M of the silicon power MOSFET, which also serves as the gate G_B of the composite switch. This switches the silicon MOSFET to its highly conductive state. When a positive voltage is applied to the drain D_B, current can now flow through the undepleted MESFET channel and the silicon MOSFET. The current flowlines obtained with the simulations of the concatenated structure are shown in Fig. 17. From this figure, it can be clearly seen that the current is transported via the channel of the MOSFET and the JFET, followed by a very uniform distribution within the drift region of the JFET. This excellent current distribution results in the specific on-resistance of the SiC MESFET being very close

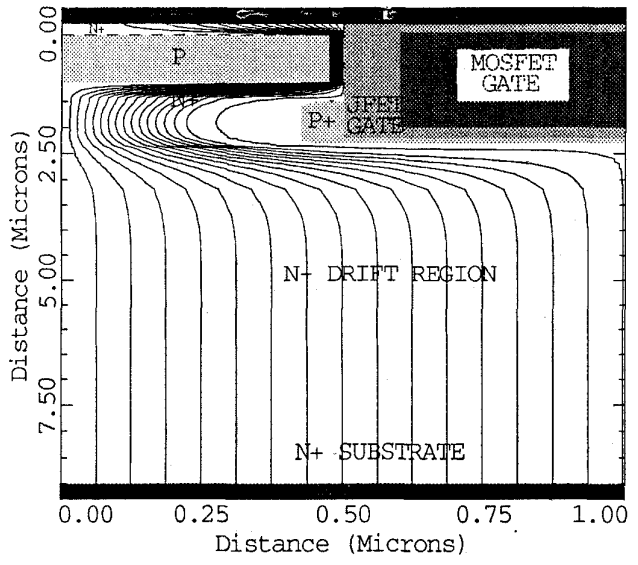

Fig. 17. Current flow lines at obtained by two-dimensional numerical simulation using a concatenated structure to demonstrate that the current is uniformly distributed in the drift region of the JFET device. The on-state current density is 100 A/cm^2 with a gate bias of 15 V applied to the MOSFET.

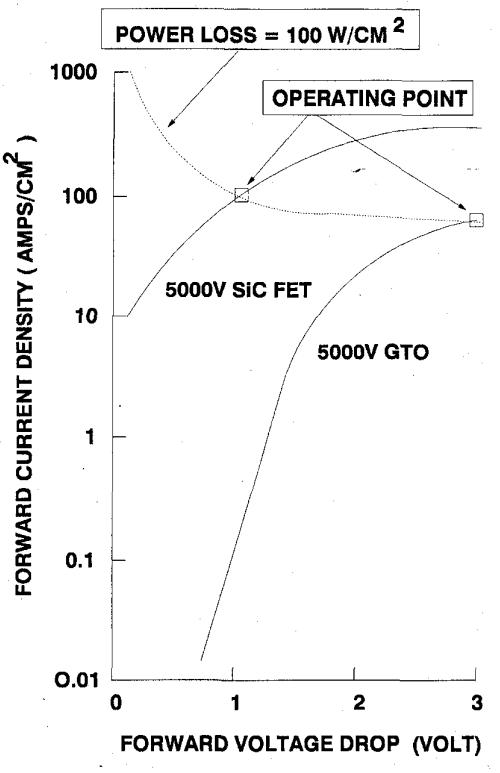

Fig. 18. Comparison of the forward I-V characteristics of the 5 kV silicon carbide FET with that for the 5 kV GTO.

to the ideal specific on-resistance for the drift region. The resistance contribution from the MESFET channel increases the specific on-resistance by less than 25 percent because the current is transported in the bulk and not along a surface. Thus, the Baliga-pair is projected to have on-state voltage drop of only 0.1 V when the SiC MESFET is designed to block up to 1000 V.

The Baliga-pair has several other important attributes. The first is an excellent forward biased safe operating area. This is achieved by simply reducing the gate bias applied to the switch until it approaches the threshold voltage for the silicon power MOSFET. In this case, when a voltage is applied to the drain D_B, the MOSFET operates in its current saturation regime. This limits the current flowing through the composite switch. When the voltage applied to the drain D_B is increased, the voltage across the MOSFET increases until the channel of the MESFET is pinched-off allowing high voltages to be sustained with a current flow dictated by the MOSFET channel. Numerical simulations indicate a square FBSOA for the Baliga-pair because no minority carrier transport is involved. The absence of minority carrier transport in the Baliga-pair is also important in obtaining a high switching speed. Since both the silicon MOSFET and the silicon carbide MESFET are unipolar devices, the turn-off time for the composite switch is determined by the charging and discharging time constants for the silicon MOSFET. Well optimized silicon power MOSFET's can be designed at the required low breakdown voltages resulting in a very high switching speed for the Baliga-pair. This is attractive for the reduction of power losses in medium/high voltage power electronic systems operating at high frequencies.

Another attribute of the Baliga-pair is that it incorporates an excellent integral fly-back diode. In the case of the silicon power MOSFET, the junction between the P-base region and the N-drift region can be utilized as a reverse conducting (fly-back) diode. However, this diode operates with the injection of minority carriers into the drift region which compromises the switching speed and power losses in the devices. In the case of the SiC MOSFET structure, there is an additional disadvantage that the potential required for the injection of minority carriers is much larger (typically 3 V) when compared with silicon (typically 1 volt) due to its larger energy band gap. This results in a severe increase in the power losses for the flyback rectifier. In contrast to this, in the case of the Baliga-pair, the application of a negative bias to the drain D_B forward biases the Schottky barrier gate structure in the case of a SiC MESFET. The SiC Schottky barrier rectifier has been demonstrated to have excellent on-state and switching characteristics because it is a unipolar device. Thus, the Baliga-pair also contains an excellent flyback diode if implemented by using a high voltage SiC MESFET structure.

Recently, a relationship for the specific on-resistance of a lateral FET operating with the RESURF principle has been derived [65]:

$$R_{\mathrm{on,sp(ideal)}} = \frac{BV^2}{\epsilon_s \mu E_c^3}. \tag{2}$$

From this expression, it can be seen that the figure of merit for lateral FET's is identical to that for the vertical FET's. However, in comparison with the specific on-resistance for a vertical FET given by (1), it can be seen that the lateral device is 4 times better. This has motivated the development of high voltage lateral MESFET's and JFET. Among silicon carbide

FET's, the highest blocking voltage reported until now is a 450 V lateral substrate gate JFET structure [68].

Based upon above discussion, it is recommended that high performance MESFET's be developed from SiC to enable exploitation of the low projected specific on-resistance of the drift region for these devices. If the problems with the SiC UMOSFET structure are overcome, it would be preferable to utilize this device because of the simplification in packaging. In either case, these developments are expected to impact all power electronics applications with operating voltages above 100 V. The theoretical calculated [58] on-state characteristic of a 5000 V SiC FET is compared with that of a state-of-the-art GTO in Fig. 18. It can be seen that the SiC FET has a lower forward voltage drop than the GTO for the same on-state power loss. Thus, it can be concluded that the SiC FET's have the potential to displace all silicon devices with voltage ratings above 100 V.

V. Conclusions

In this review paper, the trends in the development of power rectifiers and switches with improved electrical characteristics have been discussed with emphasis on the MOS based technology. The advent of MOS-gate structures, in particular the power MOSFET and IGBT, has led to a revolutionary (sometimes referred to as the *second electronic revolution*) changes in the way power electronic systems are designed because of the ability to integrate the drive circuits for the power devices. The resulting reductions in size and weight of systems has enabled greater market penetration. With gains in operating frequency achieved by reducing device switching losses, operation at above 10 kHz has enabled reduction of acoustic noise is consumer power electronic systems, such as adjustable speed motor control for heating, ventilating and air-conditioning [67].

The future portends significant further improvements in the performance of power devices by the replacement of silicon with silicon carbide. Much improved high voltage power rectifiers have already been experimentally demonstrated from silicon carbide and a vigorous effort is underway in the research community to create power switches from this material. Thus, a clear roadmap exists for making advances in power device performance into the twenty-first century, which will reflect in superior power electronic systems for consumer and industrial applications.

Acknowledgment

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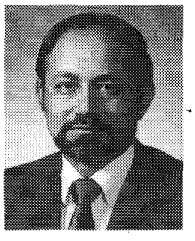

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