A New Vertical Power MOSFET Structure with Extremely Reduced On-Resistance

DAISUKE UEDA, HIROMITSU TAKAGI, AND GOTA KANO

Abstract—A new vertical power MOSFET structure called rectangular-grooved MOSFET (RMOS) is proposed, in which the vertical channels are provided along the sidewalls of the rectangular grooves formed by a reactive ion-beam etching (RIBE) technique. The structure is characterized by reduced ON-resistance and high packing density. The relationship between the ON-resistance and the packing density in the new structure is calculated. It is demonstrated that the structure essentially possesses a lower ON-resistance per unit area than VMOS and DMOS structures. Experimental results are also described in detail.

I. Introduction

POWER MOSFET's are attracting much attention from circuit designers for a variety of power applications. Their inherent characteristics include fast switching response, high input impedance, and high thermal stability [1], [2]. The major disadvantage of the power MOSFET's is their large voltage drop when compared to bipolar transistors. Although many efforts [3], [4] have been made to reduce the ON-resistance per unit area for conventional VMOS and DMOS structures, few significant improvements have been made.

In this paper, a new vertical power MOSFET structure is proposed that permits significant reduction of the ON-resistance per unit area in the low breakdown voltage range. The main feature of this new structure is the location of the channel along the sidewalls of rectangular grooves formed by a reactive ion-beam etching (RIBE) technique [5]. The device is called a rectangular-grooved MOSFET (RMOSFET). The RMOS transistor design concept is presented, and the resulting ON-resistance is compared with that of conventional VMOS and DMOS structures. An experimental device having an ON-resistance of 50 mΩ and a breakdown voltage of 50 V was fabricated on a 3.5 mm × 3.5 mm chip.

II. RMOS Structure and Technology

It has been shown that the ON-resistance of vertical power MOSFET's with high source-to-drain breakdown voltage is predominantly determind by the resistance of the lightly doped epitaxial drain region [6]. In low breakdown voltage devices, the ON-resistance is dominated by the channel region resistance, not that of the drain region.

This paper proposes a new vertical power MOSFET structure with rectangular grooves for reducing the resistance of the channel region. A cross section of the structure is shown in Fig. 1. The channels of the RMOS transistor are formed along the vertical walls of rectangular grooves that penetrates into the n^- buffer region through n^+ source and p-body regions. The channel length is shorter and packing density is higher than that of conventional VMOS and DMOS structures. As a result the channel resistance per unit area is lower than in previous devices.

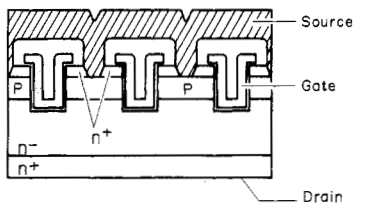

Fig. 1. Cross section of the RMOSFET structure.

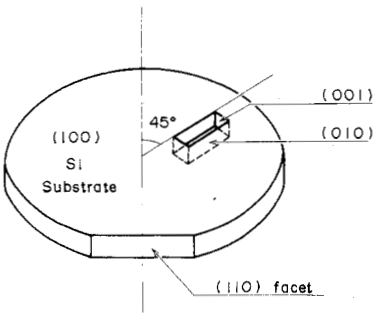

Fig. 2. A diagram of the formation of rectangular groove with (100) sidewall planes.

A reactive ion-beam etching (RIBE) technique is employed to form the rectangular grooves, since it permits anisotropic etching regardless of the crystallographic orientation [7]. The (100) sidewall plane, which has the highest surface electron mobility, is obtainable by orienting the rectangular groove 45° away from the (110) axis of a (100) wafer, as illustrated in Fig. 2. This increased electron mobility is another advantage that the RMOS structure has over conventional nonplanar vertical power MOSFET structures.

The processing steps for RMOSFET fabrication are shown in Fig. 3.

Step 1 p-body and n^+ source regions are diffused into an n^--n^+ epitaxial wafer.

Step 2 Rectangular grooves are formed using a RIBE technique.

Step 3 Slight wet etching is subsequently applied to obtain a smooth surface on the sidewalls of the groove.

Step 4 After the gate oxide is grown, a polysilicon layer is

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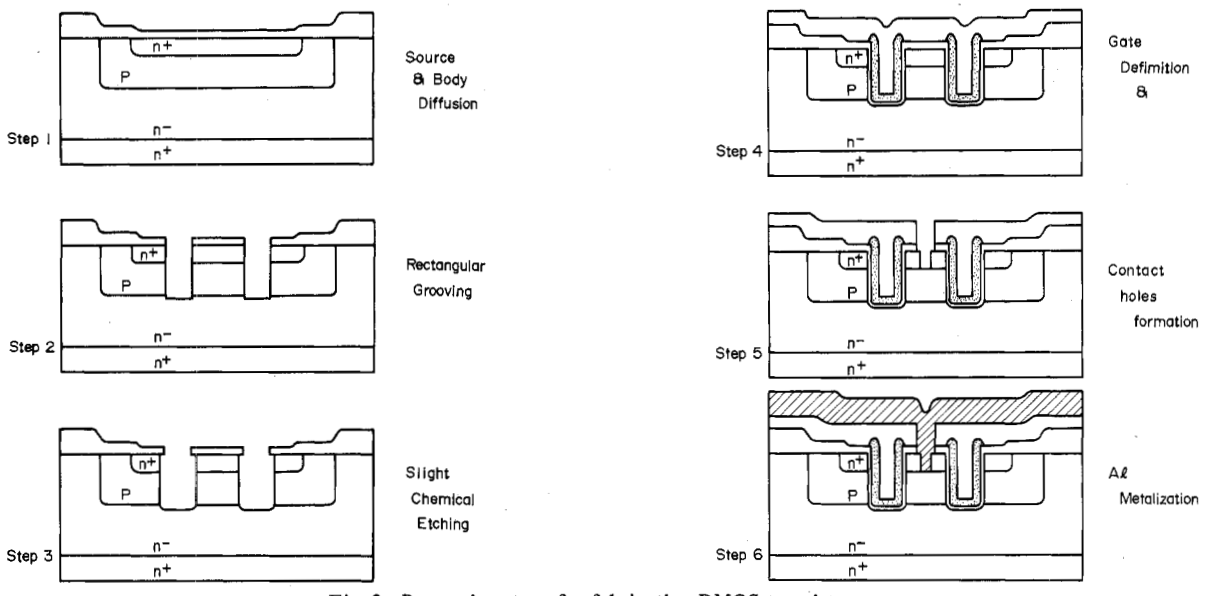


Fig. 3. Processing steps for fabricating RMOS transistors.

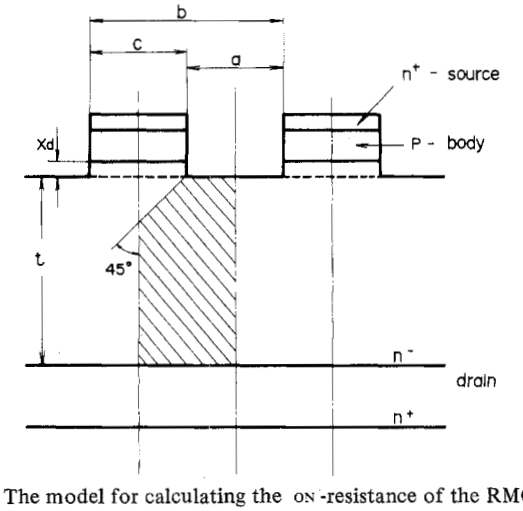


Fig. 4. The model for calculating the ON-resistance of the RMOSFET.

deposited for the gate conductor, and then a phosphosilicate glass film is deposited.

Step 5 The source oxide layer and a portion of the source are sequentially etched away to simultaneously form contact holes to the n^+ source and p-body regions [8].

Step 6 After depositing an aluminum film, source and gate electrodes are defined.

III. ON-Resistance

An ON-resistance of the vertical power MOSFET is the sum of the channel resistance (R_{ch}) and the resistance of epitaxial drain-buffer region (R_{epi}) as

$$R_{ON} = R_{ch} + R_{epi}. \tag{1}$$

Fig. 4 is a schematic drawing which is used for the calculation of the ON-resistance. The ON-resistance design considered is concerning the unit active area of the device. Use of the well-known formula for the channel resistance gives

$$R_{ch} = \frac{L_g}{W_g} \cdot \frac{1}{\mu_n \epsilon_{si}} \cdot \frac{T_{ox}}{V_G - V_T} \tag{2}$$

where

L_g is the gate length,
W_g is the total gate width,
μ_n is the surface electron mobility,
ϵ_{si} is the permittivity of silicon,
T_{ox} is the gate oxide thickness,
V_G is the applied gate voltage, and
V_T is the threshold voltage.

Assuming that the structure is an interdigitated design with a finger pitch b, the total gate width per unit area W_g is given by

$$W_g = \frac{2}{b}. \tag{3}$$

Assuming uniform carrier flow from the accumulation layer formed under the gate-drain overlap to the n^+ drain region shown by the hatched pentagonal area in Fig. 4, the formula for R_{epi} is obtained by the resistance integration in the above region. The resultant formula is

$$R_{epi} = \begin{cases} \rho \cdot \left(\frac{b}{2} \log \frac{b}{a} + t - \frac{b-a}{2} \right), & \left(t > \frac{b-a}{2} \right) \quad (4a) \\ \rho \cdot \left(\frac{b}{2} \log \frac{b}{a} \right), & \left(t \leq \frac{b-a}{2} \right) \quad (4b) \end{cases}$$

where ρ and t are the resistivity and the thickness of the lightly doped drain region, respectively, and a is the length of the gate-drain overlap. Note that (4a) and (4b) correspond to two cases with and without the overlap of the current fluxes between the adjacent grooves, respectively.

For the numerical calculation of (2) we assume [9] the

maximum electric field in the gate oxide as

$$\frac{V_G - V_T}{T_{ox}} = 2 \times 10^6 \quad \text{(V/cm)}. \tag{5}$$

As for the gate length L_g, we now consider a case where the channel resistance becomes minimum. This case occurs when the breakdown voltage BV_{DSS} equals the punchthrough voltage V_p. Assuming a uniform donor distribution in the n^- drain buffer region and a linear acceptor profile in the p-body region, the punchthrough voltage V_p is calculated by solving the one-dimensional Poisson's equation as [10]

$$BV_{DSS} = V_p = x_{jp}^2 \cdot \frac{q}{\epsilon_{si}} \left(\frac{N_{A\max}}{6} + \frac{N_{A\max}^2}{8N_D} \right) \tag{6}$$

where

- x_{jp} is the diffusion length of the p-body region,
- q is the charge of an electron,
- $N_{A\max}$ is the maximum acceptor density of the p-body region, and
- N_D is the donor density of the epitaxial region.

For the RMOS structure, $x_{jp_{\min}}$ is equal to $L_{g_{\min}}$. Substitution of $x_{jp} = L_{g_{\min}}$ into (6) yields

$$L_{g_{\min}} = \sqrt{\frac{\epsilon_{si}\, BV_{DSS}}{q\left(\frac{N_{A\max}}{6} + \frac{N_{A\max}^2}{8N_D} \right)}}. \tag{7}$$

For the numerical calculation, 5×10^6 atoms/cm^3 is used for $N_{A\max}$ that determines the threshold voltage of the device [10].

R_{epi} of (3) is calculated on the assumption that the epitaxial layer has the ideal resistivity and thickness to meet the theoretical breakdown voltage [11]. Then

$$\rho = \frac{2BV_{DSS}}{\mu_{nb}\, \epsilon_{si}\, E_C^2} \tag{8}$$

and

$$t = \frac{2BV_{DSS}}{E_C} \tag{9}$$

where E_C is the electric field at which the avalanche breakdown occurs and μ_{nb} is the bulk electron mobility in the drain region. Substitution of (8) and (9) into (3) provides a formula for R_{epi} as a function of the breakdown voltage BV_{DSS}. For numerical calculations, values of 3×10^5 V/cm and 1500 cm^2/V · s for E_C and μ_{nb} [11] were used.

Fig. 5 shows the calculated results of the R_{ch} and R_{epi} as a function of the breakdown voltage BV_{DSS} for different values of b. This figure demonstrates that the ON-resistance is dominated by R_{ch} for low values of BV_{DSS} and R_{epi} for high values of BV_{DSS}. Consequently, the higher packing density, which is the main feature of the RMOSFET, makes possible the lower ON-resistance obtainable in the low breakdown voltage region.

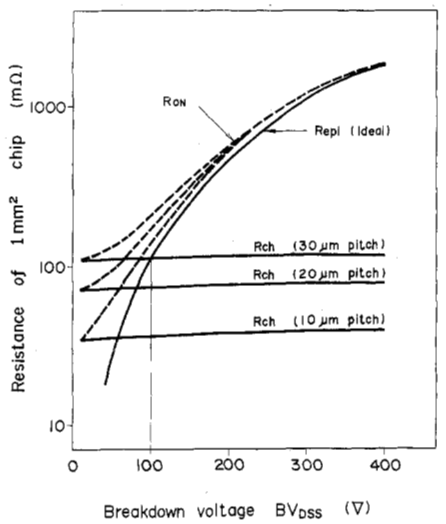


Fig. 5. Calculated results of R_{ch} and R_{epi} versus BV_{DSS} for three different pitches b.

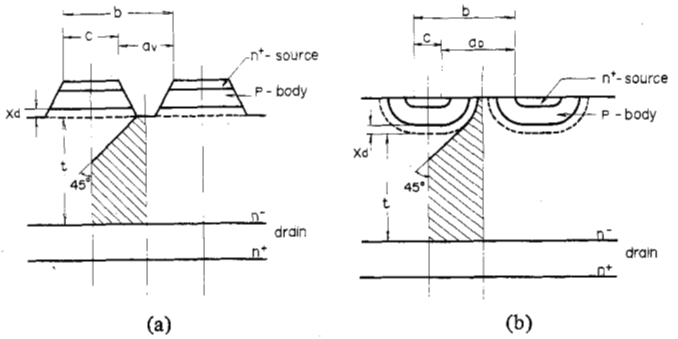


Fig. 6. Models for calculating the ON-resistance of (a) VMOS, and (b) DMOS structures.

IV. Comparison with Other Vertical MOS Structures

Fig. 6 shows the models used to calculate the ON-resistance of VMOS and DMOS structures. Calculations were performed as described in the previous section. These three structures are compared in terms of the ON-resistance per unit area. Table I lists the formulas and parameters used to calculate R_{ch} and R_{epi} of the VMOS, DMOS, and RMOS structures. Note that the parasitic JFET resistance R_{JFET} and the nonbias depletion widening x_d are taken into consideration for the DMOS and VMOS structures.

In Fig. 7, calculated results of the ON-resistance per unit area shown as a function of the pitch b for three structures. The results are summarized as follows.

1) The RMOS structure has the lowest ON-resistance over the whole range of the pitch b among the three structures.

2) The minimum points appear in R_{ON} versus b curves for all structures.

3) The smallest b is found in the RMOS structure.

The principal reason for 1) is that the RMOS structure has the lowest channel resistance due to its short channel length and the highest electron mobility of the (100) crystal. In addition, the gate-drain overlap area a of Fig. 6 is largest in the

TABLE I
FORMULAS AND PARAMETERS USED IN NUMERICAL COMPARISON OF ON-RESISTANCE AMONG VMOS, DMOS, AND RMOS STRUCTURES PER UNIT AREA

	VMOS	DMOS	RMOS
R_{ch}	$\frac{b \cdot Lg}{2} \cdot \frac{1}{\mu_n \varepsilon_{si}} \cdot \frac{T_{ox}}{V_G - V_T}$		
Lg	$\sqrt{\frac{3}{2}}\, x_{jp}$	x_{jp}	x_{jp}
x_{jp}	2.5 (μm)		
$\frac{V_G - V_T}{T_{ox}}$	2×10^6 (V/cm)		
μ_n	450	550	500 ~ 550 (cm^2/V.S)
Repi	$\rho\left(\frac{b}{2}\log\frac{b}{a} + t - \frac{b-a}{2}\right) : t > \frac{b-a}{2}$ $\rho \cdot \frac{b}{2}\log\frac{b}{a} : t \leq \frac{b-a}{2}$		
a	$a \Leftarrow a-\sqrt{2}(x_{jp}+x_d)$	$a \Leftarrow a-\sqrt{2}(x_{jp}+x_d)$	$a \Leftarrow a$
x_d	1.0 (μm)		
ρ	1.0 (Ω . cm)		
t	10 (μm)		
R_{JFET}	0		0
	$\frac{\tan^{-1}\left(\frac{\pi}{8} \cdot \sqrt{\frac{a + 2(x_d + x_{jp})}{a - 2(x_d + x_{jp})}}\right)}{\sqrt{a^2 - 4(x_{jp} + x_d)^2}} - \frac{\pi}{4}$		
b_{min}	$b_3 = c+2(x_{jp}+x_d)$	$b_2 = c+\sqrt{2}(x_{jp}+x_d)$	$b_1 = c$
W_{gmax}	$1/b_3$	$1/b_2$	$1/b_1$
c	8 (μm)		

RMOS structure, so that the R_{epi} becomes smallest among three structures.

The reason for 2) is that confinement of the current flow [12] under the gate-drain overlap region occurs when the pitch b becomes sufficiently small.

The reason for 3) is that the new structure possesses the highest packing density because the sidewall channels are formed perpendicular to the substrate.

V. EXPERIMENTAL RESULTS

This new vertical power MOSFET structure was fabricated on n^--n^+ epitaxial wafers. The thickness and the resistivity of the epitaxial layer were 10 μm and 1 $\Omega \cdot$ cm. A dose of 7×10^{13} boron atoms/cm^2 and 2×10^{15} arsenic atoms/cm^2 were implanted and annealed. Junction depths of 3.0 and 0.4 μm for the p-body and n^+ source regions were obtained (Step 1). The rectangular grooves with a depth of 3.5 μm were formed by RIBE using a gas mixture of $CF_4 + O_2$ with 1.2 kV of acceleration and a chamber pressure of 8×10^{-5} torr (Step 2). Slight wet chemical etching was applied to remove the damaged and contaminated surface of the groove (Step 3). After a gate oxide of 1000 Å was thermally grown, a polysilicon layer with a thickness of 5000 Å was deposited using a LPCVD technique. A phosphosilicate glass with 8-percent phosphorus was deposited and annealed in $H_2 + O_2$ at 1000°C (Step 4). Contact windows were opened by RIBE using the same mixed gas with an acceleration voltage of 800 V and a chamber pressure of 1×10^{-4} torr. Etching of the n^+ source region was then performed making contact to the p-body region simultaneously with the same RIBE conditions used to etch the rectangular grooves (Step 5). A sputtered Al-Si-Cu ternary alloy was used for source and gate electrodes (Step 6).

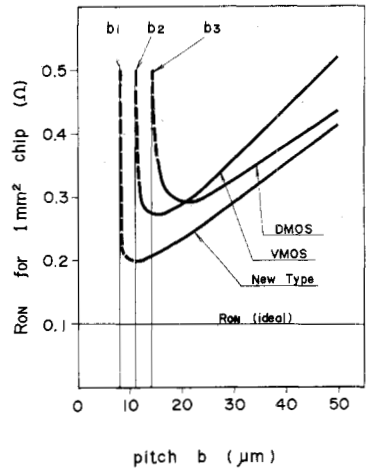


Fig. 7. Calculated result of ON-resistance as a function of pitch b for the three structures from formulas and values listed in Table I.

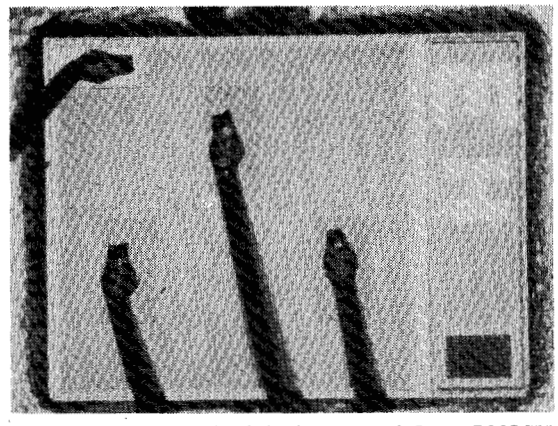


Fig. 8. Photomicrograph of the 3.5 mm × 3.5 mm RMOSFET.

A photograph of the chip pattern is shown in Fig. 8. A cross sectional view of the fabricated device is shown in Fig. 9.

The experimentally fabricated RMOSFET has a total gate width of 140 cm and the groove pitch of 14 μm on a 3.5 mm × 3.5 mm chip with cross-striped rectangular grooves.

In Fig. 10, typical I-V characteristics are shown. An ON-resistance of 50 mΩ is obtained for a gate voltage of 20 V. In Fig. 11, the 50-V hard breakdown is observed, which implies no damage and no contamination during above processes. This 50 mΩ/3.5 mm × 3.5 mm/50 V chip represents the best performance for the various types of vertical power MOSFET's so far developed.

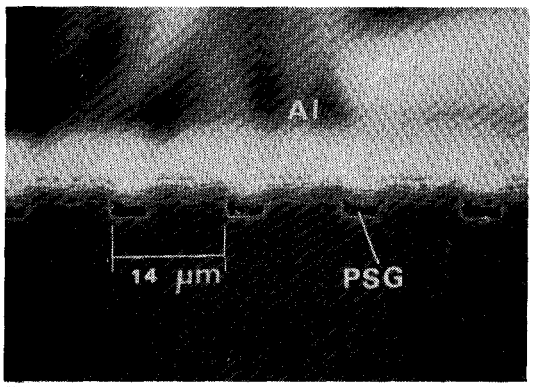
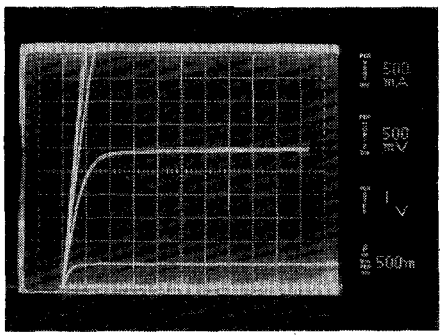
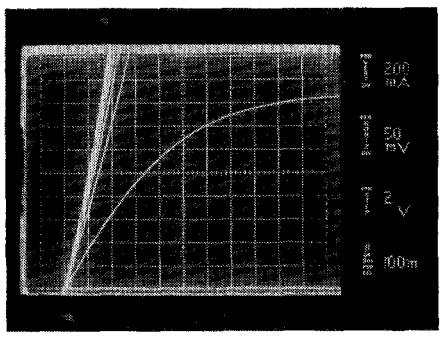


Fig. 9. SEM photomicrograph of the cross section of the fabricated RMOSFET.



(a)



(b)

Fig. 10. Typical *I-V* characteristics of RMOSFET devices with 3.5 mm × 3.5 mm chip area. (a) ON-characteristics of RMOSFET, and (b) ON-resistance characteristics of RMOSFET.

Further reduction of the ON-resistance could be expected, since deeper etching reduces the current confinement beneath the groove.

VI. Conclusion

A new vertical power MOSFET with rectangular grooves has been demonstrated. The new RMOSFET features low ON-resistance characteristics resulting from its shorter channel length, higher electron mobility, and higher packing density when compared to conventional VMOS and DMOS FET's. For low breakdown voltage devices, the ON-resistance improvement that is obtained is significant.

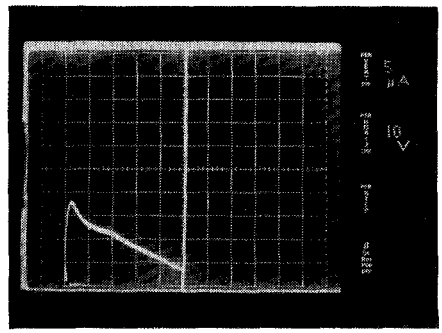


Fig. 11. Typical breakdown characteristics of the RMOSFET.

An experimentally fabricated device showed an ON-resistance of 50 mΩ with 50-V source-to-drain breakdown voltage with 15-μm groove pitch on a 3.5 mm × 3.5 mm chip.

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