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Review

Bulk and epitaxial growth of silicon carbide

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Abstract

Silicon carbide (SiC) is a wide bandgap semiconductor having high critical electric field strength, making it especially attractive for high-power and high-temperature devices. Recent development of SiC devices relies on rapid progress in bulk and epitaxial growth technology of high-quality SiC crystals. At present, the standard technique for SiC bulk growth is the seeded sublimation method. In spite of difficulties in the growth at very high temperature above 2300 °C, 150-mm-diameter SiC wafers are currently produced. Through extensive growth simulation studies and minimizing thermal stress during sublimation growth, the dislocation density of SiC wafers has been reduced to 3000–5000 cm^{-2} or lower. Homoepitaxial growth of SiC by chemical vapor deposition has shown remarkable progress, with polytype replication and wide range control of doping densities (10^{14}–10^{19} cm^{-3}) in both n- and p-type materials, which was achieved using step-flow growth and controlling the C/Si ratio, respectively. Types and structures of major extended and point defects in SiC epitaxial layers have been investigated, and basic phenomena of defect generation and reduction during SiC epitaxy have been clarified. In this paper, the fundamental aspects and technological developments involved in SiC bulk and homoepitaxial growth are reviewed.

Keywords: silicon carbide; sublimation; chemical vapor deposition; impurity doping; extended defect; deep level

1. Introduction

Silicon carbide (SiC) is a IV-IV compound material with unique physical and chemical properties. The strong chemical bonding between Si and C atoms (4.6 eV) gives this material very high hardness and chemical inertness. Due to the strong bonding, the bandgap of SiC is large, 2.3–3.3 eV, depending on the crystal structure, or polytype. This material exhibits about ten times higher critical (breakdown) electric field strength and three times higher thermal conductivity than silicon (Si), making it especially attractive for high-power and high-temperature electronic devices [1–4]. For example, the on-state resistance of SiC power devices is orders-of-magnitude lower than that of silicon devices at a given blocking voltage, leading to much higher efficiency in electric power conversion. The wide bandgap and high thermal stability make it possible to operate certain types of SiC devices at junction temperatures of 300 °C or higher for indefinite periods without degradation. Among various wide bandgap semiconductors, SiC is exceptional because it can be easily doped to produce either p-type or n-type over a wide range. In addition, SiC is the only compound semiconductor whose native oxide is SiO_2. This makes it possible to fabricate the entire family of metal-oxide-semiconductor (MOS)-based electronic devices in SiC such as metal-oxide-semiconductor field effect transistors (MOSFETs).

In recent years, remarkable effects in energy saving by using SiC power devices (Schottky barrier diodes and power MOSFETs) have been demonstrated in air conditioners, photovoltaic converters, industrial motor control,

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railcars, etc. Recent progress in SiC electronic devices is presented in Refs. [5,6]. The physical and chemical stability of SiC, however, had made growth of large and high-quality SiC crystals extremely difficult and severely hampered development of SiC semiconductor devices. The existence of various SiC structures with different stacking sequences (known as polytypism) [7] has also been the major challenge in growth of electronic-grade SiC crystals.

This paper reviews fundamentals, current status, and future challenges of SiC bulk and epitaxial growth. Growth kinetics, techniques, impurity doping, and defects in SiC crystal growth are described.

2. Crystal structures and polytypism of SiC

In SiC, both Si and C atoms are tetrahedrally bonded with covalent bonds by sharing electron pairs in sp^3–hybrid orbitals to form a SiC crystal. The tetrahedra (or Si–C pairs) can occupy three different positions referred to as A, B, and C with each layer containing only tetrahedra in one position. In SiC, there exist over 200 known stacking structures called "polytypes" [7]. The structures of three major SiC polytypes are schematically shown in Fig. 1. In Ramsdell's notation, polytypes are represented by the number of Si–C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal, and R for rhombohedral). 3C-SiC (zincblende) is often called β-SiC, and other polytypes are referred to as α-SiC.

It is still not fully understood why so many SiC polytypes exist. In general, crystals with strong covalent bonding crystallize in the zincblende structure, while the wurtzite structure is more stable for crystals with high ionicity. The intermediate ionicity of SiC (11% according to Pauling's definition) may be a possible reason for the occurrence of SiC polytypism [8,9]. The *ab initio* calculations of the polytype energies indicate that the bulk energy differences among different SiC polytypes are extremely small, below 1 meV/atom [10,11]. The stability and nucleation probability of SiC polytypes strongly depend on temperature [12]. For example, 3C-SiC is not stable, and is transformed into hexagonal SiC polytypes such as 6H-SiC at high temperatures above 1900–2000 °C [13]. This instability of 3C-SiC makes it difficult to grow large 3C-SiC ingots at a reasonable growth rate. 2H-SiC (wurtzite) is also unstable at high temperature, and large 2H-SiC crystals have not been obtained. Thus, 4H-SiC and 6H-SiC polytypes are popular, and have been extensively investigated to date. 3C-SiC is another popular polytype because 3C-SiC can be heteroepitaxially grown on Si substrates.

Because all SiC polytypes consist of similar Si–C bonds, mechanical and thermal properties such as hardness and thermal conductivity are very similar among different SiC polytypes [1,14]. However, different electronic potentials in different SiC polytypes result in very different electronic band structures and thus significant variation in optical and electronic properties. This means that, for device applications, it is crucial to grow only the single

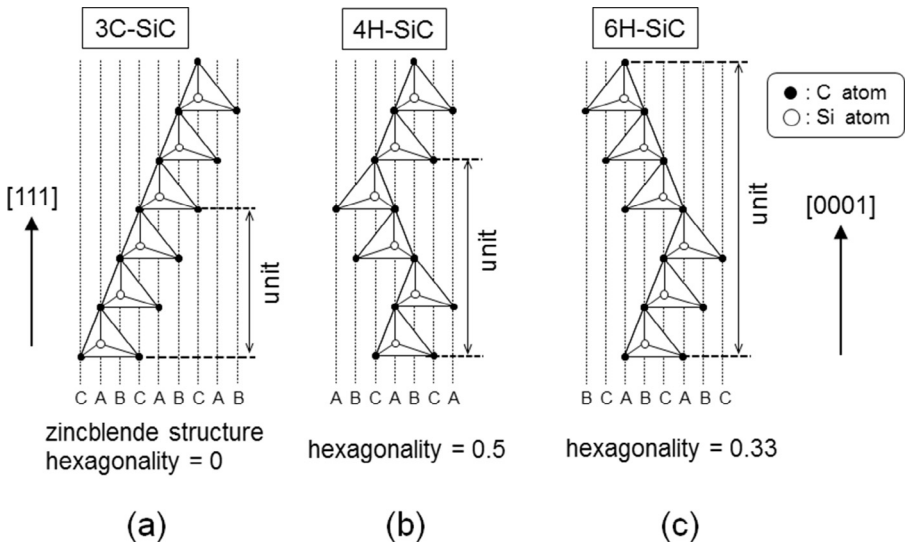

Fig. 1. Stacking sequences of 3C, 4H and 6H polytypes of SiC. The letters A, B, and C denote the three possible positions of a closely-packed structure. Open and closed circles show Si and C atoms, respectively.

desired SiC polytype; polytype control is a vital aspect in crystal growth of SiC.

For high-power and other electronic device applications, 4H-SiC exhibits a significantly higher figure of merit (theoretical potential) than other SiC polytypes, owing to the high critical electric field strength and high electron mobility along the *c*-axis. This is the main reason why 4H-SiC has been almost exclusively employed for power device applications [15–20]. Furthermore, the availability of single-crystalline 4H-SiC{0001} wafers with large diameters and reasonable quality has driven fabrication of 4H-SiC-based electronic devices.

3. Bulk growth of silicon carbide

3.1. Fundamentals

At present, the standard technique for SiC bulk growth is the seeded sublimation (or modified Lely) method [21–23]. However, a few alternative growth techniques have been intensively developed.

Fig. 2 shows the phase diagram of the Si–C binary system [24,25]. Because there exists no stoichiometric SiC liquid phase, it is impossible to employ congruent melt growth for SiC bulk growth at technically relevant system pressures. Instead, SiC sublimes at high temperatures above

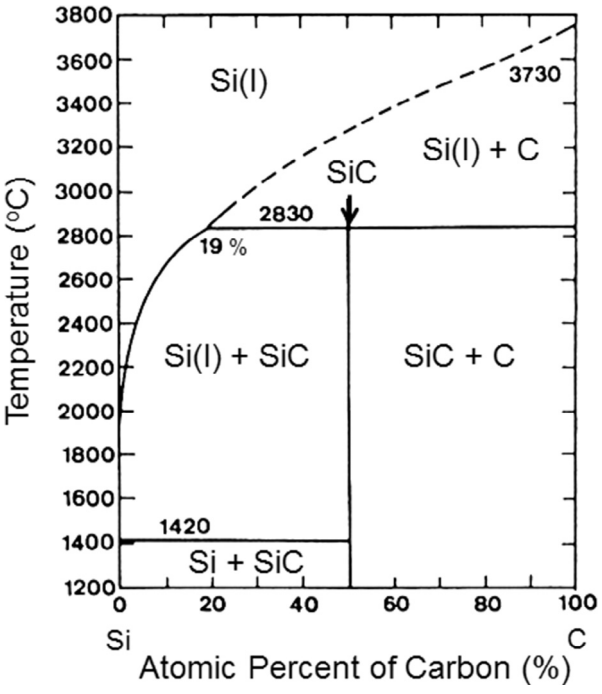

Fig. 2. Phase diagram of the Si–C binary system [24,25]. There exists no stoichiometric liquid phase.

1800–2000 °C. This is the key process of source supply in sublimation growth of SiC. The phase diagram indicates that up to 15% of carbon can be dissolved in a Si melt at about 2800 °C.

Sublimation growth of SiC consists of three steps: (1) sublimation of the SiC source, (2) mass transport of sublimed species, and (3) surface reaction and crystallization. Thus, this growth method is also called "physical vapor transport (PVT)" growth. Fig. 3 plots the partial pressures of sublimed species from (a) SiC + C and (b) SiC + Si systems at high temperature [26,27]. In the gas phase, the dominant species are not stoichiometric SiC molecules, but Si_2C and SiC_2 molecules and atomic Si.

3.2. Sublimation growth

3.2.1. Basic phenomena occurring during sublimation growth

Fig. 4 shows a schematic illustration of a crucible used for seeded sublimation growth of SiC [28–30]. The SiC source (SiC powder or sintered polycrystalline SiC) is placed at the bottom of a cylindrical dense graphite crucible, and a SiC seed crystal is placed near the lid of the crucible. The distance between the top of the SiC source and the seed crystal is typically 20–40 mm. The crucible is heated by radio frequency (rf) induction or resistive heating up to 2300–2400 °C. The crucible is thermally insulated by porous graphite. The seed temperature is fixed at about 50–100 °C lower than the source temperature, so that sublimed SiC species condense and crystallize on the seed. Growth is usually performed at low pressure to enhance the mass transport from the source to the seed. A high-purity Ar (or He) flow is employed for growth.

The growth rate in sublimation growth is mainly determined by the flux of the source supply (sublimation rate) and the transport efficiency from the source to the seed. Here, the sublimation rate is a function of the source temperature, while the transport efficiency strongly depends on the growth pressure, the temperature gradient, and the distance between the source and the seed. Because the mass transport is diffusion limited in sublimation growth, the growth rate is almost inversely proportional to the growth pressure. Here, the concentration gradient is basically determined by the source and seed temperatures (temperature gradient). Any fluctuations in the temperature profile and pressure can result in constitutional supercooling (e.g. Si droplet formation), surface graphitization, and C inclusions. All these phenomena lead to formation of macro- and micro-defects in SiC boules. Understanding of thermodynamic phenomena during sublimation growth has rapidly been updated [31,32].

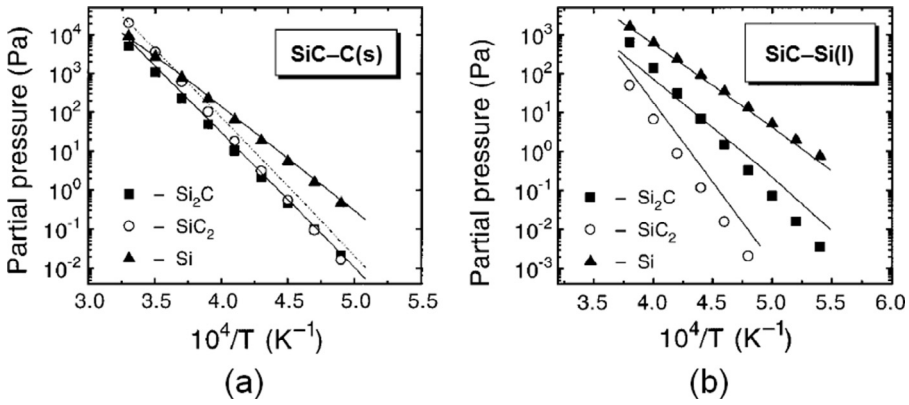

Fig. 3. Arrhenius plots of partial pressures of sublimed species from (a) SiC + C and (b) SiC + Si systems at high temperature [26,27].

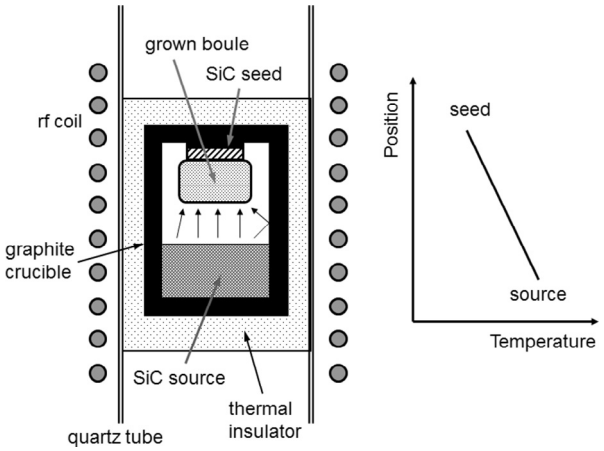

Fig. 4. Schematic illustration of a crucible and associated parts used for seeded sublimation growth of SiC [28–30].

In state-of-the-art growth technology, SiC boules are usually grown with a growth rate of 0.3–0.8 mm/h at several hundreds Pa or lower. Although the growth rate can be increased to 1–2 mm/h, this faster growth often results in significant generation of extended defects in the grown crystal. One obvious obstacle in sublimation growth is the limitation of growth time. At present, the length of SiC boule crystals is limited to 30–50 mm. To overcome this problem, several modifications to achieve continuous feeding of source materials have been investigated [33,34].

In seeded sublimation growth of SiC, the growth is carried out in a quasi-closed graphite crucible, and one can control the process parameters such as the temperature and pressure only from the outside, without monitoring the inside. Toward better control of SiC growth, modeling and simulation of SiC sublimation growth have been extensively investigated [35–38]. Calculation of heat and mass transport during sublimation growth of SiC is standard technology. These realistic simulations can be used to design crucible geometries and temperature profiles for the growth of high-quality SiC boules. To treat chemical reactions in the gas phase and at the growing surface, a reliable database for a number of chemical reactions at very high temperatures is mandatory, which at present is a challenge. Nevertheless, a recent simulation package offers reasonably good agreement with experimental results such as the growth rate and shape of a grown boule, and has been employed as a powerful tool for crystal growers.

Another important role of simulation in the sublimation growth of SiC is the simulation of stress in the boules [39,40]. As will be described in section 3.2.3, thermal stress plays a critical role in the generation of extended defects in SiC boules. The causes of thermal stress include different thermal expansion coefficients between SiC and the crucible (graphite) and radial or axial temperature inhomogeneity. When the resolved shear stress on a primary slip system exceeds a critical resolved stress, glide and multiplication of dislocations take place, leading to a significantly increased dislocation density in the boule. It is often observed that the dislocation density is high near the center and near the wafer edge. This distribution is consistent with the distribution of the shear stress predicted by simulation [39]. More recently, three-dimensional modeling and simulation of SiC sublimation growth have been reported [41,42]. Effects of the SiC boule shape, growth conditions, and cooling rate on generation and multiplication of basal plane dislocations have been clarified in great detail [41,42].

Through extensive efforts in sublimation growth of SiC, the wafer size and quality have remarkably been improved in the last decade [43,44]. 4H-SiC{0001} wafers with a diameter of 150 mm are currently in mass production by several manufacturers, and 200 mm wafers were demonstrated in 2015 [44].

3.2.2. Polytype control in sublimation growth

From a materials science point of view, the kinetic and thermodynamic factors which determine the SiC polytype actually grown are not completely understood. Because SiC{0001} is usually employed as the seed crystal, polytype switching or nucleation of foreign polytypes may occur during growth, unless intentionally controlled. One obvious kinetic factor is the polytype replication through spiral growth around threading screw dislocations. Along the step edges, the stacking information is provided, which ensures replication of that polytype in the growing crystal.

Although spiral growth is favorable for polytype replication, nucleation on the terraces can naturally take place in the initial stages of growth as well as during growth. It has been suggested that there exists a close relationship between the polytype stability and the C/Si ratio (C enrichment) in the growth ambient [45]. When the growth ambient is C-rich, a polytype with a higher hexagonality tends to be more stable. For example, 4H-SiC (hexagonality: 0.5) is more stable than 6H-SiC (hexagonality: 0.33) under C-rich growth conditions. In real experiments, the most striking parameter determining the polytype is the polarity of the seed crystal. Sublimation growth on SiC(0001) (Si face) under adequate conditions gives a 6H-SiC boule, even if the seed is 4H-SiC(0001). In contrast, a 4H-SiC boule is grown on SiC($000\bar{1}$) (C face), irrespective of the seed polytype [46]. This result is explained by the difference in surface energy between the Si and the C faces [11]. Furthermore, 4H-SiC is preferentially grown at relatively low temperature and low pressure, while relatively high temperature and high pressure result in 6H-SiC growth (The growth temperature and pressure, of course, influence the C/Si ratio on the growing surface). Another important factor is impurity incorporation. Nitrogen (N) doping during the growth stabilizes 4H-SiC, while aluminum (Al) doping leads to preferential growth of 6H-SiC. Because N atoms occupy the carbon lattice sites, incorporation of N atoms will cause the growth environment to become slightly C-rich, which favors the growth of 4H-SiC. In recent years, the stability of SiC polytypes during sublimation growth has been studied using classical thermodynamic nucleation theory, and the theoretical analyses are in good agreement with these experimental results [47]. Furthermore, it is reported that impurity additives such as Sc and Ce stabilize 4H-SiC [45,48]; this can also be explained by a shift in the growth ambient toward C-rich conditions.

3.2.3. Defect evolution and reduction

Table 1 shows the major extended defects observed in SiC boules and wafers. The Burgers vector, the major direction, and the typical density of dislocations present in boules (wafers) prepared using state-of-the-art technology (for n-type 4H-SiC) are shown. Note that inclusions of foreign polytypes and stacking faults have been greatly reduced. The typical stacking fault density along the *c*-axis is below 1 cm^{-1}. Generation of double Shockley stacking faults observed in heavily N-doped SiC is described in section 3.2.4.

A micropipe (MP) defect is a hollow core associated with a superscrew dislocation. When the magnitude of the Burgers vector is very large, the strain field around the dislocation core becomes extremely high (proportional to $|\boldsymbol{b}|^2$, where $\boldsymbol{b}$: Burgers vector), and a microscopic pinhole is formed by breaking bonds [49,50]. The minimum magnitudes of the Burgers vector for MPs have been determined as $|3\boldsymbol{c}|$ for 4H-SiC and $|2\boldsymbol{c}|$ for 6H-SiC [51,52], both of which correspond to 3 nm. Because a MP is a pinhole extending along the <0001> direction through the entire SiC wafer, it is not surprising that SiC devices which contain a MP exhibit severely degraded performance, such as excessive leakage current and premature breakdown [53]. Through development of stable growth under well-controlled conditions and enhanced dissociation of MPs, MP defects have been almost

Table 1
Major extended defects observed in SiC wafers. The Burgers vector, primary direction, and typical density of the extended defects in bulk wafers and epitaxial wafers prepared using the state-of-the-art technology (for n-type 4H-SiC) are shown.

Dislocation	Burgers vector	Primary direction	Density in bulk wafers	Density in epitaxial wafers
Micropipe (MP)	$n<0001>$ ($n>2$)	<0001>	0–0.1 cm^{-2}	0–0.1 cm^{-2}
Threading Screw Dislocation (TSD)	$n<0001>$ ($n=1, 2$) (partly mixed dislocations)	<0001>	300–500 cm^{-2}	300–500 cm^{-2}
Threading Edge Dislocation (TED)	$\langle 11\bar{2}0\rangle/3$	<0001>	2000–5000 cm^{-2}	2500–6000 cm^{-2}
(Perfect) Basal Plane Dislocation (BPD)	$\langle 11\bar{2}0\rangle/3$	in {0001} plane (preferably $<11\bar{2}0>$)	500–1000 cm^{-2}	0.1–1 cm^{-2}
Stacking Fault (SF)	mostly Shockley type	in {0001} plane	<1 cm^{-1}	0.05–0.5 cm^{-1}

eliminated (density < 0.1 cm^{-2}) [40,43,54]. MP-free wafers are currently commercially available from most vendors.

A threading screw dislocation (TSD) is located at the center of spiral growth during sublimation growth on a SiC{0001} surface. TSDs usually propagate almost along the <0001> direction. Recent studies using synchrotron x-ray topography revealed that many of TSDs possess a Burgers vector of $\boldsymbol{c}+\boldsymbol{a}$ [55,56], which means that a significant portion of TSDs is not of pure screw type but mixed dislocations. TSDs are basically replicated from a seed crystal. A major cause of TSD nucleation in SiC sublimation growth is the generation of a half loop at the initial stage of bulk growth. It is reported that the number of TSDs with a Burgers vector of $+1\boldsymbol{c}$ is almost the same as that with $-1\boldsymbol{c}$, and that $+1\boldsymbol{c}$ and $-1\boldsymbol{c}$ dislocations are often observed nearby as if they are a pair [57].

A threading edge dislocation (TED) and basal plane dislocation (BPD) possess the same Burgers vector of $\boldsymbol{a}\left(\langle 11\bar{2}0\rangle/3\right)$. Therefore, TED and BPD have similar basic nature; the name simply differs depending on the dislocation direction. In fact, inside the boule crystals, conversion from BPD to TED and from TED to BPD is often observed [58,59]. Note that pure edge-type BPDs are not very abundant, and often BPDs lie along the <11$\bar{2}$0> directions, due to the Peierls potential. Both TEDs and BPDs in a seed are replicated in the SiC boule, though dislocation conversion may occur, as mentioned above.

It is important to consider the nucleation of dislocations (grown-in dislocations) to reduce the dislocation density. In addition to the kinetics during the initial stage of growth, thermal stress is another important factor for dislocation nucleation. BPDs are relatively easily introduced into the growing boule (plastic deformation) when the resolved shear stress exceeds a certain (critical) value [60,61]. A major source of the stress is thermal stress, which develops during sublimation growth when the temperature profile is not appropriate. Both radial and axial temperature gradients cause inhomogeneous thermal expansion inside the boule. Furthermore, the difference in the thermal expansion coefficients of SiC and graphite parts causes severe thermal stress during cooling. Fig. 5 depicts a schematic illustration of the shear stress, the associated dislocations, and the bending of a basal plane in a growing SiC boule, taking account of typical radial and axial temperature gradients [62]. The temperature is higher along the periphery of the boule than in the center because of radiation from the crucible walls. The temperature of the growing surface is higher than the seed temperature because of the temperature gradient designed to promote mass transport from the source to the seed. Under these circumstances, thermal expansion is

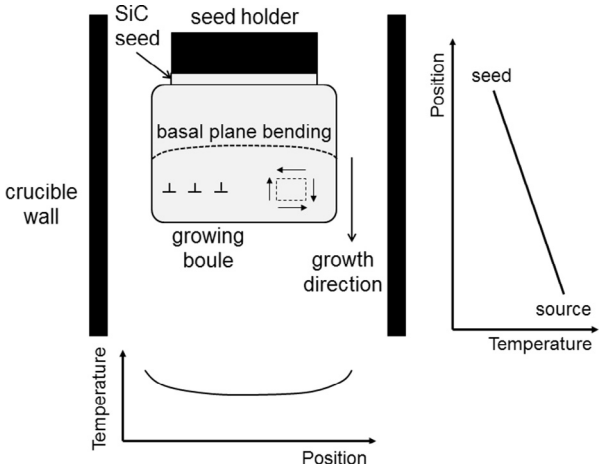

Fig. 5. Schematic illustration of the shear stress, the associated dislocations, and the bending of a basal plane in a growing SiC boule, taking account of typical radial and axial temperature gradients during sublimation growth.

not uniform inside the boule; this causes significant thermal stress and bending of basal planes. Furthermore, multiplication of BPDs can take place via the Frank-Read mechanism, when the thermal stress is significant [63]. Most TEDs are formed by conversion from BPDs along the growth direction during growth.

Fig. 6 shows a schematic illustration of dislocation networks observed in SiC boules, as revealed by plane-view and cross-sectional synchrotron x-ray topography [59]. Threading dislocations are mostly propagating along the <0001> direction, and BPDs often connect neighboring TSDs. BPDs tend to align along the <11$\bar{2}$0> directions. TEDs and BPDs are transformed into each other, as described above.

One striking technique to reduce extended defects in SiC boules is the so-called "Repeated *a*-face Growth (RAF)" method [64]. The main concept is the preparation of an almost dislocation-free seed and subsequent sublimation growth on the high-quality seed under stabilized conditions. The almost dislocation-free seed can be prepared by repeating SiC boule growth on *a*- and *m*-face seeds, which were cut from a boule grown in the previous step. The dislocation density exhibits rapid decrease as the growth is repeated on *a*- and *m*-faces. A low dislocation density of 75 cm^{-2} achieved by employing this technique was demonstrated [64].

3.2.4. Doping control

In the sublimation growth of SiC, N and Al are the dopants of preference for growth of n- and p-type boules, respectively. However, the purity of SiC boules grown by the sublimation method is not as high as Si and it is

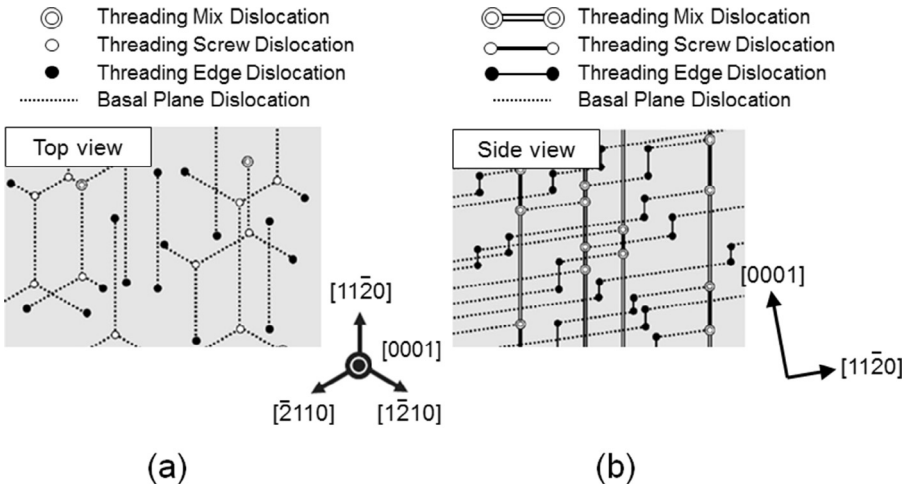

Fig. 6. Schematic illustration of dislocation networks observed in SiC boules, as revealed by plane-view and cross-sectional synchrotron x-ray topography of high-quality SiC crystals [59].

strongly dependent on the purity of the SiC source and graphite parts. The typical unwanted impurities include Ti, V, Cr, Fe, Co, Ni, and S [28], and the density of these metallic impurities is in the range of 10^{13}–10^{15} cm^{-3}. In addition to the metallic impurities, N, B, and Al are commonly incorporated in the boule crystals, at densities of 10^{14}–10^{16} cm^{-3}, even in nondoped growth. The net doping density of nondoped SiC boules grown by sublimation ranges from a mid 10^{15} to a low 10^{16} cm^{-3}.

N-type doping is performed simply by introducing a N_2 gas into the growth ambient. The N dopant density can be increased to 10^{20} cm^{-3}, which results in a very low resistivity of 0.005 Ωcm [65,66]. However, the typical resistivity of commercial n-type 4H-SiC wafers range from 0.015 to 0.025 Ωcm (N density: 6×10^{18}–1×10^{19} cm^{-3}). It is known that stacking faults are formed when heavily-doped 4H-SiC wafers are oxidized or annealed in Ar at temperatures higher than 1000–1100 °C [66–69]. Stacking fault formation becomes pronounced when the N density exceeds about 2×10^{19} cm^{-3}, and the structure of the stacking fault has been identified as (6,2) in Zhdanov's notation (or "double Shockley stacking fault") [68,70]. It has been suggested that the electrostatic potential energy of the crystal can be lowered by formation of quantum-well-like stacking faults and subsequent electron trapping [70]. After several models were proposed and examined, the major trigger for generation of stacking faults is now believed to be stress and the resulting BPD segments in the crystal; in particular, polishing-induced damage can act as generation sites [71].

P-type doping is achieved by adding Al (or Al-containing compound) to the SiC source. Al doping is much more difficult than N doping in SiC sublimation growth because severe depletion of the Al source occurs during growth. In 4H-SiC boule growth, heavy Al doping creates a condition favorable for 6H-SiC stabilization. Thus, sublimation growth of p^+-type 4H-SiC is a challenge. The resistivity of typical p-type 4H-SiC wafers is rather high, about 1–5 Ωcm.

High-resistivity wafers are required for fabrication of SiC or GaN-based high-frequency devices to minimize the parasitic capacitances. The main approach to obtain semi-insulating boule crystals is (i) to reduce the background impurities as much as possible and (ii) to intentionally introduce deep levels, which act as efficient trap centers (energetically deeper levels are preferable).

In SiC, vanadium (V) was the first element used as a compensating center to create semi-insulating wafers [72,73]. The V impurity acts as an acceptor-like (–/0) trap in n-type SiC and a donor-like (0/+) trap in p-type SiC. The acceptor level of V is $E_C - (0.81–0.97)$ eV in 4H-SiC, while the donor level is estimated as $E_V + (1.3–1.5)$ eV [74,75]. Because the donor level is deeper, V doping was performed for slightly p-type SiC boules to achieve very high resistivity. The resistivity of the semi-insulating SiC wafers is about 10^{11}–10^{13} Ωcm at room temperature [72,73]. The solubility limit of V in SiC is not very high, in the mid 10^{17} cm^{-3}, while the residual dopant density in SiC boules can be 10^{16} cm^{-3}, indicating that precise control of V doping is required.

More recently, use of intrinsic point defects, which create deep levels, has been investigated, and "high-purity semi-insulating" (HPSI) wafers have been obtained [76,77]. Intrinsic point defects can be introduced by adjusting the growth conditions or by high-energy particle irradiation after growth [78]. The obtained resistivity

exceeds 10^{12} Ωcm at room temperature; the activation energy of the resistivity was found to vary significantly for different wafers, and ranges from 0.8 to 1.5 eV [76,77]. Recent studies based on electron paramagnetic resonance (EPR) measurements revealed that (i) silicon vacancies (V_{Si}) are the dominant traps in HPSI wafers with activation energies of 0.8–0.9 eV, (ii) carbon antisite–carbon vacancy pairs (C_{Si}-V_C) or carbon vacancies (V_C) are dominant in wafers with an activation energy of 1.1–1.3 eV, and (iii) V_C or divacancies (V_C-V_{Si}) are the main trap centers in wafers with an activation energy of 1.5 eV [79].

3.3. Other growth techniques

3.3.1. High-temperature chemical vapor deposition

To overcome the limitations of the sublimation method of SiC, high-temperature chemical vapor deposition (HTCVD) has been developed [80–82]. Fig. 7 schematically illustrates a reactor and a temperature profile used for HTCVD of SiC. The SiC boule growth is performed in a vertical crucible made of graphite, where the precursor gases are fed upward through a heating zone to the seed crystal holder placed at the top. The precursor gases are SiH_4 and a hydrocarbon, such as C_2H_4 and C_3H_8, diluted in a carrier gas. The geometry is similar to that of the vertical CVD reactors used for epitaxial growth, but the typical growth temperature is very high, 2100–2300 °C. Inside the hot zone, Si and SiC clusters are formed via homogeneous nucleation because of the high supersaturation in the gas phase. These clusters act as a virtual source for SiC boule growth on the seed. The temperature of the gas-cracking zone and the walls should be slightly higher than that of the seed crystal, to ensure mass transport and condensation on the seed. The typical growth pressures and growth rates are 25–80 kPa and 0.3–1.5 mm/h, respectively [82–84].

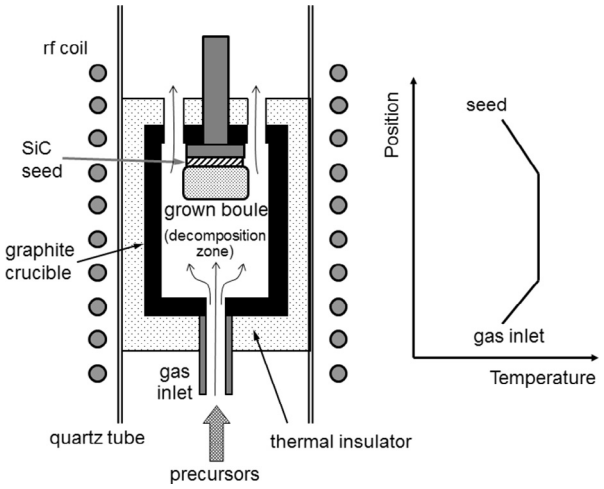

Fig. 7. Schematic illustration of a reactor (core part) and temperature profile used for SiC bulk growth by high-temperature chemical vapor deposition.

The major advantages of HTCVD compared with the sublimation method include (1) high purity, (2) intentional control of C/Si ratio, and (3) continuous supply of the source materials. For example, the density of residual impurities (N, B) is in the mid 10^{14} cm^{-3}, and is much lower for other impurities. Because of this purity, it is relatively easy to produce HPSI wafers by HTCVD [85]. Although reports on HTCVD of SiC are still limited, this method possesses much potential for production of high-quality, long SiC boules.

3.3.2. Solution growth

Fig. 8 shows a schematic illustration of a typical furnace and temperature profile used for solution growth of SiC. A graphite crucible is filled with Si-based melt, and the seed crystal is placed in contact with the melt surface (Top Seeded Solution Growth: TSSG). The seed temperature is slightly lower than the melt, and this provides a driving force for growth. Growth is carried out in an inert atmosphere, such as in Ar. The growth temperature ranges from 1750 to 2100 °C.

In spite of the great promise, several special cares are required in solution growth of SiC. As described in section 3.1, there exists no stoichiometric SiC liquid phase at atmospheric pressure, and the C solubility in the Si melt is only 15% even at 2800 °C. At such high temperature, Si evaporation is significant, making continuous growth almost impossible. Furthermore, the Si melt reacts significantly with the graphite crucible (which in turn acts

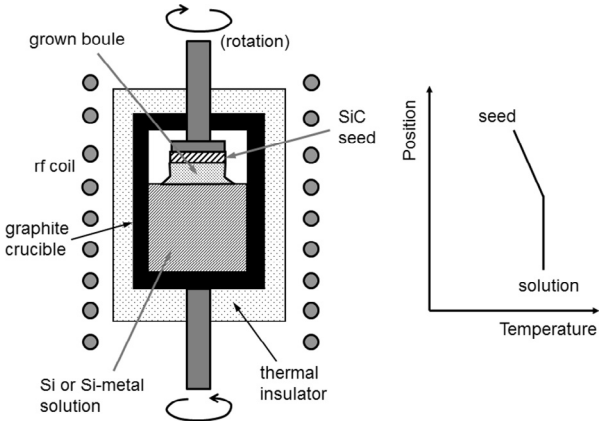

Fig. 8. Schematic illustration of a typical furnace and temperature profile used for SiC solution growth (top seeded solution growth).

as a carbon source for the growth), which presents another challenge for long growth.

In the early stage, high-pressure solution growth was investigated to suppress Si evaporation [86]. The growth rate was below 0.3 mm/h at 2200–2300 °C, and the size of the SiC boule crystals grown was very limited. In recent years, solution growth with a metal-added solvent is a hot topic in the field of SiC bulk growth. It is known that the C solubility can be remarkably increased by adding rare-earth or transition metals such as Sc, Pr, Fe, Ti, or Cr. By using Si-Sc-C or Si-Ti-C solvent, for example, reasonable growth rates of about 0.3–0.5 mm/h were attained at relatively low temperatures of 1750–1950 °C [30,87–91]. These studies already demonstrate low dislocation density in the grown crystals. MPs are easily closed, and TSDs are mostly converted to Frank-type stacking faults in the basal planes [92]. Metallic contamination from the solvent could be a problem, and this subject is now being investigated. By controlling the meniscus near the growing surface, remarkable diameter enlargement has been achieved without degradation of quality [93]. A tradeoff between high growth rate and growth stability is currently being investigated. Recent progress in solution growth of SiC bulk crystals is rapid, and a "dislocation free" 4H-SiC boule was demonstrated by solution growth on a $(000\bar{1})$ seed sliced from a $<1\bar{1}00>$-grown boule [94], though the boule size is small. Furthermore, solution growth of SiC has another advantage in terms of impurity doping. Doping efficiency of both N and Al can be higher in solution growth, and low resistivities of n- and p-type SiC bulk materials have been achieved [95,96].

4. Epitaxial growth of silicon carbide

4.1. Fundamentals

4.1.1. Polytype replication in SiC epitaxy

In the early stage, polytype mixing, or more specifically inclusion of twinned crystalline 3C-SiC, had been a serious problem in homoepitaxy of a hexagonal SiC polytype by chemical vapor deposition (CVD) [97–100]. The concept of perfect polytype replication in 6H-SiC epitaxial layers on 6H-SiC substrates was proposed in 1987 [97,101,102]. Using step-flow growth on 2–6° off-axis 6H-SiC{0001}, homoepitaxial growth of 6H-SiC with a smooth surface was achieved by CVD at 1450–1550 °C. In the same manner, homoepitaxial CVD growth of 4H-SiC was demonstrated on 5–6° off-axis 4H-SiC{0001} [48,103]. This growth technique, referred to as "step-controlled epitaxy", is applicable to homoepitaxy of other polytypes such as 15R-SiC. Homoepitaxial growth of high-quality SiC on off-axis SiC{0001} substrates has been described in several review papers [97,104–108].

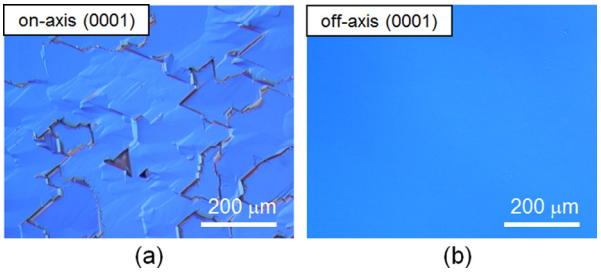

Fig. 9. Surface morphology for SiC epitaxial layers grown on (a) on-axis and (b) 5° off-axis 4H-SiC(0001) substrates at 1500 °C at a growth rate of 3 μm/h.

In SiC CVD, SiH_4 and C_3H_8 or C_2H_4 are usually employed as the precursors. The carrier gas is H_2, and Ar is sometimes added. The typical growth temperature and growth rate are 1500–1650 °C and 3–15 μm/h, respectively. The CVD growth process for SiC usually consists of (1) *in-situ* etching and (2) main epitaxial growth. The *in-situ* etching is performed with pure H_2, HCl/H_2, hydrocarbon/H_2, or SiH_4/H_2 at high temperature (typically the same temperature as used for the main growth). The purpose of *in-situ* etching is to remove the subsurface damage due to substrate polishing and to obtain regular step structures. Immediately after etching, the main growth of SiC is performed.

Fig. 9 shows the surface morphology for epitaxial layers grown on on-axis and 5° off-axis 4H-SiC(0001) substrates at 1500 °C at a growth rate of 3 μm/h. On an on-axis (0001) face, the epitaxial layer exhibits a mosaic-like surface morphology, and relatively smooth domains are separated by step- or groove-like boundaries. From transmission electron microscopy (TEM) and Raman scattering, the grown layer is identified as 3C-SiC(111) with twinning. In contrast, the epitaxial layer on the off-axis substrate exhibits a specular smooth surface, and the structural analysis revealed homoepitaxy of single crystalline 4H-SiC(0001). The preferred off-direction is $<11\bar{2}0>$, because CVD growth on off-axis (0001) substrates inclined toward $<1\bar{1}00>$ often results in a stripe-like morphology, which is caused by pronounced step bunching [102,109]. The inclusion of 3C-SiC domains is occasionally observed after prolonged growth times on off-axis (0001) substrates inclined toward $<1\bar{1}00>$.

Fig. 10 shows a schematic illustration of growth modes and stacking sequences of the layers grown on (a) on-axis 4H-SiC(0001) and (b) off-axis 4H-SiC(0001). The bond configuration near an atomic step and on the (0001) terrace is also shown in Fig. 10(c). The precursors are heated and decomposed, and the source species diffuse

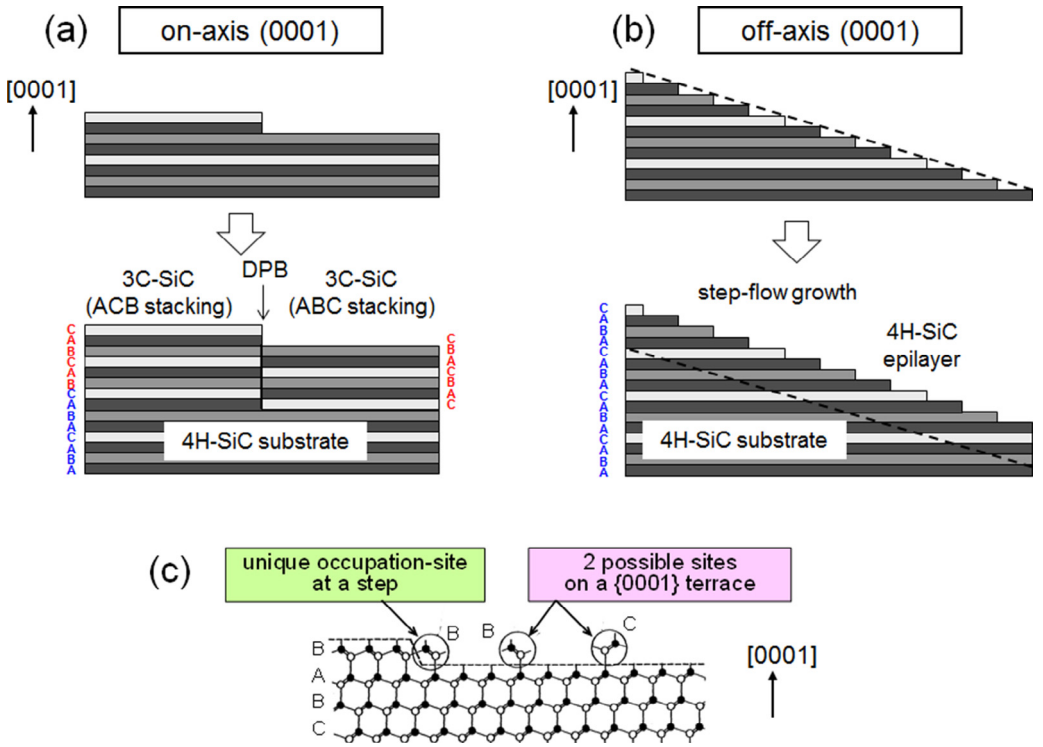

Fig. 10. Schematic illustration of growth modes and stacking sequences of the layers grown on (a) on-axis 4H-SiC(0001) and (b) off-axis 4H-SiC(0001). (c) Bond configuration near an atomic step and on the (0001) terrace.

toward the substrate surface. Adsorbed species migrate on the surface and are incorporated into a crystal at steps and/or kinks. However, there exists another competitive growth process of nucleation on terraces, which takes place when the supersaturation is high enough.

On on-axis {0001}, the step density is very low with large {0001} terraces. The crystal growth must occur predominantly through two-dimensional nucleation because of high supersaturation. The polytype of the grown layers is determined by growth conditions, especially the temperature. This leads to the growth of 3C-SiC, which is stable at low temperature [8,110]. It is pointed out that defects such as polishing-induced damage on the surface can trigger 3C-SiC nucleation when the supersaturation is high [111]. The growing 3C-SiC can take two possible stacking orders of ABC… and ACB…, as shown in Fig. 10(a).

On off-axis {0001}, the step density is high, and the terrace width is narrow enough for adsorbed species to migrate and reach steps. At a step, the incorporation site (A, B, C) is uniquely determined by bonds of the step, as shown in Fig. 10(b). Hence, homoepitaxy can be achieved through step-flow growth, inheriting the stacking order of the substrate. In other words, the surface steps serve as a template, which forces the replication of the substrate polytype in the epilayer.

A simple surface diffusion model based on the BCF (Burton, Cabrera, and Frank) theory [112] is useful to predict the step-flow growth condition where stable homoepitaxy of SiC is achieved [113]. In this model, the distribution of adatom density and the supersaturation ratio (σ_s) on a vicinal surface are estimated. Since σ_s takes a maximum value σ_{s_max} at the center of a terrace between neighboring steps, nucleation occurs most easily at this location. σ_{s_max} depends on experimental conditions such as the growth rate, growth temperature, and terrace width (off-angle and step structure), and is an essential parameter that determines whether the growth mode is step-flow or two-dimensional nucleation. Because the two-dimensional nucleation rate J_{nuc} increases exponentially with the supersaturation ratio on a surface, nucleation becomes significant when σ_{s_max} exceeds a critical value σ_{s_crit}. Thus, the growth modes on SiC{0001} are determined according to the relationship between σ_{s_max} and σ_{s_crit} as follows:

$\sigma_{s\_max} > \sigma_{s\_crit}$: two-dimensional nucleation (growth of twinned 3C-SiC),

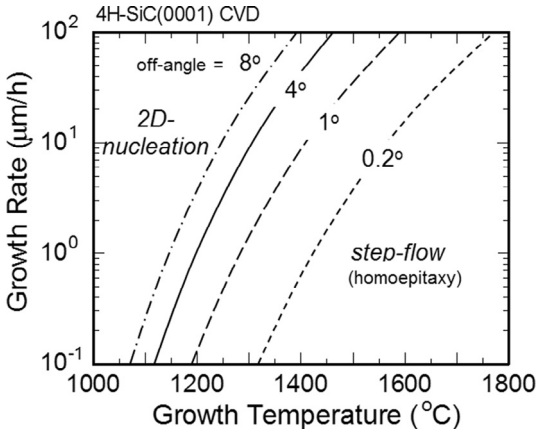

Fig. 11. Critical growth conditions for CVD growth of 4H-SiC(0001), where the maximum growth rate is plotted as a function of growth temperature for a given off-angle of the substrate. The top-left and bottom-right regions separated by a curve correspond to the two-dimensional nucleation (severe 3C-SiC inclusions) and step-flow growth (4H-SiC homoepitaxy) conditions, respectively.

$\alpha_{s\_max} < \alpha_{s\_crit}$: step-flow (growth of single crystalline 4H-SiC).

In experiments, critical growth conditions (boundary conditions between step-flow and two-dimensional nucleation) can be found by analysis of CVD results under various growth conditions. The growth temperature and off-angle were varied in the range of 1100–1700 °C and 0.2–10°, respectively. Higher growth temperature, larger off-angle and lower growth rate are preferable for homoepitaxy of 4H-SiC (step-flow growth). Furthermore, CVD growth with a low C/Si ratio (the ratio of carbon and silicon atoms in the supplied precursors) is beneficial to promote homoepitaxy [114]. By combining the BCF model and several critical growth conditions obtained by experiments, critical growth conditions can be predicted. For example, if the growth temperature and off-angle of substrates (terrace width) are fixed, a critical growth rate (maximum growth rate to realize step-flow growth) can be estimated. Curves for the critical growth conditions are shown in Fig. 11 for substrates with off-angles of 0.2, 1, 4, and 8°. Note that this chart has been significantly updated from one presented in Reference [113], because recent experimental data were employed in the analysis. In the figure, the top-left and bottom-right regions separated by the curves correspond to the two-dimensional nucleation (growth of twinned 3C-SiC) and step-flow growth (homoepitaxy of 4H-SiC) conditions, respectively. At 1700 °C, a very small off-angle of 0.2°, which yields almost "on-axis" {0001}, is sufficient to achieve step-flow growth with a growth rate of about 50 μm/h. Note that spiral growth around threading screw dislocations is not considered in the present model. Spiral growth naturally promotes homoepitaxial growth. Conversely, large off-angles greater than 4° are needed to achieve homoepitaxy at a low temperature of 1200 °C with a reasonable growth rate (>1 μm/h).

4.1.2. Reactor design for SiC CVD

Because high temperature (1500–1700 °C) is required in SiC CVD, several unique reactor designs have been developed. For example, buoyancy-driven convection is significant, and radiation dominates as the main mechanism for heat loss in this temperature range. In the early stage, cold-wall CVD reactors, similar to metal-organic CVD of III-V semiconductors have been developed [97–99]. In these reactors, however, the high growth temperature can result in a large temperature gradient normal to the wafer surface (>100 K/mm), which causes severe warpage of SiC wafers [115]. The heating efficiency is poor, since significant heat is lost by radiation.

These problems have been overcome by introduction of the hot-wall CVD concept [100,105]. Fig. 12 shows schematic illustrations of several typical hot-wall or warm-wall reactors employed for SiC CVD. In hot-wall CVD reactors, SiC wafers are placed inside a gas-flow channel inside a heated susceptor. The susceptor is made of dense graphite coated with polycrystalline SiC or TaC and is surrounded by a thermal insulator, such as porous graphite. By adjusting the frequency employed for rf-induction heating, the susceptor can be efficiently heated with minimal loss in the thermal insulator. In hot-wall CVD reactors, SiC wafers are heated from both sides, by radiation from the front side and by conduction (as well as radiation) from the back side. Therefore, the temperature gradient is considerably reduced (<10 K/mm), and good temperature uniformity can easily be established, which is critical for large-scale production of high-quality epitaxial wafers. The heating efficiency is also high in hot-wall CVD. So far, several hot-wall (or warm-wall) configurations have been proposed, as shown in Fig. 12. Among these reactor designs, a horizontal hot-wall CVD reactor with a rotating holder and a planetary warm-wall CVD reactor are commonly used for mass production of SiC epitaxial wafers. Very good uniformities of thickness and doping density have been achieved for multiple-wafer (10×100 mm wafers, 6×150 mm wafers) CVD systems [116,117]. Furthermore, a quasi-hot-wall vertical CVD reactor with single-wafer loading has been developed, as shown in Fig. 12(d) [118]. The boundary layer thickness is reduced by high-speed wafer rotation and low growth pressure, leading to a high growth

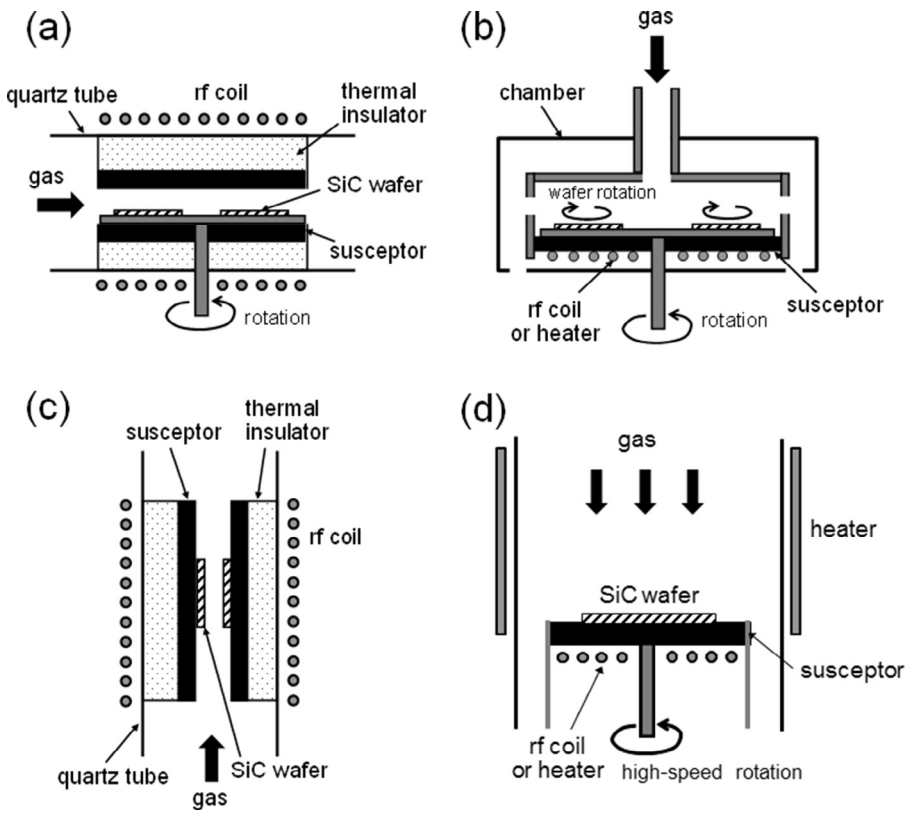

Fig. 12. Schematic illustrations of several typical hot-wall or warm-wall reactors employed for SiC CVD. (a) Horizontal hot-wall reactor, (b) hot-wall (or warm-wall) planetary reactor, (c) chimney-type vertical hot-wall reactor, and (d) vertical quasi-hot-wall reactor.

rate over 50 μm/h, while keeping high purity and high quality of epitaxial layers.

4.1.3. Growth rate and modeling

Under typical conditions for CVD growth of SiC, differences in the growth rates on different SiC faces such as (0001), $(000\bar{1})$, and $(11\bar{2}0)$ are very small, indicating that the SiC growth is diffusion limited [119]. Fig. 13 depicts the C/Si ratio dependence of the growth rate for 4H-SiC(0001) CVD [120]. In this particular experiment, the C/Si ratio was varied by changing the C_3H_8 flow rate while fixing the SiH_4 flow rate. When the C/Si ratio is lower than 1.0–1.3, the growth rate increases with increasing C/Si ratio (C_3H_8 flow rate). Above some C/Si ratio, the growth rate does not change when the C/Si ratio (C_3H_8 flow rate) is increased. In this saturation region, the growth rate is almost proportional to the SiH_4 flow rate. These are common trends in CVD growth of compound semiconductors. When the ambient is Si-rich, the growth rate is dominated by the C supply, while the growth rate is mainly determined by the Si supply under C-rich conditions. Near the "kink point" (C/Si ratio = 1.0–1.3), a nearly stoichiometric condition must be established

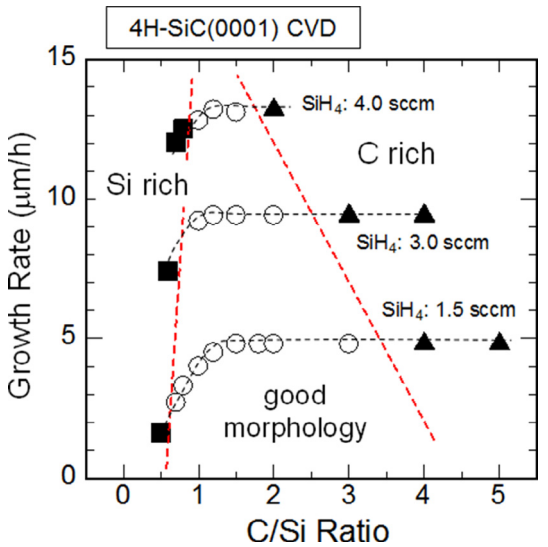

Fig. 13. C/Si ratio dependence of the growth rate for 4H-SiC(0001) CVD [120]. In this particular experiment, the C/Si ratio was varied by changing the C_3H_8 flow rate while fixing the SiH_4 flow rate.

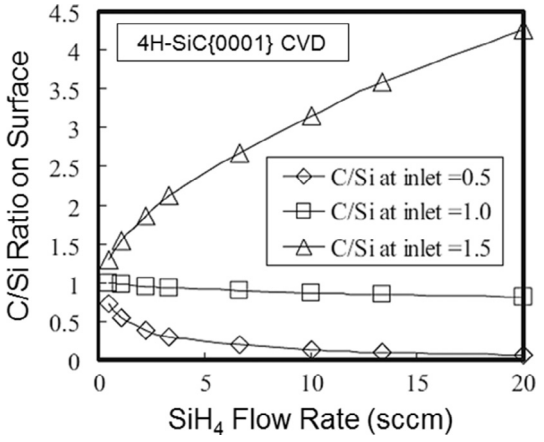

Fig. 14. Actual C/Si ratio as a function of the SiH_4 flow rate simulated for a few fixed C/Si ratios at the gas inlet [122]. The growth temperature and pressure are 1873 K and 25 kPa, respectively.

on the growing surface. In general, very good surface morphology is obtained near this stoichiometric condition. When the C/Si ratio is too low, the surface suffers from formation of severe macrosteps and Si droplets. In contrast, surface morphological defects such as triangular defects are easily generated when the C/Si ratio is too high.

Chemistries in SiC CVD have been studied extensively taking account of gas-phase and surface reactions at 1200–1600 °C in a SiH_4–C_3H_8–H_2 system [121]. The study has shown that the dominant species that contribute to SiC growth are Si, SiH_2, and Si_2H_2 species from SiH_4, and CH_4, C_2H_2, and C_2H_4 molecules from C_3H_8. More recently, accurate simulation models for SiC CVD were established [122–125]. In these models, the heat transfer and mass transfer equations are solved. Simulation of SiC CVD gives important insights into the temperature distribution of wafers, surface kinetics (including actual C/Si ratio, doping efficiency), and provides guidelines for up-scaling a reactor. In the simulation, the temperature dependences of gas-phase and surface reactions are considered. The effects of changes in the precursor supply, the C/Si ratio, the growth temperature, and the pressure on the growth rate can be well predicted by simulation. Fig. 14 depicts the actual C/Si ratio as a function of the SiH_4 flow rate simulated for a few fixed C/Si ratios at the gas inlet [122]. The growth temperature and pressure are 1873 K and 25 kPa, respectively. When the C/Si ratio at the inlet is fixed at 1.0, the actual C/Si ratio on the growing surface gradually decreases as the precursor flows are increased to obtain high growth rates. When the C/Si ratio at the inlet is 0.5 (Si rich) or 1.5 (C rich), the actual C/Si ratio is considerably shifted toward the Si-rich or C-rich condition, respectively, as the precursor flows increase. These results are important to understand the changes in surface morphology and impurity incorporation when the growth conditions are varied. The dependence of N and Al doping on the growth conditions has also been well described using simulation results [122].

4.1.4. Surface morphology and step dynamics

When the growth process is optimized, the surface of SiC homoepitaxial layers is mostly featureless, and the density of macroscopic surface defects is typically 0.1–0.5 cm^{-2}. The surface roughness defined by the root mean square (r_{rms}) is 0.14–0.22 nm for a scan area of $10 \times 10\ \mu m^2$. Although the surface roughness tends to increase in thick (>50 μm) layers, chemical mechanical polishing (CMP) of substrates, and optimized etching and growth conditions, greatly improve the surface morphology. When 4H-SiC(0001) substrates with small off-angles (2–4°) are used, formation of macrosteps is often observed [126,127]. Macrostep formation is not desirable because electric field crowding can take place, especially in gate oxides formed on such a surface. CVD growth under Si-rich conditions combined with an optimized etching condition [126,127] or the growth on $(000\bar{1})$ substrates [127,128] is effective for suppressing macrostep formation.

The step structure of SiC{0001} homoepitaxial layers has been studied using atomic force microscopy (AFM) and TEM. The majority of the surface steps on a 4H-SiC{0001} epitaxial layer exhibits a two- or four-bilayer height (half or full unit cell of 4H-SiC) [129]. The distribution of step heights is, of course, dependent on the growth condition, but the appearance of half- or full-unit-cell height steps is common for any hexagonal SiC epitaxial layers grown by CVD. It has been suggested that the surface energy is different for each SiC bilayer plane because of the peculiar stacking sequence [11,110]. Different surface energies may lead to different step velocities for each Si–C bilayer, and thereby cause "structurally-induced step bunching" [129].

4.2. Doping control

In SiC CVD (and other growth techniques), the site-competition effect is a key concept for achieving wide-range doping control [130,131]. The N incorporation is remarkably enhanced under Si-rich (low C/Si ratio) conditions and reduced under C-rich (high C/Si ratio) conditions. This phenomenon can be qualitatively explained by the competition between N and C atom incorporation on the growing surface, because N atoms occupy the C lattice site in SiC. Low C-atom coverage on the growing

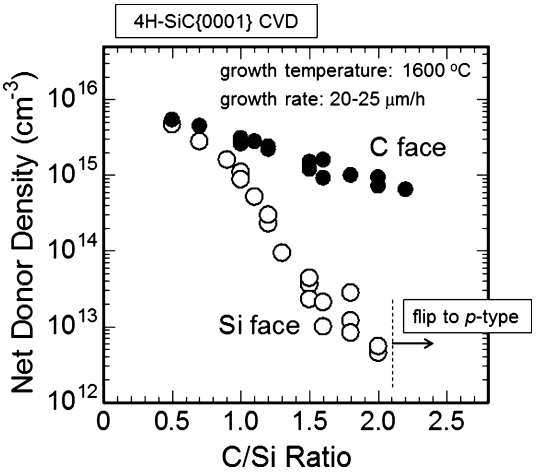

Fig. 15. C/Si ratio dependence of the doping density of nominally undoped 4H-SiC(0001) and $(000\bar{1})$ epitaxial layers grown by hot-wall CVD.

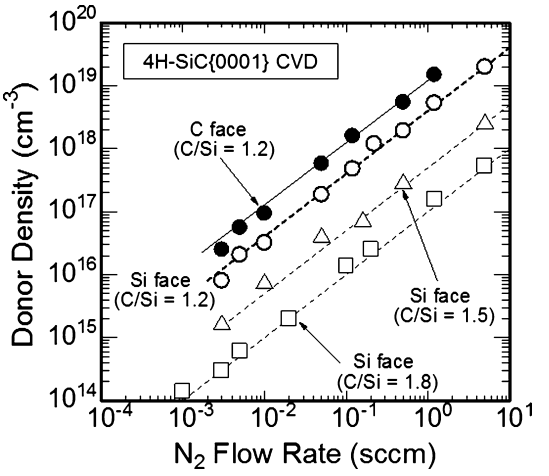

Fig. 16. Donor density versus N_2 flow rate in hot-wall CVD of 4H-SiC(0001) at 1550 °C.

surface promotes N incorporation into the lattice, while high C-atom coverage prevents N incorporation. Conversely, the doping of Al and B, which substitute the Si lattice site, shows the opposite trend: Al and B incorporation is reduced under Si-rich conditions and enhanced under C-rich conditions.

The purity of nominally undoped SiC epitaxial layers is high. Since the major source of unintentional dopants is N, key ways to obtain high purity are (1) increase of the C/Si ratio [130,131] and (2) decrease of the growth pressure [132,133]. Fig. 15 shows the C/Si ratio dependence of the doping density of nominally undoped 4H-SiC{0001} epitaxial layers grown by hot-wall CVD. In the case of C/Si ratio of 0.5, the donor density is about 5×10^{15} cm^{-3}, irrespective of the substrate polarity. On the (0001) face, the donor density can be drastically reduced by increasing the C/Si ratio; for example, it reaches 5×10^{12} cm^{-3} for growth with a C/Si ratio of 2. Further increase in the C/Si ratio causes the conduction type to change from n-type to p-type. Here, the p-type materials are obtained by reduction of N incorporation and enhancement of Al or B incorporation. On the $(000\bar{1})$ face, however, the C/Si ratio dependence of the doping density is much smaller, and the lowest donor density is about 8×10^{14} cm^{-3} in this particular case. Higher N incorporation (and lower Al incorporation) on the C face is commonly observed in SiC CVD [134–136] as well as in other growth techniques, including bulk growth. This result can be qualitatively explained by the different bond configurations on SiC(0001) and $(000\bar{1})$ faces [1].

In-situ n-type doping is easily achieved by introduction of N_2 during CVD growth. Fig. 16 plots the donor density versus N_2 flow rate in hot-wall CVD of 4H-SiC(0001) at 1550 °C. The donor density determined from capacitance–voltage (*C–V*) measurements is proportional to the N_2 flow rate over a wide range for CVD on both (0001) and $(000\bar{1})$ faces. When the growth temperature and pressure are fixed, the N_2 flow rate and the C/Si ratio are important parameters to achieve wide-range control of N doping (1×10^{14}–2×10^{19} cm^{-3}). Phosphorus doping has also been investigated, but it appears it is difficult to achieve high doping density.

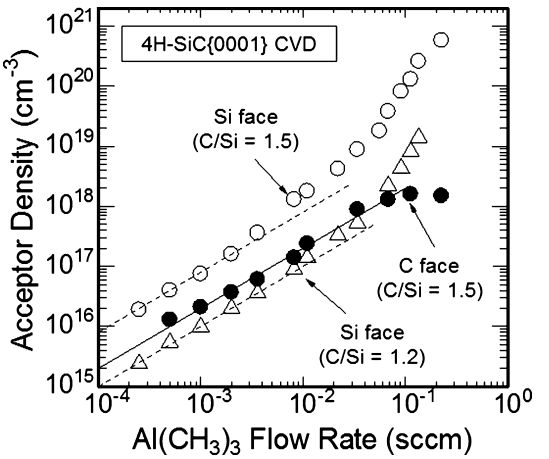

Fig. 17. Acceptor density versus trimethylaluminum (TMA) flow rate in hot-wall CVD of 4H-SiC{0001} at 1550 °C.

The addition of a small amount of trimethylaluminum (TMA: $Al(CH_3)_3$) is effective for *in-situ* p-type doping in SiC CVD [137]. Fig. 17 depicts the acceptor density versus the TMA flow rate in hot-wall CVD of 4H-SiC{0001} at 1550 °C. The acceptor density determined from *C–V* measurements agrees well with the Al atom density determined by secondary ion mass

spectrometry (SIMS) measurements. The Al doping efficiency is much higher (by a factor of 10–80) on the Si face than on the C face. On the Si face, the acceptor density increases super-linearly with the TMA supply. Such dependence may be attributed to the increased effective C/Si ratio under high TMA flow conditions. The supply of TMA causes the growth conditions to become more C-rich as a result of release of CH_3 species during decomposition of TMA. The accessible range of Al doping is about 2×10^{14}–5×10^{20} cm^{-3} on SiC(0001). Heavily-doped p-type layers can be easily grown only on the Si face, while it is difficult on the C face [97]. When the TMA supply is high, growth on the C face suffers from two- or three-dimensional nucleation, leading to a rough surface. Details of the dependence of aluminum doping on the growth conditions (temperature, pressure) are found in References [136,138]. A very low resistivity of 0.0165 Ωcm has been achieved by heavy Al doping over 5×10^{20} cm^{-3} [139]. Other p-type dopants include B and gallium (Ga), which can be introduced using B_2H_6 gas [140] or trimethylgallium (TMG) [141], respectively. However, B- or Ga-doped SiC exhibits high resistivity, because of the large ionization energy of these dopants. Abnormal diffusion of B atoms also causes problems in device processing [142].

4.3. Defects in SiC epitaxial layers

4.3.1. Extended defects

Various kinds of extended defects are present in SiC epitaxial layers. Some defects come from the substrates, while other defects instead nucleate during the epitaxial process. Roughly speaking, however, the total dislocation density terminating on the surface of a SiC epilayer is about the same as that intersecting the surface of the substrate [143], as shown in Table 1. Although dislocations cannot terminate inside the crystal, the line directions of the dislocations can change and this plays an important role in SiC epitaxy. Fig. 18 illustrates the dislocation replication and conversion typically observed in 4H-SiC epitaxial layers grown on off-axis {0001} by CVD [106,143,144]. Almost all the TSDs in a substrate are replicated in an epitaxial layer, but a small portion (typically < 1%) of TSDs is converted to Frank-type partial dislocations [145]. A TSD in the substrate can act as a nucleation site for a carrot defect, which is described later in this subsection. Although MPs in a substrate are replicated in the epitaxial layer without special treatment, MPs can be dissociated into several elementary closed-core screw dislocations during CVD growth, leading to "MP closing" [146,147]. Si-rich conditions in CVD enhance MP closing [147], and the MP closing probability

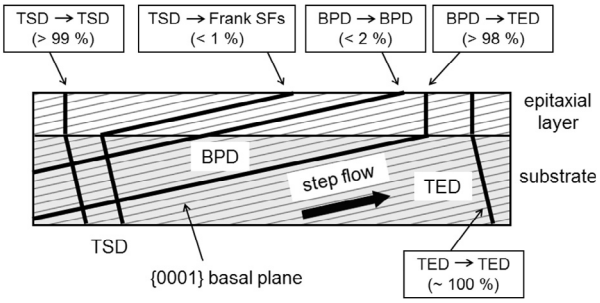

Fig. 18. Schematic illustration of dislocation replication and conversion typically observed in 4H-SiC epitaxial layers grown on off-axis {0001} by CVD.

reaches 99% or higher by decreasing the C/Si ratio to 0.7. TEDs in a substrate are also replicated in the epitaxial layer.

The most intense effort of the dislocation engineering during SiC epitaxy focused on BPDs. This focus stems from their detrimental effect on reliability of SiC bipolar devices [148–150], because a BPD can be the source of a Shockley-type stacking fault upon carrier injection, and such a stacking fault causes local reduction of carrier lifetimes (increase of on-resistance) and increase in leakage current [148,151]. This is called "bipolar degradation". When a BPD is replicated in an epitaxial layer, it extends in a basal plane, which is inclined by several degrees from the crystal surface. Since the elastic energy of a dislocation is naturally proportional to the dislocation length, BPD replication in an epitaxial layer grown on off-axis {0001} results in a large increase in elastic energy of the dislocation. This energy is greatly decreased by conversion of BPD to TED, by which process the dislocation length is considerably shortened by a factor of $\cot\theta$ (θ: off-angle). This dislocation conversion can be explained by a so-called "image force" applied to a BPD [143]. In reality, most (>90%) BPDs in the substrate are converted to TEDs within a few micrometers of an initial epitaxial layer without any special treatment [143,152,153]. Some BPDs are, however, replicated in a SiC epitaxial layer; it has been discovered that all these BPDs propagating in basal planes of an epitaxial layer are of a screw character [106,154,155]. Conversion from BPDs to TEDs is enhanced by several techniques such as molten KOH etching [156,157] or H_2 etching [158] prior to epitaxial growth or growth interruption [159]. Furthermore, increasing the growth rate also effectively enhances the BPD–TED conversion [160]. By combining these techniques, the conversion ratio has been increased to 99.9% or higher.

Nucleation of stacking faults (SFs) takes place during epitaxial growth, even if the substrate is free of stacking

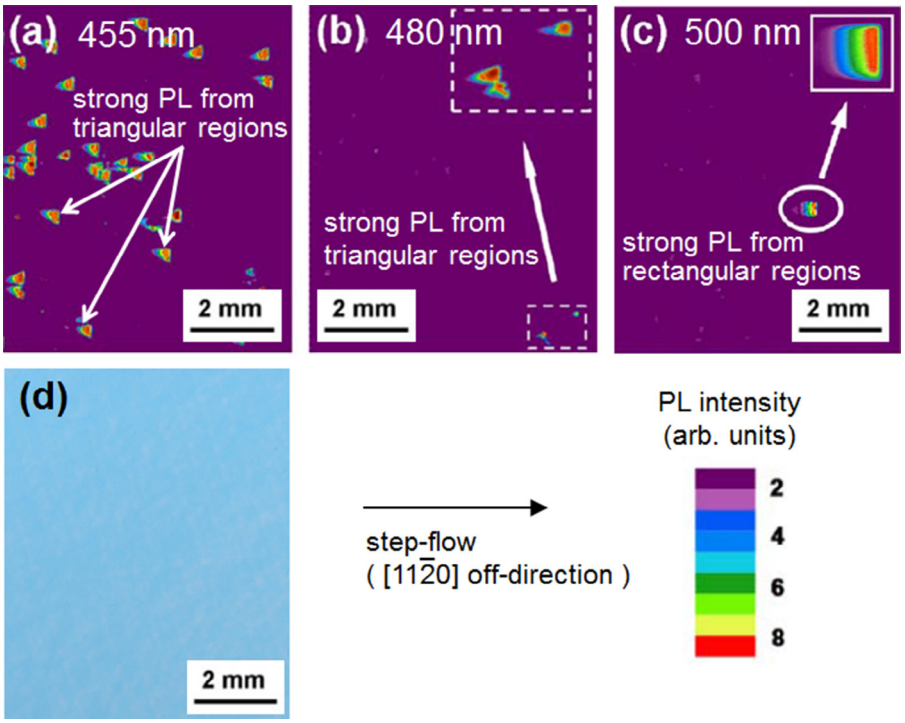

Fig. 19. Examples of photoluminescence-intensity maps taken at (a) 455 nm, (b) 480 nm, and (c) 500 nm from the same location by using band-pass filters [169]. An optical microscope image at the same location is shown in (d).

faults. It has been reported that both in-grown stacking fault and triangular 3C inclusion densities increase with increase of the growth rate [161], decrease of the off-angle [162,163], and decrease of the growth temperature. A majority of these SFs are caused by slips in basal planes (Shockley type), but Frank type SFs are also observed [164]. Note that most in-grown SFs are invisible in optical microscopy, and photoluminescence (PL) mapping/imaging is a powerful method to detect these defects [164–168], since each SF exhibits a distinct PL peak.

Fig. 19 shows examples of PL-intensity maps taken at (a) 455 nm, (b) 480 nm, and (c) 500 nm from the same location by using band-pass filters [169]. The optical microscope image is also shown in Fig. 19(d). The shape of these SFs is a triangle with its apex pointed toward the upstream side of the step flow. The lengths of all these SFs along the off-direction agree with the projected length of a basal plane in the epitaxial layer. This result implies that these SFs nucleated in the initial stage of epitaxial growth (near the epilayer/substrate interface). Although misalignment of atoms during step-flow growth has been suggested as the nucleation mechanism for SFs [170], the detailed mechanism is not very clear at present. Fig. 20 depicts high-resolution TEM images taken from the major in-grown SFs that exhibit PL peaks at (a) 455 nm, (b) 480 nm, and (c) 500 nm, respectively [169]. The stacking sequences have been determined as (44), (53), and (62) types, respectively, in Zhdanov's notation. One-to-one correlation has been established between the PL peak position and the stacking sequence. These in-grown SFs adversely affect device characteristics, for example, increase of leakage current [171]. Optimization of *in-situ* H_2 etching and use of lower growth rates at the start of epitaxial growth effectively reduce the density of these SFs. The total density of SFs is typically in the range of 0.05–0.5 cm^{-2} for epilayers grown at a standard growth rate (5–15 μm/h).

SiC epitaxial layers grown on off-axis {0001} substrates exhibit several types of macroscopic surface defects which contain extended defects. Fig. 21 shows the typical surface defects observed in 4H-SiC{0001} homoepitaxial layers, (a) "carrot" defect [106,172–174], (b) triangular defect [161,174], and (c) down-fall. Although the exact formation mechanisms of these defects are not fully understood, these defects are usually created by technical issues such as incomplete removal of polishing damage or non-optimized growth processes. The carrot (in some case, named "comet" depending on the defect shape and structure) and triangular defects are usually elongated along the down-step direction of step-flow growth. TEM studies revealed that the carrot (and comet) defects contain

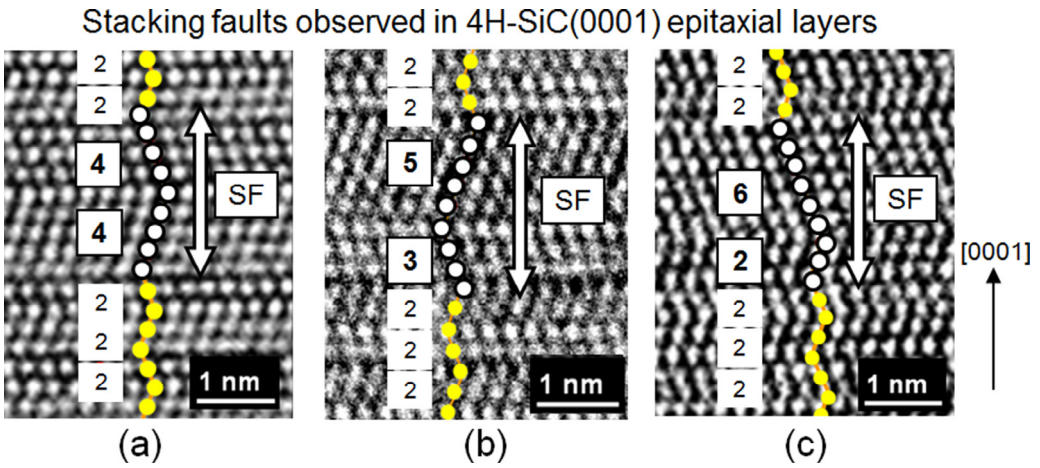

Fig. 20. High-resolution TEM images taken from the major in-grown SFs that exhibit PL peaks at (a) 455 nm, (b) 480 nm, and (c) 500 nm, respectively [169]. The stacking sequences have been determined as (44), (53), and (62) types, respectively, in Zhdanov's notation.

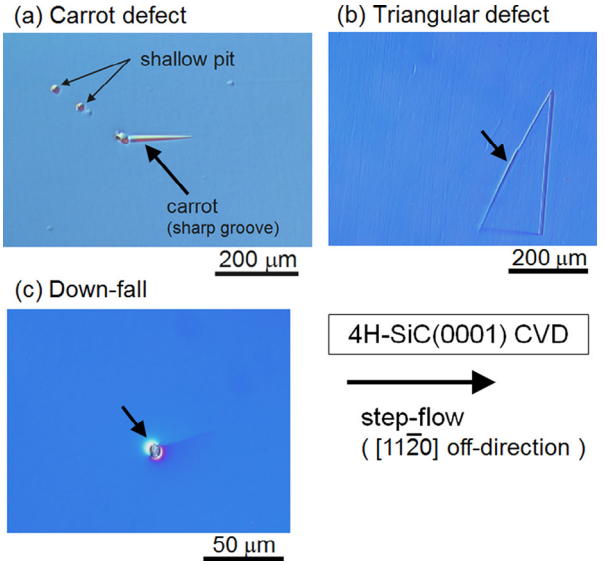

Fig. 21. Typical surface defects observed in 4H-SiC{0001} homoepitaxial layers, (a) "carrot" defect, (b) triangular defect, and (c) down-fall.

both a basal plane fault and a prismatic plane fault [106,172]. In most triangular defects, a 3C-like laminar region is extended in the basal plane [174]. The down-fall is generated by the fall of a SiC particle initially formed on the susceptor wall. The density of these defects is mostly influenced by the surface quality of the substrates and the conditions used for the growth process. The typical density of these macroscopic defects induced by epitaxial growth is approximately 0.1–1 cm^{-2}. When SiC devices include carrot (or comet) defects, triangular defects, or down-falls, the devices exhibit excessive leakage current and significantly decreased breakdown voltage [4,175].

4.3.2. Deep levels

Fig. 22 illustrates the energy levels of major deep levels observed in as-grown n-type and p-type 4H-SiC epitaxial layers [75,176–179]. Among these levels, the $Z_{1/2}$ (E_c − 0.63 eV) [75] and EH6/7 (E_c − 1.55 eV) [176] centers are the dominant defects (commonly observed at

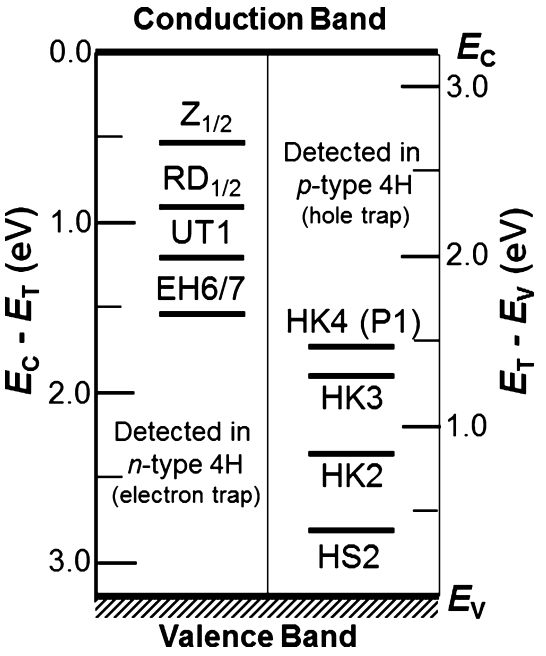

Fig. 22. Energy levels of major deep trap centers observed in as-grown n-type and p-type 4H-SiC epitaxial layers.

densities of $((0.3–2) \times 10^{13}$ cm^{-3}) in all as-grown epitaxial layers by CVD. Both centers are extremely stable against high-temperature (~1700 °C) annealing. In the lower half of the bandgap, the HK2 (E_v + 0.84 eV), HK3 (E_v + 1.24 eV), and HK4 (E_v + 1.44 eV) [179] centers are dominant deep levels. The densities of HK2, HK3, and HK4 centers are typically in the range of $(1–4) \times 10^{12}$ cm^{-3}. Because the HK2, HK3, and HK4 centers almost disappear upon annealing at 1450–1550 °C [179], the $Z_{1/2}$ and EH6/7 centers are more important. Indeed, the $Z_{1/2}$ center has been identified as the primary carrier-lifetime killer [180,181]. In addition to these levels, a few impurity-related levels are often observed in as-grown SiC epitaxial layers. For example, B contamination creates the B acceptor level (E_v + 0.35 eV) [182] and the B-related "D center" (E_v + 0.55 eV) [182]. Another common impurity is Ti, which creates very shallow electron traps (E_c − 0.11/0.17 eV) in 4H-SiC [183]. The typical impurity density in CVD-grown 4H-SiC epitaxial layers is about $(1–5) \times 10^{13}$ cm^{-3} for B and $(0.5–5) \times 10^{12}$ cm^{-3} for Ti.

The density of $Z_{1/2}$ center can be controlled by growth conditions. The most pronounced dependence is the decrease of the defect density with the increase of the C/Si ratio [184,185]. This indicates that the center likely contains a C vacancy, and this was recently confirmed by EPR measurements [186,187]. Careful optimization of the growth conditions including decreasing the growth temperature and increasing the C/Si ratio allowed for epitaxial growth with deep trap densities ($Z_{1/2}$ and $EH_{6/7}$) below 5×10^{12} cm^{-3} and increase of the carrier lifetime to 2–5 μs [118,120,188]. Further increase of the lifetime with keeping good surface morphology is difficult during the epitaxy. On the other hand, the post-growth treatment including C ion implantation (and subsequent annealing) [189,190] and thermal oxidation [191,192] proved effective for lifetime enhancement. By optimization of these processes, a "$Z_{1/2}$–center-free" region can be extended to more than 150 μm from the surface, and long carrier lifetimes over 30 μs have been achieved [193].

4.4. Frontiers of SiC epitaxy

4.4.1. Fast epitaxy of SiC

Fast epitaxial growth of SiC is beneficial to increase the throughput, and thereby decrease the cost, of an epitaxial process. This is especially true for fabrication of very high-voltage (>5 kV) devices, because the standard growth rate for mass production is 5–15 μm/h at present. The growth rate in SiC CVD can, in principle, be increased by increasing the supply of precursors. In fast epitaxy of SiC, however, a few unique problems arise. Such problems include (i) homogeneous nucleation of Si clusters in the gas phase and (ii) unstable step-flow growth on the growing surface.

In conventional CVD of SiC, SiH_4 and C_3H_8 (or C_2H_4) are employed as the precursors. Hydrocarbon molecules are rather stable and start to decompose at relatively high temperatures, above 1000–1200 °C, whereas the decomposition temperature of SiH_4 molecules is much lower (around 400 °C). When the SiH_4 partial pressure becomes high to increase the growth rate in SiC CVD at 1550–1700 °C, the SiH_4 molecules introduced into a hot zone immediately decompose and homogeneous nucleation (nSi → Si$_n$: Si-cluster formation) takes place. Because Si clusters can grow into a significant size (in excess of several nm), such Si clusters have detrimental impacts on atomic-level epitaxial growth of SiC. Even if Si clusters are not formed in the gas phase, the supersaturation on the growing surface must be minimized to ensure stable step-flow growth. High supersaturation causes unwanted nucleation of a 3C-SiC phase on {0001} terraces or defect sites, which is also detrimental to high-quality homoepitaxy of 4H-SiC.

To overcome homogeneous nucleation in the gas phase, (i) decrease of the growth pressure [160,194,195], (ii) use of chlorine (Cl)-based chemistry [107,108,196–198], and (iii) increase of growth temperature [81,199] are effective. In the first approach (decrease of growth pressure), the partial pressure of SiH_4 is reduced, which naturally hinders Si-cluster formation in the gas phase. As a result, more Si species are supplied onto the substrate surface, with minimal loss in the gas phase, resulting in a higher growth rate and improved morphology as the growth pressure is decreased. In fact, remarkable improvement of surface morphology in fast epitaxy of 4H-SiC(0001) has been attained, with growth rates of 50–250 μm/h.

The second approach (Cl-based chemistry) can be more elegant, because the chemistry is more suitable for fast epitaxy. The larger bonding energy of Si-Cl compared with that of Si-H and Si-Si means that appropriate precursors containing Cl greatly suppress formation of Si clusters. Such precursors include $SiHCl_3$ [200], SiH_2Cl_2 [201], and SiH_3Cl [202]. These precursors do not decompose below 800 °C (cf. 400 °C for SiH_4) and start to form $SiCl_x$ (mainly $x = 2$) above about 1000 °C in a H_2 ambient [203]. CH_3Cl [204] and $SiCH_3Cl_3$ [205,206] have also been used successfully for fast epitaxy of SiC. Another way is to simply add HCl into a conventional SiH_4-based chemistry [196,197,207]. By using the Cl-based chemistry, high growth rates of 50–170 μm/h have been reported, while maintaining good morphology. The

optimum Cl/Si ratio is dependent on the precursors and growth temperature, and is typically 1.5–3 (or 3–5 in the case of HCl addition). Incorporation of Cl atoms or generation of Cl-related deep levels has not been observed in the epitaxial layers. Cl-based CVD of SiC has been reviewed in literature [107,108].

The extent of step bunching and other morphological instabilities in fast epitaxy of 4H-SiC has been considerably reduced by recent process optimization. However, the density of in-grown SFs tends to increase when the growth rate is increased. Thus, nucleation of in-grown SFs can be an inherent challenge in fast epitaxy of SiC.

4.4.2. *Homoepitaxy on nearly on-axis growth*

A major driving force for developing SiC homoepitaxy on nearly on-axis {0001} substrates is elimination of BPDs in the epitaxial layers. The wafer cost may be reduced by using nearly on-axis {0001} wafers since the SiC boules are usually grown on on-axis {0001}. It is, however, not easy to achieve stable step-flow growth if the substrate's off-angle becomes smaller than 2°, as shown in Fig. 11. The disturbance or instability of step-flow growth can result in nucleation of 3C-SiC and/or stacking fault generation.

In an early study [111], homoepitaxy of 6H-SiC on 0.2° off-axis 6H-SiC(0001) was demonstrated by removal of defective sites by appropriate *in-situ* HCl/H_2 etching. This process was refined, and relatively large-area homoepitaxy of 6H-SiC on nearly on-axis (0001) substrates was achieved under Si-rich conditions [208]. CVD growth under Si-rich (low C/Si ratio) conditions is a common approach in SiC homoepitaxy on {0001} substrates with low off-angles, since the Si-rich conditions increase the surface migration length of adsorbed species, and thus result in low supersaturation on the growing surface [209]. The major drawback of CVD under Si-rich conditions is greater N incorporation in SiC epitaxial layers. Homoepitaxy of dislocation-free 4H- and 6H-SiC(0001) by using small (0.4 mm × 0.4 mm) mesa structures is also reported [210]. More recently, it was found that 4H-SiC without 3C-SiC inclusions can be grown by using nearly on-axis (about 0.3° off-axis) 4H-SiC($000\bar{1}$) [128,211]. Although the reasons for this success are unclear at present, the difference in the surface energy was suggested (this is also the reason why bulk 4H-SiC can be easily grown on a ($000\bar{1}$) seed by sublimation) [46]. Homoepitaxy on nearly on-axis 4H-SiC(0001) has been significantly improved by adopting *in-situ* etching with SiH_4 addition prior to CVD growth [212,213]. Homoepitaxy of 4H-SiC with good morphology is attained on 0.3° off-axis ($000\bar{1}$) and 0.79° off-axis (0001) with a growth rate of about 5 μm/h at 1600 °C. The use of Cl-based chemistry is also effective for 4H-SiC homoepitaxy on nearly on-axis (0001) substrates, and homoepitaxy at high growth rates over 100 μm/h was realized [214,215]. However, the surface morphology and reproducibility are still challenges in 4H-SiC epitaxy on nearly on-axis {0001}. Homoepitaxy on nearly on-axis {0001} will become more difficult when TSDs in SiC wafers are almost eliminated in the future.

5. Summary

Bulk and epitaxial growth of SiC, mainly 4H-SiC, has been reviewed. Regarding bulk growth of SiC, the seeded sublimation method is the most mature, and is the choice for SiC wafer production because of superior process stability and cost. Large SiC wafers with a relatively low dislocation density of 3000–5000 cm^{-2} or lower have been produced (<100 cm^{-2} in the research level). However, understanding of defect generation and reduction in SiC is still limited. Further refinement of growth simulation is required to assist in controlling the thermal stress and surface stoichiometry to allow dislocation engineering in SiC. In recent years, alternative growth techniques such as solution growth and HTCVD have exhibited much potential of high quality and high purity, respectively.

Basic homoepitaxial growth technologies of hexagonal SiC by CVD have been established. Polytype replication in epitaxial layers is realized by step-flow growth on off-axis SiC{0001} substrates. Growth of very pure SiC with a net doping density below 1×10^{13} cm^{-3} and wide-range control of both n-type (10^{14}–10^{19} cm^{-3}) and p-type (10^{14}–10^{20} cm^{-3}) doping has been achieved using the site-competition effect and optimization of growth conditions. Though behavior of extended defects during SiC epitaxial growth has been studied in detail, further reduction in defects and physical understanding of defect behavior are required. In particular, BPDs and macroscopic defects induced by epitaxial growth must be completely eliminated to ensure the performance and reliability of large-area SiC devices. The density of deep levels in as-grown SiC epitaxial layers is rather low, in the range of $(0.3–2) \times 10^{13}$ cm^{-3}. Recent advances in SiC epitaxial technology include high uniformity in multi-wafer CVD systems, very fast (>100 μm/h) growth and homoepitaxial growth on nearly on-axis SiC{0001} substrates.

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