



# ZC702 Built-In Self Test Flash Application

June 2014

XTP180

# Revision History

Date	Version	Description
06/09/14	10.0	Recompiled for 2014.2.
04/16/14	9.0	Recompiled for 2014.1. AR58941 fixed. Added AR60358.
12/18/13	8.0	Recompiled for 2013.4. Added AR58941.
11/18/13	7.1	Updated with patch from AR58347 in place of AR58278.
10/23/13	7.0	Recompiled for 2013.3. Converted to IPI. Added AR58278.
06/19/13	6.0	Recompiled for Vivado 2013.2. AR55581 and AR55431 fixed.
04/18/13	5.2	Added AR55581.
04/16/13	5.1	Added AR55431, AR54225. Removed AR51207.
04/03/13	5.0	Recompiled for 14.5. AR53593 fixed. AR53306 fixed.
04/16/13	4.1	Added AR52143
12/18/12	4.0	Recompiled for 14.4. Added AR53593. Added AR53306.
10/23/12	3.0	Recompiled for 14.3. Added AR51807.
07/25/12	2.0	Recompiled for 14.2. Added AR51207.
05/25/12	1.0	Initial version for 14.1.

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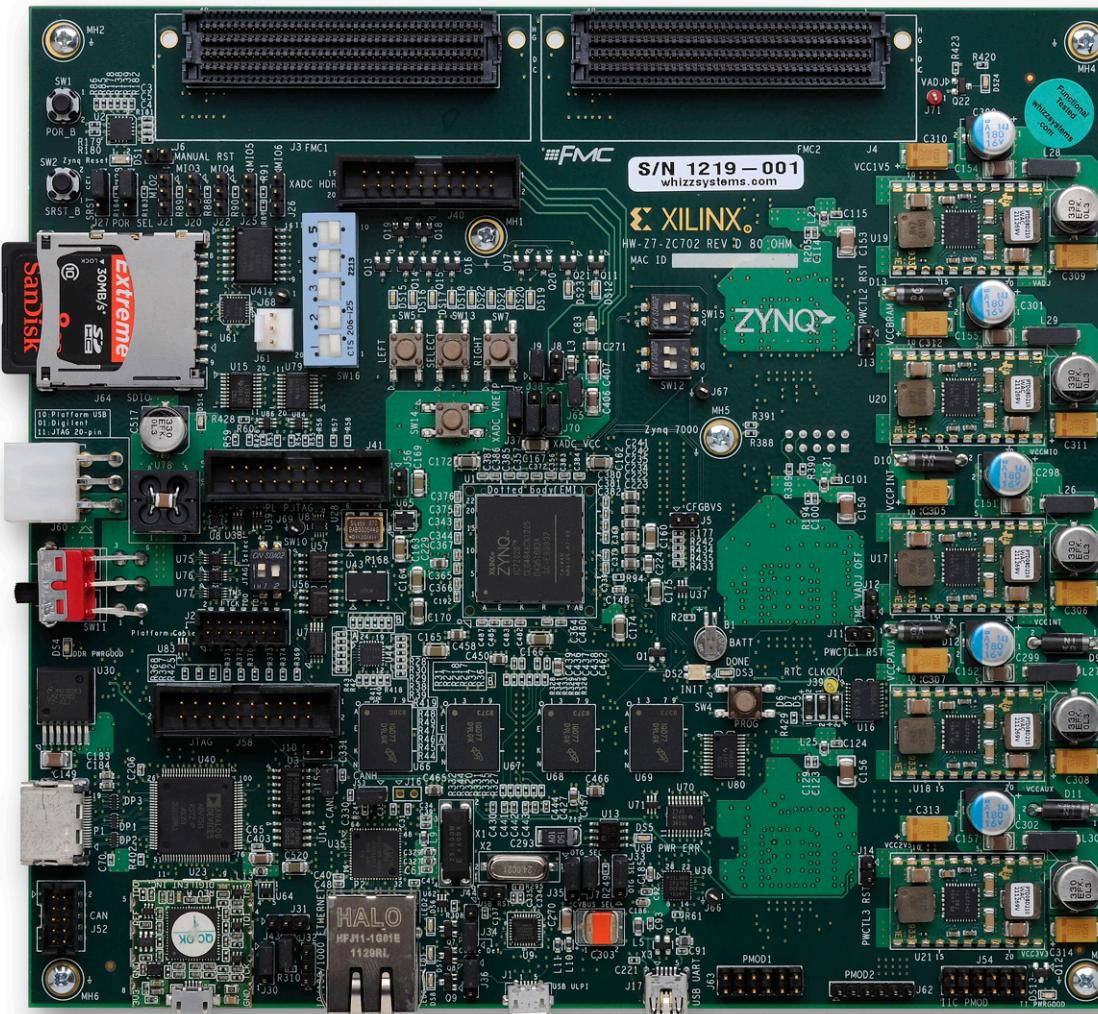
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# Overview

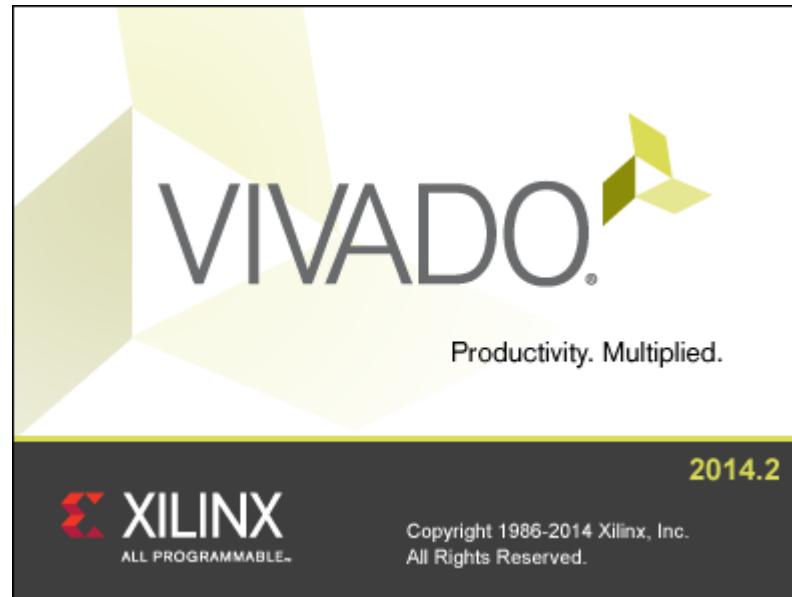
- **Xilinx ZC702 Board**
- **Software Requirements**
- **ZC702 Setup**
- **ZC702 BIST (Built-In Self Test)**
  - Run the BIST Design
  - Run the USB Design
  - Run the LwIP Ethernet Design
- **Compile ZC702 BIST Design**
  - Creating a BOOT Image
  - Programming the ZC702 QSPI
  - Run the USB Design from SDK
  - Run the LwIP Ethernet Design
- **References**

# ZC702 Board



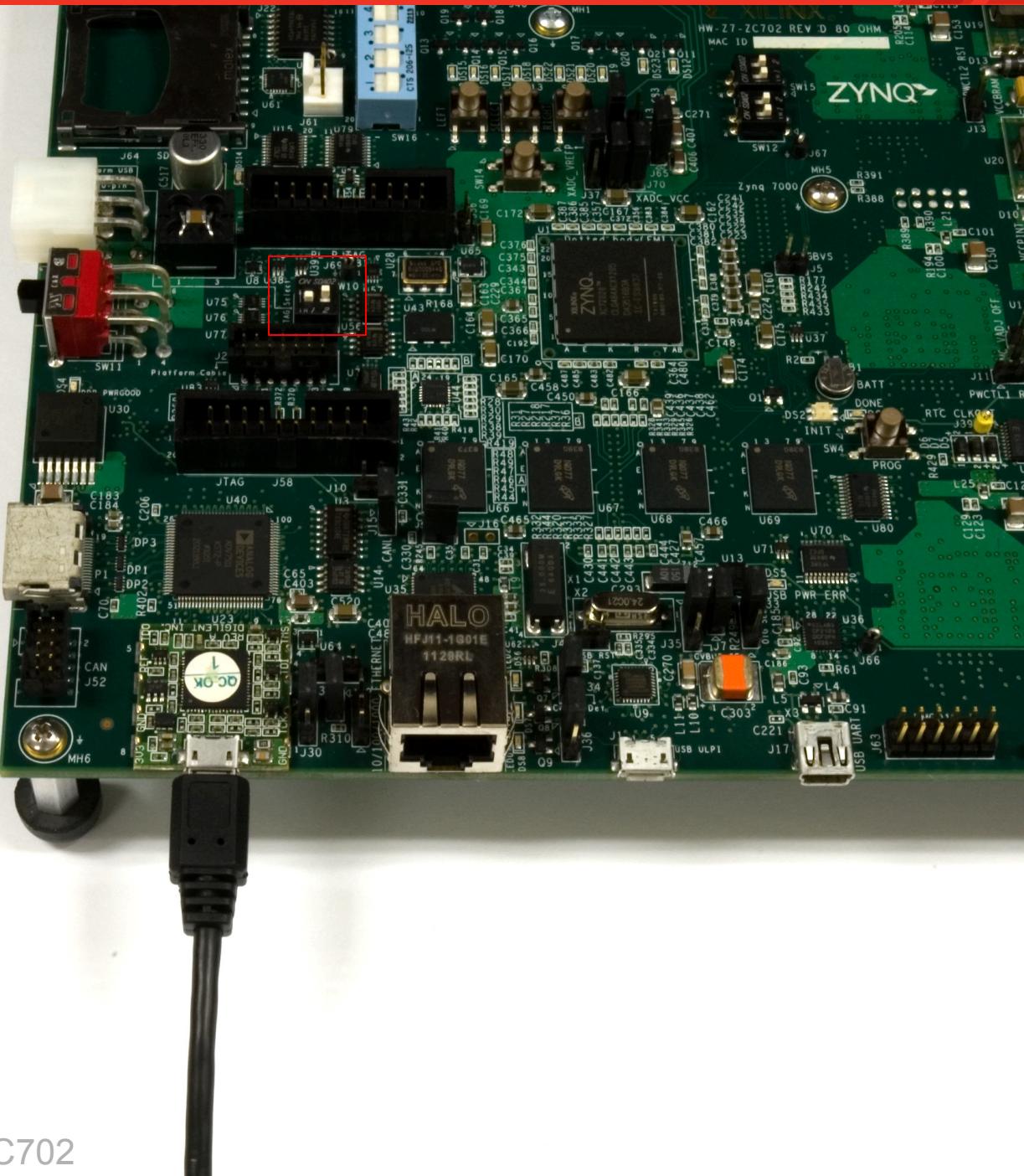
# Vivado Software Requirements

- Xilinx Vivado Design Suite 2014.2, Design Edition + SDK
  - Combined installer



# ZC702 Setup

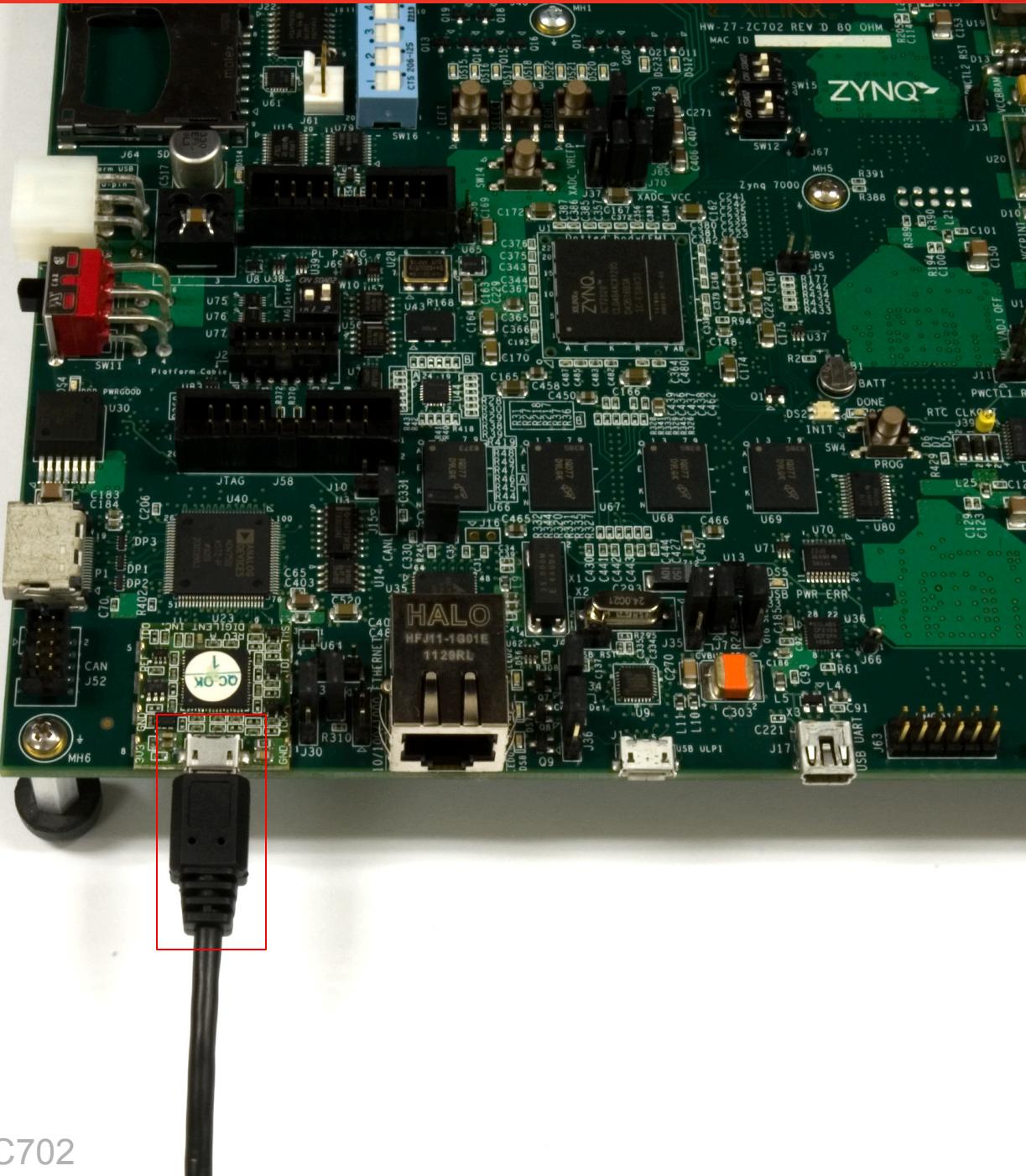
- Set the JTAG Select Switch, SW10, to 01
  - If using a Platform Cable USB (II) JTAG Cable, set SW10 to 10



**Note:** Presentation applies to the ZC702

# ZC702 Setup

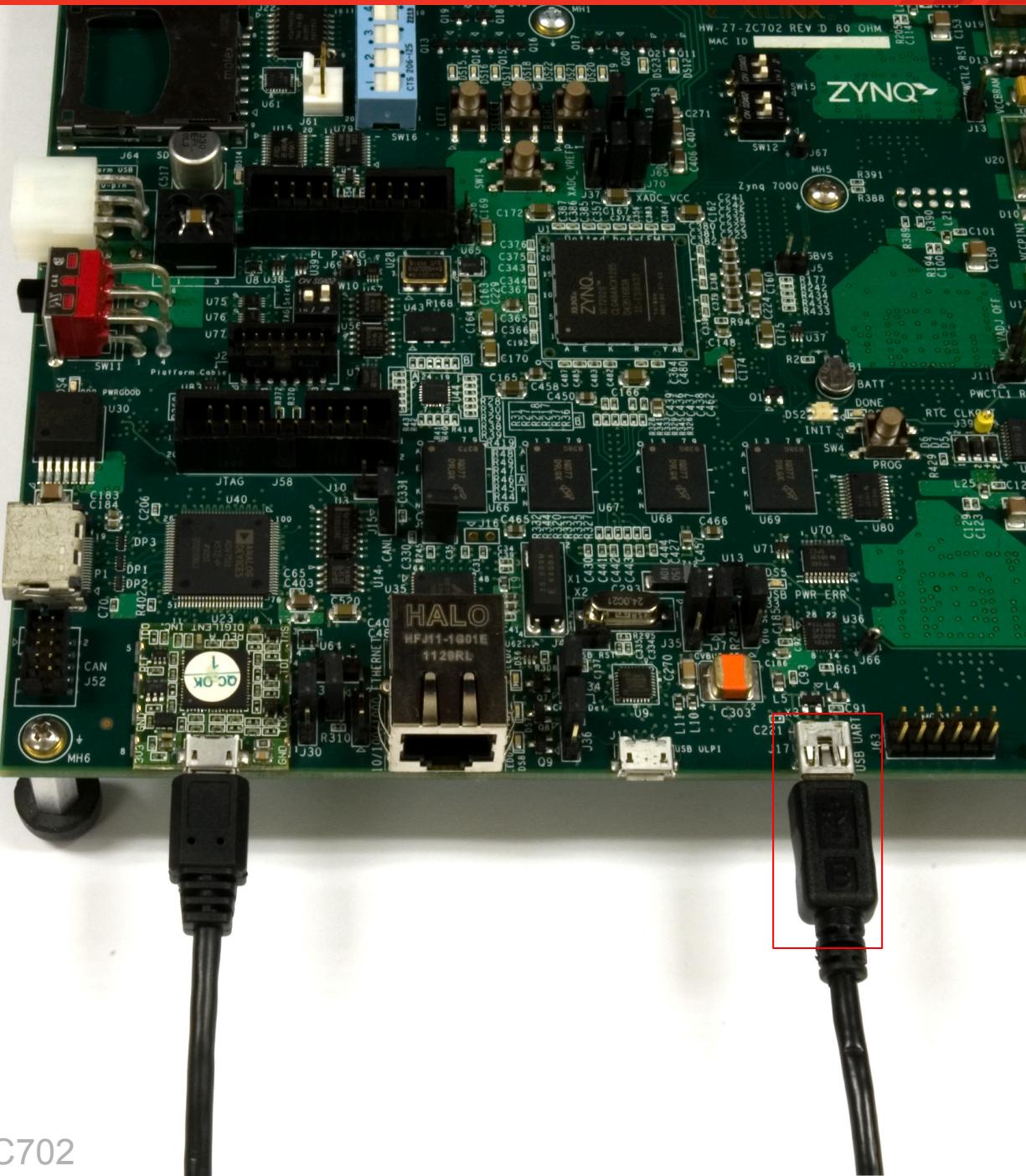
- ▶ Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the ZC702 board
  - Connect this cable to your PC



Note: Presentation applies to the ZC702

# ZC702 Setup

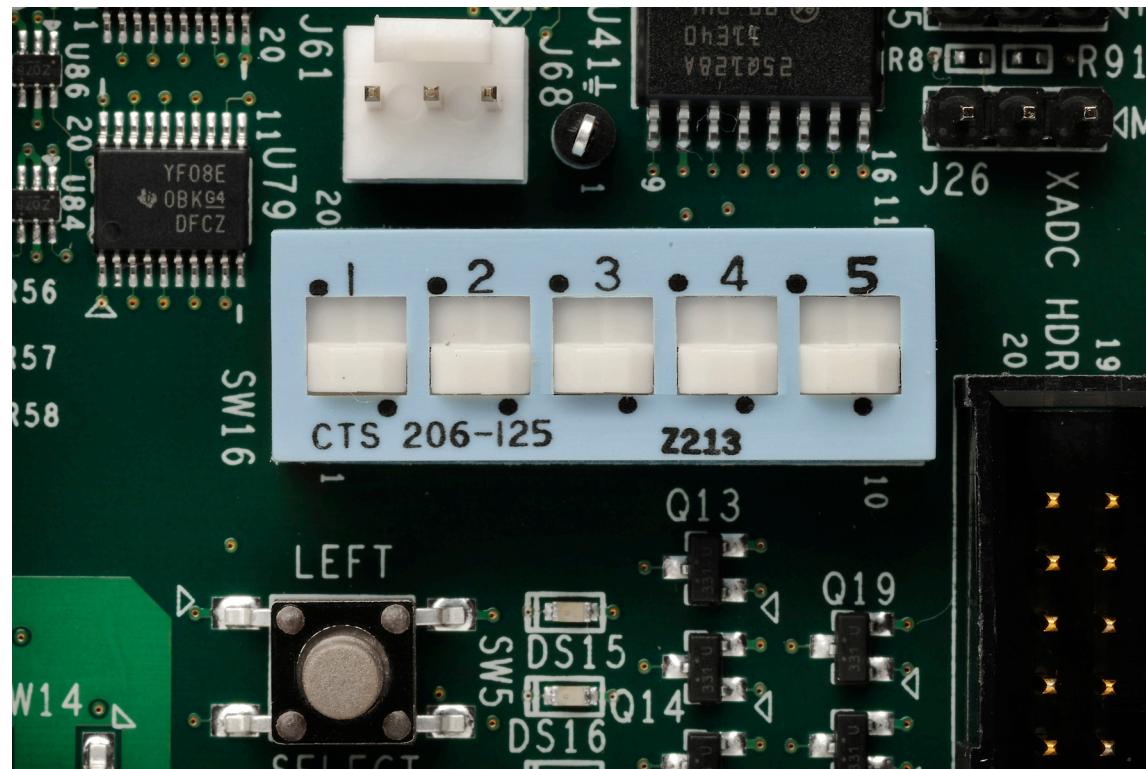
- ▶ Connect a USB Type-A to Mini-B cable to the USB UART connector on the ZC702 board
  - Connect this cable to your PC



# ZC702 Setup

## ► Set SW16 DIP Switches to 00000

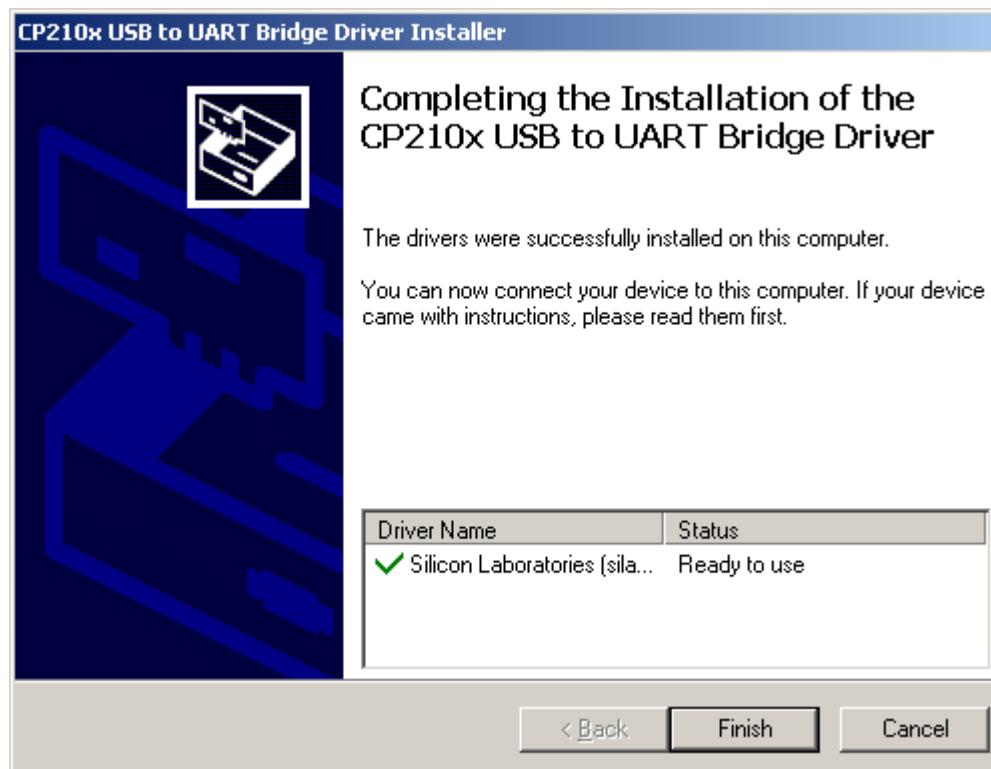
- Power on the ZC702 board for UART Drivers Installation



# ZC702 Setup

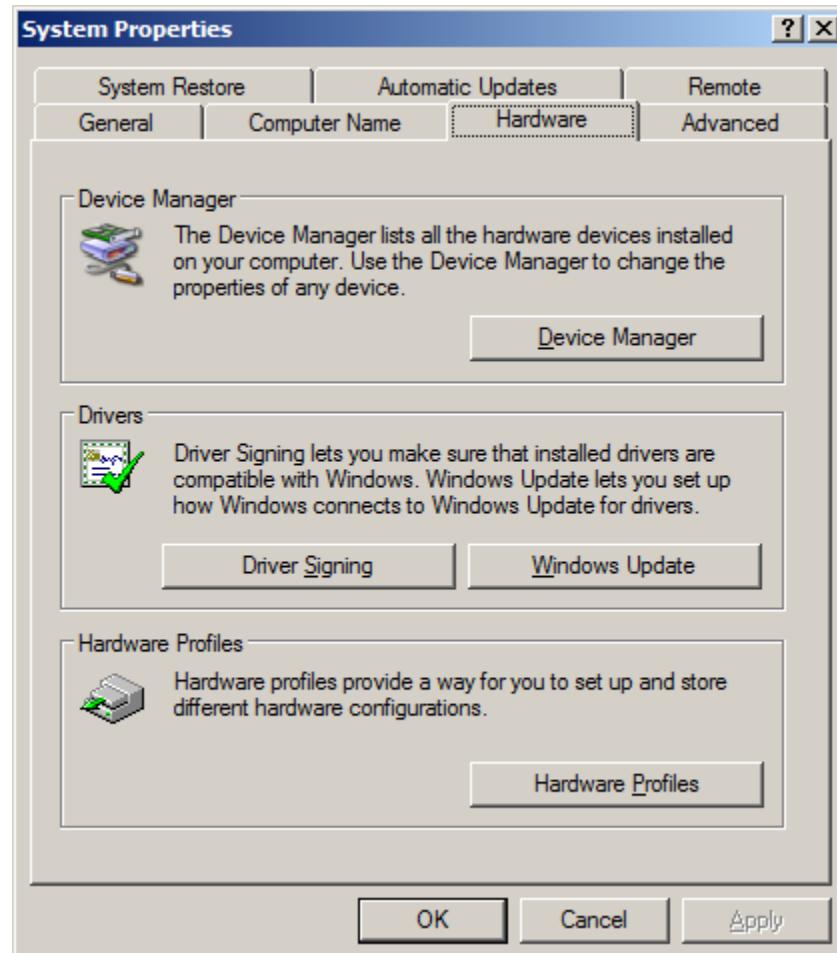
## ➤ Install USB UART Drivers

- Refer to [UG1033](#) for details on installing the USB to UART Drivers



# ZC702 Setup

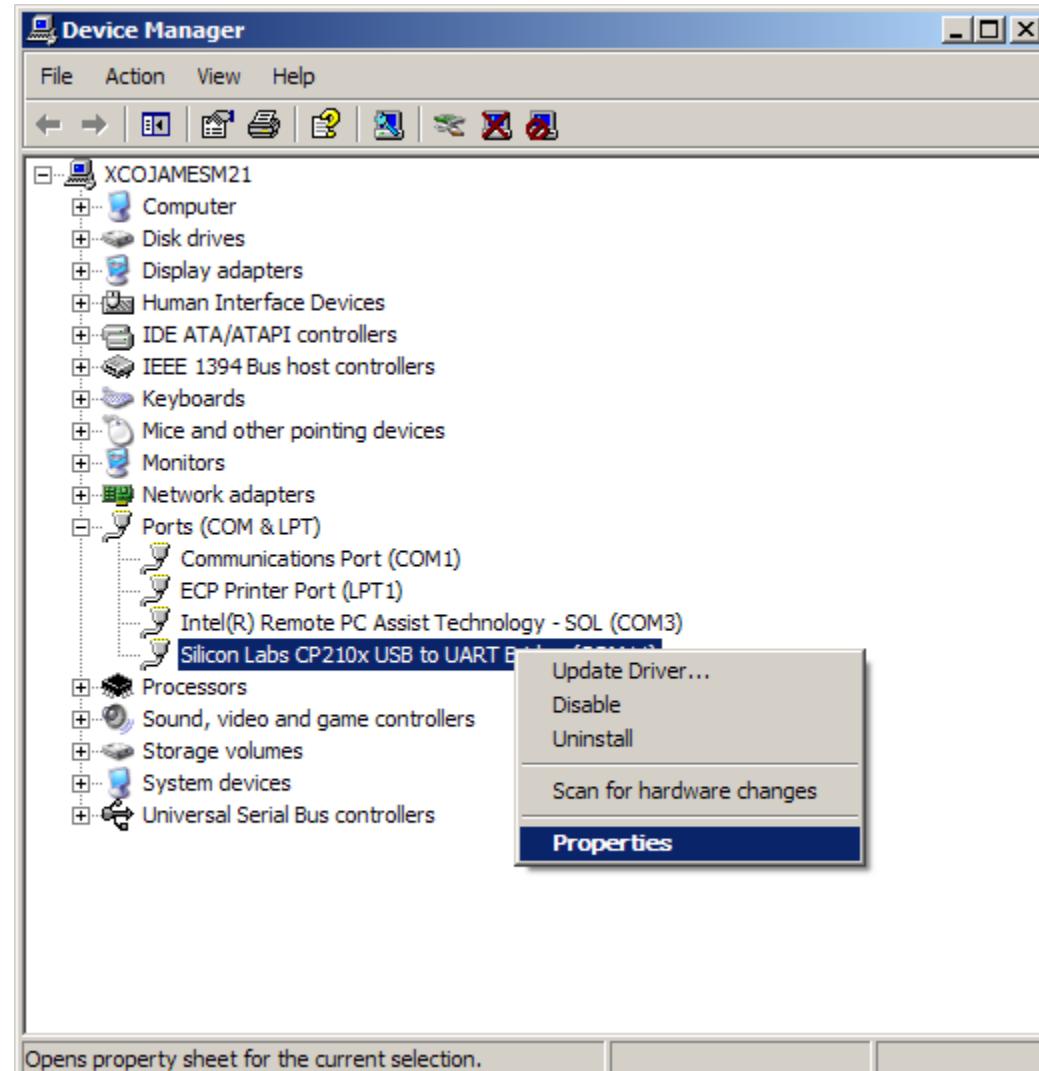
- Reboot your PC if necessary
- Right-click on My Computer and select Properties
  - Select the Hardware tab
  - Click on Device Manager



# ZC702 Setup

## ► Expand the Ports Hardware

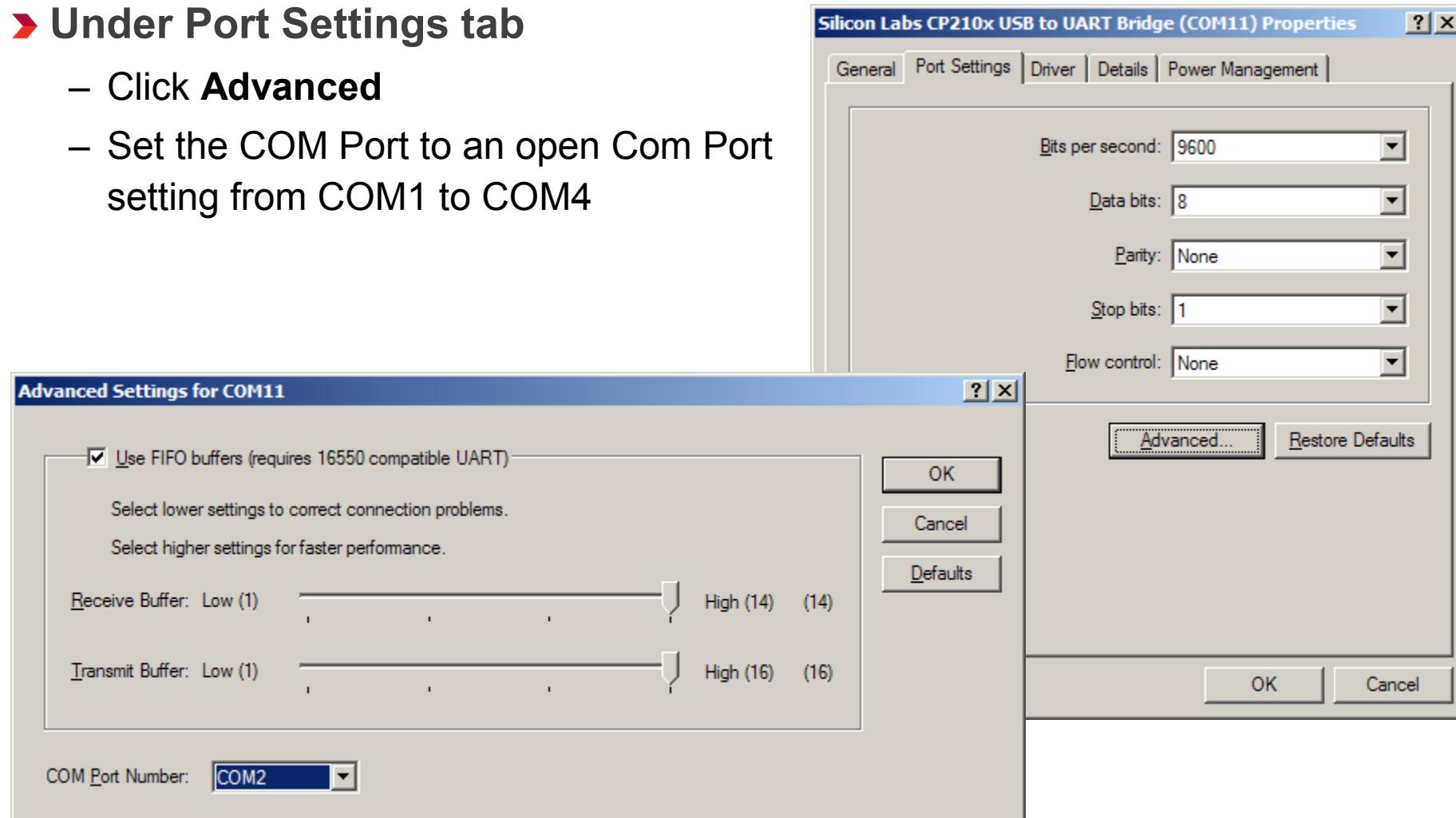
- Right-click on **Silicon Labs CP210x USB to UART Bridge** and select Properties



# ZC702 Setup

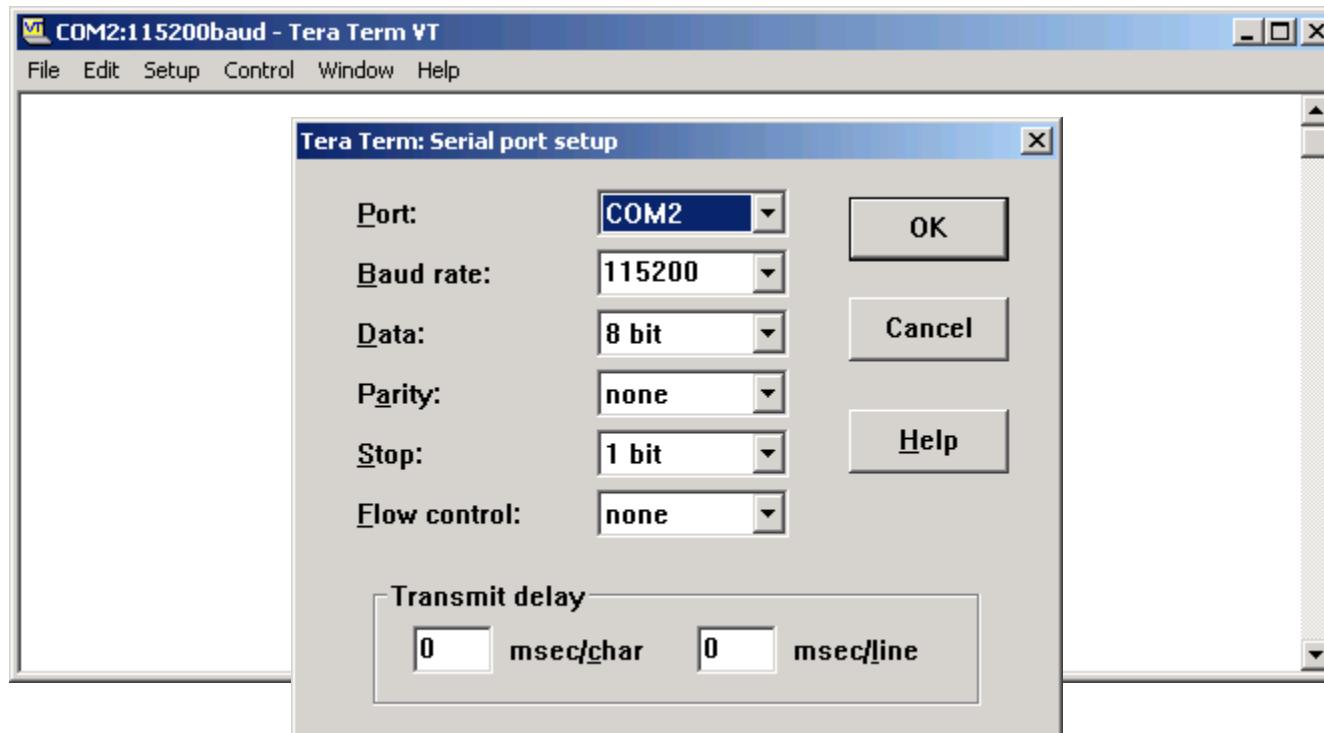
## ► Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



# ZC702 Setup

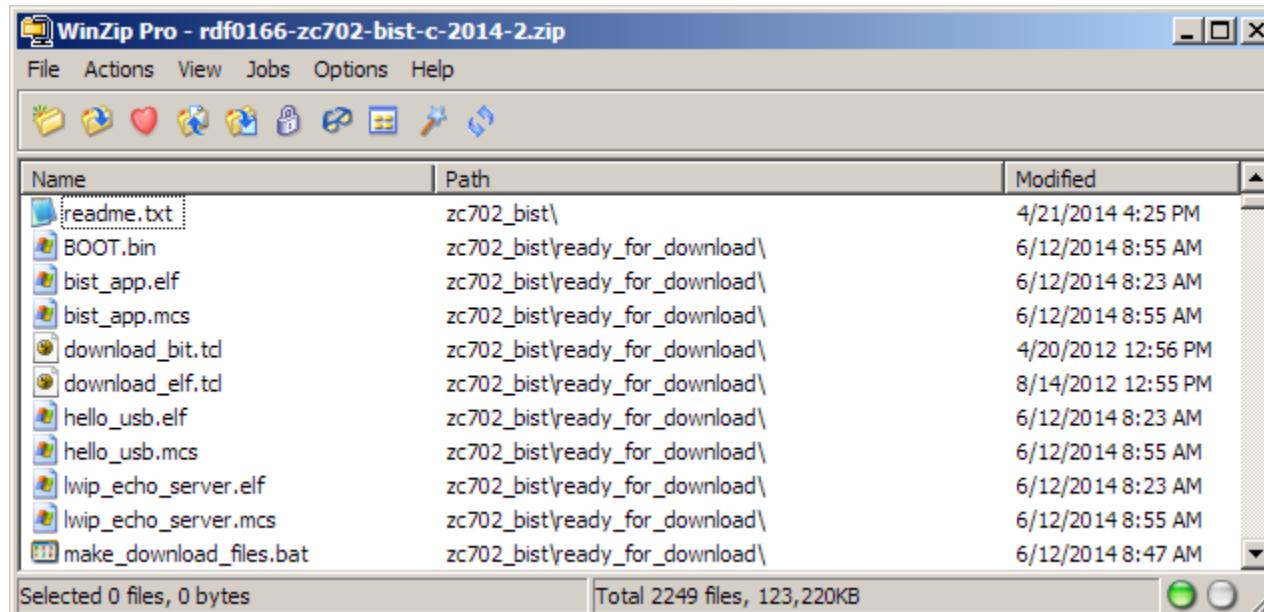
- Refer to [UG1036](#) regarding Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
  - Select your USB Com Port
  - Set the baud to **115200**



# ZC702 Setup

## ► Unzip the RDF0166 - ZC702 BIST Design Files (2014.2 C) zip file

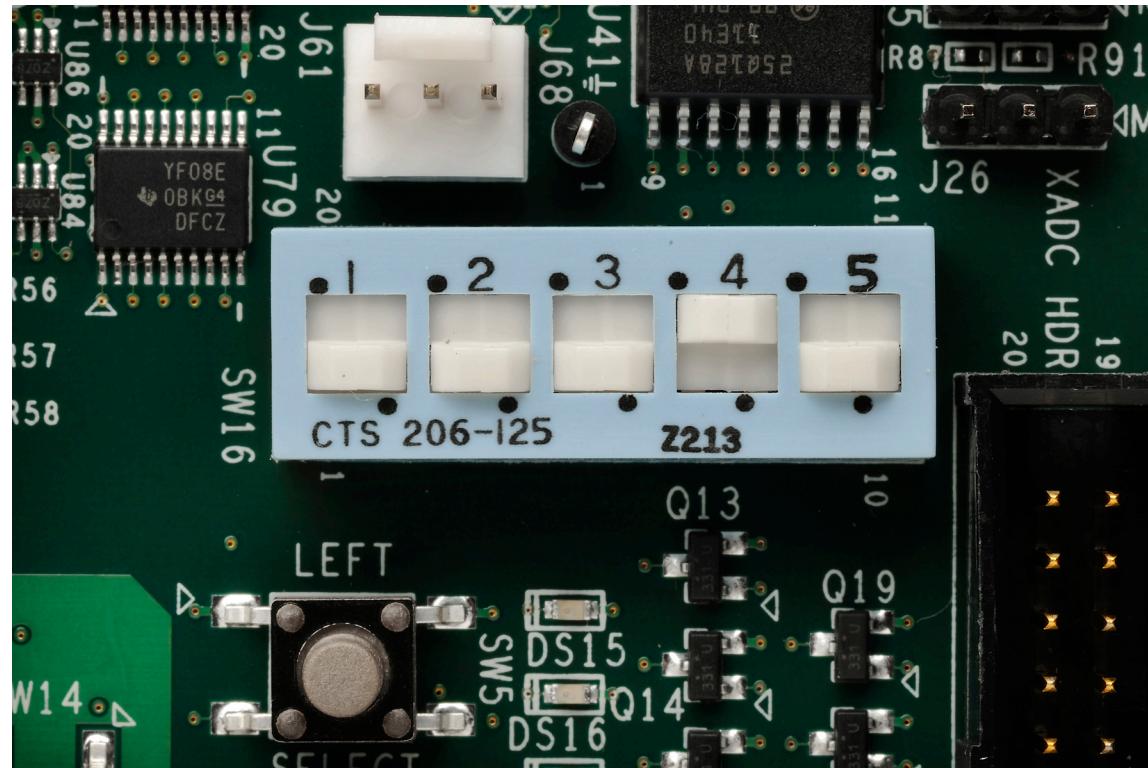
- Available through <http://www.xilinx.com/zc702>
- It is recommended to unzip these design files to **C:\** for SDK compatibility



# ZC702 Setup

## ► Set the SW16 DIP switches to boot from QSPI: 00010

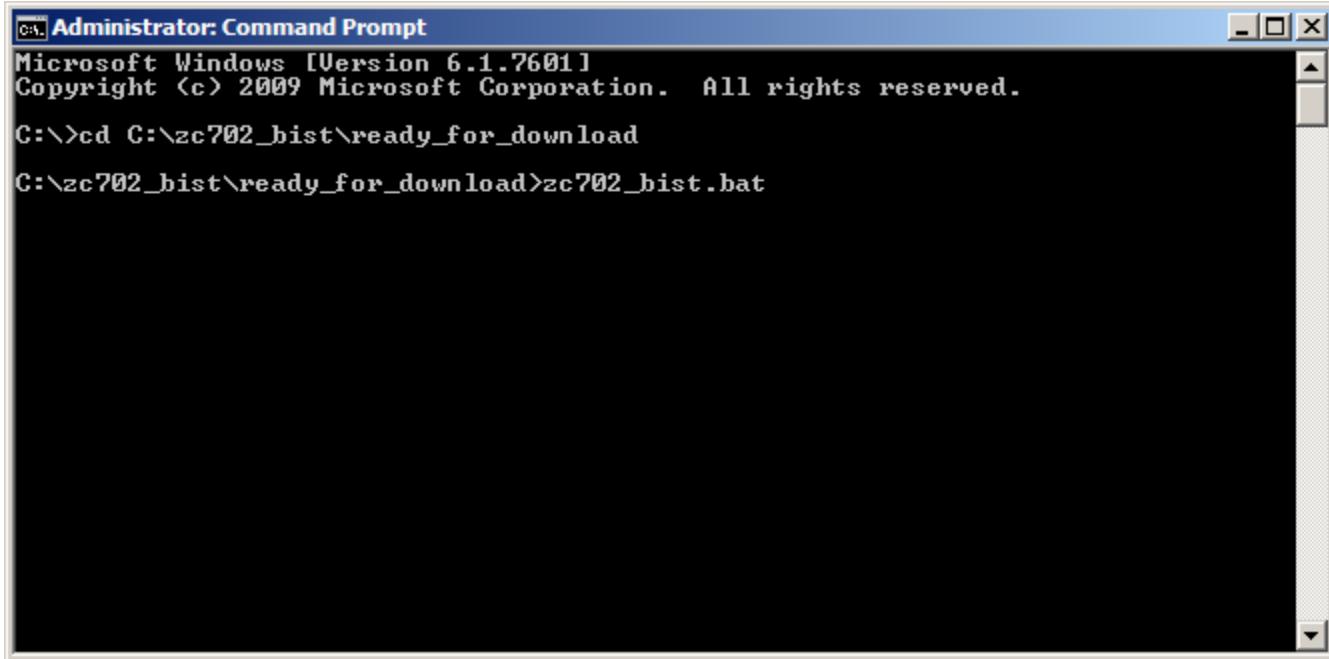
- The ZC702 QSPI comes preloaded with the BIST Application
- Cycle power to start the BIST Application



# ZC702 BIST

- BIST can also be loaded from the command line
- To do this, open a Windows prompt and type:

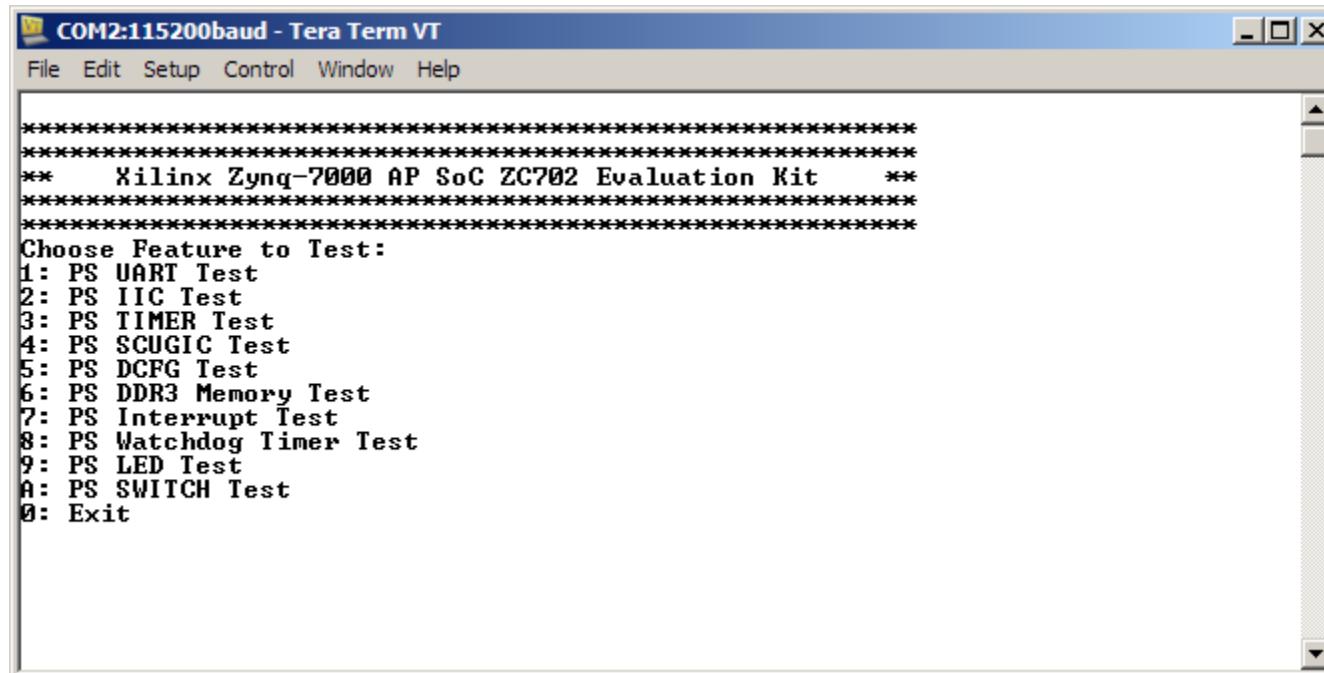
```
cd C:\zc702_bist\ready_for_download  
zc702_bist.bat
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window title bar includes the text "Administrator: Command Prompt" and the standard window control buttons (minimize, maximize, close). The main area of the window displays the following text:  
Microsoft Windows [Version 6.1.7601]  
Copyright © 2009 Microsoft Corporation. All rights reserved.  
C:\>cd C:\zc702\_bist\ready\_for\_download  
C:\zc702\_bist\ready\_for\_download>zc702\_bist.bat

# ZC702 BIST

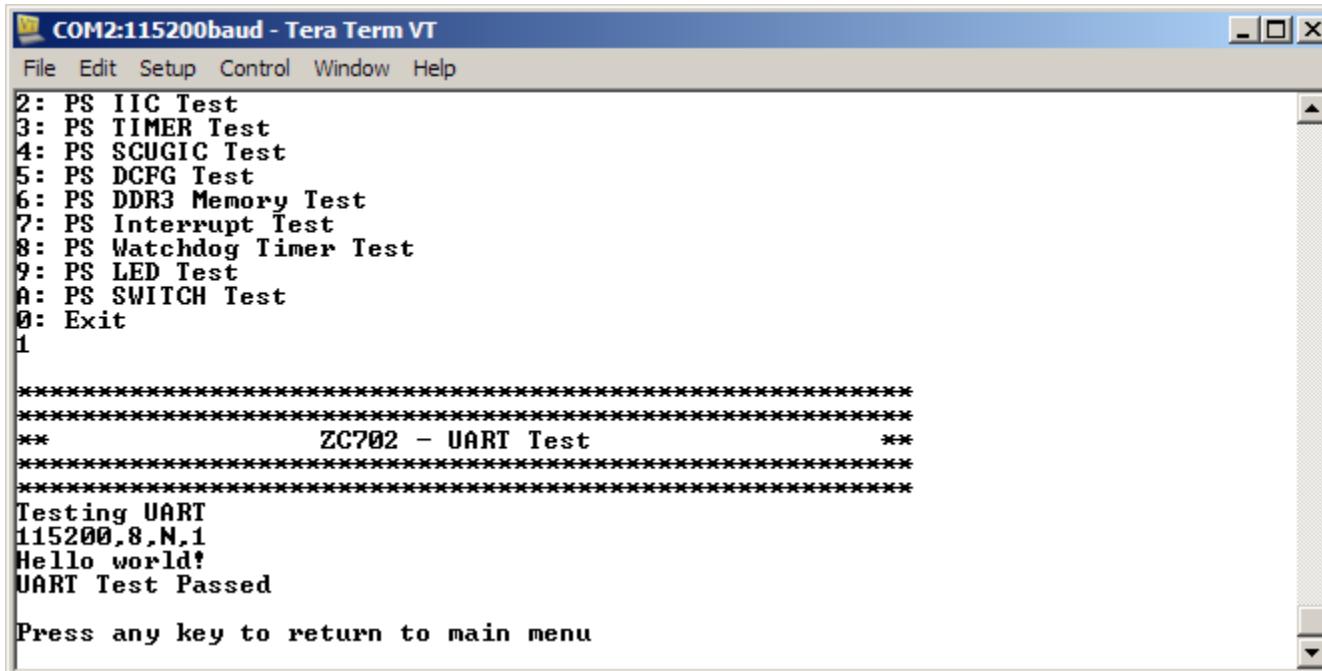
## ► View initial BIST screen



# ZC702 BIST

## ➤ UART Test

- Type “1” to start the PS UART Test
- After each test, press any key to return to the main menu



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main text area displays a test menu:

```
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
1
```

Following the menu, the text "\*\*\*\*\*" appears twice, followed by "ZC702 - UART Test" centered between two double asterisks. Then, the text "\*\*\*\*\*" appears again. Below this, the output of the test is shown:

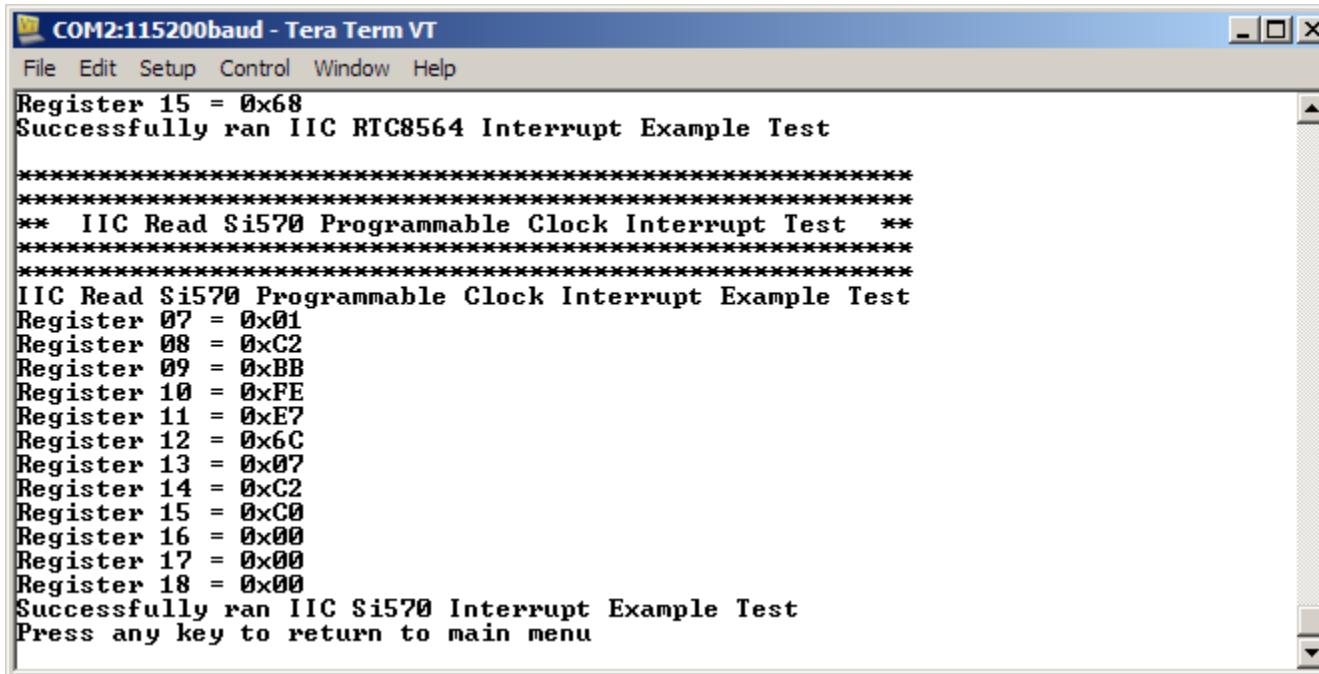
```
Testing UART
115200,8,N,1
Hello world!
UART Test Passed
```

At the bottom of the window, the text "Press any key to return to main menu" is displayed.

# ZC702 BIST

## ► IIC Test

- Type **2** to begin PS IIC Tests
- Completes four different IIC tests



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window contains the following text output from an IIC test script:

```
Register 15 = 0x68
Successfully ran IIC RTC8564 Interrupt Example Test
*****
** IIC Read Si570 Programmable Clock Interrupt Test **
*****
IIC Read Si570 Programmable Clock Interrupt Example Test
Register 07 = 0x01
Register 08 = 0xC2
Register 09 = 0xBB
Register 10 = 0xFE
Register 11 = 0xE7
Register 12 = 0x6C
Register 13 = 0x07
Register 14 = 0xC2
Register 15 = 0xC0
Register 16 = 0x00
Register 17 = 0x00
Register 18 = 0x00
Successfully ran IIC Si570 Interrupt Example Test
Press any key to return to main menu
```

# ZC702 BIST

## ➤ Timer Test

- Type 3 to begin PS Timer Test

The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window has a menu bar with File, Edit, Setup, Control, Window, and Help. The main text area displays the following sequence of commands and output:

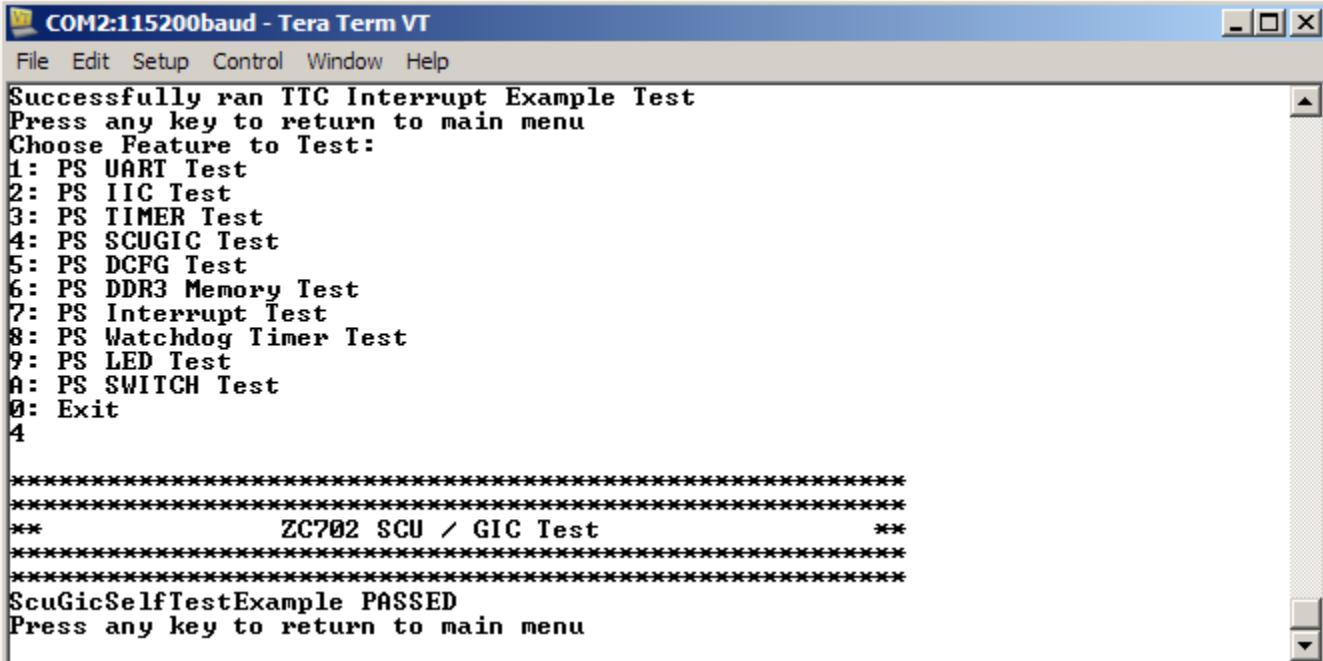
```
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
3

*****
**          ZC702 - Timer Test          **
*****
TTC Interrupt Example Test
Successfully ran TTC Interrupt Example Test
Press any key to return to main menu
```

# ZC702 BIST

## ► SCU / GIC Test

- Type 4 to begin SCU / GIC Test



```
COM2:115200baud - Tera Term VT
File Edit Setup Control Window Help
Successfully ran TTC Interrupt Example Test
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
4

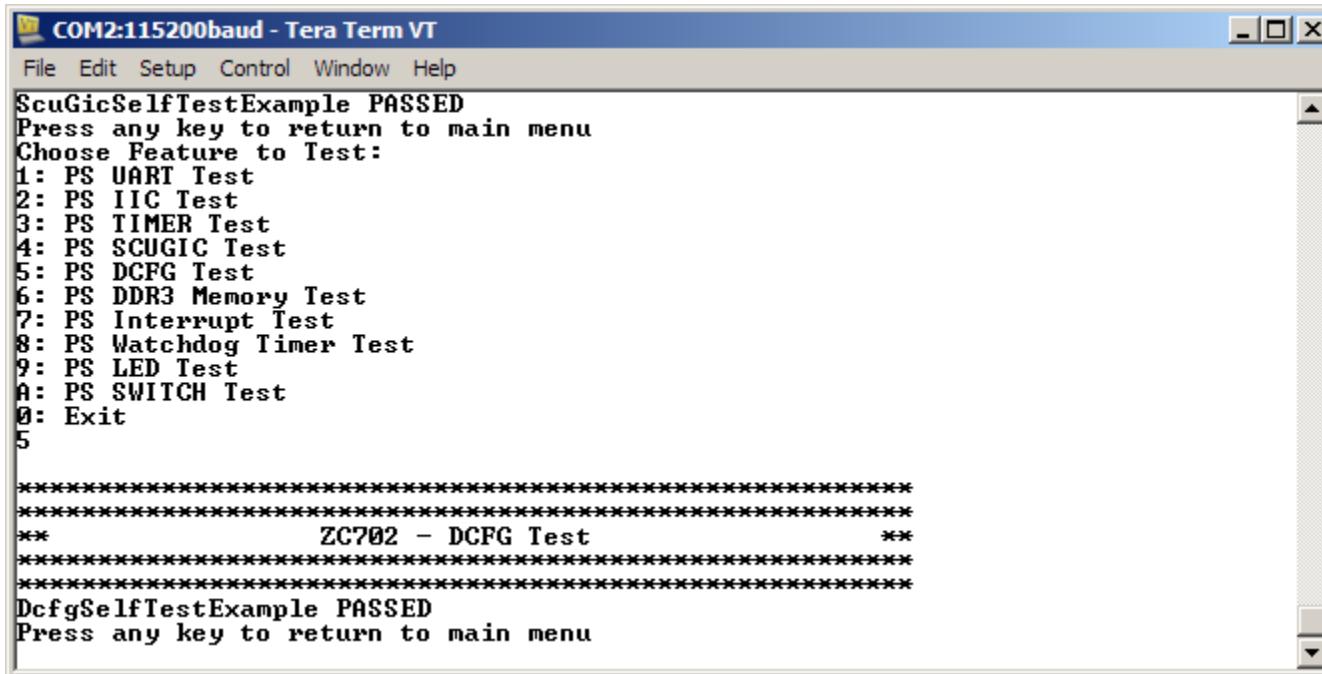
*****
**          ZC702 SCU / GIC Test      **
*****
ScuGicSelfTestExample PASSED
Press any key to return to main menu
```

**Note:** SCU / GIC means Snoop Control Unit / Generic Interrupt Controller

# ZC702 BIST

## ► DCFG Test

- Type **5** to begin Device Configuration Interface Test



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window contains the following text:

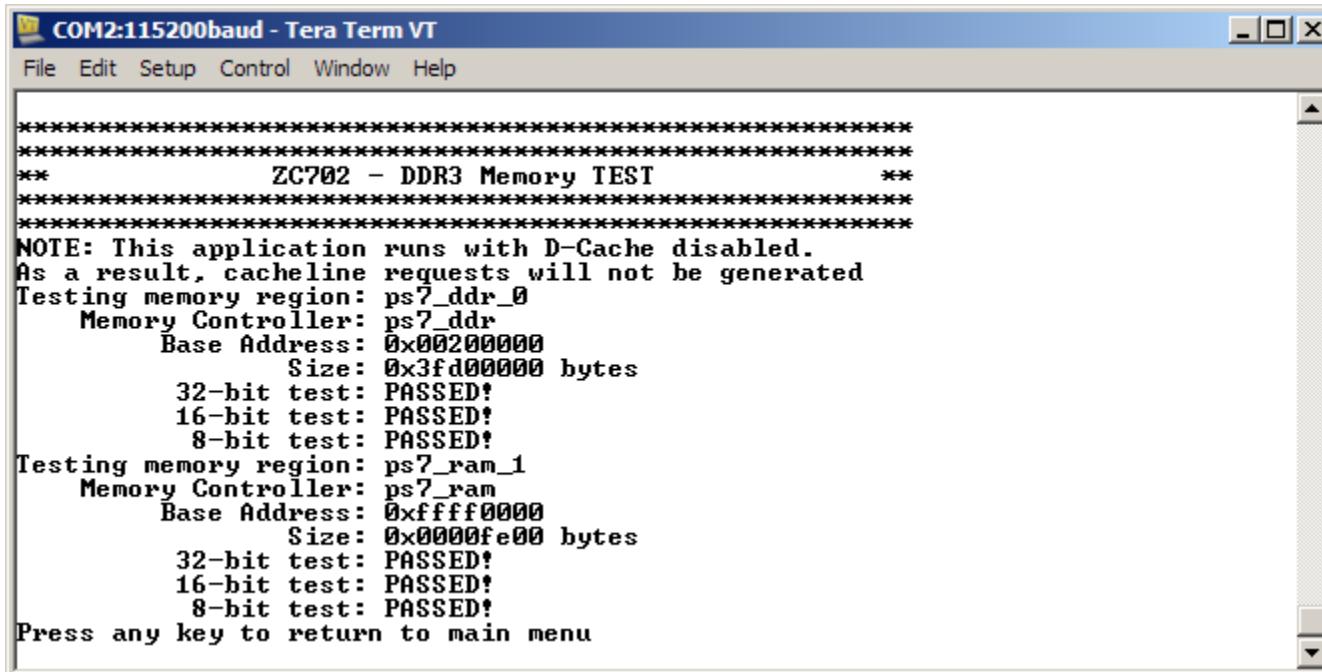
```
ScuGicSelfTestExample PASSED
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
5

*****
**          ZC702 - DCFG Test          **
*****
DcfgSelfTestExample PASSED
Press any key to return to main menu
```

# ZC702 BIST

## ➤ Memory Test

- Type **6** to begin PS DDR3 Memory Test



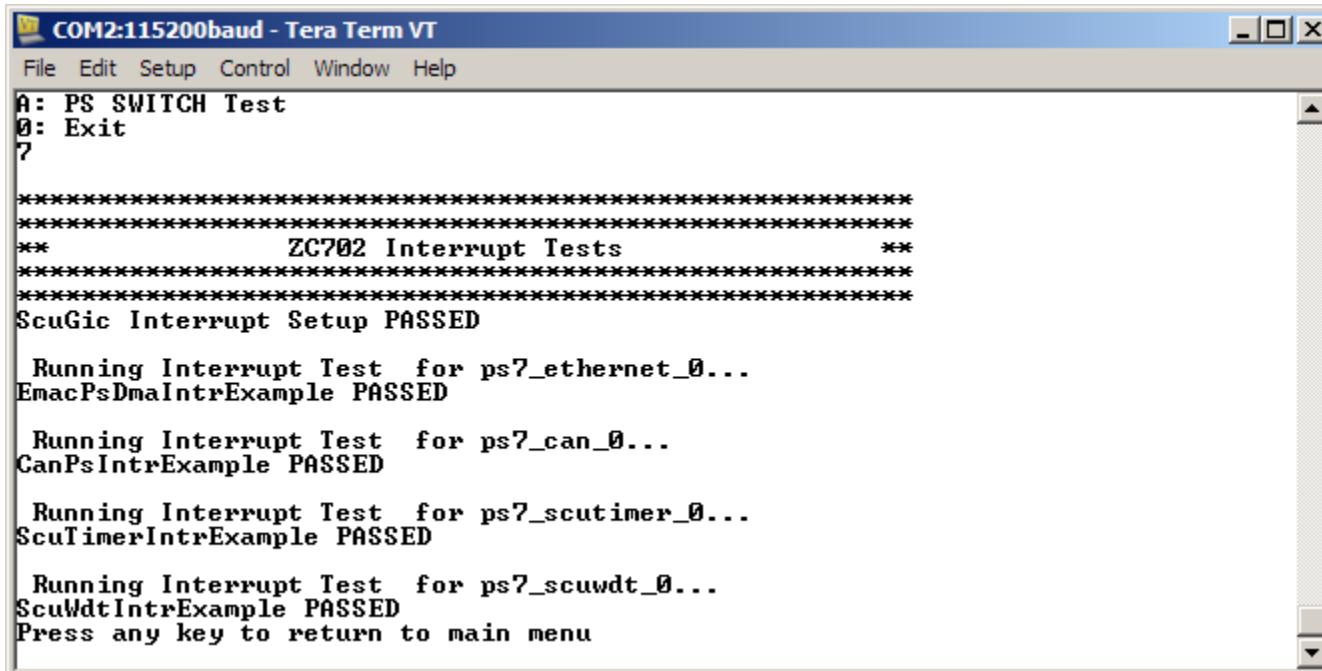
The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window displays the output of a memory test application. The output is as follows:

```
*****  
**          ZC702 - DDR3 Memory TEST      **  
*****  
NOTE: This application runs with D-Cache disabled.  
As a result, cacheline requests will not be generated  
Testing memory region: ps7_ddr_0  
    Memory Controller: ps7_ddr  
        Base Address: 0x00200000  
        Size: 0x3fd00000 bytes  
        32-bit test: PASSED!  
        16-bit test: PASSED!  
        8-bit test: PASSED!  
Testing memory region: ps7_ram_1  
    Memory Controller: ps7_ram  
        Base Address: 0xfffff0000  
        Size: 0x00000fe00 bytes  
        32-bit test: PASSED!  
        16-bit test: PASSED!  
        8-bit test: PASSED!  
Press any key to return to main menu
```

# ZC702 BIST

## ► Interrupt Test

- Type 7 to begin PS Interrupt Tests



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays the following text:

```
A: PS SWITCH Test
0: Exit
?

*****
**          ZC702 Interrupt Tests          **
*****
ScuGic Interrupt Setup PASSED

Running Interrupt Test for ps7_ethernet_0...
EmacPsDmaIntrExample PASSED

Running Interrupt Test for ps7_can_0...
CanPsIntrExample PASSED

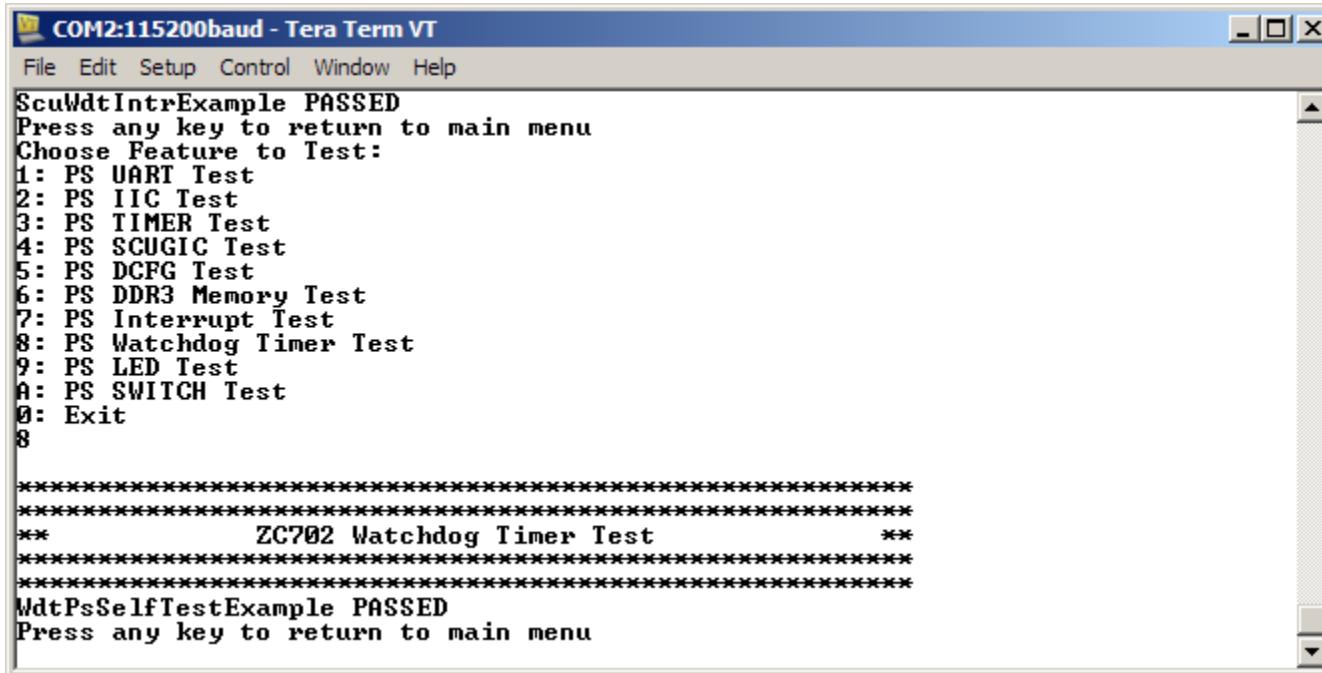
Running Interrupt Test for ps7_scutimer_0...
ScuTimerIntrExample PASSED

Running Interrupt Test for ps7_scuwdt_0...
ScuWdtIntrExample PASSED
Press any key to return to main menu
```

# ZC702 BIST

## ➤ Watchdog Timer Test

- Type 8 to begin PS Watchdog Timer Test



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window contains the following text:

```
ScuWdtIntrExample PASSED
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
8

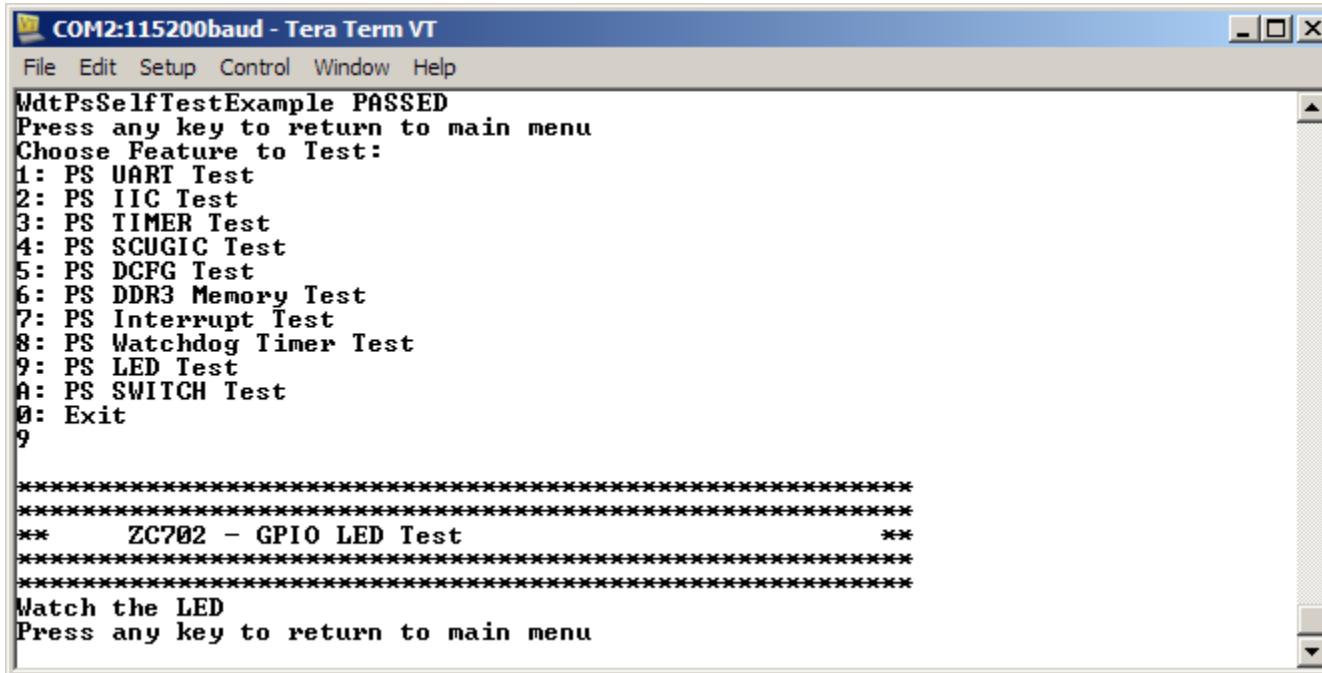
*****
**          ZC702 Watchdog Timer Test      **
*****
WdtPsSelfTestExample PASSED
Press any key to return to main menu
```

# ZC702 BIST

## ➤ LED Test

- Type **9** to begin LED Test

## ➤ View LED DS23 blinking



COM2:115200baud - Tera Term VT

File Edit Setup Control Window Help

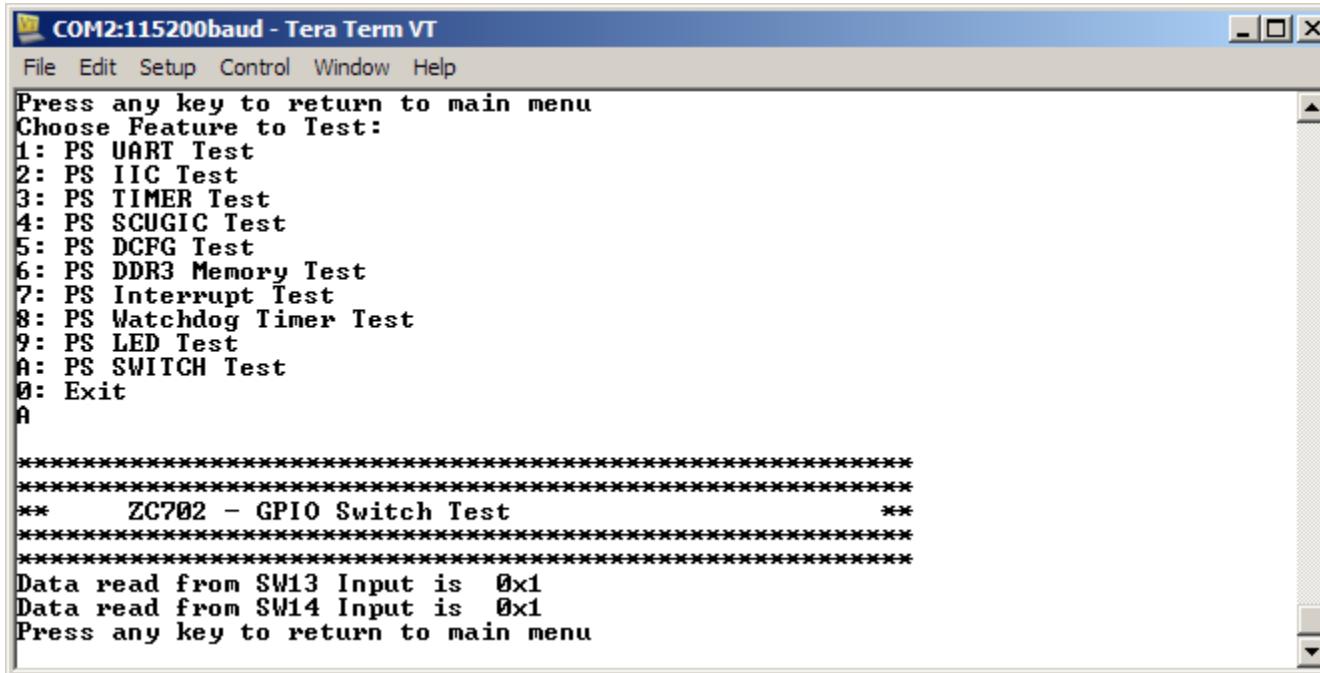
```
WdtPsSelfTestExample PASSED
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
9

*****
**      ZC702 - GPIO LED Test      **
*****
Watch the LED
Press any key to return to main menu
```

# ZC702 BIST

## ➤ GPIO Switch Test

- Set 2-position GPIO DIP Switch (SW15) or depress SW13 and SW14
- Type **A** to begin GPIO Switch Test
  - Reads switch settings



COM2:115200baud - Tera Term VT

File Edit Setup Control Window Help

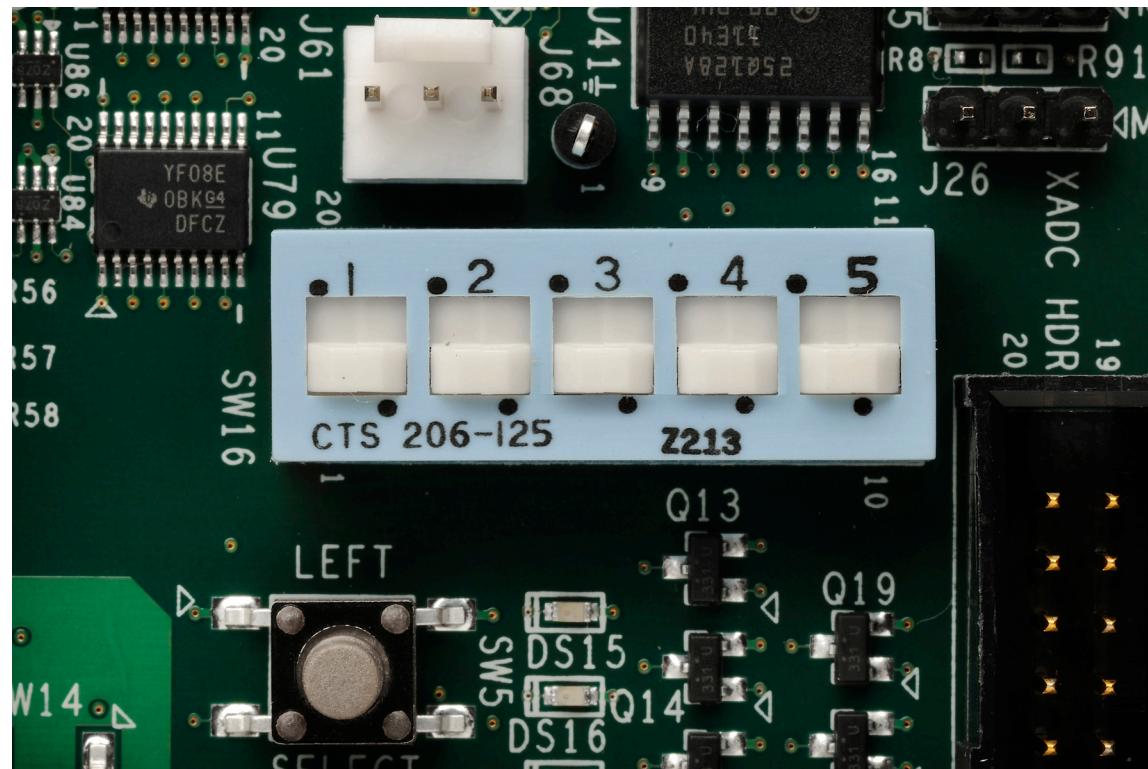
```
Press any key to return to main menu
Choose Feature to Test:
1: PS UART Test
2: PS IIC Test
3: PS TIMER Test
4: PS SCUGIC Test
5: PS DCFG Test
6: PS DDR3 Memory Test
7: PS Interrupt Test
8: PS Watchdog Timer Test
9: PS LED Test
A: PS SWITCH Test
0: Exit
A

*****
**      ZC702 - GPIO Switch Test      **
*****
Data read from SW13 Input is 0x1
Data read from SW14 Input is 0x1
Press any key to return to main menu
```

# **Run the USB Design**

# Run the USB Design

- Set SW16 DIP Switches to 00000
- Cycle board power to clear the BIST program





# Caution



## ► This procedure will format a disk drive

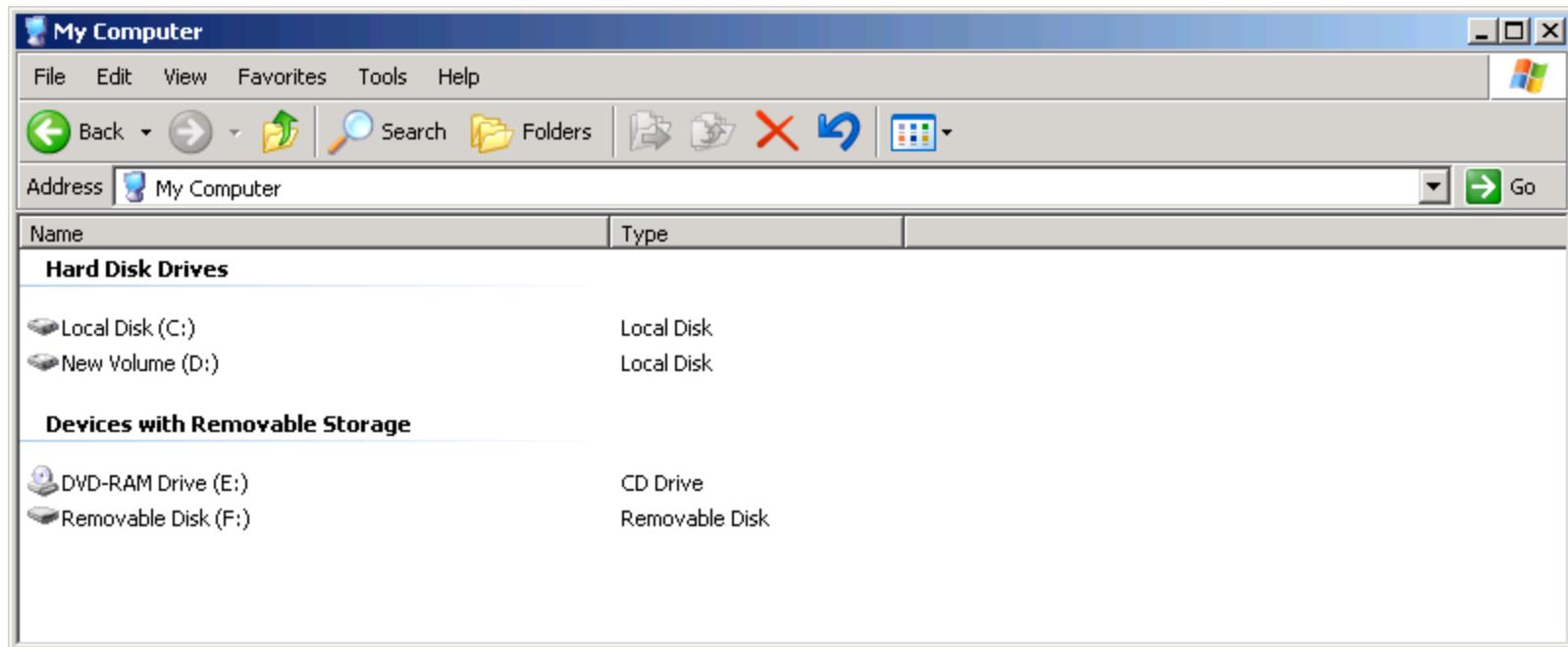
- Make sure you are formatting the ZC702 USB Flash and not your PC's hard drive
- Drive letters mentioned in this procedure will vary from PC to PC - **Verify** the drive letter before formatting

## ► Xilinx cannot take responsibility for lost data or damaged hard drives



# Run the USB Design

- ▶ View your current set of disk drives



# Run the USB Design

- ▶ Connect a USB Type-A to Micro-B cable to the USB ULPI connector on the ZC702 board
  - Connect this cable to your PC



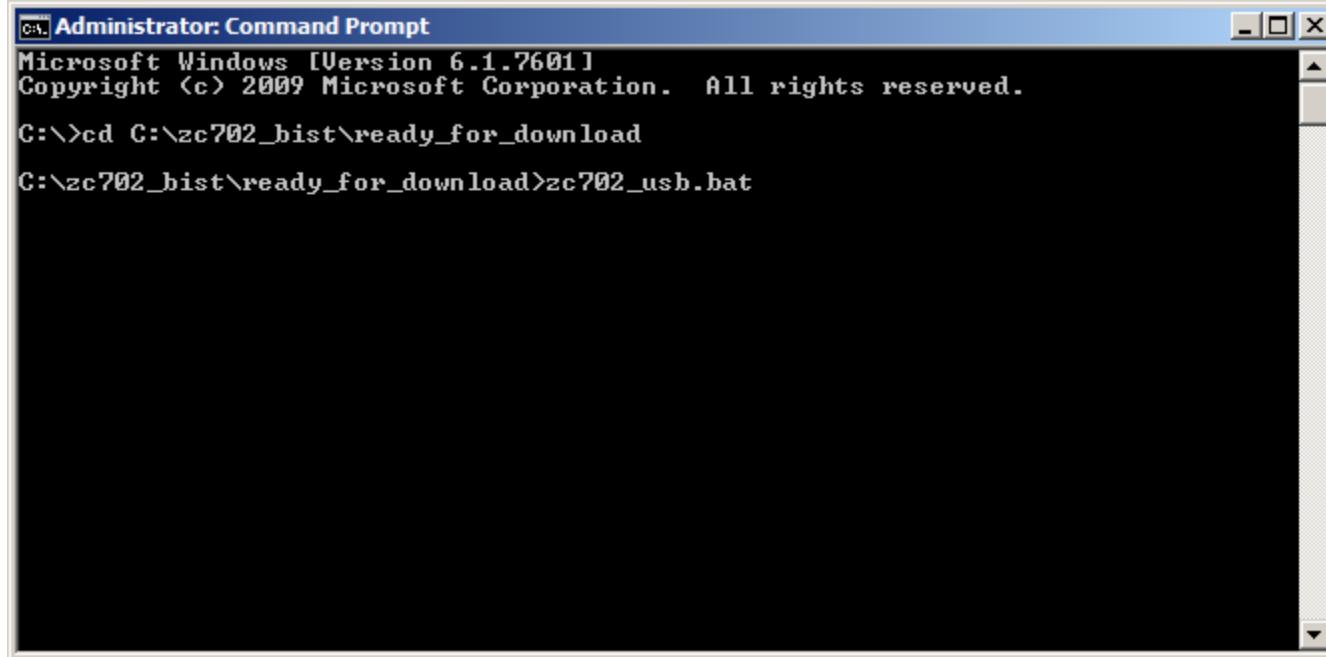
Note: Presentation applies to the ZC702

# Run the USB Design

➤ Download the USB ELF

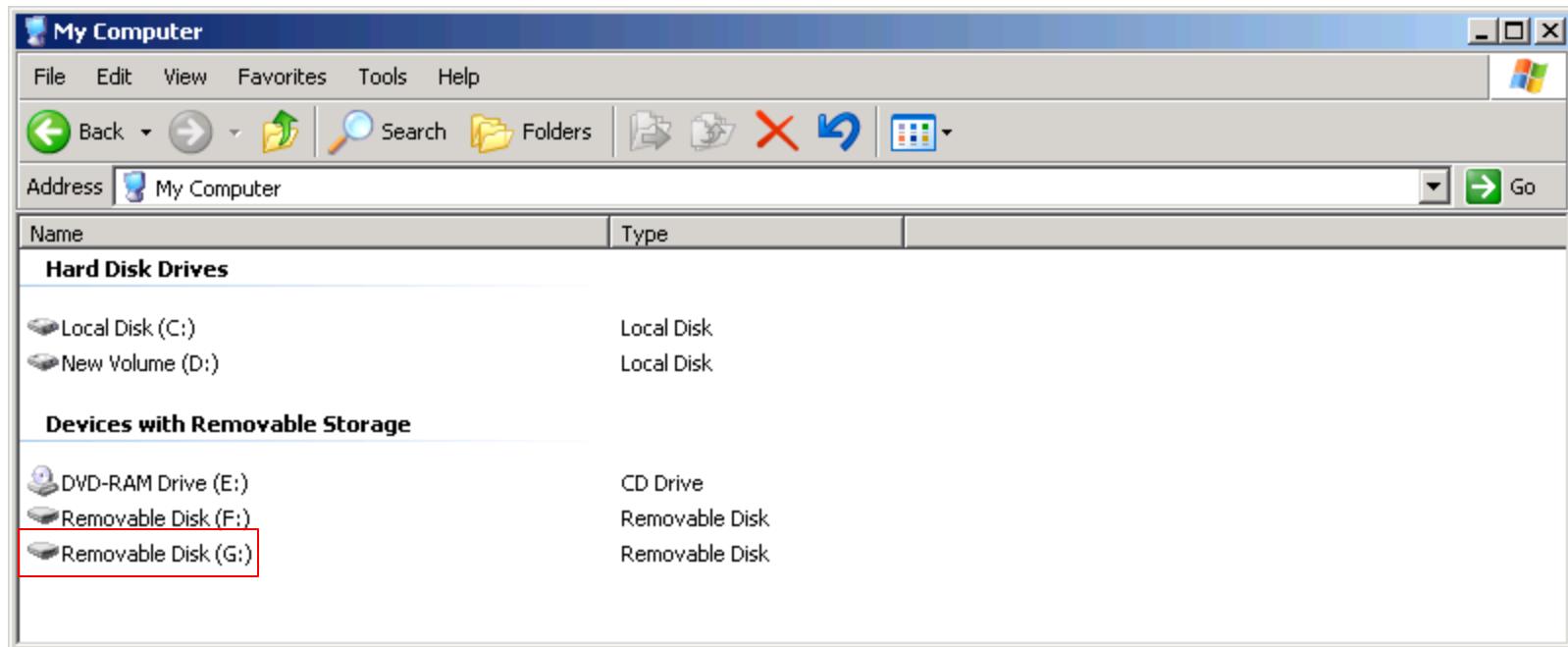
➤ In a Windows prompt type:

```
cd C:\zc702_bist\ready_for_download  
zc702_usb.bat
```



# Run the USB Design

- An extra removable drive will appear
  - In this case, “G:”

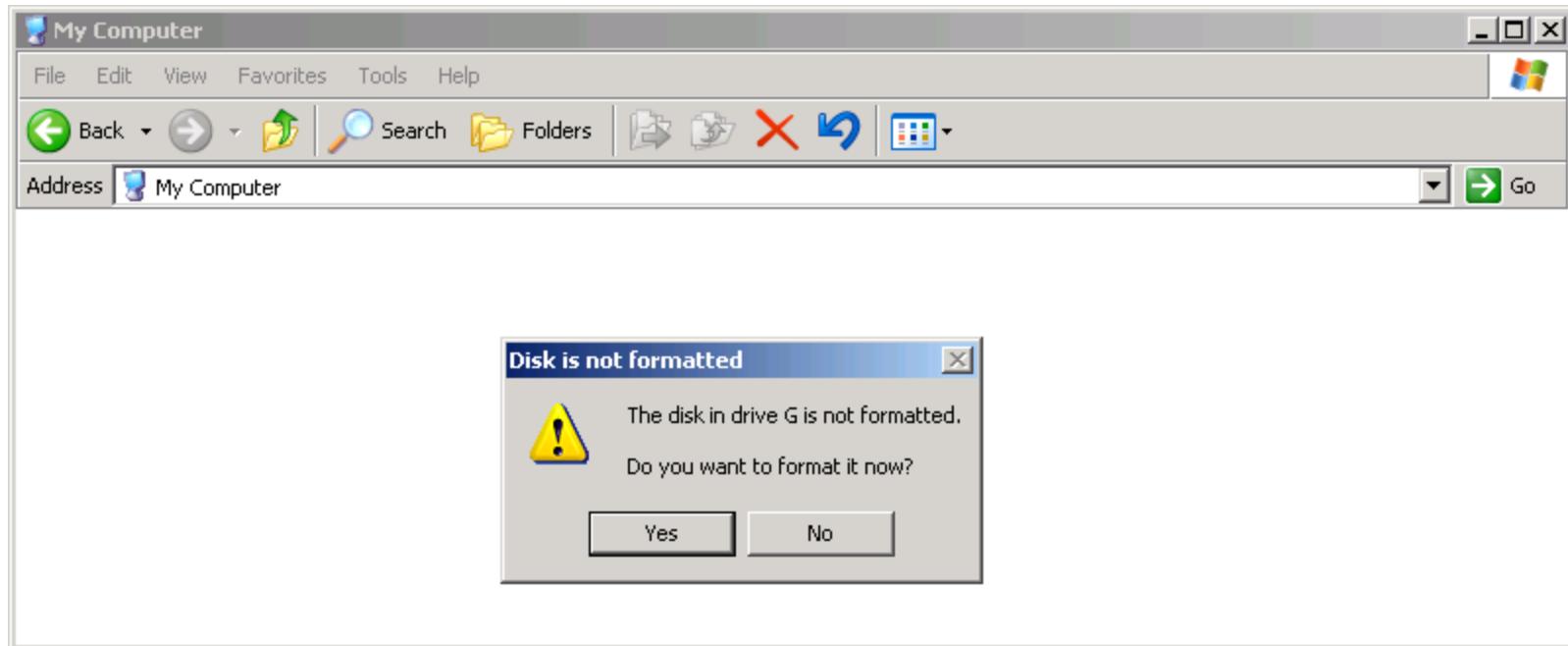


# Run the USB Design

## ► Open the “G:” drive

- A “Disk is not formatted” message will appear

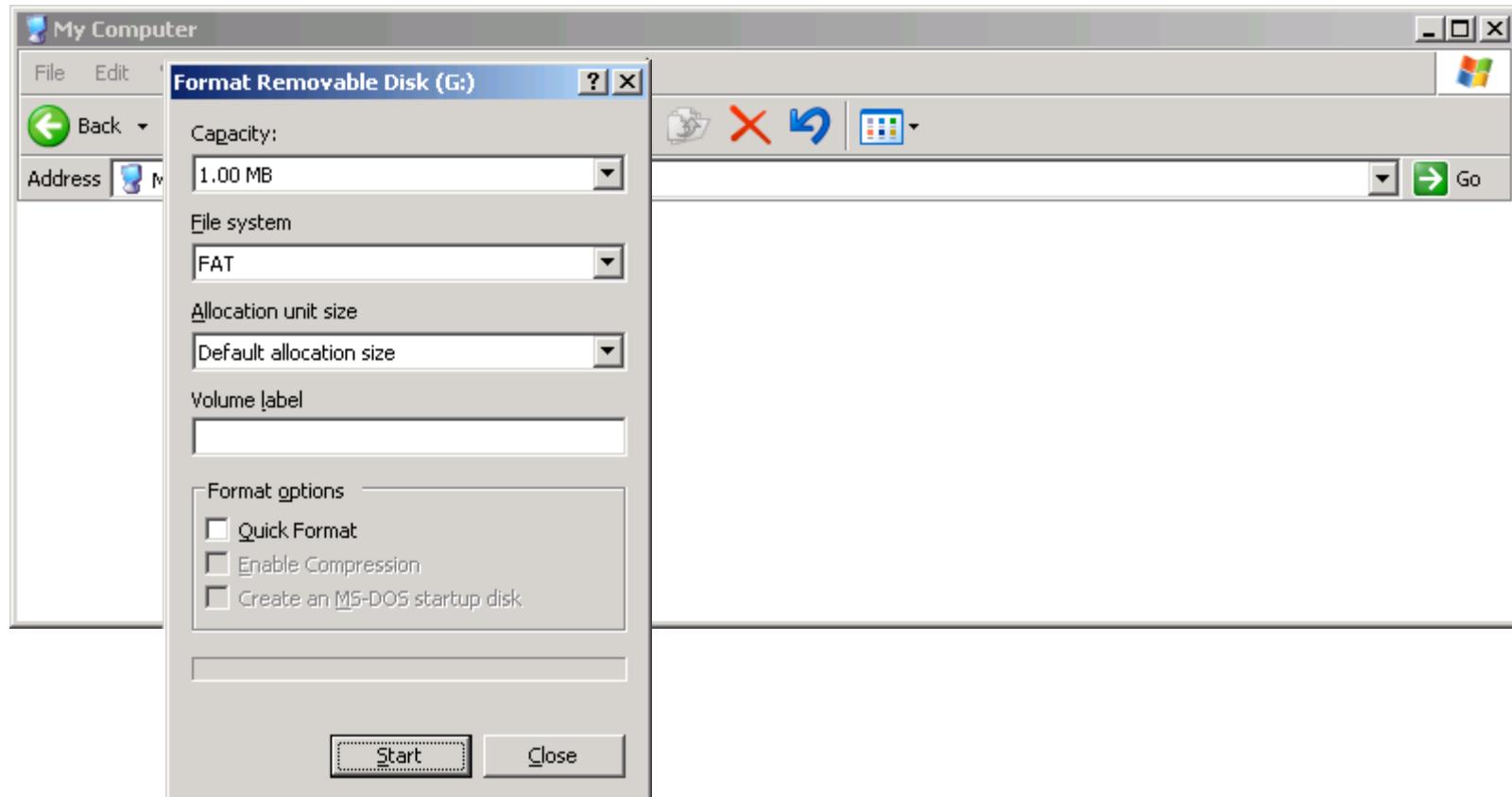
 If this is the correct drive, click **Yes**; if not, click **No**



# Run the USB Design

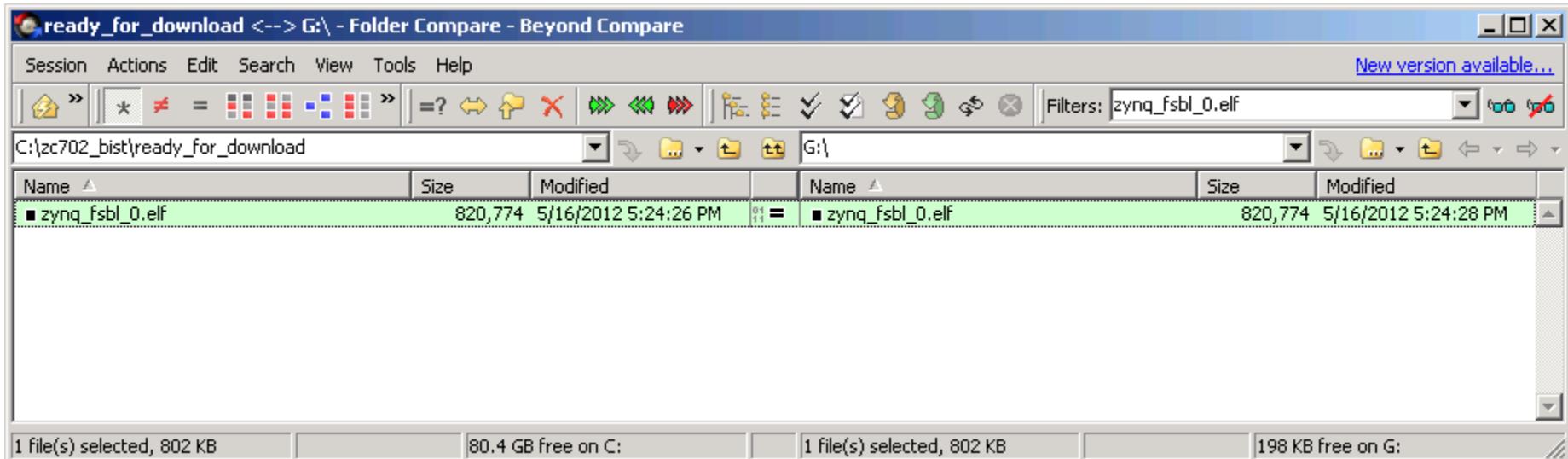
► A format dialog for drive G: will appear

- The size should be 1.00 MB
- If this is the correct, click **Start**
- Close this dialog when done



# Run the USB Design

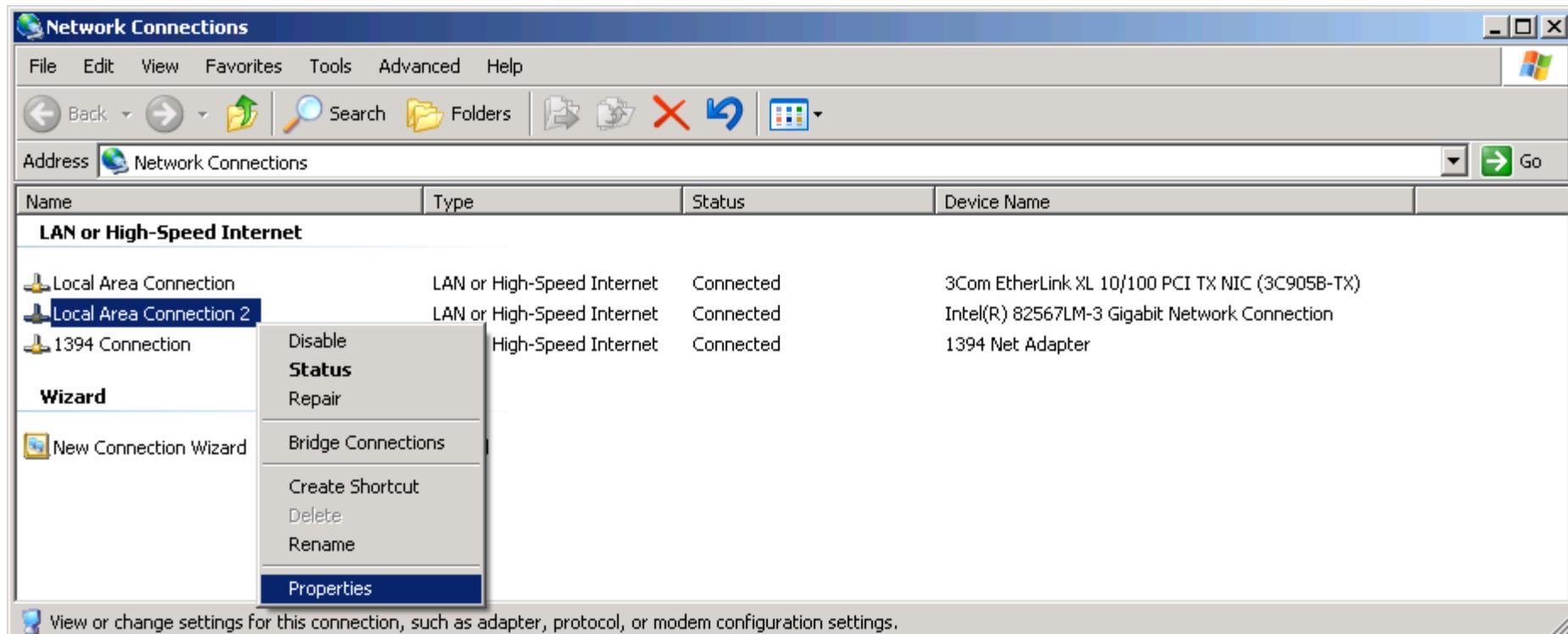
- At this point, you can copy small files to G: and verify the operation of this drive
- Disconnect USB cable before running LwIP



# Run the LwIP Ethernet Design

# Run the LwIP Ethernet Design

- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties



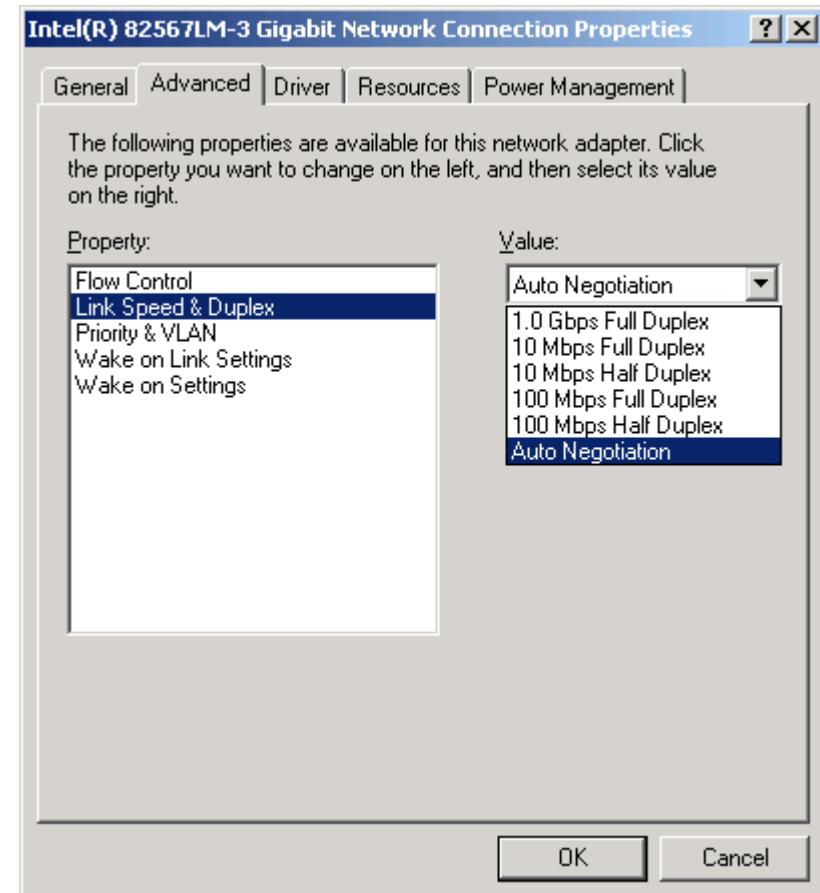
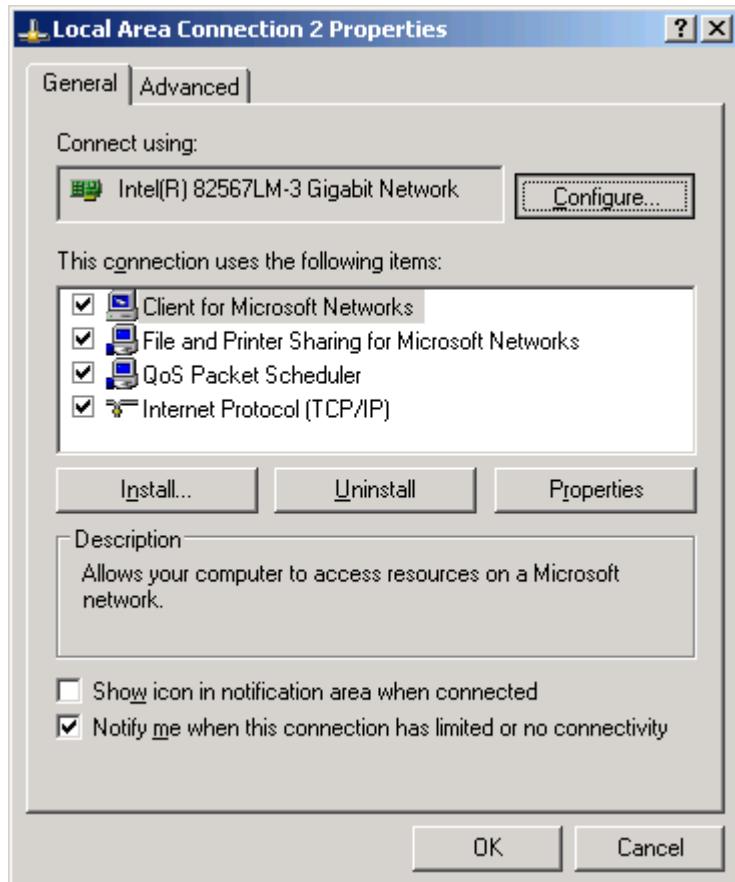
Note: The LwIP SDK project has AR60358 applied

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# Run the LwIP Ethernet Design

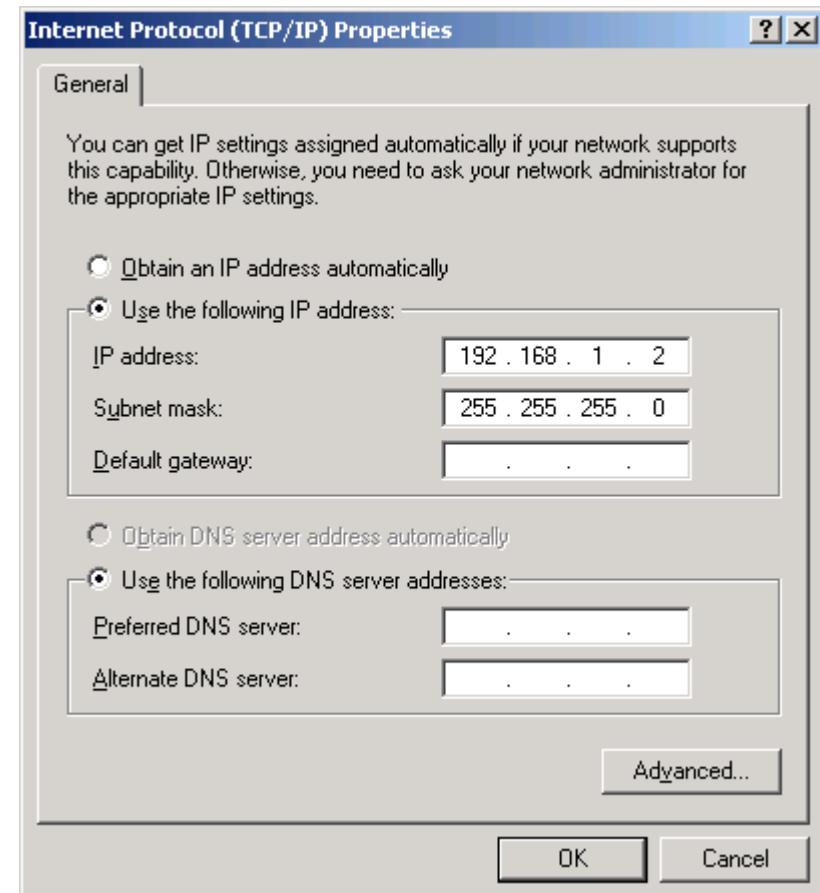
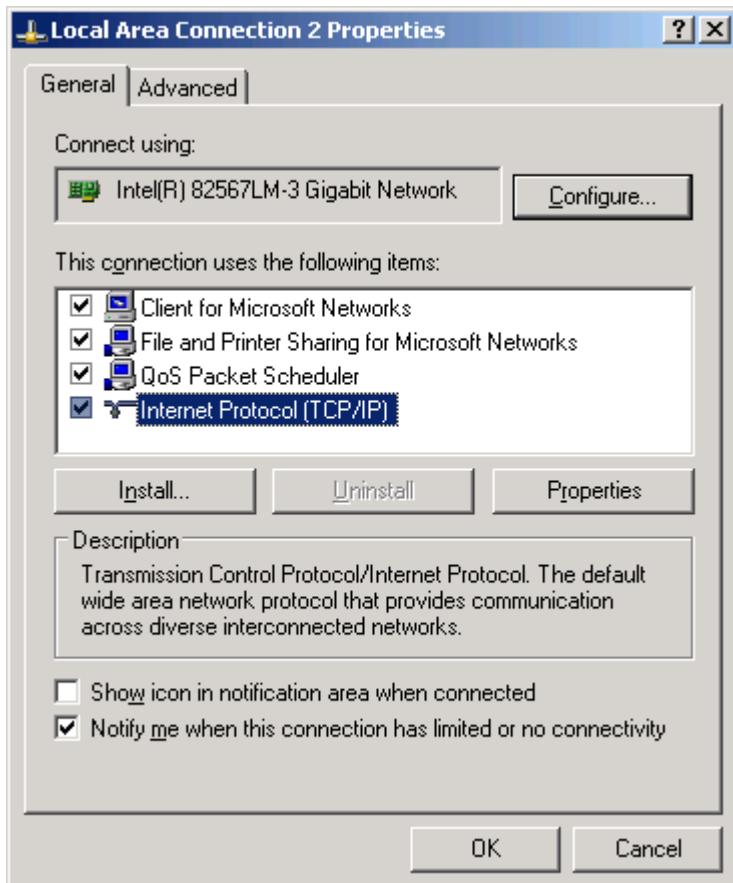
## ► Click Configure

- Set the Media Type to Auto for 1 Gbps then click OK



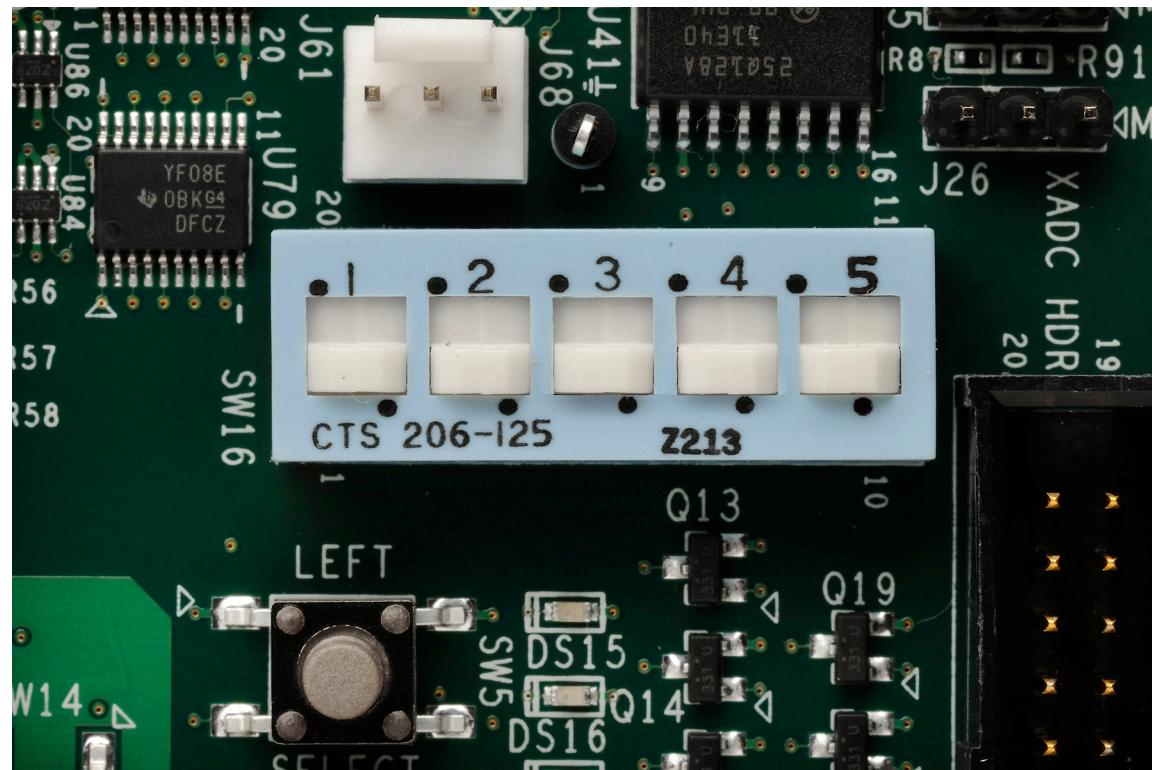
# Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:



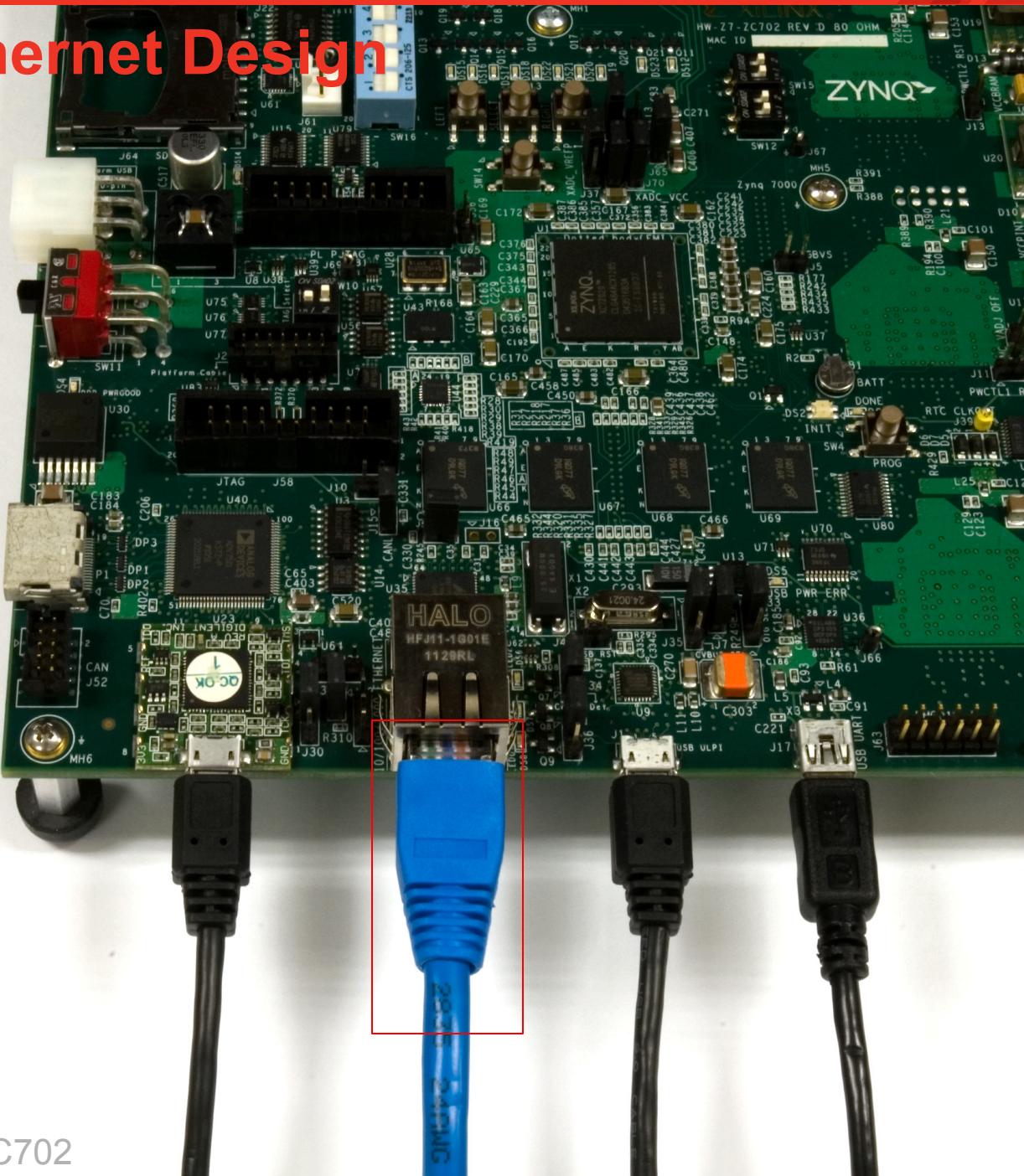
# Run the LwIP Ethernet Design

- Set SW16 DIP Switches to 00000
- Cycle board power to clear the USB program



# Run the LwIP Ethernet Design

- ▶ Connect an Ethernet cable to the Ethernet connector on the ZC702 board
  - Connect this cable to your PC



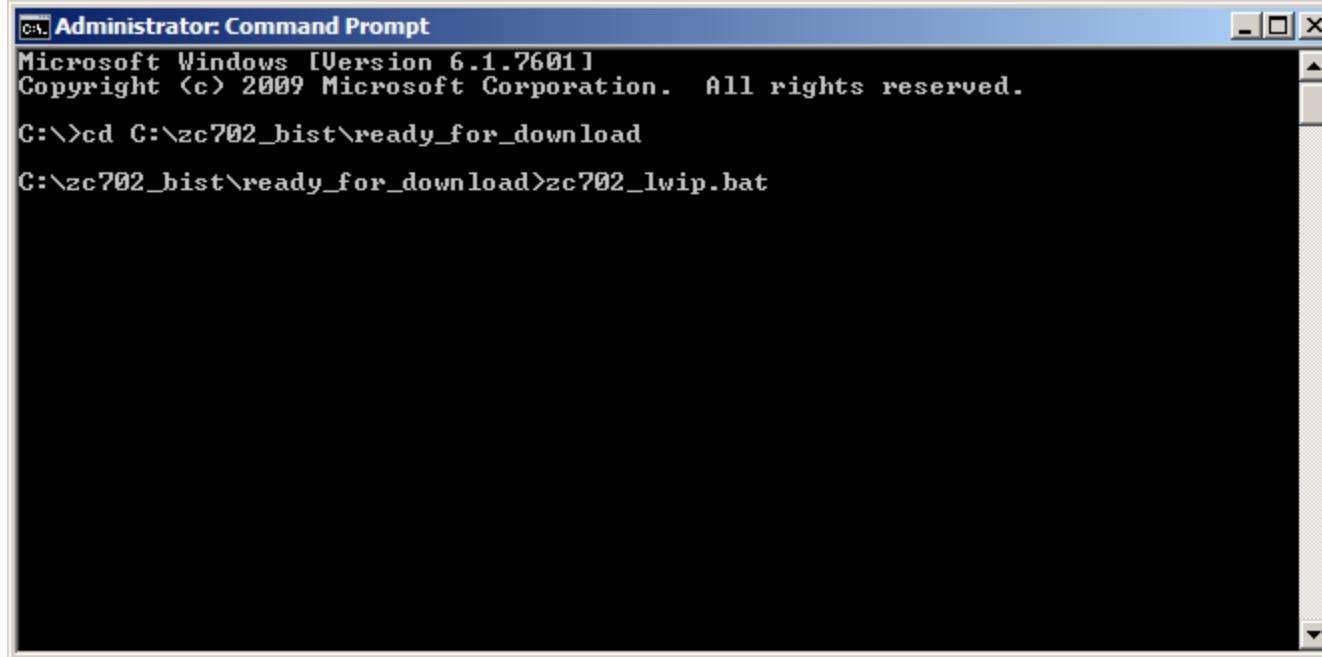
Note: Presentation applies to the ZC702

# Run the LwIP Ethernet Design

➤ Download the LwIP ELF

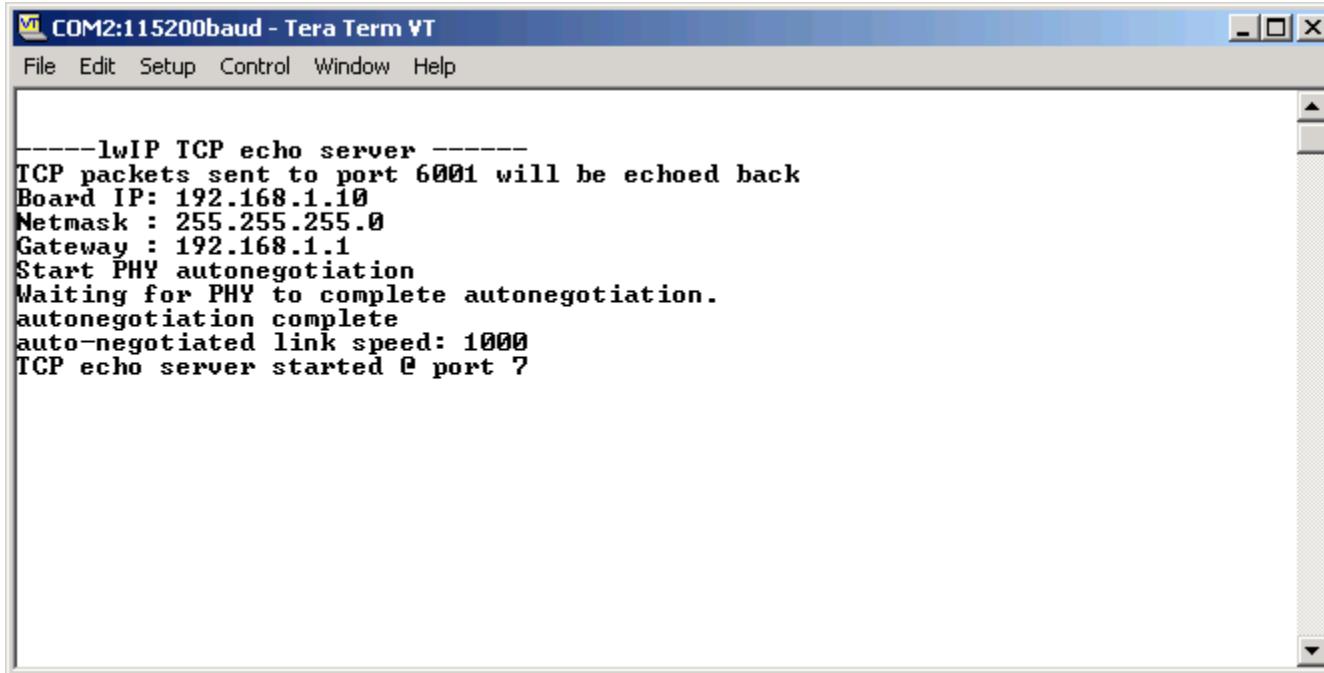
➤ In a Windows prompt type:

```
cd C:\zc702_bist\ready_for_download  
zc702_lwip.bat
```



# Run the LwIP Ethernet Design

## ► View LwIP echo server screen



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window contains the following text output from the LwIP TCP echo server:

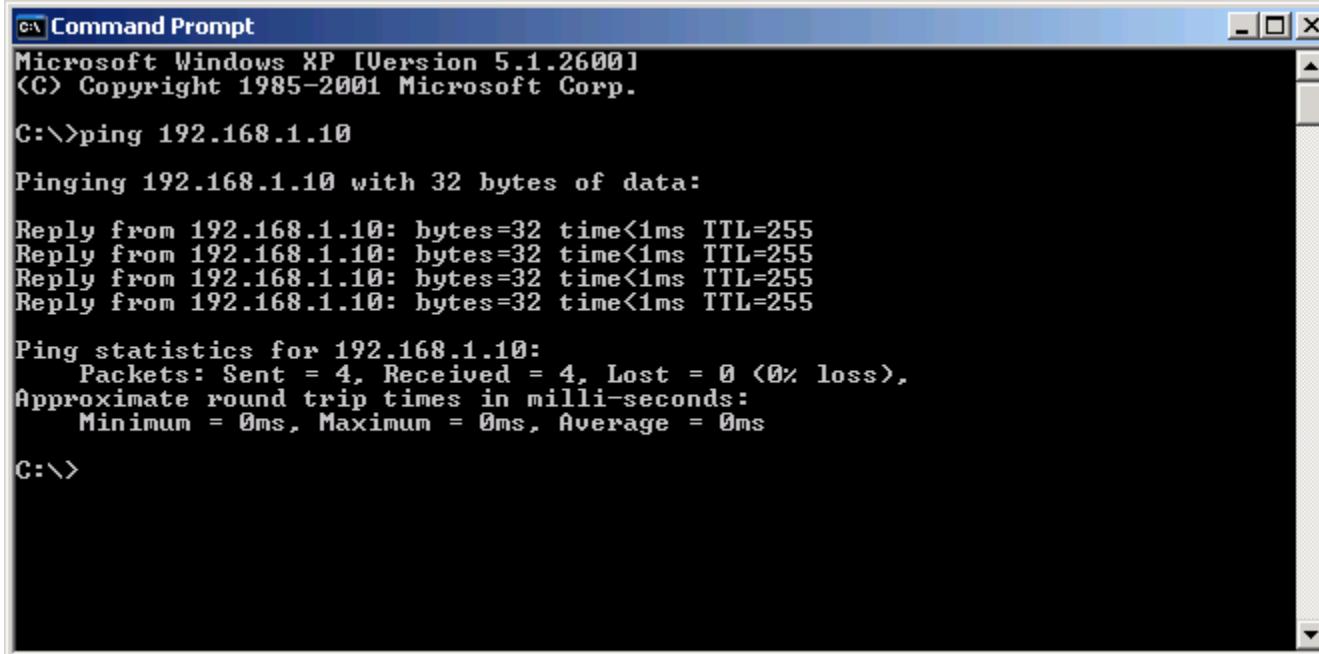
```
----lwIP TCP echo server ----
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
auto-negotiated link speed: 1000
TCP echo server started @ port 7
```

# Run the LwIP Ethernet Design

► From a Windows prompt on the PC Host, enter the command:

**ping 192.168.1.10**

- Ping from PC host 192.168.1.2 to ZC702 target 192.168.1.10



A screenshot of a Microsoft Windows XP Command Prompt window. The title bar reads "C:\ Command Prompt". The window displays the output of a "ping" command. The text shows four successful replies from the target IP address 192.168.1.10, each with 32 bytes and a TTL of 255. Below the replies, ping statistics are provided: 4 packets sent, 4 received, 0 lost (0% loss), and approximate round trip times of 0ms for minimum, maximum, and average.

```
C:\Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:

Reply from 192.168.1.10: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\>
```

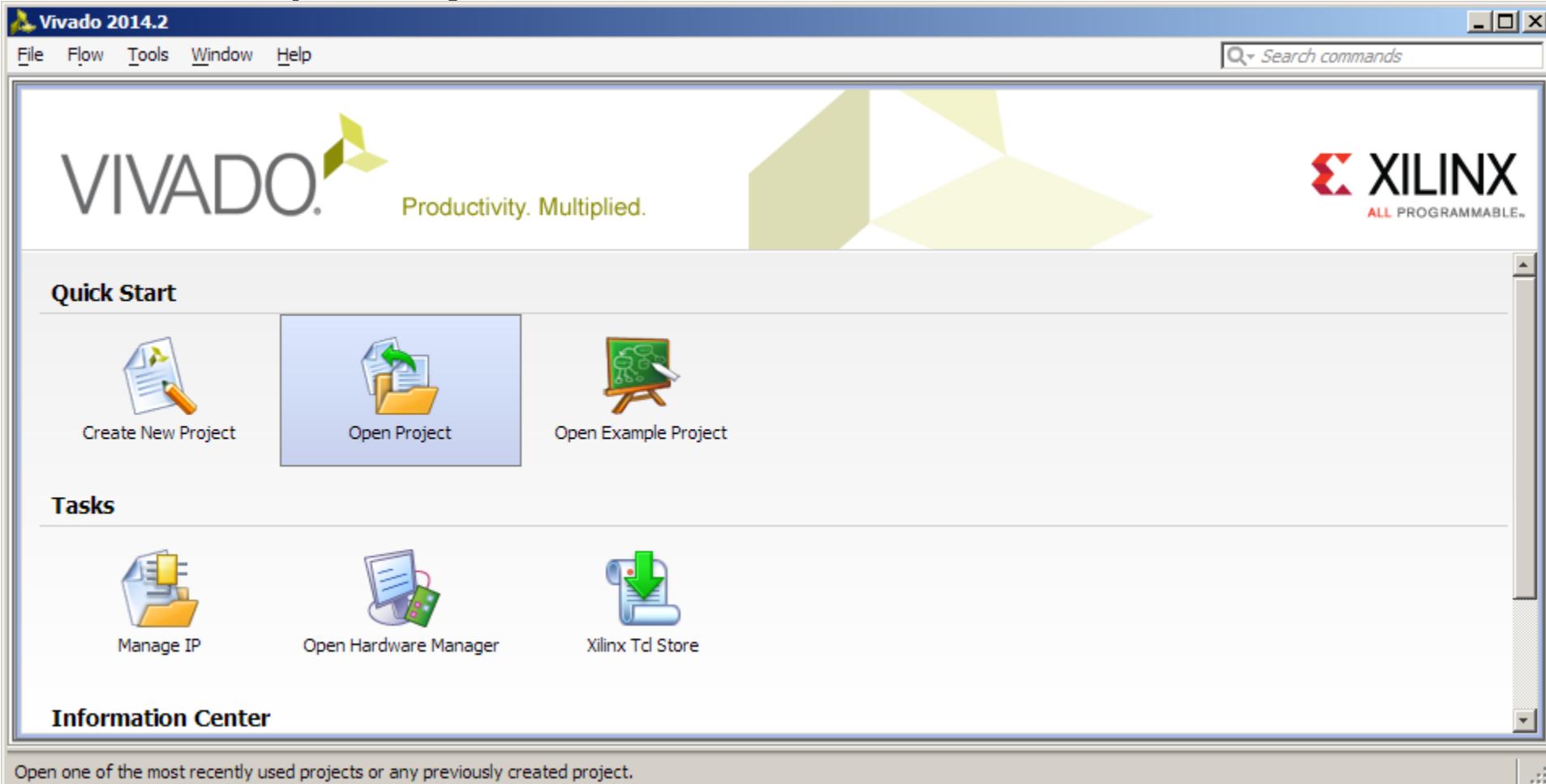
# **Compile ZC702 BIST Design**

# Compile ZC702 BIST Design

## ► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2014.2 → Vivado

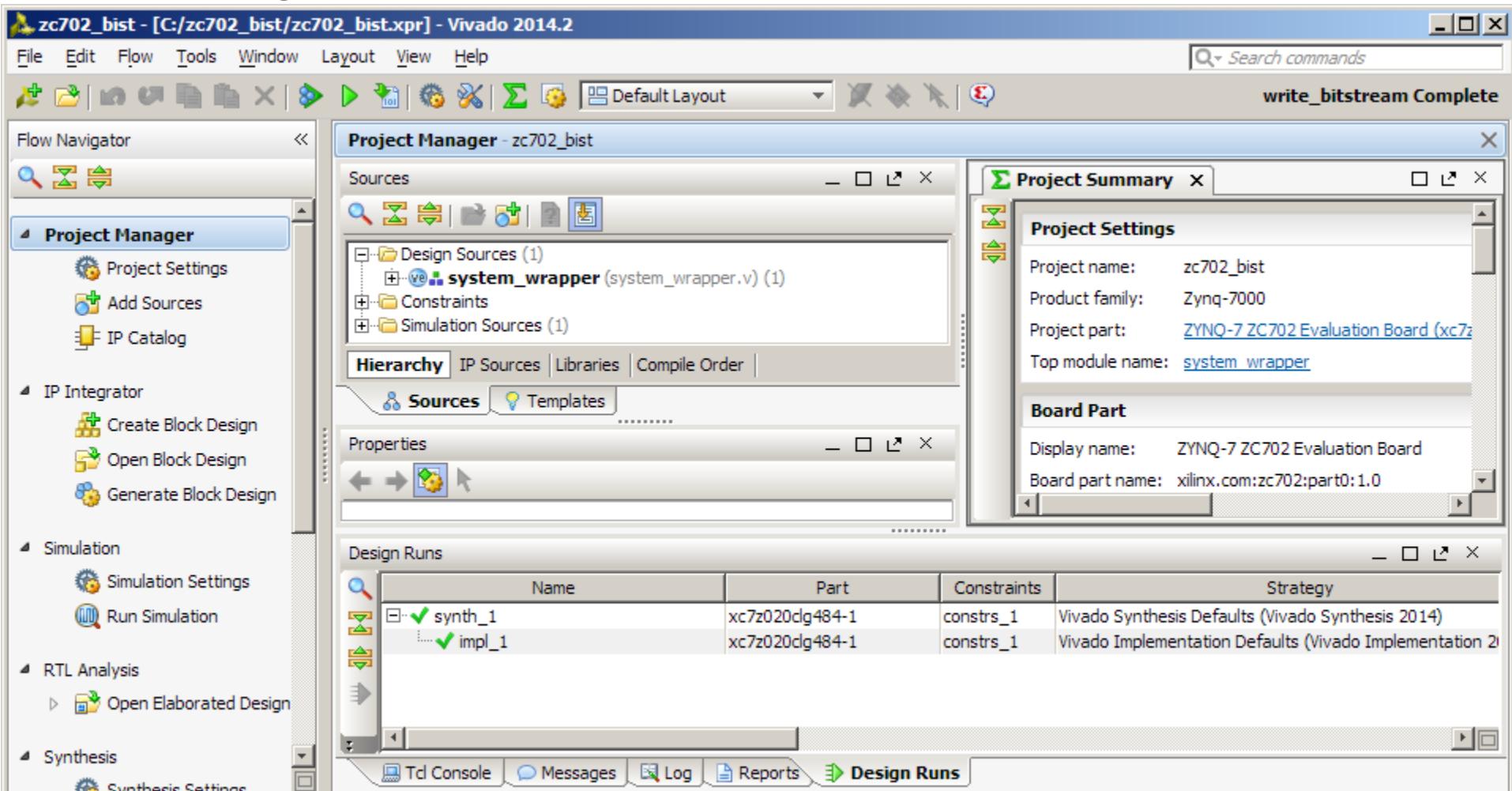
## ► Select Open Project



# Compile ZC702 BIST Design

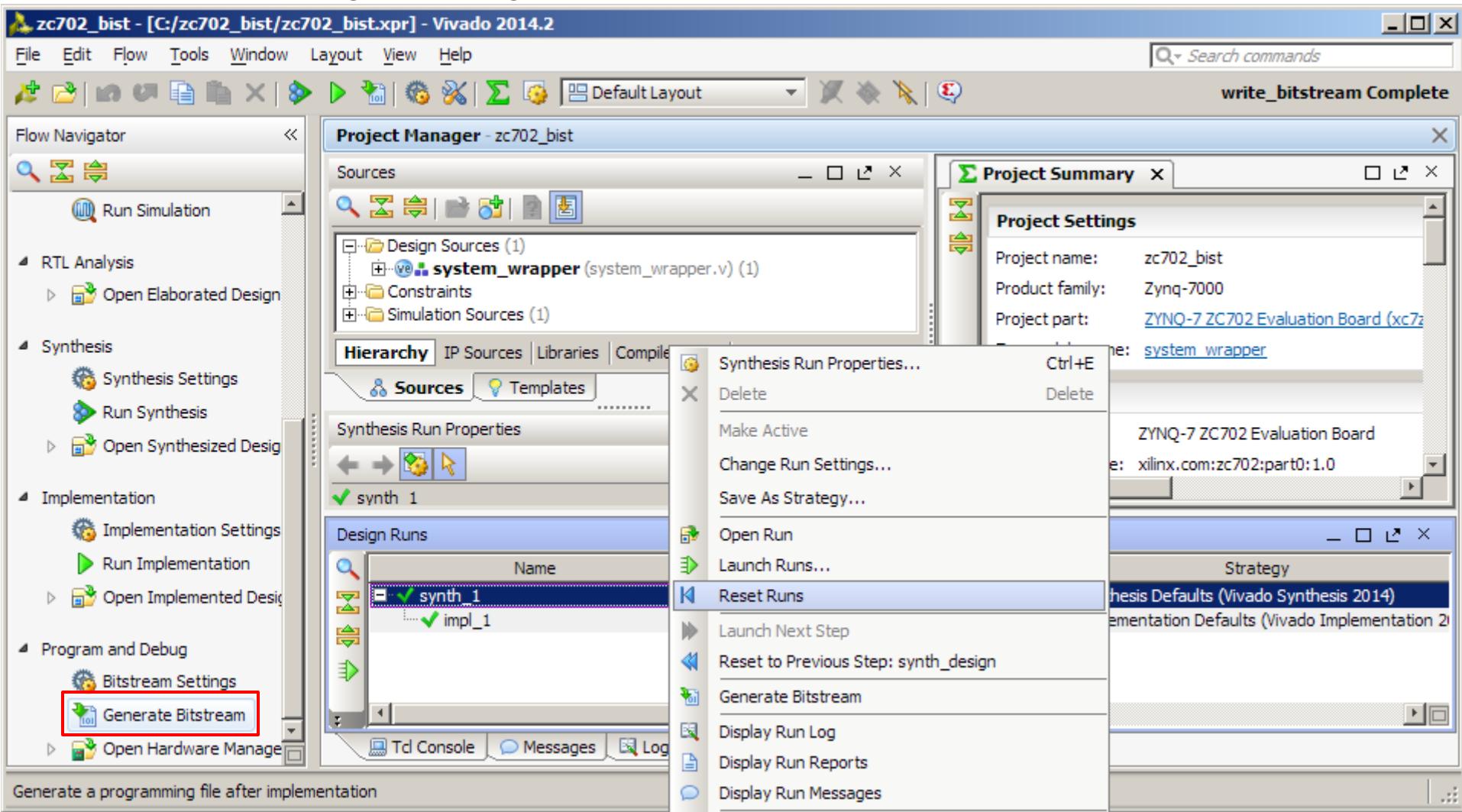
## ► Open the ZC702 Design:

– <Design Name>\zc702\_bist\zc702\_bist.xpr



# Compile ZC702 BIST Design

- The design is fully implemented; you can recompile, or export to SDK
  - To recompile, right-click **synth\_1**, select **Reset Runs** then **Generate Bitstream**

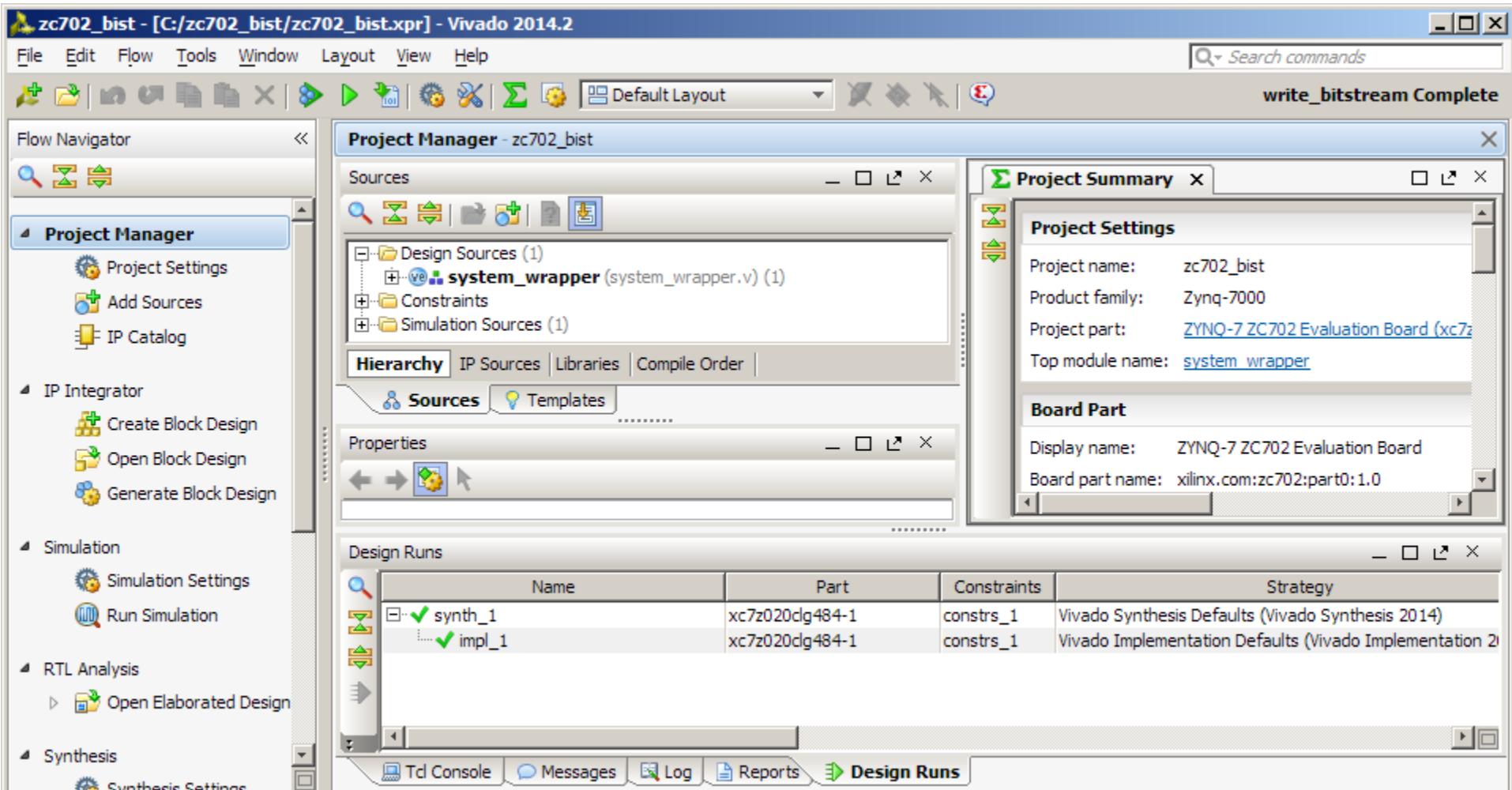


Note: Presentation applies to the ZC702

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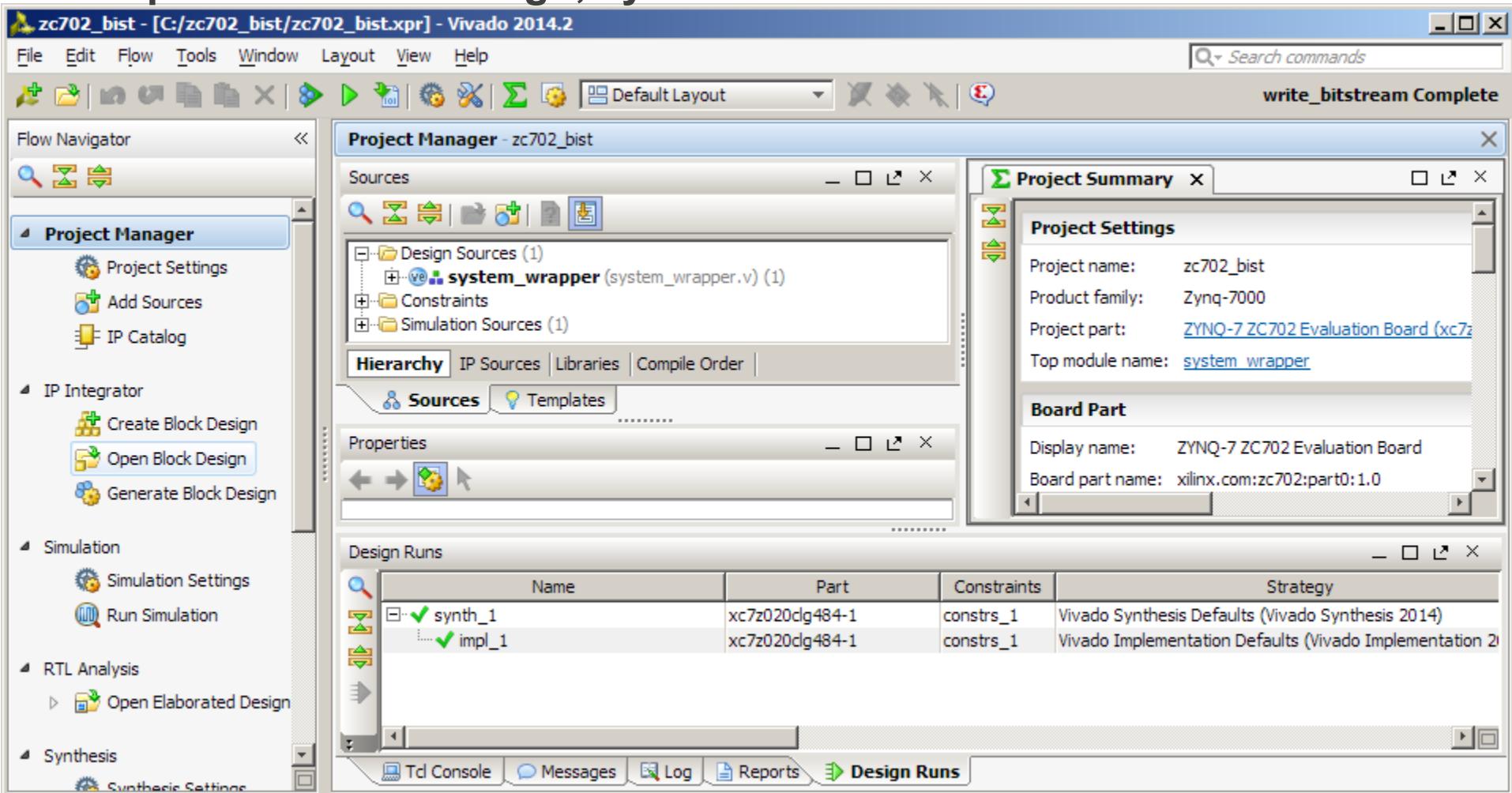
# Compile ZC702 BIST Design

- Once done, both the Synthesis and Implementation will have green check marks



# Compile ZC702 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Open the Block Design, system.bd



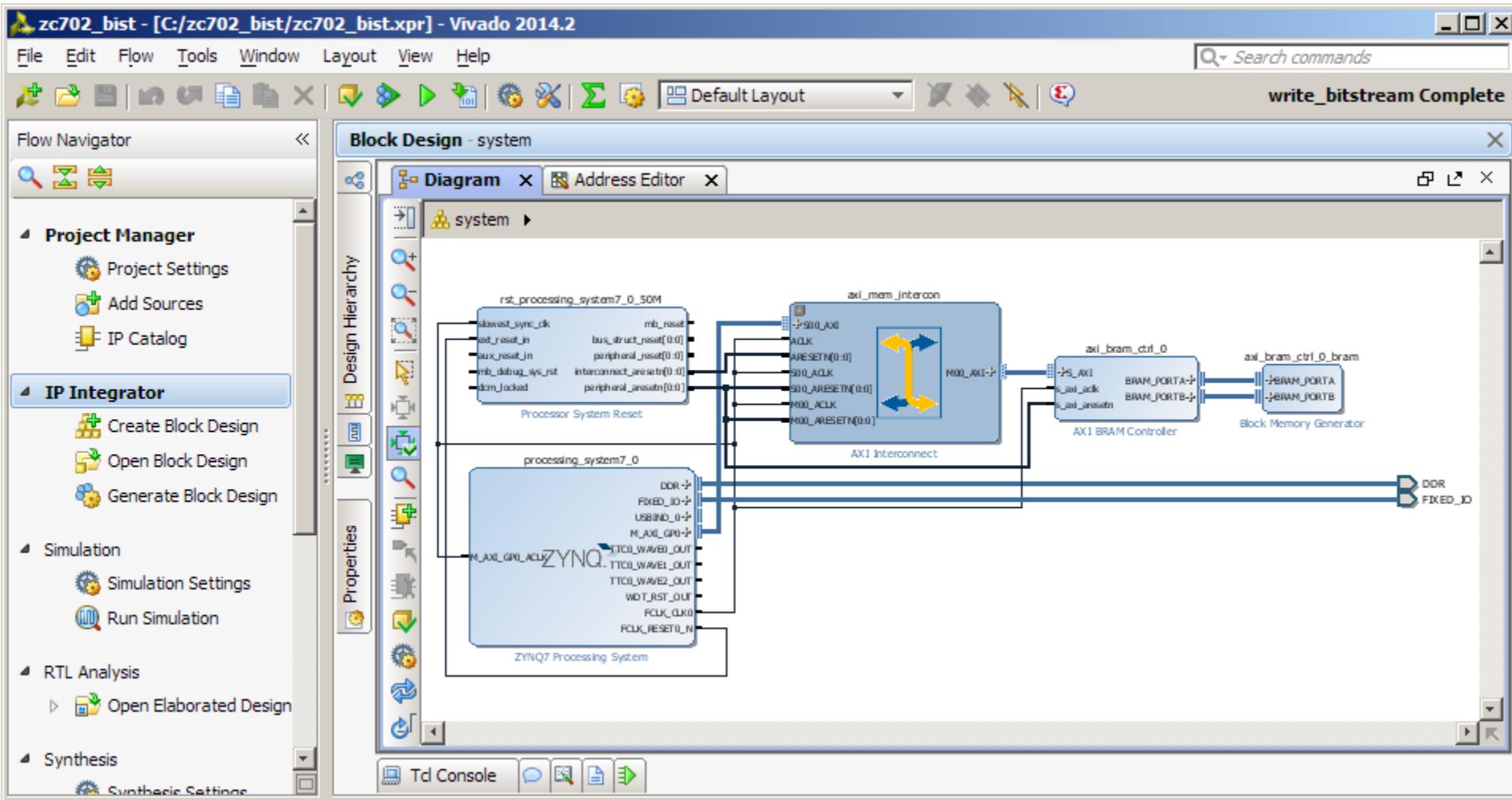
Open an IP subsystem from the current project

Note: Presentation applies to the ZC702

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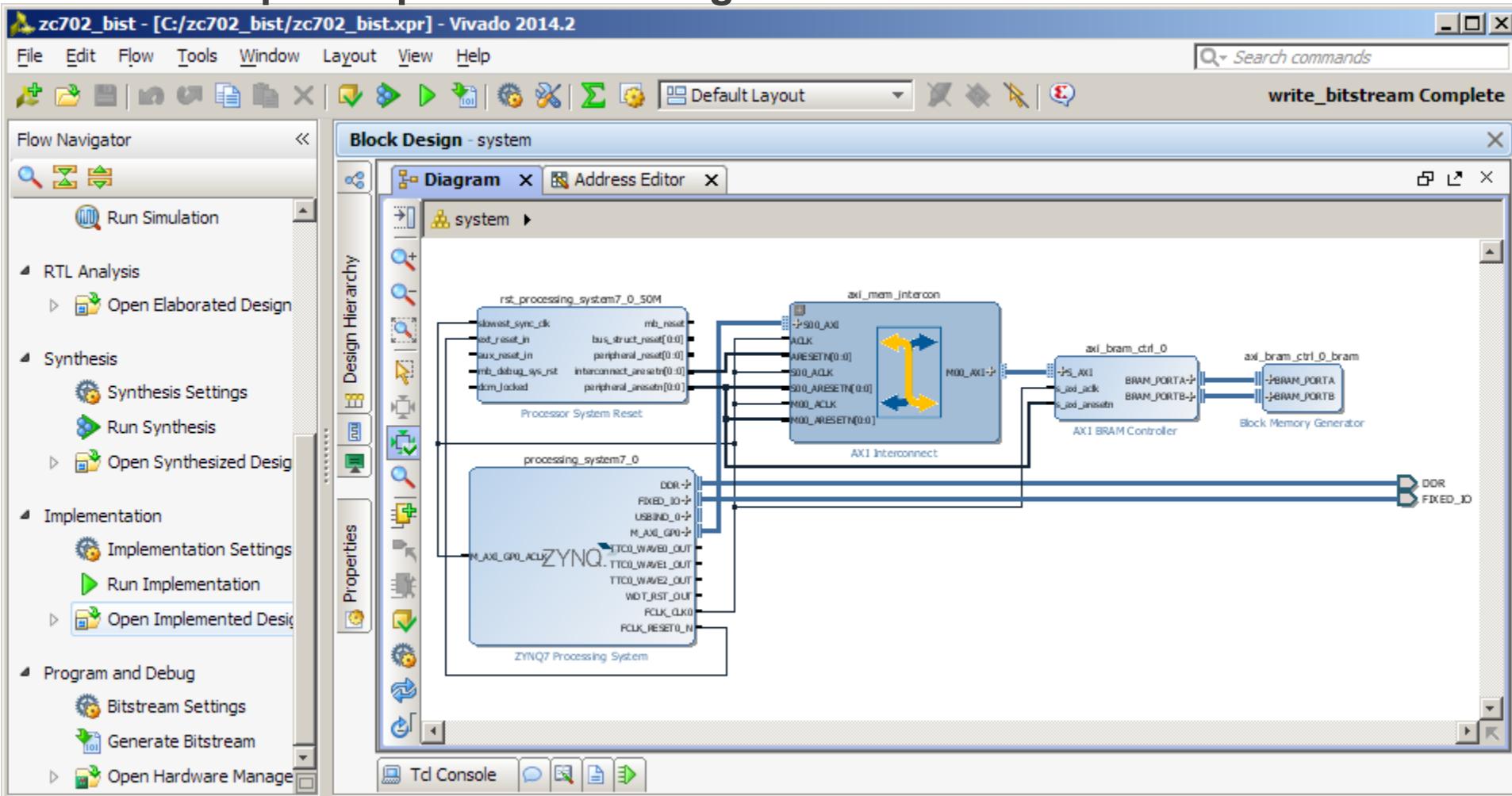
# Compile ZC702 BIST Design

► All the IP Blocks used in the design can be seen in this view



# Compile ZC702 BIST Design

- To export to SDK, the Block and Implemented designs must be open
- Click Open Implemented Design

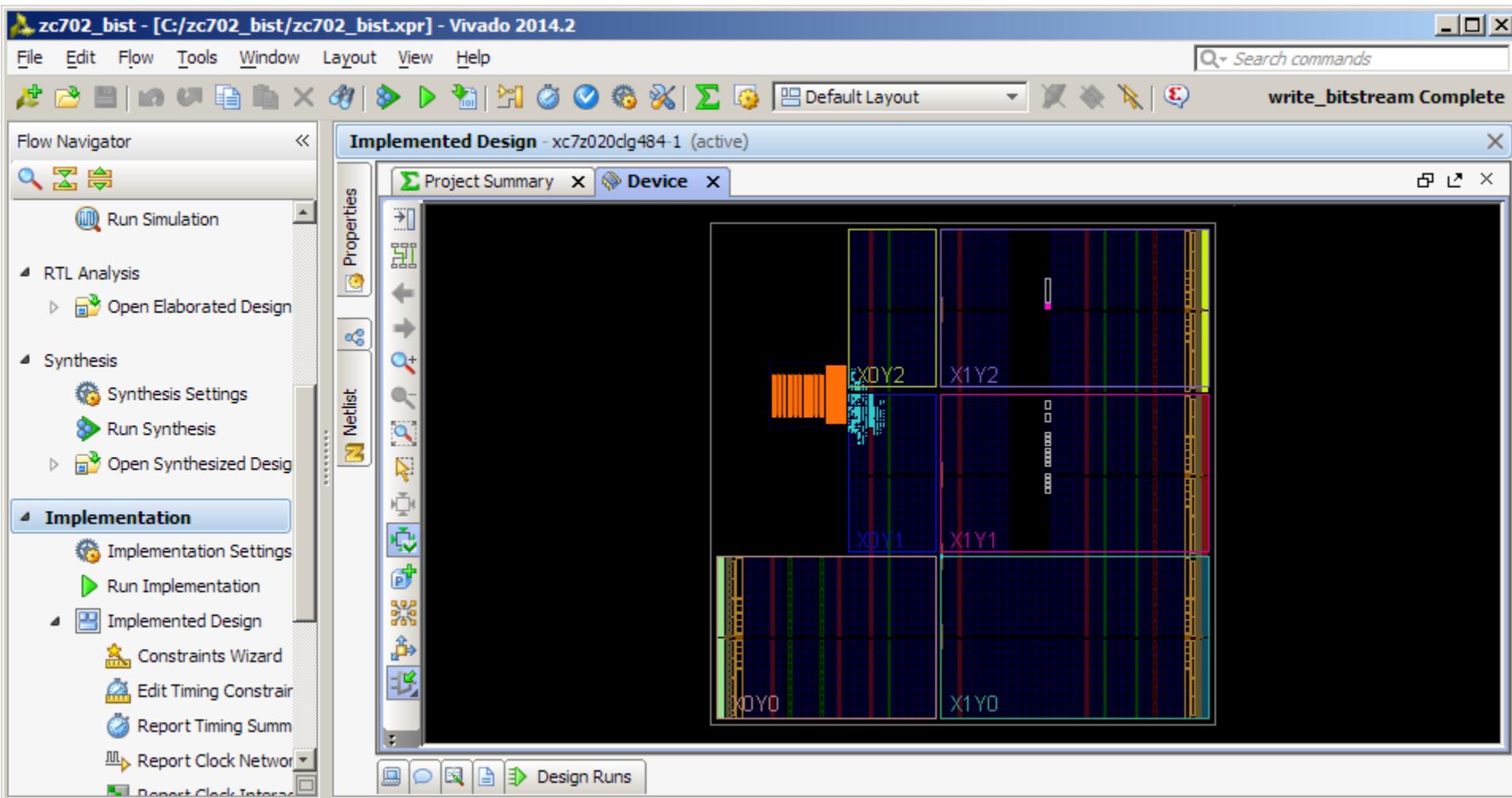


Note: Presentation applies to the ZC702

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# Compile ZC702 BIST Design

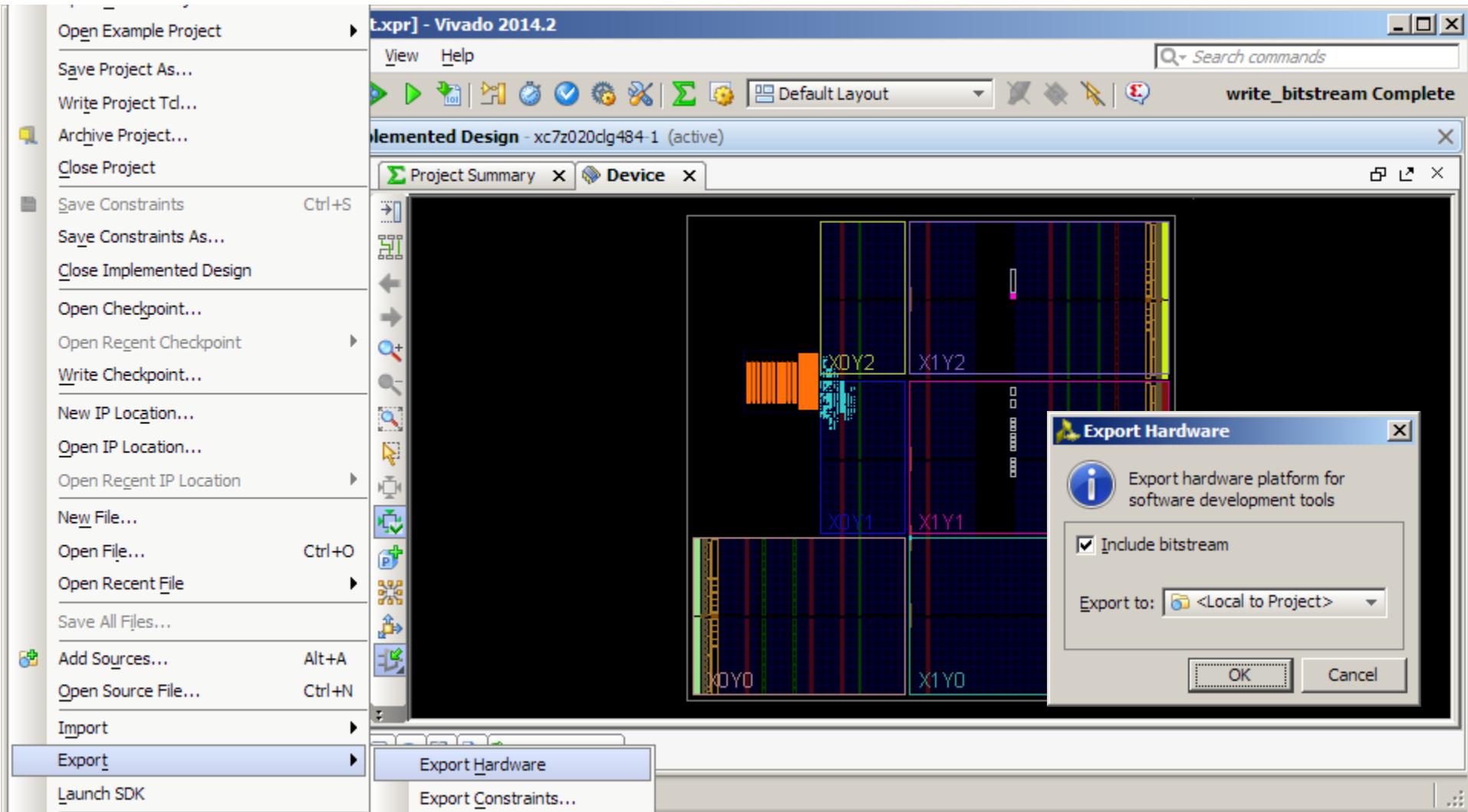
## ► View Implemented Design



# Compile ZC702 BIST Design

► Select File → Export → Export Hardware

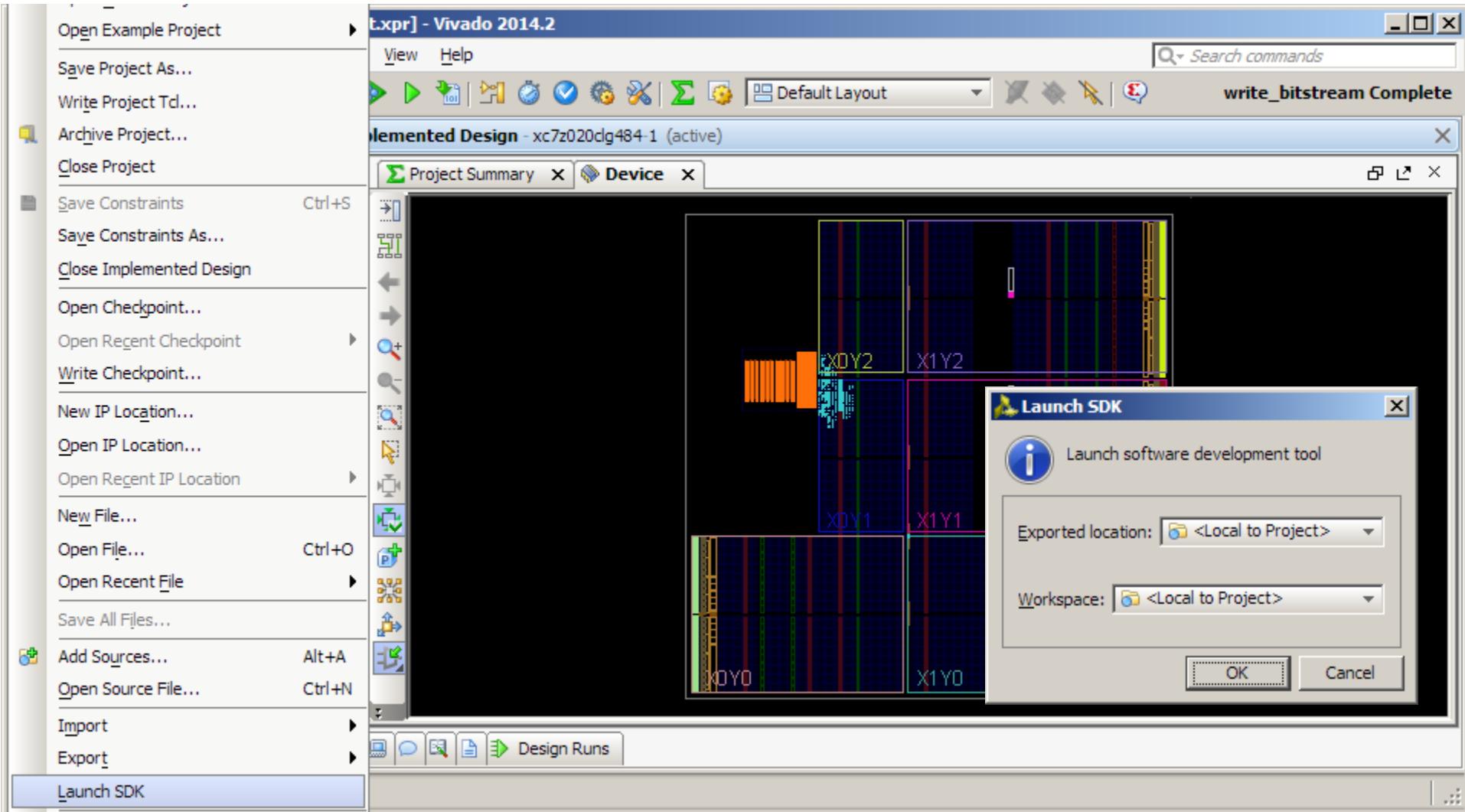
► Click OK



# Compile ZC702 BIST Design

► Select File → Launch SDK

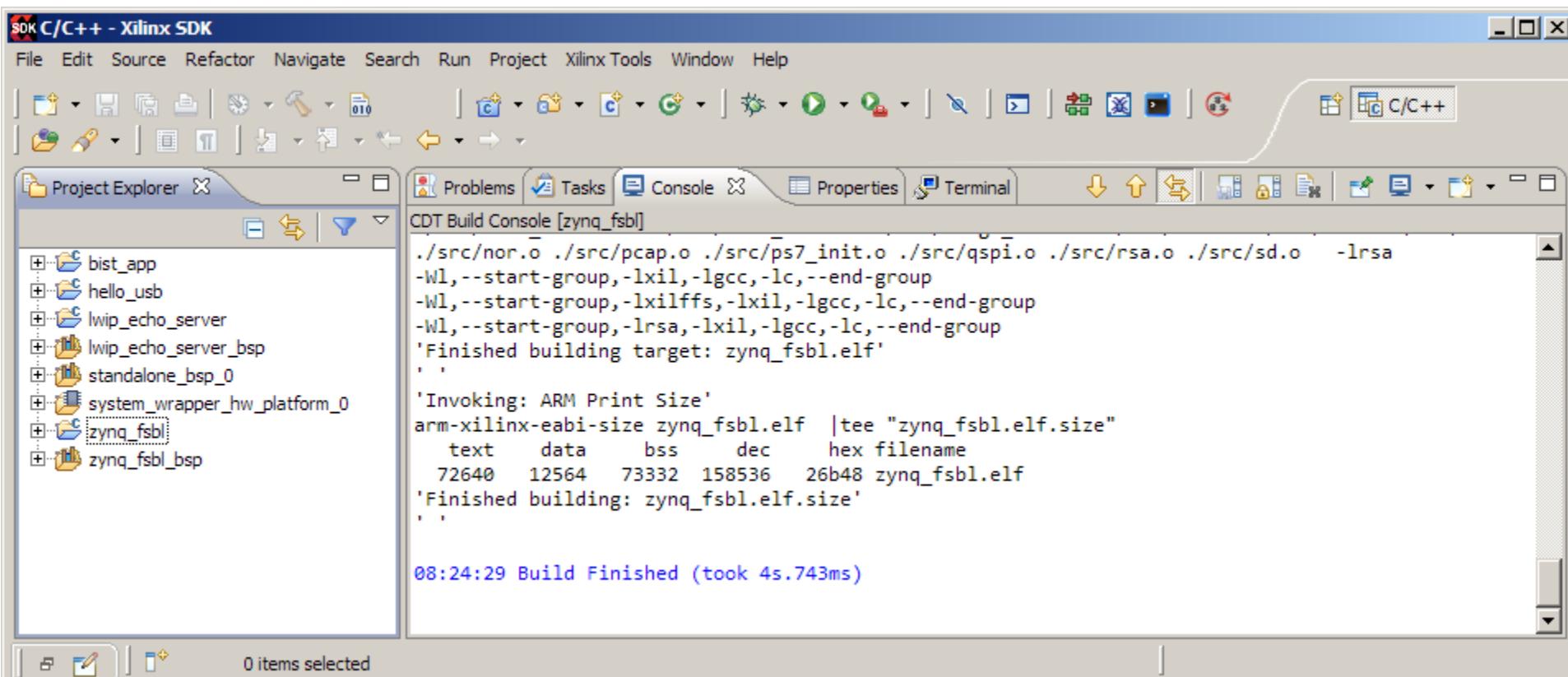
► Click OK



# Compile ZC702 Software in SDK

## ► SDK Software Compile - Build ELF files in SDK

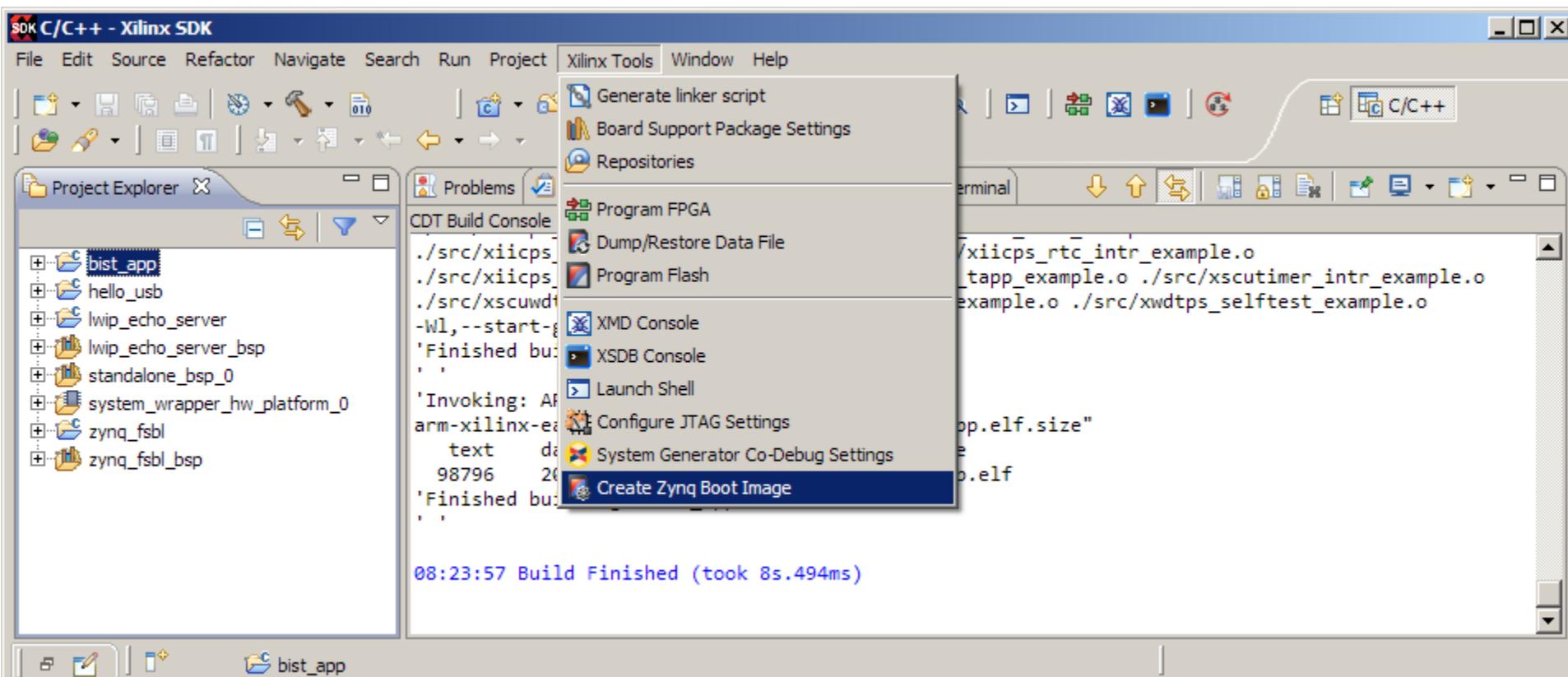
- Project builds automatically



# **Creating a BOOT Image**

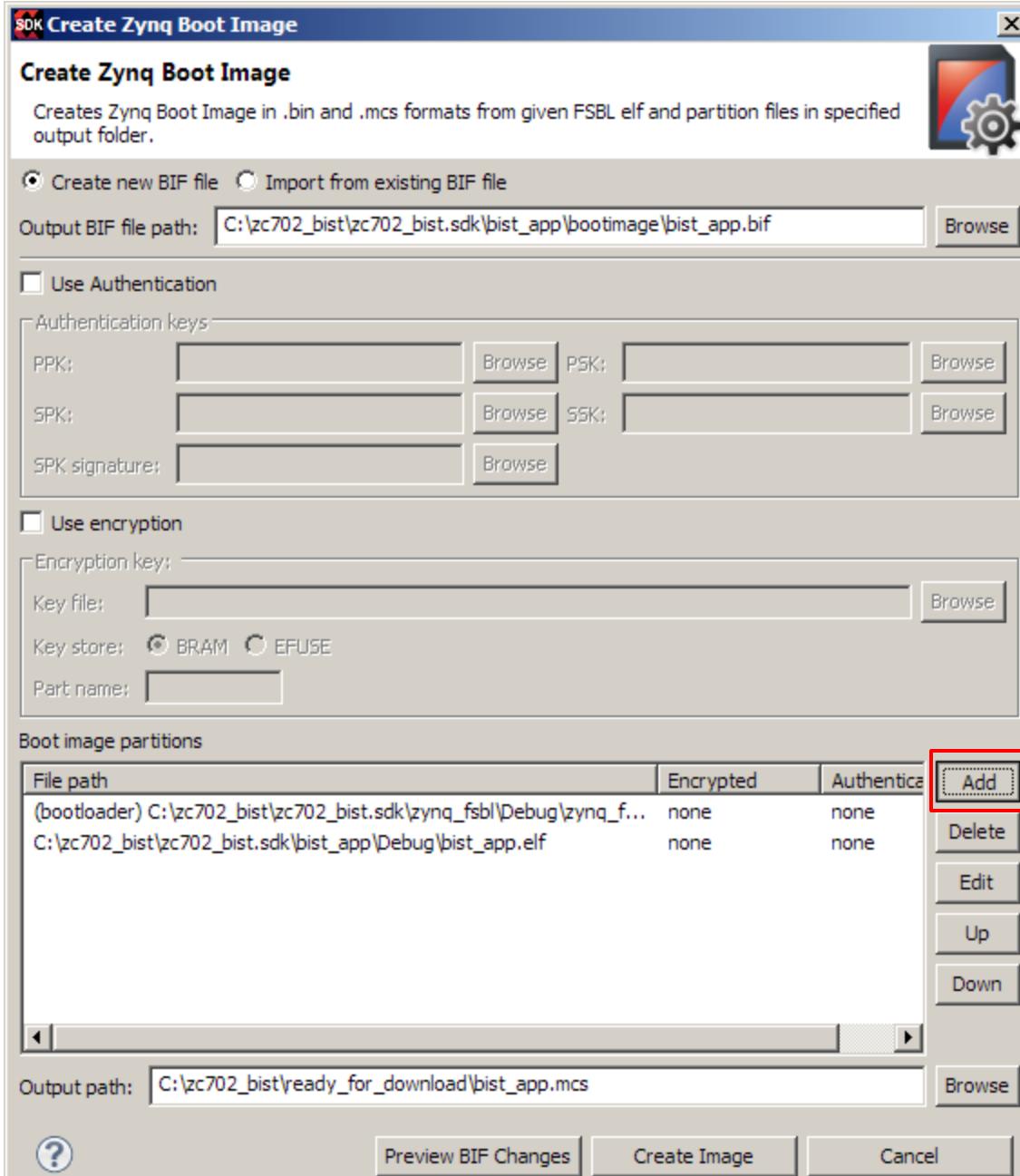
# Creating a BOOT Image

- Select `bist_app`
- Select Xilinx Tools → Create Zynq Boot Image



# Creating a BOOT Image

- Create the BIST MCS
- Use the default BIF file path
- Set the Output path to:
  - C:\zc702\_bist\ready\_for\_download\bist\_app.mcs
- Click Add

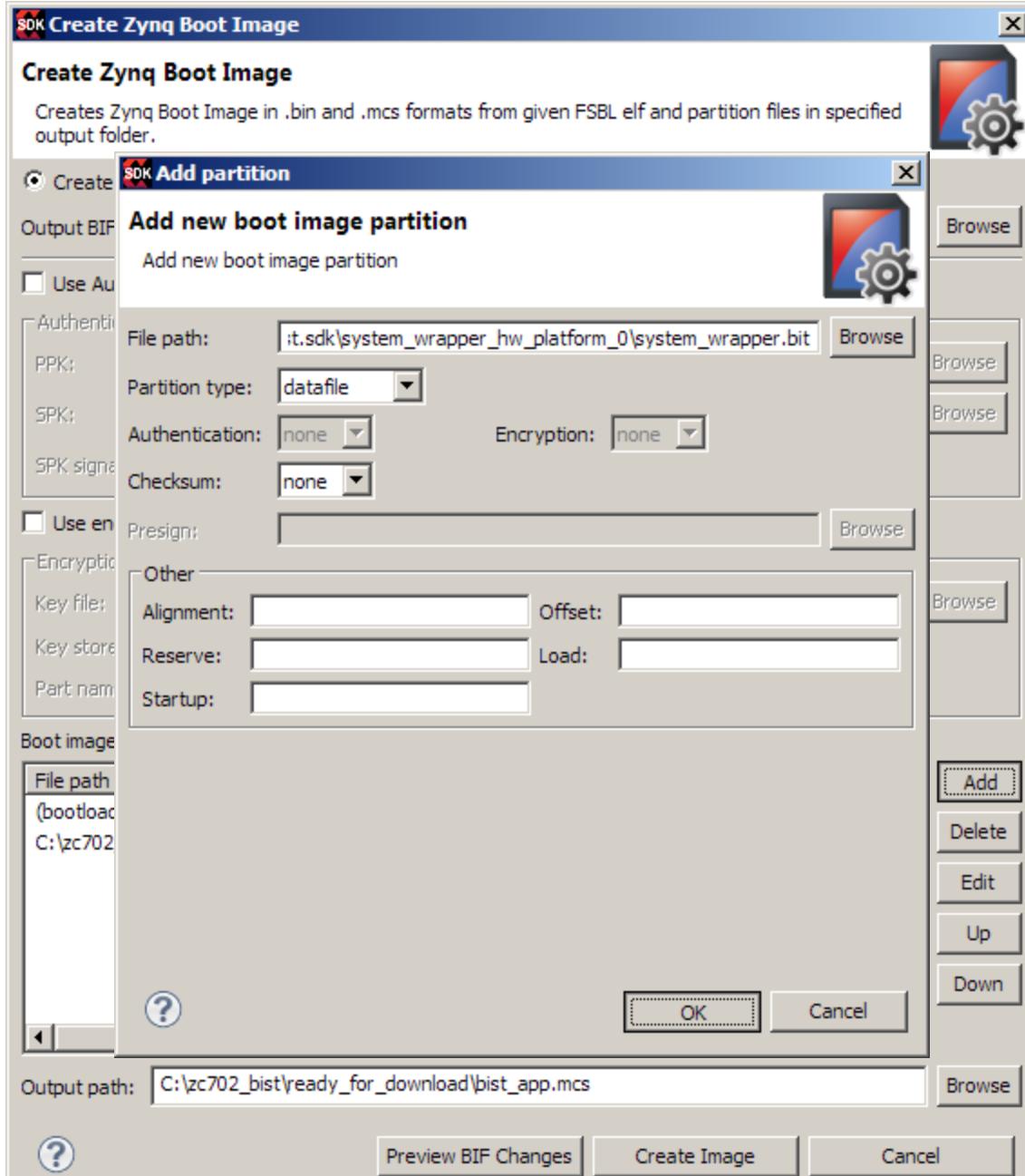


# Creating a BOOT Image

## ► Select the bitstream:

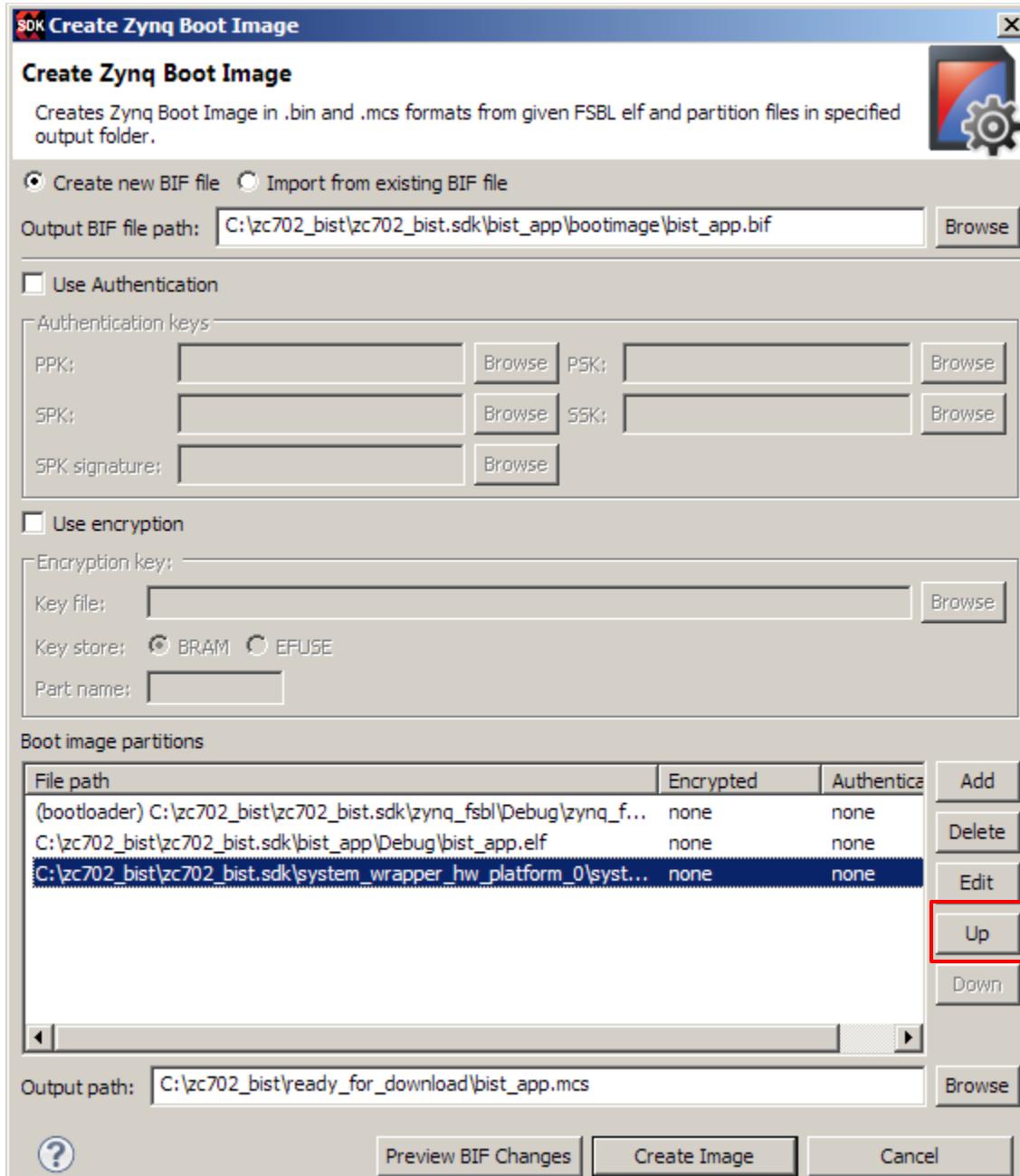
- C:\zc702\_bist\zc702\_bist.sdk\system\_wrapper\_hw\_platform\_0\system\_wrapper.bit

## ► Click OK



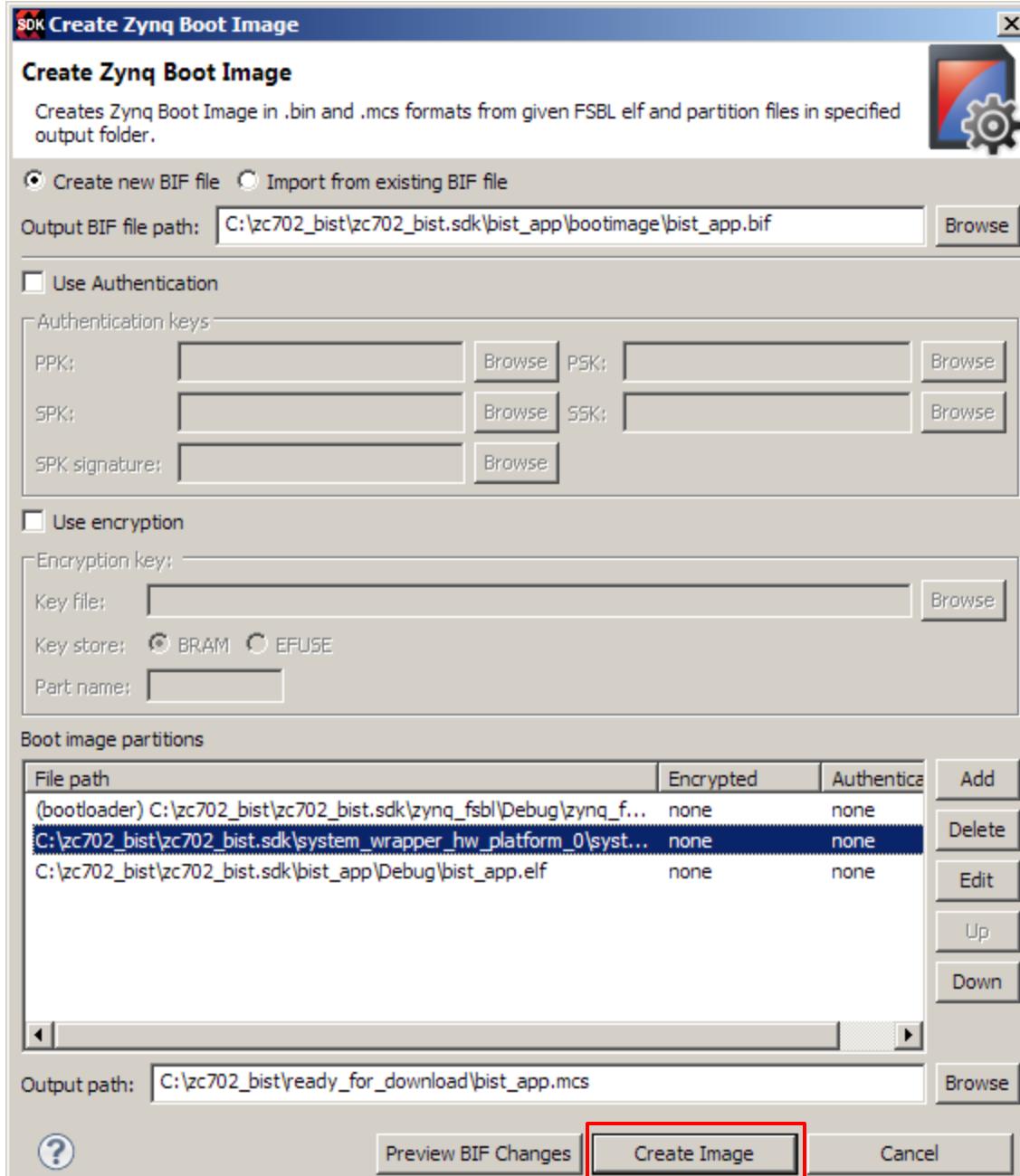
# Creating a BOOT Image

➤ Select the bitstream item in the list and use the Up button to move the bitstream to second place



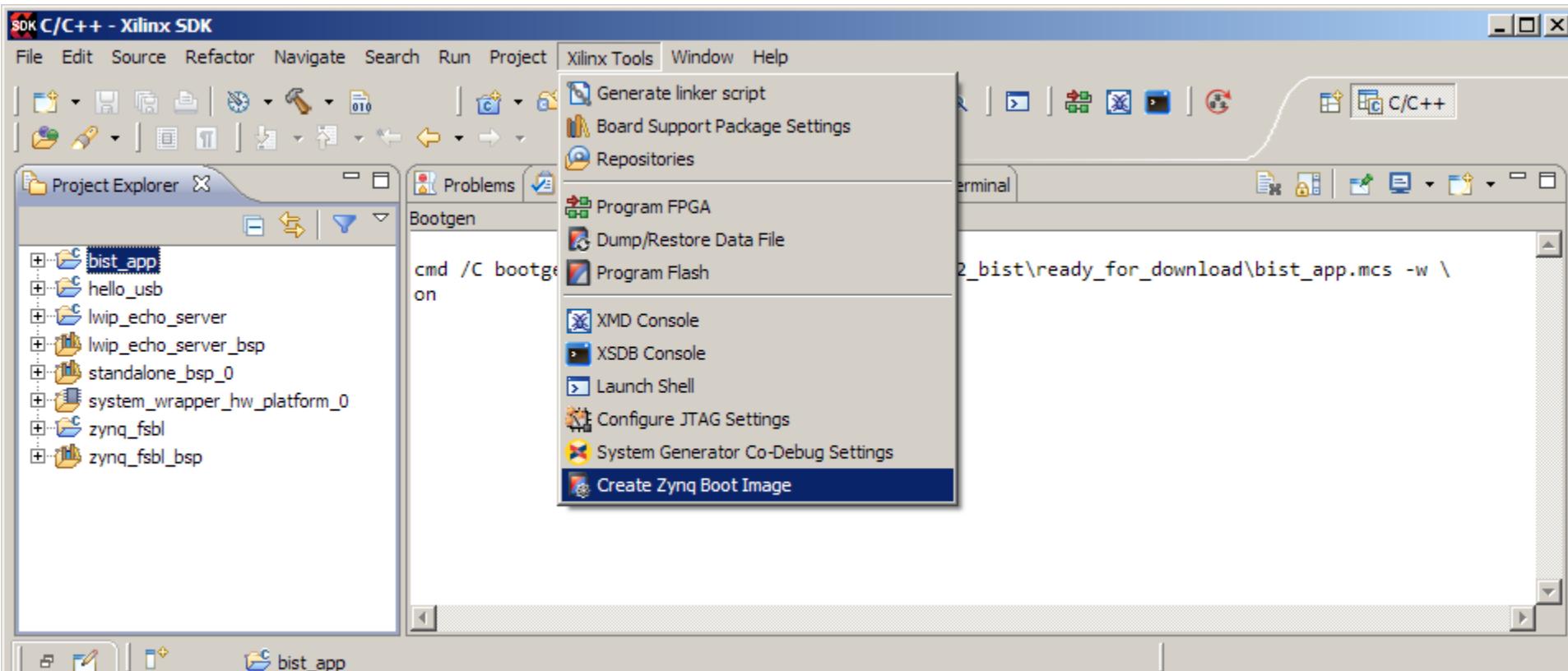
# Creating a BOOT Image

► Click “Create Image”



# Creating a BOOT Image

- With **bist\_app** still selected, select **Xilinx Tools** → **Create Zynq Boot Image**



# Creating a BOOT Image

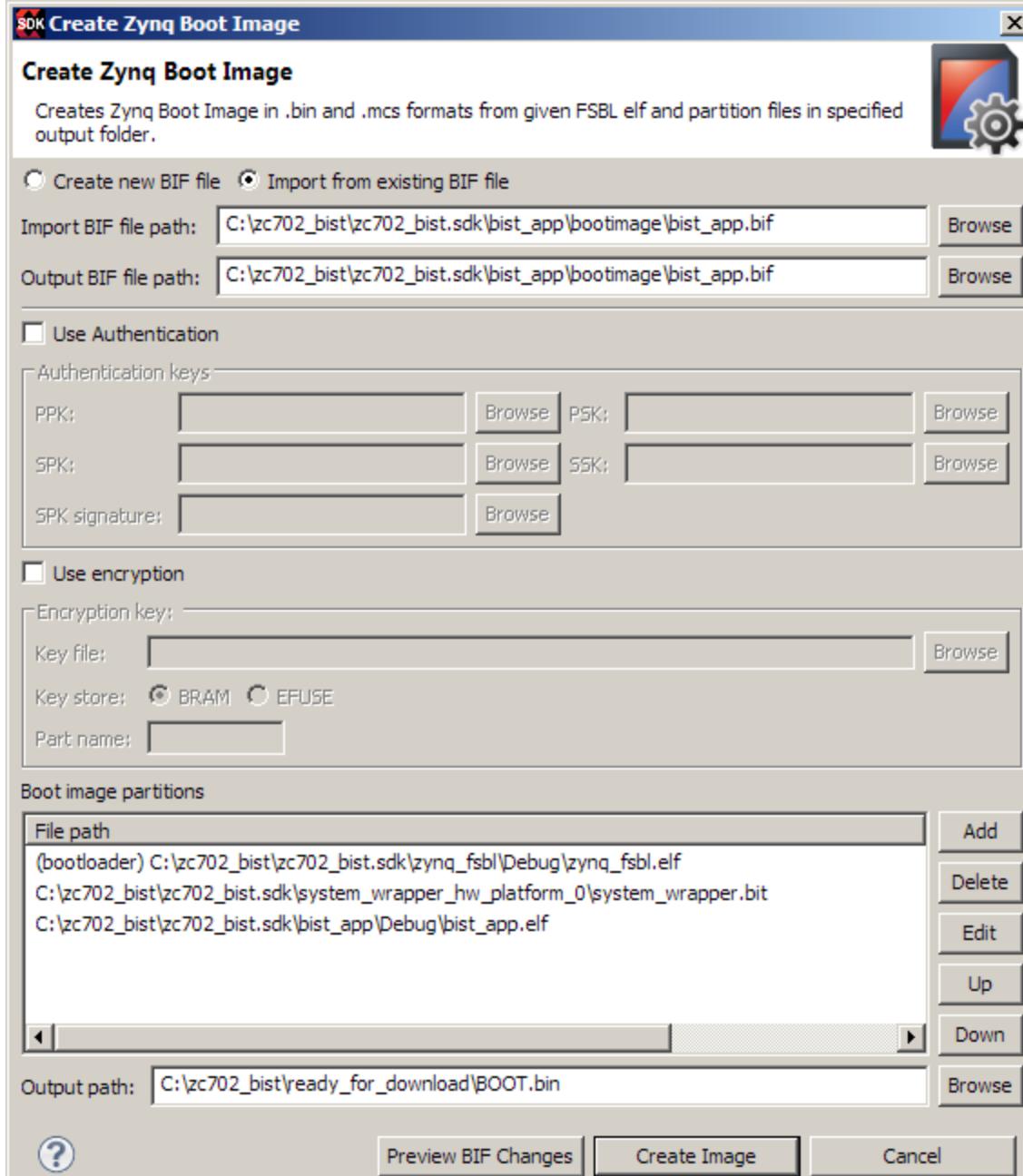
## ➤ Import the BIST BIF file

- The tool reloads your previous settings

## ➤ Set the Output path to:

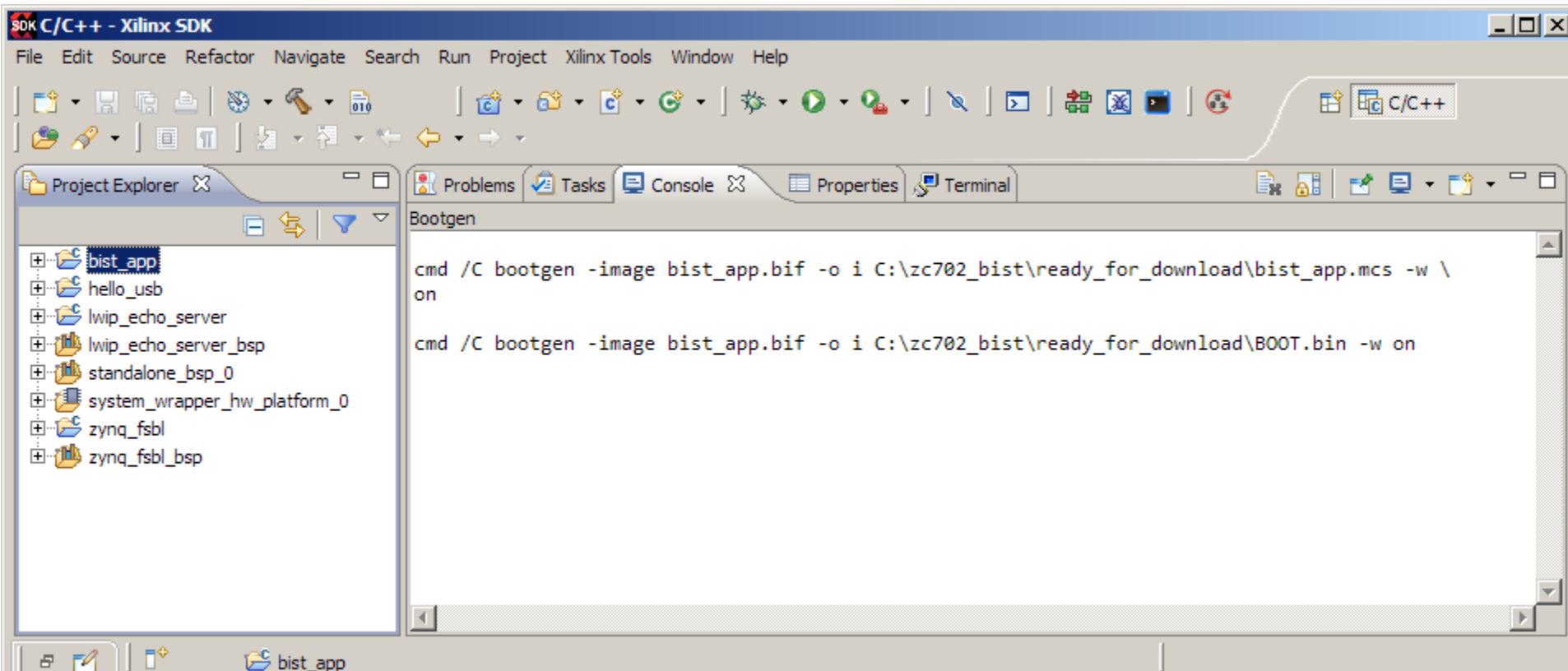
- C:\zc702\_bist\ready\_for\_download\BOOT.bin

## ➤ Click “Create Image”



# Creating a BOOT Image

- Two files are created:
    - bist\_app.mcs for programming the Flash
    - BOOT.bin for use on an SD card



**Note:** Presentation applies to the ZC702

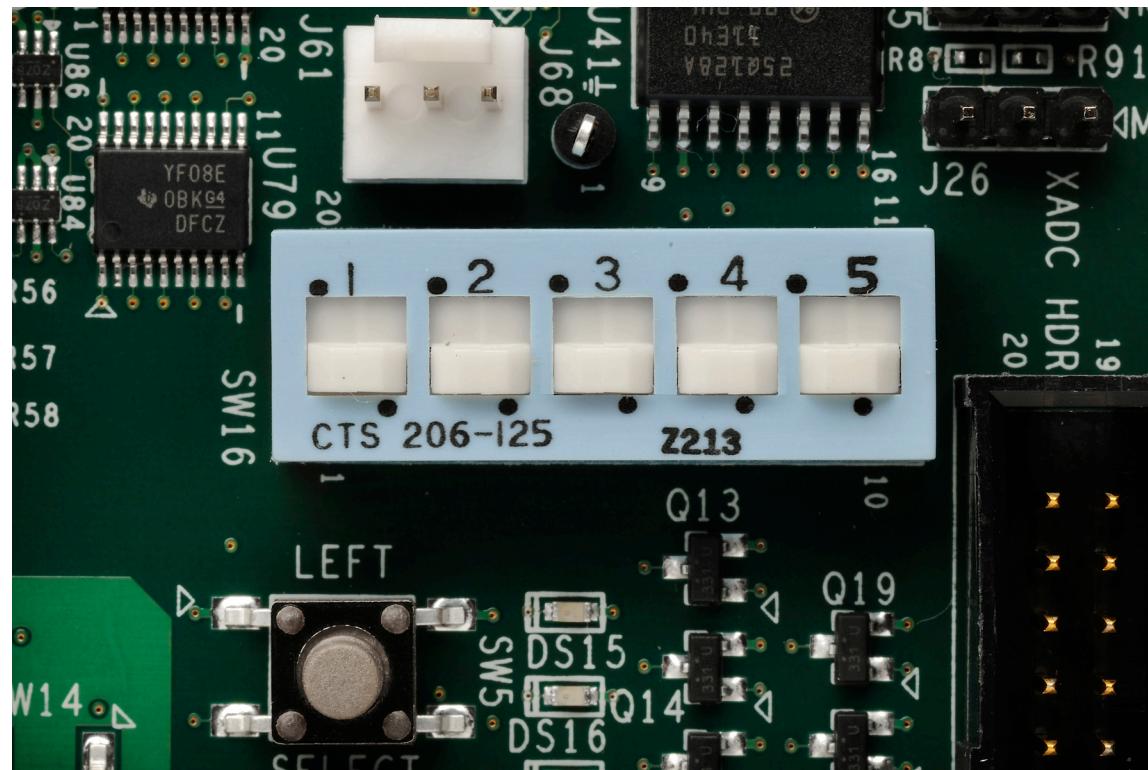
 XILINX  ALL PROGRAMMABLE™

# Programming the ZC702 QSPI

# Programming the ZC702 QSPI

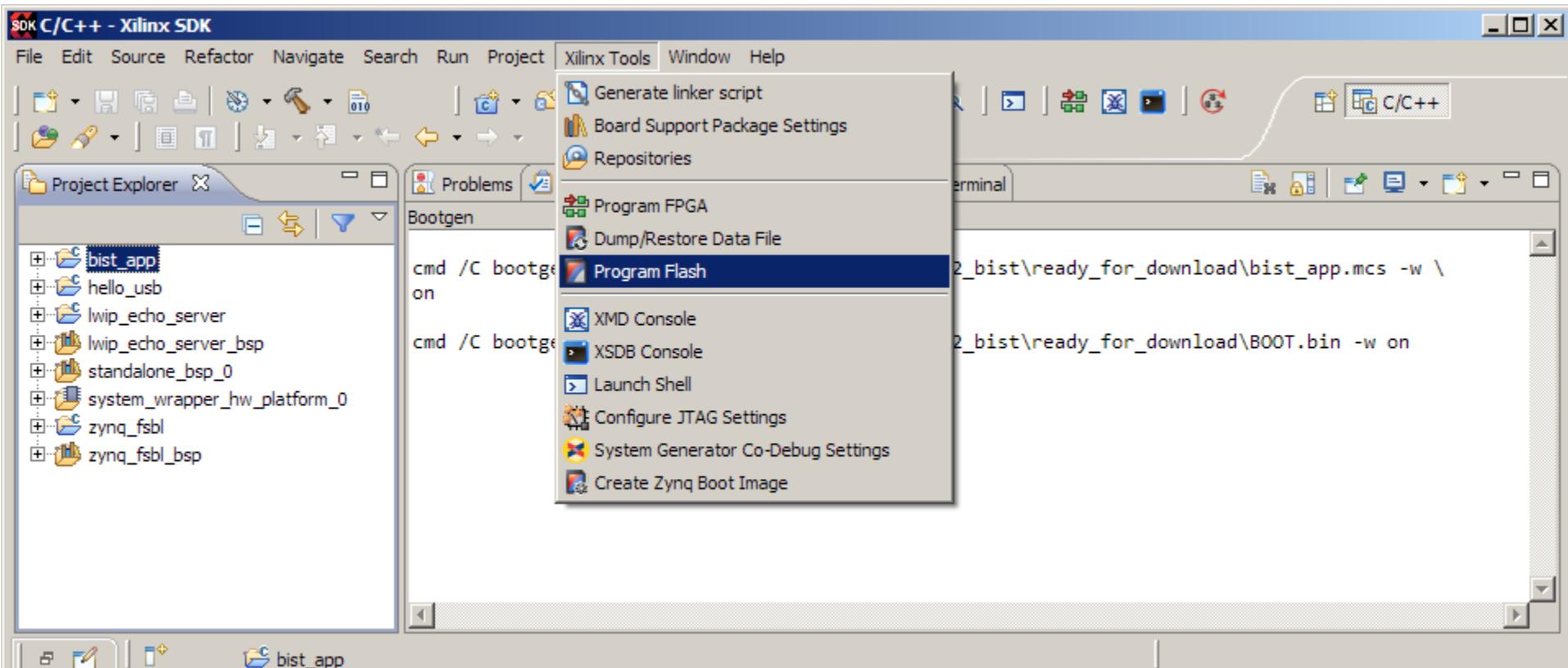
## ► Set SW16 DIP Switches to 00000

- As per [AR52143](#), if using “CES” Silicon, set the mode pins to 00010
- Cycle board power



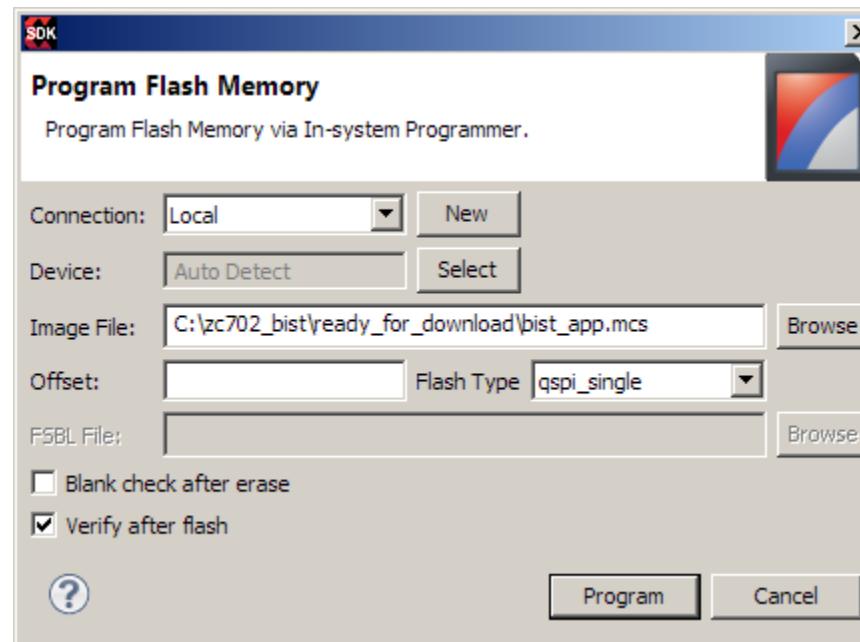
# Programming the ZC702 QSPI

► Select Xilinx Tools → Program Flash



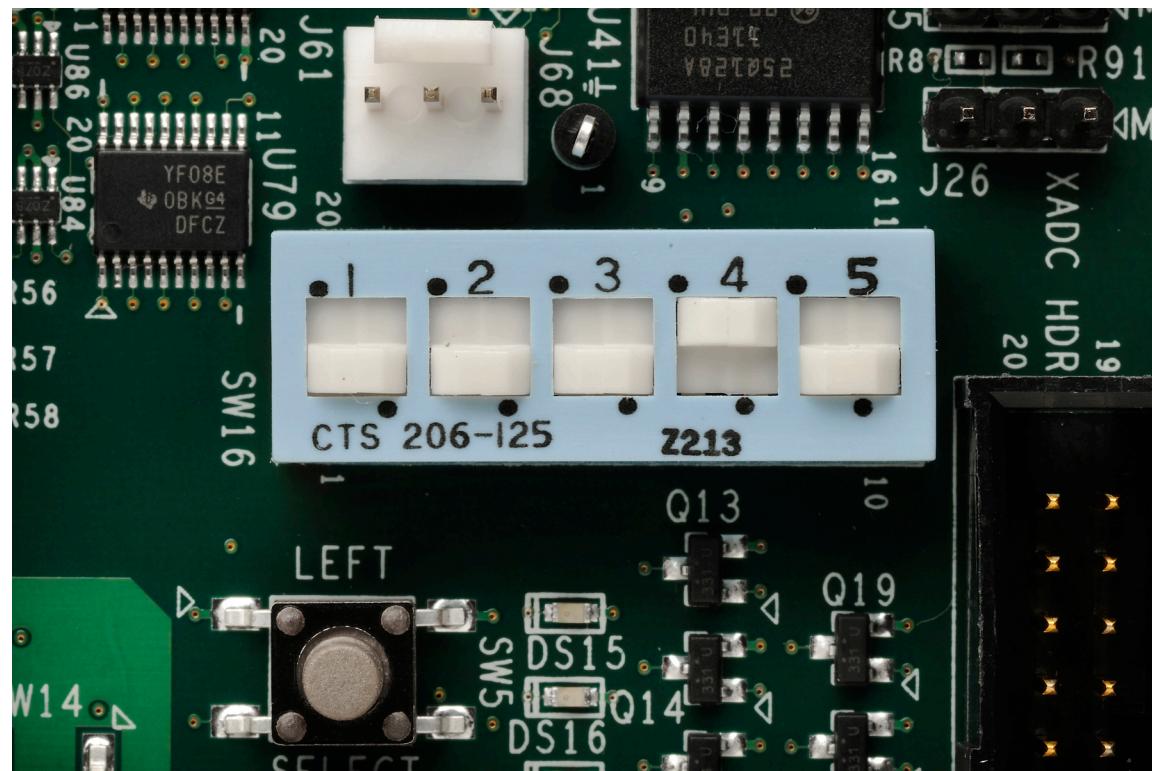
# Programming the ZC702 QSPI

- Select the `bist_app.mcs` as the image file
- Set Flash Type to `qspi_single` and select Verify
- Click Program



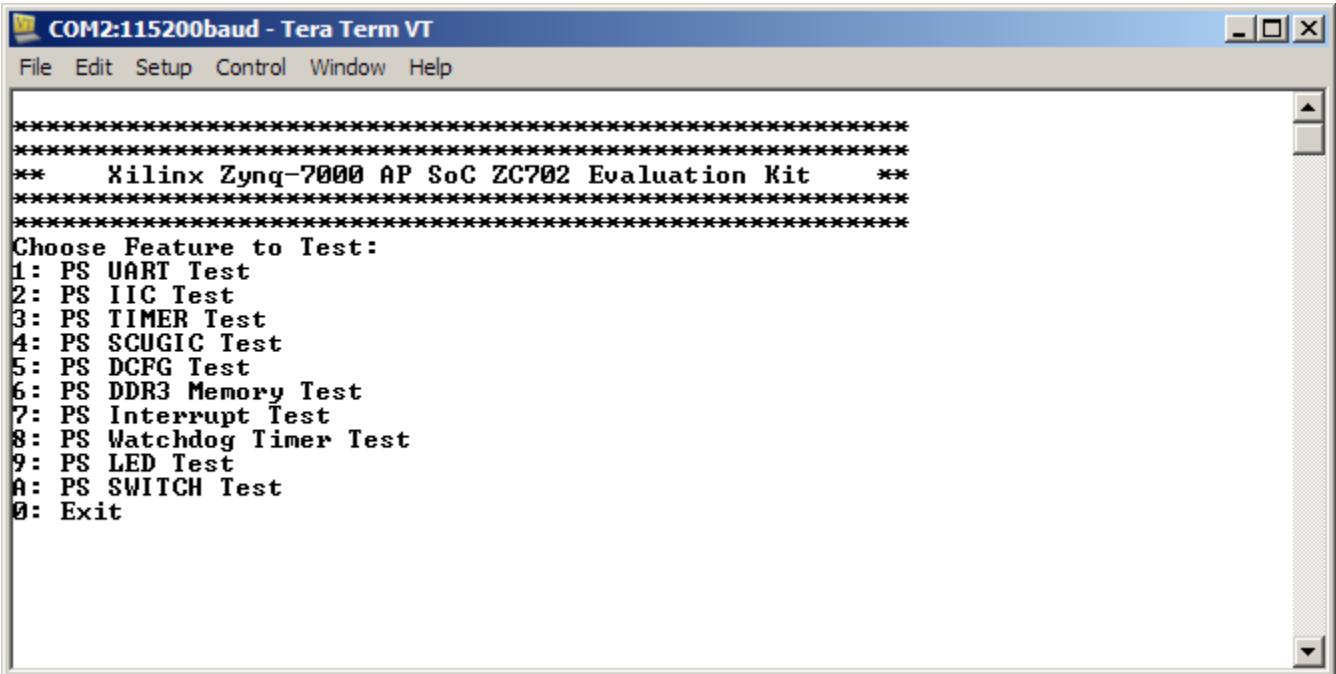
# Programming the ZC702 QSPI

- After programming is complete, set the SW16 DIP switches to boot from QSPI: 00010



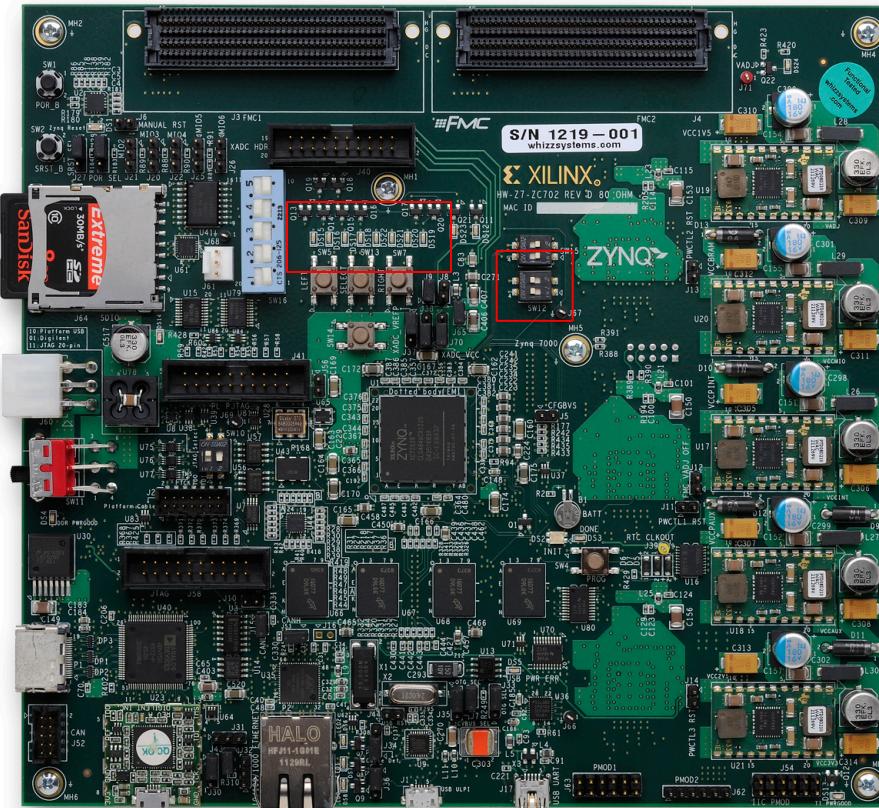
# Programming the ZC702 QSPI

## ► Push POR\_B Button (SW1)



# Programming the ZC702 QSPI

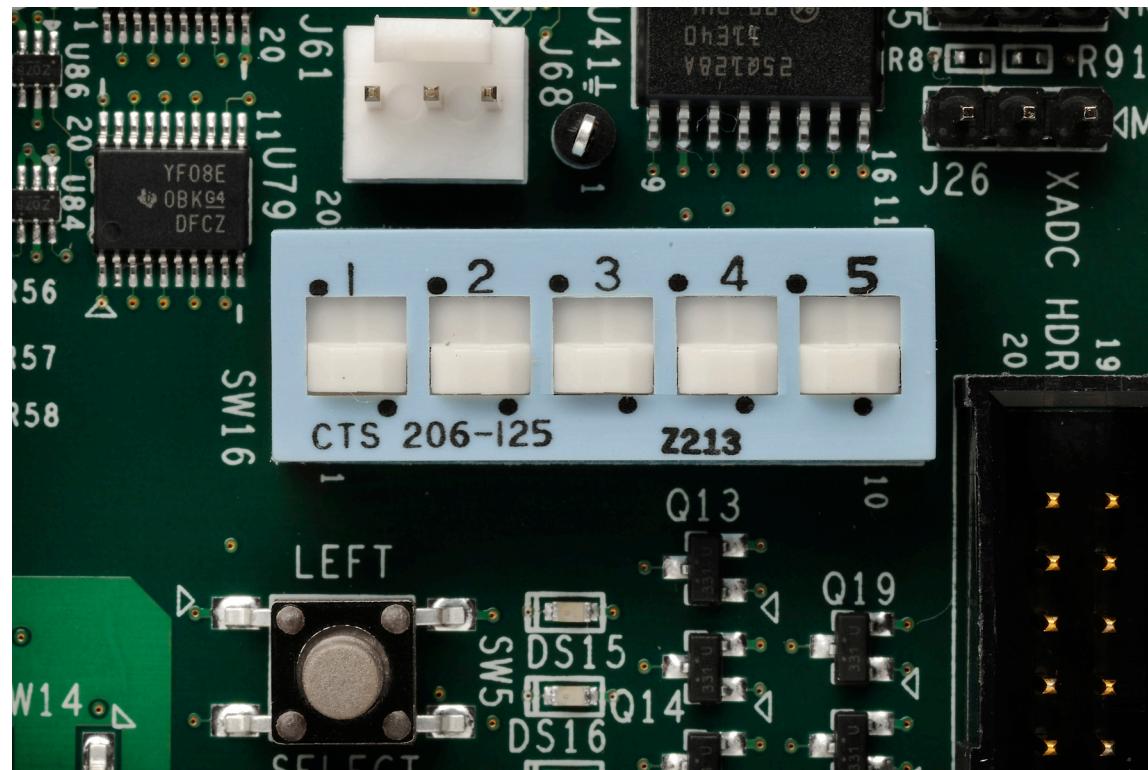
- The PL LEDs will be blinking in a pattern controlled by SW12



# **Run the USB Design from SDK**

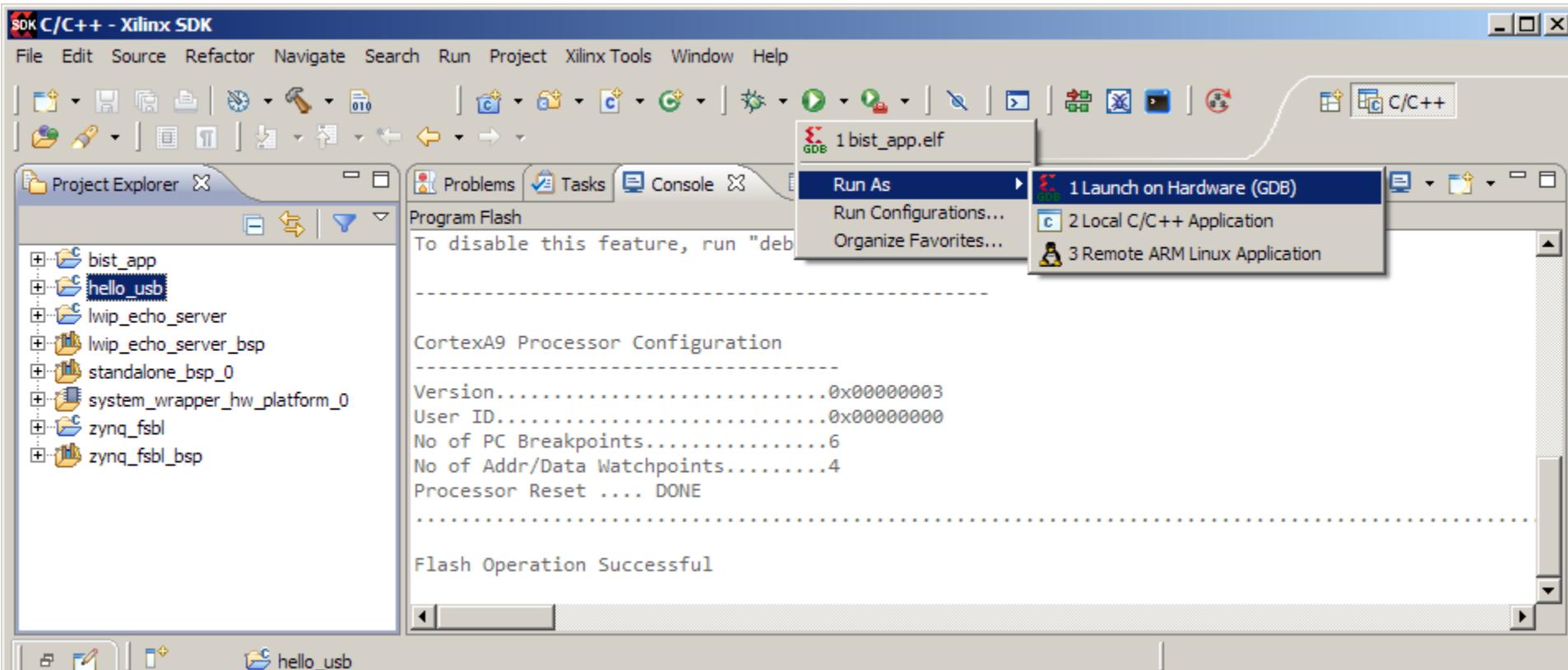
# Run the USB Design from SDK

- Set SW16 DIP Switches to 00000
- Cycle board power



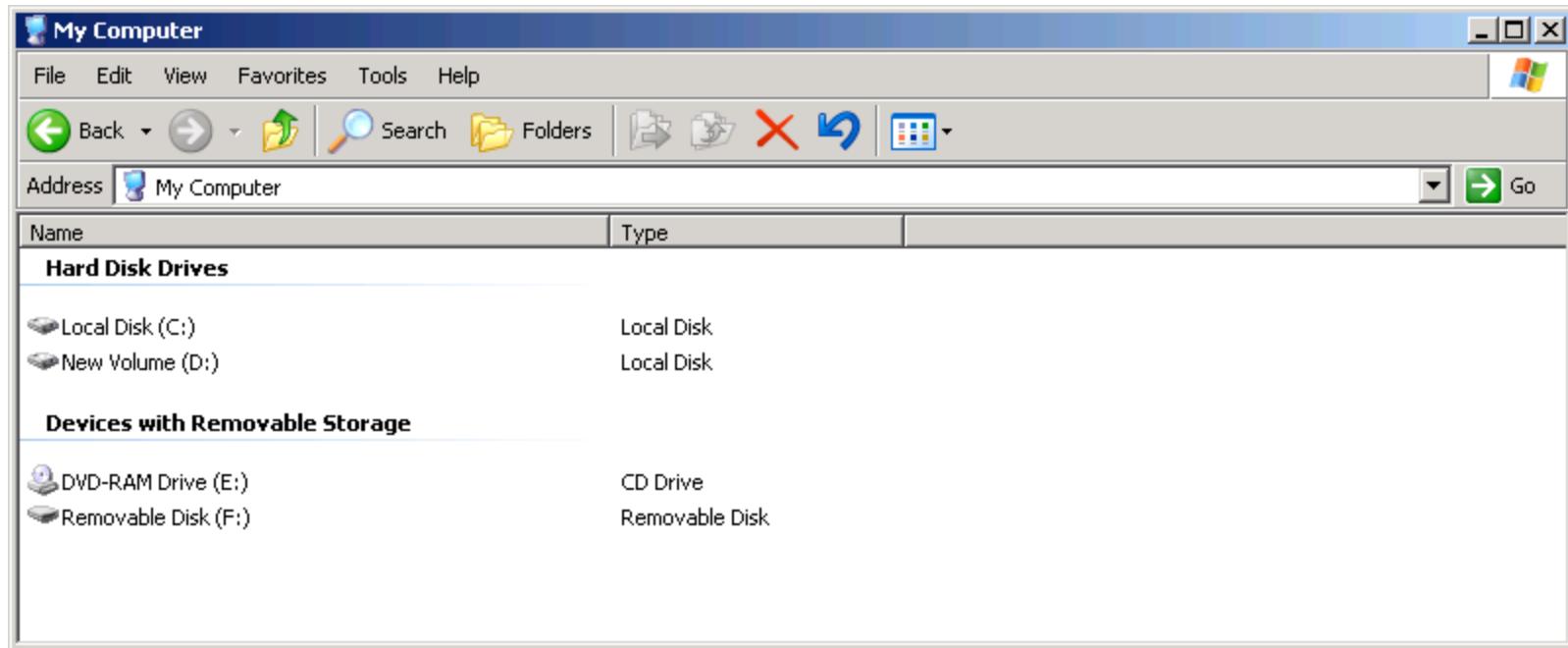
# Run the USB Design from SDK

- Select “hello\_usb”
- Under the green “Run” button, select Run As → Launch on Hardware



# Run the USB Design from SDK

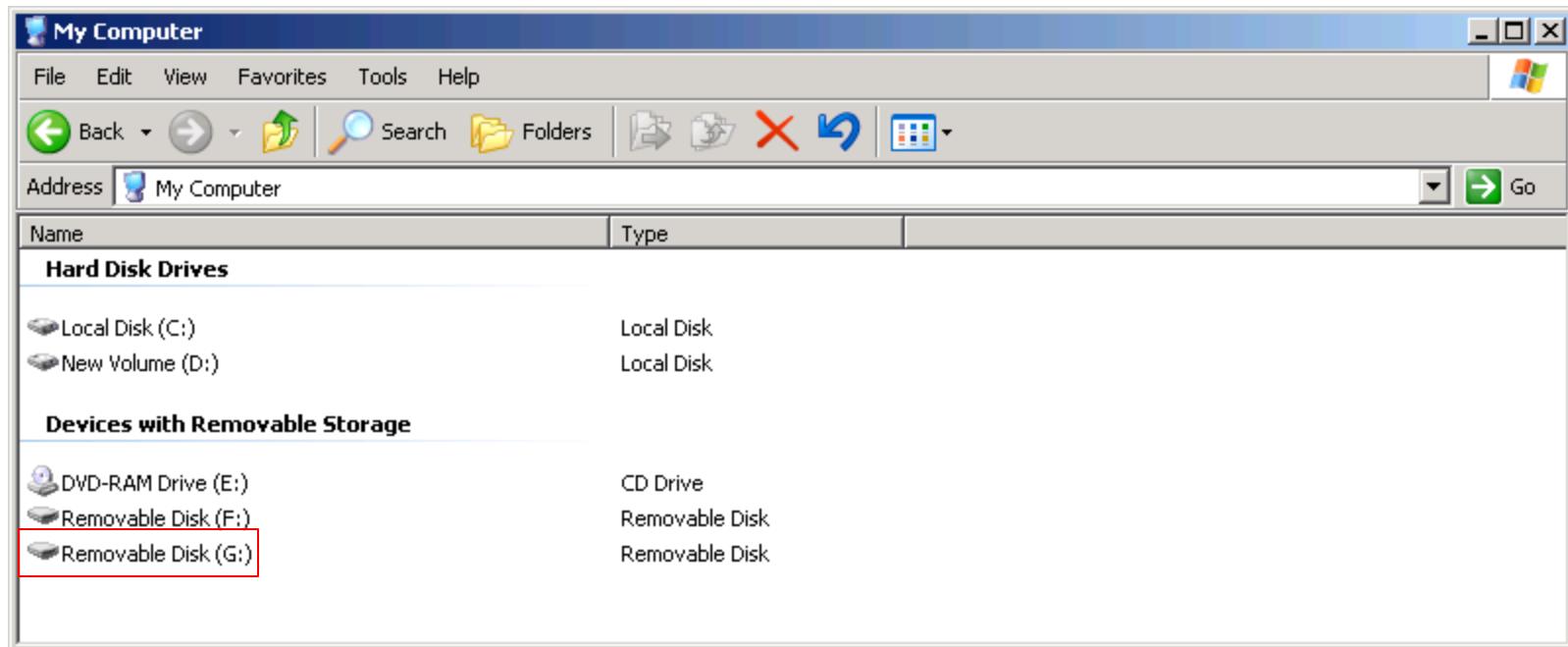
- ▶ View your current set of disk drives



# Run the USB Design from SDK

- An extra removable drive will appear

- In this case, “G:”

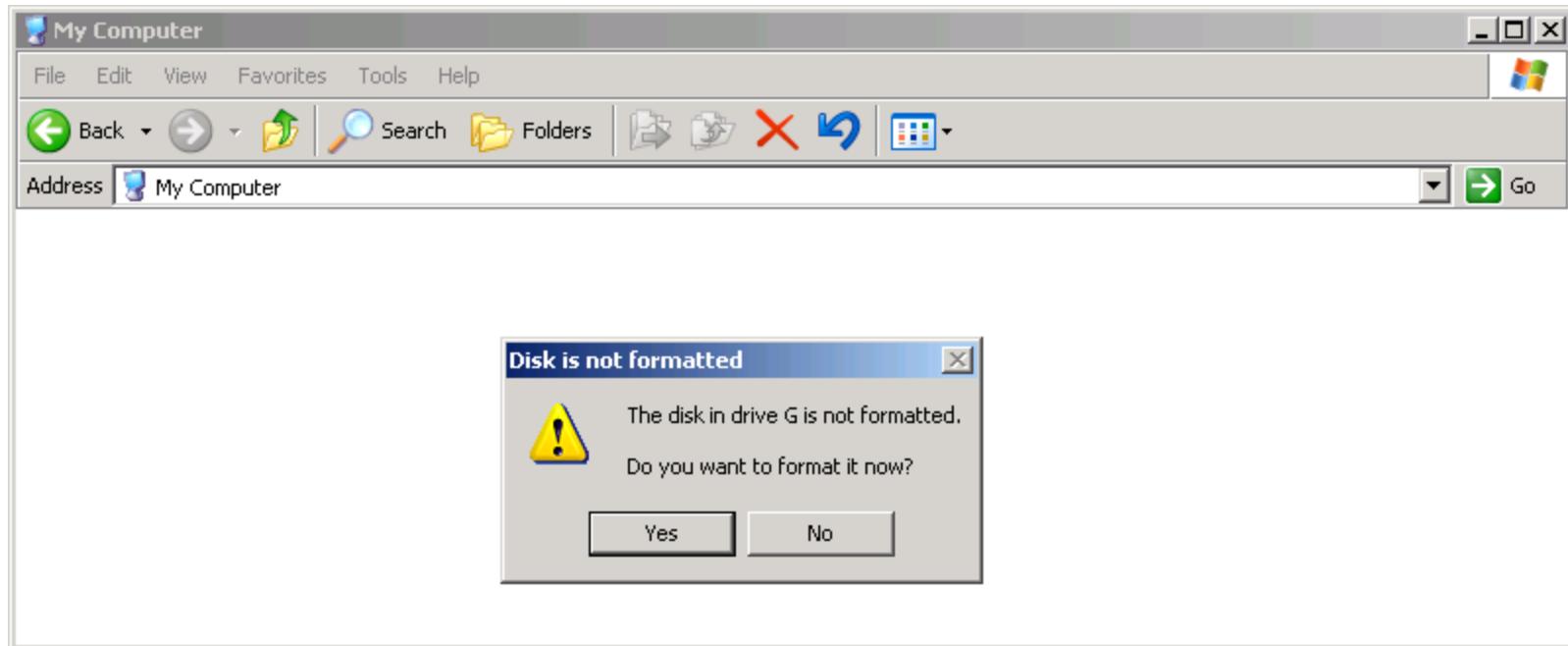


# Run the USB Design from SDK

## ► Open the “G:” drive

- A “Disk is not formatted” message will appear

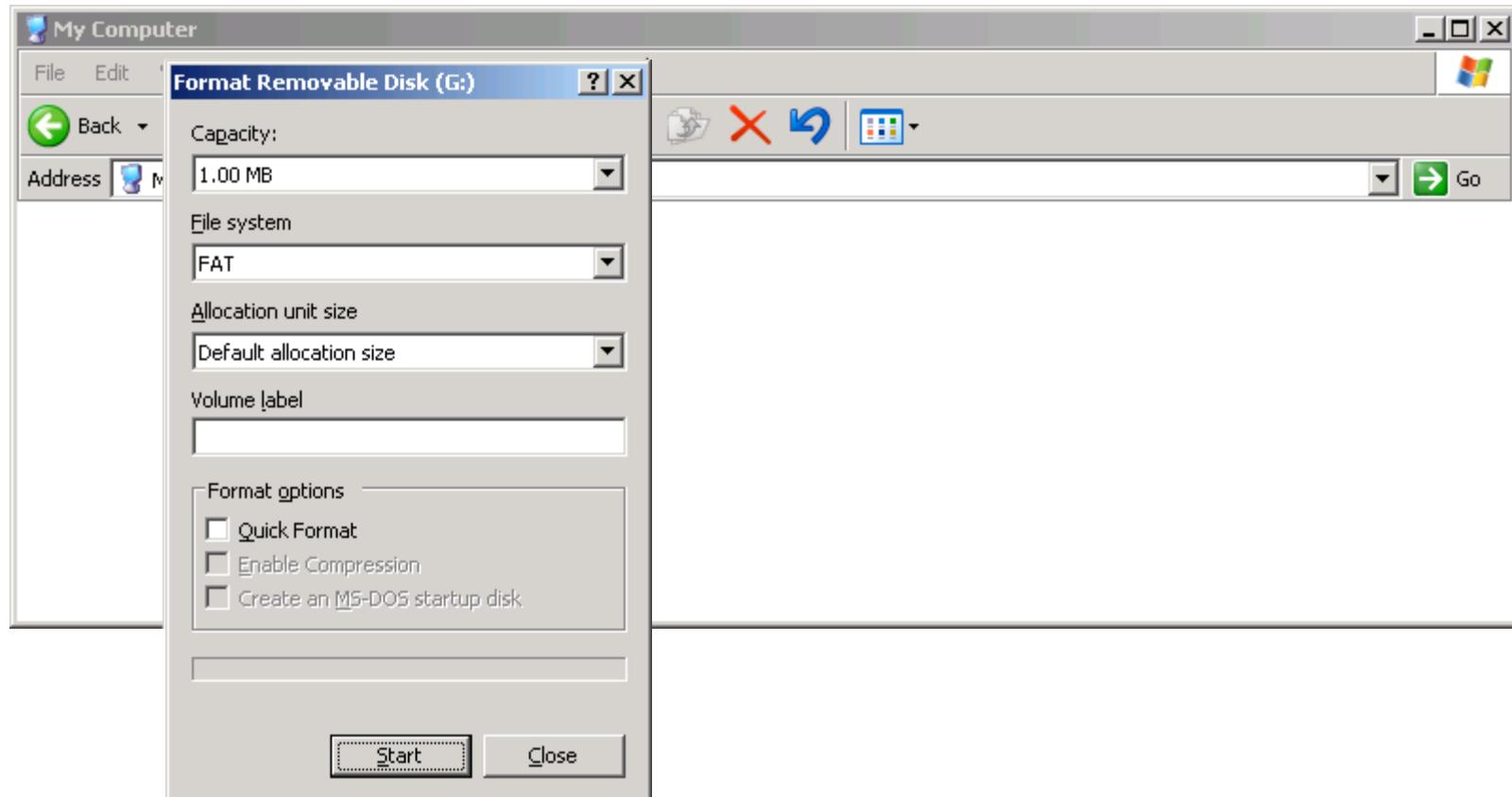
 If this is the correct drive, click **Yes**; if not, click **No**



# Run the USB Design from SDK

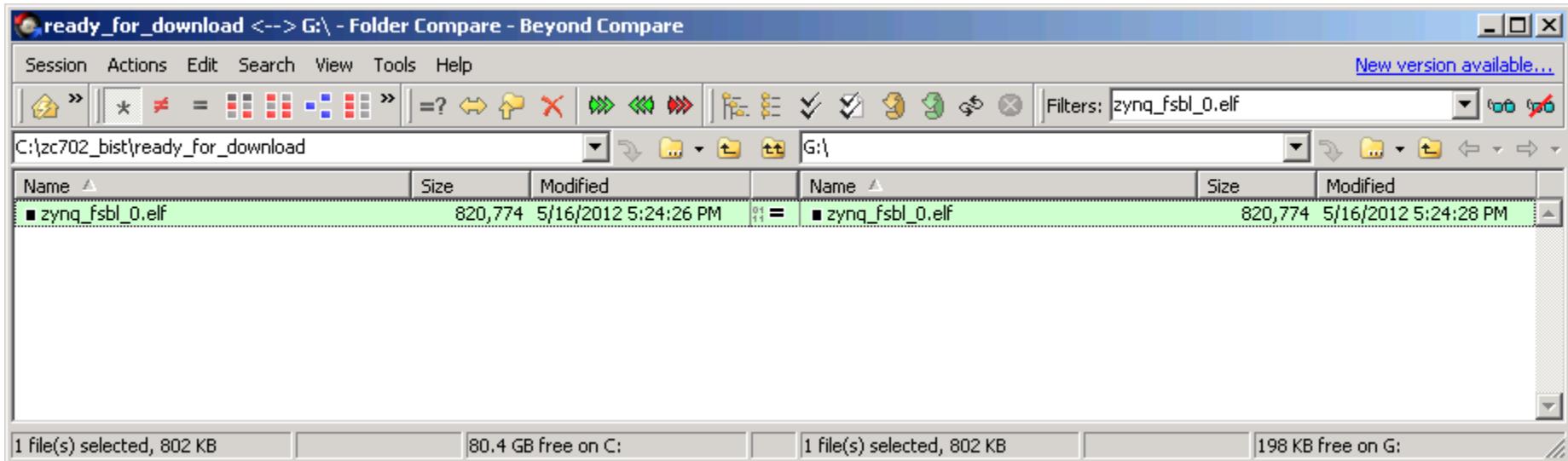
## ► A format dialog for drive G: will appear

- The size should be 1.00 MB
- If this is the correct, click **Start**
- Close this dialog when done



# Run the USB Design from SDK

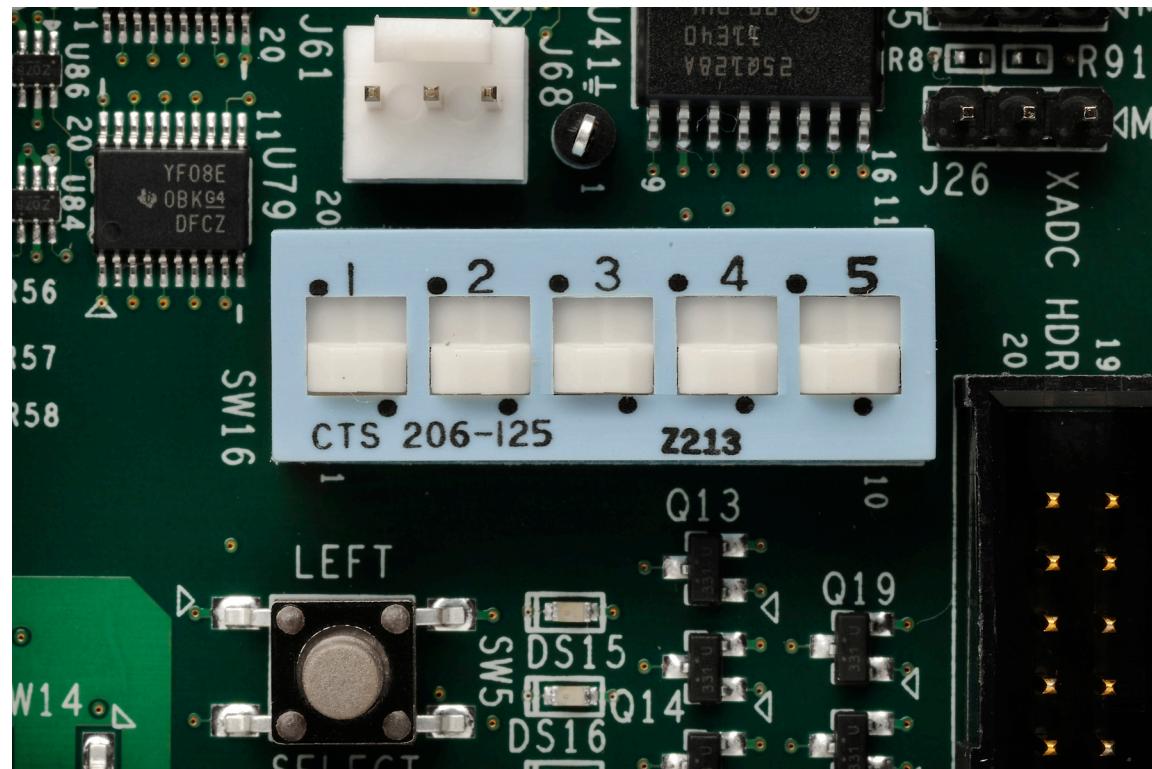
- At this point, you can copy small files to G: and verify the operation of this drive



# Run the LwIP Ethernet Design

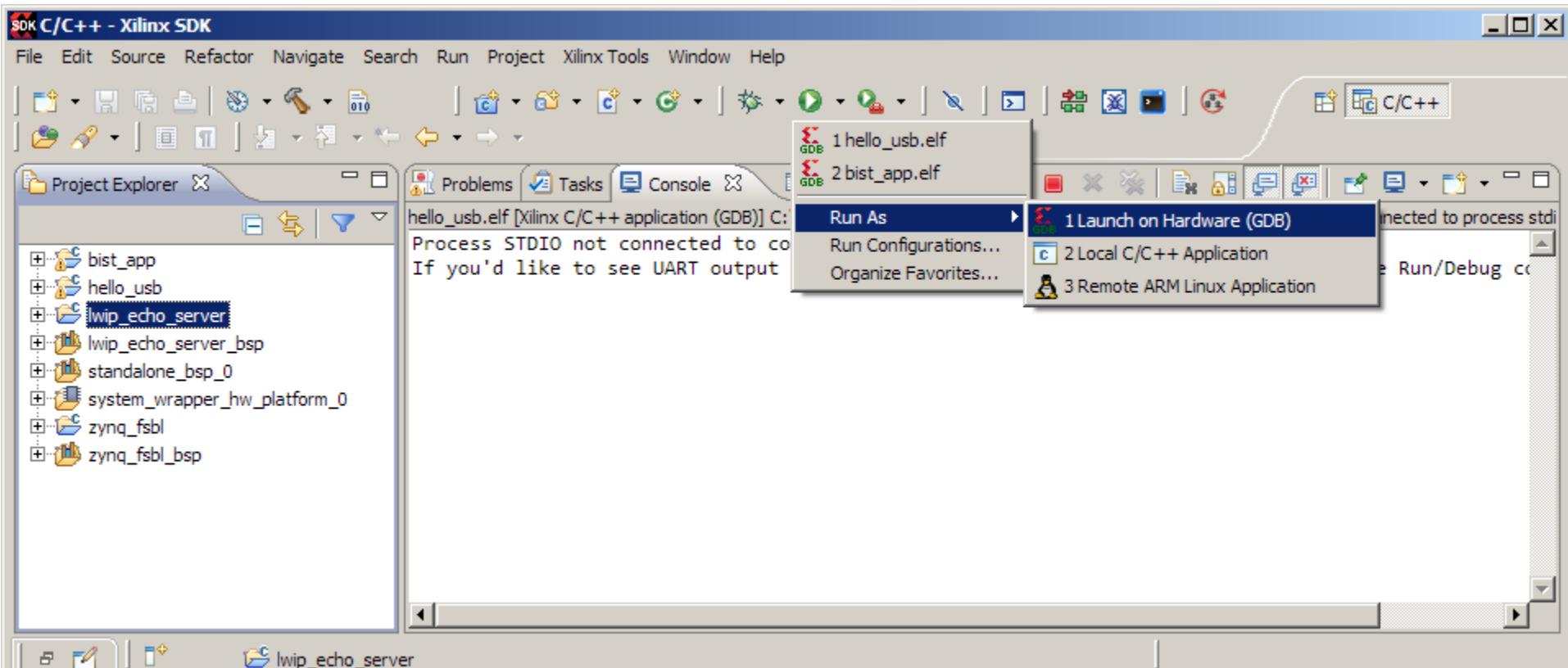
# Run the LwIP Ethernet Design

- Set SW16 DIP Switches to 00000
- Cycle board power



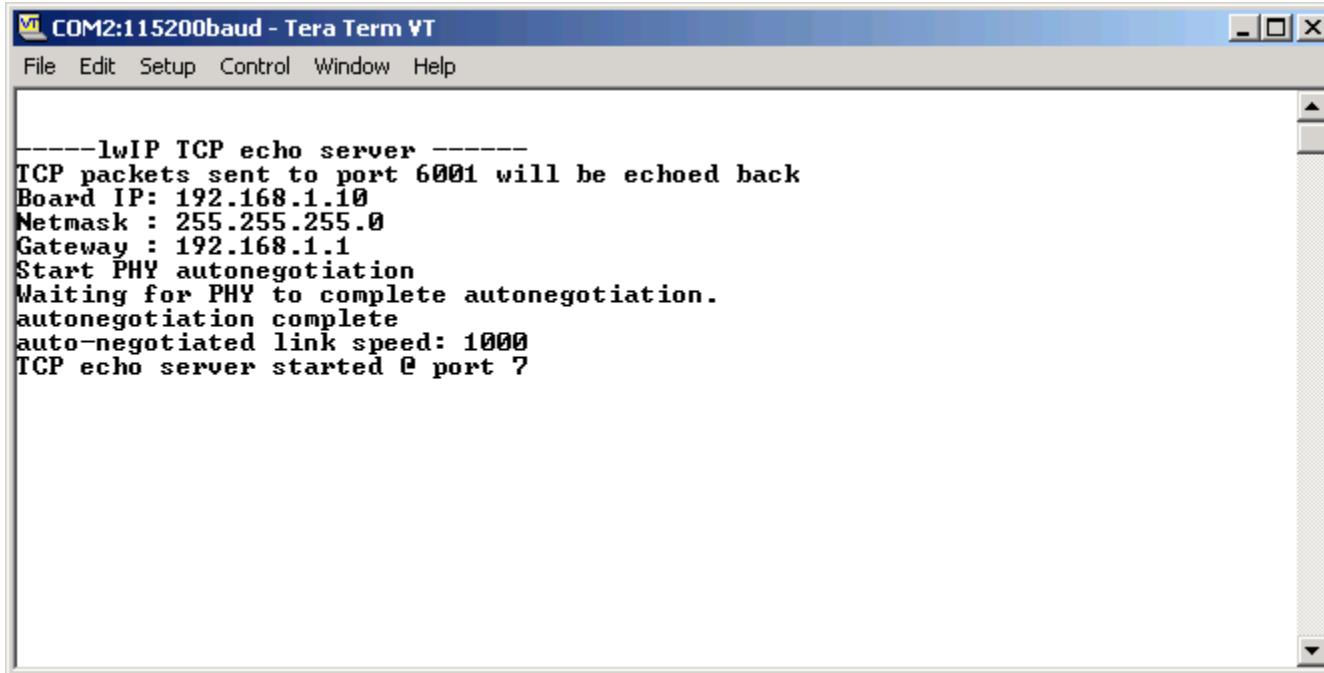
# Run the LwIP Ethernet Design

- Select “lwip\_echo\_server”
- Under the green “Run” button, select Run As → Launch on Hardware



# Run the LwIP Ethernet Design

## ► View LwIP echo server screen



The screenshot shows a terminal window titled "COM2:115200baud - Tera Term VT". The window contains the following text output from the LwIP TCP echo server:

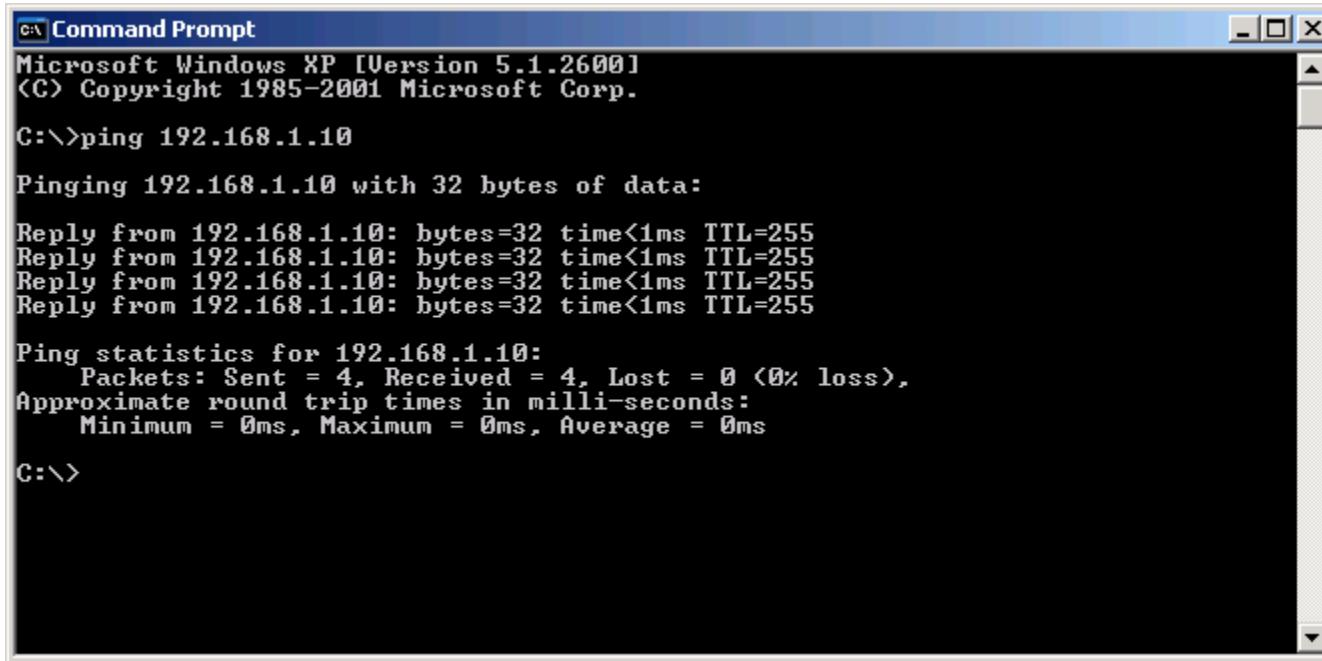
```
----lwIP TCP echo server ----
TCP packets sent to port 6001 will be echoed back
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation.
autonegotiation complete
auto-negotiated link speed: 1000
TCP echo server started @ port 7
```

# Run the LwIP Ethernet Design

► From a DOS window on the PC Host, enter the command:

**ping 192.168.1.10**

- Ping from PC host 192.168.1.2 to ZC702 target 192.168.1.10



```
C:\Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:

Reply from 192.168.1.10: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\>
```

## References

# References

## ► IP Integrator Documentation

- Vivado Design Suite Tcl Command Reference Guide
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2014\\_2/ug835-vivado-tcl-commands.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug835-vivado-tcl-commands.pdf)
- Designing IP Subsystems Using IP Integrator
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2014\\_2/ug994-vivado-ip-subsystems.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_2/ug994-vivado-ip-subsystems.pdf)

## ► 7 Series Configuration

- 7 Series FPGAs Configuration User Guide
  - [http://www.xilinx.com/support/documentation/user\\_guides/ug470\\_7Series\\_Config.pdf](http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf)

# Documentation

# Documentation

## ➤ Zynq-7000

- Zynq-7000 All Programmable SoC
  - <http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm>

## ➤ ZC702 Documentation

- Zynq-7000 AP SoC ZC702 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/EK-Z7-ZC702-G.htm>
- ZC702 Getting Started Guide – UG926
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/zynq-7000/zc702\\_gsg/v3\\_0/UG926\\_Z7\\_ZC702\\_Eval\\_Kit.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/zynq-7000/zc702_gsg/v3_0/UG926_Z7_ZC702_Eval_Kit.pdf)
- ZC702 User Guide – UG850
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/zc702\\_zvic/ug850-zc702-eval-bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/zc702_zvic/ug850-zc702-eval-bd.pdf)