

# Placement optimization for field effect transistors

**Abstract.** In this fast-paced world where technology has been established in all aspects of human society, there is a constant demand for higher processing capabilities with smaller packaging which leads to increased power dissipation per unit volume. This warrants innovative and more efficient cooling solutions. A Printed circuit board (PCB) is a layered insulating board which mechanically supports the semiconductor chips and facilitates electrical connection between them through an etched metallic coating (usually copper) laminated on its surface. The components are fastened to the PCB by means of solder. Due to increasing density and number of heats producing components, it becomes necessary to decrease the overall temperature of the PCB before installing the cooling system, the heat producing elements must be optimally placed so as to not be too close to the boundary nor be in the range to thermally interfere with other chips, to prevent localized high temperature regions which could further damage the PCB. This is done through the process of PCB optimization, where prior data from thermal simulations will be used to generate an optimized layout to minimize the board temperature. In the first phase of our project, we worked on modelling the board, chips and enclosure. We made several approximations to start of with, and slowly refined the model in successive steps. Our goal is to create a model as close to reality as possible, and use this to optimize the placement of the chips and various parameters involved.

**Keywords:** Thermal Modelling, Simulation, Placement Optimization.

## 1 Introduction

Thermal management of electronic components is essential in this day and age because of the increasing density of electronic components. Improper placement of the chips has adverse effects on the longevity and efficiency of the chips. It is becoming increasingly important to ensure proper placement of the components. To maintain the operating temperature below the optimum temperature, optimization and various cooling methods are employed.

Suwa et al. [3] talked about the optimization of PCB board layout subject to multiple objectives and pre-defined constraints. The overlap and thermal penalties included made sure the GA learnt to avoid those in order to minimize the

function. Studies were conducted to find initial population size and number of generations. The methodology was then used on a real-world application and the results were shown.

Ismail et al. [1] presents a new type of genetic algorithm to solve the multi objective function used to optimize the PCB layout. The SOGA approach will ensure an optimal placement of each electronic component on PCB by minimizing the objectives function simultaneously while satisfying a few constraint parameters. In this paper resistance thermal network is used to predict the junction temperatures.

Jain et al. [2] presents an approach to find the optimal design layout of chips on a circuit board in a manner that minimizes the area covered on the board and the connections between the various chips. The authors demonstrate the working with an example. They tweak different parts of the objective function and show the difference in final output as well.

Tohru et al. [4] introduces a multidisciplinary optimization methodology for placement of heat generating semiconductor logic blocks on integrated circuit chips. The thermal and wiring length criteria is simultaneously optimized using genetic algorithm. The main advantage of the present multidisciplinary design and optimization methodology is its ability to handle multiple design objectives simultaneously for optimized placement of heat generating logic blocks.

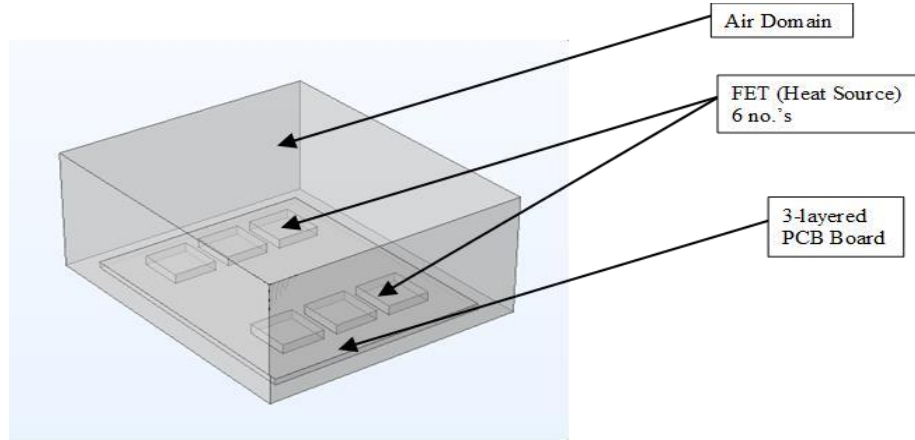
From the literature reviewed the main points and methods to best optimize the placement are summarized. The placement of the chips has a major effect on the junction temperatures of the FET's. The other factors affecting the junction temperature is local heat generation through copper traces, copper distribution, placement of vias and thermal resistance of components such as PCB and heat sink. Higher ambient temperature has a negative impact on the performance of the IC. Size reduction and overlapping algorithms can be incorporated to reduce the overall area occupied by the PCB, decreasing the weight of the heat sink to be coupled. The papers reviewed have used approximations for the model and the trade-off between decrease in modelling complexity vs the accuracy of the obtained results was not studied.

## **2 Methodology**

### **2.1 Problem Formulation**

FET has a maximum temperature which cannot be exceeded without destroying the device or at least shortening its life. The heat is generated in a bipolar transistor directly under the emitters and very close to the upper surface of the die. For all practical purposes, the heat is considered to be generated throughout the volume of the chip or die. The maximum power rating of the transistor is largely governed by the temperature of the collector/base junction as can be seen from [5], if too much power is dissipated, this junction gets too hot and the transistor will be destroyed as such, the performance of a power transistor is closely dependent on its ability to dissipate the heat generated at the junction.

## 2.2 PCB Modelling



**Fig. 1.** Geometric model of PCB with FET's surrounded by an air domain.

Geometric Modelling. In order to collect data for the ANN, a simple model of the PCB was constructed. 6 FETs were placed vertically upon a 3-layered PCB. The PCB contains alternate layer of copper and FR4, the copper layer being the traces of the PCB. This PCB is then surrounded by an air domain to mimic the effect of an enclosed space. The enclosure is modelled as insulated walls. Convection currents are setup in the air in contact with the PCB. The PCB and enclosure lose heat through the back surface of the PCB as shown in Fig. 1.

**Table 1.** Dimensions of the model

Part		Length	Breadth	Height
PCB	Copper layer	50 mm	60 mm	0.035 mm
	FR4 layer	50 mm	60 mm	1.43 mm
FET's		9.9 mm	10.375 mm	2.3 mm
Air Domain		60 mm	70 mm	30 mm

The materials used for the model is presented in Table 2.

To simulate the heat generated by the FET, a volumetric heat generation function of magnitude 30 W/chip was applied on the blocks. The chips are in contact with the air domain where natural convection occurs. The PCB is connected to a heat sink at the bottom, which is depicted as a negative boundary heat flux of magnitude  $10e8 \text{ W/m}^2$ .

**Table 2.** Material properties

Part	Materials	Properties	
		Density	Thermal conductivity
FET's	Silicon	2328 kg.m <sup>-3</sup>	148 Wm <sup>-1</sup> K <sup>-1</sup>
PCB	Copper	8950 kg.m <sup>-3</sup>	401 Wm <sup>-1</sup> K <sup>-1</sup>
	FR4	1850 kg.m <sup>-3</sup>	0.294 Wm <sup>-1</sup> K <sup>-1</sup>
Ambient	Air	1.225 kg.m <sup>-3</sup>	0.024 Wm <sup>-1</sup> K <sup>-1</sup>

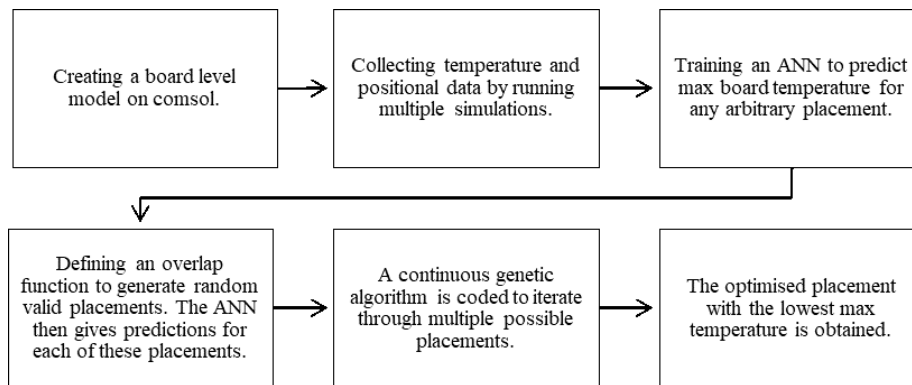
The base and wall temperatures are taken to be 25°C, and the copper laminated layer covers 25% of the surface, which leads to a net thermal conductivity of 100.12 Wm<sup>-1</sup>K<sup>-1</sup> by the copper layer. There is a laminar type of flow within the enclosure.

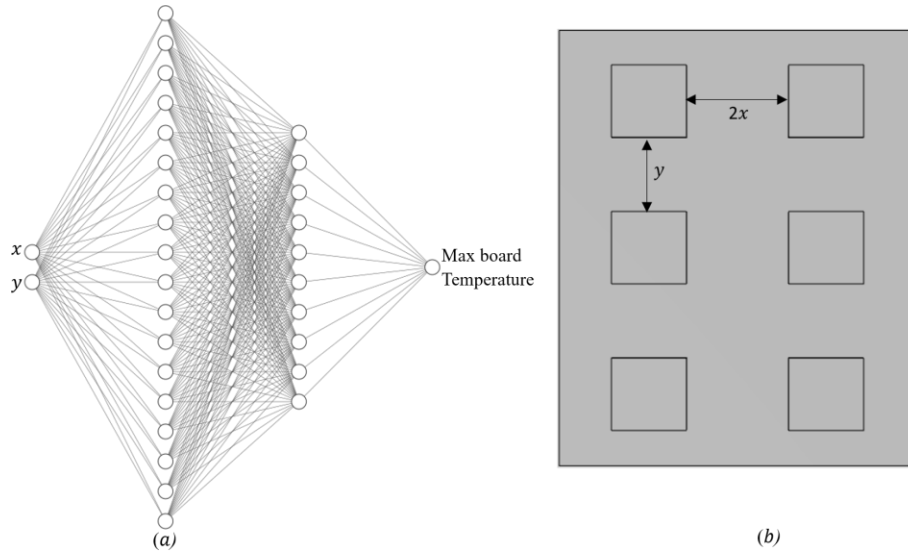
**Table 3.** Table of model parameters

Parameter	Value		
Solver	PARDISO solver with Steady-State formulation		
Turbulence model	Laminar flow with standard wall function		
Properties of air (From COMSOL library)	Density	1.184 kg.m <sup>-3</sup>	Ambient Temp = 25°C
	Viscosity	1.849 e <sup>-5</sup> Kg.m <sup>-1</sup> . s <sup>-1</sup>	
Velocity inlet/outlet	0 m. s <sup>-1</sup> (Enclosed case)		
Pressure outlet	0 Pa (gauge pressure)		
Convergence criteria	Residuals of continuity, e less than 10 <sup>-3</sup>		

### 2.3 Optimization Methodology

After going through multiple papers, a common structure for optimization was discerned,





**Fig. 2.** a) Model Architecture; b) Input Parameters

An ANN [5] was constructed using TensorFlow with the architecture shown in Fig. 2(a). Two hidden layers with RELU activation function are used. The two layers have 18 and 10 neurons respectively. This was then trained with MSE as the cost function and Adam as the optimizer. A train/test split of 0.8/0.2 was used. It was trained for 200 epochs. An  $R^2$  value greater than 0.97 was obtained for both train and test set showing that the model generalizes well and the pattern has been recognised. A continuous genetic algorithm was then coded to find the optimal placement. The algorithm generates a random placement and checks for overlap. If the placement is deemed valid, the co-ordinates are then used as input to the ANN which then gives a temperature prediction. This acts as the fitness value for the chromosome. Fig. 2(b) represents the parameters used for the ANN.

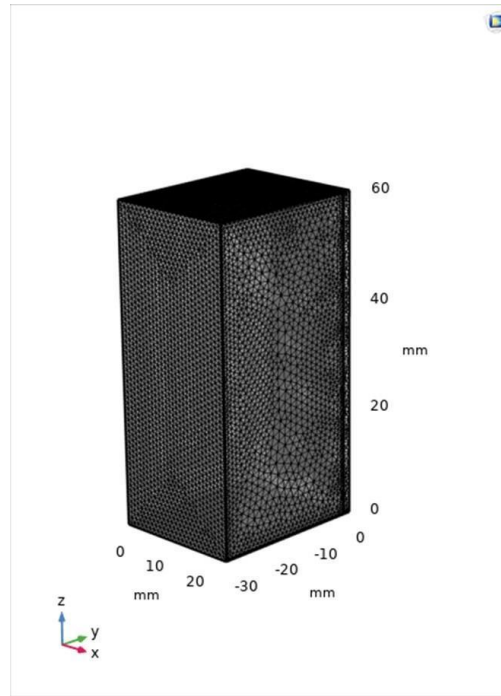
### 3 Mesh Independence Study

As the number of discrete elements used to approximate the continuous solution increases, the accuracy of the CFD analysis of the actual solution also increases. But with the increase in the number of elements the computational cost required to run the simulation also increases. Mesh independence study is carried out to determine the optimal point which gives a compromise between computational time and accuracy. 'Fine' mesh size was chosen for the simulation. A continuous genetic algorithm was then coded to find the optimal placement. The algorithm generates a random placement and checks for overlap. If the placement is deemed valid, the coordinates

are then used as input to the ANN which then gives a temperature prediction. This acts as the fitness value for the chromosome.

**Table 4.** Mesh property values for standard mesh sizes

Mesh sizes	Coarser	Normal	Fine	Extra fine
No. of elements	46395	212649	560560	6155529
Min. Element quality	0.238	0.31	0.33	0.3
Avg. element quality	0.548	0.662	0.678	0.711
Element volume ratio	5.37e-04	3.51e-04	2.12e-04	1.04e-04
Mesh volume (mm <sup>3</sup> )	4725	4725	4725	4725
Convergence parameter (Temperature)	84.19°C	84.15°C	84.14 °C	84.14°C

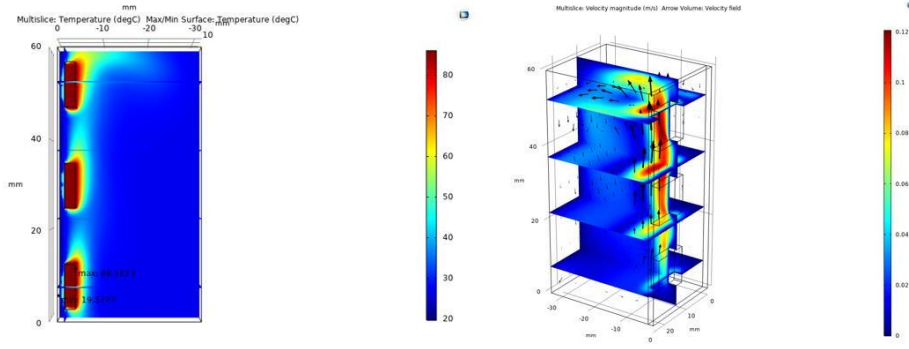


**Fig. 3.** Meshed model of board and air domain.

## 4 Results and discussion

### 4.1 Simulation results

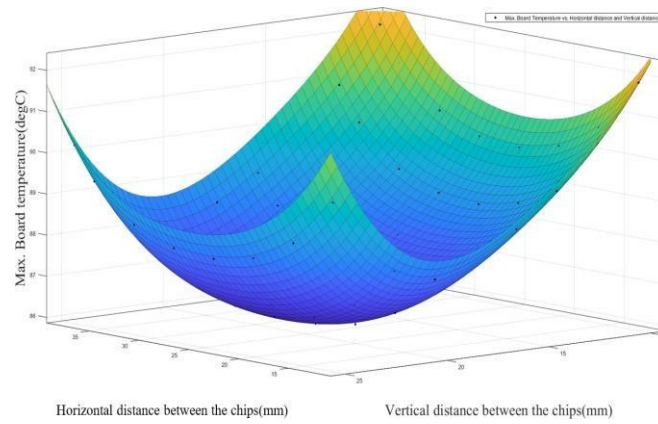
The effect of heat sources and motion of air in the PCB casing is studied through temperature plot as shown in Fig. 4.a and velocity graph as shown in Fig. 4.b. The changes in junction temperatures are studied by varying the positions of the FETs on the board and the values are tabulated and used to train the ANN. A laminar flow air current is setup in the enclosure as shown in Fig. 4.a.



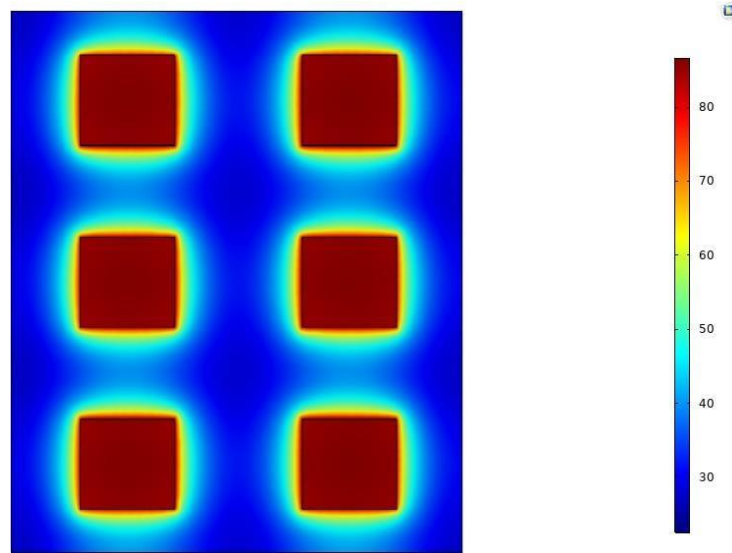
**Fig. 4.** a) Temperature Graph for air inside casing; b) Velocity plot.

### 4.2 Optimization Results

After collecting data by running a parametric sweep, it was observed that symmetric placements had more uniform temperature distribution and lower maximum temperature. This is due to the fact that symmetric placements maximise thermal spread per chip. Hence to obtain the lowest possible board temperature, it suffices to go through only symmetric placements. Two inputs are sufficient to specify a symmetric placement as can be seen in the figure. The optimal placement for our symmetric case was found to be  $x = 12.269$  mm and  $y = 20.086$  mm, with the maximum board temperature being  $86.163^{\circ}\text{C}$ . The answer obtained is intuitive as the maximum temperature obtained can be viewed as a trade-off between the chip's proximity to each other and the chips proximity to the edge of the board. The placement that gives the optimal result is the one that isn't too close the edge but not too close to the center either. This behaviour can be observed in the graph. The validity of the optimization method depends on the degree to which the ANN can reproduce this pattern.



**Fig. 5.** Maximum board temperature for various placements



**Fig. 6.** Temperature distribution for final optimized placement

## 5 Conclusion

We have created a methodology to optimize board level placements based on placement of heat sources which can be extended to solve more complex problems, which include more parameters. The result obtained from minimizing the curve in



Fig. 4 is found to be 86.155. The result obtained from the optimization methodology is 86.163, and hence is in good agreement with the theoretical result.

## Acknowledgement

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