1 Project details

- **Optimization overview-**

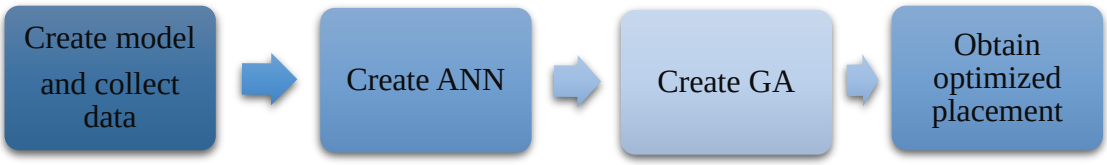

Figure 1:process flowchart

These were the stages followed over the course of the internship. The major steps implemented are explained using flowcharts and pictures in the following pages.

- **Neural network-**

The methodology followed to create the neural network is as follows:

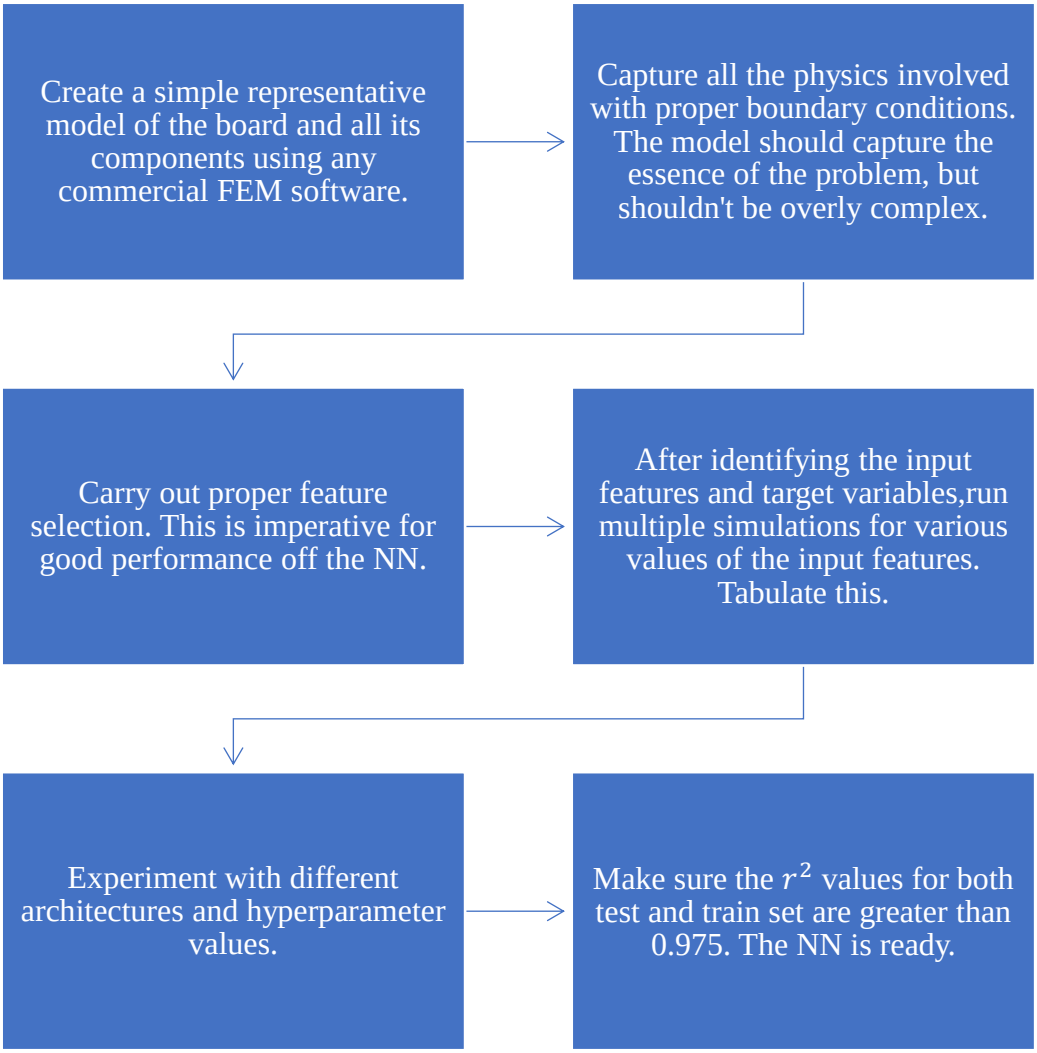

Figure 2:NN process flowchart

The model is first built on COMSOL It consists of 6 FETs approximated as heat generating blocks. Each chip generates 5W. Heat flux through forced convection with air velocity=10m/s occurs on all surfaces. The board is represented as a FR4 block of thickness 1.5 mm. The board is of dimensions 60mm by 50mm. The chips are made of silicon. This time dependant study takes 40 seconds to execute. The temperatures are recorded at t=40 seconds. The following picture is a temperature profile obtained for a random placement at t=40.

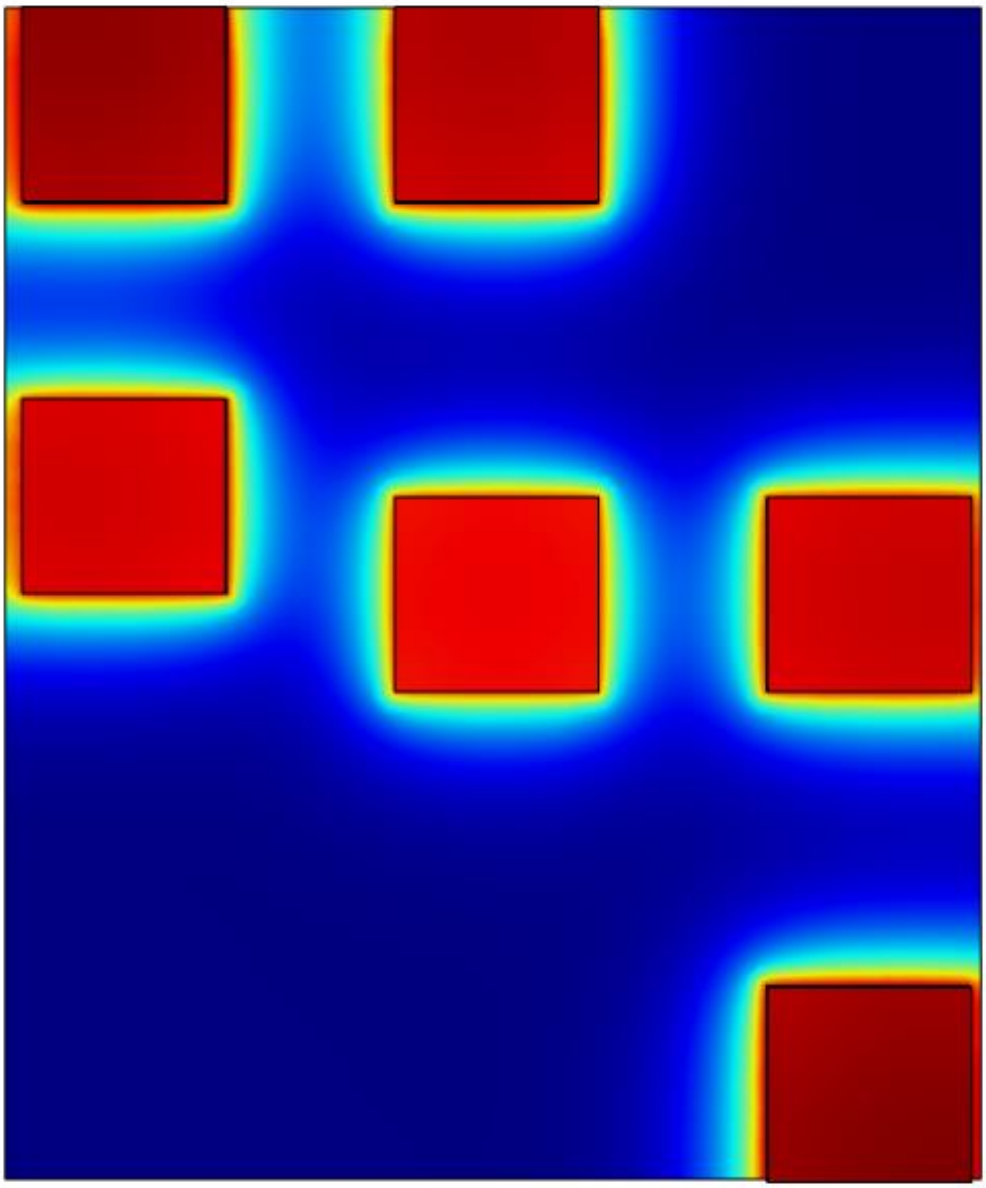

Figure 3:Temperature plot for an arbitrary placement

The input features arrived at after feature selection studies are as follows:

The features were decided after checking for correlation between input and output variables.

All distances are measured from the chips top right corners.

DXY-distance from chip X to chip Y, NEX-Distance from chip X to nearest edge,

D12	**D23**	**D35**	**NE1**	**NE6**
D13	**D24**	**D36**	**NE2**	
D14	**D25**	**D45**	**NE3**	
D15	**D26**	**D46**	**NE4**	
D16	**D34**	**D56**	**NE5**	

There is a total of 21 input features.

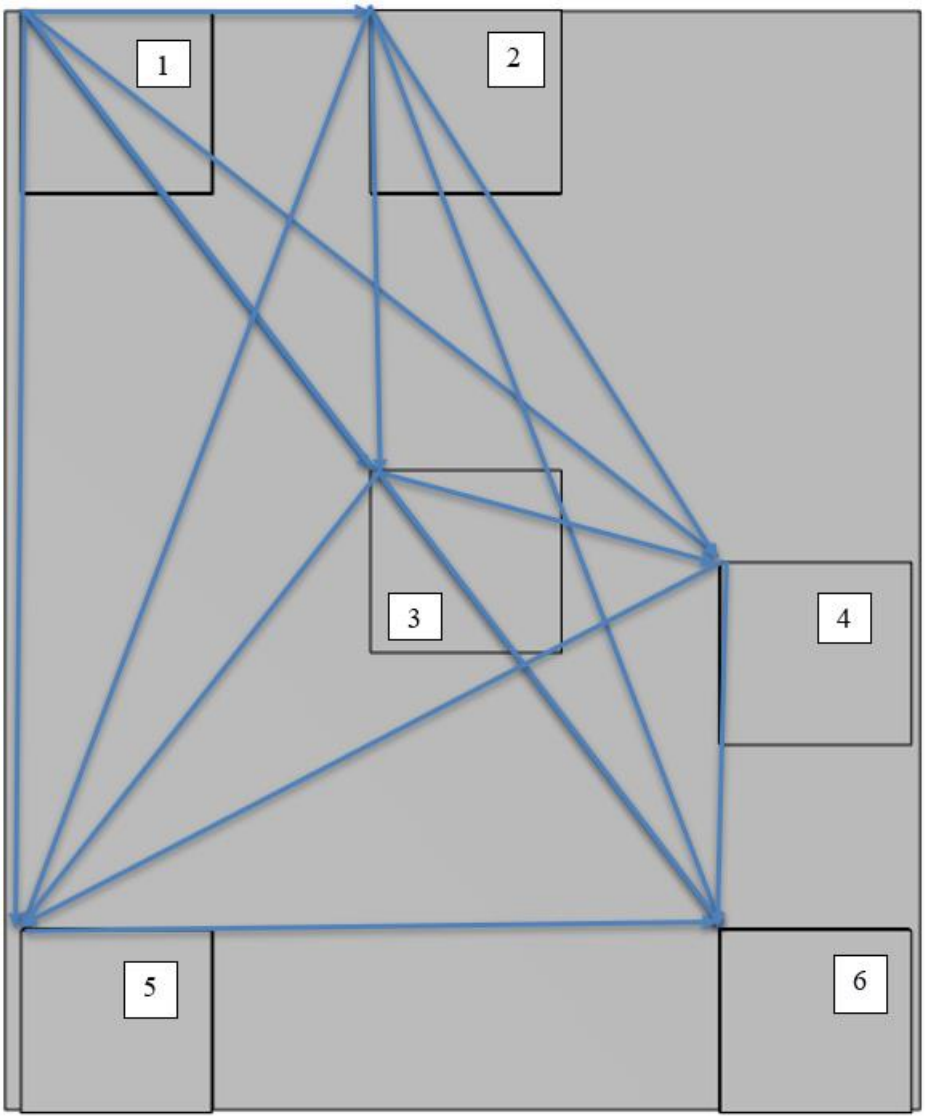

Figure 4:Top right corner to corner distances, DXY

Target variables are-
TX-Maximum temperature of chip X
T1 **T6**
T2
T3
T4
T5
There is a total of 6 outputs.

Simulations were then run for different values of the 21 input features. The 6 outputs were then recorded from the simulation. A database was created with 1024 simulations.
An ANN was then constructed with following architecture using TensorFlow:
The activation function used was RELU and linear. There are 2 hidden layers with 32 and 10 neurons respectively. The neural network after successful training outputs the 6 temperatures, given an input of the 21 features that define a placement.

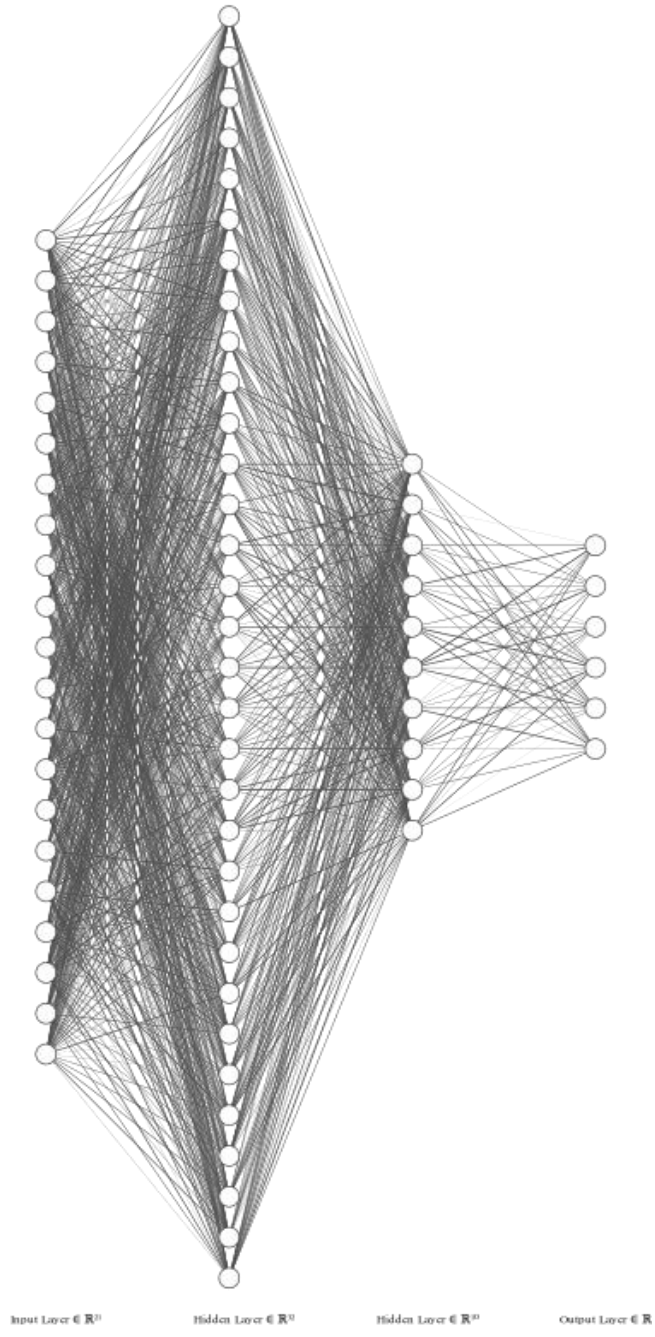

Figure 5:Neural network trained for this example

- **Genetic algorithm**

  Genetic algorithms are a huge collection of algorithms which are inspired by evolution and the natural world. After going through a number of different algorithms, I selected continuous genetic algorithm [1]. It was coded in python and tailormade for the problem at hand.

  The implementation was as follows:

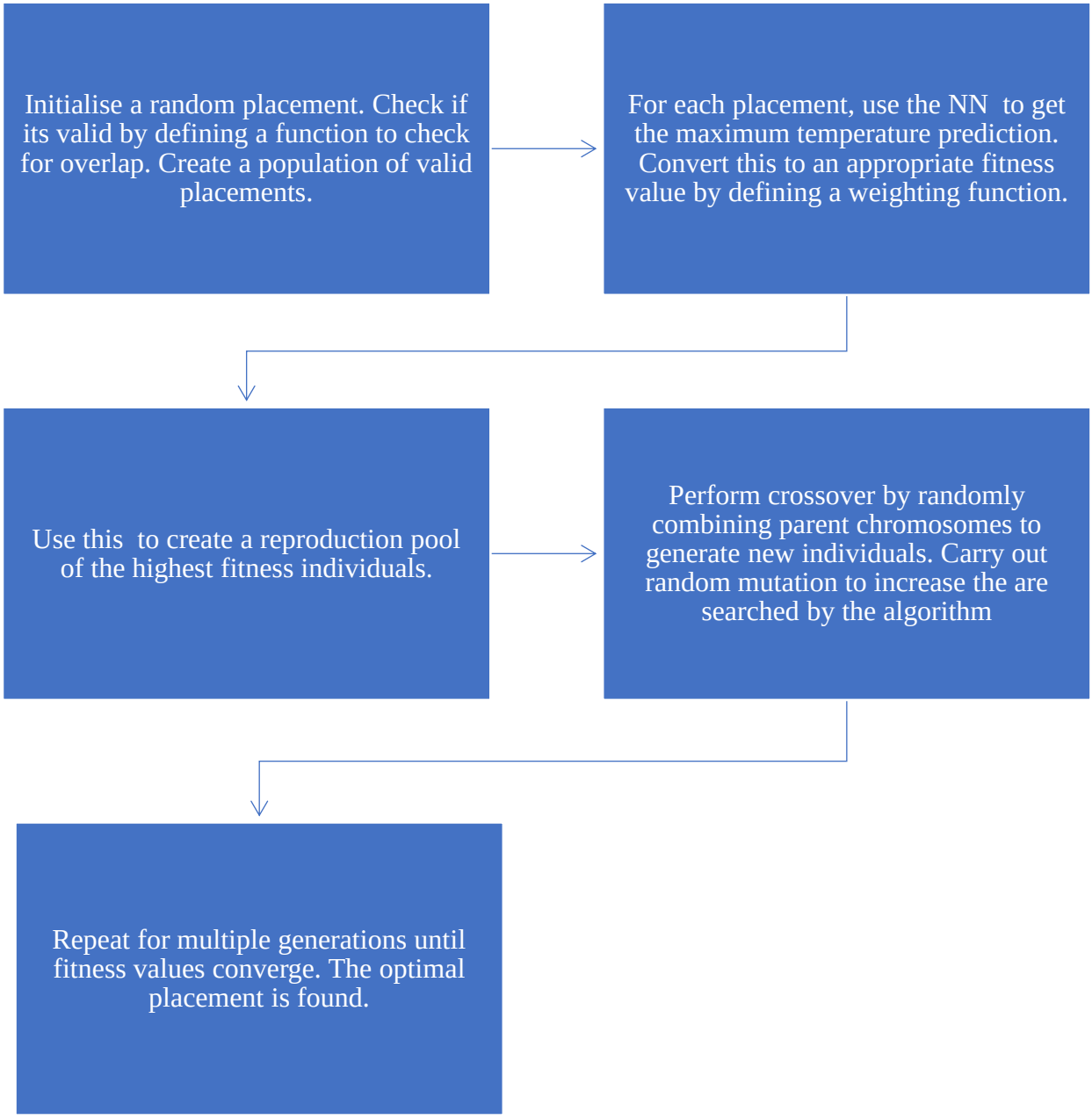

Figure 6:GA process flowchart

The parameters used in the various steps of the genetic algorithm can be found in [2]. They include variables such as population size, no. of generations, mutation rates, crossover distribution etc. These are tweaked based on problem specifics.

2 Results

The optimization workflow created was then implemented on our simple example with 6 FETs. The result obtained is as follows:

This is the placement with the minimum temperature. It had a maximum temperature of 30.12C which is 2C lower than the average. This result also agrees with our intuition and is further proof that the methodology works. This the placement that maximises thermal spread per chip. Thus, by changing the ANN and GA parameters any board level model can be successfully optimised.

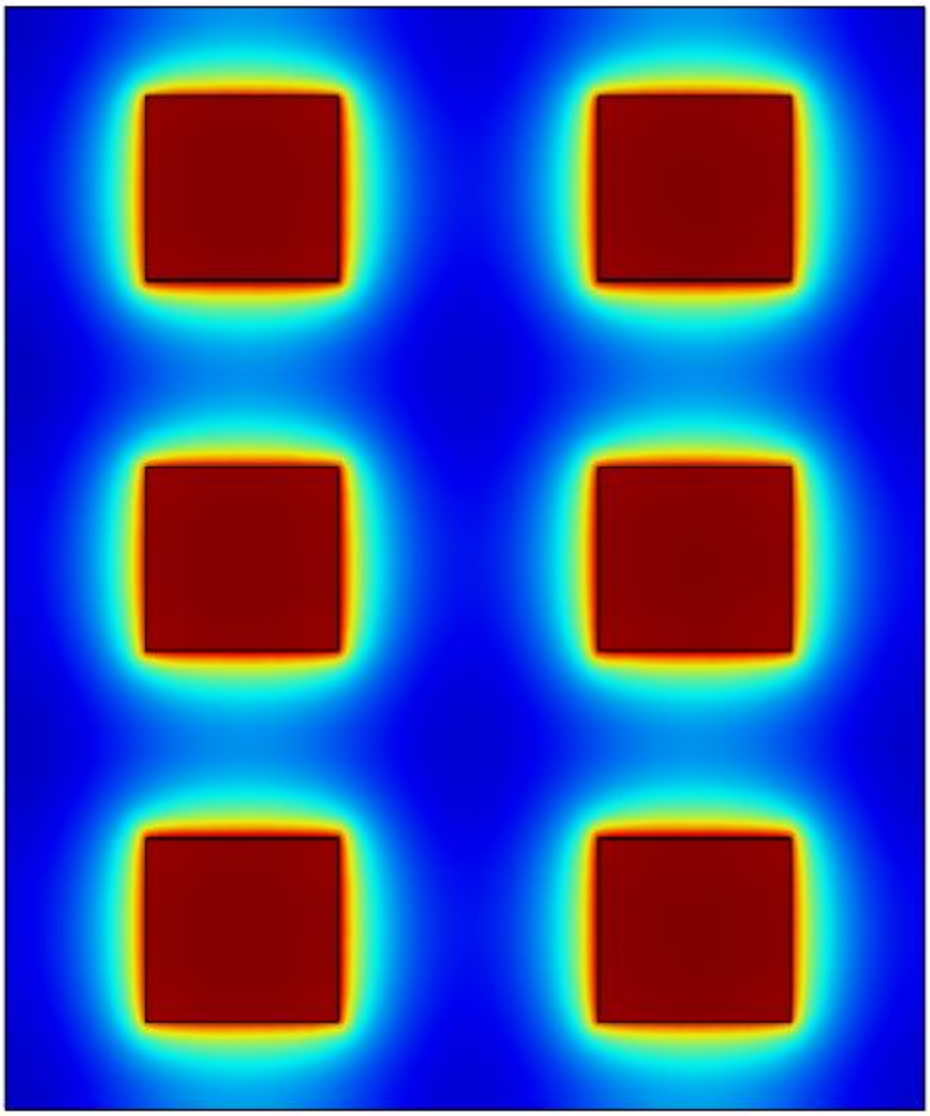

Figure 7:Temperature distribution of optimal placement obtained