COL215: LAB ASSIGNMENT 4
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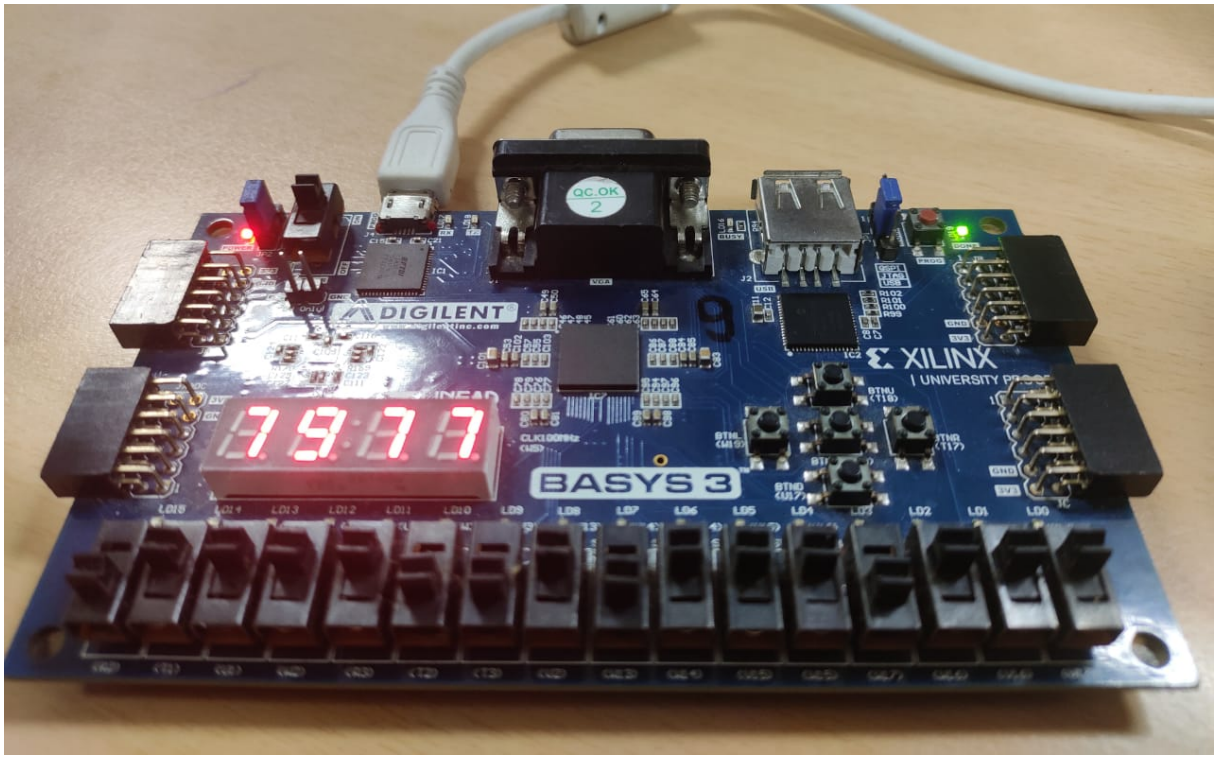
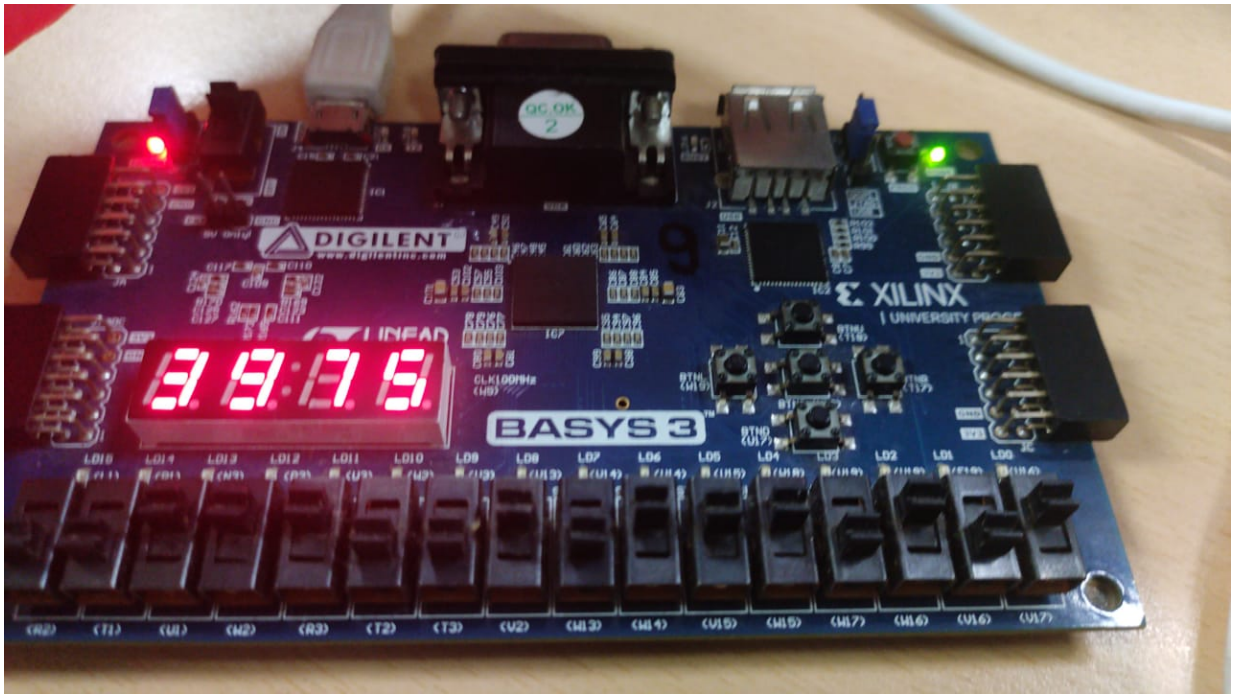
- We have tested our timing circuit (tim_circuit) as well as the Assignment4 file both on simulator and FPGA board.
- All test cases are passing.
- All digits are lighting properly with equal intensity

We have used 15 T-Flipflop to decrease the frequency of the clock from 100MHz to get the desired frequency to around 3 KHz. Followed by another T-Flipflop to make two bit counter. We gave this signal to decoder which decodes and signal A0, A1, A2, A3 accordingly.
We have used four mux, Whenever A0 is true and rest A1,A2,A3 are false, In this case each of our four multiplexer selects 0^{th}, 1^{st}, 2^{nd}, 3^{rd} bit respectively of 0^{th} digit. Which in turn is fed to a decoder which decode this four bit input and give signal corresponding to its decimal value, which is further more processed to display on seven segment display.
NOTE: whenever A0 have signal, in that case rest of anodes i.e. A1, A2, A3 are false. Also A0, A1, A2, A3 are being signaled one by one respectively in a very high frequency which is unperceivable by human eye, which make us feel all four digits are lighting simultaneously.





THANK YOU