

We have implemented six command-

1. add- It is in R-format with opcode="000000" funct="100000" shamt="00000".
Destination address in rd, first and second operand in rs and rt respectively.
 $\text{reg(rd)} = \text{reg(rs)} + \text{reg(rt)}$
2. sub- opcode="000000" funct="100010" in R-format with shamt="00000".
 $\text{reg(rd)} = \text{reg(rs)} - \text{reg(rt)}$
3. sll- Again in R-format. Shamt stores shift amount in binary. Opcode="000000"
funct="000000". rs="00000".
 $\text{reg(rd)} = \text{shift_left} [\text{reg(rt)}] , \text{shamt}$
4. srl- Same as of sll with funct="000010"
 $\text{reg(rd)} = \text{shift_right} [\text{reg(rt)}] , \text{shamt}$
5. lw- I-format with opcode="100011" offset value is stored in address in binary.
 $\text{reg(rt)} = \text{mem}(\text{reg(rs)} + \text{offset})$
6. sw- I-format with opcode="101011" as in lw offset is stored in address in binary.
 $\text{mem}(\text{reg(rs)} + \text{offset}) = \text{reg(rt)}$

We read file at specified location to load the program in the memory which is array (0 to 4095) of std_logic_vector (31 downto 0).

We stop execution when we read "00000000000000000000000000000000".

In order to read file we created a impure function which takes file name in string value as an argument. Open a file and until it is read completely, we read it line by line and each line give std_logic_vector which is stored in memory. We have a internal data structure for register which is array (0 to 31) of std_logic_vector (31 downto 0).