

COL215: LAB ASSIGNMENT 7

Student_1: Pavas Goyal (2018CS10363)

Student_2: Dipen Kumar (2018CS50098)

Description of logic-

1. We have reduced the frequency of the clock from 100MHz to 2MHz by frequency divider (clock generator).
2. We had also made 1KHz clock.
3. We give two output CS and SCK and take one input that is SDO.
4. We were supposed to request data read from PMOD ALS every 1Hz. We know 2000000 cycles of 2MHz frequency results in 1 cycle of 1 Hz frequency. Also we CS is made low while taking input SDO for exactly 15 cycles of 2MHz frequency with SCK equals to clk. This implies CS will be high for next (2000000-15) cycles and again it will be low for 15 cycles and this will continue. In this way we are displaying the brightness of the ambient light in every 1 second.
5. The input SDO received by us while CS was low and SCK was clk is a 15 bit vector. We need to skip first three and last four bit which are leading and trailing zeroes. Apart from this those 8 bit left are input according to ambient light. That is from 3rd bit to 10th bit from most significant to least significant. Also we need only first four most significant bit.
6. This we will process and calculate duty cycle and accordingly it will display brightness. Whenever the value of 't' is less than the value of duty cycle then output='1' else output='0' of LEDs. Value of 't' is changing with a frequency of 1KHz.

Status of Work-

Completed and cross checked. All level of light from 0 to 15 in hexadecimal are being displayed by Basys Board and brightness are being shown by LEDs accordingly.

