

COL215: LAB ASSIGNMENT 4

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Here we were supposed to design a stopwatch. Concept used here are-

1. Reduce 100MHz frequency to 10 Hz frequency for 1/10 of a second. We have done this by using a 10 modulo counter. We used it 7 times to decrease it by the factor of 10^7 .
2. Used another 10 modulo counter to count from 0 to 9 whose clock frequency is 10 Hz. This will show up on Anode_0 of Basys board. This will represent 1/10 of a second.
3. Again another 10 modulo counter with clock frequency of 1 Hz. It will change after every second from 0 to 9. It is basically ones place of the digit which is representing second.
4. For tens place of the number displaying second we used 6 modulo counter. Which changes with 1/6 Hz frequency from 0 to 5.
5. Finally for minutes we further reduced the frequency of tens place of second by 1/10 with the help of 10 modulo counter. Now its frequency is 1/60 Hz. It will count from 0 to 9.

We have used J-K Flipflop for start/continue and pause.

When $J=1$, Q will be 1 and store this value and hence counter will continue to count.

When $K=1$, Q will be 0 and hence counter will be paused. That is because in J-K flipflop will not change the output when $T=0$.

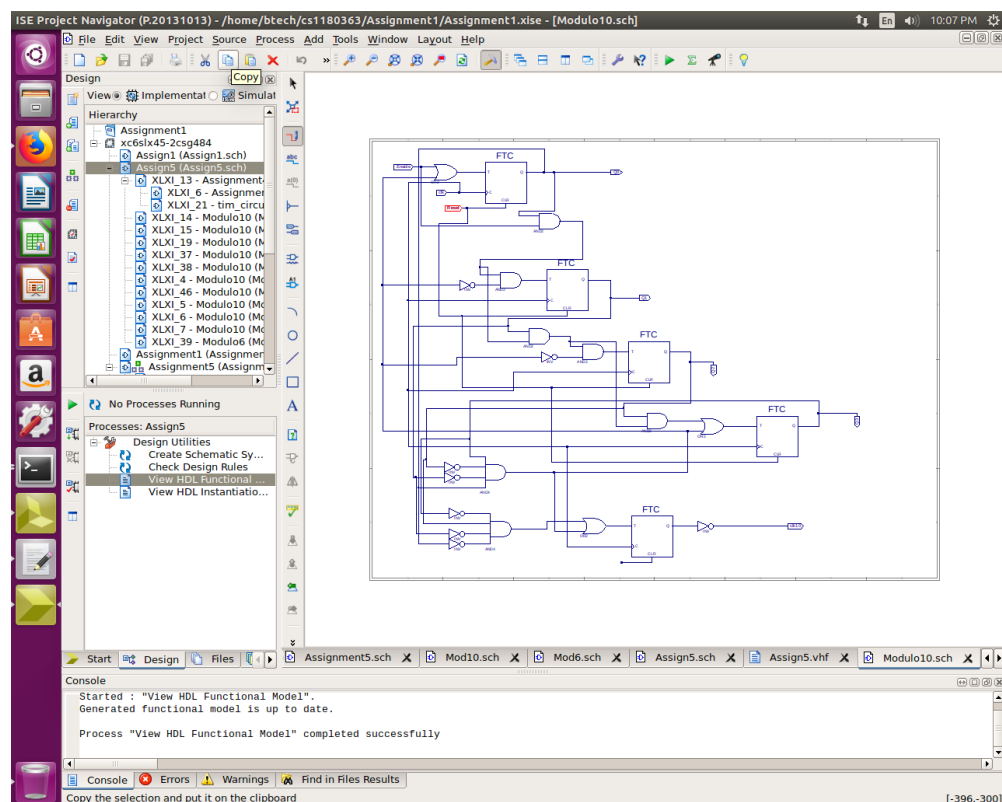
NOTE: Flipflop is edge triggered. Here in this case we have used the frequency of the clock of as high as 100MHz. So In this case even if, when we just press and release the press button for a very short period of time, many rising edges had passed away.

We have used D flipflop as register for shifting purpose because we have used positive edge triggered T-flipflop. Next lower frequency generated by the current frequency was zero at beginning half of 5 cycle and 1 at remaining half of 5 cycle out of total 10 cycle. Due to this our next digit was changing at 5. That is it starts counting from 5 to 9 then 0 then 1 then 2 then 3 then 4 and finally at 5 it changes its next significant digit. To resolve this problem we have used register which shifts our wave form. Now it changes at 0.

Status of Our Assignment:

1. We have implemented a correct logic design with working start/continue, pause and reset push button.
2. Anode_0 is used for 1/10 of a second.
3. Anode_1 and Anode_2 are used for second, it counted from 00 to 59 and again comes back to 00. Anode_2 representing the most significant digit and Anode_1 representing the least.
4. Anode_3 used for min. with frequency of 1/60 Hz.
5. When ever start/continue button is pressed it starts counting/continues counting.
6. Paused is used here to stop counting and remain at its position until continue is pressed which will further continue its counting.
7. Reset button is used to rest the current value to 0000. That is 0 min 00 second and 0 decisecond.

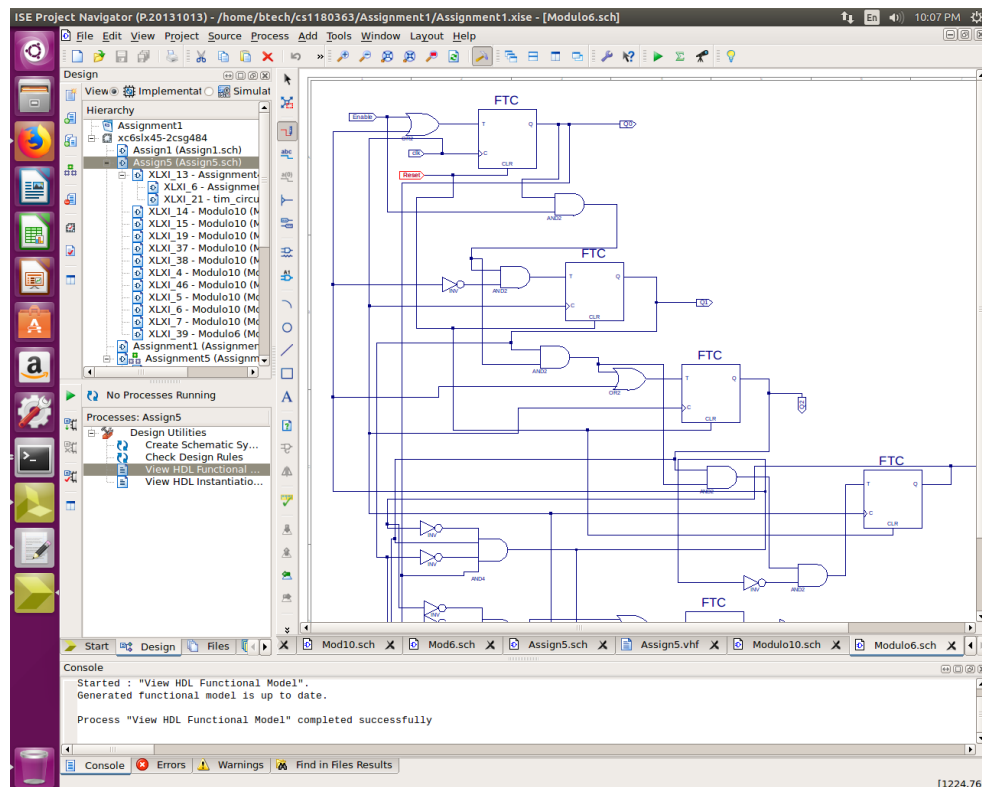
Below are our 10 modulo and 6 modulo counter-



It takes a clock as an input and returns another clock whose frequency is reduced by the factor 10.

It also gives four output Q0, Q1, Q2, Q3 which are used to display the current count of the counter.

Similarly we made 6 modulo counter where we made changes in EoC and starts repeating counting after 5. That is 0,1,2,3,4,5 and then again 0,1,2,3,4,5...



Fully completed with-

1. Assign5.bit
2. Assignment5.xdc
3. Assign5.vhf
4. Assign5.sch
5. Assignment4.vhf
6. Assignment4.sch
7. Assignment3.vhf
8. Assignment3.sch
9. Modulo6.vhf
10. Modulo6.sch
11. Modulo10.vhf
12. Modulo10.sch

THANK YOU...