An On-Chip CMOS Relaxation Oscillator With Voltage Averaging Feedback

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***Abstract*—An on-chip CMOS relaxation oscillator with voltage averaging feedback using a reference proportional to supply voltage is presented. A voltage-averaging feedback (VAF) concept is proposed to overcome conventional relaxation oscillator problems such as sensitivity to comparator delay, aging, and flicker noise of current sources. A test-chip with typical frequency of 14.0 MHz was fabricated in a 0.18 μm standard CMOS process and measured frequency variations of $\pm$0.16% for supply changes from 1.7 to 1.9 V and $\pm$0.19% for temperature changes from $-$40 to 125 °C. The prototype draws 25 μA from a 1.8 V supply, occupies 0.04 mm^2, and achieves 7$\times$ reduction in accumulated jitter (at 1500th cycle) as compared to a oscillator without VAF.**

***Index Terms*—Frequency stability, jitter, MOSFET oscillators, oscillator noise, phase noise, relaxation oscillators.**

I. Introduction

RECENTLY, on-chip reference oscillators are required for low-cost one-chip applications including biomedical sensors, microcomputers, high-speed interfaces such as DDR I/F and HDMI (for initial negotiation), and SoCs. RC-oscillators, including relaxation oscillators, were developed to realize on-chip oscillators with standard CMOS processes.

Table I shows a comparison of conventional oscillators. Crystal oscillators have the best accuracy of ppm order, otherwise RC-oscillators are at least % order more accurate. However, RC-oscillators can allow communication links such as UART if frequency variation is kept within $\pm$1%, which enhances their value as on-chip reference oscillators. Moreover, much faster start-up time is more suitable for intermittent low-power operation than crystal oscillators.

There have been conventional accurate RC-oscillators such as a ring oscillator type with a bandgap reference [2], a relaxation type with BGR [3] and peak holding feedback using hybrid oscillation with relaxation and ring [1], [4]; however, their total frequency variations with voltage and temperature were out of $\pm$1%.

Therefore, to achieve frequency variation within $\pm$1%, we propose a voltage averaging feedback (VAF) concept for accurate oscillators with low power and small area.

TABLE I
COMPARISON OF OSCILLATORS

	Conventional Oscillators			Target
Implementation	Off-chip	On-chip	On-chip	On-chip
Oscillation	Xtal	RC (relaxation)	RC (ring)	RC (relaxation)
Frequency	1kHz - 100MHz (*1)	1kHz - 100KHz	10MHz - 1GHz	14MHz
Freq. variation	1-100ppm	±1%	±5%	<±1%
Current	10μA - 100mA	1μA - 100μA	10μA - 100mA	25μA@14MHz
Size	<5cm^3	0.1mm^2	0.01mm^2	<0.1mm^2
Start-up	1ms - 10ms	10μs - 100μs	1μs - 10μs	1μs - 10μs
Cost	>10 cents (*2)	1 - 3 cents	<1 cent	1 - 3 cents

*1:PLLs are required for high freq.
*2:w/o implementation cost

This paper consists of four sections. Section II illustrates a conventional RC-oscillator, the proposed voltage averaging feedback concept and its characteristics of sensitivity and noise reduction. An efficient method to compensate the temperature dependency of oscillation is also described. Section III shows performance results of the test chip, and Section IV gives the conclusion.

II. Oscillator Architecture

A. Conventional RC-Oscillator

Fig. 1 illustrates a commonly known conventional relaxation oscillator. Oscillation is performed by iteration of charging and discharging the capacitor C as follows:

1) The voltage $V_{\rm osc}$ rises while charging C by I_1.

2) If $V_{\rm osc} > V_{\rm high}$, a comparator sets RS-FF and changes the state of oscillator into discharging phase.

3) $V_{\rm osc}$ falls while discharging C by I_2.

4) If $V_{\rm osc} < V_{\rm low}$, another comparator resets RS-FF and the state returns to charging phase. The issues of this oscillator are as follows:

i) Variation of comparator's delay t_d results in frequency variation with voltage and temperature.

ii) Aging of current sources $(I_1,\ I_2)$ will degrade the accuracy of the slope of $V_{\rm osc}$ and varies frequency.

iii) Flicker noise of current sources $(I_1,\ I_2)$ will degrade low offset-frequency phase noise or accumulated jitter.

B. Voltage Averaging Feedback Concept

A simple solution to obtain a stable and accurate oscillation is to shorten t_d to be neglected, however, this approach needs huge power to comparators so that it does not match with our motivation for low power dissipation. Therefore, we propose a feedback concept called VAF to achieve both accuracy and low power dissipation by maintaining whole oscillation waveform

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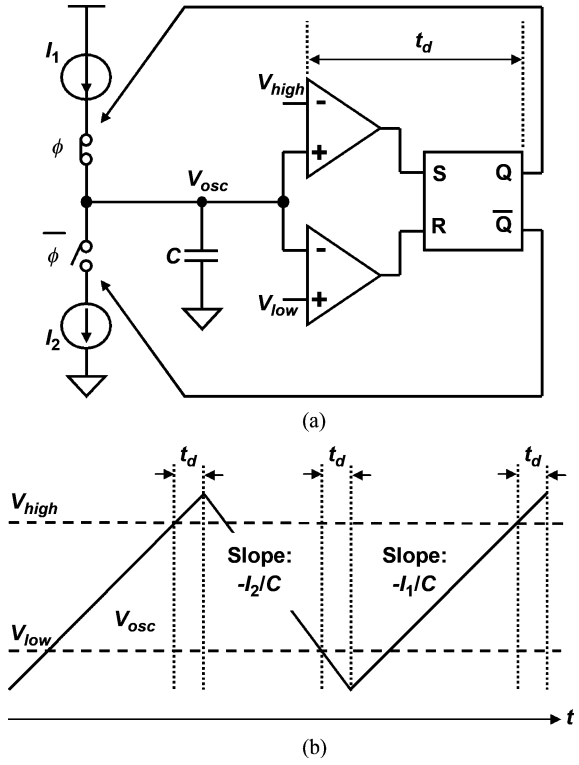

Fig. 1. (a) Conventional RC-oscillator. (b) Waveform.

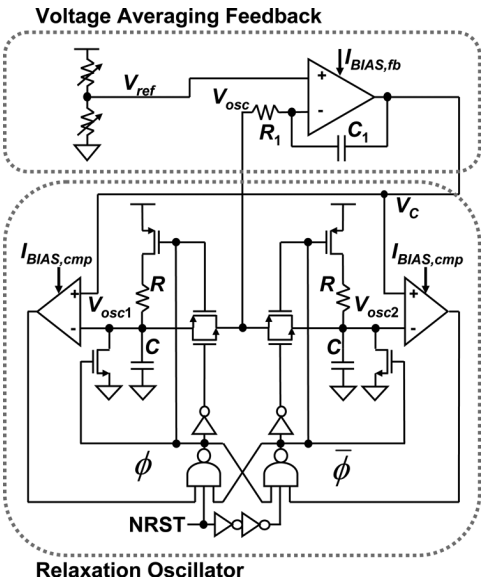

Fig. 2. Proposed VAF concept.

including t_d. Applying VAF to a oscillation with first order lag is our solution for conventional issues; for i) VAF achieves oscillation independent of comparator's delay t_d, for ii) and iii) oscillation without current source means aging free and significant reduction of flicker noise.

1) Oscillation Mechanism: Fig. 2 shows our concept which comprises a complementary relaxation oscillator and an active filter for VAF, where the same complementary design is chosen

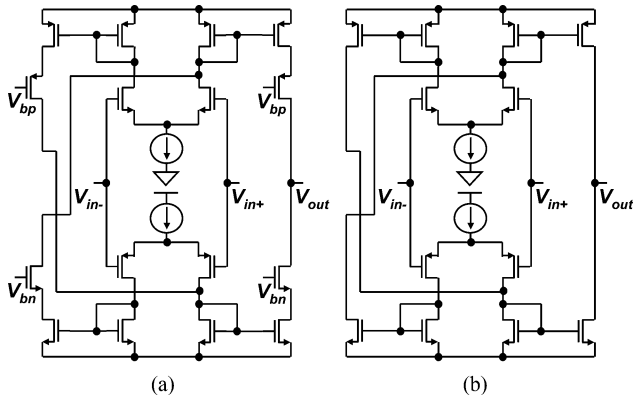

Fig. 3. Circuit schematics of (a) feedback amplifier and (b) comparator.

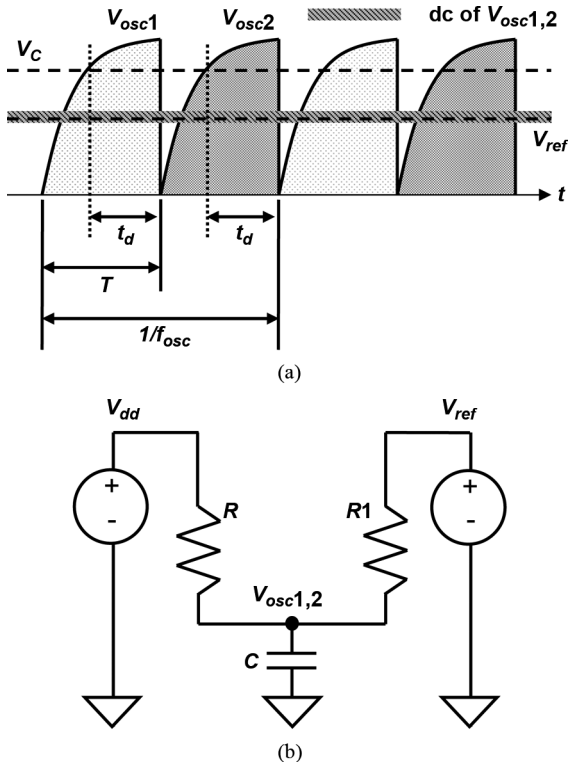

Fig. 4. (a) Waveform and (b) modeling of oscillation.

for comparators and a feedback amplifier for rail-to-rail input and easiness to obtain enough phase margin (see Fig. 3).

The relaxation oscillator part is considered as a voltage-controlled oscillator with a control signal V_c. Oscillation waveforms $V_{\rm osc1}$ and $V_{\rm osc2}$ are summed up to $V_{\rm osc}$ and transferred to the active filter part. At this condition, the active filter maintains DC voltage of whole oscillation at the reference voltage $V_{\rm ref}$ as shown in Fig. 4(a).

$V_{\rm osc}$ and $V_{\rm ref}$ are virtually shorted in a low-frequency domain defined by a time constant of R_1C_1. For simplicity, let us assume the feedback amplifier of the active filter as ideal; the half circuit of the relaxation oscillator part can be simplified as Fig. 4(b). The oscillation waveform under $R_1 \gg R$ is

$$V_{\rm osc1,2}(t) = V_{\rm dd}\left(1 - e^{-1/RCt}\right). \quad (1)$$

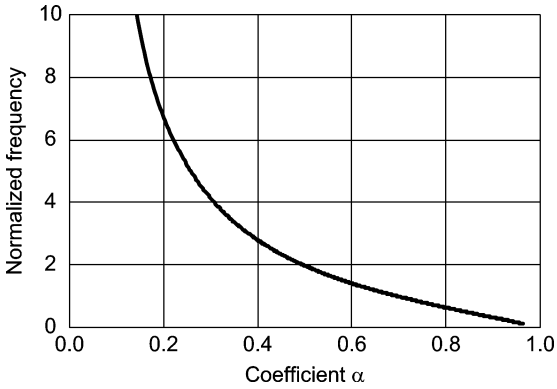

Fig. 5. Normalized frequency characteristic.

As mentioned above, the VAF loop equalizes DC of the oscillation waveform with $V_{\rm ref}$ as

$$\frac{1}{T}\int_0^T V_{\rm osc1,2}(t)dt = V_{\rm ref}. \tag{2}$$

In Fig. 2, $V_{\rm ref}$ is generated by a voltage divider of rail-to-rail voltages. Therefore, we obtain the following simplified equation:

$$\frac{(1-\alpha)\,T}{RC} = 1 - e^{-T/RC}, \tag{3}$$

$$\text{where} \quad \alpha = \frac{V_{\rm ref}}{V_{\rm dd}}. \tag{4}$$

Equation (3) means that the oscillation frequency is just defined by a time constant RC and α. Thus, the normalized frequency (whose basis is $1/(2\pi RC)$) with α is plotted as shown in Fig. 5, which is general for any design using VAF. The variation of t_d has little effect on T because VAF automatically adjusts V_C to keep the equilibrium condition of (2), which results in a stable desired frequency. If t_d is shorter, V_C will become higher to keep the same frequency, while t_d is longer, V_C will become lower in a similar fashion [see Fig. 6(a) and (b)]. This fact enables us to choose low-power design for comparators and results in low power and accurate oscillation.

Equation (3) also means that oscillation frequency does not have any sensitivity to $V_{\rm dd}$ because α is stiffly fixed by the resistive divider. A numerical analysis was performed where T was set to be 25 ns. As shown in Fig. 7, we confirmed that the cross point of $V_{\rm ref}$ and averaged integration of $V_{\rm osc1,2}(=$ DC of $V_{\rm osc1,2})$ is always at 25 ns with different $V_{\rm dd}$.

The oscillation frequency is tunable by applying a digital trimming configuration to the resistive divider, which compensates absolute variations of R and C. With temperature independent capacitance (e.g., metal-oxide-metal capacitance in standard CMOS processes), (3) implies that the sensitivity to temperature is just dominated by R so that it is important to choose a resistive device with low sensitivity.

Peak holding feedback [1] is another solution for oscillation independent of comparator's delay. However, its discrete sampling behavior will cause aliasing issues, therefore, we chose the continuous feedback of VAF.

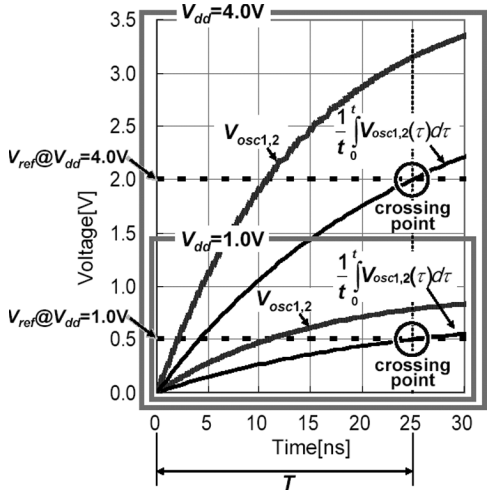

Fig. 6. Waveforms in equilibrium situation where (a) comparator's delay is short and (b) comparator's delay is long.

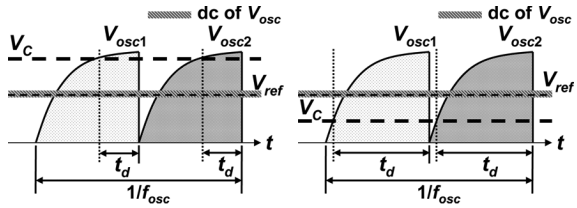

Fig. 7. Numerical analysis of oscillation @ $\alpha = 0.5$.

2) Aging Free Oscillation: Aging degradation of MOS transistors is inevitable and a non-negligible issue for reference oscillators, therefore, oscillators using current source for oscillation have concern in principle about their accuracy at the end of life. However, the proposed design uses passive devices (R and C) for oscillation so that its accuracy lasts to the end of life. Of course, the feedback amplifier suffers from aging degradation. However, because the same aging effect will occur to transistors of the differential pair, the random offset will not change from the time of production to the end of life. The systematic offset may be degraded; however, high enough gain of the feedback amplifier minimizes this issue.

3) Noise Consideration: For conventional oscillators, the main noise sources are current sources and comparators. Although there are oscillators with first order lag oscillation, comparators still remain as a significant noise source. The only way to reduce their noise is to apply huge power (for thermal noise) and large size (for flicker noise) to comparators; however, huge power does not match with low-power applications and large size of gates increases the ratio of gate parasitic capacitors including $C_{\rm ox}$ which is sensitive to voltage and temperature. Of course, large parasitic capacitors of comparators result in more power dissipation of oscillation.

However, the proposed VAF concept releases these issues from comparator design. Thanks to its negative feedback effect, the phase noise spectrum of the oscillator in the low-offset frequency domain is suppressed by the high-pass filter-like transfer function of VAF. Therefore, we can keep the comparators small and low power. The low-offset characteristic of phase noise is

dominated by the feedback amplifier of the active filter, however, its role is to generate V_c and its parasitic capacitor has no effect for oscillation. Therefore, the size of the feedback amplifier can be large enough to reduce flicker noise. This fact implies that the proposed oscillator can achieve both significant long-term stability and low power dissipation. A detailed noise analysis is given in Section II-F.

C. Startup Sequence

The startup sequence is important for multi-vibrator systems. Here, we describe the startup sequence of oscillation as follows;

1) Let us set V_c as a certain voltage (e.g., $V_{\rm ref}$) at the reset state (where NRST is "Low"). $V_{\rm osc1}$ and $V_{\rm osc2}$ are pulled down to "Low" by NMOSs with "High" input from the RS-FF.
2) Let us assume the time difference to start-up two NANDs in the RS-FF by an inverter-delay line and the left-side NAND is firstly released from the reset state and outputs a "Low" signal. Therefore, the capacitance of the left-side half-circuit starts to be charged and to rise $V_{\rm osc1}$. At this time, the left-side transfer gate is shorted and $V_{\rm osc1}$ is transmitted to the LPF as $V_{\rm osc}$.
3) When $V_{\rm osc1}$ exceeds V_c, the left-side comparator pulls down the output itself to "Low" and the output of the left-side NAND rises up to "Hi" again. Then, $V_{\rm osc1}$ is pulled down to "Low", the output of the left-side comparator returns to "High" and the left-side transfer gate is opened to stop transmission of $V_{\rm osc1}$.
4) When the output of the left-side NAND is "High", the right-side NAND changes the output itself to "Low" because of it's inputs are all "High", and $V_{\rm osc2}$ of the right-side half-circuit starts to rise and to be transmitted to the LPF as $V_{\rm osc}$.
5) In the same manner as the left-side half-circuit, when $V_{\rm osc2}$ exceeds V_c, the right-side comparator pulls down the output itself to "Low" and flips the RS-FF, which results in pulling down of $V_{\rm osc2}$ to "Low". The right-side transfer gate is shorted and transmission of $V_{\rm osc2}$ to the LPF is stopped. Then, the output of the right-side comparator returns to "High".
6) "Low" output of the left-side NAND causes $V_{\rm osc1}$ rising again.

The proposed circuit oscillates as a multi-vibrator iterating the above steps from 3 to 6. Settling waveforms of $V_{\rm osc1}$ and $V_{\rm osc2}$ are transmitted alternately to the LPF. Then the DC voltage of the waveform is virtually shorted to $V_{\rm ref}$ by the active filter.

D. Duty-Cycle Variation

The symmetry of a multi-vibrator defines the duty-cycle of the oscillation. However, the proposed oscillator can achieve high enough ($\pm 1\%$) accuracy by the following reasons.

Passive devices for R and C are well matched in commercial standard CMOS processes. For example, mismatch of polysilicon resistors which depends on the size is less than $\pm 0.2\%$ @ 1σ for the case we assigned 200 μm $\times$ 1 μm for $R = 65$ kΩ. On the other hand, mismatch of metal-oxide-metal capacitors is lower than that of polysilicon resistors and less than $\pm 0.1\%$ @ 1σ for tens of fF (where we assigned 500 fF for oscillation).

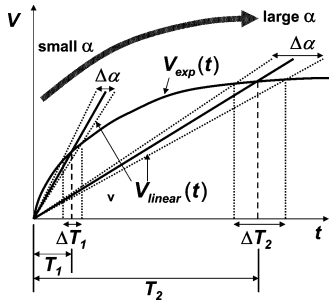

Fig. 8. Sensitivity analysis with the relationship between linear and exponential functions.

Therefore, it can be said that whole passive mismatch should dominated by R with 0.2% @ 1σ variation.

Another principal factor is $V_{\rm th}$ mismatch of differential pairs of comparators. However, it is not a critical issue because a reasonable design will keep $V_{\rm th}$ mismatch small enough and results in duty-cycle degradation by less than $\pm 1\%$ which is negligible for actual applications.

E. Sensitivity to Reference

Equation (3) means the oscillation period T can be a function of α, therefore, it is important to analyze the sensitivity of T to α and figure out the optimal condition.

First, we define the normalized sensitivity of T to α as $(\partial T/T)/\partial\alpha$. By applying derivative to (3), we obtain the sensitivity and α as follows:

$$\frac{\partial T/T}{\partial \alpha} = \frac{1}{\frac{RC}{T}\left(1 - e^{-T/RC}\right) - e^{-T/RC}} \tag{5}$$

$$\alpha = 1 - \frac{RC}{T}\left(1 - e^{-T/RC}\right). \tag{6}$$

Because these equations include super functions of T, it is quite difficult to derive the exact solution as a function of α. But, by approximating exponentials with Taylor expansion, it should be easier to solve and suggest an interesting characteristic of the sensitivity.

Here, we separate (3) into two equations:

$$V_{\rm exp}(t) = 1 - e^{-t/RC} \tag{7}$$

$$V_{\rm linear}(t) = \frac{(1-\alpha)\,t}{RC}. \tag{8}$$

Fig. 8 illustrates the relationship of $V_{\rm exp}(t)$ and $V_{\rm linear}(t)$, where the cross point of the two gives the oscillation period $T \cdot T_1$ and T_2 mean oscillations at a high frequency with small α and a low frequency with large α near 1, respectively. The cross point of (7) and (8) is forced to move by the variation of the coefficient α:$\Delta\alpha$, which results in the variation of T:ΔT. Therefore, we define the sensitivity of the oscillation to reference as $(\Delta T/T)/\Delta\alpha$ and estimate its behavior by approximation with restricted t.

Case 1: We can expand the exponential by second-order Taylor expansion within $t \ll \tau$, where $\tau = RC$ and obtain the

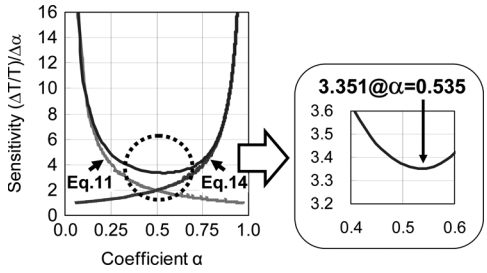

Fig. 9. Sensitivity analysis with coefficient α.

following simultaneous equations by $V_{\rm exp}(T) = V_{\rm linear}(T)$ at α and $V_{\rm exp}(T+\Delta T) = V_{\rm linear}(T+\Delta T)$ at $\alpha+\Delta\alpha$.

$$T = 2RC\alpha \tag{9}$$

$$T+\Delta T = 2RC\left(\alpha+\Delta\alpha\right). \tag{10}$$

Then, the sensitivity is

$$\frac{\Delta T/T}{\Delta\alpha} = \frac{1}{\alpha}. \tag{11}$$

Case 2: We can approximate the exponential as $V_{\rm exp}(t) = 1\ {\rm V}$ where $t \gg \tau$ and obtain the following simultaneous equations in the same fashion as case 1:

$$(1-\alpha)\,T = RC \tag{12}$$

$$RC = (1-(\alpha+\Delta\alpha))\,(T+\Delta T). \tag{13}$$

With neglecting $\Delta\alpha\Delta T$, the sensitivity is achieved as

$$\frac{\Delta T/T}{\Delta\alpha} = \frac{1}{1-\alpha}. \tag{14}$$

Cases 1 and 2 imply that the sensitivity has the minimum value at a certain α under the central limiting theorem of sensitivity which monotonously decreases and increases when $\alpha \cong 0$ and $\alpha \cong 1$, respectively. The most important fact is that the sensitivity to α is independent of RC. In other words, the sensitivity to α is invariant for any frequency.

Numerical analysis helps us to obtain the sensitivity as a function of α. Fig. 9 illustrates the result of numerical analysis and approximations by (11) and (14), where the adequacy of the above approximation, the sensitivity only defined by α, and the theoretical minimum sensitivity of 3.351 at $\alpha = 0.535$ for any RC and $V_{\rm dd}$ are shown.

This sensitivity is easily converted to the sensitivity % per 1 mV. For example, with $V_{\rm dd} = 1.8\,{\rm V}$, the minimum achievable sensitivity of period is converted to 0.19%/mV as follows:

$$\frac{\Delta T/T}{\Delta\alpha} = \frac{\Delta T/T}{\Delta V_{\rm ref}} V_{\rm dd} \tag{15}$$

where $\Delta\alpha = \Delta V_{\rm ref}/V_{\rm dd}$. Then, $(\Delta T/T)/\Delta V_{\rm ref} = (3.351/1.8)\times(100/1000) = 0.19\%/{\rm mV}$.

F. Noise Reduction With VAF

Flicker noise is another important issue for low-power accurate oscillation. One efficient method to reduce noise was an anti-jitter technique based noise reduction method [6] at the cost of additional dc current source. Other reasonable approaches to reduce phase noise of oscillators [7], [8] were based on balancing the impulse sensitivity function [9], but their improvements were limited to at most 3 dB.

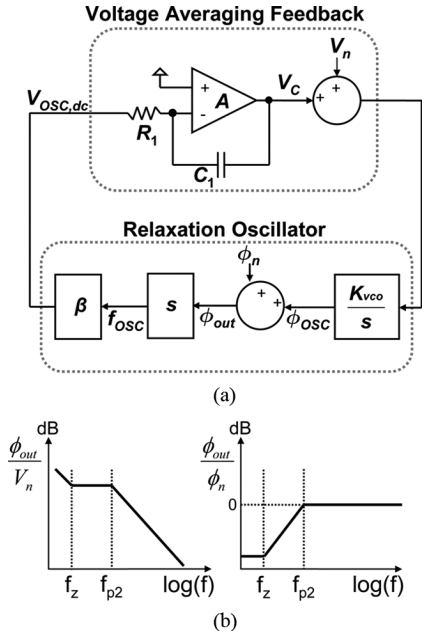

Fig. 10. (a) Noise transfer model and (b) noise transfer gains from two dominant noises to phase noise.

On the other hand, it is a good idea for flicker noise reduction to get rid of current sources from oscillation. Remaining flicker noise mainly comes from comparators, so that enlarging the size of transistors that impact noise is efficient to reduce it. However, the large size of the gate increases the ratio of gate parasitic capacitors including $C_{\rm ox}$ which is sensitive to voltage and temperature; thus, the conventional solution for accurate oscillation was only to increase power with larger C.

The proposed VAF concept overcomes this tradeoff by its closed-loop structure. Fig. 10 illustrates the noise transfer function model. The relaxation oscillator part is modeled as a voltage-controlled oscillator (VCO), where the frequency gain is $K_{\rm vco}$ and the periodic integration of $V_{\rm osc}$: $V_{\rm osc,dc}$ is proportional to the input voltage V_C with a coefficient β. Dominant noises from an active filter and a VCO are transferred to the phase noise by their closed-loop transfer functions respectively and summed up by RMS manner at $\phi_{\rm out}$. The benefit of VAF is that the low offset frequency part of phase noise of the VCO part is suppressed by negative feedback effect. This means that the VAF concept allows us to use small transistors in comparators for accurate oscillation with low power.

Here, we analyze the phase noise transfer function of the proposed RC-oscillator with VAF and consider dominant noise sources as 1) noise generated from the active filter in the VAF loop and 2) phase noise from the VCO part. The total phase noise is a summation of these noises applied the closed loop transfer function, respectively. In Fig. 10(a), the VCO part is described as a series transfer model so that it changes domains of function as "voltage $\rightarrow$ phase $\rightarrow$ frequency $\rightarrow$ averaged voltage".

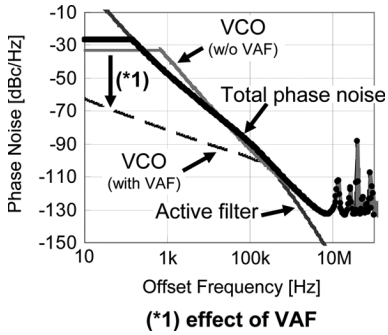

Fig. 11. Phase noise simulation with VAF.

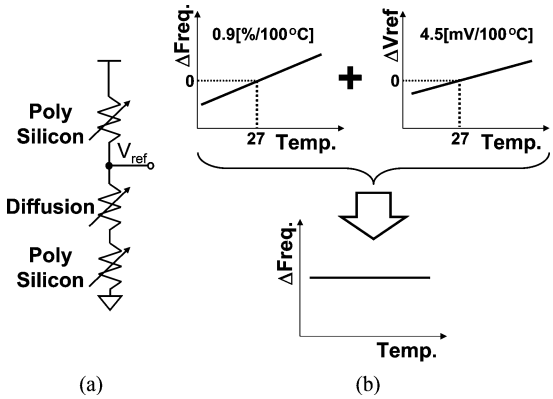

Fig. 12. (a) Resistive divider for $V_{\rm ref}$ generation. (b) Cancellation of temperature dependency.

Thanks to the closed-loop transfer function, two dominant noises of the phase noise are transferred as follows. The output-referred noise of the active filter is transferred and up-converted to the phase noise with a low-pass filter-like transformation as (16). On the other hand, a high-pass filter-like transformation is applied to the phase noise of the VCO part as (17).

$$\phi_{\rm out} = \frac{K_{\rm vco}\left(sC_1R_1A+1\right)}{sA\left(sC_1R_1+\beta K_{\rm vco}\right)}V_n \tag{16}$$

$$\phi_{\rm out} = \frac{sC_1R_1A+1}{A\left(sC_1R_1+\beta K_{\rm vco}\right)}\phi_n. \tag{17}$$

Equation (16) has one zero at f_z and two poles at f_{p1} and f_{p2}, as follows:

$$f_z = \frac{1}{2\pi C_1R_1A} \tag{18}$$

$$f_{p1} = 0 \tag{19}$$

$$f_{p2} = \frac{\beta K_{\rm vco}}{2\pi C_1R_1}. \tag{20}$$

Equation (17) also has zero and pole at f_z and f_{p2}. Therefore, transfer gains of (16) and (17) form shapes shown in Fig. 10(b).

Fig. 11 shows a phase noise prediction with simulations applying (16) and (17) for the test chip in Section III. Thanks to the HPF characteristic of the closed-loop transfer function, the proposed VAF loop will succeed in significant reduction of the phase noise of the VCO part at low offset frequency. It will result in lower phase noise of total performance at the low offset frequency domain.

A Lorentzian-like finite flat level of phase noise spectrum near the carrier frequency is well known [10], [11], [12], which originates from the fact that the total power of oscillation is invariant. Consider Wiener–Khintchine's theorem for each harmonic

$$R_\phi(0) = \int_{-\infty}^{+\infty} L(f)df \tag{21}$$

where $R_\phi(\tau)$ is auto-correlation with $R_\phi(0) = 1$ and $L(f)$ is phase noise spectrum. It is difficult to calculate analytically the flat-level near-carrier frequency. Therefore, we executed a numerical calculation for the first harmonic under the condition of (21), where the higher offset frequency part of the phase noise is approximated by referring Leeson's model [13]. This calculation was applied to a simulation result of periodic steady-state analysis of the VCO part without VAF and derived total phase noise spectrum by (16) and (17). Resulting phase noise spectra are shown in Fig. 11, which means that phase noise at low offset frequency is dominated by the active filter.

G. Temperature Dependency Compensation

Considering on-chip resistive devices of the standard CMOS process, one of them with high resistance is the polysilicon resistor which typically has a negative temperature coefficient. The ratio of it we used is $-0.86\%/100\,^\circ$C.

On the other hand, there should be a resistive material with a positive temperature coefficient: diffusion resistor so that we can cancel the temperature characteristic of the oscillation by blending polysilicon and diffusion resistors. [See Fig. 12(a). Note that the negative temperature dependency of polysilicon resistors is changed to the positive one in frequency of the RC-oscillator.]

Section II-E shows the minimum achievable sensitivity is 3.35 at $\alpha = 0.535$, which is converted to 0.19%/mV at $V_{\rm dd} = 1.8$ V. Variation of oscillation frequency will be proportional to the temperature dependency: $0.86\%/100\,^\circ$C within small fluctuation, therefore, the desired $V_{\rm ref}$ compensation is $0.86/0.19 = 4.53$ mV/100 °C [see Fig. 12(b)].

III. Performance Results

The proposed relaxation oscillator was fabricated in 0.18 μm standard CMOS process with $R = 65$ kΩ, $C = 200$ fF, $R_1 = 1$ MΩ, $C_1 = 1$ pF, and $\alpha = 0.54$. The active area is 0.04 mm^2 (see Fig. 13). The target frequency is 14 MHz and current consumption is typically 25 μA @ 14 MHz, where $V_{\rm dd} = 1.7$ to 1.9 V and temperature $= -40$ to 125 °C. A separable active filter is applied to compare oscillations with and without VAF.

Measured phase noises, period jitters and accumulated jitters are shown in Fig. 14. Fig. 14(a) illustrates that plots of phase noises of both measurement and simulation were almost overlapped so that the prediction in Section II-F achieved a good agreement with measurement. In comparison of phase noise spectra with and without VAF, it is confirmed that VAF reduced the crossover frequency between flicker and thermal noises from

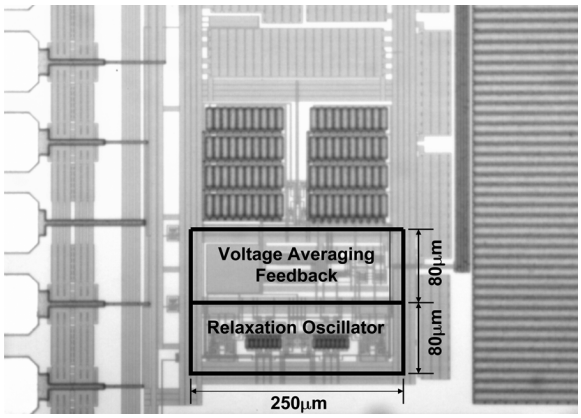

Fig. 13. Die micrograph.

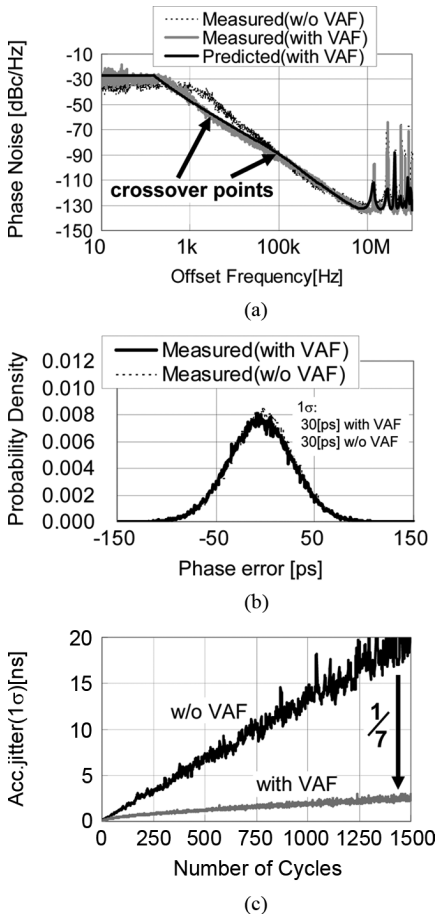

Fig. 14. (a) Measured and simulated phase noises. (b) Measured period jitters. (c) Measured accumulated jitters.

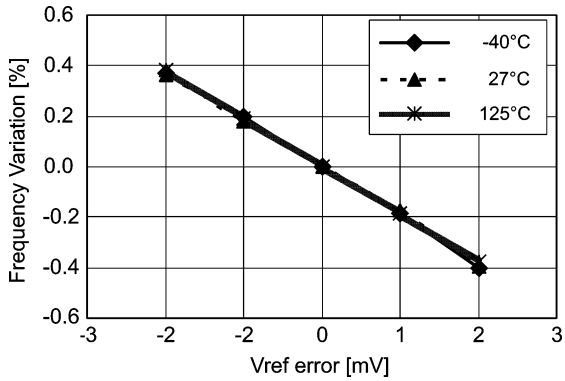

Fig. 15. Measured frequency variation with $V_{\rm ref}$ error at $V_{\rm dd} = 1.8$ V.

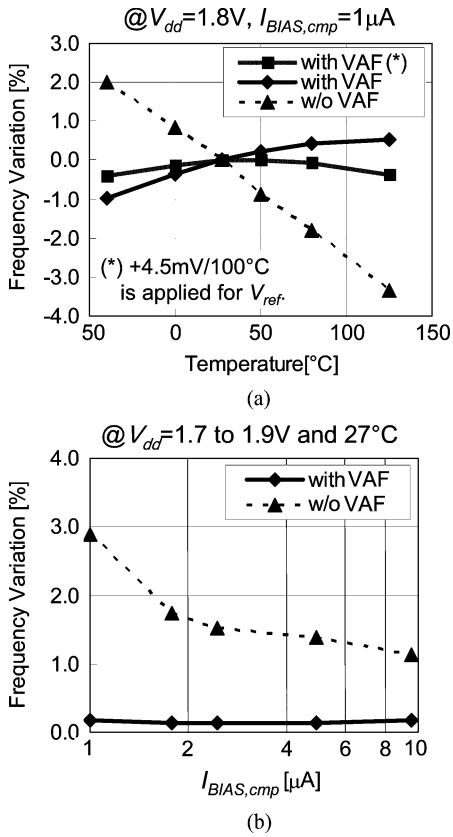

Fig. 16. (a) Measured frequency variation against temperature. (b) Measured frequency variation against voltage and bias.

100 kHz to 4 kHz, which resulted in a significant reduction of the phase noise at low offset-frequency domain.

Fig. 14(b) and (c) illustrate time domain measurement of oscillation accuracy. Almost the same period jitters were measured with and without VAF [$\sigma = 30$ ps in Fig. 14(b)]. However, suppression of phase noise resulted in a significant reduction of accumulated jitter to 1/7 of without VAF at the 1500th cycle [reduction from 20.0 ns to 2.8 ns in Fig. 14(c)]. This reduction of accumulated jitter is nearly equivalent to that of phase noise by 16.9 dB.

Fig. 15 illustrates the frequency sensitivity to $V_{\rm ref}$ with VAF at $V_{\rm dd} = 1.8$ V. The measured -0.19%/mV achieved a good agreement with the theoretical calculation in Section II-G (the sign is opposite due to the different point of view between frequency and period).

Fig. 16 shows measured frequency variations ($\pm$ percent). By the measurement varying temperature at $V_{\rm dd} = 1.8$ V and bias for comparator $I_{\rm BIAS,cmp} = 1$ μA, the oscillation without VAF resulted in a large variation of $\pm 2.67\%$ because of comparators' delay. On the other hand, the oscillation with VAF achieved $\pm 0.75\%$ because temperature characteristic is mainly dominated by R, not comparators. According to the consideration in Section II-G, applying an appropriate temperature

TABLE II
PERFORMANCE COMPARISON

	Sundaresan[2]	Vilas Boas[3]	Lasanen[4]	Choe[7]	Sebastiano[15]	This Work
Type	Ring	Relaxation	Hybrid	Relaxation	Relaxation	Relaxation
Feature	Biasing with BGR	Biasing with BGR	Peak holding feedback	Offset Cancellation	Mobility-based Current	Voltage Averaging Feedback
Process	0.25μmCMOS	0.5μmCMOS	0.35μmCMOS	0.13μmCMOS	65nmCMOS	0.18μmCMOS
Area[mm²]	1.14	0.19	0.09	0.07	0.11	0.04
Frequency [MHz]	7	11.6	5	3.2	0.1	14
Vdd[V]	2.5	3	1	1.5	1.2	1.8
Current Consumption [μA]	600	133	20	25.6	34	25
FoM[dB]	N/A	N/A	N/A	N/A	N/A	-146@100kHz, -146@4kHz
Variation[%] with Vdd	±0.31 @2.4 to 2.75V	±0.8 @3 to 5.5V	±0.95 @1.0 to1.3V	±0.4 @1.4 to1.6V	±0.23 @1.05 to1.35V	±0.16 @1.7 to 1.9V
Variation[%] with Temp.	±0.84 @-40 to 125°C	±2.5 @-40 to 125°C	±0.7 @-20 to 60°C	±0.25 @20 to 60°C	±1.1(*1) @-20 to 80°C	±0.75 ±0.19(*2) @-40 to 125°C

(*1)Considering 3σ spread.
(*2)Temperature compensation for Vref (+4.5mV/100°C) is applied.

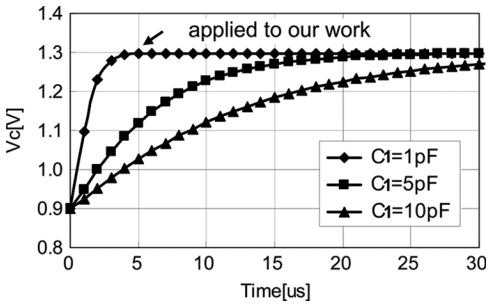

Fig. 17. Simulated V_c settling with $R_1 = 1\ \mathrm{M\Omega}$.

gradient of +4.5 mV/100 °C to V_{ref} generation, by blending diffused and polysilicon resistors with different sensitivities to temperature, reduced frequency variation from ±0.75% to ±0.19% [Fig. 16(a)]. By the measurement varying $I_{\mathrm{BIAS,cmp}}$ at $V_{\mathrm{dd}} = 1.7$ to 1.9 V and 27 °C, it is confirmed that the VAF concept achieved significant reduction of sensitivity to V_{dd} and comparator's delay [Fig. 16(b)].

The dominant pole of the VAF loop is defined by the time constant of the active filter so that the startup time of the oscillator is also dominated by R_1C_1. Fig. 17 illustrates the simulation of startup of V_c which represents a settling behavior of the oscillator from the initial value of $V_{\mathrm{dd}}/2$. From these results, we confirmed that resulting respective startup times with $R_1 = 1\ \mathrm{M\Omega}$ and $C_1 = 1$ pF, 5 pF, 10 pF were about 1 μs, 5 μs, and 10 μs which made good agreements with $\tau = R_1C_1$. We chose $C_1 = 1$ pF so that a sufficient settling time of 10τ is 10 μs for the proposed oscillator.

Finally, the simulated frequency variation (14.0 MHz at $V_{\mathrm{dd}} = 1.8$ V, 27 °C) with process corner variation (SS, SF, FS, FF, and TYP) is shown here as ±0.4%. Of course, this variation is easily fixed by trimming of α even at a mass-production test. Fig. 9 illustrates that a few % variation of α does not cause significant change of sensitivity; therefore, it is not a serious problem at all for mass production.

Table II shows the comparison to recent works of near-process generations or targets; ring oscillator with a BGR [2], relaxation oscillator with a BGR [3], peak holding hybrid oscillator [4], offset cancellation [7], and mobility-based current [15], where [2] and [3] are oscillators with a BGR providing a fixed reference voltage, [4] is a peak holding relaxation oscillator with negative feedback using a VCO, [7] is an offset cancellation technique for comparators that degrade phase noise and enlarge temperature and voltage dependencies, and [15] is another constant biasing technique with a fixed current reference (reverse of [2] and [3]). In comparison with [2]–[4], [7] and [15], we confirmed our work achieved small area and low power with competitive low sensitivity to voltage and temperature.

Figure of merit (FoM) [16] is a well-known measurement for oscillation quality with phase noise due to white noise. Therefore, the aforementioned crossover frequency reduction will be demonstrated by FoM. The time constant of R_1C_1 defined the loop frequency f_c as 159 kHz so that phase noises within f_c are considered as those from the feedback amplifier. FoMs at a offset frequency from the crossover frequency to f_c should be the same due to thermal noise. Consequently, measured FoMs of our work were −146 dB, −148 dB, and −146 dB at 100 kHz, 10 kHz, and 4 kHz offset, respectively. Thus, these results prove that the long-term stability of oscillation is improved by VAF.

Navid derived the minimum achievable phase noise of RC-oscillators [14]. From this definition, the minimum achievable FoM of our work (considering power dissipation of whole core) is derived as −162 dB which is 16 dB better than measurement. Of course, Navid's minimum achievable FoM is somewhat ideal with oversimplification; however, it remains as a future challenge to come close to it with additional and inevitable building blocks such as comparators, bias circuit, reference generator, and so on.

IV. Conclusion

This paper has proposed a new concept of VAF for relaxation oscillators and analytically explained its immunity to variations of voltage and comparator's delay. The minimum achievable sensitivity was generalized to be independent of oscillation frequency. The noise reduction mechanism of VAF was explained. Consequent phase noise reduction was also estimated by a simulation using derived noise transfer functions.

For immunity to temperature, we suggested that blending two resistive materials with opposite temperature dependency into reference generator is reasonable to suppress temperature dependency.

A test chip was fabricated in a 0.18 μm standard CMOS process. Effects of VAF with the above blended resistance technique was confirmed to significantly reduce dependencies of voltage, temperature and comparator's delay. It was also confirmed that VAF succeeded in depleting low offset frequency phase noise (or accumulated jitter). A performance comparison with recent works resulted that our work achieved small area and low power with competitive low sensitivity to voltage and temperature.

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