

Weitao Li
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High-Resolution and High-Speed Integrated CMOS AD Converters for Low- Power Applications

Analog Circuits and Signal Processing

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Springer

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Preface

The future is the Internet of Things (IoT) and it is already here, e.g., in the environmental monitoring, in the manufacturing, and in the building and home automation. By the technology of IoT, there have been millions of mobile devices that are collecting data and exchanging it across the Internet. Typically, that is implemented by three main steps: the data input, the data processing, and the data transfer. Since powerful processors and high-speed network access are available, the data input becomes one of the bottlenecks for the whole system. Not only is the high-resolution and high-rate data input required but also the high power efficiency is expected by the low-power mobile applications.

The data is provided by the analog-to-digital (AD) converter, which bridges the physical world and the computational system. Extreme requirements have been imposed on the AD converter by the rapid growth of the IoT. The low power, the high resolution (not less than 12 bit), and the high speed (not less than 100 MSps) are of crucial importance for contemporary AD converter. To realize that, the CMOS integrated AD conversion is one of the technologies used widely, which has the benefits of both the high performance and the low cost. However, to implement the power-efficient, high-resolution, and high-speed AD converter, some particular design techniques are needed, i.e., the architecture and the circuit optimization, such that the AD converter can meet the requirements provoked by the applications. While many researches have focused on it, the lack of the systematic and comprehensive tutorial results in the inefficiency of the learning and designing.

This book deals with design techniques to realize the integrated AD converter with the unprecedented combination of the power efficiency, the resolution, and the speed in advanced CMOS technology. It consists of eight chapters and is prepared for readers having a solid understanding of the analog IC circuit and data conversion. The contents and orders are organized carefully to provide readers with a step-by-step tutorial. Two aspects, from the system level to the circuit block level,

are both covered. Three types of improved architectures, three circuit blocks, and the calibration for different architectures are all discussed in detail. In addition, a design case is included as an example.

Beijing, China
December 2016

Weitao Li
Fule Li
Zhihua Wang

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Chapter 1

Introduction

1.1 Why ADC?

In the recent five decades, integrated circuit (IC) technologies have developed enormously, promoting the rapid advancement of the digital signal processing. Although meanwhile analog circuits shrink, they have proved irreplaceable, as the only circuits that directly cope with the analog environment humans live in. Thus, ADCs that can bridge the analog circuits and digital ones are fundamentally necessary in systems.

1.1.1 ADC History

As for the evolution of ADC, it has a history of almost 200 years and the roadmap is illustrated in Fig. 1.1. Although its history is long and complex, the development of the ADC is undoubtedly determined by some important factors, including applications, the process technology and the design techniques. The applications is the original driving force, the process technology determines the performance and the design techniques promotes the improvement of the performance.

- **Early History and Vacuum Tube ADC**

According to the textual research, the first data converter dates back to the eighteenth century and was a binary-weighted water metering system, built near Istanbul [1]. That is not electronic, but hydraulic. The early ADCs were driven by the pulse code modulation (PCM) proposed for the telephone. During World War II, the digital computer was invented for military applications in 1946 and the first vacuum successive-approximation-register (SAR) ADC emerged in the same year. As time went on, more interests were created in the digital processing and hence in the commercial ADCs. The first 11-bit 50 kSps vacuum tube commercial ADC was introduced in 1954.

- **Transistor ADC**

Although the first germanium transistor was invented at Bell Labs in 1947, it took one decade for the transistors to be widely used. During the mid-1950s and the

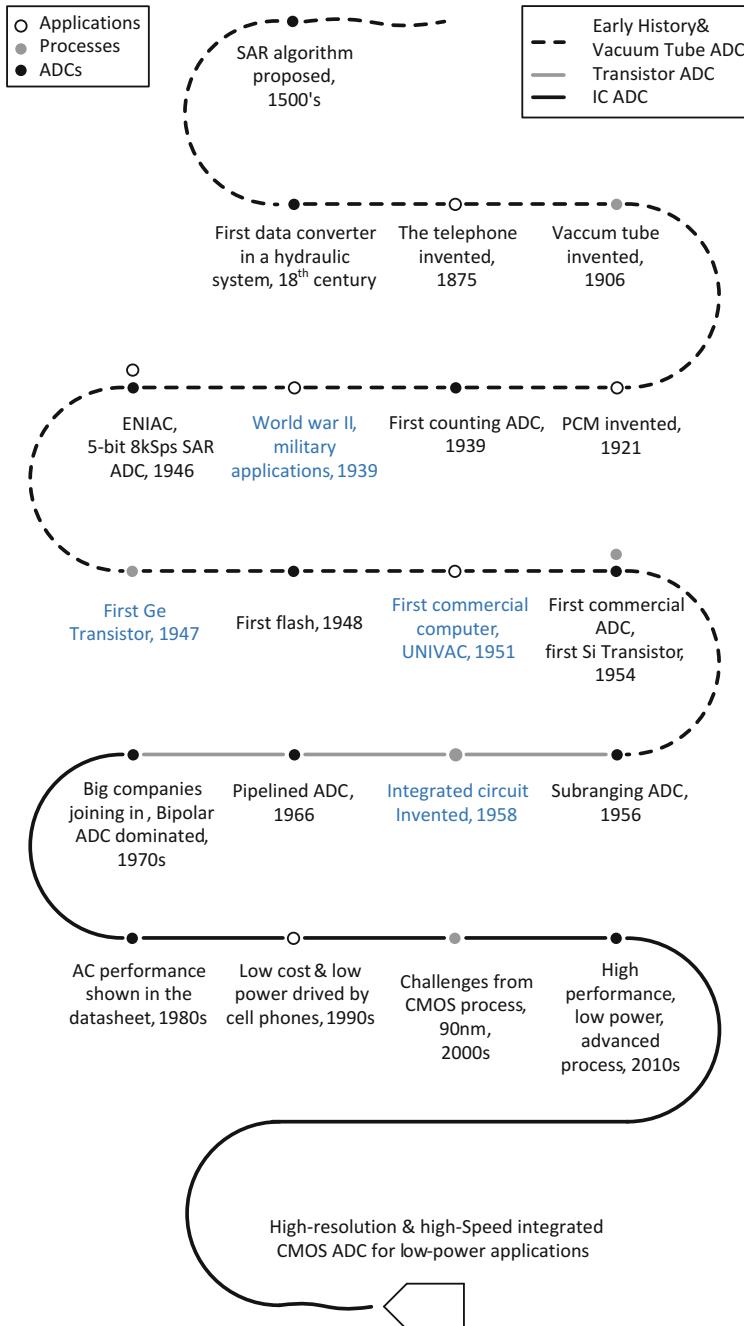


Fig. 1.1 The roadmap of the ADC

early 1960s, the circuit designs migrated from the vacuum tubes to the transistors, thereby enabling new possibilities of the ADC. ADCs based on different architectures were proposed, like the subranging ADC introduced in 1956 and the pipelined ADC introduced in 1966.

• Integrated Circuit ADC

- A number of big companies, like Analog Devices and Analogic Corporation, moved into the ADC field in 1970s and began one of the most exciting decades in the roadmap of ADC. ADCs were widely used in industrial process control, digital video, high-resolution digital voltmeters, military-phased array radar and medical imaging [2].

In this decade, the bipolar ADCs were still dominant for its better performance. Certainly, the designers began to be interested in the advantage of the complementary metal–oxide–semiconductor (CMOS) process. CMOS switches make ideal building blocks for data acquisition systems. Besides, the process provides the possibilities to add CMOS digital circuit to the ADC with low power dissipation and small area.

- Until 1980s, the emphasis in ADCs shifted to the dynamic performance, like the signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and effective number of bits (ENOB). Higher resolution of the ADC was required by the data acquisition, the medical imaging, and so on.
- In 1990s, due to the applications of mobile phones and wireless base stations, communications became the biggest driving force for ADCs again. Not only the high performance but also the low power were required.
- The trend of increased resolution and speed of the ADC continued in 2000s. But that was challenged by the advanced CMOS technology due to the dropped power supply voltage and minimum gate length. During the decade, 14-bit 105 MSps IF-sampling ADC and 12-bit 210 MSps IF-sampling ADC emerged.
- In 2010s, the internet of things (IoT) is widely used in the environmental monitoring, the manufacturing, and the building and home automation. Extreme requirements have been imposed on the ADC by the rapid growth of the IoT. The low power, the high resolution (not less than 14 bit), and the high speed (more than 100 MSps) are of crucial importance for contemporary ADC.

1.1.2 *Modern ADC*

The Highest resolution and speed ADCs (at the time of the publication of this book) are summarized in Table 1.1. In the industry field, the highest resolution is 24 bits provided by AD7767 (18 mW, \$8.60). The fastest sample rate is as high as 5 GSps, provided by LM97600 (3 W, \$250).

Additionally, in the academic field, two 16-bit ADCs [3, 4] have been introduced. But their conversion rates are only 125 MSps (385 mW, 180 nm CMOS) and 500 kSps (6 mW, 130 nm CMOS). Additionally, the conversion rate distributes from 100

Table 1.1 The highest resolution or speed ADCs

	Conversion rate (Sps)	Resolution (bit)	Power (W)	Process/Part#/Price
Industry Field	128 k	24 (Highest)	18 m	AD7767, \$8.60
	5/2.5/1.25 G (Fastest)	8	3	LM97600, \$250
Academic Field*	125 M	16 (Highest)	385 m	180 nm CMOS [3]
	500k	16 (Highest)	6m	130 nm CMOS [4]
	40 G (Fastest)	6	1.5	65 nm CMOS [5]

*Only CMOS Nyquist ADCs

MSps to 10 GSps [5–8]. The fastest ADC converts at 40 GSps, but the resolution is only 6 bit (1.5 W, 65 nm CMOS) [5].

Typically, to achieve the high resolution and sampling rate, the power consumption is large. And hence, this book focuses on low power designs for ADCs with more than 12-bit resolution and conversion rate over 100 MSps.

1.2 Why This Book?

By the technology of IoT, there have been millions of mobile devices that are collecting data and exchanging it across the Internet. Typically, that is implemented by three main steps: data input, data processing, and data transfer. Since powerful processors and high-speed network access are available, data input becomes one of the bottlenecks for the whole system. Not only is the high-resolution and high-rate data input required but also the high power efficiency is expected by the low-power mobile applications.

This book presents in depth the design techniques to realize the integrated AD converter with the unprecedented combination of the power efficiency, the resolution, and the speed in advanced CMOS technology. Two aspects, the system level and the circuit block level, are both discussed in detail. Three types of improved architectures, three circuit blocks, and the calibration for different architectures are all talked about. In addition, one design case is included as the example.

This book

- Provides an in-depth introduction to the newest design techniques for the power-efficient, high-resolution (not less than 12 bit), and high-speed (not less than 100 MSps) AD converter;
- Presents three types of power-efficient architectures of the high-resolution and high-speed AD converter;
- Discusses the relevant circuit blocks (the reference voltage buffer, the amplification, and the comparator) in two aspects, relaxing the requirements and improving the performance;

- Analyzes the calibration for different AD converter architectures;
- Describes a design case, a power-efficient pipelined AD converter.

1.3 General Concepts

Some general concepts are illustrated here as the preparation for the following chapters.

1.3.1 Nyquist ADC

What we discuss in the book are Nyquist ADCs. Based on the relationship between the analog signal bandwidth (f_{in}) and the sampling frequency (f_s), ADCs are classified into two categories, Nyquist ADCs ($f_s \approx 2f_{in}$) and oversampling ADCs ($f_s \gg 2f_{in}$) [9]. Their differences lie in the conversion principle and the implementation.

1.3.2 Resolution

The input/output characteristics of the ADC can be described as

$$V_{ref} \left(\frac{D_{N-1}}{2^1} + \frac{D_{N-2}}{2^2} + \frac{D_{N-3}}{2^3} + \dots + \frac{D_0}{2^N} \right) = V_{in} \quad (1.1)$$

where N is the resolution, V_{in} is the analog input, D_{N-1} , D_{N-2} , D_{N-3} , ..., and D_0 are binary outputs, and V_{ref} is the reference voltage. For a single-ended ADC, V_{ref} defines the full-scale voltage range.

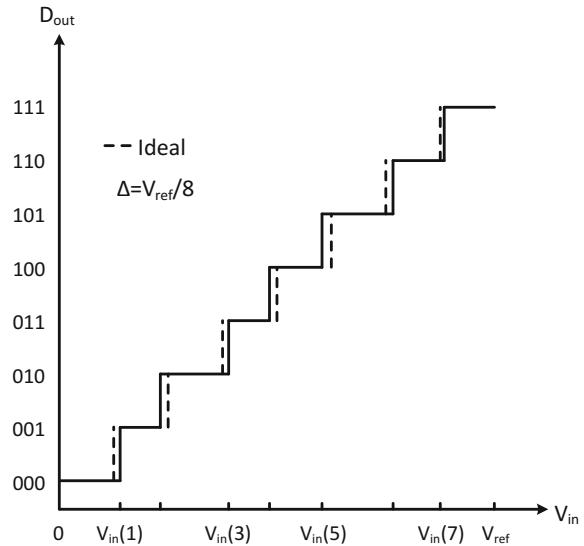
A 3-bit ADC is taken as an example, as is shown in Fig. 1.2. Ideally, the quantization voltage of 100 is $V_{ref}/2$, and 100 is the conversion result of the input between $V_{ref}/2$ and $5V_{ref}/8$.

1.3.3 Quantization Error

As is mentioned above, due to the limited resolution, the quantization error, ϵ , is introduced and its root mean square (RMS) value can be described as

$$P_{noise} = \int_{-\Delta/2}^{\Delta/2} \epsilon^2 = \frac{\Delta^2}{12} \quad (1.2)$$

Fig. 1.2 The input/output characteristics of a 3-bit ADC



where

$$\Delta = V_{ref}/2^N \quad (1.3)$$

The quantization error depends on the resolution and the full-scale voltage range.

1.3.4 Static Specifications

Because of the nonlinearity in the conversion, the input/output characteristics deviates from the ideal one, as is shown in Fig. 1.2. The differential nonlinearity (DNL) and integral nonlinearity (INL) are used to evaluate the nonlinearity of the ADC.

And,

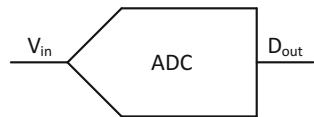
$$DNL(i) = \frac{V_{in}(i) - V_{in}(i-1)}{\Delta} \quad (1.4)$$

$$INL(i) = \sum_{k=1}^k DNL(k) \quad (1.5)$$

1.3.5 Dynamic Specifications

For a N-bit ADC, considering the input of $\frac{V_{ref}}{2} \sin \omega t$, the signal power satisfies

Fig. 1.3 The symbol of the ADC



$$P_{signal} = V_{ref}^2 / 8 \quad (1.6)$$

If the quantization error contributes all the conversion errors, the SNR can be defined as

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{V_{ref}^2 / 8}{\Delta^2 / 12} \quad (1.7)$$

Therefore,

$$10 \log_{10} SNR = 6.02N + 1.76 \quad (1.8)$$

If the resolution increases by 1 bit, the SNR increases by 6 dB.

The nonlinearity introduces the distortion in the output spectrum of the ADC, and the total harmonic distortion (THD) is the ratio of the fundamental to the total harmonic distortion. For the fully differential ADC, the third harmonic is normally the largest distortion. And the ratio of the fundamental to the largest harmonic (or noise) is the SFDR.

The SNR, THD, and SFDR are usually adopted to measure the performance of the ADC in the frequency domain.

1.3.6 Symbol

The symbol of the ADC is shown in Fig. 1.3.

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Chapter 2

ADC Architecture

2.1 Introduction

While lots of Nyquist-rate ADCs are proposed to resolve resolutions at different speeds throughout the years, there are three types of architectures most widely used and they are the pipelined ADC, the SAR ADC, and the flash ADC. Furthermore, the three ones all have the potential to achieve the high performance and the high-power efficiency, via the adjustment in the architecture level or with the aid of useful techniques.

2.1.1 Traditional Architectures

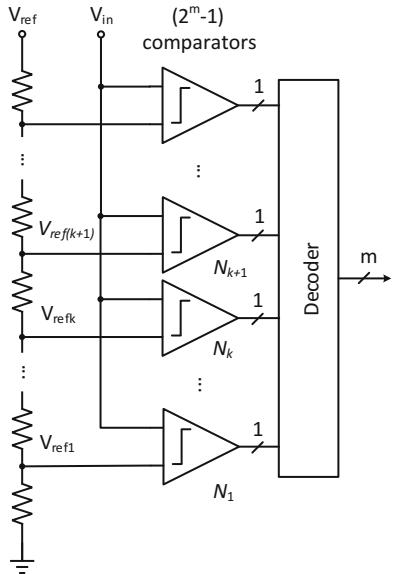
The three architectures all date back to 1900s. To authors' best knowledge, the first flash ADC was built in 1963 at Columbia University [1], and it has the property of the high speed. In 1971, the pipelined ADC was first proposed by Texas Instrument in a patent [2], the all-MOS one appears later in [3], and since then becomes flourish. Its advantage lies in the competitive tradeoff between the speed and the resolution. As to the SAR ADC, while the earliest SAR topology can be found in a 1947 paper by Bell Laboratories [4], the all-MOS SAR ADC was reported in the 1970s [5] and lays dormant until the 2000s, benefiting from the all digital implementation.

2.1.1.1 Flash ADC

A m -bit flash ADC is depicted in Fig. 2.1, consisting of $2^m - 1$ comparators, a resistor ladder and a decoder. The resistor ladder is composed of 2^m equal segments and generates $2^m - 1$ reference voltages, which compare with the analog input at the same time. Thanks to the parallelism, the architecture achieves a high-conversion rate.

Here is an example. If the input is between V_{refk} and $V_{ref(k+1)}$, the comparator N_1 , N_2, \dots , and N_k output 1, and the remaining ones output 0. The $(2^m - 1)$ -bit thermometer code is converted to the m -bit binary code via the decoder.

Fig. 2.1 Basic flash ADC architecture



2.1.1.2 Pipelined ADC

A pipelined ADC consists of cascade low-resolution stages, which are similar or identical, the synchronous block, and the correction block, as shown in Fig. 2.2. Every stage accomplishes the operation in two phases, the sampling phase and the amplification phase. When one stage amplifies the residue via the multiplying digital-to-analog converter (MDAC), the following stage samples its input and converts that to the digital code, which is described in Fig. 2.3a. The digital code is sent to the correction block through the synchronous block to obtain the final output, and the residue attaches to the following stage as its input.

Figure 2.3a illustrates the implementation of cascade 1-bit stages. A single stage consists of a sub-ADC and a MDAC. Here, 1-bit sub-ADC is implemented by one comparator. The MDAC is composed of the capacitive digital-to-analog converter (DAC) and the opamp, and the S/H block shown in Fig. 2.2 is merged in the capacitive DAC (CDAC), where $C_1 = C_2$. As shown in Fig. 2.3a, the first stage amplifies the difference between the input and the DAC's output and V_{res} is

$$V_{res} = \begin{cases} 2V_{in} - V_{ref} & V_{in} > 0 \\ 2V_{in} + V_{ref} & V_{in} < 0 \end{cases} \quad (2.1)$$

which is plotted in Fig. 2.3b. Meanwhile, V_{res} is sampled by the second stage as its input.

The amplification provided by the MDAC enables the pipelined ADC to achieve the high accuracy. The residue of the coarse conversion is so small that it is difficult to

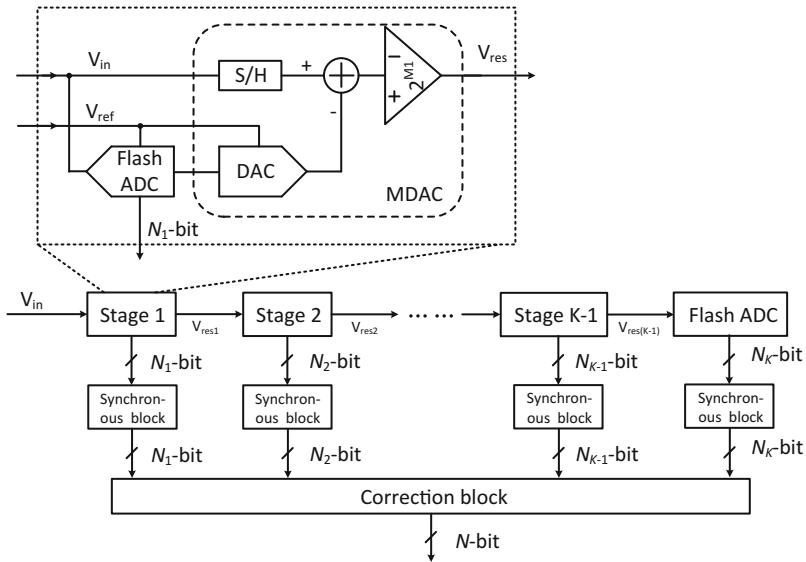


Fig. 2.2 Basic pipelined ADC architecture

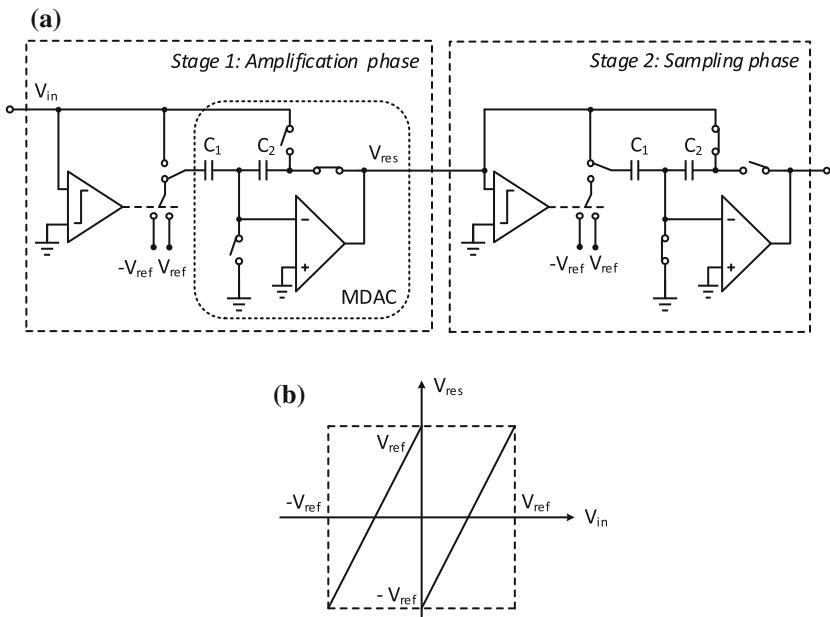


Fig. 2.3 Cascade stages: **a** the first stage operating in the amplification phase and the second one operating in the sampling phase, and **b** the input/output characteristics

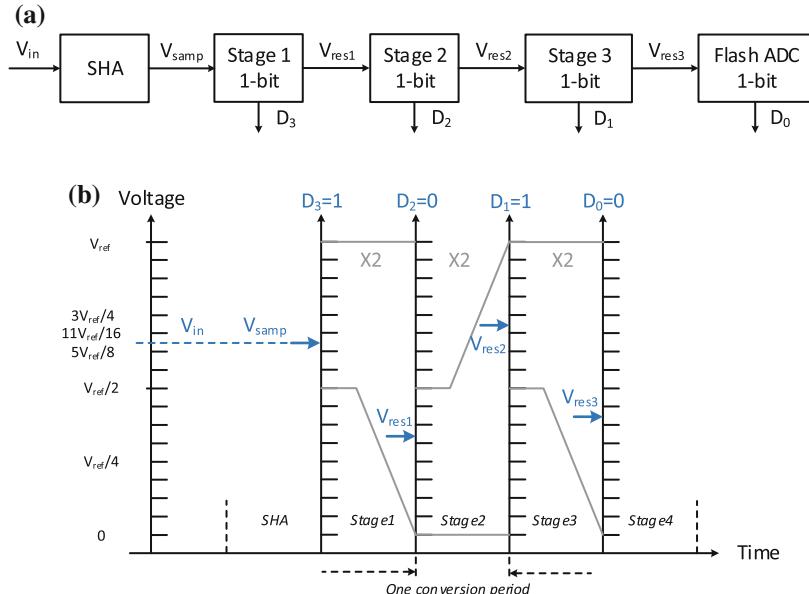


Fig. 2.4 **a** A 4-bit pipelined ADC and **b** its operation versus time

convert it precisely. Thanks to the amplification, the original residue is enlarged and the equivalent error from the following stages is compressed. Take a 4-bit pipelined ADC as an example. The ADC consists of a sample-and-hold amplifier (SHA), followed by three 1-bit stages and a 1-bit flash ADC, as shown in Fig. 2.4a. Besides, its operation versus the time is depicted in Fig. 2.4b, which can be described as follows.

1. The analog input is sampled and held by the SHA as V_{samp} .
2. The first stage compares V_{samp} with the comparator threshold, 0 Volts, outputs the code, 1, and then amplifies the original residue by 2.
3. The similar operation is accomplished by the following stages and the digital codes are 0, 1, 0, respectively.

It is noted that the amplification is absent in the last stage, because its residue does not contribute the information anymore. Due to five conversion periods spent to obtain a 4-bit code, the delay is introduced between the input and its code. Fortunately, the interval between two codes is still one period. In summary, in the pipelined ADC, every stage scales the original residue up by 2^{N_i} (N_i is the effective resolution of the i th stage shown in Fig. 2.2) to the full scale, and then the enlarged residue is converted to improve the accuracy.

2.1.1.3 SAR ADC

The interest in the SAR ADC increases for it is as digital as it can get. It derives the beauty from three properties: the ability to achieve high resolutions, the absence of opamps, and the ability to consume no static power dissipation [6].

In the view of the sampling and quantification, a SAR ADC is conceptually shown in Fig. 2.5. It is composed of a DAC, a comparator, and some logic, which are in a feedback loop. The CDAC is commonly adopted, because it can accomplish the sampling besides the digital-to-analog conversion.

For a N -bit ADC with 1 bit per cycle in Fig. 2.5, the conversion time is approximately $N(T_{COMP} + T_{DAC} + T_{logic})$, where T_{COMP} , T_{DAC} , and T_{logic} are the response time of the comparator, the DAC, and the SAR logic.

An example is taken to illustrate the operation in one period, as shown in Fig. 2.6. Once the input voltage is frozen to V_{samp} , the feedback loop begins to search its quantified value, which can be described as follows.

1. The analog input is sampled and held as V_{samp} .
2. The feedback loop sets V_{DAC} to $V_{REF}/2$ in the first cycle. Comparing V_{DAC} with the input, the first bit, 1, is generated.
3. Based on the first bit, the feedback loop sets V_{DAC} to $3V_{REF}/4$ in the second cycle. Comparing V_{DAC} with the input, the second bit, 0, is generated.
4. The similar operation is accomplished in the third and fourth conversion cycles.

After four conversion cycles, the digital output is 1010. Compared with the operation of the pipelined ADC in Fig. 2.4, in the SAR ADC, the amplification of the residue is removed and the comparator's threshold voltages change with more and more resolutions resolved.

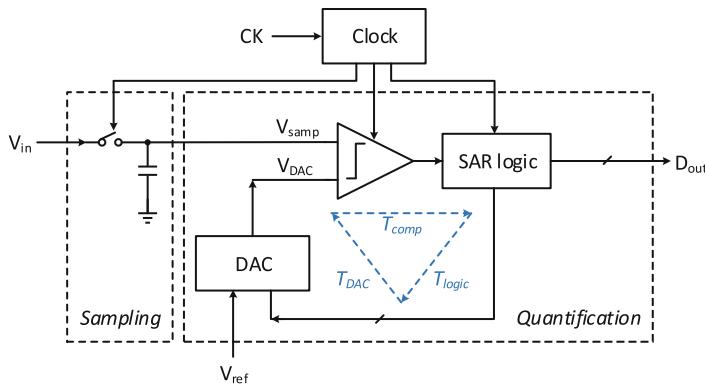


Fig. 2.5 Basic SAR architecture

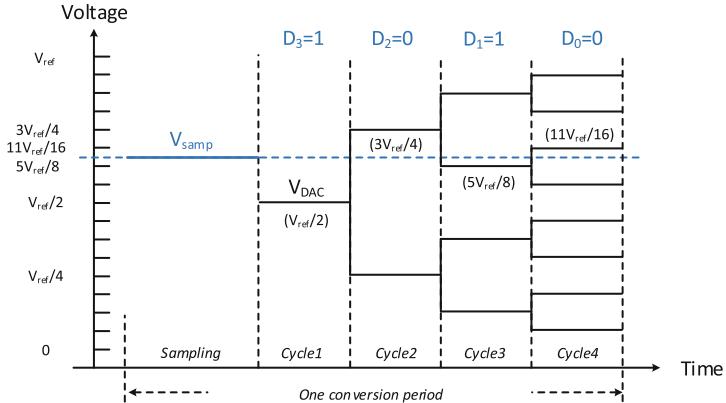


Fig. 2.6 SAR operation versus time

2.1.2 Limitations

There are limitations for the traditional architectures, the flash ADC, the pipelined ADC and the SAR ADC, to realize the high performance and the high-power efficiency.

For the flash architecture, while the parallelism helps the converter to achieve a high speed, it makes the architecture suffer from the problem of area. To obtain m -bit code, $(2^m - 1)$ comparators are needed and hence the area is enlarged at an exponential rate with the resolution. The flash architecture is commonly adopted by the ADC with the resolution of no more than 6 bits.

For the pipelined architecture, the inaccuracy is resulted in by the capacitor mismatch, the finite opamp gain, the opamp nonlinearity, the comparator offset, KT/C noise, and the opamp noise. Besides, the conversion rate is limited by the sum of the sampling time and the amplification time. The sampling time is a number of constant time of the sampling network, and the amplification time is determined by the bandwidth of the opamp.

For the SAR architecture, while it is digital and efficient, it suffers from issues if a high performance is required. First, the conversion speed is limited by the multiple clock cycles in one period. For a N -bit ADC with 1 bit per cycle, the conversion time is approximately $N(T_{COMP} + T_{DAC} + T_{logic})$. For a given CMOS process, the response time of each component is related to the power dissipation and its architecture, which cannot be neglected. The higher the resolution is, the longer the conversion period will be. Second, the resolution is limited by the property of the single stage. Since SAR topology imposes all the bits on the only one DAC, the area of the DAC limits the resolution of the SAR ADC. For example, in a differential 12 bit ADC, 8192 capacitor units are required. Considering that the capacitor unit is limited by the matching, the area occupied by the CDAC tends to be large and even can not be accepted. Third,

the accuracy is limited by the noise of the comparator. A low-noise comparator is desired, but its response time and power dissipation are usually unexpected.

2.2 Improved Pipelined ADC

Many efforts have been made to reduce the power dissipation of the pipelined ADC, which provides a good compromise between the high resolution and the high speed. The power-efficient SHA-less architecture, the multi-bit stage, and the redundancy technique are to be talked about in the section. All of them help to save the power dissipation and enhance the linearity of the ADC.

2.2.1 *SHA-less Architecture*

In a multistage ADC, the front-end SHA is the dominant noise, distortion and power contributor [7]. Removing the dedicated SHA and its noise, power, distortion, and area from the whole ADC budget is attractive and it has become the trend. In the SHA-less ADC, the sampling operation is distributed inside both the MDAC and flash ADC in the first stage. In other words, two sampling paths track the input signal, instead of the unique sampling path provided by the SHA. Because of that, the aperture error is introduced and hence high-frequency input performance is challenged. The details on the aperture error and its solutions are to be discussed.

2.2.1.1 Aperture Error

Since the high-frequency input signal instead of the held signal is directly provided for the SHA-less architecture, the samples of the flash ADC and that of the MDAC may be slightly different, which is the aperture error.

Because of the aperture error, the residue falls outside the designed range. Take a 2-bit individual stage with 1-bit redundancy as an example. The ideal input/output characteristics is indicated by the black line in Fig. 2.7. The sampling instant of the flash ADC may be delayed or advanced, and the difference between the sampling instant of the flash ADC and that of the MDAC is labeled $\Delta\tau$. The difference between the flash ADC' sample and the MDAC' is labeled ΔV . Four possible combinations of the input's slope and over-range voltage's sign are identified. As is shown in Fig. 2.7, in the first and second cases, the sampled input of the flash ADC is smaller than that of the MDAC, the decision levels move right, and hence, the over-range voltage is positive. In the third and fourth cases, the sampled input of the flash ADC is bigger than that of the MDAC, the decision levels move left. And thereby, the over-range voltage is negative.

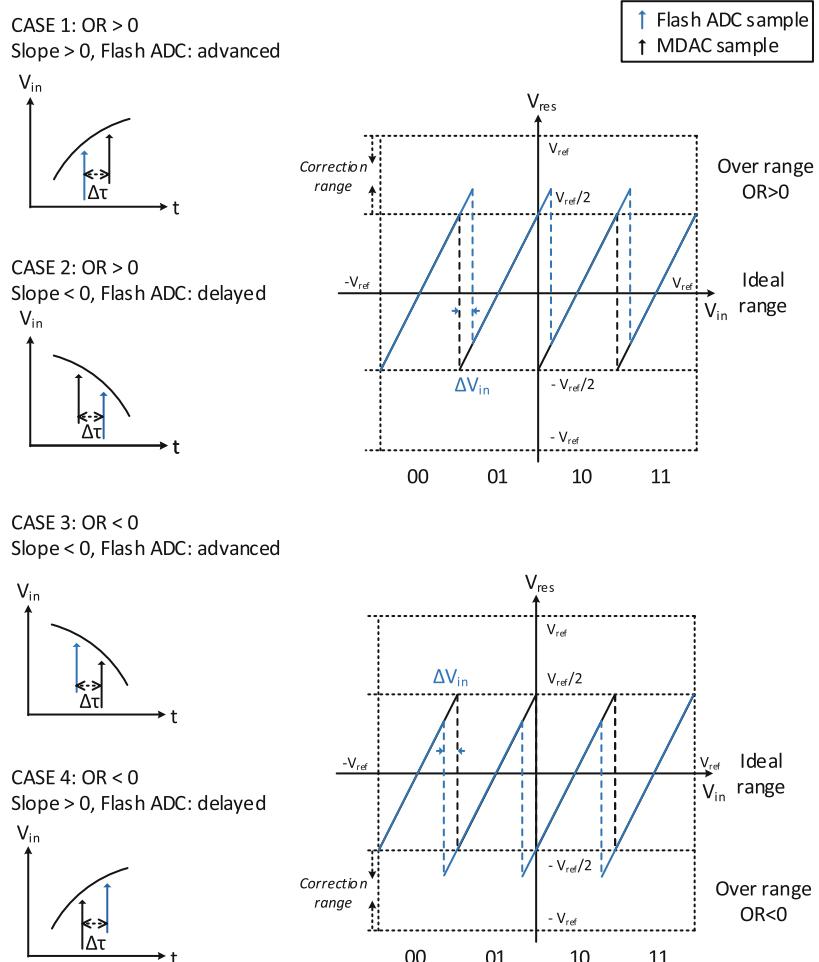


Fig. 2.7 The input/output characteristics of a 2-bit stage with the aperture error

Additionally, it should be noted that the over-range residue falls into the correction range. In other words, benefiting from the redundancy, the aperture error can be tolerated.

The aperture error limits the frequency of the analog input. Assuming the input voltage is a sinusoidal signal with the amplitude of A and the frequency of f_{in} , it can be written as

$$V_{in} = A \sin(2\pi f_{in} t) \quad (2.2)$$

The maximum sampling voltage error introduced by $\Delta\tau$ happens at the maximum slope of $2A\pi f_{in}$. Therefore,

$$V_{in,error} \leq 2A\pi f_{in}\Delta\tau \quad (2.3)$$

To realize the correct conversion, the residue voltage should not exceed the acceptable input range of the following stage. For the $(m+1)$ -bit individual stage with the redundancy of 1 bit, the tolerable input error is $\pm V_{FS}/2^{m+2}$, and thereby

$$2A\pi f_{in}\Delta\tau < \frac{V_{FS}}{2^{m+2}} \quad (2.4)$$

Assuming that the amplitude A is $V_{FS}/2$, the input frequency is limited by

$$f_{in} < \frac{1}{2^{m+2}\Delta\tau\pi} \quad (2.5)$$

Actually, $\Delta\tau$ is introduced for two reasons, the different time constant of the sampling network and different sampling instant.

In the sampling phase, both the input networks of MDAC and flash comparators track the input signal, as shown in Fig. 2.8. To provide the same time constant relative to the input, the sampling networks should satisfy [7]

$$\frac{R_{s1}}{R_{s1'}} = \frac{1/C_s}{1/C_{s'}} = \frac{R_{s2}}{R_{s2'}} = \frac{1/C_p}{1/C_{p'}} \quad (2.6)$$

where R_{s1} , $R_{s1'}$, R_{s2} , and $R_{s2'}$ are on-resistance of the sampling switches, C_s and $C_{s'}$ are the sampling capacitance, and C_p and $C_{p'}$ are the parasitic capacitance of the summing nodes. If the accurate matching cannot be realized, the aperture error appears. Besides, the sampling may happens at different instant due to the time skew between $\phi 1_p$ and $\phi 1'_p$. Although the unique sampling clock is provided to the networks, the parasitic resistance and capacitance in the two pathes results in slightly different RC delay. That also leads to the aperture error.

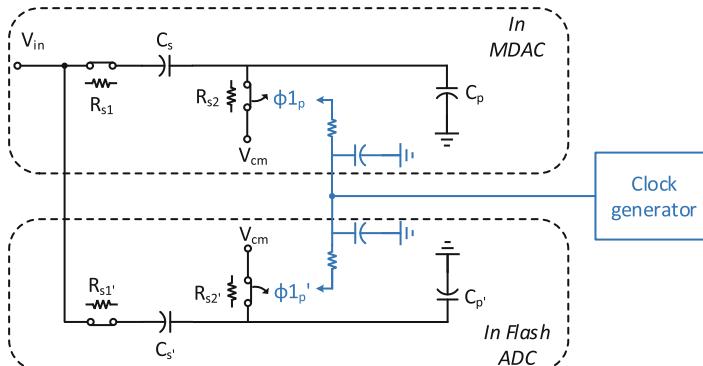


Fig. 2.8 Two input networks of MDAC and flash comparators in the sampling phase

2.2.1.2 Solutions to Aperture Error

Matching Sampling

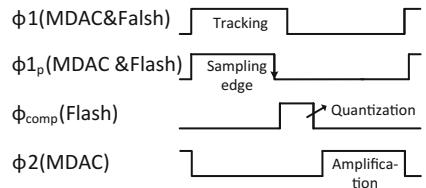
Since the aperture error is introduced by the mismatch between input networks, one of the solutions is to provide accurate matching to eliminate $\Delta\tau$ in Eq. 2.3. To realize that, the networks should be designed based on Eq. 2.6 and the high quality layout design is required.

However, one problem appears because that the sampling in the two networks is completed at the same time and there is no time left for the flash ADC to operate the normal conversion, providing the input of the MDAC in the following amplification phase. To solve that, a basic idea is to introduce an additional phase, ϕ_{comp} in Fig. 2.9, which can be adopted by the flash ADC to sample the reference voltage, redistribute the charge and make the decisions. ϕ_{comp} starts after $\phi 1_p$ and $\phi 1$, which control both the MDAC and flash ADC to track and sample the input, and ends before $\phi 2$, which controls the MDAC to amplify the residue voltage. As the cost paid for eliminating the dedicated SHA, the additional phase slows down the conversion rate of the traditional two-phase pipelined ADC, which cannot be accepted by the high-speed ADC. Another approach is to add additional capacitors to sample the reference voltage in the flash ADC, and hence reduce the charge distribution time, like in [8]. The cost is the complicated circuit and timing design.

To cope with the problem in Fig. 2.9, adopting the comparator to sample the input is proposed in [9, 10]. The first stage and its timing are described in Fig. 2.10. For the flash ADC, sampling the reference voltage is accomplished in the amplification phase, $\phi 2$, which enables that the continuing subtraction between signal and threshold is done during the tracking phase, $\phi 1$. Both the MDAC and comparators sample the input at the falling edge of $\phi 1_p$. Thanks to the charge redistribution in $\phi 1$, comparators are able to make the decisions before the rising edge of $\phi 2_d$, leaving enough time for the MDAC. To track the analog input, the comparator's pre-amplifier and the input path of the flash ADC must provide large bandwidth to rapidly respond to the high-frequency input. To avoid exceeding the stage's correction range, the matching between the MDAC sampling network and the comparator is required, and hence the bandwidth of the pre-amplifier should satisfy

$$\tan^{-1} \frac{f_{in}}{f_{BWmax}} = 2\pi \frac{f_{in}}{\Delta\tau_{max}} \quad (2.7)$$

Fig. 2.9 Adjusted timing due to the aperture error



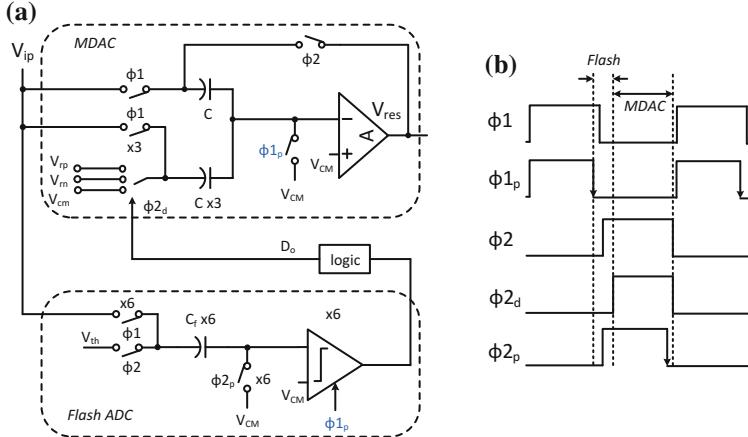


Fig. 2.10 The **a** first stage and **b** timing proposed in [9]

where $\Delta\tau_{max}$ can be obtained according to Eq. 2.4. The higher the input frequency is, the higher the bandwidth will be. This technique is verified in a 12-bit 270 MSps pipelined ADC and the measurement results are shown in Fig. 2.11. It reveals the dynamic performance for an input frequency sweep at 200 MSps and 270 MSps, (THD contains 2nd-10th harmonic). At 200 MSps, the ADC achieves the THD of 78.2 dB and the SNR of 69.5 dB for a 30.1 MHz input, and achieves the THD of 62.5 dB and the SNR of 58.9 dB for a high-frequency 195.1 MHz input. At 270 MSps, the ADC achieves the THD of 74.7 dB and the SNR of 64.4 dB for a 30.1 MHz input, and achieves the THD of 66.1 dB and the SNR of 57.3 dB for a high-frequency 195.1 MHz input. The cost of this technique is that more power is consumed in comparators. Besides, it should be noted that the total power dissipation increases at an exponential rate with the increased number of comparators in a multi-bit flash ADC, limiting the application of this technique in a multi-bit front end.

To save the power of the comparator without reducing the conversion rate, the modification of the timing is proposed in [11]. $\phi 1_a$ is introduced to enable the sampling instant to be advanced, as is shown in Fig. 2.12. The advantages are as follows.

1. The tracking time is compressed so that more time is left for comparators to make decisions. The operation time of the flash ADC is composed of the delay between the falling edge of $\phi 1_a$ and $\phi 1$ and the nonoverlapping time between $\phi 1$ and $\phi 2$.
2. From the point of view of the implementation, compared with the traditional sampling instant, $\phi 1_p$, in Fig. 2.10, the gate delay between the low-jitter clock input and $\phi 1_a$ is smaller, and thereby the jitter of $\phi 1_a$ is lower. Therefore, the proposed sampling instant is helpful to improve the sampling accuracy.

Besides, in Fig. 2.12, both input networks of the MDAC and the flash ADC accomplish the sampling at the same instant to eliminate the aperture error. Benefiting

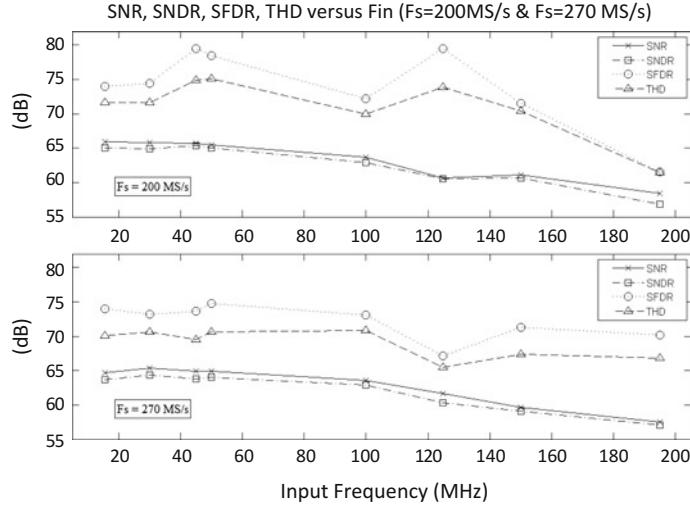


Fig. 2.11 Measured SNR, SNDR, SFDR, THD versus the input frequency

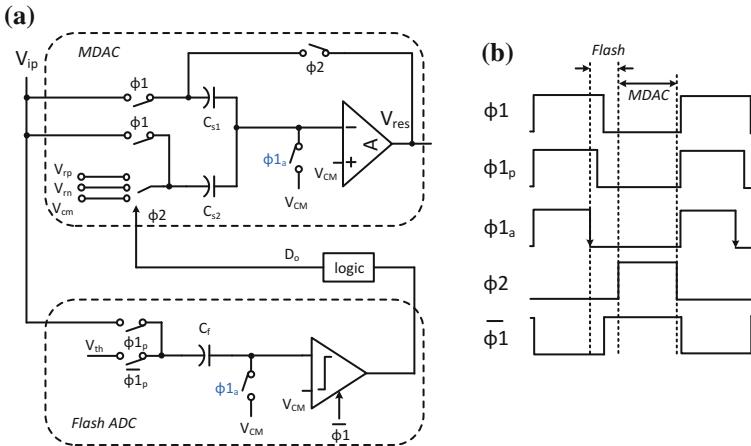


Fig. 2.12 The a first stage and b timing proposed in [11]

from the proposed timing, low-power dynamic comparator can be adopted in the flash ADC, saving the power dissipation effectively.

What's more, the requirement of the opamp's bandwidth is relaxed because of the enough time provided for the amplification. Since the opamp consumes most of power dissipation in a high-performance ADC, the power saved by it is considerable.

Calibrating Sampling

Besides matching the sampling between the MDAC and flash ADC, the calibration can be adopted by the SHA-less ADC to eliminate the aperture error. An over-range calibration is proposed in [12] and its basic idea is discussed here. It is used in a SHA-less ADC, comprising a 2.5-b MDAC, followed by a 8-b SAR ADC. With the aperture error, the residue voltage of the MDAC exceeds the ideal range, entering the correction range, and hence over range appears, as is shown in Fig. 2.13. As is discussed in Fig. 2.7, four possible combinations of the input's slope and over-range voltage's sign are identified, and the sampling instant of the flash ADC is delayed or advanced, correspondingly. The calibration works by adjusting the sampling instant of the flash ADC with respect to the MDAC's, based on the input's slope and the over-range voltage's sign. Benefit from the technique, multi-GHz input signal can be converted by the ADC. The cost of this technique is the additional power dissipation of the calibration block.

Sharing Sampling

Since the mismatch of two sampling pathes of the MDAC and flash ADC results in the aperture error, merging them into a unique sampling path can eliminate the error. An aperture error reduction technique of sharing the sampling networks is proposed and verified in a subranging SAR ADC [13]. By reusing capacitors of the flash ADC in the fine conversion phase, thermometer coarse capacitors belonging to the traditional CDAC are removed. This technique does not only minimize aperture error effectively but also reduces input capacitance. The details on the sharing sampling are to be discussed.

To illustrate the sharing sampling, the operation of the traditional and the proposed architecture are both depicted.

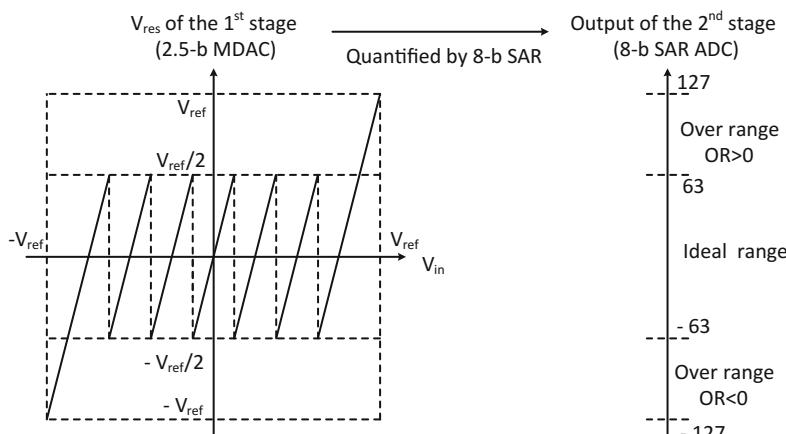


Fig. 2.13 The transfer curve of the 2.5-b MDAC in [12]

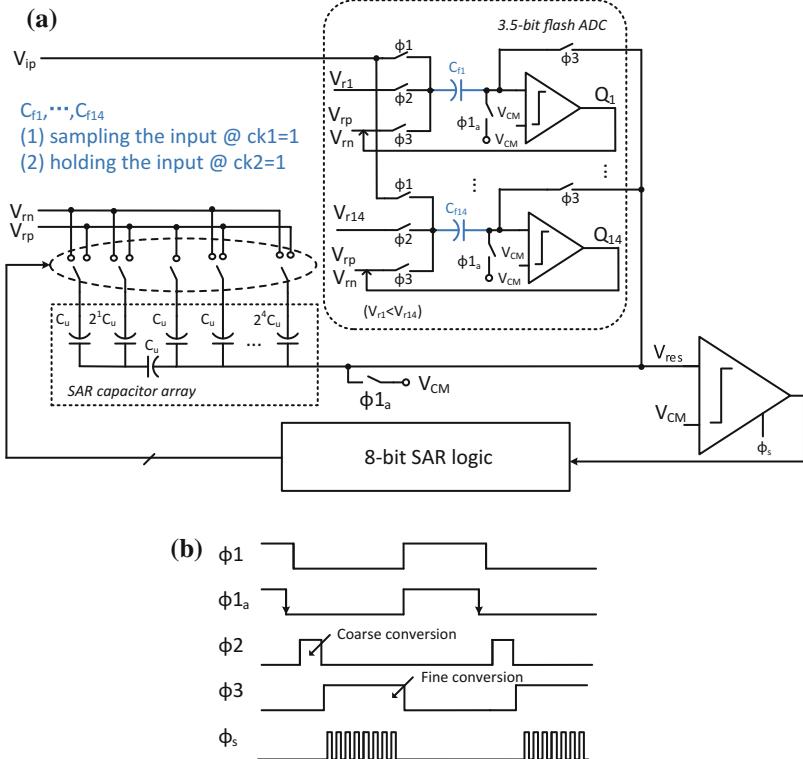
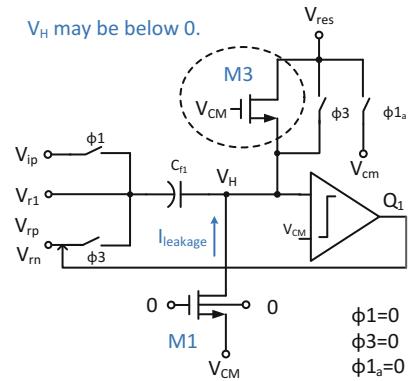


Fig. 2.14 The **a** subranging SAR ADC with aperture error reduction technique and **b** timing

1. A conventional 11-bit subranging SAR ADC without front-end T/H is depicted in Fig. 2.30a, comprising a 3.5-bit flash ADC for the coarse conversion, followed by an 8-bit SAR ADC for the fine conversion. The ADC employs two paths, capacitors $C_i (i = 1, \dots, 14)$ in the CDAC and capacitors $C_{fi} (i = 1, \dots, 14)$ in the flash ADC, to track the input in the sampling phase, $\phi 1 = 1$, as shown in Fig. 2.30b. And the sampling happens at the falling edge of $\phi 1_a$. When $\phi 2$ is high, the flash ADC operates the coarse comparison and outputs the most significant bits (MSBs), Q_i , which control the capacitors C_i during the following fine conversion phase.
2. A SHA-less subranging SAR ADC with the sharing sampling is shown in Fig. 2.14. When $\phi 1$ is high, only capacitors C_{fi} track the input and sample it at the falling edge of $\phi 1_a$. When $\phi 2$ is high, the flash ADC operates the coarse conversion and outputs Q_i , just like the conventional one. Once the flash ADC conversion finishes, $\phi 3$ goes high and capacitors C_{fi} and the SAR capacitor array are connected together. Q_i control the bottom plates of capacitors C_{fi} to attach to V_{rp} or V_{rn} , operating as the flash capacitor array in Fig. 2.30.

Fig. 2.15 The charge leakage error in the coarse conversion phase and the solution



Therefore, unlike the conventional SHA-less subranging SAR ADC, the new architecture does not employ coarse capacitors C_i . The unique sampling capacitors, C_{fi} , sample the input, hold the charge, and provide the charge for the flash ADC in the coarse conversion phase and the CDAC in the fine conversion phase. Benefit from the unique sampling path, this technique does not only minimize the aperture error but also reduces the input capacitance.

Because that the principle of the technique is based on the switched-capacitor charge redistribution, any charge injection or leakage to C_{fi} is unacceptable. Actually, in the coarse conversion phase, the charge leakage may happen in the 1st or the last comparator. Take the 1st comparator in the flash ADC to illustrate that. It should be noted that V_{r1} is close to $V_{cm} - V_{ref}/2$. As is shown in Fig. 2.15, when $\phi 2$ becomes high, the bottom plate of C_{f1} switches to the reference voltage V_{r1} . And the voltage at the capacitor's top plate, V_H , can be derived as

$$V_H = V_{cm} - V_{ip} + V_{r1} \quad (2.8)$$

where V_{cm} is the common-mode voltage, V_{ip} is the input signal. Considering that V_{ip} is the maximum, i.e., $V_{cm} + V_{ref}/2$, V_H can be rewritten as

$$V_H \approx V_{cm} - (V_{cm} + V_{ref}/2) + V_{cm} - V_{ref}/2 = V_{cm} - V_{ref}/2 \quad (2.9)$$

where V_{ref} is the full scale of the single-ended input. Normally, in the SAR ADC, V_{cm} is $V_{DD}/2$, V_{ref} is V_{DD} , and hence V_H is

$$V_H \approx -V_{DD}/2 \quad (2.10)$$

In that situation, the substrate-to-drain leakage appears in switch transistor M1 and hence unexpected charge is added to C_{f1} . In the following fine conversion phase, the residue voltage, V_{res} , will deviate, decreasing the conversion accuracy of ADC. To solve the leakage, transistor M3 is introduced. If V_H drops and becomes small

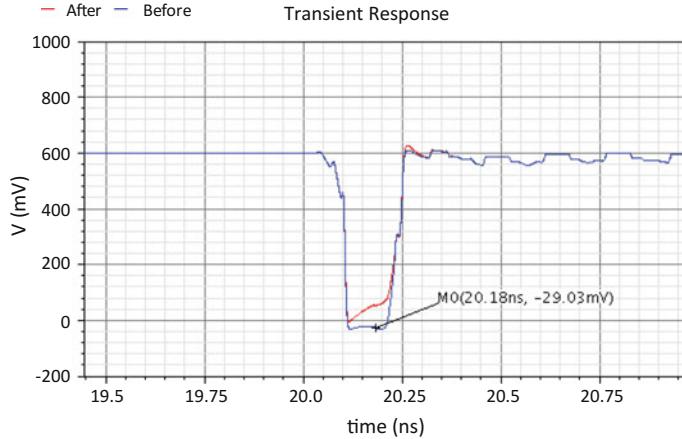


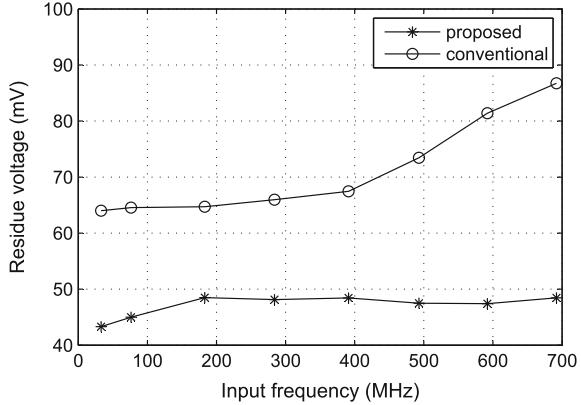
Fig. 2.16 The transient response of V_H before and after introducing M3 (simulated by Spectre)

enough ($\leq -V_{th}$) to switch on M1, M3 will also switch on ($V_{gs,M3} = V_{cm} + V_{th}$) to charge the node V_H by connecting it with V_{res} in advance. V_{res} has been charged to V_{cm} in the sampling phase. The increased V_H prevents the leakage immediately. Besides, the injected charge to V_H by M3 does not affect the comparison result. That is because it is so small that the output does not switch. The simulated transient response of V_H is shown in Fig. 2.16. With the aid of M3, V_H rises immediately to prevent the leakage. Similarly, the preventing leakage transistor is adopted by the last comparator. Additionally, the charge leakage in the the 1st or the last comparator can be decreased by compressing V_{ref} or adopting the redundancy of 0.5 bit. The 11-bit 200 Msps subranging SAR ADC with the sharing sampling in Fig. 2.14 is designed in a 65 nm CMOS technology. For the comparison, the conventional subranging SAR ADC in Fig. 2.30 is also designed. Since the flash ADC and CDAC adopt the same clock, the sampling edge's mismatch is not considered in the simulation. Fig. 2.17 contrasts the maximum residue voltage after the coarse conversion phase, which shows the influence of aperture error directly. It is indicated that the aperture error can be reduced effectively with the proposed technique. Furthermore, the benefit of this technique will be more prominent in practice due to the layout parasitic.

2.2.2 Multi-bit Front End

Multi-bit front end can significantly reduce the power dissipation for the high-SNR noise-limited ADC [14–16]. It is to be discussed from the noise, the power dissipation, and the linearity.

Fig. 2.17 Maximum residue versus input frequency (simulated by Spectre)



2.2.2.1 Noise

By adopting the multi-bit front end, the noise of the ADC can be optimized because the increased interstage gain of the first stage compresses the noise contribution of the back-end stages. If the resolution increases 1 bit, the interstage gain, G , scales up by a factor of 2 and the feedback factor, β , scales down by a factor of 2.

The noise sampled by the first stage in the tracking phase (referred to the input of the ADC) is

$$\sigma_1 \propto \sqrt{\frac{KT}{\beta G C_S}} \quad (2.11)$$

where C_S is the sampling capacitor. For extra bits, σ_1 maintains the same.

The noise sampled by the second stage is composed of two parts, the noise due to the sampling network in the second stage and the noise due to the amplifier in the first stage. When referred to the input of the ADC, they can be written as [16]

$$\sigma_{2,sw2} \propto \frac{1}{G} \sqrt{\frac{KT}{C_L}} \quad (2.12)$$

$$\sigma_{2,amp1} \propto \frac{1}{G} \sqrt{\frac{KT}{\beta C_L}} \quad (2.13)$$

where C_L is the total load, consisting of the sampling capacitor and the feedback capacitor, C_F , in the first stage, the sampling capacitor, C_{S2} in the second stage, and parasitic capacitors. For each additional bit in the first stage, $\sigma_{2,sw2}$ is reduced by $1/\sqrt{2}$, and $\sigma_{2,amp1}$ is also decreased by $1/\sqrt{2}$.

Therefore, for the fixed sampling capacitance, higher SNR can be achieved. From another point of view, for a given noise budget, the noise reduction enables the

lower power and the smaller sampling capacitance. The smaller sampling capacitance makes the ADC easy to drive, and the power saving will be talked about in detail.

2.2.2.2 Power Consumption

For a fixed noise budget, for each extra bit in the front end, C_L can be reduced to a quarter according to Eq. 2.12, and C_L can be reduced to a half according to Eq. 2.13. Based on the tradeoffs, C_L can be reduced to a value which is between 1/2 and 1/4.

Considering that the close-loop bandwidth of the amplifier is

$$BW = \beta \frac{g_m}{2\pi C_L} \quad (2.14)$$

in the best case, g_m can be reduced by half, maintaining the same bandwidth. And hence the current of the amplifier can be decreased by almost a half. Since amplifier consumes most of the power dissipation, the saved power is considerable.

2.2.2.3 Linearity

On one hand, multi-bit front end reduces the nonlinearity of the first stage. For a N -bit ADC including a M -bit first stage, the DNL error caused by the capacitor mismatch in the first stage can be derived as [17] (normalized to the LSB)

$$DNL = \frac{\gamma 2^{N-0.5M}}{\sqrt{C_{tot}}} \quad (2.15)$$

and

$$\gamma = \frac{\Delta C_i}{\sqrt{C}} \quad (2.16)$$

where ΔC_i is the error of each capacitance, C is the nominal value of each capacitor, and C_{tot} is the total capacitance. Therefore, the DNL error is compressed by $\sqrt{2}$ with every extra bit in the first stage, and it is also reduced by $\sqrt{2}$ with the doubled total capacitance.

On the other hand, the increased interstage gain associated with a high-resolution stage reduces the nonlinearity of the following stages(referred to the input of the ADC).

While the multi-bit front end enables the ADC to optimize the noise, reduce the power, and compress the nonlinearity, one problem is introduced. Since the tolerable input error is $\pm V_{FS}/2^{m+2}$ for the $(m+1)$ -bit individual stage with the redundancy of 1 bit, the tolerable comparator's offset (referred to the input of the flash ADC) is reduced. Therefore, multi-bit front end increases the comparator complexity.

2.2.3 Redundancy Technique

Besides precision analog design techniques and calibration techniques, introducing redundancy is another solution to mitigating the nonideal factors in the ADC. The fundamental differences from the calibration is that the errors are neither measured nor corrected, but simply tolerated and rejected by the redundancy [18]. From another point of view, the idea behind the technique is that the accurate value can be expressed in multiple and equivalent ways with the redundancy. The redundancy-aided conversion dates back to 1964 [19]. And after that, many variations are proposed to cope with the noise, as well as other nonidealities, such as the capacitor mismatch, finite sampling bandwidth, comparator's offset, DAC settling errors, and so on.

2.2.3.1 Redundant Decision Levels

Redundant decision levels is first proposed in [19], where four comparators instead of three ones are adopted to convert 2 bits, absorbing large conversion errors. Since then, the technique is widely adopted in the pipelined ADCs. In the redundancy-aided ADC, the sum of the stage's resolution is larger than the total resolution and then the redundancy is corrected to tolerate the nonlinearity.

The individual stage with 1-bit redundancy is described in [3] to tolerate the comparator' offset by scaling down the interstage gain by 2, as shown in Fig. 2.18. The 2-bit digital outputs are 00, 01, 10, and 11. The input-referred offset as large as $\pm V_{ref}/4$ in the comparator can be tolerated and the correction rang of the residue is $\pm V_{ref}/2$. The redundancy is eliminated by a correction logic, which is illustrated by an ADC comprising five pipelined stages, as shown in Fig. 2.19. Since that the interstage gain is reduced by half, the output of the next stage moves left to compensate for that. The disadvantage of this algorithm is that an offset is introduced to the ADC. For example, if the input is $-V_{ref}$, the output is 001111 based on Figs. 2.18 and 2.19 but the expected code is 000000. That offset can be avoided by the individual stage with 0.5-bit redundancy proposed in [20].

The input/output characteristics of a 1.5-bit stage is illustrated in Fig. 2.20. Considering a 6-bit ADC consisting of 4 1.5-bit stages and a 2-bit stage, the input of $-V_{ref}$ is converted into 000000, eliminating the offset. Although the long tail of V_{res} exceed $\pm V_{ref}/2$, the corrected comparator's offset is still $\pm V_{ref}/4$. Besides, the absence of code 11 avoids the overflow of the corrected output. And removing the decision level of 0 is helpful to improve the linearity of the small swing input's conversion. As to the name of 1.5 bit, it is because $2^n - 2$ (n is the number of digital output bits and here n is 2) comparators are needed in 1.5-bit stage and the resolution is $\log_2(2^n - 1) = 1.5$ bit.

Based on the discussion above, for a $(m+1)$ -bit or $(m+0.5)$ -bit individual stage with the unique error source of the comparator's offset, the offset of $\pm V_{FS}/2^{m+2}$ can be tolerated by the of 1-bit or 0.5-bit redundancy. And V_{FS} is the full scale of the input.

Fig. 2.18 Ideal residue versus input with the redundancy of 1 bit

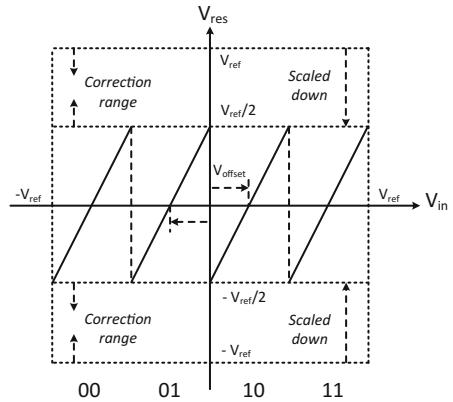


Fig. 2.19 A 6-bit output calculated by the correction algorithm

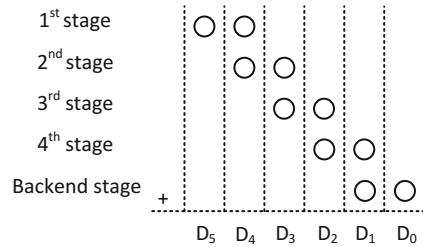
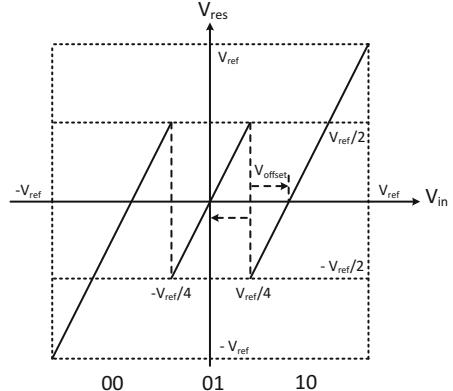


Fig. 2.20 Ideal residue versus input with the redundancy of 0.5 bit



2.2.3.2 Redundant Decision Steps

The technique of redundant decision steps is usually adopted in the SAR ADC to absorb conversion errors via increasing conversion cycles. Therefore, a unique N-bit code can be described by multiple (N+R)-bit codes and R is the number of extra bits. Besides, the cost is the additional hardware of logics for redundant cycles.

For an ideal ADC with the radix of 2, the conversion result can be described by a binary expansion, which is

$$V' = \sum_{k=1}^N D_k 2^{-k} \quad (2.17)$$

where D_k is either 0 or 1 and $V' - V$ is the quantization error. The bit, D_k , is obtained by a binary search algorithm that uses the recursion of

$$V_k = V_{k-1} + S_k 2^{-k} \quad (2.18)$$

where

$$S_k = \begin{cases} 1 & V > V_k \\ -1 & V \leq V_k \end{cases} \quad (2.19)$$

and

$$b_k = (S_k + 1)/2 \quad (2.20)$$

Besides, the modification of Eq. 2.17 is

$$V' = \alpha \sum_{k=1}^N D_k \beta^{-k} \quad (2.21)$$

where $1 < \beta < 2$ and $\alpha = \beta - 1$ is a scale factor to set the full scale to unity. It is called beta-expansion [21].

From another point of view, Eq. 2.18 is realized by the DAC settling and Eq. 2.19 is realized via the comparator's operation. Those operations introduce two types of errors to the SAR ADC, the DAC settling error due to the finite speed of the DAC and the comparison error due to the finite accuracy of the comparator. Both of them can be tolerated by the redundancy.

Redundancy in Designs of Radix = 2

Incomplete settling can be tolerated by the redundancy and the associated calibration. Actually, the digital output of the ADC is obtained by comparing the analog input voltage with the reference voltage. For the traditional conversion in Fig. 2.21a, the equivalent reference voltage is reduced by half in each conversion cycle. For the conversion in Fig. 2.21b, the settling error is compensated for by shifting the equivalent reference voltage and using the extra bit to obtain the same code [22]. The operation in each cycle is illustrated in Fig. 2.21b in detail. The cost of this method is additional compensative capacitors and a error correction logic circuit.

Redundancy in Designs of Radix < 2

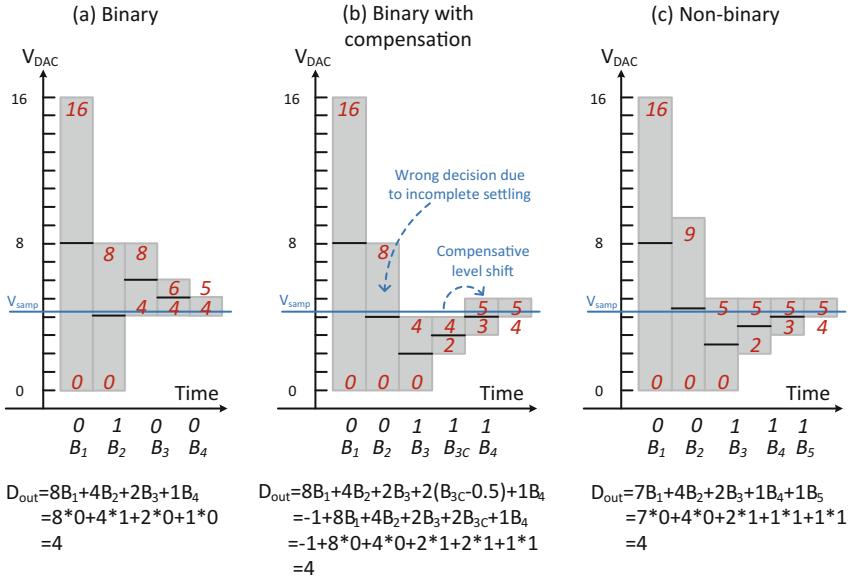


Fig. 2.21 Successive approximations using different methods

The output of a non-binary ADC is described by Eq. 2.21 and an example of the operation is illustrated in Fig. 2.21c, where the equivalent reference voltage is reduced by a factor of smaller than 2 after each DAC switching. Thanks to the redundancy, the settling error with a certain range can be tolerated. However, more conversion cycles and non-binary conversion lead to additional control logic and ROM to store the bit weights [23].

2.3 Improved SAR ADC

A lot of improvements have been achieved after 2000s, because the SAR ADC is digital and friendly to the CMOS technology. To raise the power efficiency, the set-and-down architecture is adopted. In the view of speed improvement, the asynchronous SAR conversion, the multi-bit/cycle SAR ADC, the conversion of redundancy and the time-interleaved SAR ADC are proposed. To effectively increase the resolution, the SAR ADC with a bridge capacitor is commonly used. The techniques are described here.

2.3.1 Power-Efficient Architecture

Switching the capacitive array consumes significant power. While the unit capacitance is limited by the KT/C noise, the switching sequence can be modified to improve the power efficiency. The set-and-down architecture is proposed in [24]. It saves time and power, compared with the classical SAR ADC in [25]. Examples of 3 bit switching operation are described in Figs. 2.22 and 2.23. In the sampling phase in

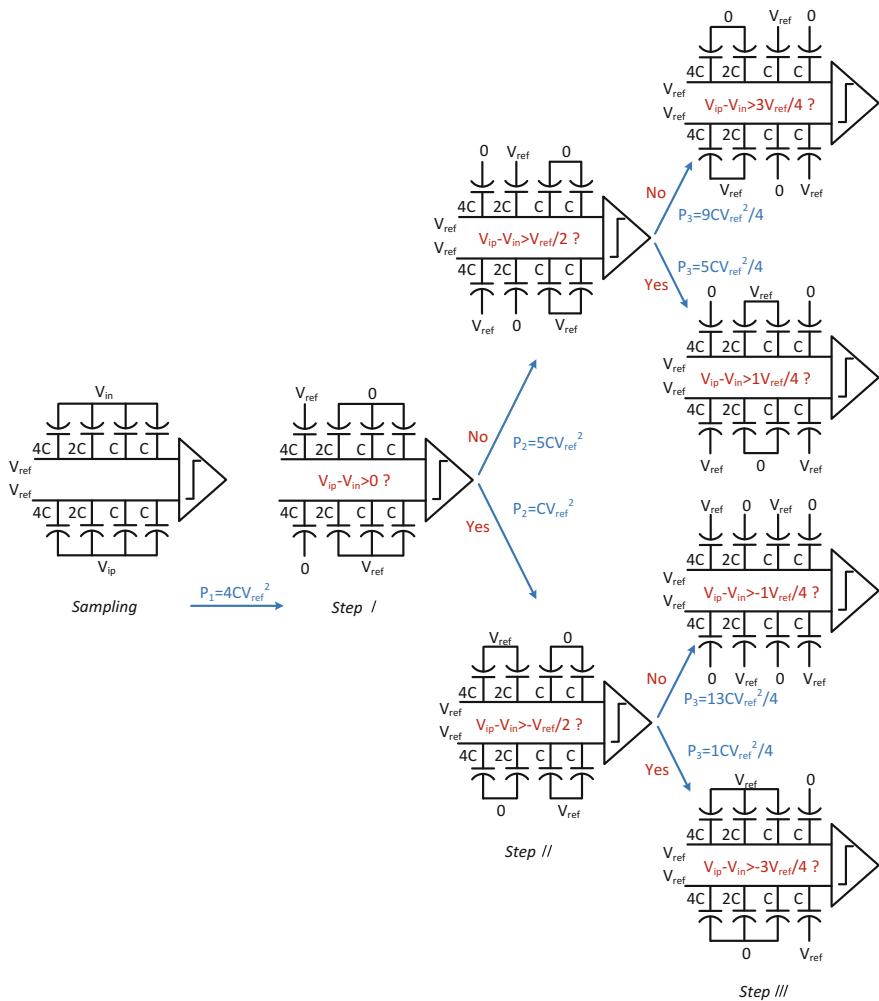


Fig. 2.22 Conventional switching sequence of 3 bit SAR ADC

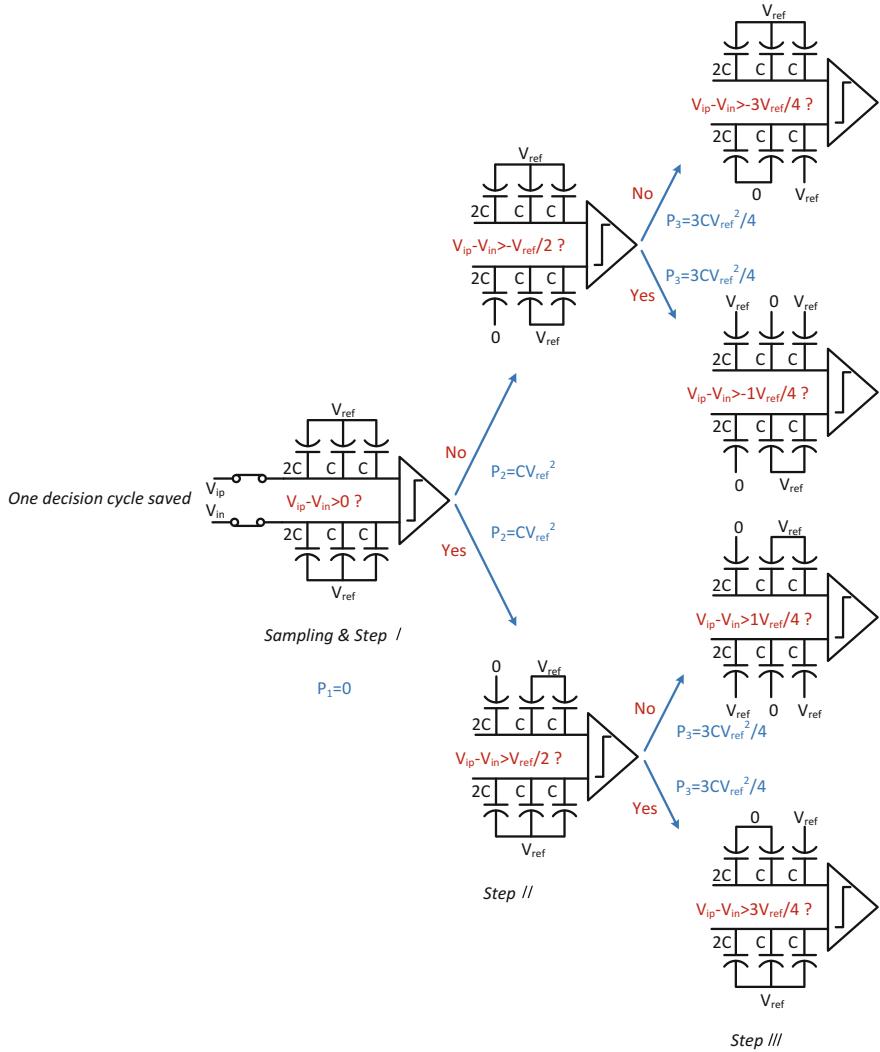


Fig. 2.23 Improved switching sequence of 3 bit SAR ADC in [24]

Fig. 2.23, the input voltage is directly connected to the input node of the comparator and the top plates of the capacitors. The bottom plates of the capacitors are set to V_{ref} at the same time. The comparator tracks the analog input and latched at the end of the sampling phase. Next, the input of the DAC is changed by connecting only one relevant capacitor to 0, resulting in the change of the input of the comparator. Then, a new output of the comparator resets the input of the DAC and starts another conversion cycle. For an n -bit SAR ADC with the conventional switching sequence in Fig. 2.22, the average switching energy can be derived as [25]

$$E_{total,n \text{ bit}} = \sum_{i=1}^n 2^{n+1-2i} (2^i - 1) CV_{ref}^2 \quad (2.22)$$

For an n -bit SAR ADC using the set-and-down switching sequence, the average switching energy can be derived as [24]

$$E_{total,n \text{ bit}} = \sum_{i=1}^{n-1} (2^{n-2-i}) CV_{ref}^2 \quad (2.23)$$

While a 10-bit SAR ADC using the conventional switching sequence consumes $1363.3CV_{ref}^2$, the one using the set-and-down switching sequence only consumes $255.5CV_{ref}^2$ and saves 81.3% power dissipation. Besides, one cycle is saved by the set-and-down switching method, which is competitive for the high-resolution and high-speed SAR ADC.

However, the conversion accuracy suffers from the architecture in Fig. 2.23. Sampling switches directly attach to differential inputs of the comparator, and hence the charge in the switches is injected to the comparator at the sampling instant. As a result, inputs of the comparator are disturbed, which may lead to the incorrect outputs and degrade the conversion accuracy. Therefore, the approach requires a comparator with good common-mode rejection.

2.3.1.2 Vcm-Based Architecture

Vcm-based switching approach is proposed in [26] to reduce the power further and avoid large common-mode jumps. Compared with the set-and-down switching, before bit decisions are obtained, bottoms of capacitors are connected to V_{cm} instead of V_{ref} or 0. However, the on-resistance in the switch connected to V_{cm} , like SW_3 in Fig. 2.24a, increases, because that V_{gs} of the switch transistors is reduced (V_{cm} is normally half of V_{ref}). As a result, the increased RC constant slows down the DAC settling. To respond to that, the split capacitor Vcm-based architecture is proposed. A capacitor from the DAC capacitor array is described in Fig. 2.24 to illustrate the modification. In the Vcm-based architecture, the capacitor bottom may be connected to 0, V_{ref} , or V_{cm} via switch SW_1 , SW_2 , or SW_3 in Fig. 2.24a. In the split Vcm-based architecture, the capacitor, SW_1 , and SW_2 split, and SW_3 is removed in Fig. 2.24b. And the operation of shorting $2C$ and V_{cm} is replaced by shorting C_1 and 0 and shorting C_2 and V_{ref} , as shown in Fig. 2.24c. Compared with [26], the modification not only increases the DAC settling, but also simplifies the SAR logic. But, for the minimum capacitor (which is normally the capacitor unit) in the capacitor array, the approach can not be adopted.

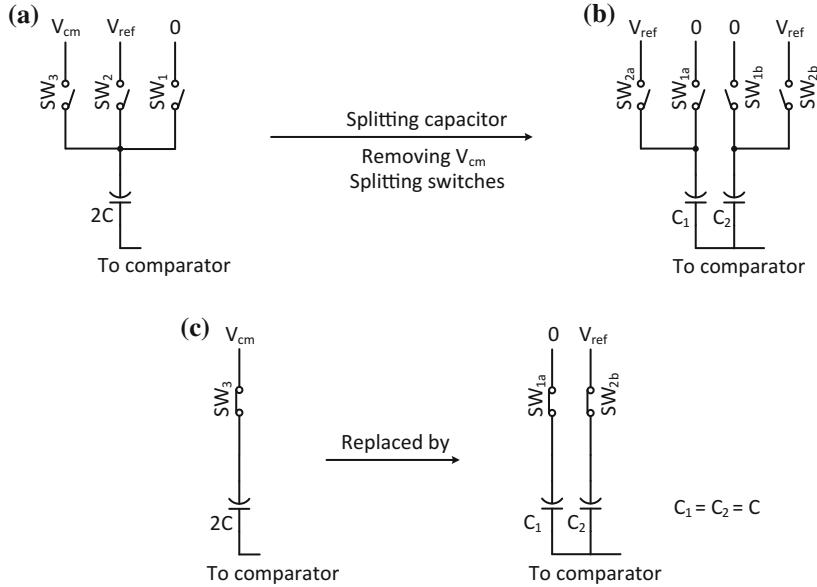


Fig. 2.24 A capacitor in **a** V_{cm}-based architecture and **b** split capacitor V_{cm}-based architecture, and **c** the operation of shorting the capacitor bottom and V_{cm}

2.3.2 High-Speed Architecture

2.3.2.1 Asynchronous Clocking Architecture

An asynchronous SAR ADC is proposed in [27] to exceed the power and speed limitations of a synchronous SAR ADC. For a synchronous N -bit SAR ADC with the conversion rate of F_S , an internal clock running at least $(N + 1)F_S$ is required, which is described in Fig. 2.25a. To implement a high-resolution and high-speed ADC, the clock generator and clock distribution network would consume more power than the ADC core itself, which is a significant overhead. Besides, every clock has to tolerate the worst conversion time and consider the margin for the clock jitter, which slows down the speed of the ADC. For an asynchronous SAR ADC, the high-speed internal clock is removed, shown in Fig. 2.25b. The comparison is triggered from the MSB to LSB like dominos. Once the current comparison is finished, a signal is generated to trigger the next comparison. The asynchronous clocking is commonly adopted by high-performance SAR ADC.

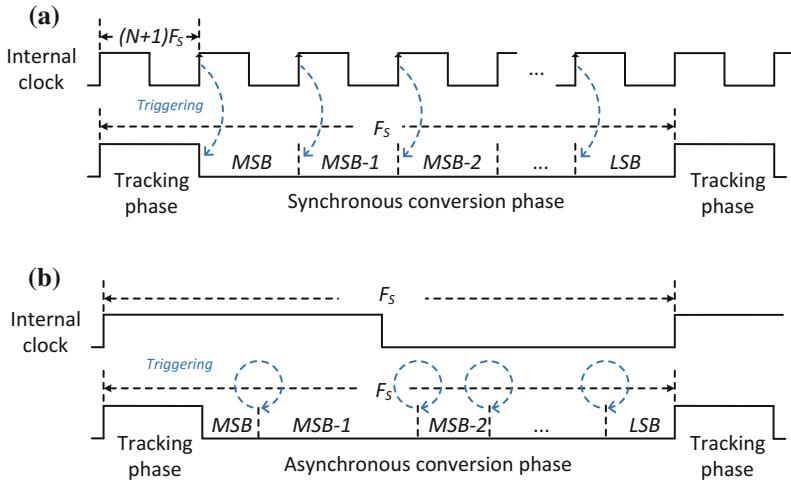


Fig. 2.25 Conversion of **a** synchronous and **b** asynchronous SAR ADC

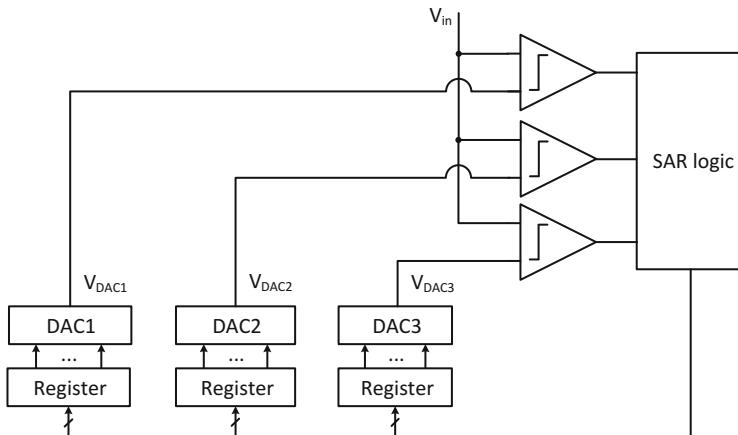


Fig. 2.26 SAR ADC with 2 bits per cycle

2.3.2.2 Multi-Bit-Cycle Architecture

To combine the high speed of a flash ADC and the low-power dissipation of a SAR ADC, converting more than one bit per cycle is proposed, like 2 bits per cycle in [6, 28, 29] and 3 bits per cycle in [30]. A simple 2-bit-cycle SAR ADC is illustrated in Fig. 2.26. In each cycle, 2 bits are provided to speed up the conversion rate. However, 3 comparators, 3 DACs and additional logics are required. The considerable growth in area, complexity and input capacitance (for capacitive DAC) lead to large hardware overhead, especially for the case of more than 2 bits per cycle. Besides, the random

offsets of the comparators limit the linearity of the conversion. To solve these issues, interpolation is adopted in [30] to decrease the number of comparators and DAC capacitors, and the offset calibration is used in [28–30] to improve the accuracy of the ADC.

2.3.2.3 Others

Interleaving channels of SAR ADC is a direct way to proportionally increase the speed. The generic issues of the time-interleaved architecture (to be discussed in Sects. 2.5 and 6.2.4) apply here as well, including increased area and input capacitance and interchannel mismatches. Besides, the channels couple with one other through the shared reference voltage, limiting the accuracy of the ADC [6].

2.3.3 Low-Area Architecture

To respond to the problem that the number of the unit capacitors exponentially increases with the raising resolutions, the capacitor array with a bridge capacitor is commonly adopted [6, 31]. A $(M + L + 1)$ -bit SAR ADC with a bridge capacitor, C_b , is described in Fig. 2.27a. There are M binary weighted capacitors and a C_{d1} in the MSB segment, and L binary weighted capacitors and a C_{d2} in the LSB segment. The contribution of the capacitors in LSB segment to the DAC output is scaled down due to C_b . Therefore, the unit capacitor in the LSB segment is scaled up, decreasing the capacitor mismatch and improving the linearity of the ADC. In order to calculate the capacitance, C_b , the response to bottom plates of its adjacent capacitors, $2^{L-1}C_u$ and kC_u , is illustrated in Fig. 2.27b. C_{Mt} and C_{Lt} are the total capacitance of the MSB segment and the LSB segment, respectively. They are given by

$$C_{Mt} = (2^M - 1)kC_u + C_{d1} \quad (2.24)$$

$$C_{Lt} = (2^L - 1)C_u + C_{d2} \quad (2.25)$$

At the DAC output, the step response of the two capacitors should satisfy

$$\Delta V_{o1} = 2\Delta V_{o2} \quad (2.26)$$

where

$$\Delta V_{o1} = \frac{kC_u(C_b + C_{Lt})}{X} \Delta V \quad (2.27)$$

$$\Delta V_{o2} = \frac{2^{L-1}C_bC_u}{X} \Delta V \quad (2.28)$$

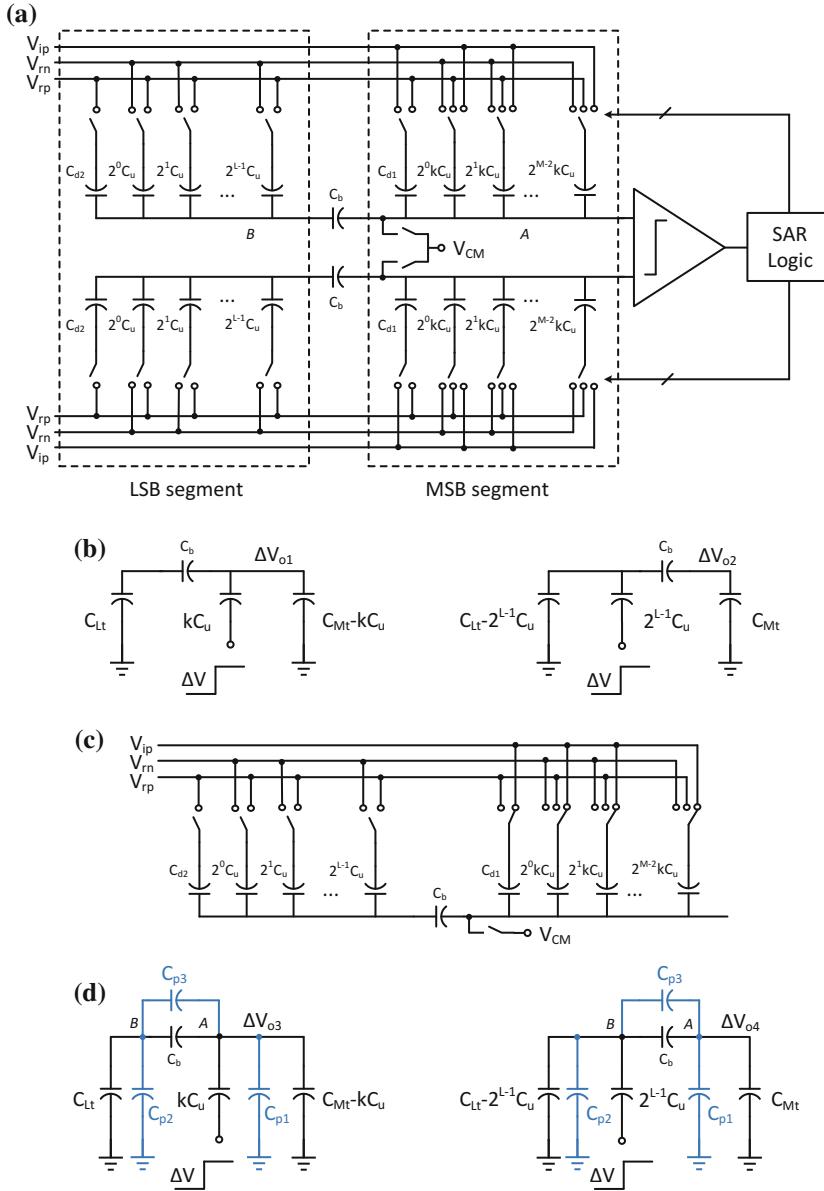


Fig. 2.27 **a** SAR ADC adopting a bridge capacitor, **b** the response to a *bottom plate* swing of ΔV , **c** operations in the sampling phase, and **d** the response to a *bottom-plate* swing of ΔV (single end is shown for simplicity in **b**, **c** and **d**)

And,

$$X = C_{Mt}(C_b + C_{Lt}) + C_b C_{Lt} \quad (2.29)$$

Therefore, the bridge capacitor can be derived as

$$\frac{C_b}{C_u} = \frac{k}{2^L - k} \frac{C_{Lt}}{C_u} = \frac{k}{2^L - k} \frac{(2^L - 1)C_u + C_{d2}}{C_u} \quad (2.30)$$

And,

$$\frac{C_{d2}}{C_u} \geq 0 \quad (2.31)$$

In Eqs. 2.30 and 2.31, C_b/C_u is the positive integer and C_{d2}/C_u is the nonnegative integer. For a given segmented capacitive DAC, M , L and k are fixed and C_b only depends on C_{d2} . C_b is usually calculated according to the minimum C_{d2} . Several examples of segmented DACs and the bridge capacitors are described in Table 2.1.

As to C_{d1} , it satisfies

$$C_{d1} = kC_u \quad (2.32)$$

Because C_{d1} samples the input, capacitors in the LSB segment do not sample the input voltage, as shown in Fig. 2.27c. Input capacitance is reduced and there is no gain error caused. Capacitor C_{d1} and its parasitics have no contribution to the gain error, which only depends on the ratio of total sampling capacitors to total DAC capacitors.

The bridge capacitor architecture suffers from the parasitic capacitors, including the grounded ones at A and B and the coupling one between A and B , which cause errors at the DAC output. To analyze the errors, the step response to the adjacent capacitors of C_b , $2^{L-1}C_u$ and kC_u , is described in Fig. 2.27d. ΔV_{o3} and ΔV_{o4} can be derived as

$$\Delta V_{o3} = \frac{kC_u(C_b + C_{p3} + C_{Lt} + C_{p2})}{Y} \Delta V \quad (2.33)$$

$$\Delta V_{o4} = \frac{2^{L-1}(C_b + C_{p3}C_u)}{Y} \Delta V \quad (2.34)$$

where

Table 2.1 Design of bridge capacitors

DACs	Given parameters	C_b (minimum C_{d2} adopted)
DAC1	$M = 4, L = 4, k = 1$	$C_b = C_u \ (C_{d2} = 0)$
DAC2	$M = 2, L = 6, k = 2^4$	$C_b = 21C_u \ (C_{d2} = 0)$
DAC2	$M = 4, L = 6, k = 2^2$	$C_b = 5C_u \ (C_{d2} = 12C_u)$
DAC2	$M = 4, L = 8, k = 2^4$	$C_b = 17C_u \ (C_{d2} = 0)$

$$Y = (C_{Mt} + C_{p1})(C_b + C_{p3} + C_{Lt} + C_{p2}) + (C_b + C_{p3})(C_{Lt} + C_{p2}) \quad (2.35)$$

Ideally, the binary bit weights require

$$\Delta V_{o3} = 2\Delta V_{o4} \quad (2.36)$$

The nonideal bit weights caused by the bridge capacitor's parasitics can be described as

$$\epsilon = \frac{\Delta V_{o3} - 2\Delta V_{o4}}{2\Delta V_{o4}} \approx \frac{C_{p2}}{C_{Lt}} - \frac{C_{p3}}{C_b} \quad (2.37)$$

Therefore, the bit weights suffer from C_{p2} and C_{p3} , resulting in the nonlinearity of the ADC. C_{p1} only leads to the gain error at the DAC output.

2.3.4 Summing up

Techniques discussed above and their cost are as follows.

To save the power dissipation, different switching approaches are proposed. While set-and-down architecture with top-plate sampling saves the power and time, it requires a comparator with good common-mode rejection, since large common-mode jumps occur during charge redistribution. Vcm-based architecture saves the power further and reduces common-mode jumps, but it suffers from the slow DAC settling. To respond to that, split capacitor Vcm-based switching is proposed. However, for the minimum capacitor (which is normally the capacitor unit) in the capacitor array, the approach can not be adopted.

The asynchronous clocking and multi-bit-cycle architecture are commonly adopted by high-speed single-channel SAR ADC. However, for the case of more than 2 bits per cycle, the considerable growth in area, complexity and input capacitance (for capacitive DAC) lead to large hardware overhead. Besides, the random offsets of the comparators limit the linearity of the conversion. For the time-interleaved SAR ADC, the cost of the increased speed includes increased area and input capacitance, interchannel mismatches, and so on.

To respond to the problem that the number of the unit capacitors exponentially increases with the raising resolutions, the capacitor array with a bridge capacitor is commonly adopted. Parasitic capacitors of the bridge capacitor degrade the linearity.

2.4 Hybrid ADC

As shown in Fig. 2.28, the hybrid ADC combines the high speed of the flash ADC, the low power of the SAR ADC, and the effective compromise of high speed and high resolution in the pipelined ADC, improving the performance and saving the power

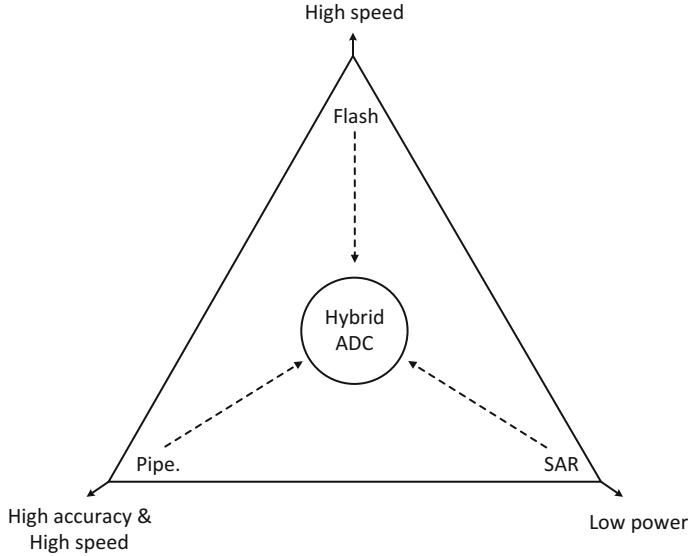


Fig. 2.28 The hybrid ADC based on traditional architectures

dissipation. In this section, we discuss the subranging SAR ADC and the pipelined SAR ADC.

2.4.1 Subranging SAR ADC

The subranging SAR has the potential to realize the fast and power-efficient conversion. A common subranging architecture is depicted in Fig. 2.29. It consists of a coarse ADC, a DAC, a fine ADC and a correction block, operating the sampling, the coarse, and the fine conversion in one period. For the subranging SAR ADC, the coarse conversion is accomplished by the flash ADC and the fine conversion is done by the SAR ADC. The first N_1 MSBs are output in parallel, speeding up the conversion. The comparators' accuracy of the flash ADC is relaxed due to the redundancy. Furthermore, the power-hungry opamp is removed in the architecture, reducing the power dissipation.

Here is an 11-bit subranging SAR as an example, as shown in Fig. 2.30. It includes a 3.5-bit flash ADC for the coarse conversion, followed by an 8-bit SAR ADC for the fine conversion. When $\phi 1$ is high, the capacitor array and the flash ADC track the input and sample it at the falling edge of $\phi 1_a$. When $\phi 2$ is high, the flash ADC operates the coarse comparison and outputs the MSBs, Q_i , which control the capacitors C_i during the following fine conversion phase. From a point of view of the capacitive DAC, the 3.5-bit MSB settling are overlapped, and hence there is only one critical

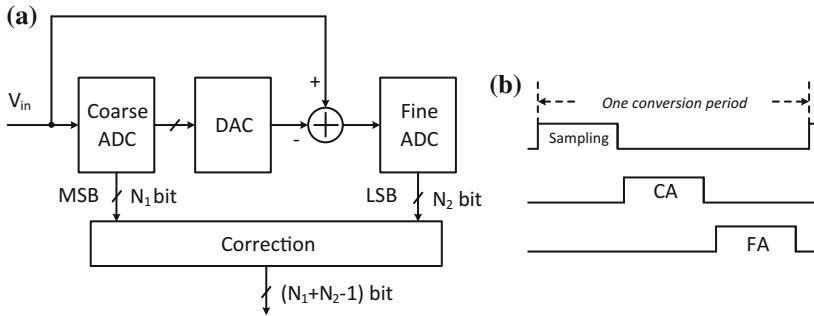


Fig. 2.29 **a** The concept of a subranging ADC and **b** the timing

DAC settling. The 8-bit LSB settle times are based on the SAR principle. As a two-stage architecture, its input/output characteristics of the coarse stage is similar to that of a individual stage in a pipelined ADC and the slope is 1 due to the absence of the residue amplifier, as is show in Fig. 2.30c.

2.4.2 Pipelined SAR ADC

The pipelined SAR ADC adopts the SAR architecture as the sub-ADC in the pipelined stages, avoiding requirements of high-accuracy comparators and the extra front-end sample-and-hold. It combines the high resolution of the pipelined architecture and the low-power dissipation of the SAR ADC.

The topology of a pipelined SAR ADC is shown in Fig. 2.31. The ADC is composed of two stages, the SAR-assisted first-stage and the second-stage SAR. In the first stage, both the sampling networks of the sub-ADC and the MDAC are merged in the capacitive DAC. Besides, the DAC, the comparator and the SAR logic generate N_1 -bit code and the residue voltage to be amplified. The interstage gain of 2^{M1} is provided by the closed-loop opamp. The second stage is implemented by a N_2 -bit SAR ADC.

2.5 Time-Interleaved ADC

The time-interleaved ADC speeds up the conversion rate using n parallel identical ADCs, which operate in time multiplexing way. As is shown in Fig. 2.32, although every ADC converts data at the low rate of F_s/n (here n is 4 as an example), the time-interleaved ADC achieves the high speed of F_s . Besides, time-interleaved architecture can be adopted by any ADCs, such as the pipelined ADC, the SAR ADC, the flash ADC, and so on.

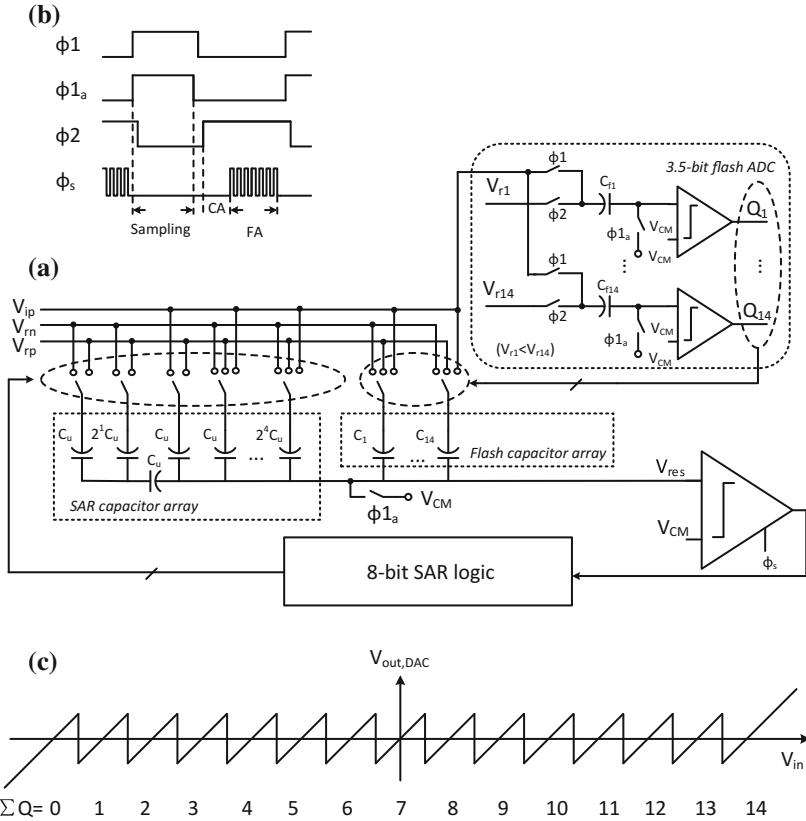


Fig. 2.30 **a** An 11-bit subranging SAR ADC, **b** the timing, and **c** the input/output characteristics of the coarse stage

2.6 Summing up

In this chapter, different ADC architectures are discussed. First, three traditional ADCs are presented. Although lots of Nyquist-rate ADCs are proposed to resolve resolutions at different speeds throughout the years, there are three types of architectures most widely used and they are the pipelined ADC, the SAR ADC, and the flash ADC. Second, the improvement of them are analyzed, because they all have the potential to achieve the high performance and the high-power efficiency, via the adjustment in the architecture level or with the aid of useful techniques. Then, we talk about the hybrid ADC, which combines the high speed of the flash ADC, the low power of the SAR ADC, and the effective compromise of high speed and high resolution in the pipelined ADC. In addition, the time-interleaved technique is discussed. It effectively assists the low-power single-channel ADC in improving the conversion rate.

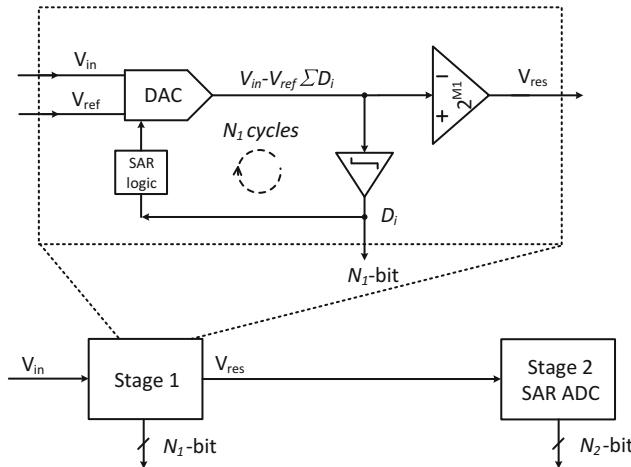


Fig. 2.31 The pipelined SAR ADC

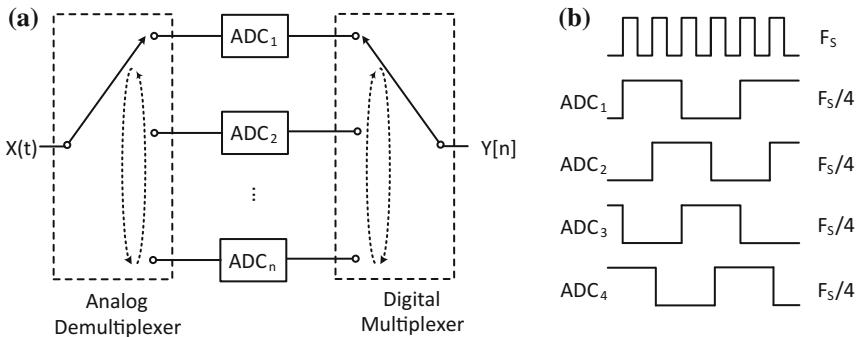


Fig. 2.32 The **a** time-interleaved ADC and **b** timing

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Chapter 3

Reference Voltage Buffer

3.1 Introduction

Analog-to-digital convertor converts the analog signal by weighting it against the reference voltage. Accurate reference voltage is provided by the reference buffer to support the high-performance data conversion. Designing the high-performance reference buffer is a big challenge, especially for the high-speed and high-resolution switched-capacitor (SC) ADC.

High-performance ADC requires the fast-settling and precise reference voltage. In Fig. 3.1, a reference buffer drives a SC circuit in the amplification phase. The current is drawn out of the reference voltage, V_{ref} , to charge or discharge the capacitive load. Considering a 14-bit 150MSps ADC with $T = 6.67$ ns, V_{ref} is required to set the desired level with a error ($<V_{LSB}/4$) within T_1 . T_1 is much shorter than $T/2$ (assuming that the amplification phase is $T/2$) to leave enough time for the accuracy settling of SC circuit.

3.2 Traditional Reference Voltage Buffer

Different techniques of reference voltage buffers have been developed. There are mainly two categories, reference voltage buffers with off-chip capacitors and fully integrated reference voltage buffers. They are to be discussed in the following sections.

3.2.1 Buffer with Off-Chip Capacitor

The large-capacitor-aided narrow-bandwidth buffer [1–3] is composed of an inverting amplifier in the close loop and a large decoupling capacitor, as is shown in Fig. 3.2.

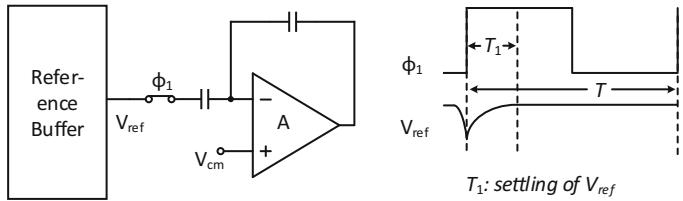
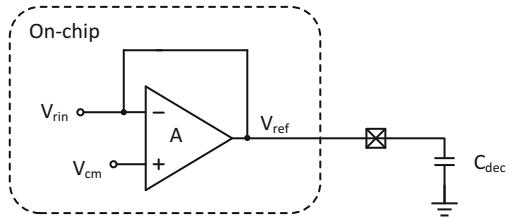


Fig. 3.1 Reference voltage buffer driving a switched-capacitor circuit

Fig. 3.2 The large-capacitor-aided narrow-bandwidth buffer



Off-chip capacitor is usually adopted in the area-saving ADC. This type of buffer results in low power and low noise [3]. However, off-chip capacitor leads to extra pads. Even though the double or triple bonding could be used to minimize the bond wire inductance, the settling accuracy is still limited.

3.2.2 Fully Integrated Buffer

Fully integrated wide-band reference buffer includes the passive resistor ladder, the active source follower or source follower based reference buffer [4–7]. They usually consume quiet amount of power (e.g., 20–30% of the overall power consumption) in a high-speed ADC. Therefore, it is worthy of putting efforts in optimizing the power consumption.

The conventional fully integrated reference buffers are presented in Fig. 3.3. Figure 3.3a is a passive resistor ladder [4, 5]. Its bandwidth is $1/RC_L$ (R is the impedance of the node V_{ref}). Figure 3.3b is an active source follower and the bandwidth is gm/C_L (gm is the transconductance of transistor M_n). The power consumption of high-speed buffer tends to be large. Normally the resistor ladder consumes power one order of magnitude larger than the source follower. Besides, in Fig. 3.3b, kicks introduced by the capacitive load disturb the gate voltage of the source follower by capacitor coupling, which limits the accuracy of the reference voltage.

The reference buffers in Fig. 3.3c, d are both composed of slow feedback loops and open-loop *Buffer Branch* [6, 7]. The bandwidth is determined by source followers in *Buffer Branch*. In Fig. 3.3c, *Buffer Branch* is composed of PMOS and NMOS transistors. The main disadvantage of this topology is the high power consumption and the low-power supply rejection ratio (PSRR), caused by the slow PMOS transis-

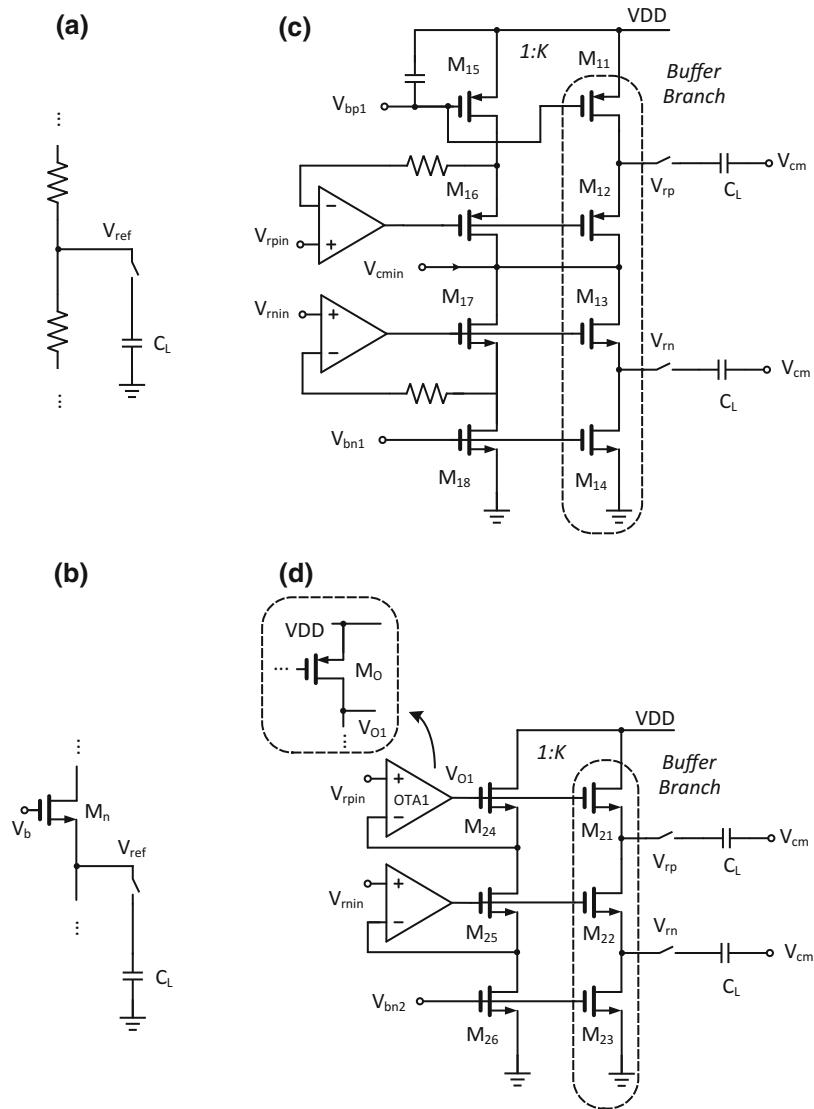


Fig. 3.3 Topology of the conventional fully integrated reference buffers (single-ended reference buffers are presented in **a** and **b** for simplicity)

tors M_{11} and M_{12} . The parasitic capacitors of PMOS transistors do not only increase the load, but also couple the noise of the power supply to V_{rp} to degrade the PSRR. In Fig. 3.3d, only fast NMOS transistors are used in *Buffer Branch*. However, the maximum output voltage is limited by M_{21} at $VDD - V_{gs21} - V_{ov}$ and the output swing is only

$$VDD - V_{gs21} - V_{ov} - V_{ov23} \quad (3.1)$$

where V_{ov} and V_{ov23} are the overdrive voltages of the output transistor in *OT A1* and M_{23} , respectively. The low swing limits the SNR of the ADC.

3.3 Improved Reference Voltage Buffer

The challenges of reference voltage buffer include increasing the output swing and improving the accuracy. To respond to those, a level-shifter-aided CMOS reference voltage buffer is proposed to enlarge the swing, and a charge-compensation-based (CCB) technique is proposed to cancel the input-dependent errors. They are to be discussed in the following sections.

3.3.1 Level-Shifter-Aided Buffer

A level-shifter-aided CMOS reference voltage buffer for high-speed high-resolution switched-capacitor ADC is presented in this section. It adopts a level shifter for wide swing and a NMOS-only branch circuit for low power. Besides, the proposed architecture improves the PSRR. This reference buffer is integrated in a 14-bit 150 MSps low-power pipelined ADC with the amplification phase of only 2.5 ns. With the input of 2.4 MHz and 2 V_{p-p} , the measurement of the fabricated ADC shows that the SNDR is 71.3 dB and the SFDR is 93.6 dBc. And the power consumption of the reference buffer is 17 mW from a 1.3 V power supply.

3.3.1.1 Proposed Reference Buffer

The topology of the proposed reference buffer is shown in Fig. 3.4. The reference buffer has an open-loop *Buffer Branch* driven by slow negative feedback loops, and the upper loop includes a level shifter. The feedback loops monitor feedback voltages, regulate the gate voltages of M_{34} and M_{35} , and adjust their source voltages to the desired levels. Source followers M_{31} and M_{32} in the *Buffer Branch* provide the isolation between the capacitive load and the feedback loops. Besides, the branch of M_{34} , M_{35} and M_{36} is a replica of the open-loop branch, by a scale of $1/K$. The matching between them provides accurate reproduction of the feedback voltages. Therefore, V_{rp} and V_{rn} set the desired levels. C_0 is adopted to compress the noise,

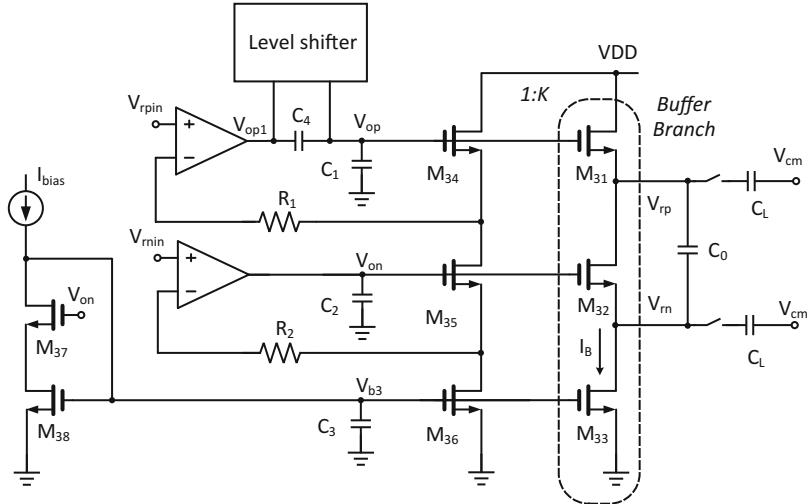


Fig. 3.4 Topology of the proposed reference buffer

and C_L is the load. Additionally, since the level shifter enables the gate voltage of M_{31} to increase, the output swing of the buffer is enlarged.

Output Swing and Power Consumption

For the wide swing, a level shifter is used to boost the gate voltages of M_{34} and M_{31} . With the gate voltage higher than VDD , V_{rp} gets close to the supply voltage. The maximum output voltage is $VDD - V_{ov31}$ and the minimum output voltage is V_{ov33} , where V_{ov31} and V_{ov33} are the overdrive voltages of M_{31} and M_{33} . The output swing is

$$VDD - V_{ov31} - V_{ov33} \quad (3.2)$$

which is wider than that of the conventional reference buffer in Fig. 3.3d.

To achieve the high bandwidth without increasing the power consumption, NMOS-only *Buffer Branch* is used in the proposed architecture. Compared with PMOS, NMOS can provide the same transconductance with smaller parasitic capacitance. NMOS-only buffer can achieve wider bandwidth than NMOS-PMOS mixed buffer under the same bias current. For node V_{rp} (single-ended output is analyzed for simplicity), the bandwidth measured in Hz can be described by

$$BW_{V_{rp}} = \frac{gm_{31}}{2\pi C_{V_{rp}}} = \frac{2I_{DS31}}{2\pi C_{V_{rp}} V_{ov31}} \quad (3.3)$$

gm_{31} is the transconductance of M_{31} , $C_{V_{rp}}$ is the load capacitor of V_{rp} and I_{DS31} is the bias current. $C_{V_{rp}}$ is composed of the capacitor in SC circuit and the parasitic capacitors in *Buffer Branch*, which can be given by

$$C_{V_{rp}} \approx C_L + C_{GS31} + C_{B31} + C_{DB32} \approx C_L + 3C_{GS31} \quad (3.4)$$

Therefore, the bias current of *Buffer Branch* is

$$I_{DS31} \approx BW_{V_{rp}}\pi V_{ov31}[C_L + 3C_{GS31}] \quad (3.5)$$

For comparison, the bias current of *Buffer Branch* in Fig. 3.3c, where both PMOS and NMOS transistors are used, can be given by

$$I_{DS11} \approx BW_{V_{rp}}\pi V_{ov12}[C_L + 3C_{GS12}] \quad (3.6)$$

For nearly the same overdrive voltage and transconductance, C_{GS} of PMOS M_{12} is about $\mu n/\mu p$ times larger than that of NMOS M_{31} . To drive high-speed SC circuit, C_{GS} may be comparable to C_L . Therefore, the bias current of M_{31} is obviously smaller than that of M_{12} . The proposed reference buffer consumes lower power than the conventional buffer shown in Fig. 3.3c.

PSRR Consideration

High PSRR of the reference buffer is expected to improve the accuracy of output voltage. As shown in Fig. 3.5a, b, the noise in the power supply is coupled to the outputs through capacitors, which reduces the stability of V_{rp} and V'_{rp} .

For the proposed reference buffer in Fig. 3.5a, C_{dec} is the decoupling capacitor (NMOS-capacitor) connected between the gate of M_{31} and the ground. The noise at the gate of M_{31} can be negligible due to the strong decoupling. R is the equivalent impedance of the cascode M_{32} and M_{33} . The noise current injecting into V_{rp} is given by

$$I_n = (g_{ds} + SC_{ds})V_n \quad (3.7)$$

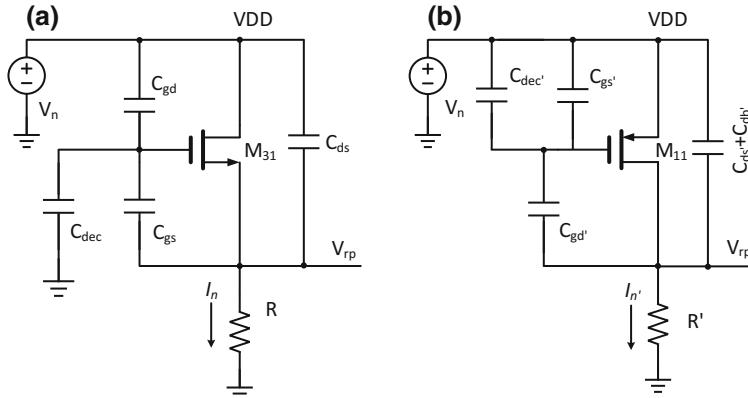


Fig. 3.5 Noise currents in **a** proposed reference buffer and **b** conventional reference buffer in Fig. 3.3c

where g_{ds} is the transadmittance of M_{31} and V_n is the noise voltage.

Then consider the PSRR of the conventional reference buffer in Fig. 3.3c. As shown in Fig. 3.5b, C'_{dec} is the decoupling capacitor (PMOS-capacitor) connected between the gate of M_{11} and the power supply. All the noise at VDD is coupled to the gate of M_{11} . R' is the equivalent impedance of M_{12} , M_{13} and M_{14} . The noise current injecting into V'_{rp} is given by

$$I'_n = (g'_{ds} + SC'_{gd} + SC'_{ds} + SC'_{db})V_n \quad (3.8)$$

where g'_{ds} is the transadmittance of M_{11} .

Comparing Eq. 3.7 with Eq. 3.8, the noise current injecting into V'_{rp} is much bigger than that injecting into V_{rp} . That means the noise gain between power supply and the output in Fig. 3.5a is smaller than that in Fig. 3.5b. Considering the gain between the input and the output is similar in the two reference buffers, the PSRR in the proposed topology is improved effectively.

3.3.1.2 Implementation

The level shifter adopted is described in Fig. 3.6. The level shifter is controlled by a two-phase nonoverlapping clock, ϕ_1 and ϕ_2 . V_{b1} and V_{b2} are the bias voltages generated by a resistor ladder shown in Fig. 3.6b. V_{op1} is the output of the OTA and V_{op} is the gate voltage of M_{34} . The top four switches in Fig. 3.6a are PMOS switches and the bottom switches are NMOS switches. The two-phase nonoverlapping clock is generated by ADC core drove by the buffer. In order to turn PMOS switches fully off, the clock with swing of 1.2 V is not adequate. A clock booster shown in Fig. 3.6b is used to increase the swing. C_5 and C_6 are charged by V_{b1} and V_{b2} to compensate for the charge on C_4 alternately. V_{op} is

$$V_{op} = V_{op1} + (V_{b2} - V_{b1}) \quad (3.9)$$

The parasitic capacitors in node N_1 , N_2 , N_3 and N_4 are non-ignorable and should be considered. The parasitic capacitors consist of the parasitic capacitors of switches and C_5 (or C_6). Taking N_1 for example, the parasitic capacitor, C_p , and the two switches connected to N_1 work as a resistor R_{cp} ($= 1/C_p f$). f is the clock frequency. In Fig. 3.6c, leakage currents I_1 and I_2 are introduced due to R_{cp} and R'_{cp} . Leakage currents at V_{op1} and V_{op} introduce a DC offset voltage. The solution is adopting small switches and capacitors, high-quality layout and connecting the top capacitor plate to V_{op} . Actually, if C_5 and C_6 are small, the settling of the reference voltages will be slow after power on. The capacitance of C_5 and C_6 is a tradeoff between leakage currents and the settling time. In this level shifter, C_5 and C_6 are both $200fF$.

The AC equivalent circuit of the level shifter is shown in Fig. 3.6d. As mentioned above, a capacitor and a two-phase nonoverlapping clock is equivalent to a resistor, $1/Cf$ (labeled as R_{eq}). C is the capacitance of C_6 (C_5 equals C_6) and f is the clock frequency. The loop gain can be given by

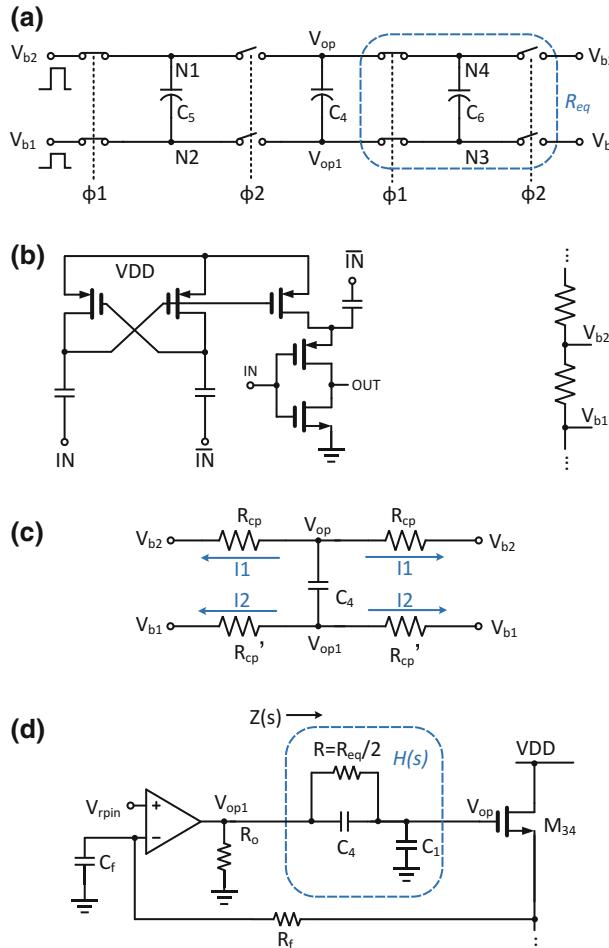


Fig. 3.6 **a** The level shifter adopted in the proposed reference buffer, **b** clock booster and bias-voltage generator, **c** leakage currents in the level shifter **d** loop analysis

$$Lp(S) = \frac{1}{1 + SC_f R_f} g_{m, OTA}(R_o/Z(S)) H(S) \quad (3.10)$$

$$H(S) = \frac{RSC_4 + 1}{RS(C_4 + C_1) + 1}, \quad Z(S) = \frac{RS(C_1 + C_4) + 1}{(RSC_4 + 1)SC_1} \quad (3.11)$$

$$\omega_z = \frac{1}{RC_4} \approx \omega_{p2}, \quad \omega_{p1} \approx \frac{1}{R_o C_1}, \quad \omega_{p3} = \frac{1}{C_f R_f} \quad (3.12)$$

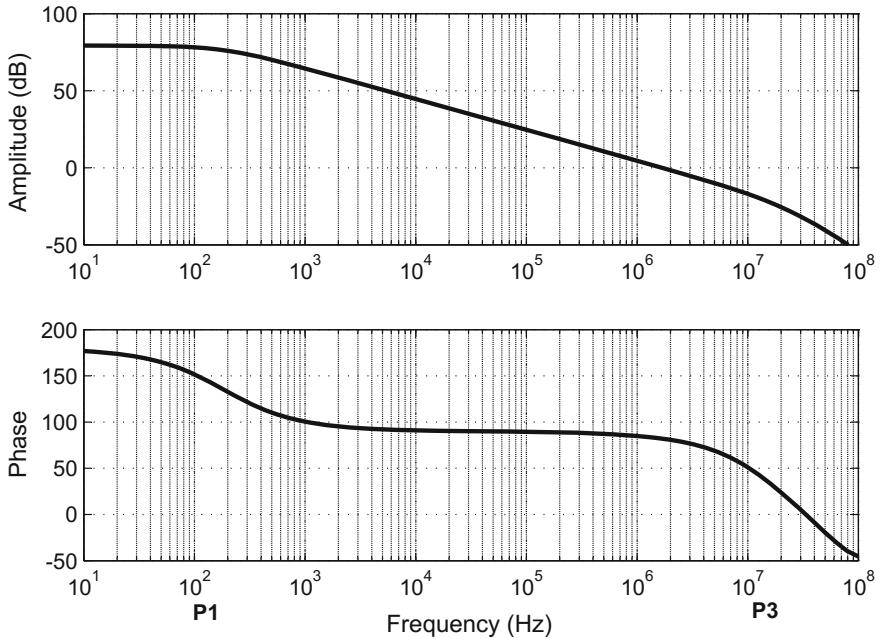


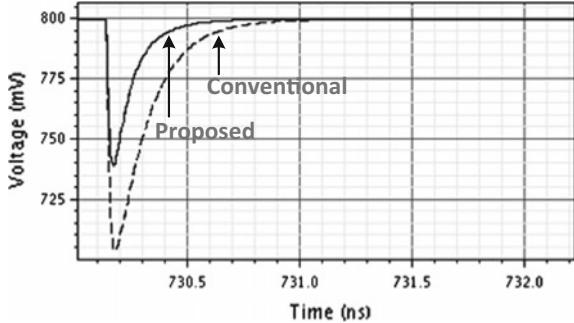
Fig. 3.7 Bode plot of the loop gain

where $g_{m,OTA}$ and R_o are the equivalent transconductance and the output impedance of OTA, respectively. The magnitude and phase plot of the loop gain is shown in Fig. 3.7. The loop contributes three poles and a zero. The neighboring pole-zero pair ω_{p2} and ω_z cancel each other. The phase shift is only 90° within the gain crossover frequency. This loop with the level shifter is always stable.

Besides, the output swing of the buffer, $V_{rp} - V_{rn}$, is 1 V. The overdrive voltages of M_{31} , M_{32} and M_{33} , shown in Fig. 3.4, are all as small as 60 mV. Consuming the same current, small overdrive voltage makes the transconductance large and increases the output swing. The decoupling MOSFET capacitors C_1 , C_2 and C_3 are all about 100 pF . C_1 and C_2 are helpful to suppress the kick-back glitches introduced by the load and the thermal noise.

In a standard 0.13- μm CMOS process, the proposed reference buffer and the conventional buffer in Fig. 3.3c are designed for comparison. The load capacitors are both 3 pF . The bias currents of M_{11} and M_{31} are both 10 mA. The average power of the level shifter with boosted clocks and the bias is 390 μW . Figure 3.8 shows the simulated transient response. The solid line is the differential reference voltage of the proposed reference buffer. With the same bias current, it settles faster than the conventional buffer in Fig. 3.3c.

Fig. 3.8 Simulated transient response comparison of the proposed reference buffer and the conventional one in Fig. 3.3c with the same bias current (simulated by Spectre)



3.3.1.3 Measurement Results and Comparisons

Reference buffer integrated in a pipelined ADC

A NMOS-only reference buffer with level shifter has been integrated in a 14-bit 150MSps low-power pipelined ADC, described in Fig. 3.9. The ADC includes FSSTAGE and four consecutive 2.5-bit stages. FSSTAGE is a power-efficient stage with opamp and capacitor sharing [8]. It is composed of a 3-bit first stage and a 2.5-bit second stage. The ADC works with three clock phases: sample phase (about 2.5 ns), discharge phase (about 1.1 ns), and amplification phase (about 2.5 ns), as shown in Fig. 3.9b. In Fig. 3.9, stage 1, 3, and 5 work in the amplification phase. The output of the buffer, V_{rn} , drives C_{L1} , C_{L3} and C_{L5} . The total load is 2.63 pF . In the following phase, stage 2, 4, and 6 work in the amplification phase and V_{rn} will drive C_{L2} , C_{L4} and C_{L6} . The total load will be 0.56 pF .

The prototype ADC has been fabricated in a standard 0.13- μm 1P6M mixed-signal CMOS process. Fig. 3.10 presents its chip micrograph. The total area including pads is 4.4 mm^2 and the reference buffer occupies 0.15 mm^2 .

Measurement

To verify the performance of the proposed reference buffer, the power spectrum density of the ADC is measured. It is well known that an ADC core is composed of the SHA and the quantizer, and the reference buffer only drives the quantizer. No matter the input frequency is low or high, the quantizer always processes the frozen signal from the SHA. In other words, the performance of the reference buffer is independent of the input frequency. Therefore, the measurement of the ADC at full conversion speed and low input frequency can be used to verify the reference buffer, avoiding the degradation of the ADC performance due to the high frequency of the input signal.

The measured spectrum with the differential input signal of 2.4 MHz and $2 V_{p-p}$ is shown in Fig. 3.11. The SNDR is 71.3 dB and the SFDR is 93.6 dBc, which indicates that the SNDR/SFDR of the proposed buffer's output is higher than 71.3 dB/93.6 dBc. At 150MSps from a 1.3 V supply, the total power consumption is 85 mW (excluding LVDS IO drivers), including 17 mW for the proposed reference buffer.

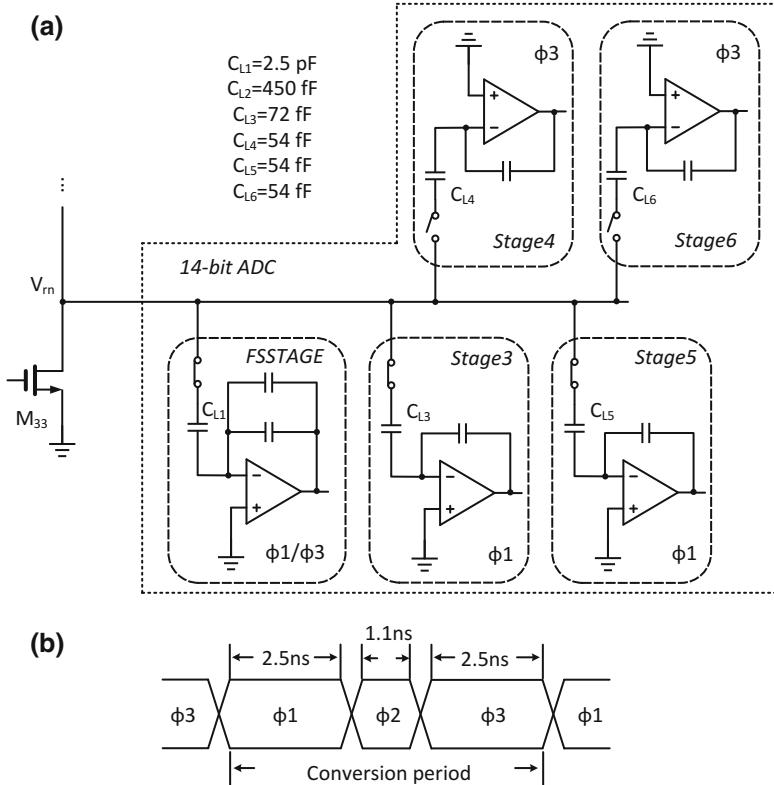


Fig. 3.9 **a** The proposed reference buffer integrated in a 14-bit 150 MSps pipelined ADC (single-ended reference buffer is presented for simplicity), **b** clock timing of the ADC

Table 3.1 shows the comparison with recently published reference buffers in pipelined ADC. Compared with [9], the proposed reference buffer allows the precise settling in a much shorter amplification phase. Compared with [10], the proposed buffer provides better performance and consumes less power.

3.3.1.4 Further Discussion

The advancement of the level-shifter-aided structure in Fig. 3.4 is described in Fig. 3.12. What is different from that in Fig. 3.4 is the push-pull *Buffer Branch*, consisting of M_1 , M_2 , and M_5 . To provide a low enough voltage for the gate of M_2 , a second level shifter is adopted to shift V_{op2} .

Fig. 3.10 The chip micrograph of the proposed reference buffer in a 14-bit 150MSps low-power pipelined ADC

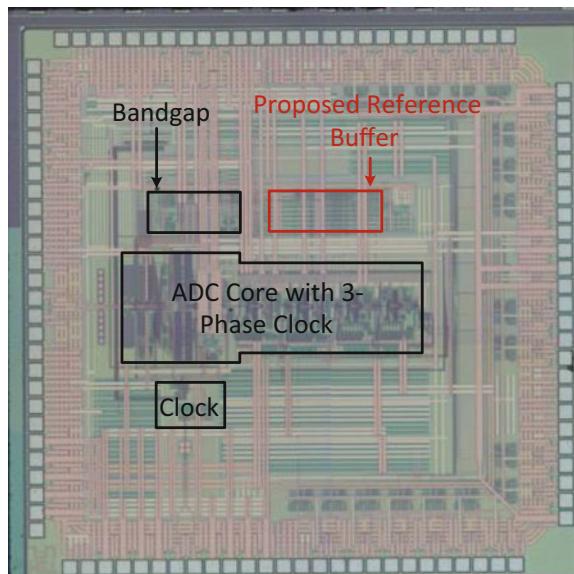


Fig. 3.11 Measured FFT spectrum

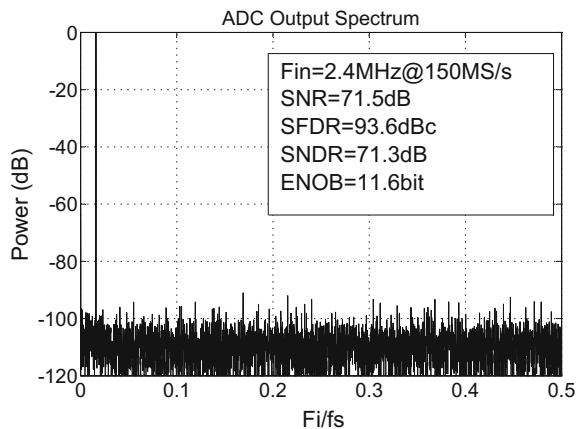


Table 3.1 Comparison of the measured performance

		[9]	[10]	This work
ADC core	Resolution (bit)	14	13	14
	Amplification phase (ns)	8	5	2.5
	SNDR (dB)	76.9	66.4	71.3
	SFDR (dBc)	91.2	80.3	93.6
Ref. buffer	Power (mW)	11	54.6	17

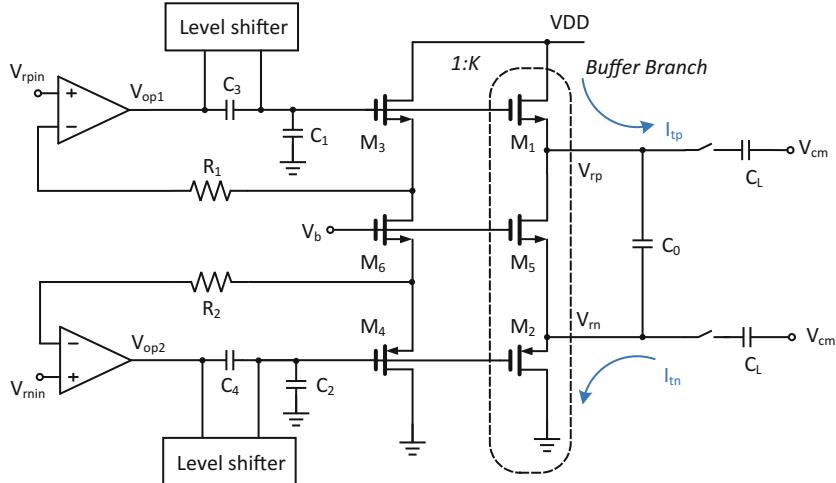


Fig. 3.12 Topology of the push-pull reference buffer

For the buffer *Buffer Branch* in Fig. 3.4, the slew rate is limited by the bias current and can be described as I_B/C_L , where I_B is the bias current and C_L is the capacitive load. For the push-pull buffer *Buffer Branch* in Fig. 3.12, the slew rate depends on the current pushed to or pulled from the output nodes. Taking the note of V_{rn} as an example, if its load attaches to the maximum analog input in the previous sampling phase, the largest current will be pushed to it. Benefit from bias-current-independent slew rate, the settling of V_{rp} and V_{rn} in Fig. 3.12 speed up.

3.3.1.5 Conclusion

A level-shifter-aided CMOS reference buffer with wide swing for high-speed and high-resolution switched-capacitor ADC is proposed. NMOS-only *Buffer Branch* is used to save the power consumption. A level shifter is adopted to increase the output swing. High PSRR is guaranteed by the proposed architecture. Besides, the level-shifter-aided push-pull reference buffer is introduced. The bias-current-independent slew rate saves the response time further.

3.3.2 Charge-Compensation-Based Buffer

A novel charge-compensation-based (CCB) technique for the reference voltage generation of the SC ADC is to be presented in this section. It relaxes power and area requirements for the reference voltage generation by reducing the input-dependent errors of the reference voltage. The circuit implementation of the CCB technique

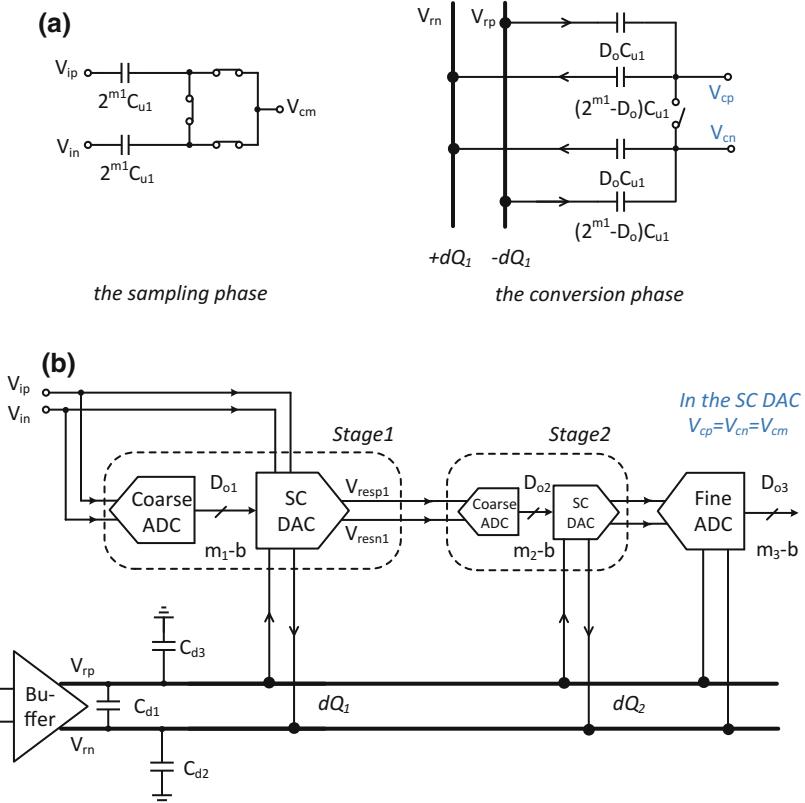


Fig. 3.13 **a** General error model for the reference voltage in a pipelined stage and **b** the SC DAC error model for the reference voltage in a pipelined ADC

consumes no static current and has low overhead on the area. In addition, the CCB technique is specifically applied to a 11-bit 200 MSps ADC for verification.

3.3.2.1 Error Model for the Reference Voltage

The accuracy of the reference voltage suffers from the losing charge caused by the SC circuit, which is to be discussed in a pipelined ADC and a subranging SAR ADC.

1. Error model in the pipelined ADC:

Figure 3.13a shows a general error model for the reference voltage in an m_1 -bit pipelined stage. C_{u1} is the unit sampling capacitor and D_{o1} is the output of the coarse ADC. The bottom plates of the capacitors are connected to the input at the sampling phase and connected to V_{rp} or V_{rn} based on D_{o1} at the conversion phase. The losing charge of V_{rp} is

$$\begin{aligned} dQ_1 = & (V_{rp} - V_{in} - V_{cn} + V_{cm})(2^{m_1} - D_{o1})C_{u1} + \\ & (V_{rp} - V_{ip} - V_{cp} + V_{cm})D_{o1}C_{u1} \end{aligned} \quad (3.13)$$

V_r and V_i are defined as

$$V_r = V_{rp} - V_{cm} = V_{cm} - V_{rn}, \quad V_i = V_{ip} - V_{cm} = V_{cm} - V_{in} \quad (3.14)$$

Therefore,

$$\begin{aligned} dQ_1(V_i) = & V_r C_{u1} 2^{m_1} + V_i C_{u1} (2^{m_1} - 2D_o) + (V_{cm} - V_{cp}) C_{u1} D_o + \\ & (V_{cm} - V_{cn}) C_{u1} (2^{m_1} - D_{o1}) \end{aligned} \quad (3.15)$$

The losing charge of V_{rn} is $-dQ_1$. The charge of dQ_1 transfers from V_{rp} to V_{rn} in the conversion phase, leading to a voltage drop on $V_{rp} - V_{rn}$. The error is input-dependent and results in the nonlinearity of the ADC.

The m_1 -bit CDAC is included by a n -bit ADC driven by a narrow-band reference buffer, which is shown in Fig. 3.13b. C_{d1} , C_{d2} and C_{d3} are on-chip decoupling capacitors. Besides the m_1 -bit stage, the ADC is partitioned by a second m_2 -bit stage 2 and a fine ADC. The unit sampling capacitor of stage 2 is C_{u2} . At the conversion phase, $V_{cp} = V_{cn} = V_{cm}$ and the losing charge caused by stage 1 is

$$dQ_1(V_i) = V_r C_{u1} 2^{m_1} + V_i C_{u1} (2^{m_1} - 2D_{o1}) \quad (3.16)$$

Based on the output of stage 1, the input can be approximated as

$$V_i \approx 2V_r \left(\frac{D_{o1}}{2^{m_1}} - 0.5 \right) \quad (3.17)$$

Therefore,

$$dQ_1(V_i) \approx dQ_1(D_{o1}) = \frac{-4}{2^{m_1}} (D_{o1}^2 - 2^{m_1} D_{o1}) V_r C_{u1} \quad (3.18)$$

$$\varepsilon = dQ_1(V_i) - dQ_1(D_{o1}) \approx 2V_r C_{u1} (2^{m_1} - 2D_{o1}) \left(\frac{D_{o2}}{2^{m_2}} - 0.5 \right) \quad (3.19)$$

which is also labeled as $dQ_1(D_{o1}, D_{o2})$. Additionally, the losing charge caused by stage 2, dQ_2 , can be analyzed similarly.

Taking a 3.5-bit (8 comparators are used and the effective resolution is 3 bit) pipelined stage as an illustration, $dQ_1(V_i)$, $dQ_1(D_{o1})$ and ε are shown in Fig. 3.14. In Fig. 3.14a, the losing charge is symmetrical about $D_{o1} = 4$, and is monotonic for every D_{o1} . The relationship between the losing charge and the coarse conver-

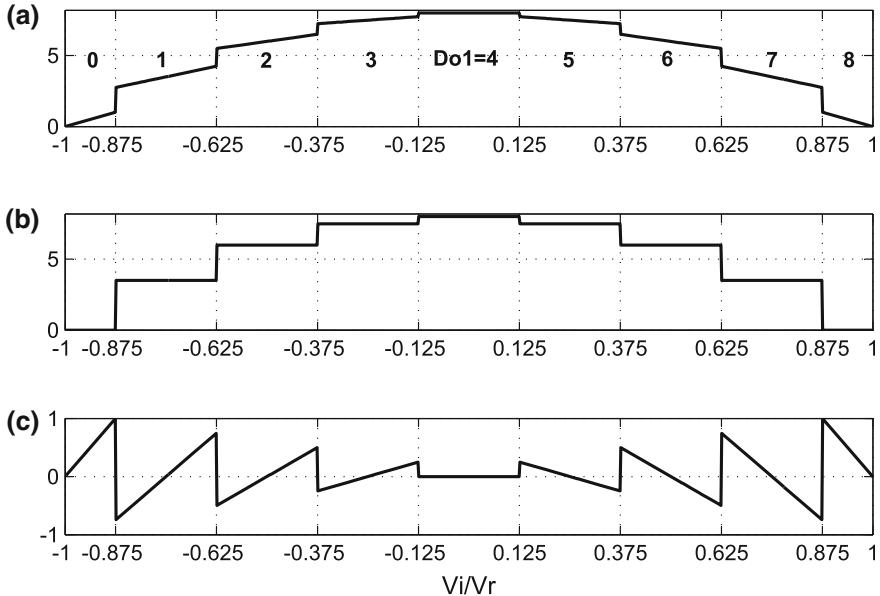


Fig. 3.14 Losing charge caused by a 3.5-bit pipelined stage ($2^{m_1} = 8$). **a** $dQ_1(V_i)/(C_{u1} V_r)$, **b** $dQ_1(D_{o1})/(C_{u1} V_r)$ and **c** $\epsilon/(C_{u1} V_r)$ ($\approx dQ_1(D_{o1}, D_{o2})/(C_{u1} V_r)$) (simulated by MATLAB)

sion results is shown in Fig. 3.14b, and the approximated losing charge is fixed for every D_{o1} . Figure 3.14c is the error caused by the approximation.

2. Error model in the subranging SAR ADC:

Figure 3.15a shows a general error model for the reference voltage in an m_1 -bit subranging SAR stage. C_S is the total sampling capacitance. In the first conversion cycle, the bottom plates of the capacitors attach to V_{rp} and V_{rn} , based on the conversion results of the m_1 -bit coarse ADC. The losing charge of V_{rp} also can be described as Eq. 3.13. At the end of the first conversion cycle, the differential voltages at top plates of capacitors can be derived as

$$V_{cp} = 2V_{cm} - V_{ip} + \frac{D_{o1}C_{u1}V_{rp} + (2^{m_1} - D_o)C_{u1}V_{rn} - 2^{m_1}C_{u1}V_{cm}}{C_S} \quad (3.20)$$

$$V_{cn} = 2V_{cm} - V_{in} + \frac{D_{o1}C_{u1}V_{rn} + (2^{m_1} - D_o)C_{u1}V_{rp} - 2^{m_1}C_{u1}V_{cm}}{C_S} \quad (3.21)$$

Substitute Eq. 3.14 in Eq. 3.20,

$$V_{cp} = V_{cm} - V_i + \frac{2D_{o1}C_{u1}V_r - 2^{m_1}V_rC_u}{C_S} \quad (3.22)$$

Substitute Eq. 3.14 in Eq. 3.21,

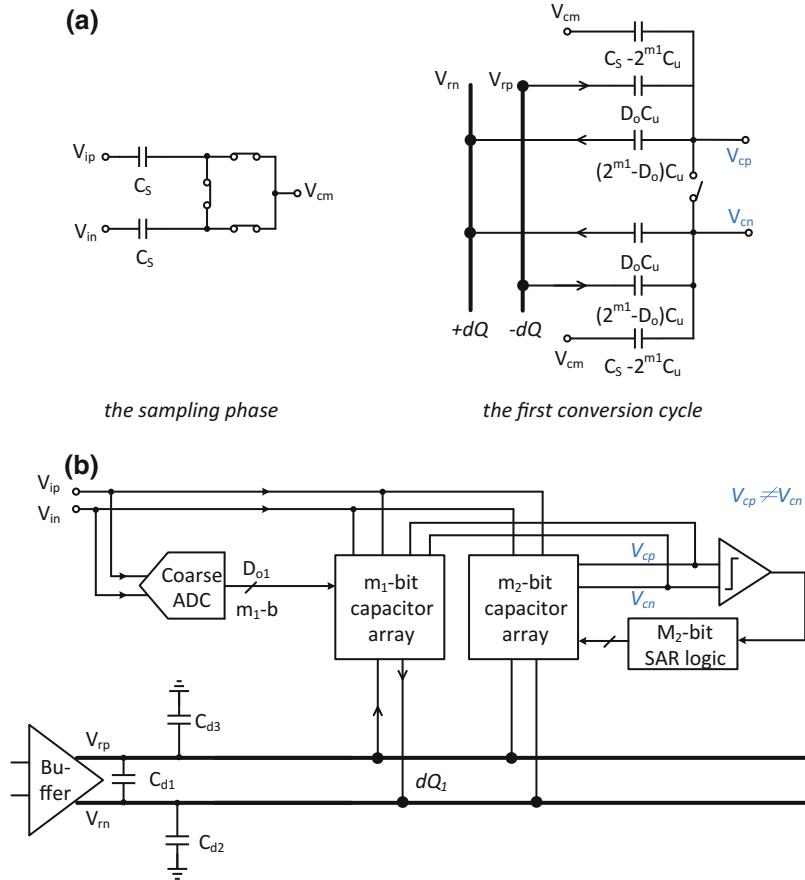


Fig. 3.15 **a** General error model for the reference voltage in a subranging SAR stage and **b** the SC DAC the error model for the reference voltage in a subranging SAR ADC

$$V_{cn} = V_{cm} + V_i - \frac{2D_{o1}C_{u1}V_r - 2^{m_1}V_rC_u}{C_S} \quad (3.23)$$

The losing charge of V_{rp} in Fig. 3.15 can be obtained by substituting Eqs. 3.22 and 3.23 in Eq. 3.15. And it is

$$\frac{dQ_1(D_{o1})}{C_{u1}V_r} = 2^{m_1} - \frac{C_{u1}}{C_S}(2D_{o1} - 2^{m_1})^2 \quad (3.24)$$

Therefore, the losing charge, dQ_1 , depends on the coarse conversion result, D_{o1} , which is different from Eq. 3.16 in the pipelined stage, where the losing charge depends on not only D_{o1} but also V_i .

Taking a 3.5-bit (8 comparators are used and the effective resolution is 3 bit)

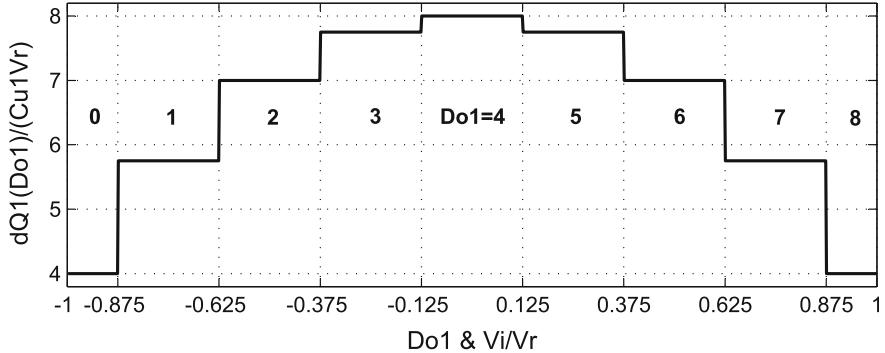


Fig. 3.16 Losing charge caused by a 3.5-bit subranging stage ($2^{m_1} = 8$) (simulated by MATLAB)

subranging stage as an illustration, $dQ_1(D_{o1})/(C_{u1}V_r)$ is shown in Fig. 3.16, where C_{u1}/C_S is 1/16. The losing charge is symmetrical about $D_{o1} = 4$, and it is fixed for every D_{o1} . Different from that in Fig. 3.14a, the losing charge does not depend on the analog input, but the coarse code.

3.3.2.2 Principle of Charge-Compensation-Based Technique

The CCB technique compensates for input-dependent errors of the reference voltage. The key idea behind the compensating is to transfer the constant charge from V_{rp} to V_{rn} for all the input. In addition to the losing charge caused by the SC circuit, the compensated charge of $Q_{comp,i}$ for stage- i is discharged from V_{rp} . Since the error model in the pipelined stage is different from that in the subranging SAR stage, the compensated charges for the two architectures are to be discussed, respectively.

1. Compensated charges in the pipelined ADC:

As mentioned in Eqs. 3.18 and 3.19, since the input signal is converted into the combination of D_{o1} , D_{o2} and so on, the input-dependent losing charge caused by the first stage satisfies

$$dQ_1(Vi) \approx dQ_1(D_{o1}) + dQ_1(D_{o1}, D_{o2}) \quad (3.25)$$

And the corresponding compensated charge is $Q_{comp,11} + Q_{comp,12}$. Conceptually, the sum of the losing charge and the compensated charge is constant, which is

$$dQ_1(Vi) + Q_{comp,11} + Q_{comp,12} \approx \text{constant} \quad (3.26)$$

And,

$$Q_{comp,11} = \begin{cases} \sum_{i=D_{o1}+1}^{2^{m_1}-1} dq_1(i) & 0 \leq D_{o1} < 2^{m_1}-1 \\ \sum_{i=2^{m_1}-D_{o1}+1}^{2^{m_1}-1} dq_1(i) & 2^{m_1}-1 < D_{o1} \leq 2^{m_1} \\ 0 & D_{o1} = 2^{m_1}-1 \end{cases} \quad (3.27)$$

where dq_1 is

$$\begin{aligned} dq_1(i) &= dQ_1(D_{o1})|_{D_{o1}=i} - dQ_1(D_{o1})|_{D_{o1}=i-1} \\ &= \frac{2^{m_1} + 1 - 2i}{2^{m_1-2}} V_r C_{u1}. \end{aligned} \quad (3.28)$$

The comparator offset cannot be neglected in the multi-bit stage. Taking it into account, $dQ_1(D_{o1}, D_{o2})$ mentioned above deviates and is labeled $dQ_1(D_{o1}, D_{o2})'$. As is shown in Fig. 3.17, $dQ_1(D_{o1}, D_{o2})'$ is composed of two parts, which can be described as

$$dQ_1(D_{o1}, D_{o2})' = dQ_1(D_{o1}, D_{o2})'_a + dQ_1(D_{o1}, D_{o2})'_b \quad (3.29)$$

For $D_{o1} = k$ ($k = 0, 1, \dots, 8$),

$$Q_{comp,12} = \begin{cases} k \frac{V_r C_{u1}}{2^{m_2-4}} + \sum_{i=D_{o2}+1}^{2^{m_2}} dq_2(k) & 0 \leq k \leq 2^{m_2}-1 \\ (2^{m_2} - k) \frac{V_r C_{u1}}{2^{m_2-4}} + \sum_{i=D_{o2}+1}^{2^{m_2}} dq_2(k) & 2^{m_2}-1 < k \leq 2^{m_2} \end{cases} \quad (3.30)$$

where $dq_2(k)$ is

$$\begin{aligned} dq_2(k) &= dQ_1(k, D_{o2})|_{D_{o2}=k} - dQ_1(k, D_{o2})|_{D_{o2}=k-1} \\ &= 2V_r C_{u1} (2^{m_1} - 2k) \frac{1}{2^{m_2}}. \end{aligned} \quad (3.31)$$

The ADC with a 3.5-bit first stage and a 3.5-bit second stage is taken as an illustration. If the second stage outputs 4 when $D_{o1} = 2$, the charge of $dq_1(3) + dq_1(4) + V_r C_{u1} + 4dq_2(2)$ is compensated.

2. Compensated charge in the subranging SAR ADC:

In the subranging SAR ADC, the compensated charge satisfies

$$dQ_1(D_{o1}) + Q_{comp,11} = constant \quad (3.32)$$

where $dQ_1(D_{o1})$ and $Q_{comp,11}$ are described in Eqs. 3.24 and 3.27, respectively. Since the losing charge depends on the coarse code, it can be compensated for accurately.

The subranging SAR ADC with a 3.5-bit coarse stage and a second fine stage is

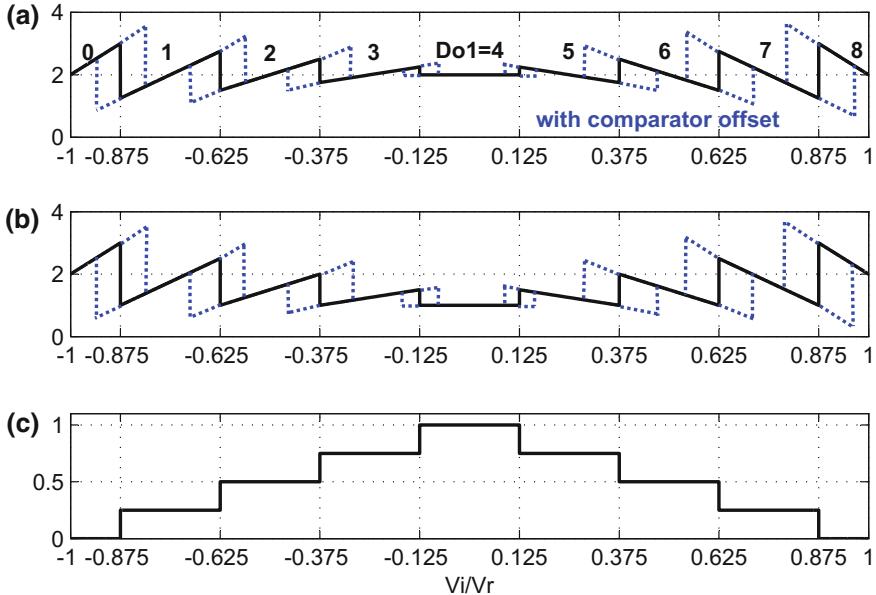


Fig. 3.17 **a** $dQ_1(D_{o1}, D_{o2})'/(C_{u1}V_r)$ ($2^{m_1} = 8, 2^{m_2} = 8$), **b** $dQ_1(D_{o1}, D_{o2})'_a/(C_{u1}V_r)$ and **c** $dQ_1(D_{o1}, D_{o2})'_b/(C_{u1}V_r)$ (simulated by MATLAB)

taken as an illustration. If coarse output is 2, the charge of $dq_1(3) + dq_1(4)$ is compensated to cancel the input-dependent error caused by the 3.5-bit stage.

3.3.2.3 Charge Compensation Unit

The compensated charge is provided by the charge compensation unit (CCU), as is shown in Fig. 3.18. It works with two phases: resetting phase and compensating phase. At the resetting phase, C_i discharges. At the compensating phase, the discharging may happen or not, depending on h_i . If h_i is 0, N_i switches off, resulting in no transferred charge in this period. If h_i is 1, C_i is connected between V_{rp} and V_{rn} . The charge discharged is

$$dq'(i) = (V_{rp} - V_{rn})C_i = 2V_rC_i. \quad (3.33)$$

For $Q_{comp,11}$, $dq_1(i) = dq'(i)$ should be satisfied and

$$C_{i,11} = \frac{2^{m_1} + 1 - 2i}{2^{m_1-1}} C_{u1}. \quad (3.34)$$

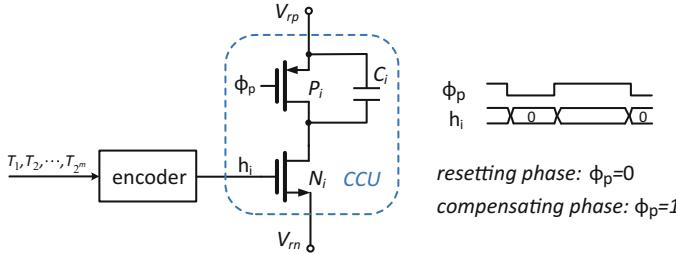


Fig. 3.18 Proposed CCU compensating for m-bit SC ADC and the timing diagram

Table 3.2 Truth table of h_i for $Q_{comp,11}$ ($m_1 = 3$)

D_{o1}	$T_1 T_2 T_3 T_4 T_5 T_6 T_7 T_8$	$h_1 h_2 h_3 h_4$
0	00000000	1111
1	10000000	0111
2	11000000	0011
3	11100000	0001
4	11110000	0000
5	11111000	0001
6	11111100	0011
7	11111110	0111
8	11111111	1111

Besides, the truth table of h_i in the CCU is shown in Table 3.2 (taking $m_1 = 3$ as an example), where T_i is the output of the $i - th$ comparator in the coarse ADC. h_i can be described by

$$h_i = \overline{T_i \overline{T_{2^{m_1}+1-i}}}. \quad (3.35)$$

Based on the analysis above, the CCU consumes no static current and is area-saving.

3.3.2.4 Measurement Result

The CCB technique is verified in an 11-bit 200 MSps subranging SAR ADC fabricated by 65 nm CMOS process. The subranging SAR ADC adopting the CCB technique is shown in Fig. 3.19. The 11-bit resolution is resolved by a 3.5-bit flash ADC and a 8-bit SAR, and the reference voltage is provided by decoupling-capacitor-aided CCB reference voltage buffer. The CCB technique is adopted to compensate for the losing charge caused by the first stage. As for the losing charge caused by the second stage, it is much smaller than dQ_1 because the capacitance in the second stage is reduced sharply, and hence it is neglect. The CCUs are controlled by the outputs

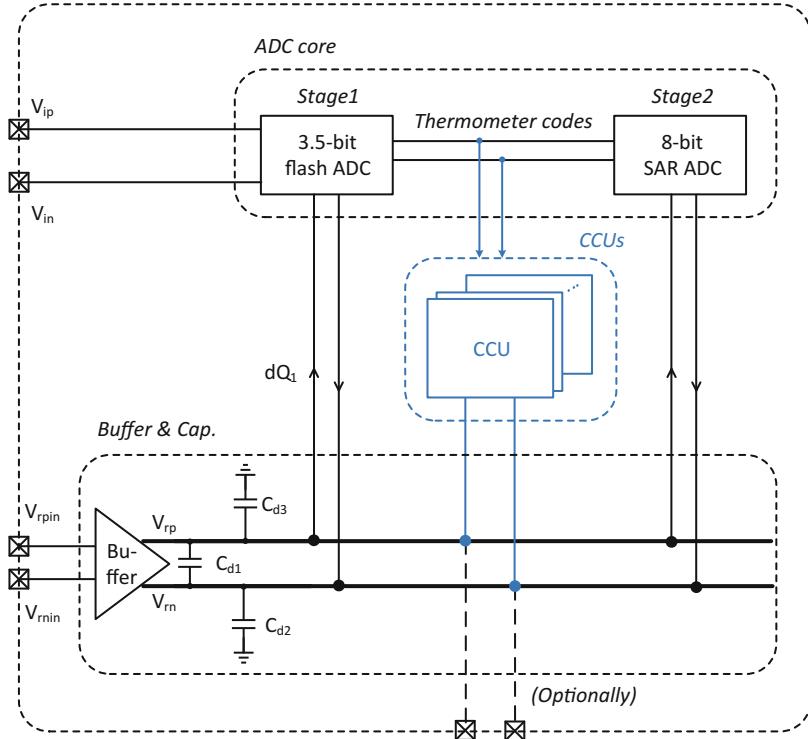


Fig. 3.19 An 11-bit 200 MSps subranging SAR ADC adopting CCB buffer

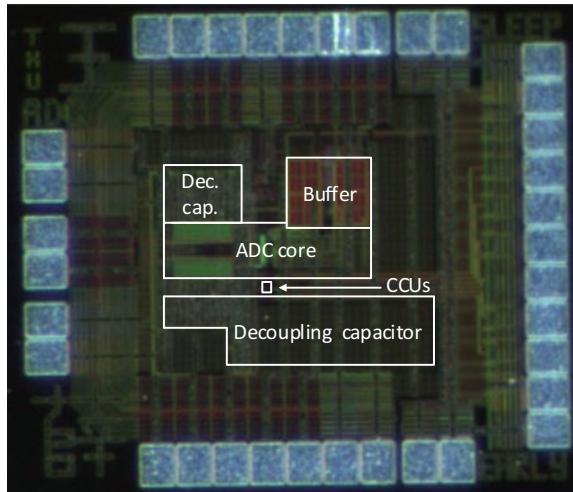
of the flash ADC, and they attach to V_{rp} and V_{rn} . Optionally, the off-chip decoupling capacitor can be connected between V_{rp} and V_{rn} via pads. With the bonding wires, the ADC works in the off-capacitor-aided conversion mode. Removing the bonding wires of V_{rp} and V_{rn} , the ADC works in the fully integrated conversion mode.

Figure 3.20 displays the microphotograph of the ADC, which is composed of the ADC core, the narrow-bandwidth buffer, the decoupling capacitors, and the CCUs. They occupy 0.03, 0.067, and 0.0005 mm^2 , respectively. Thanks to the CCUs, the decoupling capacitance, C_d , is reduced, and C_d/C_s is only 250. The total sampling capacitance, C_s , is 1.28 pF . Besides, C_d is mainly implemented by the oxide capacitor of the MOSFET and metal-oxide-metal capacitor, improving the area efficiency. The full scale differential input swing is 2V. Operating at 200 MSps, the ADC totally consumes 3.91 mW from 1.2 V supply, and the CCUs consume only $95.7 \mu\text{W}$.

1. Fully Integrated Conversion Mode

If bonding wires of V_{rp} and V_{rn} in Fig. 3.19 are removed, the SAR ADC operates in the fully integrated mode. The ADC core operates at 200 MSps, its output is decimated by 2 before being captured by a FPGA evaluation board, and the analog input level is -1 dBFS.

Fig. 3.20 The microphotograph of the ADC



Figures 3.21 and 3.22 show the output spectrums for inputs at 2.4 MHz and 70 MHz. At 2.4 MHz input, the CCB technique improves the SNDR from 50.8 to 59.3 dB, and increases the SFDR from 51.1 to 66.1 dBc. At 70 MHz input, the CCB technique improves the SFDR from 67.4 to 73.7 dBc, and maintains the SNDR of 56.2 dB.

Figure 3.23 plots the SNDR and SFDR versus the input frequency. The conversion rate is 200 MHz. The CCB technique improves the average SNDR from 54.8 dB to 57.8 dB, increases the average SFDR from 60.3 dBc to 67.7 dBc. With the CCB technique, the SNDR/SFDR is 59.5 dB/67.0 dBc at 4.9 MHz input, and the SNDR/SFDR is 56.2 dB/73.4 dBc at 70 MHz input. Besides, with the aid of the CCB technique, the SFDR is improved significantly, and the SNDR is increased only at the low input frequency or near Nyquist input frequency. This is because the input-dependent errors at the low input frequency or the Nyquist frequency are larger than errors at other frequencies, as is shown in Fig. 3.16.

Figure 3.24 plots the INL and DNL errors at 100 MSps. The CCB technique reduces the peak INL error from 2.0 LSB to 1.1 LSB, and decreases the peak DNL error from 0.87 LSB to 0.85 LSB.

2. Off-Capacitor-Aided Conversion Mode

If bonding wires of V_{rp} and V_{rn} in Fig. 3.19 are added, the SAR ADC operates in the off-capacitor-aided mode. In this case, the off-chip decoupling capacitor reduces the impedance of V_{rp} and V_{rn} and increases the driving ability. And hence the SNDR is more than 55 dB from the low frequency to the Nyquist frequency, even without the CCB technique, as shown in Fig. 3.25. That indicates that both the CCB technique and the large decoupling capacitor can improve the accuracy of the reference voltages. Besides, the SFDR is increased by 5-10 dB, which indicates that the CCB technique reduces the bonding wire effect. In other words, the large off-chip capacitor improves the SNDR of the ADC as the CCB technique

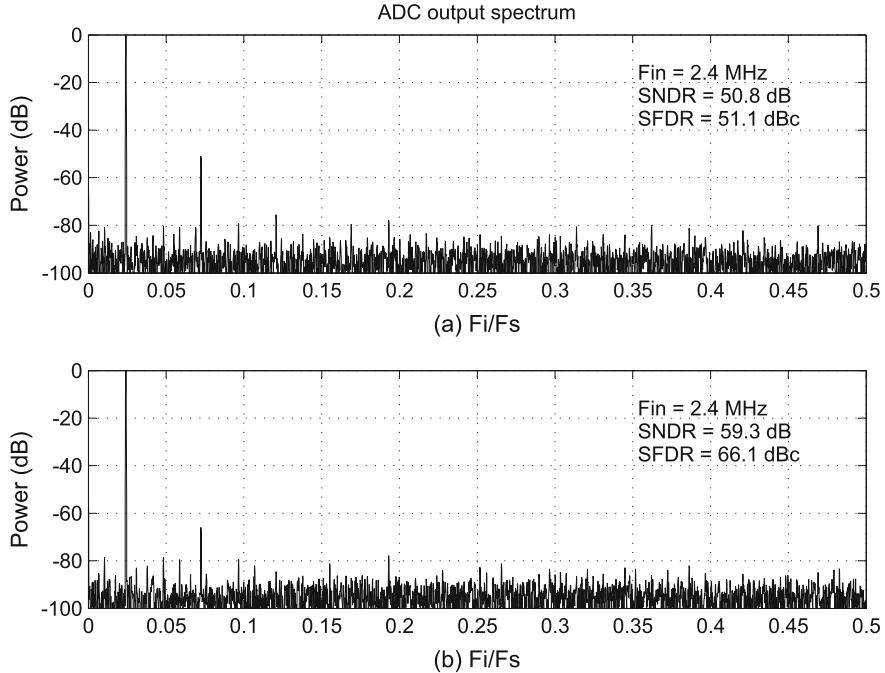


Fig. 3.21 The SNDR and SFDR at 2.4MHz input with/without the CCB technique

does, but the bonding wire effect introduced by the extra pads degrades the SFDR, which can be improved by the CCB technique.

Table 3.3 shows the comparison with recently published SAR ADC. Compared with the ADCs in [11] and [12], with the aid of the CCB technique, this ADC achieves better performance and lower figure of merit (FoM). Compared with the ADC in [13] at 250 MSps, with the aid of the CCB technique, this ADC achieves higher resolution and lower FoM.

3.3.2.5 Conclusions

A CCB technique is proposed to relax the requirements for the on-chip reference voltage generator. Effectively reducing input-dependent errors of the reference voltage, integrated CCB reference generator provides more stable reference voltage without increasing the power dissipation or the decoupling capacitor. Besides, the implementation of the CCB technique consumes no static current. It is a competitive solution to the reference voltage generator of the power-efficient and area-saving SC ADC.

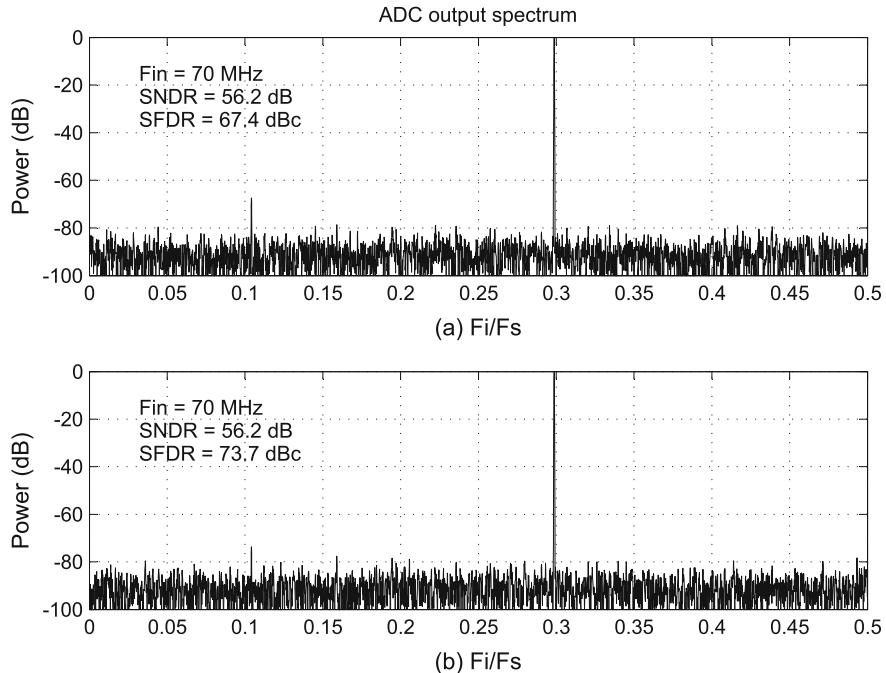


Fig. 3.22 The SNDR and SFDR at 70 MHz input with/without the CCB technique

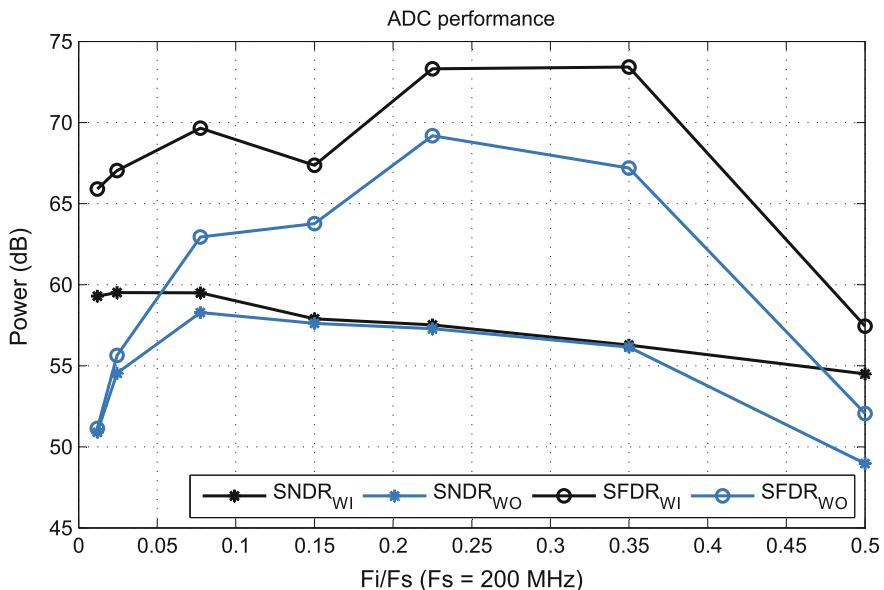


Fig. 3.23 SNDR and SFDR versus the input frequency in the fully integrated mode

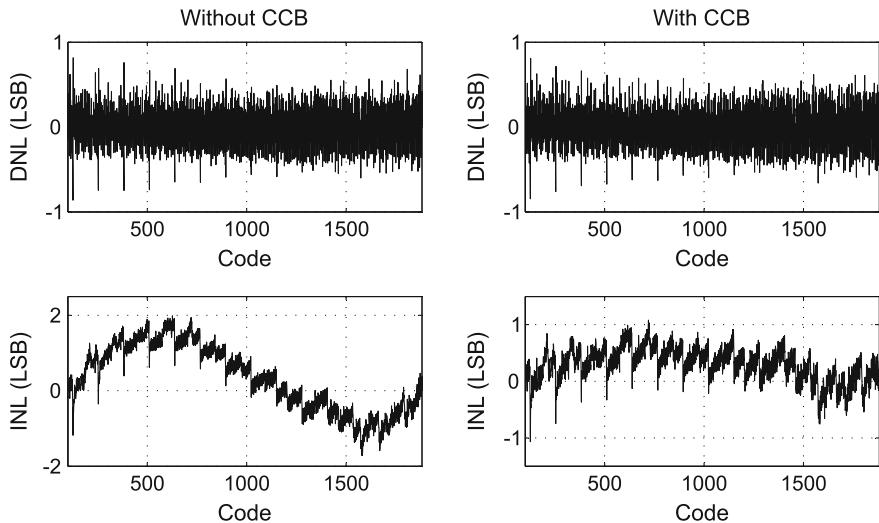


Fig. 3.24 INL and DNL errors in the fully integrated mode

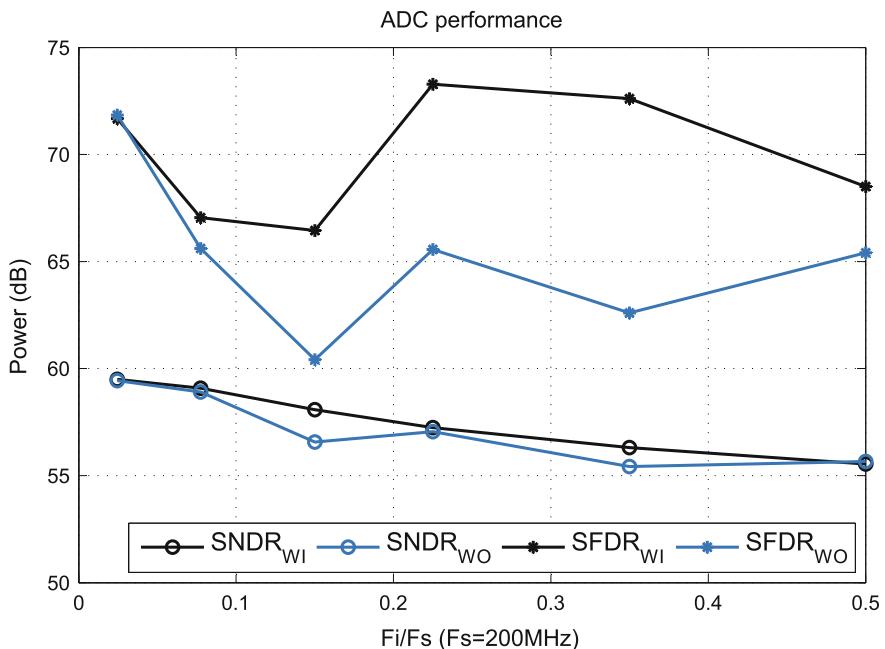


Fig. 3.25 SNDR and SFDR versus the input frequency in the off-capacitor-aided mode

Table 3.3 Comparison of the Measured Performance

	[11]	[12]	[13]	This work
Technology (nm)	90	90	65	65
Resolution (bit)	10	9	8	11
Sample rate (MSps)	160	150	400/250	200
Supply (V)	1	1.2	1.2/1	1.2
Power (mW)	1.97	1.53	4/1.8	3.9
Peak SNDR (dB)	53.1	54.1	44.5 / 46.7	59.5
Area(mm^2)	0.11	0.028	0.024	0.03
FoM(fJ/cov.)	33.5	24.7	73 / 42	25.2

3.4 Summing up

Traditional large-capacitor-aided narrow-bandwidth voltage buffers and fully integrated wide-bandwidth voltage buffers are reviewed. The bonding wire effect, the large power dissipation, the small output swing or the low PSRR limit the ADC performance. Since providing accurate reference voltage for the high performance ADC suffers from those problems, the solutions are discussed in this chapter.

To respond to those, a level-shifter-aided CMOS reference voltage buffer is proposed to enlarge the swing, improve the PSRR, and save the power. Additionally, a charge-compensation-based (CCB) technique is proposed to cancel the input-dependent errors and reduce the decoupling capacitance. Both techniques are verified by the measurement results.

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Chapter 4

Amplification

4.1 Introduction

As discussed in Chap. 2, single-stage ADC is difficult to realize the combination of high conversion rate, high accuracy, and low power. For the multistage noise-limited ADC, in order to achieve high SNR, the residue amplification is normally required to amplify the conversion residue and improve the accuracy. The basic concept of the residue amplification refers to Sect. 2.1.1.2. In the majority of multistage ADCs, close-loop opamp are adopted due to its accurate amplification. However, high-performance opamp is not only power-hungry but also difficult to be implemented with the scaling technology.

The scaled supply voltage and the minimum gate length are shown in Fig. 4.1. As the minimum gate length is reduced from 500 to 16 nm, the power supply voltage is decreased from 5 to 0.8 V. Low power supply leads to the small signal swing, and hence the large capacitor is required to maintain the same SNR. And the large capacitor consumes more current to achieve the same speed. Besides, the decreased output resistance of the scaled device reduces the gain and hence results in the loss of the precision. To address the challenges, many approaches are adopted, including how to relax requirements and effective opamp architectures.

In recent years, power-efficient and process-friendly amplifying circuitry greatly interests designers. The innovative techniques replace static opamps by comparators or open-loop dynamic amplifiers. The three amplification approaches are to be discussed in the next section.

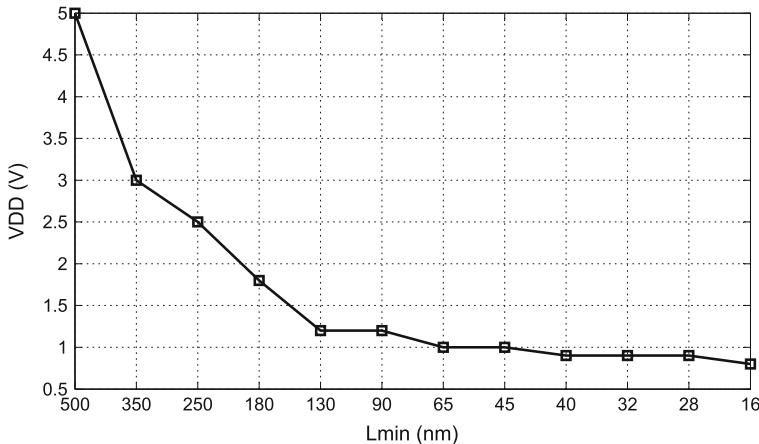


Fig. 4.1 The scaling of the supply voltage and the minimum gate length

4.2 Residue Amplification

4.2.1 Opamp-Based Residue Amplification

For the close-loop residue amplification, the function of the component (the opamp or the comparator) is to enable the fast and complete charge transfer to take place in the amplification phase. The virtual ground condition can be achieved by different approaches. For the opamp-based residue amplification, the virtual ground condition is forced by the opamp in the entire charge transfer phase.

As shown in Fig. 4.2a, in the amplification phase, the summing node, V_X , is forced to the virtual ground so that the charge sampled on C_1 and C_2 can be transferred. V_X and V_o settle at an exponential rate, depicted in Fig. 4.2b. The settling time depends on the time constant of the closed loop. After a number of constant time, both V_X and V_o settle to the steady value and then V_o is sampled by C_L . However, settling at an exponential rate reduces the power efficiency.

4.2.2 Comparator-Based Residue Amplification

Although the virtual ground condition is maintained to transfer charge in continuous time for the opamp-based MDAC, the charge is only sample by the next stage at the sampling instant. In other words, the accurate virtual ground condition is only required at the sampling instant. Therefore, the virtual ground can be detected in discrete time by the comparator [1], which is the basic idea behind the comparator-based amplification.

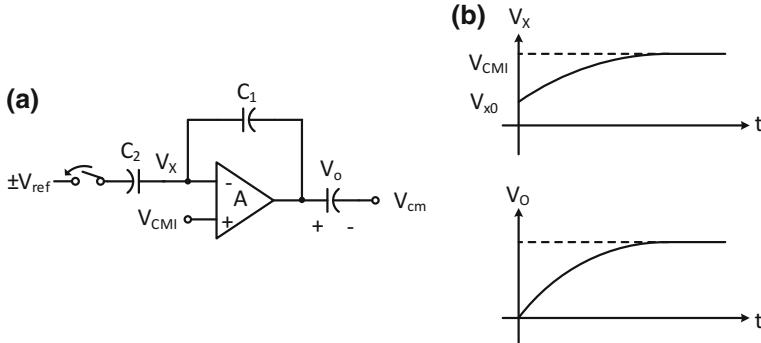


Fig. 4.2 a The opamp-based MDAC and b the settling of the summing node and output

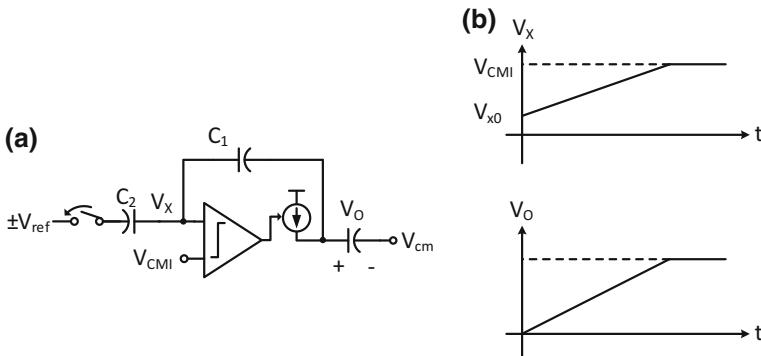


Fig. 4.3 a The comparator-based MDAC and b the settling of the summing node and output

For the comparator-based MDAC, in Fig. 4.3a, a comparator and a current source are adopted [1], replacing the opamp in Fig. 4.2a. Before the amplification phase shown, V_o is shorted to the ground, which is described in Fig. 4.3b. Then the current source turns on, charging capacitors C_1 , C_2 and C_L and resulting in the raise of V_X at a constant rate. Once V_X is over the comparator's threshold, the comparator inverts the output, turns off the current source, and triggers the sampling of the next stage.

The comparator instead of the opamp completes the charge transfer, saving the power. Additionally, the slewing reducing the settling time. And hence the power efficiency is improved. However, the comparator delay leads to the problem of overshoot, and the conversion rate is limited by the linearity and noise [1].

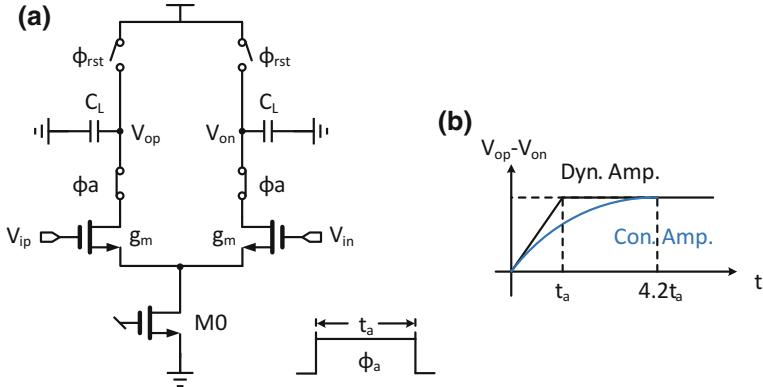


Fig. 4.4 **a** The dynamic amplifier and **b** the settling of the output

4.2.3 Open-Loop Dynamic Amplifier

Open-loop dynamic amplifier settles the output by slewing, replacing the exponential rate in the opamp-based MDAC. And hence the power efficiency is improved. Additionally, the open-loop operation avoids the overshoot in the comparator-based amplification. That helps to increase the accuracy.

A dynamic amplifier is shown in Fig. 4.4a. The interstage gain can be described as

$$G = \frac{g_m}{C_L} t_a \quad (4.1)$$

where g_m is the nonconstant input transconductance, C_L is the capacitive load, and t_a is the slewing time. The settling of the differential output is described in Fig. 4.4b. To achieve the 6-bit accuracy, the settling time of the dynamic amplifier is about a quarter of that of a conventional opamp by consuming the same bias current [2].

The issues accompanying the dynamic amplifier are that the voltage gain is sensitive to PVT variations and clock jitter [2]. Normally, the calibration is required to compensate for the gain instability or to stabilize the amplifier gain over PVT variations.

4.3 Circuit Technique Aided Opamp

Many techniques have been proposed to relax requirements of opamp in the MDAC. Nowadays, most all of pipelined ADCs adopt the stage scaling [3] and optimize the resolution per stage [4]. Additionally, the opamp sharing [5, 6] is attractive due to removing half of the opamps. This section mainly discusses techniques recently widely used and having the potential to design the power-efficient and high-

performance ADC in the scaled CMOS technology, including the correlated level shifting, range scaling, and opamp and capacitor sharing.

4.3.1 Correlated Level Shifting

To authors' best knowledge, the use of the correlated level shifting (CLS) dates back to 1978 and has the potential to relax the requirements of the opamp by one to two orders of the magnitude [7]. To implement the CLS, a level-shifting phase is added as a third step of the traditional 2-phase operation. The error at the opamp's input due to the finite gain is stored on C_{CLS} in the amplification phase and is subtracted in the level-shifting phase to suppress the finite gain effect.

The CLS is modified by operating the corrected level shifting at the output of the opamp in [8], avoiding introducing the parasitics at the opamp's input and doubling capacitors of the MDAC in [7]. The concept of the CLS is illustrated in Fig. 4.5, where C_1 and C_2 , C_p , C_L and C_{CLS} are the sampling capacitors, the parasitics at the opamp's input, the load, and the level-shifting capacitor in the MDAC. And the pipelined stage adopting CLS operates in 3 phases, which are

- sampling phase: sampling the input,
- estimation phase: coarse amplification and storing the output on C_{CLS} ,
- level-shifting phase: fine amplification by the level shifting.

The underlying principle of the technique is that the introduced C_{CLS} stores the coarse amplification result and the related errors that are to be subtracted. As is shown in Fig. 4.5, in the estimation phase, V_{est} is stored on C_{CLS} . Thanks to that, in the following level-shifting phase, the voltage at the opamp's output is $V_{on} - V_{est}$ due to the serial C_{CLS} inside the loop between the opamp and the load.

Based on the discussion above, the benefits from the CLS can be described as follows. First, in order to obtain the accurate output, what the opamp copes with is only the small swing signal, which enables that the MDAC copes with the signal with the rail-to-rail swing. Second, besides errors due to the finite swing, what is subtracted from the output includes the thermal noise, charge injection errors and errors due to the incomplete settling. Third, the loop gain increases in the level-shifting phase and is [8]

$$T_{equ} \approx \frac{T^2}{1 + \lambda} \quad (4.2)$$

where T is the loop gain in the estimation phase and is

$$T = A \frac{C_2}{C_1 + C_2 + C_p} \quad (4.3)$$

where A is the open-loop gain of the opamp. And λ is

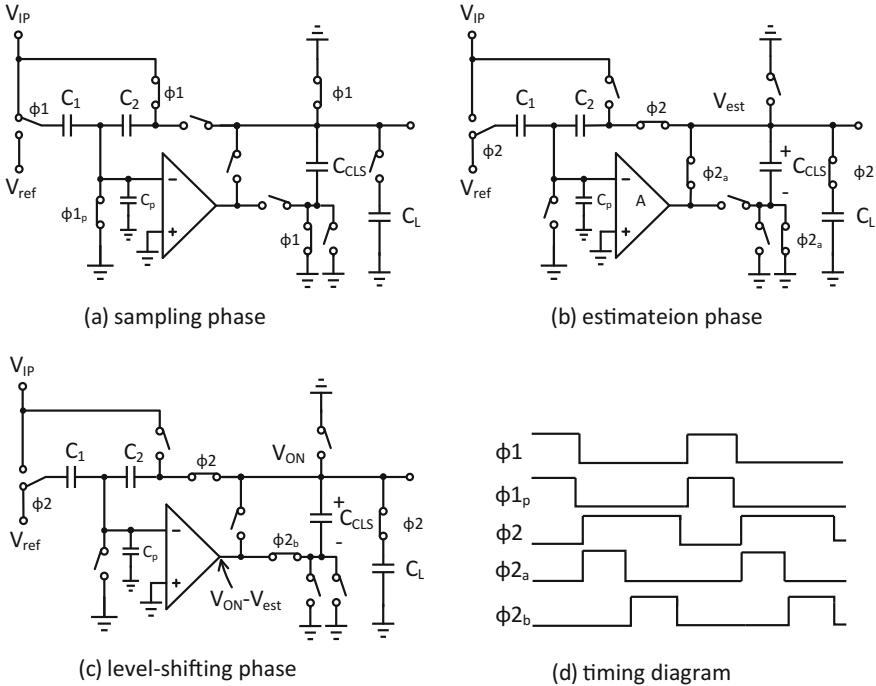


Fig. 4.5 The concept of CLS and the timing

$$\lambda = \frac{1}{C_{CLS}} \left(\frac{C_2(C_1 + C_p)}{C_1 + C_2 + C_p} + C_L \right) \quad (4.4)$$

Consequently, the CLS technique provides the potential to improve the effective resolution of the ADC. From another point of view, to realize the fixed accuracy, the requirements of both the opamp gain and its output swing are relaxed, which saves the power dissipation.

Exact value of C_{CLS} does not required, which is another advantage of this viable technique. The effect of C_{CLS} on the loop gain is illustrated by Eqs. 4.2 and 4.4. In order to increase the loop gain, the large C_{CLS} is expected to minimize λ . On the other hand, to improve the bandwidth, C_{CLS} should be as small as possible. Here is a tradeoff between the accuracy and the speed. If C_{CLS} equals the load of the stage, the loop gain has a loss of 6 dB. And If C_{CLS} equals 1/3 load, the loop gain has a loss of 12 dB. Besides, if C_{CLS} is not large compared with the load, its value weakly influences the opamp noise and distortion [8, 9].

4.3.2 Range Scaling

To relax the requirement of the opamp's output swing, the range scaling is another technique [10, 11]. Take a 2.5-bit individual stage as an example. As shown in Fig. 4.6a, the interstage gain is 4, the output range is $-V_{ref} \sim V_{ref}$ and most of the output falls in $-V_{ref}/2 \sim V_{ref}/2$. If the interstage gain is reduced by 2, as shown in Fig. 4.6b, the output range is decreased to $-V_{ref}/2 \sim V_{ref}/2$ and most of the output only falls in $-V_{ref}/4 \sim V_{ref}/4$. In this case, the required opamp output swing is reduced by half, which is attractive. However, the range scaling suffers from two issues, which are to be discussed.

A problem introduced by the range scaling is that the reference voltage driving the following stage should be scaled down. One solution is generating a compressed reference voltage. However, that introduces a new problem, the mismatch of two reference voltages. Another solution proposed in [11] is scaling the capacitors instead of the reference voltage down.

The residue voltage with the reduced reference voltage can be derived as

$$V_{res} = \frac{C_1 + C_2}{C_2} V_{in} - \frac{C_1}{C_2} \cdot 0.5 V_{ref} \quad (4.5)$$

where C_1 and C_2 refer to Fig. 4.5 and C_p is neglected here. In the sampling phase, C_1 and C_2 are sampling capacitors. In the amplification phase, C_2 is the feedback capacitor and C_1 is the capacitor attaching to the reference voltage.

The residue voltage with the reduced C_1 and the original reference voltage can be derived as

$$V_{res} = \frac{C_1 + C_2}{C_2} V_{in} - \frac{0.5 \cdot C_1}{C_2} V_{ref} \quad (4.6)$$

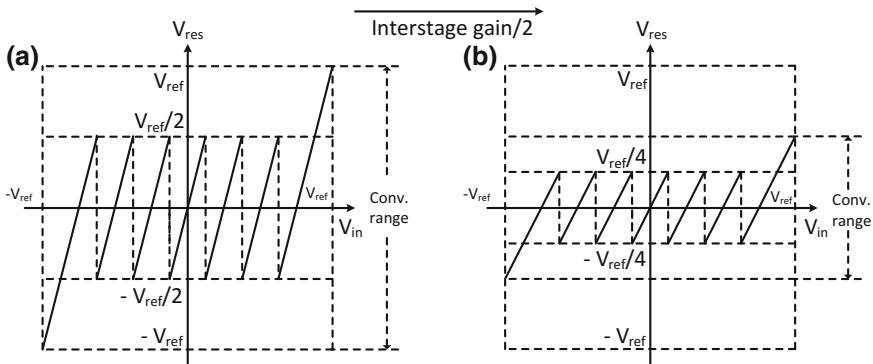


Fig. 4.6 The input/output characteristics of **a** a normal 2.5-bit stage and **b** a 2.5-bit stage adopting the range scaling

In other words, the capacitance attaching to the reference voltage is reduced by half and the sampling capacitance and feedback capacitance are unchanged. Obviously, Eqs. 4.5 and 4.6 are equivalent. What's more, matching capacitors can be provided easily.

A second problem introduced by the technique is the noise requirement of the following stage becomes strict. From the point of view of the sampling noise, in order to realize the accuracy of N-bit, the sampling capacitor, C_s , has to satisfy

$$\frac{KT}{C_s} < \frac{1}{2} \cdot \frac{\Delta^2}{12} \quad (4.7)$$

That is

$$\frac{KT}{C_s} < \frac{1}{2} \cdot \frac{1}{12} \cdot \frac{V_{ref}^2}{2^{2N}} \quad (4.8)$$

With the compressed reference voltage, V_{ref} , the tolerated sampling noise is reduced and hence the sampling capacitor must be enlarged, increasing the load of the previous stage.

Considering a second stage following a 2.5-bit stage, the sampling capacitance in the first stage is C_{s1} and the sampling capacitance in the second stage is C_{s2} . If the interstage gain of the first stage is 4, like that in Fig. 4.6a, C_{s2} is $C_{s1}/16$. If the interstage gain of the first stage is reduced to 2, C_{s2} increases to $C_{s1}/4$. For the first 2.5-bit stage, the larger load will increase the opamp's current. From the point of view of the opamp noise, similar to Eq. 4.8, the tolerated noise in the second stage is also compressed and hence the opamp power dissipation increases.

To sum up, the range scaling relaxes the requirement of the opamp's output swing. On the other hand, the increased load and the extra current compensating for the strict opamp noise requirement in the following stages should be considered.

4.3.3 Opamp and Capacitor Sharing

To save the power dissipation of the opamp, the technique of opamp and capacitor sharing is attractive via reducing the number of the opamp and its load [11, 12].

The concept of the technique is illustrated in Fig. 4.7, where a 3-bit first stage and a 3-bit second stage are merged as a single stage by sharing the opamp and capacitor.

The stage works with three clock phases: sample/amplification (S/A) phase, discharge phase, and amplification/sample (A/S) phase. The clock timing diagram is shown in Fig. 4.7d. The S/A phase means that the first/second stage works in sampling/amplification phase, and vice versa. The details on the operation are described as follows.

- During the S/A phase (ϕ_1), in Fig. 4.7a, the input signal $V_i(n)$ is sampled by the first MDAC (labeled MDAC1) and the 3-bit flash ADC (labeled ADC1) at t_n .

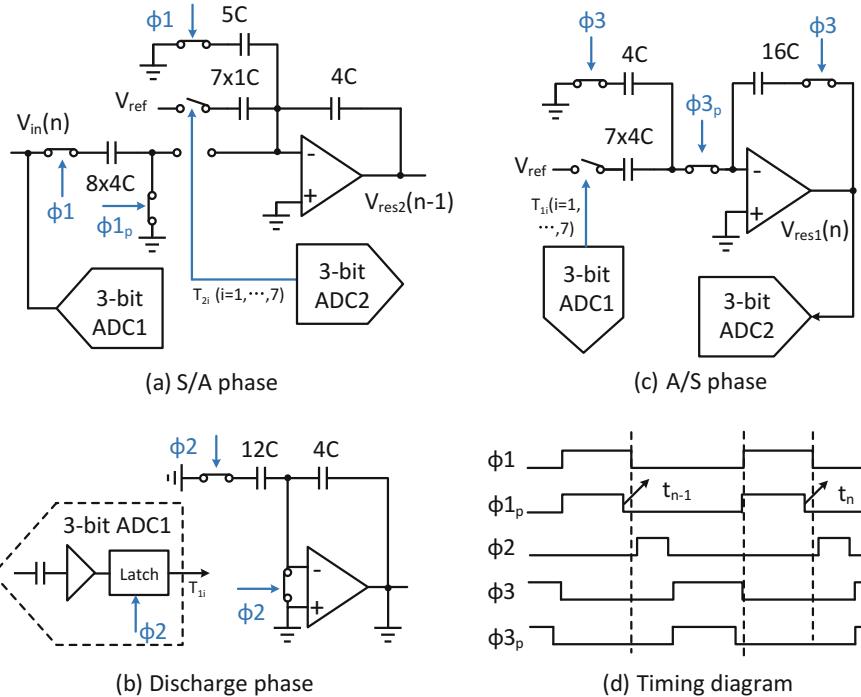


Fig. 4.7 The concept of the opamp and capacitor sharing

The sampling capacitor is labeled as $8 \times 4C$, which means eight $4C$ capacitors in parallel. And at the same time, the sample at t_{n-1} is amplified by the second MDAC (labeled MDAC2), which outputs the residue voltage $V_{o2}(n-1)$ to the third stage. The capacitor labeled as $7 \times 1C$ means seven $1C$ capacitors in parallel. $V_{res2}(n-1)$ can be derived as

$$V_{res2}(n-1) = 4V_{res1}(n-1) - \frac{1}{2} \sum_{i=1}^7 T_{2i} \frac{V_{ref}}{2} \quad (4.9)$$

where $V_{res1}(n-1)$ is the residue voltage of MDAC1 for the sample at t_{n-1} and sampled by the shared capacitor 16C. T_{2i} ($i=1$ to 7) are the thermometer code of the second 3-bit flash ADC (labeled ADC2). T_{2i} equals either 1 or -1. The gain of MDAC2 is 4 as expected.

- During the discharge phase (ϕ_2), in Fig. 4.7b, the terminals of the opamp and capacitors $12C$ and $4C$ are connected to AC ground to eliminate the memory effect. At the same time, the 3-bit ADC1 obtains the voltage differences between the sampled input and thresholds, then amplifies them, and finally latches at the falling edge of ϕ_2 .

- During the A/S phase (ϕ_3), in Fig. 4.7c, the bottom plate of the capacitor $8 \times 4C$ is equally decomposed into eight individual terminals. Seven terminals of them connect to $+V_{ref}$ or $-V_{ref}$, controlled by the output of ADC1. The shared capacitors, $16C$, work as the feedback capacitor of MDAC1. The residue voltage of MDAC1, $V_{o1}(n)$, for the sample at time t_n , is

$$V_{res1}(n) = 2V_i(n) - \frac{1}{4} \sum_{i=1}^7 T_{li} V_{ref} \quad (4.10)$$

where T_{li} ($i=1$ to 7) are the thermometer code outputs of the 3-bit ADC1. T_{li} is equal to either 1 or -1. The gain of MDAC1 is 2 as expected. $V_{o1}(n)$ is sampled on the $16C$ feedback capacitor due to the virtual short circuit of input terminals of the opamp. So the charge on the $16C$ feedback capacitor is reused for MDAC2 instead of being thrown away.

Besides the saved power dissipation, the technique has the potential to eliminate the finite gain error. The MDAC1 and the MDAC2 in the amplification phase are illustrated in Fig. 4.8. They share one unique opamp, whose DC gain is A and input parasitic capacitor is C_p .

Considering the MDAC1 in the amplification phase, as shown in Fig. 4.8a, due to the finite gain, V_{n1} at the inverting input is

$$V_{n1} = -\frac{V_{res1}}{A} \quad (4.11)$$

MDAC1 samples the charge of $32C \cdot V_{in}$ in its sampling phase, as is shown in Fig. 4.7a. Based on the principle of charge conservation, the charge of MDAC1 in the amplification phase is still $32C \cdot V_{in}$, which can be described as

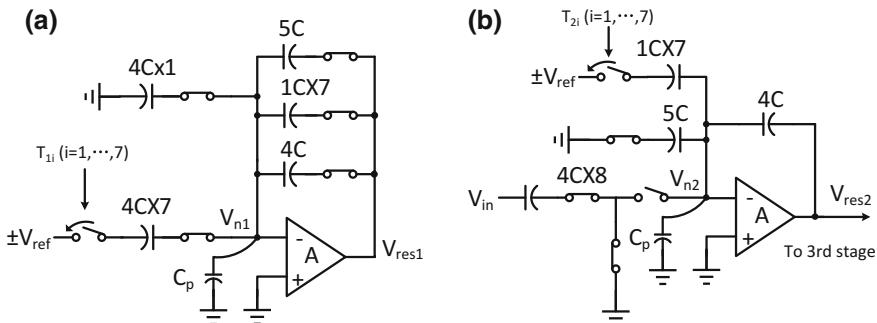


Fig. 4.8 a the MDAC1 and b the MDAC2 in the amplification phase

$$\sum_{i=1}^7 4C(V_{n1} - T_{li} V_{ref}) + 16C(V_{n1} - V_{res1}) + C_p V_{n1} + 4CV_{n1} = -32CV_{in} \quad (4.12)$$

And hence V_{res1} is

$$V_{res1} \approx (2V_{in} - \frac{1}{4} \sum_{i=1}^7 T_{li} V_{ref})(1 - \frac{3 + \frac{C_p}{16C}}{A}) \quad (4.13)$$

Because of the capacitor sharing, the charge on shared capacitors is also the charge sampled by the MDAC2 and it is

$$Q_{2t} = 16C(V_{n1} - V_{res1}) + C_p V_{n1} = -16CV_{res1}(1 + \frac{1 + \frac{C_p}{16C}}{A}) \quad (4.14)$$

Substitute Eq. 4.13 in Eq. 4.14, and

$$Q_{2t} \approx -16C(2V_{in} - \frac{1}{4} \sum_{i=1}^7 T_{li} V_{ref})(1 - \frac{3 + \frac{C_p}{16C}}{A})(1 + \frac{1 + \frac{C_p}{16C}}{A}) \quad (4.15)$$

It can be simplified as

$$Q_{2t} \approx -16C(2V_{in} - \frac{1}{4} \sum_{i=1}^7 T_{li} V_{ref})(1 - \frac{2}{A}) \quad (4.16)$$

For the comparison, the charge sampled by the second stage in a traditional ADC, composed of a 3-bit first stage, a 3-bit second stage, and the backend ADC, is also derived. The ideal residue of the 3-bit stage is

$$V'_{res1} = 4V_{in} - \frac{1}{2} \sum_{i=1}^7 T_{li} V_{ref} \quad (4.17)$$

And the charge sampled by the second stage can be derived as

$$Q'_{2t} \approx -8CV'_{res1}(1 - \frac{4 + \frac{C_p}{8C}}{A}) \quad (4.18)$$

Besides, according to Eqs. 4.16 and 4.17, Q_{2t} can be expressed by V'_{res1} as

$$Q_{2t} \approx -8CV'_{res1}(1 - \frac{2}{A}) \quad (4.19)$$

Comparing the charge sampled by the second stage in Eqs. 4.18 and 4.19, benefit from the opamp and capacitor sharing, the finite gain error is reduced by more than 50%.

Similarly, the charge sampled by the third stage can be derived. As shown in Fig. 4.8b, V_{n2} at the inverting input is

$$V_{n2} = -\frac{V_{res2}}{A} \quad (4.20)$$

Based on the principle of charge conservation, the following equation is obtained.

$$C_p V_{n2} + 5CV_{n2} + \sum_{i=1}^7 C(V_{n2} - T_{2i} V_{ref}) + 4C(V_{n2} - V_{res2}) = Q_{2t} \quad (4.21)$$

Substitute Eq. 4.20 in Eq. 4.21, and V_{res2} is simplified as

$$V_{res2} \approx \left(-\frac{Q_{2t}}{4C} - \frac{1}{4} \sum_{i=1}^7 T_{2i} V_{ref} \right) \left(1 - \frac{4 + \frac{C_p}{4C}}{A} \right) \quad (4.22)$$

Without shared capacitors between the second and third stages, the charge sampled by the third stage is

$$Q_{3t} = C_{3t} V_{res2} \quad (4.23)$$

which is the same as that in the traditional ADC. The technique does not change the finite gain effect in the second stage.

The benefit of the opamp and capacitor sharing is summarized as follows. First, adopting the technique in the first and second stages compresses the finite gain error in the first stage and does not change that error in the second stage. Second, since 3 bits are resolved by the first stage, requirements for the opamp in the two stages are different and requirements of the first stage are much stricter. Benefit from the technique, the finite gain error is reduced in the first stage, which is helpful to relax requirements of the shared opamp. Third, from another point of view, if the opamp gain is unchanged, the accuracy of the conversion can be improved by using the technique.

To verify the opamp and capacitor sharing, the ADC performance is simulated with or without the technique, as shown in Table 4.1. The DC gain is swept from 50 to 80 dB and the SNDR and SFDR are calculated. With the aid of the technique, SNDR/SFDR is improved by 7/13 dB at least. On the other hand, the requirement of the opamp gain is relaxed by about 10 dB to realize the same performance.

Table 4.1 ADC performance with or without the opamp and capacitor sharing

DC gain (dB)	SNDR(dB) / SFDR(dBc) in a traditional stage	SNDR(dB) / SFDR(dBc) with the opamp and capacitor sharing
50	53.2/55.4	62.9/71.9
60	62.9/68.7	72.6/81.7
70	72.7/74.9	81.8/91.6
80	82.2/84.6	89.2/98.5

4.4 Opamp Design

4.4.1 Traditional Opamp

Opamps usually adopted by ADCs include single-stage opamps and multistage ones, such as the telescopic opamp, the folded cascode opamp, the symmetrical opamp, Miller opamp, and so on. The details related are discussed in [13, 14]. Based on the principle of the telescopic and folded cascode opamp, a hybrid opamp is proposed.

4.4.2 Hybrid Opamp

The hybrid opamp is presented in Fig. 4.9. M1~4 attach to inputs and they quarter the total current of $2I$. The input transconductance of V_{ip} and V_{in} are equal and labeled $2G_m$. M10~13 attach to outputs, driving the load C_L and the parasitic capacitor C_p .

The DC gain of the hybrid opamp can be derived as

$$A_h = 2G_m[R_{ds3}G_{m12}R_{ds12}/(R_{ds8}/R_{ds1}G_{m14}R_{ds14})G_{m10}R_{ds10}] \quad (4.24)$$

which can be simplified as

$$A_h \approx 2G_m(R_{ds3}G_{m12}R_{ds12}/R_{ds8}G_{m10}R_{ds10}) \quad (4.25)$$

For the further simplification, $R_{ds8}G_{m10}R_{ds10}$ is labeled R_O . Since the current of M3 is half of that of M8, $R_{ds3}G_{m12}R_{ds12}$ is approximately $2R_O$. And thereby

$$A_h \approx 2G_m(2R_O/R_O) = 4G_mR_O/3 \quad (4.26)$$

Besides, the gain-bandwidth product is

$$GBW_h = \frac{2G_m}{C_L + C_p} \quad (4.27)$$

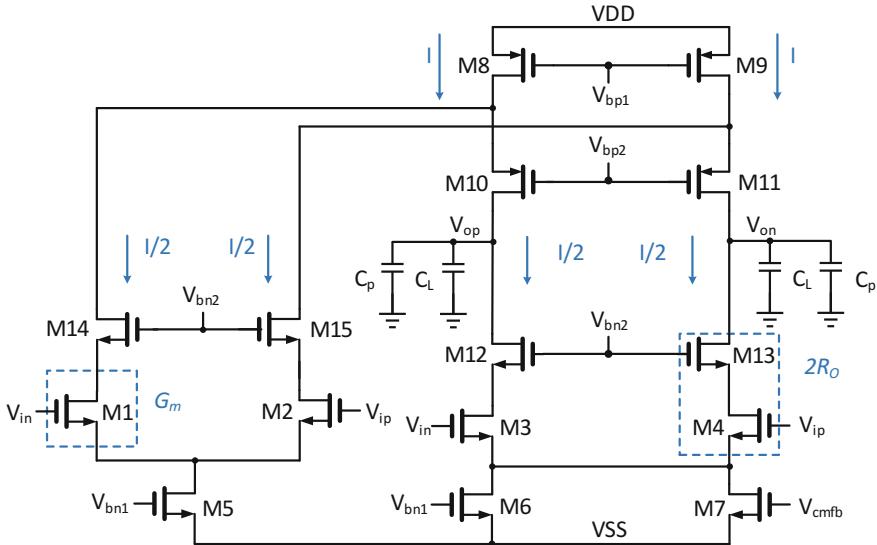


Fig. 4.9 The hybrid opamp

where C_p is composed of the gate-drain capacitors and bulk-drain capacitors of M10~13, and

$$C_p = k(W_{10} + W_{12}) \quad (4.28)$$

where k is constant and the capacitance is determined by the size of M10~13.

The architecture in Fig. 4.9 is the combination of the telescopic and folded cascode opamp. If M1, M2, M5, M14, and M15 are removed, a conventional telescopic opamp is obtained, as in shown in Fig. 4.10a. Assuming that the telescopic opamp consumes the identical current, $2I$, the size of M10~13 should be doubled and hence the parasitic capacitor of the output is correspondingly $2C_p$. The gain is

$$A_t = 2G_m(R_{ds3}G_{m12}R_{ds12}/R_{ds8}G_{m10}R_{ds10}) \quad (4.29)$$

Based on the relationship between the current and the resistance, $R_{ds3}G_{m12}R_{ds12}$ is R_O and A_t is simplified as

$$A_t = 2G_m(R_O//R_O) = G_m R_O \quad (4.30)$$

Its gain-bandwidth product is

$$GBW_t = \frac{2G_m}{C_L + 2C_p} \quad (4.31)$$

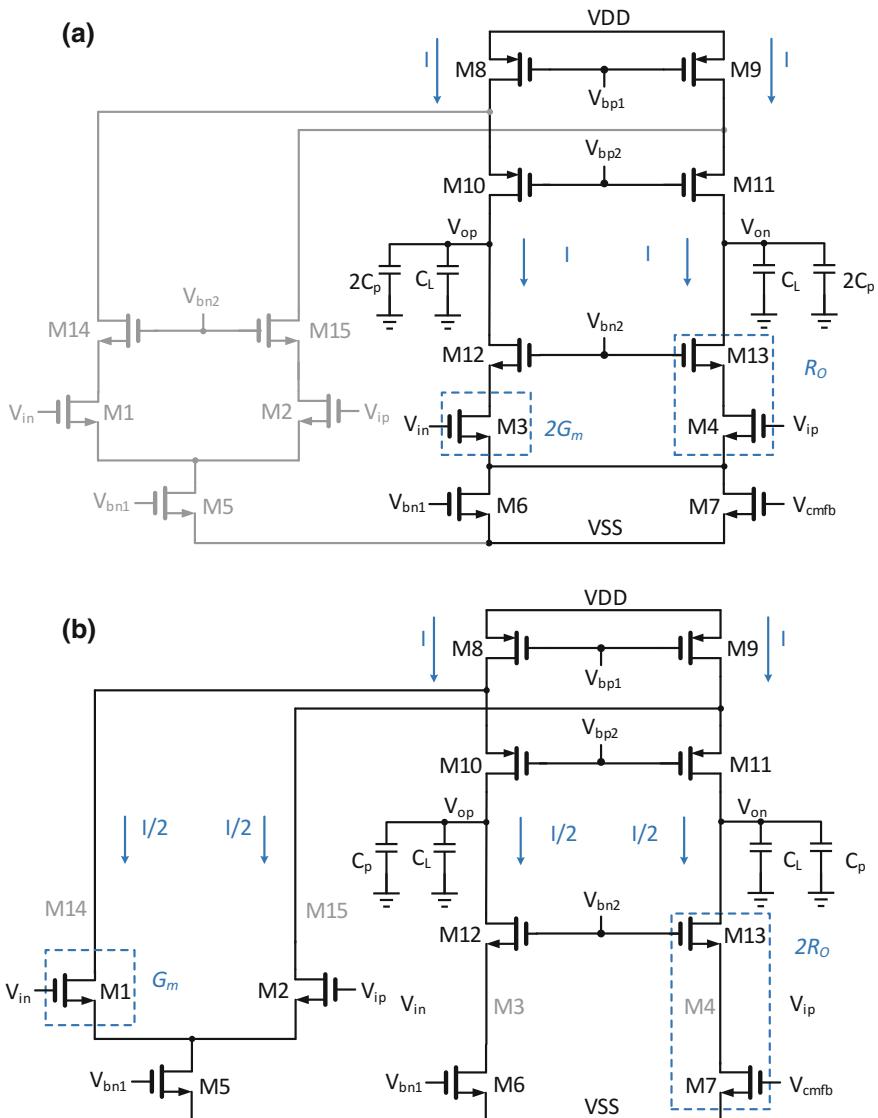


Fig. 4.10 The **a** telescopic and **b** folded cascode opamp from the hybrid opamp

If M3, M4, M14, and M15 are removed, a folded cascode opamp is obtained in Fig. 4.10b. For the folded cascode opamp consuming the current of $2I$, its input transconductance is only G_m due to removing half of the inputs. And the gain is

$$A_f = G_m [R_{ds6}G_{m12}R_{ds12}/(R_{ds8}/R_{ds1})G_{m10}R_{ds10}] \quad (4.32)$$

Based on the relationship between the current and the resistance, $R_{ds6}G_{m12}R_{ds12}$ is $2R_O$, $R_{ds8}G_{m10}R_{ds10}$ is R_O , and $R_{ds1}G_{m10}R_{ds10}$ is $2R_O$. Therefore,

$$A_f = G_m (2R_O/(2R_O/R_O)) = G_m R_O/2 \quad (4.33)$$

Besides,

$$GBW_f = \frac{G_m}{C_L + C_p} \quad (4.34)$$

Table 4.2 summarizes the performance of three opamps. For a fair comparison, they all consume the current of $2I$ and drive the load of C_L . The size of the transistors attaching to the output node is usually large to increase the transconductance or the output impedance or the output swing. And thereby the parasitic capacitance at the output node is usually large. Therefore, assume that

$$C_p = C_L \quad (4.35)$$

Based on the comparison in Table 4.2, the following conclusion can be obtained. By consuming the same current, compared with the telescopic opamp,

1. The gain of the hybrid opamp is increased by about 2.5 dB.
2. The GBW of the hybrid is improved by about 3.5 dB.

In addition, compared with the folded cascode opamp,

1. The gain of the hybrid opamp is increased by about 8.5 dB.
2. The GBW of the hybrid is improved by about 6 dB.

Therefore, the hybrid opamp is competitive in the high-performance and low-power ADC.

Table 4.2 Comparison of opamps

	A	GBW
Telescopic opamp	$G_m R_O$	$2G_m/(C_L + 2C_p)$
Folded cascode opamp	$G_m R_O/2$	$G_m/(C_L + C_p)$
Hybrid opamp	$4G_m R_O/3$	$2G_m/(C_L + C_p)$

4.5 Summing up

The advanced CMOS process brings in a big challenge of implementing the high-performance and power-efficient opamp. As the minimum gate length is reduced to 16 nm, the power supply voltage is only 0.8 V. Low power supply leads to the small signal swing and hence the large capacitor is required to maintain the same SNR. And the large capacitor consumes more current to achieve the same speed. Besides, the lower output resistance of the scaled device reduces the gain and hence results in the loss of the precision. Since opamp plays an important role in the residue amplification, it is difficult to achieve accurate amplification.

To address the challenges, two categories of solutions are presented in this chapter. First, the opamp-based amplification is replaced by the comparator-based amplification or open-loop dynamic amplifier. Second, the circuit techniques that assist in relaxing the requirements of the opamp and improving the opamp performance are introduced.

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Chapter 5

Comparator

5.1 Introduction

As the name implies, the comparator is used to compare two voltages. If one input is higher than the other, the output is one state, and the output switches, if the inputs are reversed. It is the fundamental circuit to convert the analog signal to the digital one and of importance to implement an ADC.

There are two types of comparator widely used, the opamp-type comparator and the latch-type one. The opamp-type comparator uses the opamp either in the positive feedback or no feedback at all to drive the output into saturation and the output appears to be either the maximum or the minimum. Its input/output characteristics is illustrated in Fig. 5.1a. The slope of the characteristics around $V_{id} = 0$ is the gain of the opamp (A_V), which enables it to deal with extremely small inputs (V_H/A_V). Therefore, the speed of its switching is limited by the bandwidth (when the signal swing is small) and the slew rate (when the signal swing approaches the desired value) of the opamp and hence directly proportional to the power dissipation. The latch-type comparator is triggered by the clock and operates in the discrete time. Because the transistors operate in the switching mode, the latch-type comparator provides a fast response speed and the high power efficiency. The input/output characteristics of an ideal comparator is illustrated in Fig. 5.1b, indicating an abrupt transition around $V_{id} = 0$. Comparing with the opamp-type comparator, the latch-type one is attractive to the high-performance and power-efficient ADC. Therefore, details of the latch-type comparator is to be discussed in the chapter.

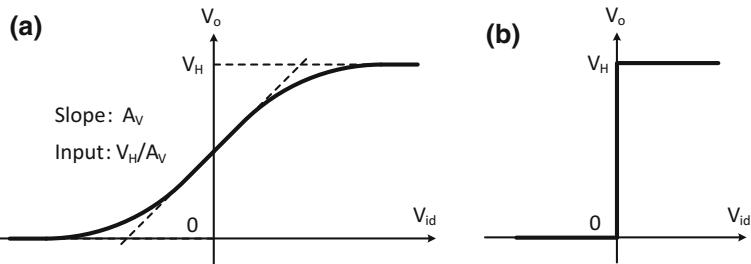


Fig. 5.1 The input/output characteristics of **a** opamp-type comparator and **b** the latch-type one

5.2 Circuit-Technique-Aided Comparator

The comparators to be discussed are prepared for an ADC and hence the requirements can be relaxed via techniques in the architecture level, to reduce the complexity of the circuit design. In this section, we discuss the redundancy technique, which can relax the requirement of the comparator offset. Besides, the reference voltage stabilization techniques are to be presented, and they are helpful to relax the requirement of the kickback noise.

5.2.1 Redundancy Technique

For the flash-based ADC, the comparator offset can be tolerated by adopting redundant decision levels. Based on the discussion in Sect. 2.2.3.1, for a $(m+1)$ -bit or $(m+0.5)$ -bit individual stage with the unique error source of the comparator's offset, the offset of $\pm V_{FS}/2^{m+2}$ can be tolerated by the of 1-bit or 0.5-bit redundancy. And V_{FS} is the full scale of the input. Here is a practical problem in the design. Although a large correction range is provided by the redundancy, it is actually used to tolerate not only the comparator's offset but also other nonideal factors, including the interstage gain's error, the aperture error in the SHA-less architecture (Sect. 2.2.1), the mismatch between the reference voltage of the sub-ADC and the MDAC, the reference voltage fluctuation and so on. The input/output characteristics in Fig. 5.2 is used as an example to illustrate the effect of those errors. It is for a 2-bit stage with 1-bit redundancy. The increased interstage gain results in the enlarged residue range in Fig. 5.2a. If the sampled voltage of the MDAC is larger than that of the flash ADC due to the aperture error, decision levels all move right and hence the residue raises in Fig. 5.2b. If the reference voltage of the flash ADC is larger than that of the MDAC, the left decision level moves left, the right one moves right, and the middle one keeps the same. And thereby the residue range increases in Fig. 5.2c. Considering the errors stated above, the tolerable comparator offset has been compressed. The comparator

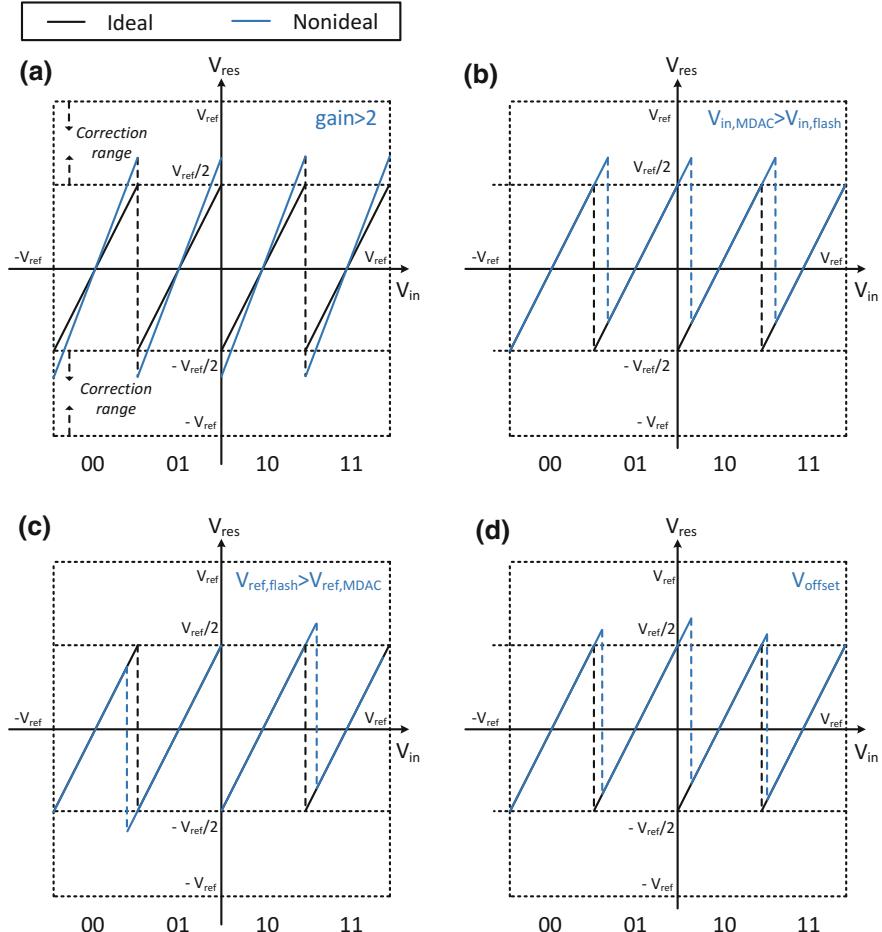


Fig. 5.2 The input/output characteristics of a 2-bit stage with nonideal factors

offset results in random deviation of the decision levels, enlarging the residue range in Fig. 5.2d.

Luckily, besides the redundancy, other techniques are usually adopted to mitigate those nonidealities. To eliminate the aperture error, solutions include matching the sampling, calibrating the sampling, and sharing the sampling (Sect. 2.2.1). To reduce the effect of the interstage gain's error, the calibration is adopted to improve the capacitor's matching and the designed gain is typically less than the ideal one (Sect. 6.4.1). As to the comparator's offset, the calibration is also adopted to reduce it (Sect. 6.4.3). With the aid of those techniques, the residue can be limited in the correction range, improving the conversion linearity of the ADC.

5.2.2 Reference Voltage Stabilization Technique

For flash ADCs, the kickback noise may disturb the analog input and the reference voltages, because a large number of comparators switch at the same time [1]. The fluctuation of the reference voltages lead to increased nonlinearity of the conversion. In flash-based ADCs, the increased nonlinearity of the flash ADC may lead to over-range residue and degrade the accuracy of the conversion. In the architecture level, the fluctuation can be compressed by increasing the current in the resistor ladder (which generates the reference voltages) and adopting decoupling capacitors, to relax the requirement of the kickback noise.

The two approaches are verified by a 3.5-bit flash ADC, where 14 comparators are used. The current in the resistor ladder is $140 \mu\text{A}$, and no decoupling capacitors are adopted. Without reference voltage stabilization techniques, the INL errors are $0.75/-0.75 \text{ LSB}$, shown in Fig. 5.3a. To improve the linearity, the resistance in the ladder is reduced by half, and the current increases to $280 \mu\text{A}$. The bandwidth of the resistor ladder is doubled, speeding up the settling of reference voltages. As a result, the INL errors reduce to $0.32/-0.32 \text{ LSB}$, as shown in Fig. 5.3b. Another solution is adopting decoupling capacitors, which are connected between 14 reference voltages and the ground. The capacitance at every node is about 5 pF . By stabilizing the reference voltage, the INL errors drop to $0.21/-0.21 \text{ LSB}$, as shown in Fig. 5.3c.

Considering that the 3.5-bit flash ADC is the first stage of a 11-bit ADC, like that in Fig. 2.30. Without reference voltage stabilization techniques, the residue of the first stage is over-range, leading to conversion errors, as shown in Fig. 5.4a. By doubling the current in the resistor ladder or adopting decoupling capacitors, the residue voltage range are both effectively compressed, as shown in Fig. 5.4b and c,

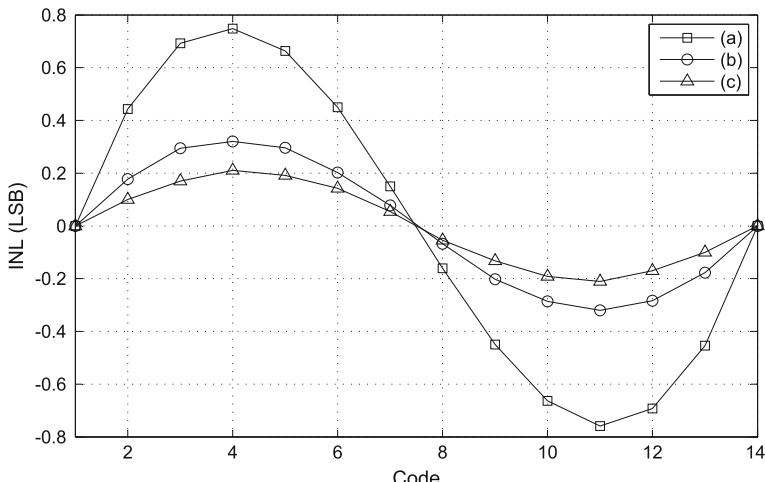


Fig. 5.3 INL errors of a 3.5-bit flash ADC **a** without the reference voltage fluctuation reduction, **b** increasing the current in the resistor ladder, and **c** adopting decoupling capacitors

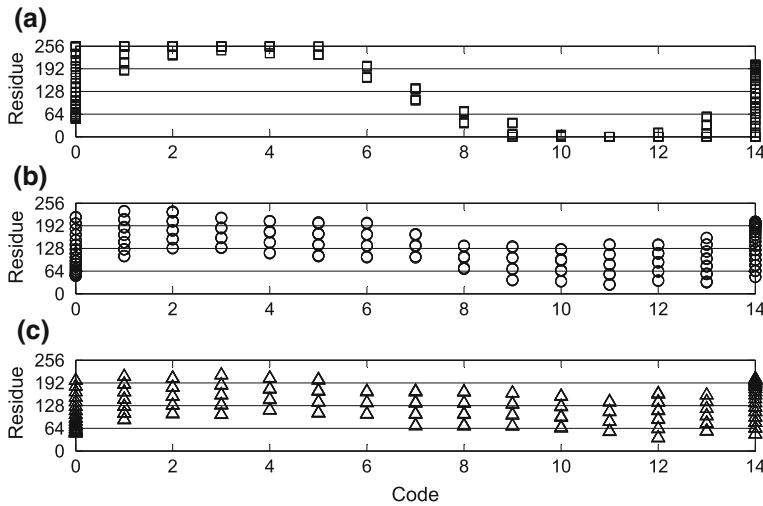


Fig. 5.4 The residue of the 3.5-bit flash ADC **a** without the reference voltage fluctuation reduction, **b** increasing the current in the resistor ladder, and **c** adopting decoupling capacitors

Table 5.1 Simulated ADC performance without/with the reference voltage fluctuation reduction

	ENOB (bit)	SNR (dB)	SNDR (dB)	SFDR (dBC)
Without fluctuation reduction	4.2	30.5	29.5	30.9
Adopting decoupling capacitors	11.0	68.1	78.9	80.0
Doubling current	11.0	68.1	78.9	80.0

to accommodate the conversion of the second stage. Benefit from the under-range residue, the accuracy of the 11-bit ADC in Fig. 2.30 is effectively improved. As summarized in Table 5.1, removing the error of the over-range residue, ENOB, SNR, SNDR, and SFDR are improved from 4.2 bit, 30.5, 29.5 dB, and 30.9 dBC to 11.0 bit, 68.1, 78.9 dB, and 80.0 dBC, respectively.

Based on the performance achieved, both of the techniques discussed are effective to stabilize the reference voltages of the flash ADC and hence improve the accuracy of the flash ADC and flash-based ADC.

5.3 Comparator Design

In the latch-type comparator, the pre-amplifier, either the static one or the dynamic one, is usually adopted to sense the small input, reducing the delay time, compressing the offset and isolating the kickback noise. A common model of the latch-type comparator is depicted in Fig. 5.5, comprising a pre-amplifier and a latch, which is simplified into two cross-coupled inverters, providing the positive feedback and resetting in every period. It is also called the regenerative comparator. The pre-amplifier changes the small input to the sufficiently large one and then applies it to the latch. It combines the best aspects of the amplifier, providing the negative exponential response, and the latch, providing the positive exponential response [2]. The step response of the latch-type comparator in the time domain is shown in Fig. 5.6. During t_1 , the pre-amplifier amplifies the input linearly to V_x , which is applied to the latch and goes to the desired voltage during t_2 .

Based on the pre-amplifier adopted, comparators are classified into two types, comparators with the static pre-amplifier and ones with the dynamic pre-amplifier. Due to the property of high power efficiency, the dynamic comparators are widely adopted in the low-power ADC. Therefore, we focus on the design of the dynamic comparators, discussed in detail in the following sections.

A commonly adopted comparator is depicted in Fig. 5.7. It consists of two stages, the pre-amplifier and the latch. In the reset phase, CLK is low and V_p and V_n are

Fig. 5.5 A simplified latch-type comparator

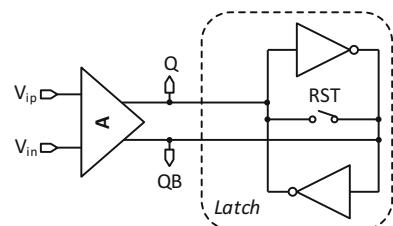


Fig. 5.6 Pre-amplifier and latch step response

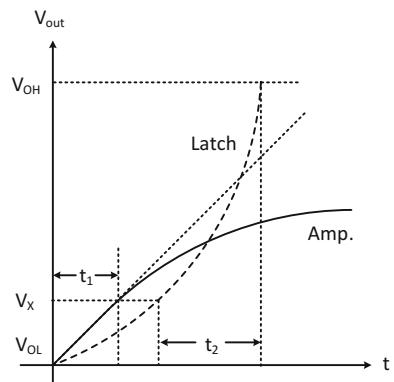
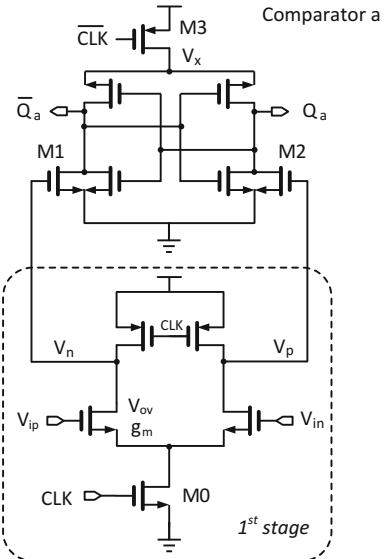


Fig. 5.7 A commonly adopted latch-type comparator



charged to VDD. As a consequence, M1 and M2 discharge the outputs to the ground. In the comparison phase, CLK becomes high and M0 turns on. V_p and V_n begin to drop at different rates, depending on the inputs, and trigger the latch after V_x charged to VDD via M3. Therefore, high-accuracy \overline{CLK} is required to turn on M3 in advance.

The comparators in Fig. 5.8a is based on the double latch-type comparator in [3, 4] and the first stage refers to Fig. 5.7. And the one in Fig. 5.8b is obtained by exchanging PMOS transistors with NMOS ones to switch the output state in the reset phase. Take the one in Fig. 5.8a to illustrate the operation. In this comparator, the falling edge of V_p or V_n instead of \overline{CLK} is used to trigger the second stage directly. Besides M1 and M2, M3 and M4 attach to V_p and V_n to increase the gain of the second stage and hence improve the comparison sensitivity. Moreover, the clock driving requirement is relaxed due to the absence of \overline{CLK} and the pre-charge switches are controlled by V_p and V_n instead. Additionally, M3 and M4 are adopted to discharge X_p and X_n to clear the charge left in the last comparison phase.

Since the positive feedback is provided by the latch, half of the differential inputs in the second stage can be cut off to reduce the switching. That is the basic idea behind the comparator in Fig. 5.9. In the reset phase, CLK is low and the outputs are discharged to the ground by M1 and M2. When CLK becomes high, if V_p is higher than V_n during the discharging, V_p is selected to control the cross-coupled inverters by turning on M8 and V_x is charged to VDD by turning M3 on. As a result, Q_d is discharged to the ground by M5 and $\overline{Q_d}$ is charged to VDD by M7. In other words, almost half of the second stage does not switch during this comparison phase, which is helpful to save the power dissipation.

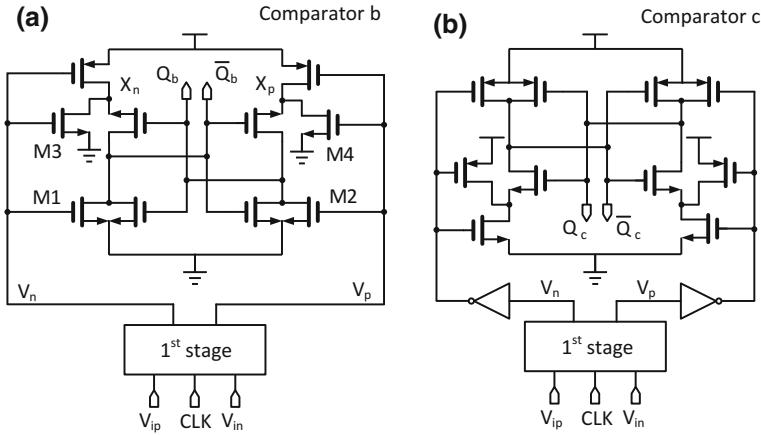


Fig. 5.8 Two comparators based on the comparator in [3] (the first stage refers to Fig. 5.7)

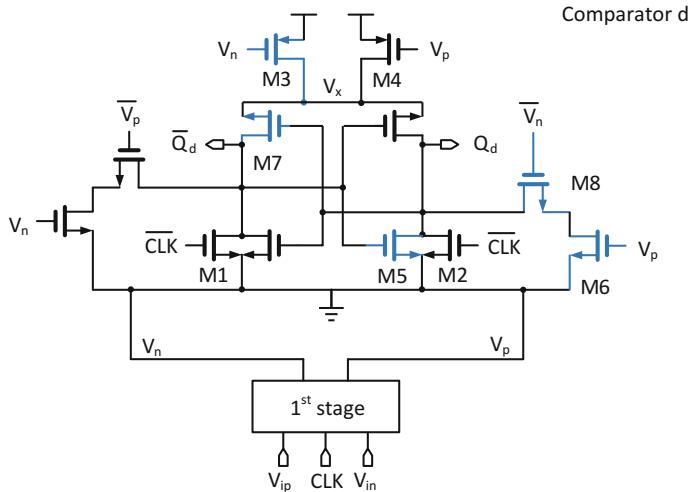


Fig. 5.9 A latch-type comparator (the first stage refers to Fig. 5.7)

5.3.1 Speed and Power Dissipation

For the power-efficient ADC, the delay of the comparator and the power dissipation are required to be as small as possible. The four comparators discussed above share the same pre-amplifier, and the latches adopted determine the delay. To compare the speed and power of the latches fairly, they are driven by one pre-amplifier and the size of the transistors at the corresponding notes are same.

The signal behavior are depicted in Fig. 5.10. The period of CLK is 2 ns and the differential input is 10 mV. As shown in Fig. 5.10b, when CLK becomes high, V_p and

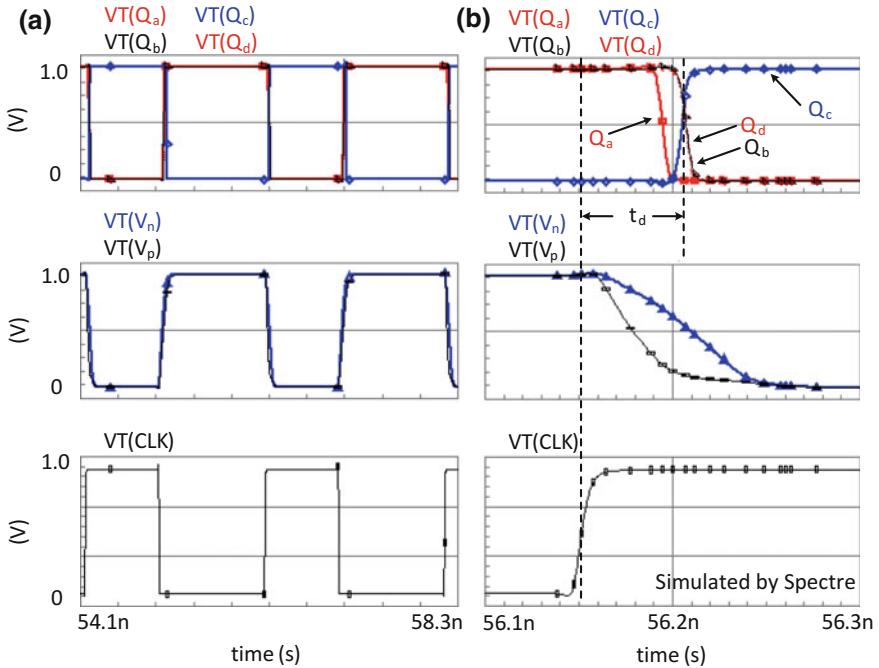


Fig. 5.10 **a** The signal behavior of four comparators and **b** that around the triggering time

Table 5.2 The current consumed comparison

Latch in	Fig. 5.7	Fig. 5.8a	Fig. 5.8b	Fig. 5.9
$I_{latch}(\mu A)$	44.33	19.69	26.33	14.06

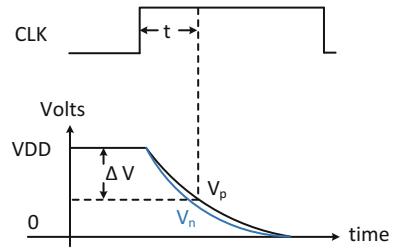
V_n begin to discharge from VDD at different rates and the outputs begin to switch from the reset states. The delay, t_d , is defined by the time between the clock edge and the instant when Q_i ($i = a, b, c, d$) crosses 50 % of VDD. The delay of comparator in Fig. 5.7 is smallest and others are similar.

The current consumed by the latches are summarized in Table 5.2. The latch in Fig. 5.9 is the most power-efficient, because that only half of the second stage are switched in the comparison phase.

5.3.2 Noise

Considering that the pre-amplifier is the main contributor, the noise generated by the latch is neglected. The noise analysis is based on the small-signal circuit model. The transient response of the pre-amplifier in Fig. 5.7 is illustrated in Fig. 5.11 and

Fig. 5.11 The transient response of V_p and V_n in Fig. 5.7



its load is C_L . The gain of the pre-amplifier varies over time and can be written as

$$A(t) = g_m t / C_L \quad (5.1)$$

where

$$t = 2C_L \Delta V / I_b \quad (5.2)$$

and $A(t)$ can be rewritten as

$$A(t) = 2\Delta V / V_{ov} \quad (5.3)$$

where g_m and V_{ov} are the transconductance and overdrive voltage of the input transistor in Fig. 5.7. The output noise power of the pre-amplifier is

$$V_{no}^2(t) = \frac{2KT}{C_L} + \frac{4KT\gamma g_m}{C_L^2} t, \quad \gamma = 2/3 \quad (5.4)$$

And the input-referred noise power is

$$V_{ni}^2(t) = \frac{2KTC_L}{(g_m t)^2} + \frac{4KT\gamma}{g_m t} \quad (5.5)$$

Substitute $A(t)$ into Eq. 5.5, and the input-referred noise power can be described as

$$V_{ni}^2(t) = \frac{2KTC_L}{(g_m t)^2} + \frac{4KT\gamma}{A(t)C_L} \quad (5.6)$$

In order to reduce the input-referred noise, the gain, $A(t)$ should be increased. And hence, it is expected that the input transistors are in the saturation region from the rising edge of CLK to the triggering time of the latch. To maintain the input transistors in the saturation region, the common-mode voltage of V_p and V_n can not drop too much, and the acceptable ΔV is

$$\Delta V_{max} = VDD - V_{CMI} + V_{th} \quad (5.7)$$

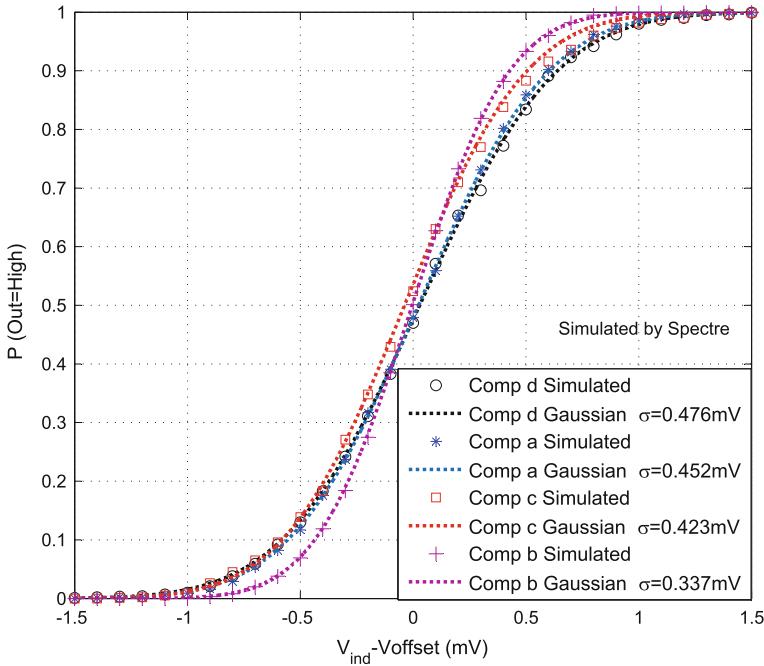


Fig. 5.12 The noise comparison

And the maximum amplification time and gain is

$$t_{max} = 2C_L \Delta V_{max} / I_b \quad (5.8)$$

$$A(t)_{max} = 2\Delta V_{max} / V_{ov} \quad (5.9)$$

Therefore, increasing the amplification time, decreasing the input common-mode voltage and compressing the overdrive voltage of the input transistors are helpful to improve the gain and hence reduce the input-referred noise. Besides, the input-referred noise can be decreased by enlarging the load at V_p and V_n .

It should be noted that increasing the amplification time and enlarging the load reduce the comparison speed. And hence the noise and the speed should be traded off.

The equivalent input noise is shown in Fig. 5.12. Fitting the result to a Gaussian cumulative distribution gives the RMS noise voltage. The RMS noise of comparator a (in Fig. 5.7), b (in Fig. 5.8a), c (in Fig. 5.8b), d (in Fig. 5.9) are 0.452 mV, 0.337 mV, 0.423 mV, 0.475 mV, respectively. Comparator b in Fig. 5.8 achieves the lowest noise.

5.3.3 Offset

The comparator offset is composed of the effective latch offset that is compressed by the amplifier gain and the amplifier offset. The comparator offset can be described as

$$V_{os} = V_{os, amp} + \frac{V_{os, latch}}{A} \quad (5.10)$$

where V_{os} , $V_{os, amp}$, $V_{os, latch}$ are the input referred offsets of the comparator, preamplifier and latch, and A is the preamplifier gain. Obviously, the amplifier offset is the main contributor and the direct method of decreasing the offset is to compress the preamplifier offset and maintain a relative high gain.

The preamplifier offset and gain are to be discussed. Figure 5.13 illustrates the static and dynamic preamplifiers. For the static preamplifier, the input referred offset and gain can be derived as

$$V_{os,static} = \Delta V_T(V_{SB}) + \frac{V_{GS} - V_T(V_{SB})}{2} \left(\frac{\Delta R_L}{R_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L} \right) \quad (5.11)$$

and

$$A_{static} = g_m(R_L//r_{ds}) \quad (5.12)$$

where $K' = \mu_n C_{ox}/2$. According to Eq. 5.11, the comparator offset is related to the size of components, the threshold voltage, the DC operation voltage, and their mismatch. Likewise, for the dynamic preamplifier, the input referred offset and gain can be derived as

$$V_{os,static} = \Delta V_T(V_{SB}) + \frac{V_{GS} - V_T(V_{SB})}{2} \left(-\frac{\Delta C_L}{C_L} + \frac{\Delta K'}{K'} + \frac{\Delta W/L}{W/L} \right) \quad (5.13)$$

and

$$A(t)_{dynamic} = \frac{g_m t}{C_L} \quad (5.14)$$

Comparing Eq. 5.11 with Eq. 5.13, the capacitor size and mismatch also determine the offset voltage in the dynamic comparator, besides the factors mentioned above.

The statistical simulation results (by 100-point Monte Carlo simulation) on the input-referred offset are shown in Fig. 5.14. The 1-sigma(σ) offset voltages of comparator a, b, c, and d are 9.31, 9.14, 8.93, and 9.14 mV, respectively. Comparator c achieves the smallest offset.

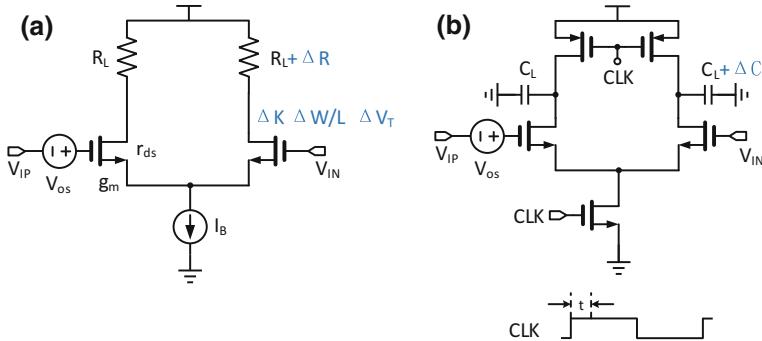


Fig. 5.13 The **a** static and **b** dynamic preamplifiers

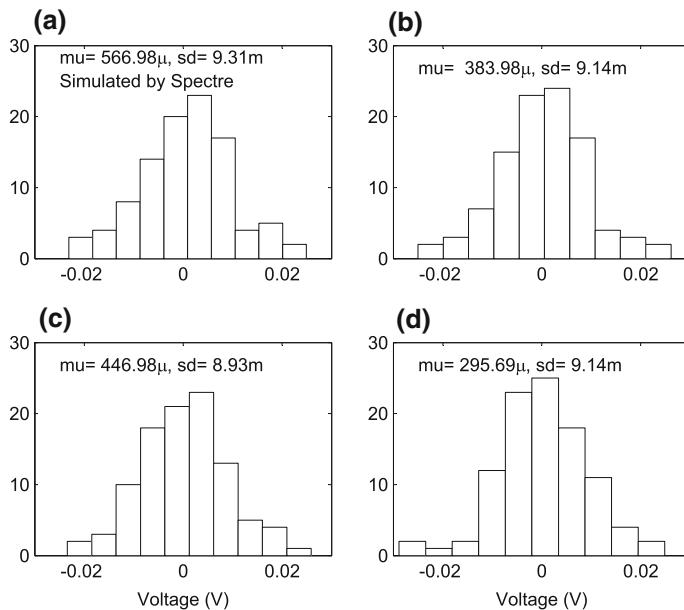


Fig. 5.14 Statistical simulated results on the input-referred offset of comparator (a) a, (b) b, (c) c, and (d) d

5.3.4 Kickback Noise

In the dynamic comparator, the large voltage variations on the node of V_c , V_n , and V_p are coupled to the input of the comparator, through the parasitic capacitance, $C_{gs,p}$, $C_{gs,n}$, $C_{gd,p}$, $C_{gd,n}$ in Fig. 5.15a. On one hand, since the circuit preceding it does not have zero impedance, once CLK becomes high, the common-mode input voltage is disturbed to a lower voltage. That is because that V_c switches from the floating

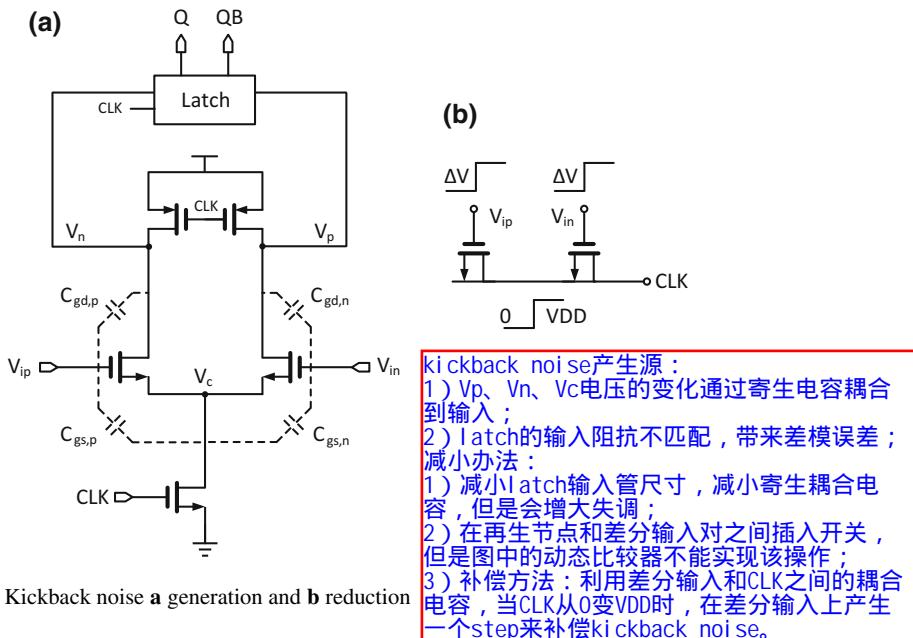


Fig. 5.15 Kickback noise **a** generation and **b** reduction

voltage (>0 V) to the ground and V_n and V_p drop from the power supply. On the other hand, since the impedances of the differential circuit preceding it may not be equal, the differential-mode voltage error is introduced to the input. The common-mode and differential-mode disturbance are usually called the kickback noise, which may degrade the accuracy of the converter. Since the differential pair operates in various regions (cutoff, saturation, and triode regions) in one period, the dynamic comparator originates larger kickback noise than the static pre-amplifier-based comparator.

The kickback noise commonly can be reduced by three types of approaches, reducing the transistor size, the isolation, and the compensation. However, reducing the transistor size leads to increased offset voltage. Inserting switches between regeneration nodes and the differential pair [5–7] cannot be applied in the dynamic comparator, because that differential pair can not be isolated from the voltage variations discussed above, as shown in Fig. 5.15a. Here, a kickback noise reduction technique for the dynamic comparator is introduced. In Fig. 5.15b, a pair of NMOS is introduced, working as the capacitor between differential input and CLK. When CLK switches form 0 to VDD, the voltages at V_{ip} and V_{in} increase due to the step response, compensating for common-mode voltage drop and differential-mode voltage variation resulted in by the kickback noise. The technique is verified by a 10-bit 100 MSps SAR ADC, and simulated results are summarized in Table 5.3. By adopting the technique in Fig. 5.15b, ENOB, SNR, SNDR, and SFDR are improved by 0.3 bit, 2, 2.1, and 2.9 dB, respectively.

Table 5.3 Simulated ADC performance without/with the kickback noise reduction

	ENOB (bit)	SNR (dB)	SNDR (dB)	SFDR (dBc)
Without kickback noise reduction	9.7	60.6	60.0	71.0
With kickback noise reduction	10.0	62.6	62.1	73.9

5.4 Summing up

The design considerations of the comparator are presented in this chapter. In the architecture level, the requirements can be relaxed. The redundancy technique enables the tolerance of the comparator offset, and the reference voltage stabilization technique effectively reduces requirements of the kickback noise. In the circuit block level, the optimization of the speed and power dissipation, the noise, the offset, and the kickback noise are discussed in detail.

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Chapter 6

Calibration

6.1 Introduction

The ADC requires the linearity enhancement and power reduction techniques. Besides the precise analog design techniques and the redundancy techniques, introducing the calibration is another solution to mitigating the nonideal factors in the ADC. First, the nonideal factors in different architectures are introduced. Then, the principle of the calibration is presented. Furthermore, typical calibration techniques for the pipelined ADC, the SAR ADC, the flash ADC, and the time-interleaved ADC are discussed in detail.

6.2 Error Mechanisms

The main nonideal factors in the pipelined ADC, the SAR ADC, the flash ADC, and the time-interleaved ADC are reviewed in this section, as the preparation for understanding calibration techniques.

6.2.1 Errors in Pipelined ADC

The dominant error sources in a pipelined ADC include the gain error, the DAC error, the aperture error, and the DNL error, as shown in Fig. 6.1. Besides, they also include the opamp nonlinearity, the settling error, the charge injection, and so on.

6.2.1.1 Gain Error

Due to the capacitor mismatch between the sampling capacitors and the feedback capacitors, and the finite opamp gain, the interstage gain can be derived as

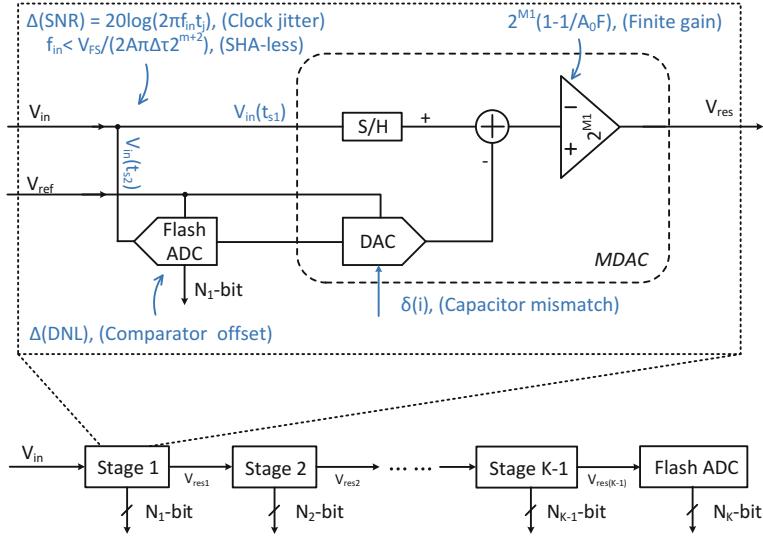


Fig. 6.1 The pipelined ADC with error sources

$$A = A_{ideal} \left(1 - \frac{1}{A_{opamp} \frac{C_F}{C_S + C_F}} \right) \quad (6.1)$$

where A_{ideal} is the ideal interstage gain and can be described as

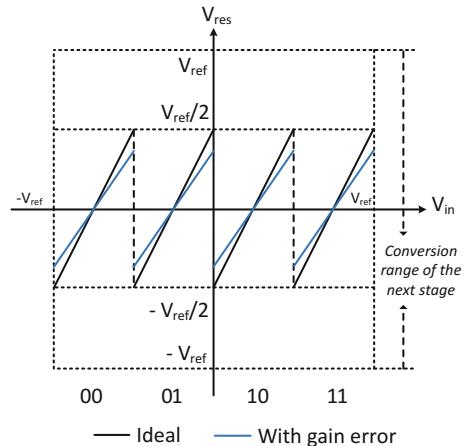
$$A_{ideal} = \frac{C_S + C_F}{C_F} \quad (6.2)$$

A_{opamp} is the opamp gain, C_F is the feedback capacitance, and C_S is the sampling capacitance. Take a 2-bit stage with 1-bit redundancy as an example. The input/output characteristics with nonideal interstage gain are illustrated in Fig. 6.2. The ideal gain of 2 is modified by $(1 - 1/A_{opamp} F)$, where F is the feedback factor, $C_F/(C_S + C_F)$. The compressed interstage gain results in the missing code at every transition point. And hence the constant DNL error and constant jump in INL curve are introduced at every transition of the bits resolved by this stage [1].

6.2.1.2 DAC Error

The DAC error is introduced by the mismatch between the feedback capacitor and each capacitor attaching to the reference voltage. Take a 2-bit stage with 1-bit redundancy as an example. The residue voltage can be derived as

Fig. 6.2 The input/output characteristics of a 2-bit stage with nonideal interstage gain



$$V_{res} = AV_{in} - \frac{V_{ref}}{C_F} \sum_{i=1}^3 D_i C_{s,i} \quad (6.3)$$

Considering that

$$C_{s,i} = \Delta C_{s,i} + C_{s,ideal} \quad (6.4)$$

Equation 6.3 is rewritten as

$$V_{res} = AV_{in} - \frac{V_{ref}}{C_F} \sum_{i=1}^3 D_i C_{s,ideal} - \delta(i) \quad (6.5)$$

$$\delta(i) = \frac{V_{ref}}{C_F} \sum_{i=1}^3 D_i \Delta C_{s,i}, \quad (6.6)$$

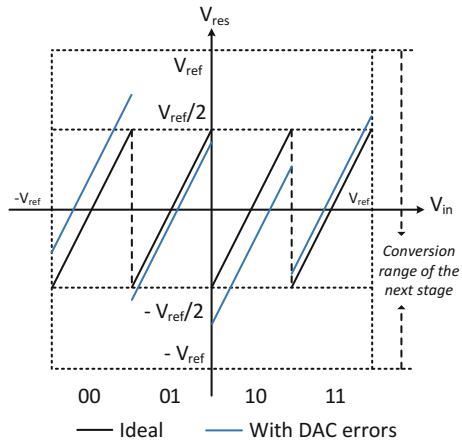
where D_i are the outputs of comparators, $C_{s,i}$ is the i th sampling capacitor, $C_{s,ideal}$ is the ideal unit sampling capacitor.

As is displayed in Fig. 6.3, every linear segment of the transfer curve is moved up or down by $\delta(i)$. Because the static random values $\delta(i)$ are different for different segments, the harmonic distortion is introduced.

6.2.1.3 Aperture Error and Clock Jitter

The aperture error is introduced due to the different sampling instant in the SHA-less architecture, and the details are discussed in Sect. 2.2.1.1. The input frequency is limited by the aperture error, which has been described in Eq. 2.4 and is rewritten as follows. For the $(m+1)$ -bit individual stage with the redundancy of 1 bit,

Fig. 6.3 The input/output characteristics of a 2-bit stage with DAC errors



$$2A\pi f_{in} \Delta\tau < \frac{V_{FS}}{2^{m+2}}, \quad (6.7)$$

where f_{in} and V_{FS} are the frequency and the differential full-scale voltage of the input.

For an ideal ADC, the clock jitter, t_j , reduces the SNR by [2]

$$\Delta SNR = 20\log(2\pi f_{in} t_j) \quad (6.8)$$

And hence the input frequency is limited by the clock jitter to achieve a fixed SNR.

6.2.1.4 Comparator Offset

The sub-ADC is usually implemented by the flash ADC, as is shown in Fig. 6.1. And in the flash ADC, the comparator offset is the main error source, which results in the nonlinearity and this error has become more serious in the multi-bit pipelined stage, which is to be presented in Sect. 6.2.3.

6.2.2 Errors in SAR ADC

In 1-bit/cycle capacitive binary SAR ADC, it is well established that the quantization error, the capacitor mismatch, and the noise limit the performance. Among nonideal factors, the capacitor mismatch, which is commonly reduced by enlarging the component size [3] or compensated for by calibration schemes, is the main static error source. To get a thorough understanding of it, errors introduced by the capacitor mismatch are to be discussed in different perspectives.

6.2.2.1 Code Density with Capacitor Mismatches

To illustrate the impact of the capacitor mismatch on the ADC performance, the code density of the ADC with a ramp signal as the input is shown in Fig. 6.4. Without the capacitor mismatch, the uniform code distribution is described in Fig. 6.4a. Considering that the MSB capacitor is mismatched, conversion errors occur around code 100..00, which are shown in Fig. 6.4b and c. If the MSB capacitor is smaller than the ideal one, missing codes occur, leading to the nonlinearity of the SAR ADC. If the MSB capacitor is larger than the ideal one, multiple input levels are mapped to one code, resulting in more codes around 100..00, which means the loss of the analog information and cannot be calibrated.

6.2.2.2 Transfer Curve with Capacitor Mismatches

The impact of the capacitor mismatch can be illustrated by the transfer curve. In [4], the transfer curve of conventional SAR ADC with capacitor mismatches is analyzed. Here is the impact of the capacitor mismatch on a subranging capacitive SAR ADC. A 11-bit subranging SAR ADC, which consists of a 4-bit flash ADC for coarse conversion and a 8-bit SAR ADC for fine conversion, is shown in Fig. 6.5. The capacitor array is composed of the flash capacitor array controlled by the digital output of the flash ADC and the SAR capacitor array controlled by the SAR logic. At the tracking phase, all the flash capacitors and the MSB segmented SAR capacitors attach to the input signal. At the flash phase, the flash capacitor array switches according to Q_i ($i = 1, 2, \dots, 15$) and the rest of capacitors attach to the common-mode voltage. The output of the DAC can be derived as

$$V_{out,DAC} = -V_{res} = V_{in} - \alpha \sum_{i=1}^{15} Q_i C_i \quad (6.9)$$

$$\alpha = \frac{V_{ref}}{47C_u} \quad (6.10)$$

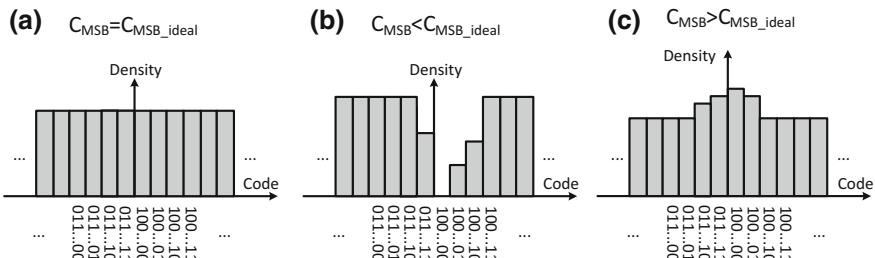


Fig. 6.4 The code density with capacitor mismatches

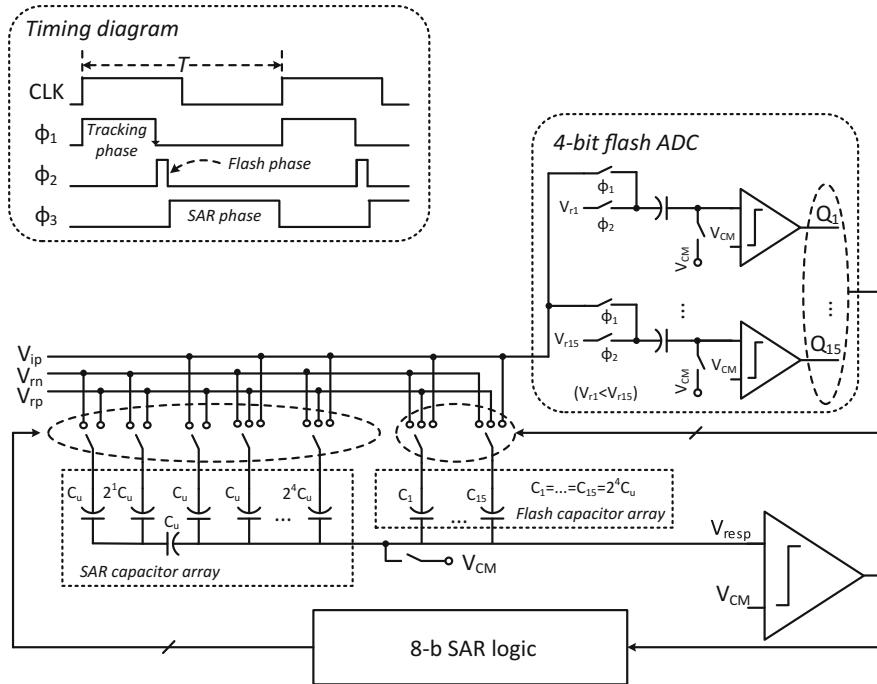


Fig. 6.5 A 11-bit subranging SAR ADC and timing diagram (single-end ADC is shown for simplification)

The transfer curve of the ADC at the end of the flash phase is described in Fig. 6.6 and the steps in the curve can be derived as

$$H_i = 2\alpha C_i \quad (6.11)$$

The deviation caused by capacitor mismatch is

$$\Delta H_i = 2\alpha \Delta C_i \quad (6.12)$$

$$\Delta C_i = C_i - C_{i,ideal} \quad (6.13)$$

It is noted that the i -th curve deviates from the ideal one only due to C_i , which results in the conversion errors of the ADC.

Additionally, in a subranging SAR ADC and an multi-bit/cycle SAR ADC, which are both flash-based architectures, the comparator offset limits the performance of the conversion. The conversion errors introduced by the comparator offset are discussed in Sect. 6.4.3.

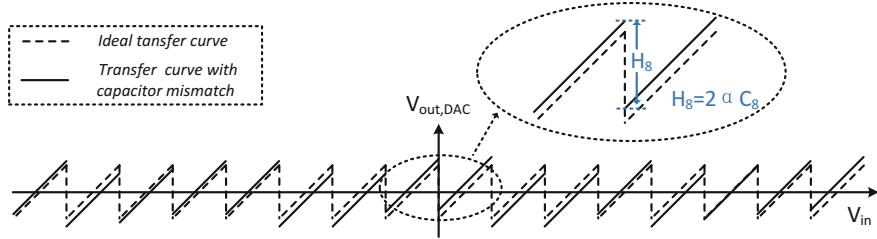


Fig. 6.6 Transfer curve of the DAC at the end of the flash phase

6.2.2.3 ENOB with Capacitor Mismatches

The impact of the capacitor mismatch can be described by the reduced ENOB. For a N -bit SAR ADC, the equation relating the ENOB and the capacitor mismatch is derived as [5]

$$\text{ENOB} = N - \log_4[1 + 3\alpha\gamma_0^2 + 3\alpha \sum_{i=1}^{N-1} (2^{i-1}\gamma_i)^2]$$

$$\alpha = \frac{3(4 - \pi)}{\pi} \approx 0.8197, \quad (6.14)$$

where γ_i is the composite fractional mismatch of the i -th capacitor groups. It is noteworthy that Eq. 6.14 is consistent with the standard sinusoidal testing.

Besides, the relationship between the ENOB and required capacitor mismatch is shown in Fig. 6.7 and Table 6.1, which could be the reference to design the capacitance. A (ENOB+1)-bit SAR ADC is modeled to operate the simulation and the yield is calculated according to 1000 times results. Figure 6.7 shows that $\sigma(\Delta C/C)$ is required to reduce nearly to a half to increase 1-bit ENOB, where

$$\Delta C/C = \frac{C_1 - C_2}{0.5(C_1 + C_2)} \quad (6.15)$$

C_1 and C_2 are the capacitor pair. The capacitor mismatch $\sigma(\Delta C/C)$ is provided by semiconductor foundries. The yield maintains above 0.9 during the simulation, and the detailed data is listed in Table 6.1.

6.2.3 Errors in Flash ADC

The flash ADC suffers from the issue of the comparator offset, which results in the nonlinearity. Take a 3-bit flash ADC as an example. The comparator offset voltages

Fig. 6.7 Required capacitor mismatch versus the ENOB

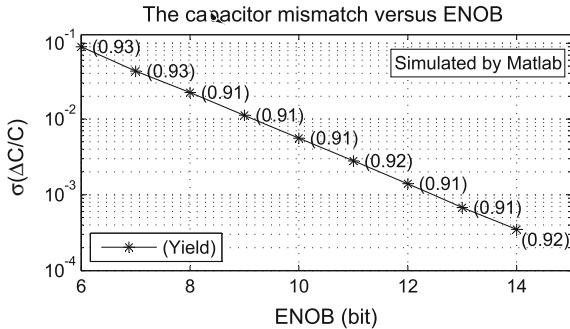


Table 6.1 Required capacitor mismatch versus the ENOB

ENOB	$\sigma(\Delta C/C)$	ENOB	$\sigma(\Delta C/C)$	ENOB	$\sigma(\Delta C/C)$
6	0.0896	9	0.0112	12	0.0014
7	0.043	10	0.0056	13	0.00068
8	0.0224	11	0.0028	14	0.00035

lead to the deviation of the transition points, as is shown in Fig. 1.2. The introduced nonlinearity can be expressed by the DNL (Eq. 1.4) and INL (Eq. 1.5).

Recently, more interests in the comparator offset have been created due to two reasons, the reduction of the tolerable offset voltage and the limitation of the scaled CMOS process.

First, the tolerable offset voltage is compressed with the increase of the resolution. It should be noted that the multi-bit (like, 5 bit) flash ADC is usually adopted in the pipelined ADC for the performance optimization. For a N-bit flash ADC, the maximum offset voltage of $\pm FS/2^{N+2}$ can be accepted. As is shown in Fig. 6.8, assuming that the full scale of the ADC is 2 V, the acceptable offset voltage is as small as 15.6 mV in a 5-bit ADC. What is worse, the acceptable offset voltage is only 1.9 mV in a 8-bit ADC. Therefore, the low-offset comparator is a challenge for the flash ADC.

Additionally, the advanced CMOS process technology makes the situation serious. The scaled CMOS process is usually adopted by the flash ADC to improve the conversion rate and save the power dissipation. With the scaled technology, L_{min} is scaled down. However, the mismatch parameter A_{VT} [6–8] does not scaled at the same rate as L_{min} . In another word, in the advanced process technology, the circuit with the same W/L_{min} will exhibit larger offset. And thereby, the offset voltage of the comparator implemented by the scaled CMOS process becomes larger. Factors which determine the comparator offset are discussed in Sect. 5.3.3.

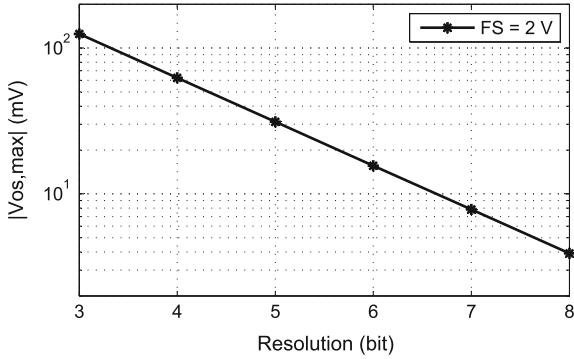


Fig. 6.8 The tolerable offset voltage versus the resolution of the flash ADC

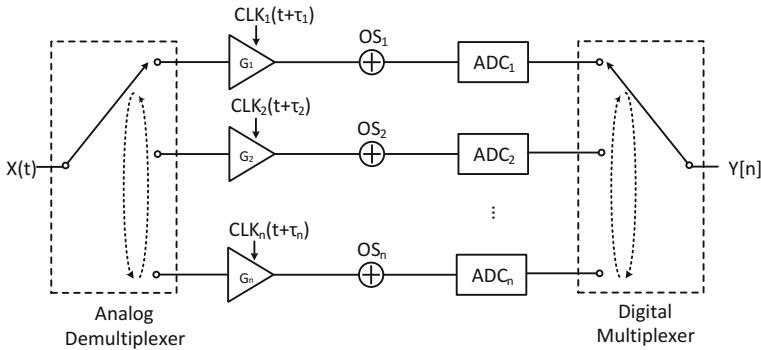


Fig. 6.9 Model of mismatches in time-interleaved ADCs

6.2.4 Errors in Time-Interleaved ADC

Time-interleaved ADC is an architecture that cycles through N channel-ADCs, with a N -phase clock to drive the sampling of each channel by turns. Ideal channel output is

$$y_i[n] = x((n - 1)N + i)T_s \quad (6.16)$$

where T_s is the sampling period of the time-interleaved ADC.

However, micro nonuniformity inevitably exists between channels due to variations in signal and clock paths, prominently reflected in offset, gain, and sampling intervals. Figure 6.9 shows the model of mismatches in time-interleaved ADCs. These mismatches modify the channel output into

$$y_i[n] = G_i x((n - 1)N + i)T_s + \tau_i + OS_i, \quad (6.17)$$

where OS_i , G_i , τ_i are the offset, gain and time skew of channel_i.

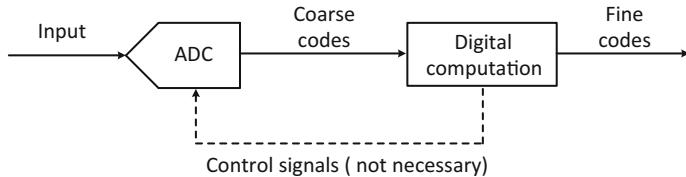


Fig. 6.10 The basic idea behind the digital calibration techniques

6.3 Calibration Principle

The calibration techniques are usually divided into three categories: the trimming, the analog domain calibration, and the digital calibration. While trimming on-chip capacitors or resistors is effective [9–11], the technique suffers from the high cost. The analog domain techniques require extra analog circuits, such as DACs, opamps or even clock generators to operate the calibration [12–15]. With additional circuits joining in the normal conversion, the conversion rate usually slows down and the power dissipation increases. Without manual modification or extra circuits, the digital domain techniques measure the nonideal factors and compensate for them in the digital domain [16–20]. As the process-friendly technique, it has become more and more popular in the recent years.

Besides, the calibration techniques can also be classified into the foreground ones [13] and the background ones [21]. The foreground calibration techniques have to interrupt the normal operation and then start a calibration cycle. Therefore, they cannot be accepted by the applications which require the real-time conversion of the input. The background calibration techniques are transparent to the users and thereby the predetermined standby modes of applications can be removed.

Considering their advantages, we focus on the digital calibration techniques. The basic idea is displayed in Fig. 6.10. The calibration block extracts the information from the coarse codes, and outputs the fine codes by efficient digital computation. If necessary, it also generates control signals to modify the ADC. From the point of view of the digital calibration techniques, it is not necessary to correct analog errors and errors in circuits can be removed from the codes by the computation.

6.4 Calibration Schemes

Calibration techniques proposed by our research group are presented in this section. For the pipelined ADC, a blind background calibration algorithm to correct the interstage gain error and capacitor mismatch is proposed. For the SAR ADC, two techniques are introduced to calibrate the capacitor mismatch. For the flash ADC, the input offset storage technique for the dynamic comparator is presented to cancel

the offset voltage. For the time-interleaved ADC, an autocorrelation-based timing mismatch calibration strategy is proposed.

6.4.1 Calibration of Pipelined ADC

The design of high-speed and high-resolution pipelined ADCs is getting more and more challenging as undesirable outcomes of technology scaling, like reduced device gain and supply voltage. The resolution is mainly limited by the capacitor mismatch and finite opamp gain. Therefore, various digital calibration techniques have been proposed to alleviate this problem.

6.4.1.1 Traditional Techniques

With the speedy development of technique of microprocessor and DSP, people become more and more rigorous about the accuracy of the sampled exoteric signal. Pipelined ADCs can provide high-resolution and high-speed data conversion with low power dissipation. However, the accuracy of pipelined ADCs is limited by nonideal factors such as finite opamp gain and capacitor mismatch. There are different calibration techniques to compensate for the nonideal effects. In [22–24], the structure of the analog circuits is modified and memories are needed, which increase the complexity and chip area. In [25], a split ADC is used, and two ADCs simultaneously process in parallel. In that method, the circuits become complex and have strict requirements on the symmetry. In [26], it inserts an uncorrelated analog signal into the input signal path and thus limits the range of the data converter. All these calibration methods need to modify the analog circuits. In [27], output code density test method is proposed and there is no need to modify the stage circuits. But it requires increased registers to store histogram bins and additional logic to perform the iterative search. Besides, the division is needed in the estimation, which increases the hardware overhead greatly. In [28], the original research on the blind background calibration to be discussed in Sect. 6.4.1.2 is presented. But, it only enables the 1-bit pipelined stage to calibrate the nonlinearity.

6.4.1.2 A Digital Blind Background Calibration Algorithm for Pipelined ADC

This section presents the improved blind background calibration algorithm to correct the interstage gain error and capacitor mismatch in the pipelined ADC [29]. It can be adopted in the 1-bit [28] or multi-bit pipelined stage. Without modifying analog circuits, the algorithm extracts the calibration information by analyzing the density of specific output codes. In the following section, the algorithm in the multi-bit pipelined stage is to be discussed.

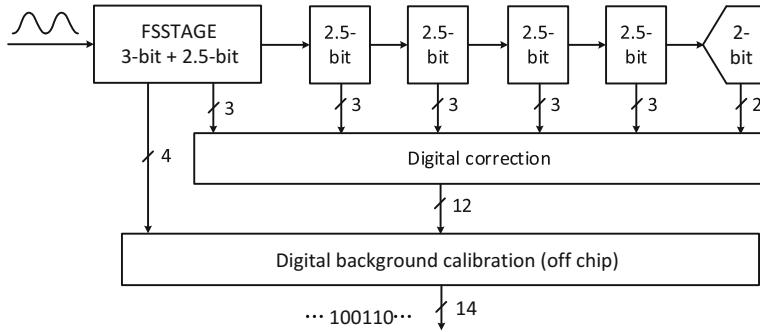


Fig. 6.11 The pipelined ADC with the calibration

For verification, it is used to calibrate a 14-bit 150 MSps ADC. As the ADC's performance is most sensitive to the first stage, the calibration technique is adopted by the first stage. Only the estimation information extracted from the outputs of following stages is stored. No modification of analog circuits is required. Besides, it is implemented by only 80 registers. Without using the multiplication or division in the digital logic, the algorithm can be implemented with a low hardware overhead, saving the power dissipation. At 15.5 MHz input, the SDNR/SFDR of the ADC is improved from 66.8 dB/78.57 dBc to 69.7 dB/87.3 dBc and the INL drops from 8 LSB to 3 LSB.

ADC Architecture

A 14-bit pipelined ADC with the calibration is shown in Fig. 6.11. A 3-bit first stage and a 2.5-bit second stage are merged as a single stage named FSSTAGE [30]. FSSTAGE is followed by four consecutive 2.5-bit stages and a final 2-bit flash ADC. And, each stage contributes 2-bit effective resolution. While the output of the first stage attaches to the calibration block, the outputs of the left stages are combined by the digital correction block. The calibration block collects the outputs of the first stage and the digital correction block to generate 14-bit codes.

Blind Calibration Algorithm

Error Model

Before illustrating the principle of the calibration, the nonlinearity error in the pipelined ADC is analyzed. A pipelined ADC with nonideal factors is shown in Fig. 6.12, where the ADC is composed of a stage to be calibrated (3-bit stage is used here) and an m-bit backend ideal ADC. The nonideal factors include the capacitor mismatch and the interstage gain error. V_{in} is the analog input and V_{ref} is the reference voltage. The output of the ADC is

$$Adout = q + \sum_{i=0}^{b_o} h_i, \quad b_o = 0, 1, 2, \dots, 8 \quad (6.18)$$

Fig. 6.12 The pipelined ADC to be calibrated

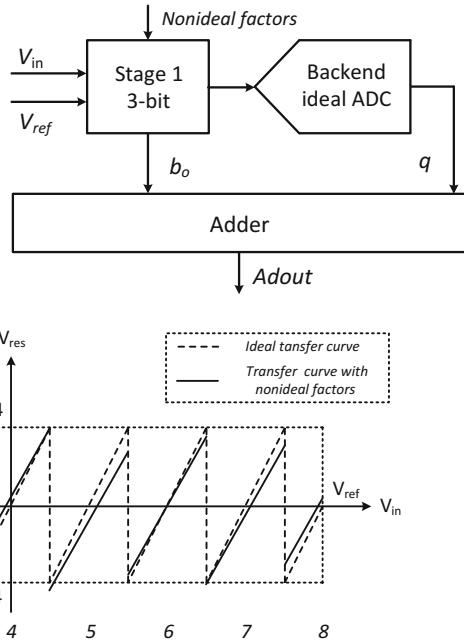


Fig. 6.13 The transfer curve of a 3-bit stage

where b_o is the digital output of the first stage in decimal, h_i is the bit weight and $h_0 = 0$, and q is the digital output of the backend ADC. h_i can also be illustrated by the transfer curve in Fig. 6.13, where h_i is the $i - th$ step. While the solid line is the transfer curve taking the nonideal factors into account, the dashed one plots the ideal curve. Since each step is the combination of the positive segment and the negative one, h_i can be written as

$$h_i = \begin{cases} 0, & i = 0 \\ h_{i1} + h_{i2}, & i = 1, 2, \dots, 8 \end{cases} \quad (6.19)$$

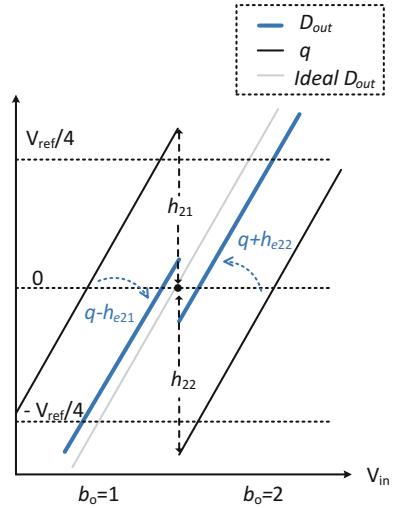
where h_{i1} is the positive segment and h_{i2} is the negative one.

The ADC output can be described as

$$Adout = \begin{cases} q, & b_o = 0 \\ q + \sum_{i=0}^{b_o} (h_{i1} + h_{i2}), & b_o = 1, 2, \dots, 8 \end{cases} \quad (6.20)$$

where h_{i1} and h_{i2} deviate from the ideal value due to nonideal factors, resulting into the nonlinearity.

Fig. 6.14 The transfer curve of the first stage when $b_1=1$ and $b_1=2$



Basic Principle

The basic idea behind the calibration algorithm is to estimate h_i by analyzing the density of specific output codes. The estimation of h_2 is discussed as an example.

In Fig. 6.14, h_2 is the combination of h_{21} and h_{22} . It is noted that h_2 is one of the steps of the transfer curve in Fig. 6.13. The estimation of h_2 , h_{21} , and h_{22} are labeled h_{e2} , h_{e21} , and h_{e22} , respectively. If the output of the first is $b_o = 1$ or $b_o = 2$, D_{out} can be defined as

$$D_{out} = \begin{cases} q - h_{e21} & b_o = 1 \\ q + h_{e22} & b_o = 2 \end{cases} \quad (6.21)$$

If the estimation are exactly the ideal h_{21} and h_{22} , D_{out} will be ideal and become a straight line, as is shown in Fig. 6.14.

In order to estimate h_{e21} , codes are categorized into two overlapping types, one with $b_o = 1$ (Type I) and the other with $D_{out} < 0$ and $b_o = 1$ (Type II). The frequencies of two types are labeled f_{e21a} and f_{e21b} , respectively. As is shown in Fig. 6.15,

1. If h_{e21} is smaller than h_{21} , D_{out} may be positive, zero or negative. And thereby f_{e21a} is bigger than f_{e21b} .
2. If h_{e21} is bigger than or equal to h_{21} , D_{out} may be negative or zero. And hence f_{e21a} equals f_{e21b} .

Therefore, the relationships between the code density and the estimation can be described as

$$\begin{cases} f_{e21a} > f_{e21b} & h_{e21} < h_{21} \\ f_{e21a} = f_{e21b} & h_{e21} \geq h_{21} \end{cases} \quad (6.22)$$

Based on the frequency of the two categories of codes, h_{e21} is adjusted by

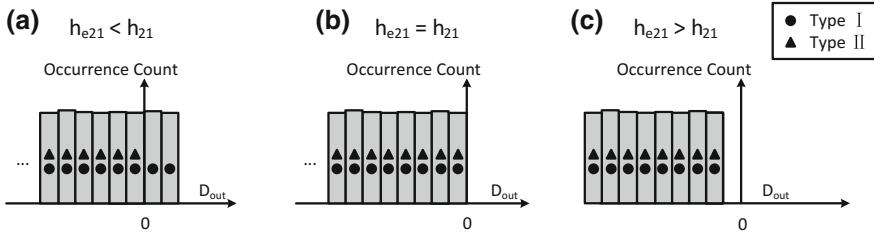


Fig. 6.15 Code frequency when $b_0=1$

$$h_{e21} = h_{e21} + \mu(f_{e21a} - f_{e21b}) \quad f_{e21a} > f_{e21b} \quad (6.23)$$

where μ is the step size and depends on the initial h_{e21} . It is noted that the initial h_{e21} should be less than the actual value. μ is usually $1/2^{R_1}$ ($R_1 > 1$), so that the multiplication can be implemented with shifters to save the cost. The calibration process of h_{e22} is similar to h_{e21} . Based on h_{e21} and h_{e22} , h_{e2} is updated by

$$h_{e2} = h_{e21} + h_{e22} \quad (6.24)$$

However, the adjustment is monodirectional based on the successive approximation discussed above. h_{e2} may keep increasing and become overlarge, so that the estimation fails. To solve it, bidirectional estimation is designed.

In order to find out an inverting estimation of h_{e2} , the effect of the comparator noise on the code frequency is analyzed. The ADC output without nonlinearity errors are described in Fig. 6.16. Since the comparator noise cannot be neglected in the operation, the code density with noise is plotted in Fig. 6.16a, where less codes appear near zero due to the threshold voltage jitter. If there is no comparator noise, the code density statistics is shown in Fig. 6.16b, where the code distribution around zero is nearly uniform. The uniform distribution of codes is used as the principle of the inverting estimation. To estimate h_{e2} , three windows are added, and the code frequency in each window are labeled d_{21} , d_{22} , and d_{23} , respectively. Besides, the width of the window, $2w$, should be as small as the comparator noise. In this situation, if the estimation is successful, codes in three windows are relativity uniform. Here, dh_2 is defined as

$$dh_2 = \begin{cases} dh_2 + \eta(d_{21} + d_{23} - 2d_{22}) & d_{21} + d_{23} > 2d_{22} \\ dh_2 - \eta & d_{21} + d_{23} \leq 2d_{22}, \end{cases} \quad (6.25)$$

where η is the step size for dh_2 , and its value is $1/2^{R_2}$ ($R_2 > 1$). Thus, h_{e2} is modified as

$$h_{e2} = h_{e21} + h_{e22} - dh_2 \quad (6.26)$$

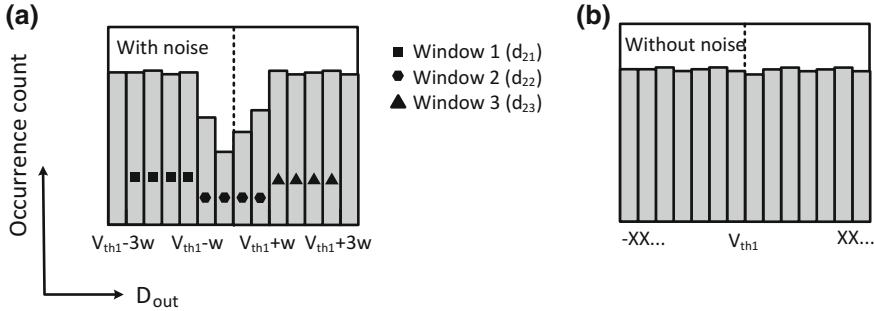


Fig. 6.16 Code density near zero with **a** noise and **b** noise compensation

When h_{e21} and h_{e22} are overlarge, dh_2 will increase and compensate for the estimation error. But dh_2 is related to σ and is usually small, so that Eq. 6.26 is only a fine adjustment. In order to speed up the convergence, another inverted estimation is added.

$$h_{e2} = h_{e21} + h_{e22} - \mu \quad dh_2 > 2\sigma \quad (6.27)$$

Thus, the bidirectional estimation is realized. The coarse h_{e2} is estimated according to Eqs. 6.23, 6.24 and 6.27. The fine estimation is operated based on Eq. 6.26 and the effect of the comparator noise is also eliminated. This method solves the single directional problem in *Max – MinEstimator* in [27].

Similarly, other h_{i1} and h_{i2} ($i = 1, 3, 4, 5, 6, 7, 8$) can be estimated and then the ADC output can be obtained by Eq. 6.20.

However, the algorithm described above is sensitive to the input signal. Therefore, the pre-judgement is introduced to skip some input candidates in case of incorrect convergence. The inputs with no distribution at the comparator threshold, the inputs with zero probability on one side of the threshold, or that with whole probability around the threshold are skipped, which can be described as

$$\begin{cases} d_{21} > K_1 \\ d_{22} > K_2 \\ d_{23} > K_3 \\ \frac{1}{K_4}d_{23} < d_{21} < K_4d_{23} \end{cases} \quad (6.28)$$

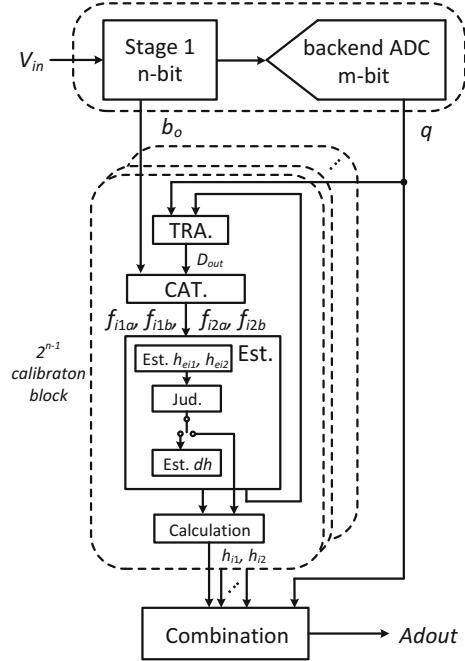
where

$$K_1 = \frac{1}{2} \frac{N}{2^{n-1}} \frac{2w}{2^m}, \quad K_2 = 0, \quad K_3 = K_1, \quad K_4 = 2 \quad (6.29)$$

The expected input candidate are codes that are relatively uniform near the comparator thresholds. Besides, a coefficient of 1/2 is added for a margin.

The calibration discussed above can be summarized in Fig. 6.17.

Fig. 6.17 An overview of the calibration algorithm



Experimental Results

The algorithm is verified by a 14-bit 150 MSps ADC, which has been shown in Fig. 6.11 and is fabricated in a 130nm 1P6M mixed-signal CMOS process. The full-scale input of the experimental ADC is $2 V_{p-p}$ and the supply voltage is 1.3 V.

To verify the blind calibration algorithm, digital outputs are input to the calibration algorithm block shown in Fig. 6.18. The statistical results are labeled $f(i)$ and $d(i)$. The process is done off-chip. Only 80 registers are needed in the calibration algorithm, to store 10 parameters, h_{en1} , h_{en2} , f_{en1a} , f_{en1b} , f_{en2a} , f_{en2b} , dh_n , d_{n1} , d_{n2} , d_{n3} . These parameters are used to estimate the steps in Fig. 6.13. Besides, counters and some simple logics are needed but no multiplier or divider digital logic is required. Therefore, the algorithm can be implemented at a low cost, which saves the hardware overhead greatly. Additionally, the analog circuit is not modified, and hence the algorithm can be integrated by ADC easily.

The measured spectrum of the ADC with the input frequency of 15.5 MHz at 150 MS/s is shown in Fig. 6.19. The results show that SNDR improves from 66.8 to 69.7 dB and SFDR improves from 78.57 to 87.3 dBc after calibration. Figure 6.20 shows the improvement of the static performance, where INL drops from 8 to 3 LSB dramatically and DNL stays about 0.6 LSB. Figure 6.21 summarizes the measured SNDR and SFDR before and after calibration versus different input frequencies. It shows that SFDR/SNDR improves by 9 dB/3 dB on average. The comparison of Nyquist rate ADC is shown in Table 6.2. The proposed calibration algorithm does

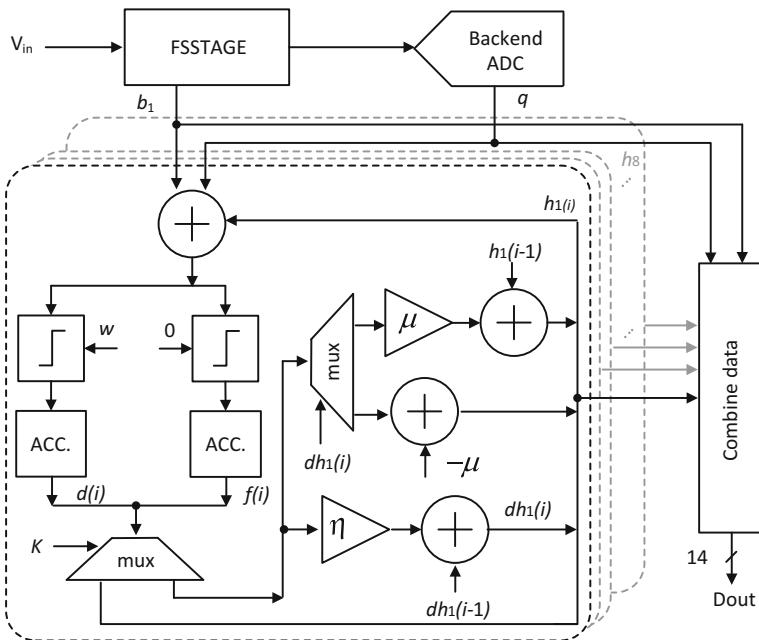


Fig. 6.18 Calibration algorithm block diagram

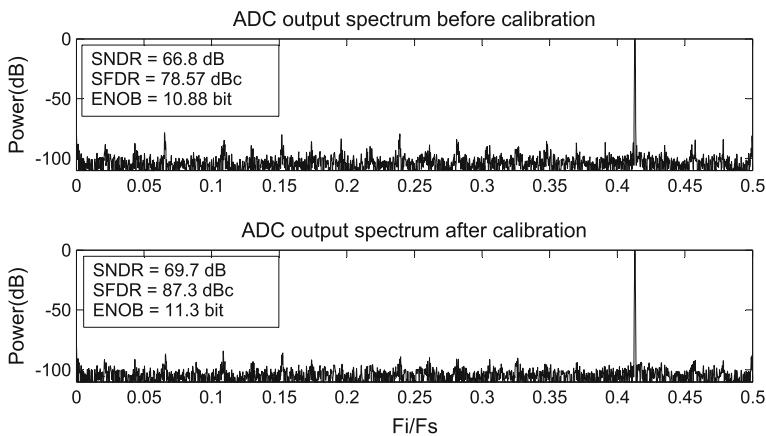


Fig. 6.19 Measured spectrum of ADC (output decimated by 4x)

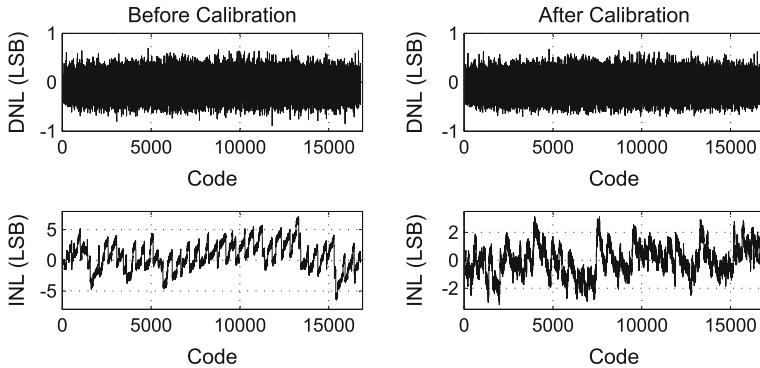


Fig. 6.20 INL and DNL errors

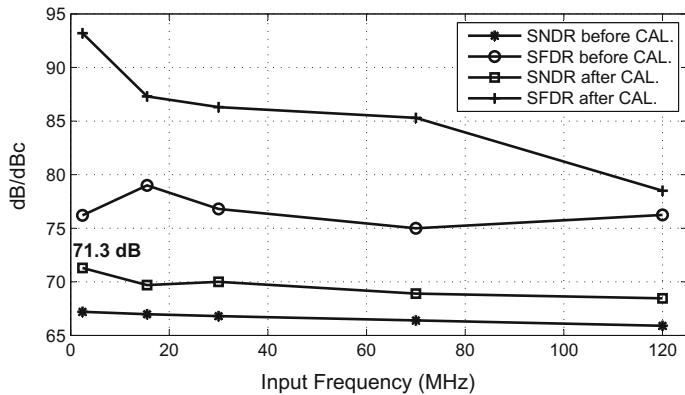


Fig. 6.21 SNDR and SFDR versus input frequency

not modify the circuits of the stages and need only 80 registers, compared with [22–24]. Besides, no multiplier or divider is needed and no iterative search is required by the proposed calibration, which makes the implementation simpler than [27].

Conclusion

A blind digital background calibration algorithm is proposed for pipelined ADC to correcting interstage gain errors and capacitor mismatches. Only 80 registers are required, and no modification is needed in analog circuits, resulting in low hardware overhead and high power efficiency. Particularly the calibration algorithm gets more robust through pre-judgment.

Table 6.2 Calibration algorithm comparison

Ref	Multiplier/Divider	RAM (Register)	Modifying Stages	Resolution
[22]	N/A	N/A	Yes	11-bit
[23]	N/A	4kX4	Yes	10-bit
[24]	N/A	128k	Yes	11-bit
[27]	Divider	N/A	No	13-bit
This Work	No	80	No	14-bit

6.4.2 Calibration of SAR ADC

While large capacitors are helpful to improve the matching accuracy in the SAR ADC, they cause ADC suffering from high power dissipation and large area. Calibration techniques enable ADC to minimize the unit capacitor and maintain high conversion accuracy and high power efficiency. One of the most straightforward methods is to adopt an additional calibration DAC, which is connected to the output of main capacitive DAC to compensate for errors in ADC conversion mode [31–33]. However, it wastes valuable conversion time to judge parameters of the calibration DAC. Therefore, they cannot be adopted in the high-speed ADC.

Two calibration techniques proposed by our research groups for high-performance and power-efficient SAR ADC are presented in this section.

6.4.2.1 Calibration with Dithering

A digital calibration technique to correct capacitor mismatches is presented in this section. The step of transfer curve is measured and the dithering method is adopted to improve the measurement accuracy by seldom modifying analog circuits [34]. The calibration technique is implemented in an 11-bit 250 MSps subranging SAR ADC. Simulated results show that the SNDR/SFDR is improved from 61.9672 dB/64.9229 dBc to 65.1233 dB/77.4320 dBc after calibration.

Basic Principle

The 11-bit subranging ADC, consisting of a 4-bit flash ADC with 1-bit redundancy for coarse conversion and 8-bit SAR ADC for fine conversion, has been discussed in Fig. 6.5. The step of the transfer curve, H_i , is derived as

$$H_i = 2\alpha C_i \quad (6.30)$$

The basic idea behind the calibration is to measure H_i in the foreground. The error of H_i is caused by the mismatch of C_i , which is called the related capacitor. The left 14 capacitors are called the unrelated capacitors. To illustrate the calibration,

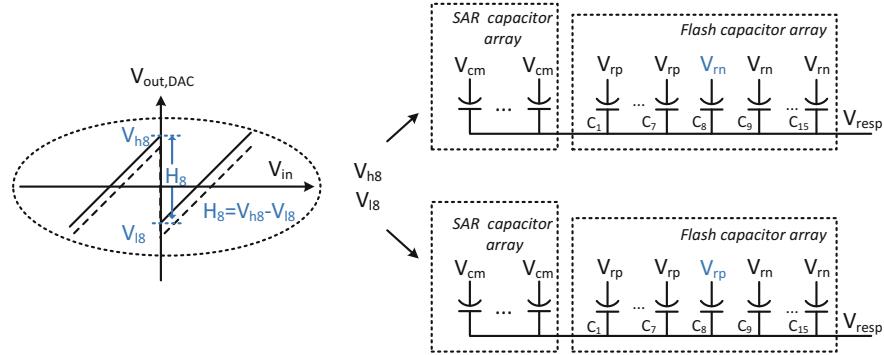
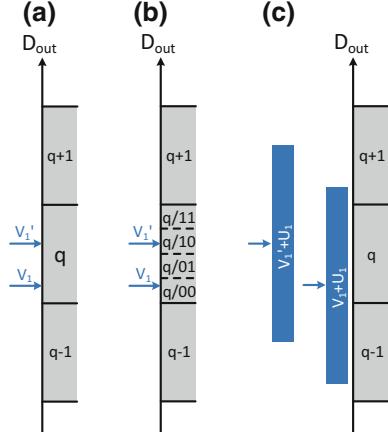


Fig. 6.22 Switching of capacitors to measure H_8 (single end is shown for simplification)

Fig. 6.23 The output versus input of **a** N -bit ADC **b** $N + 2$ bit ADC **c** N -bit ADC with dither



the measurement of H_8 is shown as an example in Fig. 6.22. Half of the unrelated capacitors attach to V_{rp} and the left 7 capacitors attach to V_{rn} . The related capacitor C_8 switches to V_{rp} to obtain V_{h8} and switches to V_{rn} to obtain V_{l8} . The difference of V_{h8} and V_{l8} is H_8 . Other steps can be similarly measured by

$$H_i = V_{hi} - V_{li} \quad (6.31)$$

The resolution of the subranging SAR ADC limits the accuracy of the calibration. An example is shown in Fig. 6.23a. The output of V_1 is code q . Taking the capacitor mismatch into account, the equivalent input shifts to V'_1 but the output is still q . In this case, the error can not be detected. To solve that, the resolution increases by 2 bit in Fig. 6.23b. The output of V_1 is code $q/00$ and the output with capacitor mismatch shifts to $q/10$. However, the additional resolution leads to more capacitors arranged in binary ratios for the SAR ADC, which increases the matching requirements of capacitors, the difficulty of layout and the power consumption.

Dithering is adopted to improve the accuracy of the calibration. In Fig. 6.23c, the analog input V_1 is added by a discrete uniform distribution, U_1 , whose expected value is 0 and the variance is $(2LSB)^2/12$ ($= LSB^2/3$). The output of $V_1 + U_1$ may be q with the probability of 0.5, $q + 1$ with the probability of x ($0 \leq x \leq 0.5$), $q + 1$ with the probability of $0.5 - x$. The output of V_1 plus a uniform distribution can be derived as

$$D_{out,V_1} = 0.5q + x(q + 1) + (0.5 - x)(q - 1) = q + 2x - 0.5 \quad (6.32)$$

An offset of $\Delta = 0.5$ is added in Eq. 6.32 to amend the digital output, which can be described as

$$D_{out,V_1} = q + 2x, \quad (6.33)$$

where q is an integer. Similarly, the output of V'_1 plus a uniform distribution can be derived as

$$D_{out,V_1} = q + 2x' \quad (6.34)$$

The output of $V'_1 + U_1$ may be $q + 1$ with the probability of x' . The outputs V'_1 and V_1 differ by adding the discrete uniform distribution, which is implemented by the dithering.

Implementation

Dithers are generated by a dither unit and injected to the output of DAC. As shown in Fig. 6.24a, the calibration block consisting of a dither unit and a pseudorandom number generator attaches to the output of the DAC by a switch sw_1 . When the calibration is operated, C_{di} ($i = 1, 2, 3$, or 4) switches to V_{cm} in the tracking phase and switches to V_{ref} or $-V_{ref}$ randomly controlled by the pseudorandom number generator. Dithers are injected to V_{res} before the first SAR conversion cycle. In order to design the capacitance in the dither unit, the response to a bottom-plate swing of ΔV is shown in Fig. 6.24b and $V_{o,d1}$ can be derived as

$$\Delta V_{o,d1} = \Delta V_{res} = \frac{C_{d0}}{C_{d0}C_t + C_{dt}(C_{d0} + C_t)} C_{d1} \Delta V_{d1} \quad (6.35)$$

where C_t is the total capacitors in the SAR and flash capacitor array and C_{dt} is the sum of C_{di} ($i = 1, 2, 3$, and 4). The response to bottom-plate swing of ΔV_{d1} , ΔV_{d2} , ΔV_{d3} and ΔV_{d4} in Fig. 6.24b is

$$\Delta V_o = \frac{C_{d0}}{C_{d0}C_t + C_{dt}(C_{d0} + C_t)} (C_{d1}\Delta V_{d1} + C_{d2}\Delta V_{d2} + C_{d3}\Delta V_{d3} + C_{d4}\Delta V_{d4}) \quad (6.36)$$

And

$$\Delta V_{o,max} = \frac{2V_{ref}C_{d0}}{C_{d0}C_t + C_{dt}(C_{d0} + C_t)} C_{dt} \quad (6.37)$$

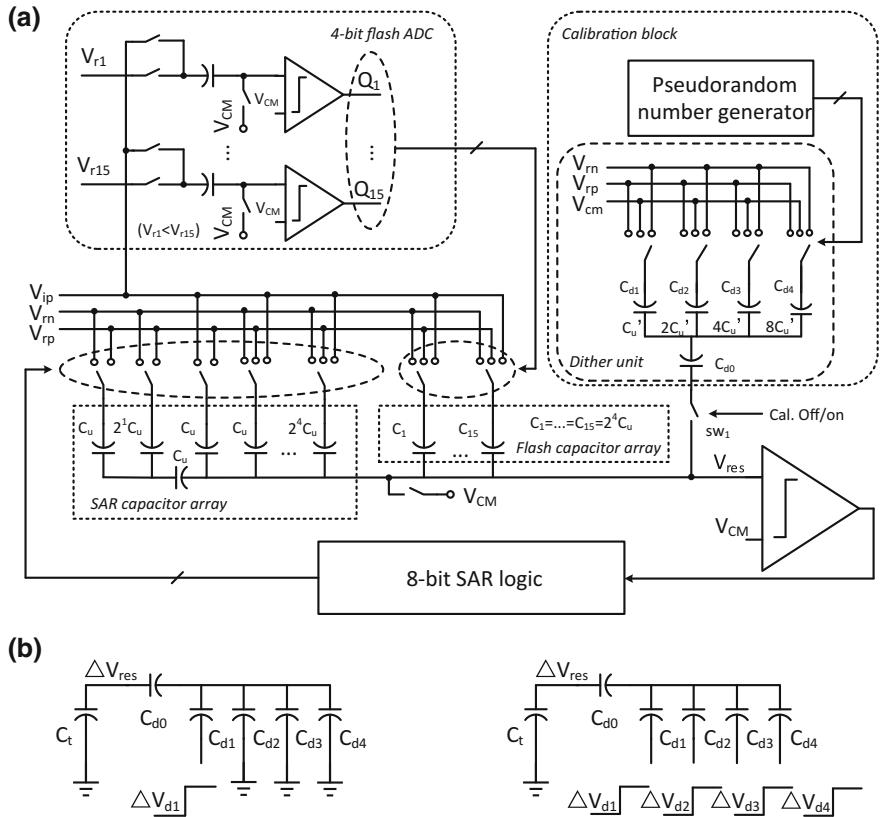


Fig. 6.24 **a** 11-b 250 MSps subranging SAR ADC with the proposed calibration (single end is shown for simplification) and **b** the response to a bottom-plate swing of ΔV

To effectively improve the accuracy of the ADC output, the amplitude of dithers should satisfy

$$\Delta V_{o,max} > 2LSB \quad (6.38)$$

Therefore, C'_u in a N -bit ADC is derived as

$$C'_u > \frac{16C_t}{15(2^{N-1} - 1)} \quad (6.39)$$

where C_{d0} is C'_u . Besides, taking the noise of the ADC into account, ΔV_o should be

$$\Delta V_o < 2V_{noise} \quad (6.40)$$

so that $V_o + V_{noise}$ is approximately under the uniform distribution.

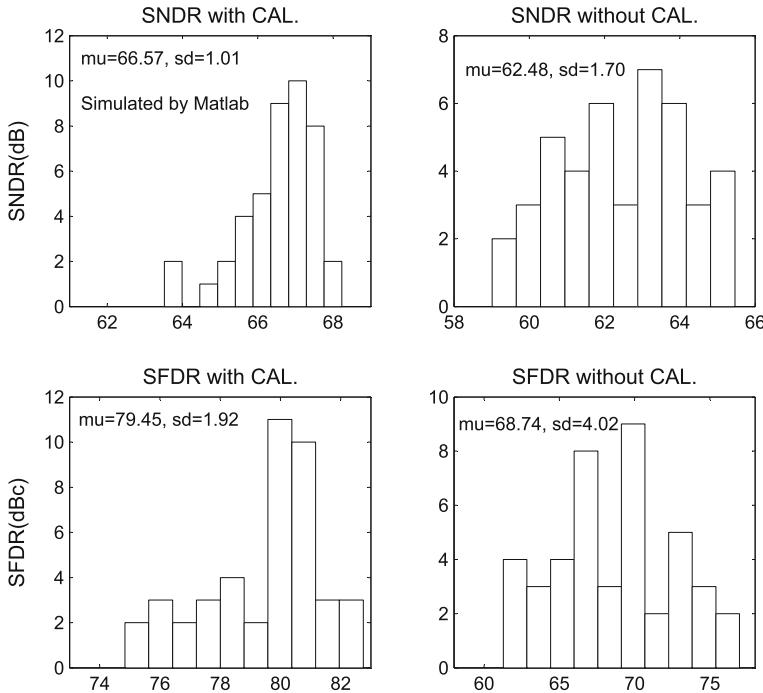


Fig. 6.25 Behavioral simulated SFDR and SNDR

Simulated Results

A behavioral model of an 11-bit 250 MSPs subranging SAR ADC is built to verify the proposed digital calibration technique in MATLAB. Since the capacitors of MSBs have larger influence on ADC, only the flash capacitors are calibrated. The variation of capacitors is assumed as the independent normal distribution with the standard deviation of 0.7%. C'_u equals C_u . Without the circuit noise in the behavioral model, V_{hi} and V_{li} ($i = 1, 2, \dots, 15$) are both calculated by averaging 8 outputs. Figure 6.25 plots the SFDR and SNDR by Monte Carlo simulations (40 times). It is indicated that the proposed calibration effectively improves the SFDR by about 14 dB and SNDR by about 10 dB. The proposed calibration improves the performance of the ADC and avoids increasing the resolution and additional power dissipation, which is attractive to the high-performance and power-efficient ADC.

6.4.2.2 Calibration Technique Based on Code Density

A foreground calibration for the capacitor mismatch in the SAR ADC is presented in this section. This calibration is based on the fact that the capacitor mismatch results in the discontinuity in the output code density [35]. It extracts the calibration

information from the digital codes and compensates for the errors in the analog domain. This technique reduces the unit capacitance and effectively improves the dynamic performances, which is verified in a 10-bit SAR ADC. Compared with the analog calibration in [31], few analog circuits, variable capacitors and switches are added instead of complex calibration DACs. Compared with the digital calibration in [36, 37], the redundant bits are removed. Reduced circuit complexity saves the power dissipation of the ADC.

ADC Architecture

A 10-bit SAR ADC adopting the proposed foreground calibration technique is shown in Fig. 6.26a. It consists of two loops, the normal SAR conversion loop and the calibration loop. The conversion loop, *loop1*, includes a comparator, a SAR logic, and a capacitive DAC. The calibration loop, *loop2*, consists of a comparator, a SAR logic, a calibration block, and calibrated variable capacitors. The calibration block based on the code density consists of a data comparator, a calibration logic block, and a signal generator. The data comparator block extracts the calibration information from the digital output of the ADC. That information drives the calibration logic to adjust the capacitors by generating the control signals, $w_d < m - 1 : 0 >$ and $Bit_EN < i >$ ($i = n - 3, n - 2 \text{ or } n - 1$). The signal generator outputs a triangular signal with a swing of V_{cal} as the input instead of V_{ip} in the calibration mode. Variable capacitors C_{n-3}, C_{n-2} and C_{n-1} are to be calibrated one by one, according to $Bit_EN < i >$. As illustrated in Fig. 6.26b, once EN_{CAL} becomes high, the calibration begins. If the calibration is completed, *Flag* becomes high, and the ADC goes into the normal conversion mode.

Calibration System Structure

In the calibration block, the data comparator block counts 8 codes and outputs the judgement signal. 8 codes are classified into two types, as is shown in Fig. 6.27a. Type I includes 100...000, 100...001, 100...010 and 100...011. Type II includes 100...100, 100...101, 100...110 and 100...111. Those two types are counted, as is shown in Fig. 6.27b. Once a counter overflows, a high level voltage is output. For example, if counter 2 overflows earlier than counter 1 does, the calibrated MSB capacitor is smaller than the expected one. To increase the MSB capacitor, G_1 and G_2 drive the calibration block in Fig. 6.28, which contains single negative pulse generators (SNPG) and registers. Signal *RDY* has two functions. On the one hand, it triggers single negative pulse generators to output R_i ($i = 0, 1, \dots, m - 1$), which generate *REST* to reset the data comparator block. On the other hand, the rising edge of signal *RDY* triggers DFFs to store the output of counter 1. DFFs output $w_d < i >$ ($i = 0, 1, \dots, m - 1$) to adjust variable capacitors. Once the last DFF is triggered, the calibration is finished and *Flag* becomes high.

It is very interesting to observe that the calibration loop is similar to the SAR conversion loop, which is illustrated in Fig. 6.29. In the conversion loop, i.e., *loop1*, the DAC's output attaches to the comparator, which drives the SAR logic to generate a series of control signals as the DAC's inputs. Similarly, in the calibration loop,

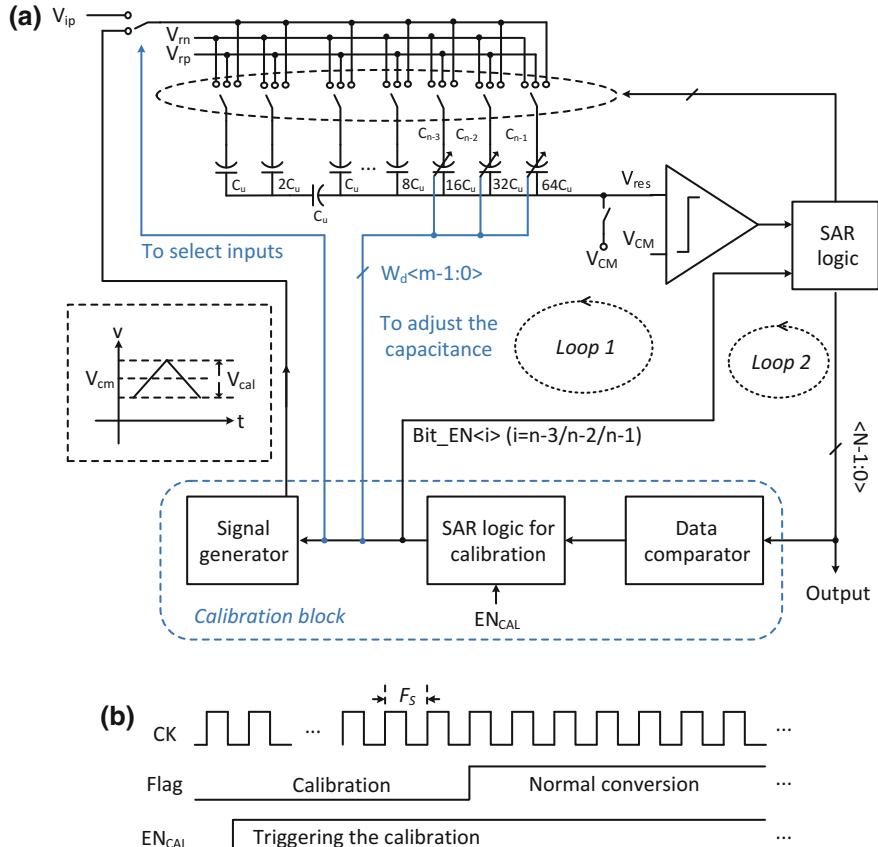


Fig. 6.26 **a** A 10-bit SAR ADC with the proposed calibration and **b** the timing diagram

i.e., *loop2*, the calibration logic utilizes the output of the data comparator, which compares the amount of two types of codes, to adjust the variable capacitors.

In the calibration mode, the input of the ADC is a triangular signal with V_{pp} of V_{cal} , which is generated by the signal generator. Parameters, V_{cal} and V_{cm} , are designed based on the two types of codes in Fig. 6.27.

As shown in Fig. 6.30, a variable capacitor is the combination of the fixed and variable parts. Take C_{n-1} as an example, it consists of a fixed capacitor and 5 binary adjustable capacitors, which can be described as

$$C_{n-1} = \sum_{i=1}^5 w_d < i > \frac{2^{i-1} C_c C_a}{2^{i-1} C_c + C_a} + 64C_u - 4\Delta C \quad (6.41)$$

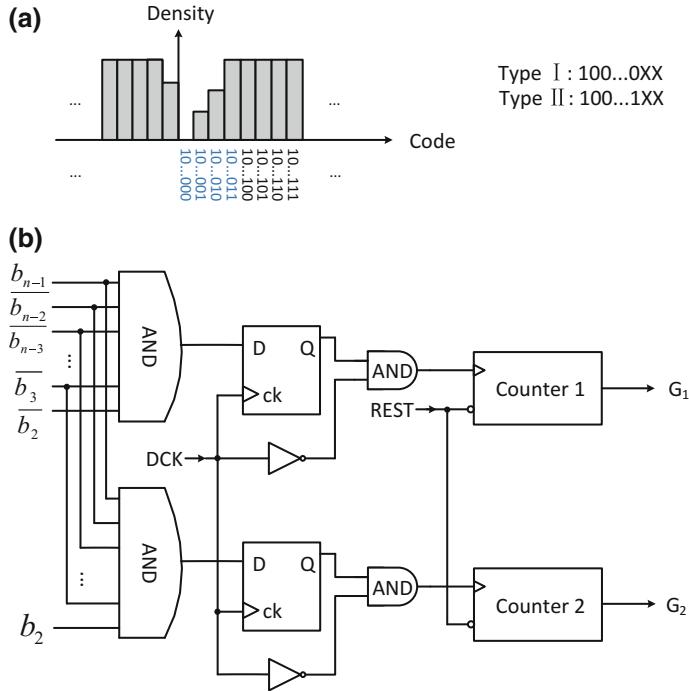


Fig. 6.27 **a** Two types of data counted and **b** the data comparator

where $w_d < i >$ ($= 0$ or 1) is generated by of the calibration block and m is 12. The maximum of the adjustable capacitor is $8\Delta C$, and thereby C_{n-1} is between $64C_u - 4\Delta C$ and $64C_u + 4\Delta C$. Besides, the default value is $64C_u$.

Simulated Results

In the 10-bit SAR ADC in Fig. 6.26, C_u is 1.4 fF, V_{cal} is 120 mV, and the differential reference voltage is 1 V. The dynamic performance simulated by Spectre is shown in Fig. 6.31. The calibration technique improves the SFDR from 54.84 to 71.17 dBc, the SNDR from 50.69 to 60.54 dB and the THD from 51.54 to 66.30 dB.

6.4.3 Calibration of Flash ADC

The flash ADC suffers from the issue of the comparator offset. And hence the calibration of the comparator offset is targeted in this section. Following the review of conventional techniques, the input offset storage technique of the dynamic comparator proposed by our research group is to be presented.

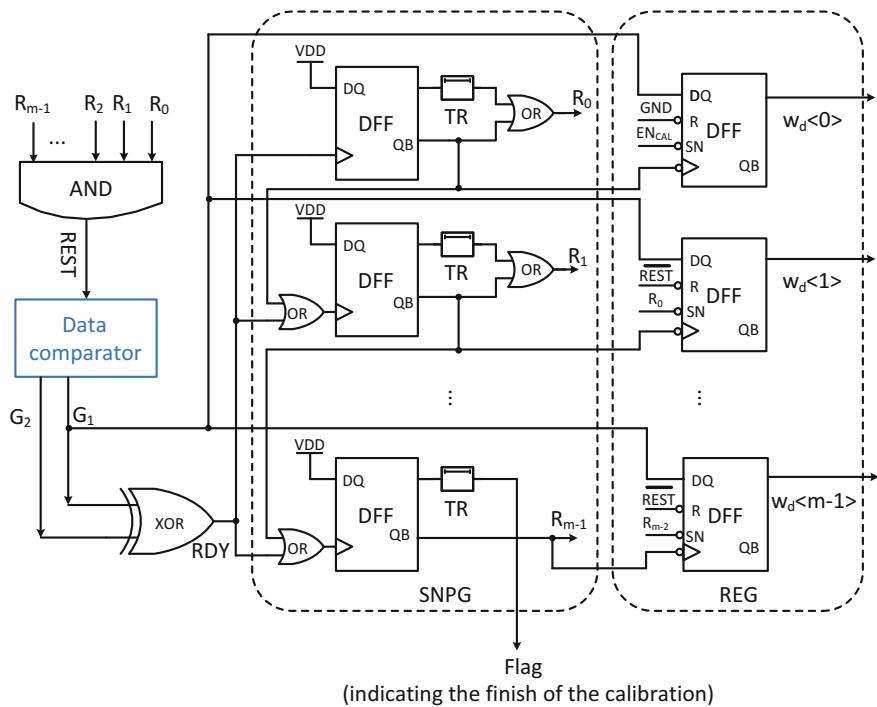
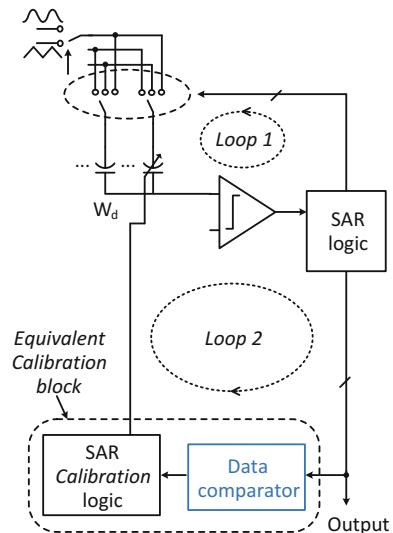


Fig. 6.28 The calibration logic

Fig. 6.29 The conversion loop and calibration loop (single end is shown for simplification)



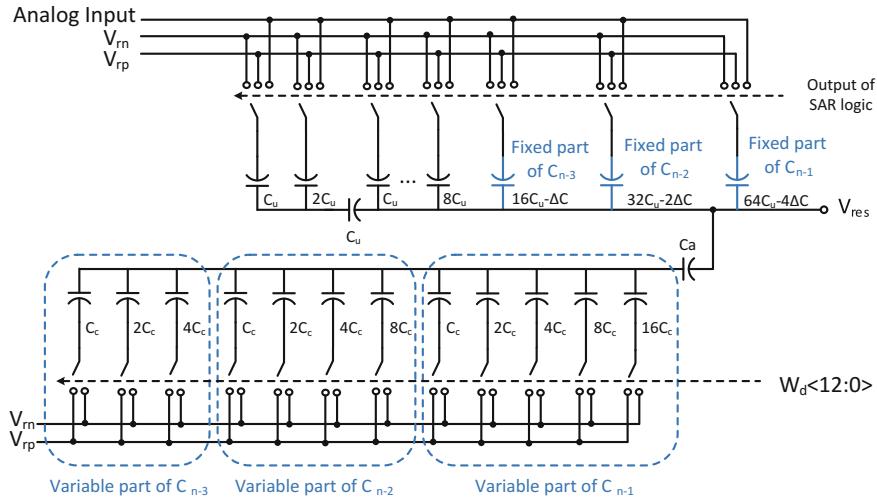


Fig. 6.30 Variable capacitors in the capacitor array

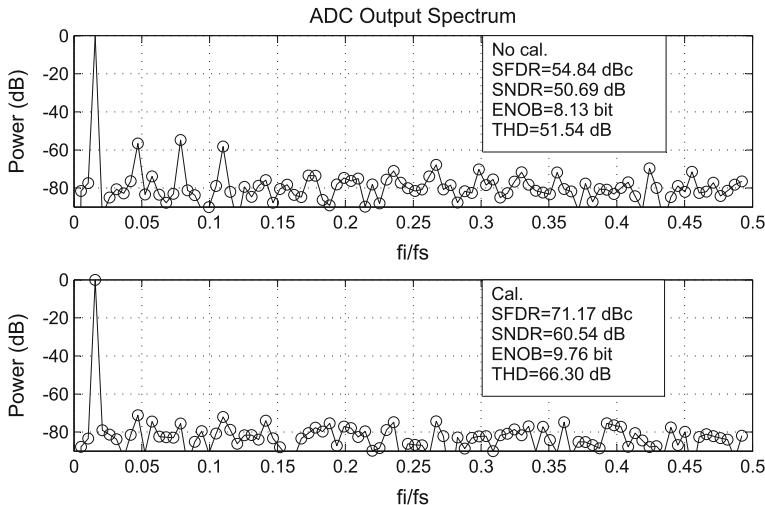


Fig. 6.31 Simulated dynamic performance of the SAR ADC

6.4.3.1 Conventional Offset Cancelation Techniques

Here are three techniques widely adopted. The principles and the limitations are discussed.

Input/Output Offset Storage Technique

The offset can be measured and stored by shorting the inputs [38], which is the basic principle of input offset storage technique and output offset storage technique.

Adopting those techniques, the additional offset cancelation phase is necessary. In the offset cancelation phase, through closing a unity gain feedback loop around the preamplifier, the input offset storage technique stores the offset on capacitors in series with the input. Likewise, the output offset storage technique stores the offset on capacitors in series with the output. Offset storage techniques are proved to be effective at a low cost. However, they can only be adopted by static pre-amplifier based comparators. Besides, the input offset storage technique introduces extra capacitors in the signal pathway, so that the parasitic of the capacitors may slow down the stability of the loop.

Comparator Reference Voltage Calibration

The comparator offset can be calibrated by adjusting the reference voltage [39, 40]. The basic idea is to determine the offset voltage, and then to use a different reference voltage to cancel the existing offset. Since this technique needs plenty of high-precision small resistances, storage cells as well as the controlling logic, it increases the design complexity.

Comparator Self-Calibration

The principle of the comparator offset self-calibration is based on Eqs. 5.11 and 5.13. The mismatch is reduced by adjusting the bias current in [41], the buck voltage in [42], the differential pair in [43–45] or the load in [46, 47]. However, high hardware overhead is needed to cancel the offset via the successive approximation.

6.4.3.2 Input Offset Storage Technique for Dynamic Comparator

While some techniques, like the offset calibration based on reference voltages and the self-calibration of the comparator, can be adopted by the dynamic comparator, the design complexity is increased. Though the conventional input offset storage techniques and output offset storage techniques are effective at a low cost, they can only be used in the static pre-amplifier based comparator.

The input offset storage technique for the dynamic comparator is proposed by our research group. To compare it with the conventional input offset storage technique, the simple blocks of static and dynamic pre-amplifiers are shown in Fig. 6.32, where both the preamplifiers work at the offset storage phase. For the static pre-amplifier in Fig. 6.32a, the offset, $V_P - V_N$, is stored in C_h through the closed loop. For the dynamic pre-amplifier in Fig. 6.32b, the additional switches controlled by $\phi 1$ enable P and N to charge and discharge. During the discharge of P and N , the offset $V_P(\phi 1) - V_N(\phi 1)$ is stored in C_h through the closed loop.

The implementation of this technique is depicted in Fig. 6.33. At the offset storage phase, the inputs attach to V_{CM} . When $\phi 2_a$ and $\phi 1_p$ are low, V_P and V_N are charged to VDD . When $\phi 2_p$ is high, the capacitors, C_h , attach to V_P and V_N and the offset storage is ready. Then, if $\phi 2_a$ becomes high, V_P and V_N start to discharge at different speeds due to the mismatch, which is recorded by capacitors. The offset storage finishes at the falling edge of $\phi 2_p$. To provide the reasonable DC operation point

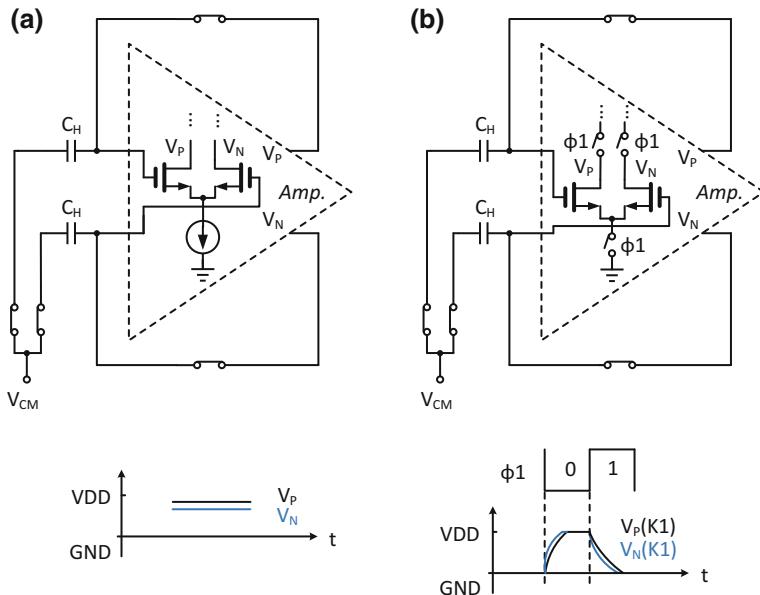


Fig. 6.32 The input offset storage in **a** static and **b** dynamic pre-amplifiers

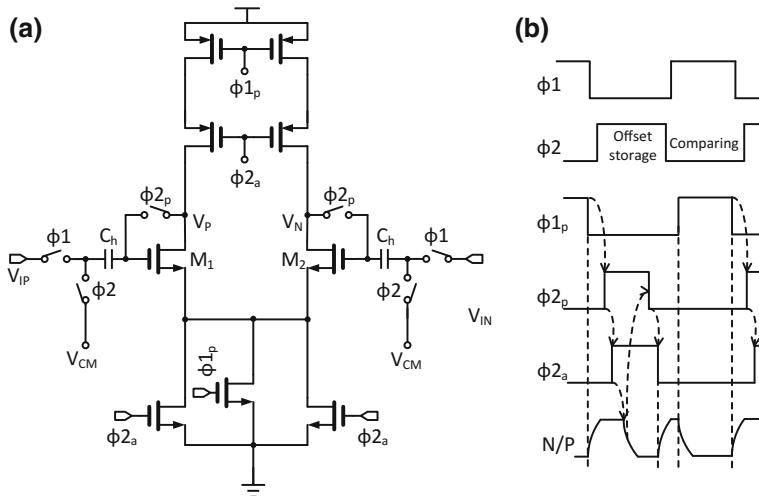
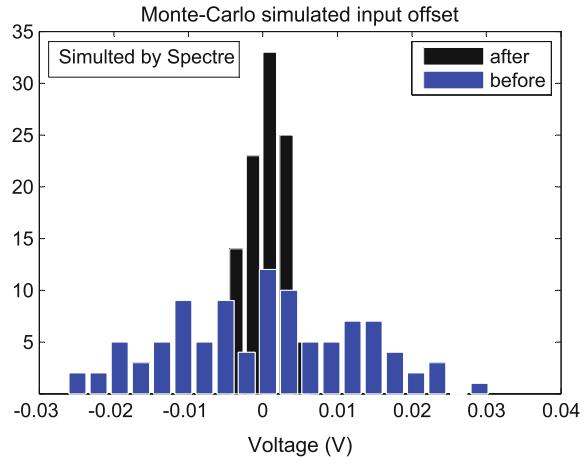


Fig. 6.33 **a** A dynamic comparator employing the input offset storage technique and **b** the timing

for M_1 and M_2 , the falling edge of $\phi 2_p$ is triggered by V_P or V_N to control the common-mode voltage of the stored V_P and V_N . At the following comparing phase, the offset of the comparator is to be canceled.

Fig. 6.34 Statistical simulation result on the input-referred offset



To verify the proposed technique, two dynamic comparators with the same architecture and size are designed. One of them adopts the input offset storage technique. Figure 6.34 shows the statistical simulation results (by 100-point Monte carlo simulation) on the input-referred offset. The 1-sigma(σ) offset voltage is reduced from 12.7 to 2.4 mV at the aid of the offset cancelation technique. The technique is proved to be effective for the dynamic comparator. Furthermore, the offset storage is completed at the resetting phase of the comparator, without additional offset cancellation cycles.

6.4.4 Calibration of Time-Interleaved ADC

6.4.4.1 Introduction

In time-interleaved ADC, mismatches between channels, mainly including offset, gain and timing mismatch, greatly limit its effective resolution. Offset and gain mismatches are relatively easy to calibrate using simple digital background calibration algorithms [48, 49]. On the contrary, timing calibration remains an active problem to explore.

Calibration of timing mismatch commonly takes two steps by turns, namely estimation and correction. Techniques to estimate timing mismatch can be broadly classified into two types: derivative-based and statistics-based.

Derivative-based technique relies on the fact that time skew creates an error in the sampled signal that is proportional to the skew with the derivative of input signal as the scaling factor. This technique is more direct, may achieve high convergence speed but at the cost of increase in hardware complexity. A case in point is [50], who uses two reference channels to obtain derivative of the input signal.

On the other hand, statistics-based technique aims at finding a statistic of the input signal that contains information of timing mismatch. Wang and Wu [51] takes samples of a common reference input, and measures timing mismatch by the difference of zero-crossing numbers between two adjacent channels. However, the reference signal generator on chip and ZC detectors may increase much hardware overhead. In [52], autocorrelation of input signal is selected for timing mismatch estimation. By maximizing autocorrelation between each channel and the reference channel, channels can achieve uniformity of sampling intervals. Compared to derivative-based counterpart, statistics-based technique has lower hardware complexity, but the statistical process may consume a longer convergence time.

As for correction, it can be carried out in either digital or analog domain. An example in digital domain is to use a cascade of FIR filters designed as differentiators [53]. By contrast, [52] corrects timing mismatch using digitally controlled delay lines (DCDL) in analog domain. Because of demand for high-order filters, digital correction obviously increases logic complexity and hardware overhead so that it may be too slow to meet the need for real-time calibration. From this perspective, analog correction is a better choice.

A novel autocorrelation-based timing mismatch calibration strategy in time-interleaved ADCs proposed by our research group is presented in this section. Compared to traditional technique [52], the proposed strategy lets autocorrelation between each channel and the reference channel converge to one of the channels with a certain time interval away from the reference channel. It aims at elevating convergence speed against $|R'(\tau)|$ decrease.

6.4.4.2 An Autocorrelation-Based Timing Calibration Strategy

This section presents a novel autocorrelation-based strategy for timing mismatch calibration in time-interleaved ADCs. Different from traditional technique, the proposed strategy does not let autocorrelation between each channel and the reference channel converge to the peak, but to one of the channels with a certain time interval away from the reference channel [54]. It can accelerate convergence. The interval can be selected with much freedom and easily implemented. Representation of channel-ADC output can be only 1-bit without a “dead zone”, thus it can further reduce hardware overhead. It is also independent from offset and gain calibration. Using the proposed strategy in a 2-channel 14-bit 500MS/s time-interleaved ADC, simulation shows a convergence time of 192ms to $0.1\%T_s$ accuracy under 212.4 MHz input and initial $5\%T_s$ timing mismatch.

System Model

A background calibration system attached to a 2-channel 14-bit 500 MSps TI ADC is proposed in Fig. 6.35. During each sampling period, there are two ADCs, one channel-ADC and a reference channel (one-bit), sampling and converting the input signal at almost the same time. Clocks are generated from an external 500 MHz source. All clocks go through a DCDL to their destinations.

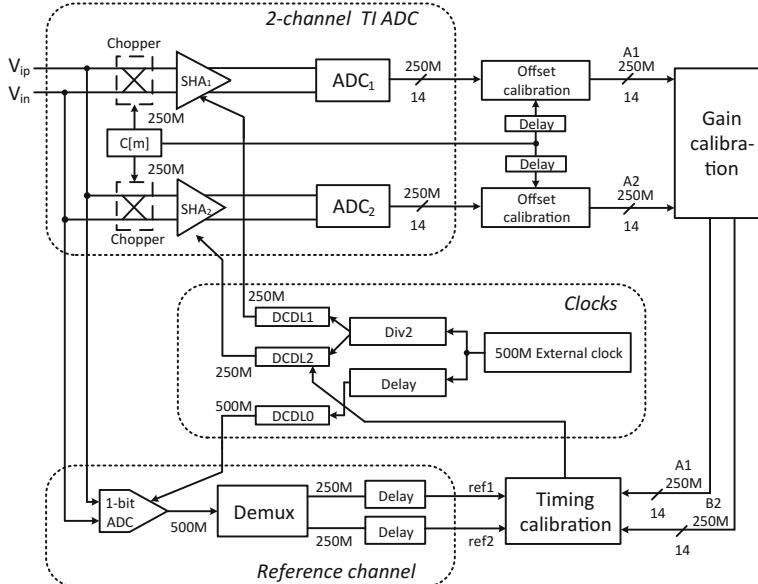


Fig. 6.35 The calibration in a 2-channel 14-bit 500MS/s TI ADC

The offset calibration relies on LMS algorithm to estimate the channel offset, with random chopper to protect original DC component of the input [48].

$$OS_i[n + 1] = OS_i[n] + \mu_{os}(y_i[n] - OS_i[n]) \quad (6.42)$$

where μ_{os} is the iteration factor. Then deducted and chopped-back channel outputs A_1 and A_2 are obtained.

The gain calibration also relies on LMS algorithm to estimate the channel gain, similarly to [49].

$$G_i[n + 1] = G_i[n] + \mu_g(|y_i[n]| - G_i[n]|y_i[n]|), \quad (6.43)$$

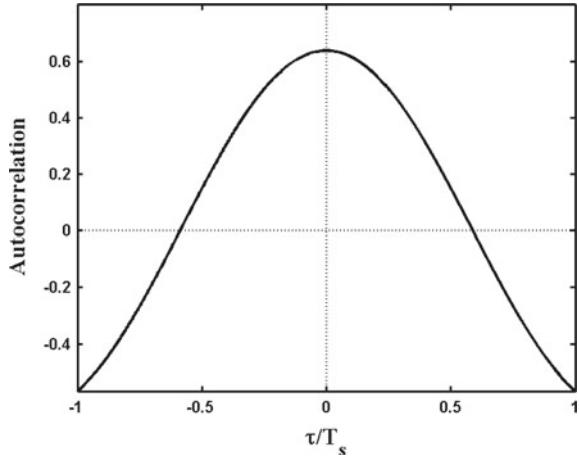
where μ_g is the iteration factor. Then multiplied channel output B_2 is obtained.

What should be noticed in both the offset and gain calibration is the case when $f_{in} = f_s/4$. One channel always picks the peak (positive or negative), while the other always picks zero, leading to the failure of calibration. However, with a simple filter $1 + z^{-1}$ [49], this problem can be easily solved.

Basic Principle

The idea of proposed strategy comes from the inquiry to autocorrelation between channel-ADCs and the reference channel. The autocorrelation can be calculated by two typical types of representation of channel-ADCs, full representation and 1-bit representation.

Fig. 6.36 The autocorrelation with full representation of channel-ADC



1. The output of the channel-ADC is considered as the copy of analog input. For a sinusoidal input with the unit amplitude,

$$\begin{aligned}
 R(\tau_i) &= E\{\text{sgn}(\sin \omega t + OS_r) \cdot [(1 + \Delta G_i) \sin \omega(t + \tau_i) + OS_i]\} \\
 &= \frac{2OS_i \arcsin OS_r}{\pi} + \frac{1 + \Delta G_i}{\pi} [\cos(\omega\tau_i + \arcsin OS_r) + \cos(\omega\tau_i - \arcsin OS_r)]
 \end{aligned} \tag{6.44}$$

where OS_r and OS_i are offsets of the reference channel and channel-ADC, and $(1 + \Delta G_i)$ and τ_i are the gain and time skew of channel-ADC. Figure 6.36 shows $R(\tau_i)$ is an even function and decreases with the increase of $|\tau_i|$. Traditional technique [52] lets autocorrelation between each channel and the reference channel converge to the peak (Fig. 6.37a). However, $|R'(\tau_i)|$ becomes very small when $|\tau_i|$ approaches 0, so that the convergence becomes slower and slower. Conversely, $|R'(\tau_i)|$ increases when $|\tau_i|$ departs a little from 0. For a micro $\Delta\tau$, larger $|R'(\tau_i)|$ provides larger ΔR for the correction, so that the convergence is accelerated. Therefore, a new strategy is proposed, which lets the autocorrelation converge to one of the channels (e.g., channel₁) with a certain time interval (τ_1) away from the reference channel (Fig. 6.37b).

2. For further simplification, the 1-bit representation of channel-ADC is utilized to calculate the autocorrelation (Fig. 6.39). For a sinusoidal input with unit amplitude,

$$\begin{aligned}
 R(\tau_i) &= E\{\text{sgn}(\sin \omega t + OS_r) \cdot \text{sgn}[(1 + \Delta G_i) \sin \omega(t + \tau_i) + OS_i]\} \\
 &= 1 - 2f \cdot [| \tau_i + \frac{\arcsin OS_i - \arcsin OS_r}{1 + \Delta G_i} | + |\tau_i - \frac{\arcsin OS_r - \arcsin OS_i}{1 + \Delta G_i}|]
 \end{aligned} \tag{6.45}$$

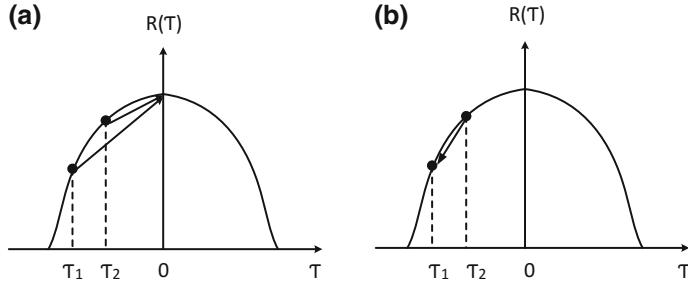
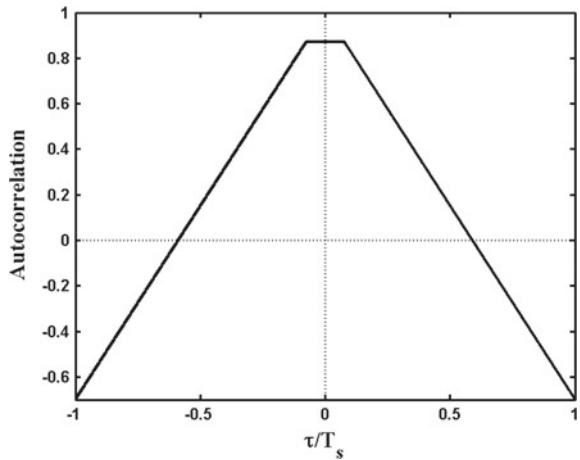


Fig. 6.37 The timing calibration of **a** traditional technique and **b** proposed strategy

Fig. 6.38 Autocorrelation with 1-bit representation of channel-ADC



When $|\tau_i| \leq |\left(\arcsin OS_r - \frac{\arcsin OS_i}{1 + \Delta G_i}\right) / \omega|$, $R(\tau_i)$ is flat (Fig. 6.38), without a unique peak that the traditional technique can converge to, which agrees with [55]. “Dead zone” occurs when the flat region is wider than the given accuracy, which leads to the restriction on OS_r and the additional offset calibration. However, the proposed strategy can easily avoid it just by setting $|\tau_1|$ bigger than the flat region, then $R(\tau_i) \approx 1 - 4f \cdot |\tau_i|$

$$\Delta R = R(\tau_1) - R(\tau_2) \approx 4f \cdot (|\tau_2| - |\tau_1|) = 4f \cdot \Delta \tau \quad (6.46)$$

This is an attractive result, for the timing calibration is independent from the offset and gain calibration, and the offset calibration of the reference channel is no longer needed. Moreover, $|\tau_1|$ can be selected with much freedom, for the convergence speed under the same input frequency is nearly the same.

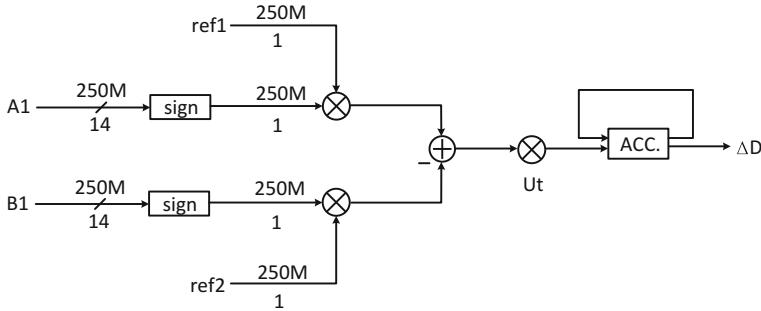


Fig. 6.39 The timing calibration in a 2-channel time-interleaved ADC

Implementation

As Fig. 6.39 shows, outputs of channel-ADCs and the reference channel are sent to the timing calibration module to drive DCDL to equalize sampling intervals. Like the offset and gain mismatch, the timing mismatch can also be calibrated by LMS algorithm. Let all channel-ADCs take samples a little ahead of the reference channel,

$$D_i[n] = D_i[0] + \text{floor}\{\mu_t \sum_{k=1}^{M_i[n]} (P_i[k] - P_i[k])\}, \quad (6.47)$$

where D_i is the control code of DCDL_i , μ_t is the iteration factor, and P_i is the product of sign of channel_i and the reference channel. Till $M_i[n]$ samples are collected, $D_i[n-1]$ are updated to another integer, $D_i[n]$, according to Eq. 6.47.

Control code of DCDL decides the number of delay cells attached to control the delay time. Letting all channel-ADCs take samples ahead of the reference channel is under the consideration that the direction of correction should not be ambiguous. In fact, letting all channel-ADCs take samples behind of the reference channel is also acceptable, but the direction of correction in (6.47) needs to be inverted. However, the reference channel a little ahead may blur the sampling of successive channel-ADC. Therefore, the former is better. To implement all channel-ADCs ahead, the control code of DCDL for the reference channel is set to the maximum and the control code of all channel-ADCs is initially set at the middle.

Simulation Results

For a 2-channel 14-bit 500MS/s TI ADC with 2 V full-scale, a sinusoidal signal ($f \approx 212.4$ MHz, -1 dBFS) with the gaussian noise ($\sigma = 0.144$ mV) is given as the input. Control code of DCDL_2 is updated according to Eq. 6.47. The accuracy of DCDL (one step) is $0.1\%T_s$, the maximum control code is 255, and the control code of the reference channel can be set at 255. Suppose initial $\Delta\tau = 5\%T_s$.

When using the full representation of channel-ADC output, $\mu_t = 2^{-32}$, the relationship between convergence cycles and $|\tau_1|$ is shown in Fig. 6.40. Convergence

Fig. 6.40 Convergence cycles at different $|\tau_1|$ with full representation

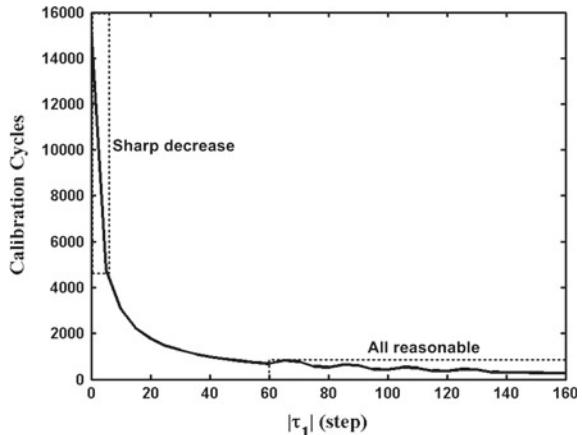
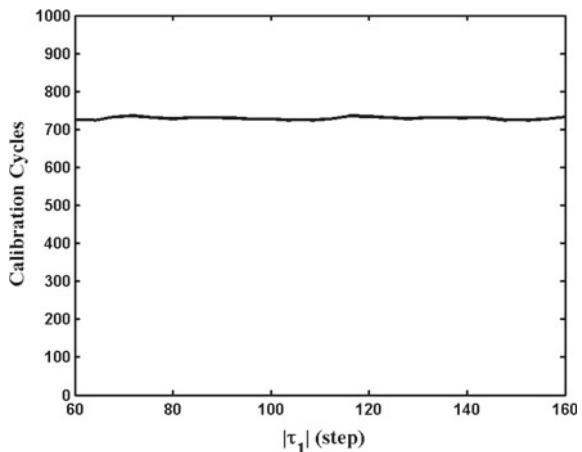


Fig. 6.41 Convergence cycles at different $|\tau_1|$ with 1-bit representation



cycles are measured with a unit called calibration cycle, which consists of 2^{17} samples. Convergence cycles go through a sharp decrease when $|\tau_1|$ increases from 0 to 5 steps, then become stable after about 60 steps, which is less than 1/20 of the cycles needed when $\tau_1 = 0$ (adopted in the traditional technique)!

When reducing the representation of channel-ADC output to 1-bit code, μ_t can be lifted to 2^{-24} because the correction is more smooth. Supposing $OS_r = 0.01$, the relationship between convergence cycles and $|\tau_1|$ is shown in Fig. 6.41. Convergence cycles stay almost unchanged in a wide range just as expected.

Setting $|\tau_1| = 128$ steps, the convergence process using the proposed strategy is shown in Fig. 6.42. It takes about 730 calibration cycles (i.e., 2^{26} samples, 192 ms) to finish the calibration and the SNDR reaches 72.4 dB.

However, when $OS_r = 0.01$, supposing the channel offset $OS_2 = 0.001$, the gain mismatch $\Delta G_2 = 0.002$, there is a “dead zone” of $3.35\%T_s$, much wider than the

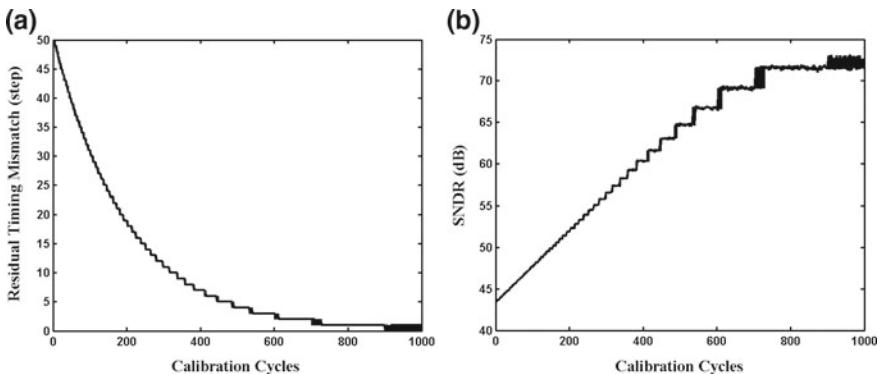


Fig. 6.42 The convergence process using the proposed strategy including **a** the residual timing mismatch and **b** the SNDR

given accuracy (i.e., $0.1\%T_s$). The traditional technique cannot calibrate the accuracy without the offset calibration of the reference channel. However, because of $|\tau_1| = 12.8\%T_s > 3.35\%T_s$, the proposed strategy can still reach the given accuracy. As a result, it is more suitable for high-accuracy applications.

Conclusion

This section presents a novel autocorrelation-based strategy to calibrate the timing mismatch in time-interleaved ADCs. Unlike the traditional technique, the proposed strategy lets the autocorrelation between each channel and the reference channel converge to one of the channels with a certain time interval away from the reference channel. The interval can be selected with much freedom, and easily implemented. The proposed strategy speeds up the convergence, further reduces hardware overhead, and is more widely applicable in high-performance time-interleaved ADCs.

6.5 Summing up

With the ease of analog design, improved linearity, and reduced power dissipation, calibration techniques have attracted more and more attentions. Especially, the process-friendly digital calibration techniques, which do not need manual modifications or extra analog circuits, greatly interest designers. That is why the chapter is created.

First, the main source errors in ADCs with different architectures are discussed, including the causes and their impacts.

Second, the chapter talks about the basic principle of the calibration algorithm, which is the basis behind various calibration techniques.

Thirdly, the calibration techniques proposed by our research group are discussed in detail. For the pipelined ADC, a blind background calibration algorithm to correct

the interstage gain error and capacitor mismatch is proposed. For the SAR ADC, two techniques are introduced to calibrate the capacitor mismatch. For the flash ADC, the input offset storage technique for the dynamic comparator is presented to cancel the offset voltage. For the time-interleaved ADC, an autocorrelation-based timing mismatch calibration strategy is proposed.

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Chapter 7

Design Case

7.1 Introduction

High performance analog-to-digital converter (ADC) is required in modern communication systems. In a radio receiver in the base station, the connectivity (WLAN, WiMAX, etc.) applications, etc., the high data rate and the large dynamic range imply the high conversion rate and the high linearity of the ADC. The pipelined ADC is a popular architecture for high-speed and high-resolution data conversion. High conversion rate, low power, and compatibility with low-voltage and aggressive device-scaling CMOS technology have become the important metrics in state-of-the-art designs. To reduce the power dissipation of the high performance pipelined ADC, low-power techniques have been proposed, such as opamp and capacitor sharing [1], range scaling [2], sample-and-hold amplifier (SHA) less [3] and digital background calibration [4, 5].

Although the SHA and the first multiplying digital-to-analog converter (MDAC) are merged in [1], the SHA still contributes a considerable part of noise. This work removes the dedicated SHA and merges the first MDAC (MDAC1) and the second MDAC (MDAC2) to lower the power and the noise. Range-scaling technique is also used to address the issue of the low power supply. A blind calibration is proposed to correct linearity errors. A 14-bit 150 MSps prototype ADC is implemented in 130 nm CMOS. This ADC can provide the high dynamic performance for the input above the nyquist frequency and consumes only 85 mW.

The organization of this section is as follows. Section 7.2 briefly introduces the architecture. Section 7.3 describes FSTAGE and highlights the differences between the conventional opamp and capacitor-sharing stage and FSSTAGE. Section 7.4 presents the proposed blind calibration. Section 7.5 describes the circuit implementation. Section 7.6 gives the measurement results and design efforts are concluded in Sect. 7.7.

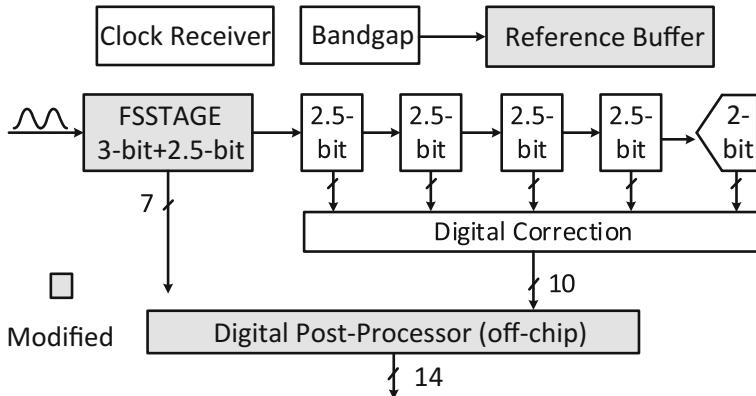


Fig. 7.1 ADC architecture

7.2 ADC Architecture

Figure 7.1 shows the proposed ADC architecture. The pipeline core is partitioned by a FSSTAGE, followed by four stages, each resolving two bits effectively, and finally, a 2-bit flash ADC. A 3-bit first stage and a 2.5-bit second stage are merged as a single stage named by FSSTAGE. The clock receiver converts the sine signal into a low jitter sampling clock. The bandgap and the reference buffer are also integrated on chip. Besides, a blind calibration algorithm is proposed to correct linearity errors.

The key modifications of this work are the replacement of the traditional stage 1 and 2 with the power-efficient FSSTAGE, the use of a level-shifter-aided reference buffer and the addition of an off-chip digital postprocessor. Conceptually, the proposed FSSTAGE can be extended to multiple pipelined stages to reduce the power further. For simplicity, only the first and second stages are converted to power-efficient stage in this demonstration vehicle.

7.3 FSSTAGE

To optimize the power and the noise, the opamp and the feedback capacitors of MDAC1 are shared between MDAC1 and MDAC2, the SHA is removed and the residue gain of MDAC1 is reduced by half. Combining those techniques, MDAC1 and MDAC2 are merged in FSSTAGE [6].

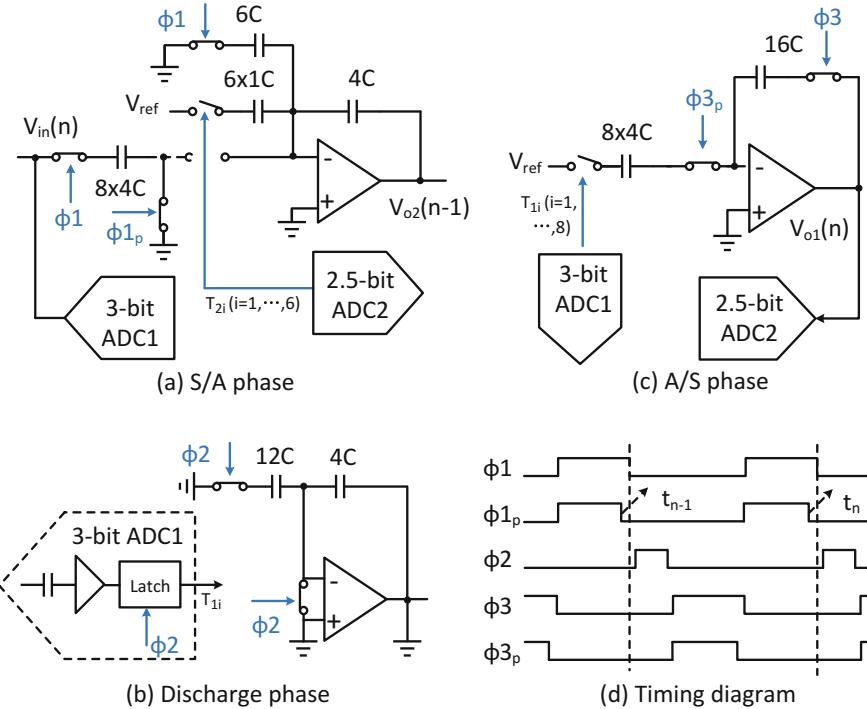


Fig. 7.2 FSSTAGE with **a** S/A phase **b** discharge phase **c** A/S phase **d** timing diagram

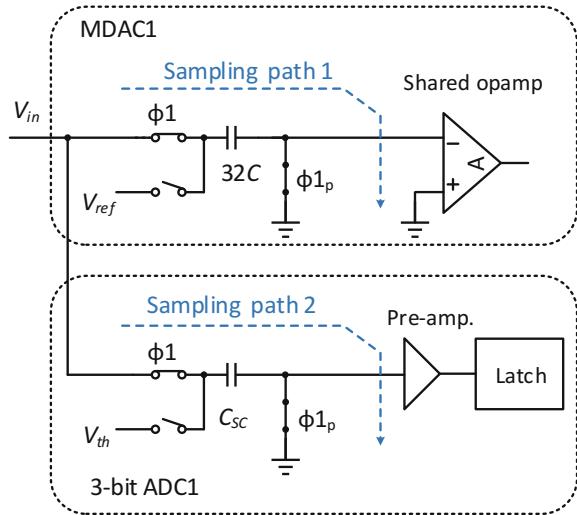
7.3.1 Opamp and Capacitor Sharing

The proposed FSSTAGE is described in Fig. 7.2 in detail. It works with three clock phases: sample/amplification (S/A) phase, discharge phase, and amplification/sample (A/S) phase. The S/A phase means that the first/second stage works in sampling/amplification phase, and vice versa. The chip area is saved and the opamp load is reduced by about 40 to 60% compared with that of a conventional stage. The memory effect in A/S phase is effectively reduced because of discharge phase. And the error caused by the memory effect between A/S and S/A phase is 25% smaller than that of a conventional SC amplifier [1].

7.3.2 SHA Less

The SHA is removed to reduce the power and the noise. To reduce the aperture error introduced by SHA less, high-bandwidth pre-amplifier can be adopted in sub-ADC to track the high-frequency input [3]. However, the power-hungry pre-amplifier is

Fig. 7.3 Sampling paths in sub-ADC and MDAC (single-ended circuit for simplicity)



not expected by the low-power design. In this work, matching sampling paths and reusing discharge phase address this issue. In Fig. 7.3, the sampling path 1 and path 2 sample the analog input and are both controlled by $\phi 1$ and $\phi 1_p$. Bandwidth matching between the two sampling paths enables the high-frequency input. After sampling, 3-bit flash ADC finds the voltage differences between the sampled input and thresholds, amplifies them and finally latches at the falling edge of $\phi 2$. At the same time, the capacitors of MDAC2 discharge to eliminate the memory effect in Fig. 7.2b. $\phi 2$ phase is necessary in sub-ADC and it is reused by discharging in FSSTAGE. The conversion rate does not suffer from the additional discharge phase.

7.3.3 Range Scaling

Range scaling reduces the residue gain to allow for a better linearity at the opamp output and increases the feedback factor to enlarge both loop gain and bandwidth. However, the drawback lies in the following stage design, for example, the scaled-down reference voltage required [2]. In this work, the residue gain is scaled to a half of the nominal (from 4x to 2x). Capacitor C_1 , in Fig. 7.2, is introduced to maintain a fixed full-scale reference voltage. The output of MDAC2 is

$$v_{o2}(n - 1) = 4V_{o1}(n - 1) - \frac{1}{2} \sum_{i=1}^6 T_{2i} \frac{V_{ref}}{2}, \quad (7.1)$$

where $V_{o1}(n - 1)$ is the residue voltage of MDAC1, and T_{2i} ($i=1$ to 6) are the thermometer codes of 2.5-bit flash ADC. The equivalent reference is $V_{ref}/2$ with the aid of C_1 .

Compared with [1], FSSTAGTE further introduces SHA less to reduce the power and the noise, and reuses the discharge phase $\phi 2$ to avoid the shrink of the conversion rate. In result, both the power and the noise are optimized without reducing the speed, and the power consumption of the analog front end can be reduced nearly by half for the same SNR. In addition, the proposed FSSTAGTE is better than [1] for the low supply application due to range scaling.

7.4 Blind Background Calibration

A digital background calibration algorithm [7], is proposed to correct linearity errors caused by capacitor mismatch and environment-sensitive finite opamp gain. The particularly interesting property of the calibration technique is that no special calibration signal or system stoppage is required and it does not modify the pipelined stages. Based on the analysis of the density of output codes, the algorithm extracts the calibration information and corrects the output. The details of the calibration is discussed in Sect. 6.4.1.

7.5 Circuit Implementation

7.5.1 Single-Stage Opamp

As is mentioned above, the residue voltage of inter-stage is limited to $\pm 0.25V_{ref}$. For example, for a $2-V_{pp}$ input signal, the output swing of the opamp is expected to be ± 0.25 V and less than ± 0.5 V. Hence a folded-cascode opamp can satisfy the output swing requirement even at a 1.3-V supply voltage. The gain-boosting technique is introduced to enhance DC gain. The opamp is shown in Fig. 7.4. Due to its high DC gain and large output swing, the inter-stage nonlinearity is negligible, so the calibration of ADC can be simplified. When $\phi 2$ is high, the opamp is reset with the input terminals connected to the input common mode voltage and the output terminals shorted together. The output terminals of the AP amplifier and the AN amplifier are also shorted. In addition, the output common mode voltage is set to half of VDD to maximize the output swing.

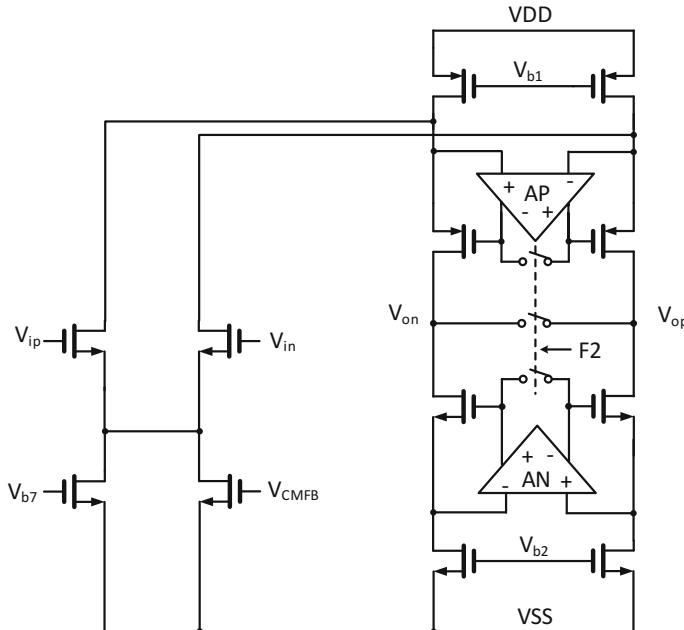


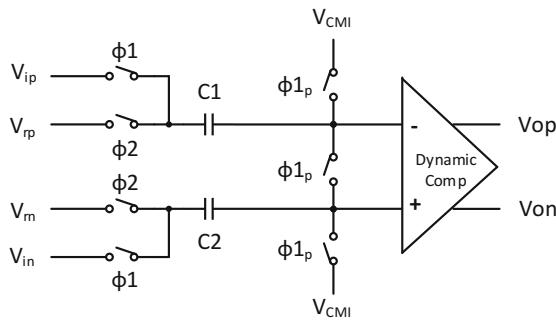
Fig. 7.4 The folded-cascode gain-boosting opamp

7.5.2 Level-Shifter-Aided Reference Buffer

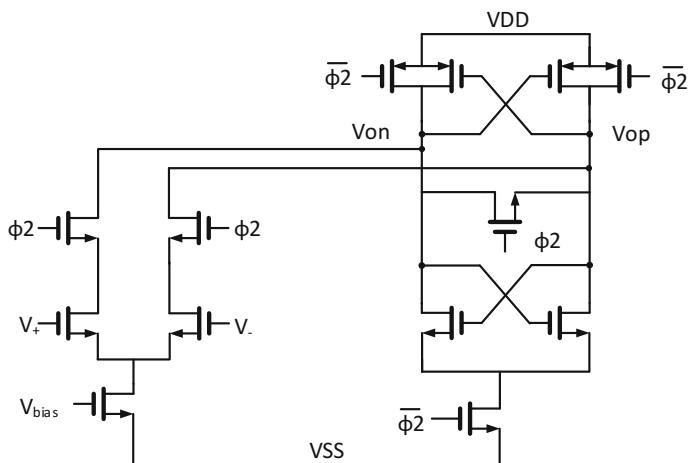
A fully integrated high-speed reference buffer is adopted, as is shown in Fig. 3.4. It has an open-loop *Buffer Branch* driven by slow negative feedback loops. A level shifter is used to increase the output swing, as large as $VDD - V_{ov31} - V_{ov33}$, where V_{ov31} and V_{ov33} are the overdrive voltages of M_{31} and M_{33} . To achieve the high bandwidth without increasing the power, NMOS-only *Buffer Branch* is used. Compared with PMOS, NMOS can provide the same transconductance with smaller parasitic capacitance. NMOS-only buffer can achieve larger bandwidth than NMOS-PMOS mixed buffer [8] under the same bias current. The details of the reference buffer is discussed in Sect. 3.3.1.

7.5.3 Comparators

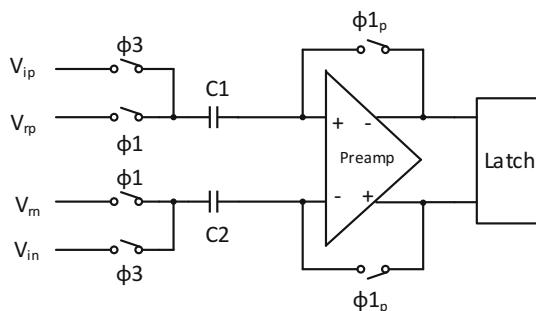
Because of 1-bit redundancy, the max comparator offset voltage to tolerate in MDAC1 is $\pm V_{ref}/8$, so a high-speed comparator is chosen shown in Fig. 7.5a. To minimize the aperture error, the switch-capacitor sampling path is designed to match that of MDAC1. Figure 7.5b presents the implementation of the dynamic comparator. It has



(a) Comparator for the 3-bit flash ADC



(b) Dynamic comparator



(c) Comparator for 2.5-bit flash ADC

Fig. 7.5 The proposed comparators

a large open-loop bandwidth to finish settling within 600 ps. However, it only works in ϕ_2 , resulting in the average current about 60 μ A.

The max comparator offset voltage to tolerate in MDAC2 is reduced to $\pm V_{ref}/16$ due to the half-gain range scaling. So an offset cancelation comparator is chosen, as shown in Fig. 7.5c.

7.5.4 Clock Receiver

A low noise clock receiver is designed, which has two differential amplifiers and a differential to single-ended amplifier in cascade. It outputs a sampling clock with steep falling edge and low jitter. For a 150 MHz $1-V_{pp}$ sine input, the RMS jitter is about 200 fs.

7.6 Measurement Results and Comparisons

The chip micrograph of the prototype ADC is shown in Fig. 7.6. It is fabricated in a 130 nm 1P6M mixed-signal CMOS process. The total area including pads is 4.4 mm² with ADC core of 1 mm². The total power consumption is 85 mW at 150 MS/s from a 1.3-V supply (excluding LVDS IO drivers), including 11 mW for the clock receiver and 17 mW for the on-chip reference buffer. The ADC core consumes only about 57 mW. This prototype ADC accepts a full-scale input signal of $2-V_{p-p}$. Figure 7.7 presents the measured output FFT spectrum with 15.5 MHz input. The SNDR is 66.8/69.7 dB and the SFDR is 78.6/87.3 dBc before/after calibration. Figure 7.8 summarizes the measured SNDR and SFDR versus input frequency. The SNDR is 71.3 dB with a 2.4 MHz input and remains 68.5 dB for a 120 MHz input, showing excellent dynamic performance at the high input frequency. Figure 7.9 shows the maximum and minimum residue voltage of MDAC1 in digital code. They vary no more than 100 LSB from low frequency to 810 MHz, which demonstrates very small aperture error. Figure 7.10 describes the DNL/INL plot and the peak DNL is 0.6 LSB. Table 7.1 shows the comparison with recently published high performance ADCs. For a fair comparison, only ADCs with the ENOB up to 11-bit and the sampling rate up to 100 MSps in CMOS are listed. FoM is defined as $power/(2^{ENOB_{DC}} F_s)$. The prototype ADC achieves FoM of 151 fJ/step, achieving the lowest FoM.

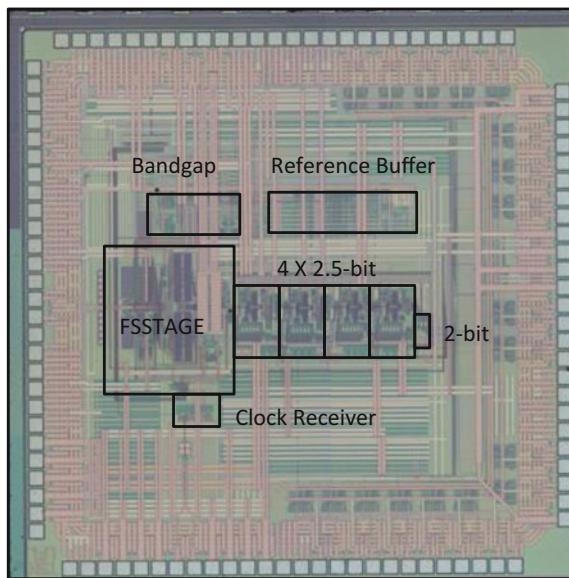


Fig. 7.6 Chip micrograph

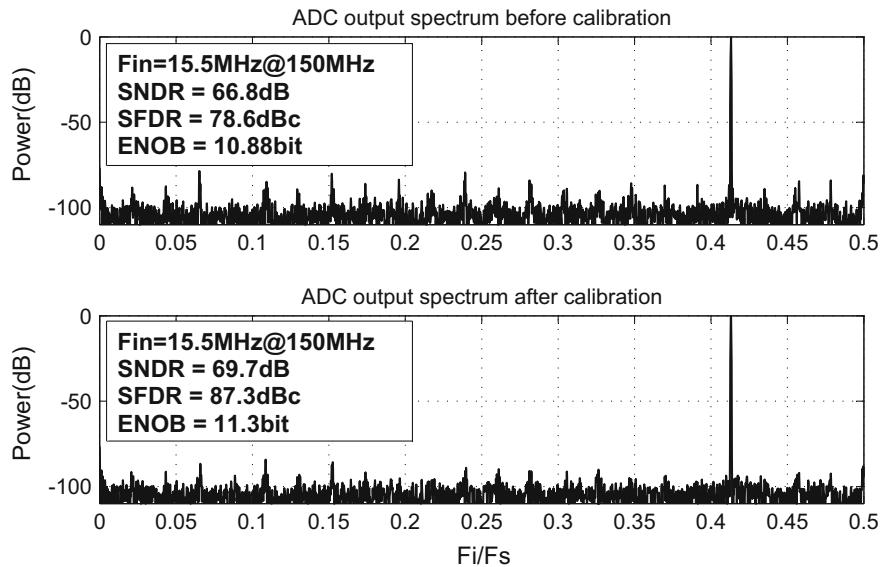


Fig. 7.7 Measured FFT spectrum (the output is decimated by 4X)

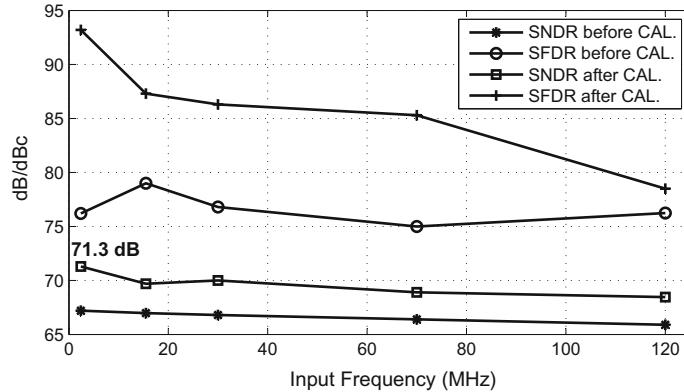


Fig. 7.8 Measured SNDR, SFDR versus input frequency with/without the calibration technique

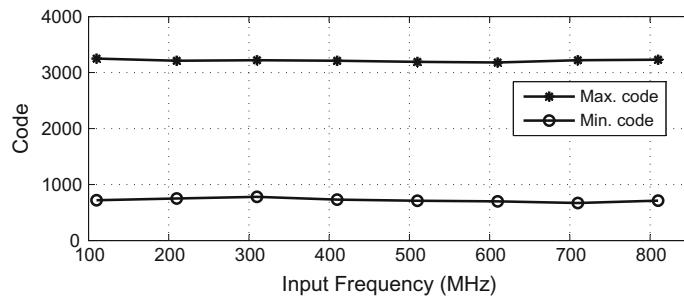


Fig. 7.9 Maximum and minimum residue voltage of MDAC1 in digital code

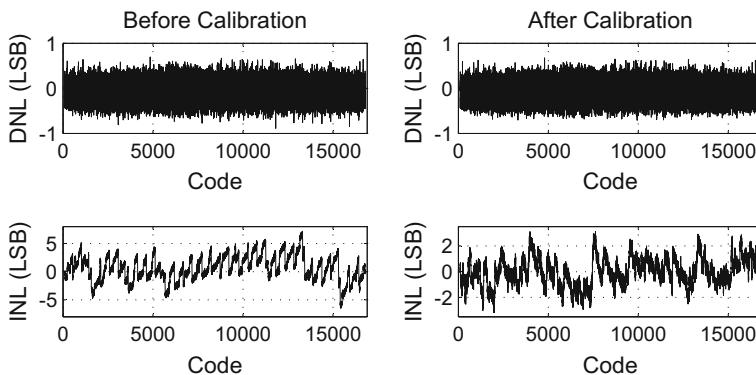


Fig. 7.10 Measured INL and DNL

Table 7.1 Performance comparison

Ref.	Sampling rate (S/s) (M)	SNDR (dB)	Power (mW)	FoM (fJ/step)
[1] ^a	100	72.4	230	691
[2]	100	73.0	250	687
[4]	100	69.8	130	515
[5] ^a	150	67.0	48	194
The ADC	150	71.3	85	188
The ADC ^b	150	71.3	68	151

^aNo fully integrated on-chip reference buffers

^bExcluding the power consumption of the high-speed reference buffer

7.7 Summing up

The ADC combines the circuit techniques of range scaling, opamp and capacitor sharing and SHA less together, extending the input signal swing at a low supply voltage and optimizing both the power and the noise. The blind calibration improves the linearity further. Additionally, a level-shifter-aided reference buffer is integrated on chip.

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Chapter 8

Contributions and Future Directions

8.1 Main Contributions

The organization of the book is shown in Fig. 8.1. We present the considerations and the techniques to design a high-performance and power-efficient ADC. Two aspects, from the system level (Chap. 2) to the circuit block level (Chaps. 3, 4 and 5), are both covered. Besides, the calibration techniques (Chap. 6) for different architectures are all discussed in detail. Furthermore, a design case is presented (Chap. 7).

A successful low-power architecture of the high-performance ADC is extremely important, because it helps to save the power dissipation in the systematic level. Although traditional architectures, the pipelined ADC, the SAR ADC, and the flash ADC, have limitations, they all have the potential to achieve the high performance and the high power efficiency, via the adjustment in the architecture level or with the aid of useful techniques, which are concluded in Fig. 8.2.

- For the pipelined architecture, the SHA-less architecture (Sect. 2.2.1, (1)) helps to reduce the power dissipation and the noise. The multi-bit stage (Sect. 2.2.2, (2)) enables the ADC to save the power dissipation and enhance the linearity. Further, the opamp and capacitor sharing (Sect. 4.3.3, (8)) can relax the requirement of the opamp, and the hybrid opamp (Sect. 4.4.2, (9)) improves the gain and the bandwidth without increasing the current. Besides, the conversion linearity can be improved by the calibration (Sect. 6.4.1.2, (10)).
- For the SAR architecture, the capacitor mismatch can be calibrated by the technique with dithering (Sect. 6.4.2.1, (11)) and the technique based on code density (Sect. 6.4.2.2, (12)).
- For the Flash architecture, the redundancy technique (Sect. 2.2.3, (3)) enables the ADC to save the power dissipation and enhance the linearity. This architecture can be combined by the hybrid architecture (Sect. 2.4.1, (4)) with other architectures to improve the performance and the power efficiency.
- The time-interleaved technique (Sect. 2.5, (5)) can effectively increase the conversion rate, with the aid of the calibration technique (Sect. 6.4.4.2, (14)). Besides,

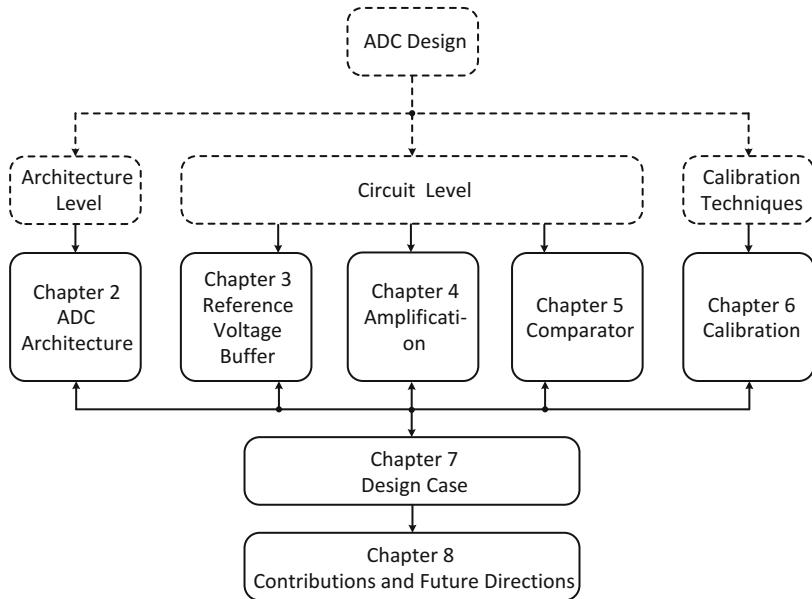


Fig. 8.1 The organization of the book

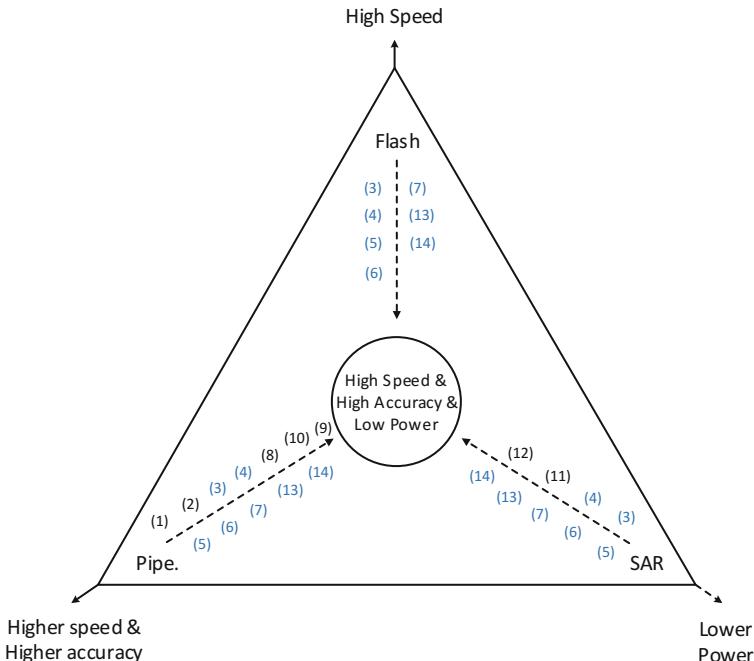


Fig. 8.2 Systematic concerns and solutions (architecture level: (1)~(5), circuit level: (6)~(9), and calibration: (10)~(14))

the reference voltage buffer can be provided by the level-shifter-aided buffer (Sect. 3.3.1, (6)) and the charge-compensation based technique (Sect. 3.3.2, (7)). The offset of the dynamic comparator can be compressed by the input offset storage technique (Sect. 6.4.3.2, (13)).

8.2 Future Directions

In the future, our research will focus on the high-speed interface, the software radio application, and the process-friendly design.

8.2.1 High-Speed Interface

For the application of the ADC with increased resolution and speed, one of the challenges is how to transmit a large amount of date in a fixed time. That imposes extreme requirements on the interface of the ADC. The traditional solution is adopting the parallel interface in the ADC, and its properties are

1. The number of pins is $N + 1$, where N is the resolution of the ADC. The increased pins result in higher cost of the packaging.
2. The increased pins make the PCB design complex. What is worse, it is difficult to reuse the resolution-dependent PCB.
3. To communicate with the optic-fiber system, additional parallel-to-serial converter is required.

Parallel interface is another candidate and its properties are

1. The number of pins is only 1.
2. The minimum pin make the PCB design simple. And thereby the general PCB can be reused.
3. The ADC with the serial interface can communicate with the optic-fiber system directly.

By considering the cost of packaging, the layout complexity on PCB [1] and the flexibility to connect with an optic-fiber communication system [2], it is necessary to replace the traditional parallel interface by a high-speed serial interface (HSSI).

HSSI protocols have been introduced, and one protocol called JESD204B has been widely adopted. It was proposed by JEDEC committee for high-speed serial data transmission between the ADC and the DAC or the FPGA. The first edition of JESD204 was published on 2006, then a revised version called JESD204A launched on 2009, some new features added based on JESD204. Three years later, JEDEC revised it again and published the newest version of this protocol called JESD204B. JESD204B interfaces have been embedded in some ADC products, like AD9625 and ADC16DX370, DAC products and FPGA.

Based on the discussion above, JESD204B HSSI should be focused on in the following work. To implement it, both the SerDes transceiver and the JESD204B protocol should be researched.

8.2.2 Software Radio Application

The amazing evolution of digital technology during the 1980s led to the emerging of the software radio [3]. It has been focused on by both the academic research and the commercial applications of the future wireless system. The ideal software radio receiver proposed by J. Mitola, III is described in Fig. 8.3. The RF circuits and the analog circuits in the traditional receiver are replaced by a RF-sampling ADC. In addition, the digital baseband completes the signal processing. In other words, former analog functionalities are now performed digitally.

The software radio receiver imposes the high sampling rate and the large dynamic range on the ADC, which is a big challenge to both the process technology and the design techniques. To respond to that, IF-sampling ADC based architectures are adopted in the current software radio products, like LMS6002D and AD9361. However, IF-sampling architecture makes the RF circuits and analog circuits complex and increases the cost, which is unexpected. In the recent years, RF-sampling ADCs have been introduced, like a 14-bit 5 GSps ADC [4] and a 14-bit 1 GSps ADC [5]. The new development of ADCs provides the possibilities to realize the software radio in Fig. 8.4. And thereby, the RF-sampling ADC is one of our future directions.

Fig. 8.3 Ideal software radio receiver

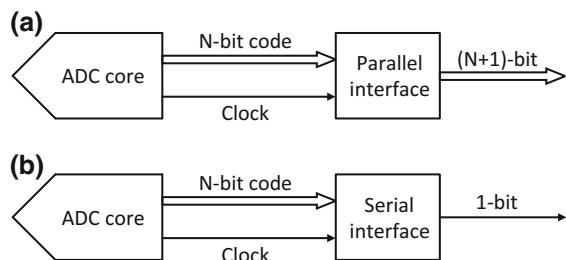
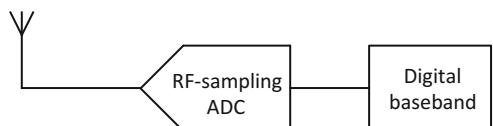


Fig. 8.4 Ideal software radio receiver



8.2.3 Process-Friendly Design

The first CMOS devices began to emerge in mid-1960s, and provided both P-channel and N-channel MOS devices on the same process. Since then, the process technology has developed enormously. The beauty of CMOS devices is from its properties: the ideal digital capability and the ability to consume no static current. However, the advanced CMOS technology make the analog designs complex and difficult due to the deeply scaled transistor size and supply voltage. In this situation, it is better to make the ADC as digital as it can to make full use of the development of the process.

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