

Electrical Characterization and Preliminary Beam Test Results of 3D Silicon CMS Pixel Detectors

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Abstract—The fabrication of 3D detectors which requires bulk micromachining of columnar electrodes has been realized with advancements in MEMS technology. Since the fabrication of the first 3D prototype in Stanford Nanofabrication Facility in 1997, a significant effort has been put forth to transfer the 3D detector technology to large scale manufacturing for future high luminosity collider experiments, in which the radiation hardness will be the primary concern, and other applications such as medical imaging and X-ray imaging for molecular biology. First, alternative 3D structures, single type column (STC) and double-side double type column (DDTC) 3D detectors, were produced at FBK-first (Trento, Italy) and CNM-Barcelona (Spain), and assessed thoroughly to improve the production technology towards the standard full-3D detectors. The 3D collaboration has been extended to include SINTEF (Norway), which is committed to small to medium scale production of active edge full-3D silicon sensors. This paper focuses on p-type 3D detectors compatible with the CMS pixel front end electronics from the second run of fabrication at SINTEF clean room facilities. The sensors that passed the wafer level electrical characterization have been bump-bonded at IZM (Germany), assembled into modules and wire-bonded for functional characterization at Purdue University. We report the leakage current characteristics, bump-bond quality, threshold, noise, and gain measurement results of these 3D modules as well as the preliminary beam test data taken at Fermi National Accelerator Laboratory.

Index Terms—3D silicon pixel detectors, beam test, CMS, radiation hardness, super-large Hadron Collider (LHC).

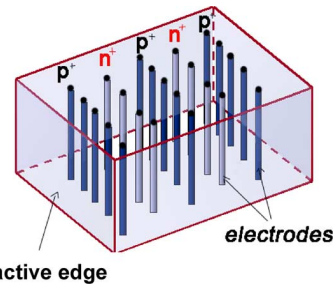


Fig. 1. 3D sensor geometry.

I. INTRODUCTION

THE tracking system of the CMS experiment at the Large Hadron Collider (LHC) will undergo a major upgrade to adapt to the foreseen 10-fold increase in luminosity of the accelerator to $10^{35} \text{ cm}^{-2} \text{ s}^{-1}$ (the so-called Super-LHC). This high luminosity presents a challenge for the detector technology to be adopted for the innermost tracking layers where the radiation fluence is expected to reach $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$, since the current planar silicon detectors are functional only up to a fluence of $10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$. The 3D detector technology [1] is regarded as one of the most promising solutions for the radiation tolerance requirements of innermost tracking layers at the Super-LHC.

3D detectors possess vertical cylindrical electrodes extending all the way through wafer thickness (Fig. 1), unlike conventional planar detectors in which the electrodes are ion-implanted on the top and bottom surfaces of the substrate. The operations of planar and 3D detectors are demonstrated in Fig. 2. In the planar structure, the depletion region grows from the top to the bottom of the substrate, and the signal carriers generated by the ionizing radiation drift vertically under the influence of the electric field and traverse the substrate thickness to reach the collecting electrodes. The full depletion and charge collection distance is equal to the substrate thickness. In the 3D architecture, on the other hand, the depletion region extends laterally and the charge carriers are swept out horizontally to the nearest columnar electrodes. The superior radiation hardness of 3D detectors is mainly due the fact that a significantly reduced inter-electrode distance can be achieved independently of the substrate thickness. A smaller inter-electrode distance leads to a lower depletion voltage, faster response and reduced carrier trapping at high fluences due to the diminished carrier drift distance. In the planar structural design, the electrode separation is equal to the substrate thickness, and therefore an attempt to reduce this distance by exploiting thinner substrates will be at the

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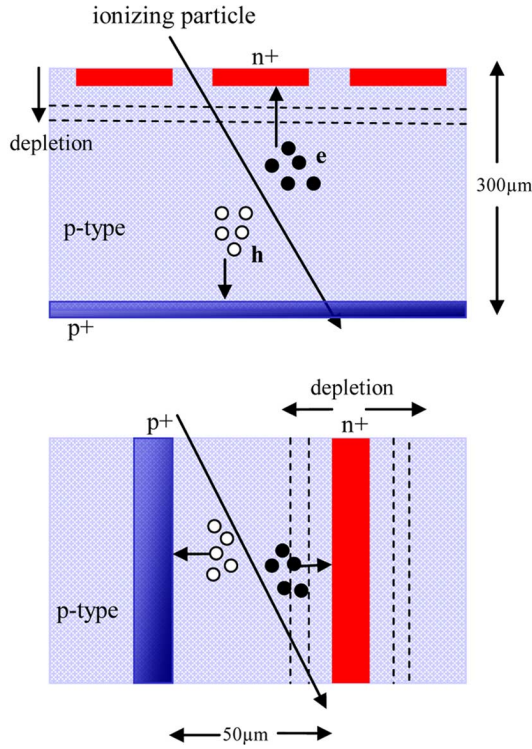


Fig. 2. Operations of planar and 3D detectors are depicted.

expense of degraded signal to noise ratio. Despite the advantages of smaller electrode separation, the optimum 3D sensor design must maintain a reasonably large inter-electrode distance to yield the best tradeoff with the undesired consequences of high electrode density, which are i) high electronic noise because of increasing pixel capacitance and ii) large dead volume introduced by the column electrodes due to loss of the charge generated within the columns.

Another advantageous intrinsic feature of the 3D detector is that it can be fabricated with an active edge [2]–[4] so that the width of the dead periphery can be reduced to only a few microns. 3D detectors also surpass the planar ones in terms of low charge sharing [5].

In this paper, the production and pre-irradiation characterization of active edge full-3D detectors bonded to the CMS pixel readout chip are presented. First, the architectures and fabrication of the sensors and the assembly of the bump-bonded modules are described with a short review of the readout electronics. Next, some important electrical and functional characteristics such as leakage current behavior, bump-bond quality, noise, threshold and gain of the wire-bonded modules are reported. Finally, the initial charge collection results obtained from the beam test are discussed.

II. DESCRIPTION OF 3D CMS PIXEL MODULES AND THEIR PRODUCTION

The fabrication of 3D sensors has been carried out at SINTEF on 200 μm and 285 μm thick p-type silicon wafers with resistivity above 10 $\text{k}\Omega\cdot\text{cm}$. The electrodes of the 3D CMS pixel sensors are arranged in two different configurations: one sensor

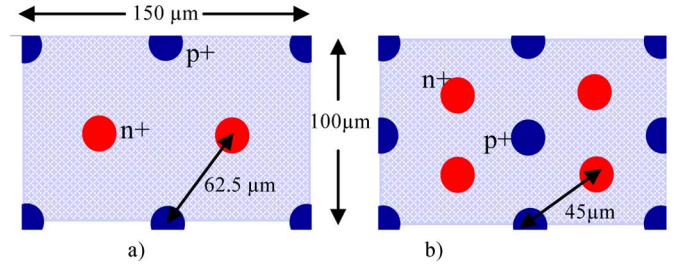


Fig. 3. Sketch of arrangement of columnar electrodes in CMS pixel sensors of (a) 2E type and (b) 4E type.



Fig. 4. Wafer layout of 3D silicon sensors fabricated at SINTEF.

type features four readout columns (4E) and the other features two readout columns (2E) per CMS pixel with size of 100 $\mu\text{m} \times 150 \mu\text{m}$ (Fig. 3). The distances between the centers of neighboring readout and bias columns of 2E and 4E sensors are 62.5 μm and 45 μm , respectively. Active edge trenches of width of 5 μm and columns of diameter of 14 μm were etched all the way through the wafer thickness with deep ion reactive etching. The wafer was bonded to a support wafer after the p-spray isolation and prior to the rest of processing in order to maintain the wafer integrity during trench etching. After the trenches and holes are filled with polysilicon, they are doped to form the p-type active edge, p-type columns which are used for biasing, and n-type columns that are used for readout. Further information on sensor description and the fabrication process can be found in [6], [7].

Fig. 4 shows the layout of the wafers processed at SINTEF. About 15% of the wafer area is covered with CMS pixel sensors, and the rest includes ATLAS (both pixel and strip) and Medipix type devices as well as some test structures. The sensors that have exhibited good I-V behavior (low leakage current and high breakdown voltage) at the wafer level are mostly located near the center of the wafer.

3D CMS pixel sensors that passed the wafer level electrical characterization have been connected to the 40 MHz CMS pixel readout chip (ROC) based on $0.25\ \mu\text{m}$ CMOS technology (PSI46v2) [8]–[10] via Pb-Sn bump-bonds at IZM, Germany [11]. The ROC consists of 4160 pixel readout channels arranged in a matrix of 52 columns and 80 rows, organized into double-column readout. Each pixel cell has a charge-sensitive preamplifier, shaper, controllable discriminator, storage capacitor, and a charge injection circuitry for calibration purposes. The calibration signals are injected either through a $4.8\ \text{fF}$ capacitor connected directly to the amplifier input node, or via the sensor through the air gap between a top metal plate in the ROC and the sensor. The signal first enters the pre-amplifier and then the shaper which limits the bandwidth of the pre-amplifier output signal to reduce the low and high frequency noise contributions introduced in particular by the sensor leakage current and by the input device. A global threshold value common to all pixels in the chip is set by a DAC register. Variations of individual pixel threshold can lead to an increased noise hit rate or to a reduced sensitivity. In order to compensate for these variations, the threshold is trimmed by a DAC register with 4-bit resolution. The discriminator compares the shaper output to the trimmed threshold value and signals above the threshold are stored in a sample-and-hold circuit. The double-column periphery is then immediately notified about the new event through a local bus line Column-OR. The first stage of data readout takes place within the double column periphery and runs at 40 MHz. The time information is stored (within 25 ns) in the time stamp buffer and the address and the analog signal of each hit pixel is transferred to the column data buffer located in the column periphery. After a trigger decision is taken in $3.2\ \mu\text{s}$, the analog hit information is sent via optical links to the off detector readout electronics where a digitizer performs digitization of the analog output, formats the event and transmits it to the CMS data acquisition. The row and column information of the hit pixel is encoded on six analog levels.

The assembly of 3D CMS pixel detectors was done at Purdue University in a similar way to the standard production Forward Pixel (FPIX) detectors currently installed in the CMS tracker [12], [13]. Fig. 5 shows a picture and a sketch of the 3D CMS pixel module assembly. Each of the bump-bonded sensors was glued to a very high density interconnect (VHDI) using a thermally conductive and electrically insulating film adhesive that matches the size of ROC backplane. The sensor overhangs the end of the VHDI in order to allow access to make a wirebond connection to the sensor HV (High Voltage) bias bond pad. The sensor/ROC/VHDI module was then mounted on a carbon fiber plate which has a “Fan Out” printed circuit board held on by screws. Wire-bond connections were made between ROC and VHDI channels and between VHDI channels and the circuit on the “Fan Out” board. An additional wirebond connection was made between the sensor and the circuit on the Fan-Out board for the bias voltage (labeled as bias wire in the picture and sketch). Due to the presence of a support chip on the top of the sensor, a small opening was made through the carbon fiber plate at the end of the VHDI and the plate was inverted on the wirebond machine for wire-bond tool access through the plate to the sensor HV bias bond

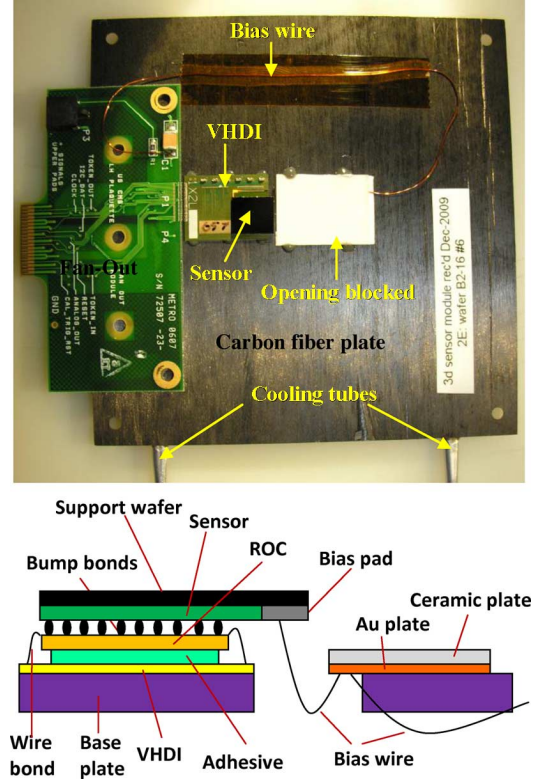


Fig. 5. A picture and schematic sketch of a 3D CMS pixel module. The sensor bump-bonded to PSI46v2 ROC is glued to a VHDI, and the sensor/ROC/VHDI module is mounted on a carbon fiber plate with a test printed circuit board. Wire-bond connections are made (i) between ROC and VHDI, (ii) between VHDI and printed circuit board, and (iii) between the sensor and the printed circuit board (bias wire).

pad and a gold-plated ceramic piece clamped onto the plate next to the VHDI. The gold-ceramic piece was electrically insulated from the carbon fiber plate and was used as an intermediate pad for connecting the sensor to the circuit on the Fan Out board by wirebond.

III. ELECTRICAL CHARACTERIZATION

A. Leakage Current Characteristics

I-V characteristics of 3D CMS pixel sensors were measured both at the wafer stage and after connecting the sensors to the front end electronics. The measurement results of four representative sensors with different electrode configuration and substrate thickness combinations are shown in Fig. 6. After detector assembly, the leakage current is observed to drop off for all sensors. The measurements on wafer were done by connecting all n-type columns with a temporary metal layer that allows the measurement of the total chip current at once. Due to the formation of a MOS layer with the presence of the metal layer, the surface inversion introduces extra leakage current, which explains the higher leakage current observed in wafer level measurements. Moreover, the soft breakdown preceding the hard breakdown for 4E sensors at wafer level disappears after detector assembly.

Due to the lack of any C-V data, the exact depletion voltages were not computed. Although the current seems roughly to saturate at a reverse bias voltage of $\sim 10\ \text{V}$, the depletion voltages can

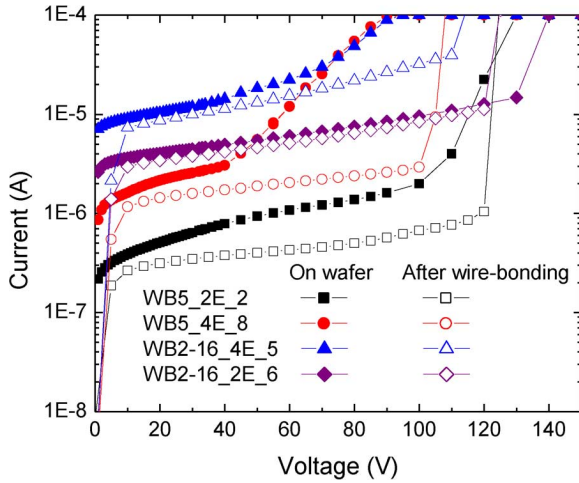


Fig. 6. I-V characteristics of four 3D CMS pixel sensors with different combinations of substrate thickness and electrode configuration as measured at wafer level and after wire-bonding. The convention used in naming is “wafer_electrode configuration_sensor number”.

be obtained more accurately using the noise or charge collection efficiency behavior as a function of bias voltage. These measurements have shown that all sensors reach full depletion at reverse bias voltages less than 40 V as will be discussed later. The leakage currents after full-depletion are in the range of $\sim 0.4 \mu\text{A}$ to $\sim 10 \mu\text{A}$ per chip for all sensors. If this current is normalized to a single pixel, it falls into the range of $\sim 100 \text{ pA}$ to $\sim 2.5 \text{ nA}$. The order of the measured leakage current is consistent with the results of TCAD simulations [6]. The experimental breakdown voltages are well above the depletion voltages, being $\sim 100 \text{ V}$ for 4E sensors and $\sim 120 \text{ V}$ for 2E sensors. Although simulations have shown slightly lower breakdown voltages (80 V for 4E sensors and 95 V for 2E sensors), the difference between the breakdown voltages of the two sensor configurations are predicted quite well. In simulations, a typical value of $1 \times 10^{11} \text{ cm}^{-2}$ was assumed for the oxide charge, which plays the most important role in determining the breakdown, although the exact value was not known. The slightly lower theoretical breakdown voltages compared to the experimental ones can therefore be attributed to the fact that the actual oxide charge was a little higher or equivalently the actual p-spray dose was slightly lower than the one employed in the simulation.

B. Bump-Bond Quality

The broken or poorly made bumps on the assembled 3D sensor modules were determined by a method called “modified external calibration” [14] using Renaissance that is the data acquisition system used for the test of the CMS FPIX assembly [15]. This technique, which does not require a radioactive or light source, is based on injection of calibration signal via the sensor through the air gap between the top metal plate in the readout chip and the sensor. It is more difficult to use external charge injection compared to the internal one because i) the injection capacitance and consequently the injected signal is much smaller and ii) some of the calibration signal couples into the amplifier through some internal path. As a result, no significant difference is observed between the pixels with

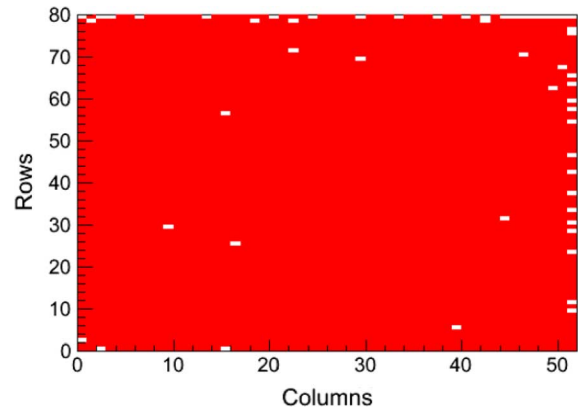


Fig. 7. Bump-bond map of the detector WB5_2E_2 at a reverse bias of 40 V. Poor bumps are shown in white.

missing bump and pixels with bump. Therefore, it is necessary to measure the difference between the parasitic internal and the intentional external coupling through the sensor. The parasitic signal is believed to originate from the charge injection bus which runs down the whole column. Two different measurements are performed:

- i) The pixel whose bump is under test is set up for external calibration and its threshold (see the next subsection) is measured.
- ii) A probe pixel in the same column as the pixel under test is set for charge injection while disabled. The pixel whose bump to be tested is enabled but not configured for calibration, and its threshold is measured again.

The pixels with broken or poorly made bumps are identified by comparing the thresholds obtained from the two measurements, which would be almost the same for these pixels and significantly different for pixels with good bump bond quality.

Fig. 7 presents the bump-bond map for one of the assembled 3D CMS pixel detectors, namely the WB5_2E_2 module, as measured at a reverse bias of 40 V. This device test has shown ~ 50 poor bumps out of a total of 4160 bumps while the bump bond map of the other three modules seemed almost perfect with only a few broken bumps.

C. Threshold and Noise Measurements

The noise performance of 3D CMS pixel detectors has been assessed using Renaissance. A threshold scan of each pixel is performed by injecting internal charge (VCAL) and evaluating the response versus deposited charge. The charge is injected through the injection capacitor at the pre-amplifier input. Although a sharp transition from 0 to 1 in the resultant efficiency curve is ideally expected at the threshold, this is normally not the case due to the fact that some injected charges below the threshold are detected and some above the threshold are not because of noise. Threshold and noise are computed by fitting this efficiency curve, named S-curve, with an error function which is a convolution of the ideal step function and the Gaussian pixel noise distribution. The threshold value of the pixel is extracted as the charge corresponding to the efficiency of 0.5 in the S-curve. The equivalent noise charge (ENC) of the pixel, which is inversely proportional to the steepness of the transition curve

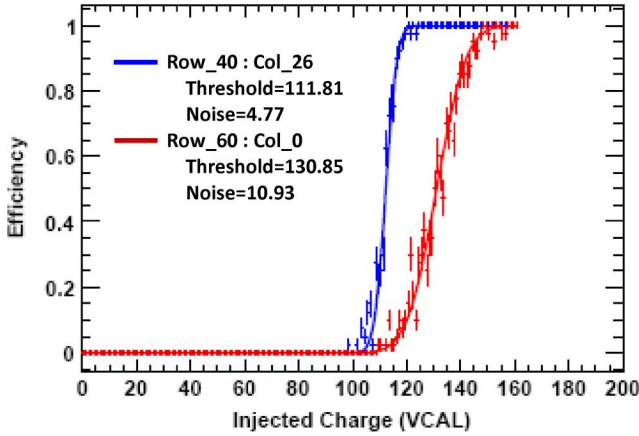


Fig. 8. S-curves of an edge pixel and a regular pixel in the sensor WB5_2E_2 at a reverse bias of 40 V. The threshold and noise values are in VCAL units.

from efficiency of 0 to efficiency of 1, is determined from

$$\text{ENC} = \frac{1}{\sqrt{2\pi}} \frac{1}{s} \quad (1)$$

where s is the slope of the S-curve at efficiency of 0.5. The thresholds and noises of individual pixels form Gaussian distributions with means giving the threshold and the noise of the entire chip, respectively.

Fig. 8 shows the S-curves for one pixel at the chip edge and one pixel near the chip center in a 2E sensor with substrate thickness of $285 \mu\text{m}$ at reverse bias of 40 V. The threshold and noise are measured in VCAL unit which corresponds to 65.5 electrons. The dominating contribution to the measured noise comes from capacitive noise. The edge pixel is noisier as it has a larger size and therefore a higher capacitance. Three edges of the chip are occupied by pixels with larger dimensions than the nominal pixel size of $100 \mu\text{m} \times 150 \mu\text{m}$ due to mechanical constraints:

- i) The pixels in the first and last columns but not in the last row are $100 \mu\text{m} \times 300 \mu\text{m}$.
- ii) The pixels in the last row but not in the first and last columns are $200 \mu\text{m} \times 150 \mu\text{m}$
- iii) The pixels in the last row and in the first and last columns are $200 \mu\text{m} \times 300 \mu\text{m}$

These atypical pixels manifest themselves in the noise map of the chip in Fig. 9. One corner pixel with size of $200 \mu\text{m} \times 300 \mu\text{m}$ exhibits the highest noise value of 16 VCAL (1048 electrons) while the other pixel with same size seem to have a broken bump. The noise of the other edge pixels is measured to be around 10 VCAL (655 electrons). The noise of regular pixels ranges between 3 VCAL (196 electrons) and 6 VCAL (393 electrons), which can be seen more clearly in Fig. 10. In evaluating the chip noise with a Gaussian function fit to this distribution, the large edge pixels and the pixels with poor bump-bonds were excluded.

The noise performance of 3D CMS pixel assemblies has been also measured as a function of bias voltage as shown in Fig. 11. The noise decreases drastically with bias voltage up to 40 V beyond which it remains essentially constant. For the 2E sensors, the minimum noise is 250–300 electrons whereas it is around 450 electrons for the 4E sensors. The initial decrease of the

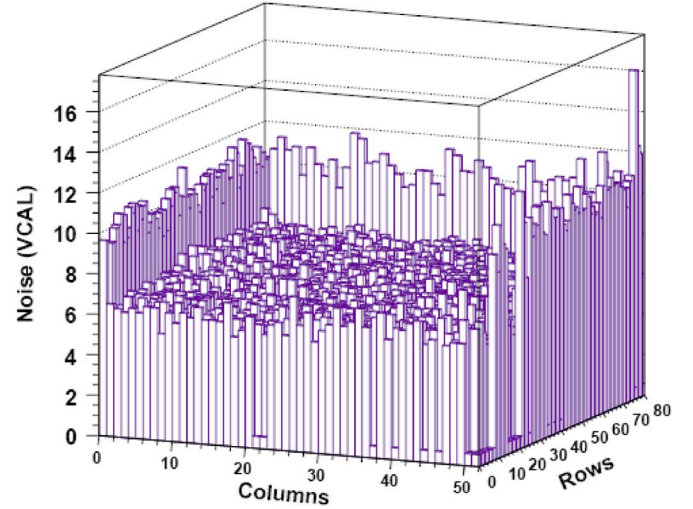


Fig. 9. Noise map of the WB5_2E_2 chip at a reverse bias of 40 V.

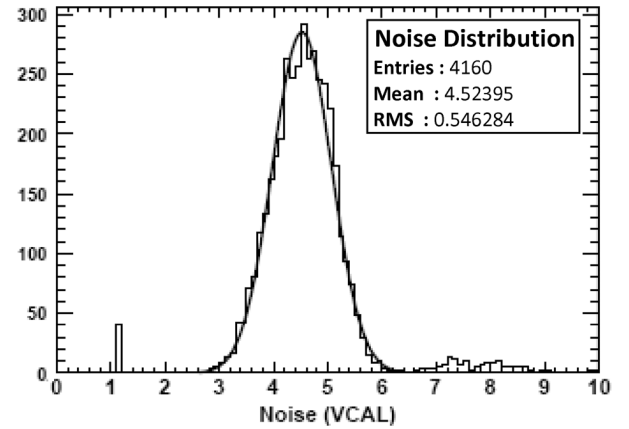


Fig. 10. Gaussian noise distribution of the WB5_2E_2 chip at a reverse bias of 40 V.

noise with bias voltage is attributed to the fact that the pixel capacitance decreases with bias voltage until the full depletion is reached. Therefore, the depletion voltages of all sensors as extracted from the bias scan of the noise are ≤ 40 V. The test stand was unable to measure the noise of the 4E sensors for bias voltages below 40 V since it is probably too high.

The higher noise of the 4E sensors compared to the 2E sensors is expected due to smaller electrode separation and consequently higher pixel capacitance. Because of the same reason, both 3D detector configurations have higher noise than planar pixel detectors. For comparison, the noise of FPIX (Forward Pixel) and BPIX (Barrel Pixel) modules currently installed in the CMS using planar pixel sensors were measured as 110 and 155 electrons, respectively [16], [17]. The origin of the lower noise of FPIX modules compared to BPIX modules is partly attributed to the different inter-electrode isolation techniques which result in different pixel capacitance. The isolation method employed in BPIX is p-spray which is the same as the 3D pixel modules while p-stop isolation is used for FPIX modules.

As explained before, a trimming algorithm is used to correct for threshold variations from pixel to pixel and unify the individual pixel thresholds to the lowest possible value, which is

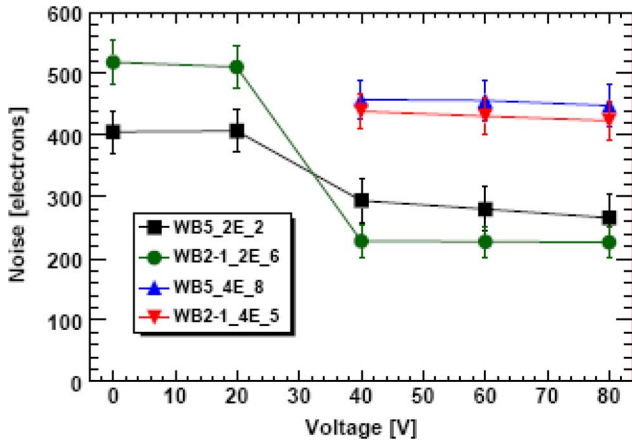


Fig. 11. Noise as a function of reverse bias voltage for the four sensors featuring different substrate thickness and electrode configuration.

needed to improve the position resolution of the detector. For this purpose, each pixel cell in the ROC is provided with a 4-bit register, *trimbit*, to tune the pixel threshold and the ROC is equipped with a global DAC register, *Vtrim*, that controls the tune rate with a single value. First, the global *Vtrim* register is set to a certain value determined by some diagonal pixels. Then, five threshold scans are performed, and for each scan, the threshold of each pixel is computed by an S-curve fit. One scan is done for each value of *trimbit* with only one out of the four bits is set and one scan with all four bits are set. The S-curve fit results are stored in a histogram and the required individual pixel threshold shift is determined by the parameters of a straight line fit to this histogram. Finally, the optimum threshold values of each pixel are set.

The reduction of threshold dispersion with trimming mechanism can be seen clearly in Fig. 12 which shows the threshold distribution for the WB2-16_2E_6 module at a reverse bias of 40 V before and after trimming. The untrimmed threshold is measured 7919 ± 362 electrons (120.9 ± 5.53 in VCAL units) while after the trimming algorithm is activated, it reduces to 6832 ± 86 electrons (104.3 ± 1.31 in VCAL units). The thresholds of WB5_2E_2, WB5_4E_8, and WB2-16_4E_5 detector modules were measured to be 7860 ± 422 , 8528 ± 99 , and 8633 ± 97 electrons, respectively. The poor threshold trimming quality of the WB5_2E_2 detector might be a consequence of large number of pixels with missing bumps. The threshold values of 3D CMS pixel detectors are too high when compared with the FPIX and BPIX detectors which have thresholds of 2870 ± 220 and 2910 ± 80 electrons, respectively [16]–[18]. The tracking efficiency of 3D detectors will be greatly impacted by such a high threshold. Currently, we are working closely with the scientists performing the commissioning of the CMS pixel detector at CERN in order to benefit from their experience to reduce the threshold of 3D detectors by proper tuning of DAC registers.

D. Gain Calibration and Optimization

A gain calibration is needed to convert the generated pulse height in each hit pixel in ADC counts to the ionization charge collected by the pixel. This is performed by injecting known

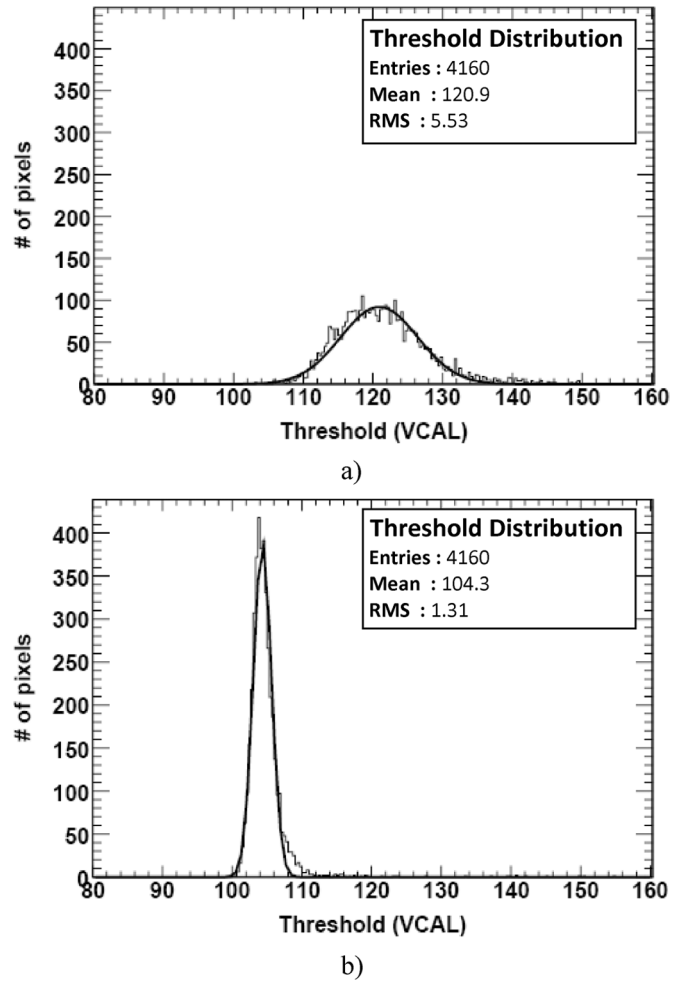


Fig. 12. Threshold distribution of the WB2-16_2E_6 chip at a reverse bias of 40 V (a) before trimming and (b) after trimming.

amounts of calibration charge (VCAL) to each pixel and measuring the corresponding signal output response. Fig. 13 shows a typical curve of the recorded pulse height as a function of the pixel injected charge. In fact, the gain curve consists of a non-linear region at low VCAL values in addition to a saturation region for high charges (above ~ 40000 electrons) and a linear region that encompasses a quite large range between these two regions. The curve in Fig. 13 is obtained after the non-linearity in the low signals region is tuned by a DAC register, *Vsf*. It is important to optimize the DAC registers to minimize this non-linearity as it degrades the position resolution when interpolating between pixel signals. The gain and pedestal of each pixel is determined from the slope and offset, respectively, of the linear region by fitting the gain curve with the following function:

$$\text{ADC} = p_3 + p_2 * \tanh(p_0 * \text{VCAL} - p_1) \quad (2)$$

where the parameter p_1 is associated with the non-linearity in small signals region. As the linearity improves, p_1 decreases, with the best straight line fit in this range obtained for $p_1 = 1$.

Fig. 14 shows the gain and pedestal distributions for all pixels in the chip WB5_2E_2. The gain and pedestal distributions of all standard planar CMS pixels have a mean of 3.6 DAC/ADC and 55 ADC (12700 electrons) with corresponding RMS values

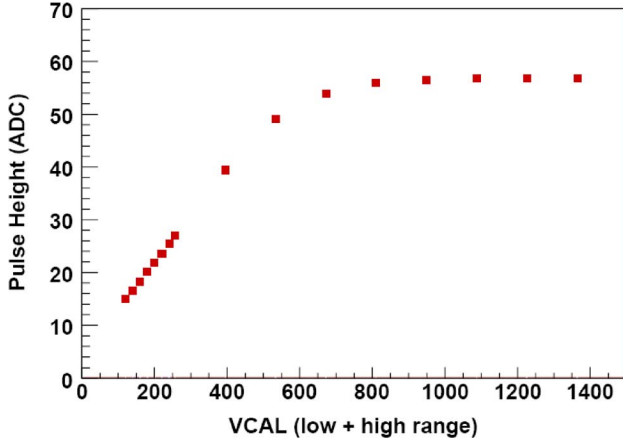


Fig. 13. A representative gain curve of a pixel from the WB5_2E_2 module.

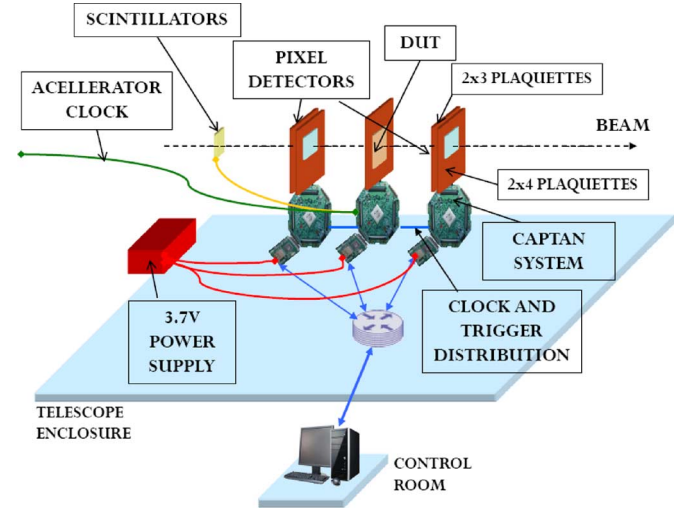


Fig. 15. Test beam setup at FNAL.

IV. BEAM TEST STUDIES

A. Test Beam Setup

The charge collection performance of the 3D CMS detectors has been studied with test beam of 120 GeV protons at Fermi National Accelerator Laboratory (FNAL). A sketch of the test beam set-up is shown in Fig. 15. The CAPTAN pixel telescope consists of three basic cells, with the pixel tracker situated on the two outer cells and the device under test (DUT) on the middle one. Each cell of the pixel telescope has a CAPTAN electronics stack, which is used as the data acquisition system, attached to it. Each of the tracker stacks supports four CMS FPIX pixel modules with configurations of 2×3 and 2×4 readout chips. The DUT stack supports the DUT (3D CMS pixel detector) and receives and distributes the clock from the accelerator and trigger from the scintillators. The average data taking rate was 20 MHz. The data was taken with DUT plane perpendicular to the beam direction. No magnetic field was used. The DUT was cooled during beam tests by a cooling circuit connected to the back of the carbon fiber plate on which the module is mounted. A thermocouple was attached to the back of the carbon fiber near the sensor to measure its temperature. An estimated ΔT of $\sim 6^\circ\text{C}$ between 3D sensor and carbon-fiber surface was used to estimate the temperature of the 3D sensor. During the beam test, the temperature on the back of the carbon fiber plate was recorded $\sim 11^\circ\text{C}$, and therefore the sensor temperature is estimated $\sim 17^\circ\text{C}$.

B. Charge Collection Results

The beam test of the 2E sensors have shown promising results while no correlation was observed for the 4E sensors although their electrical characteristics did not seem problematic. The reason for the failing of 4E detectors is currently not understood and it is still under investigation. Moreover, the gain calibration of one 2E sensor is not available, so the test beam data of only one sensor will be presented in this section.

Fig. 16 shows the map of ADC hits of the 2E sensor from the 285 μm thick wafer. The tracks from the beam through the DUT

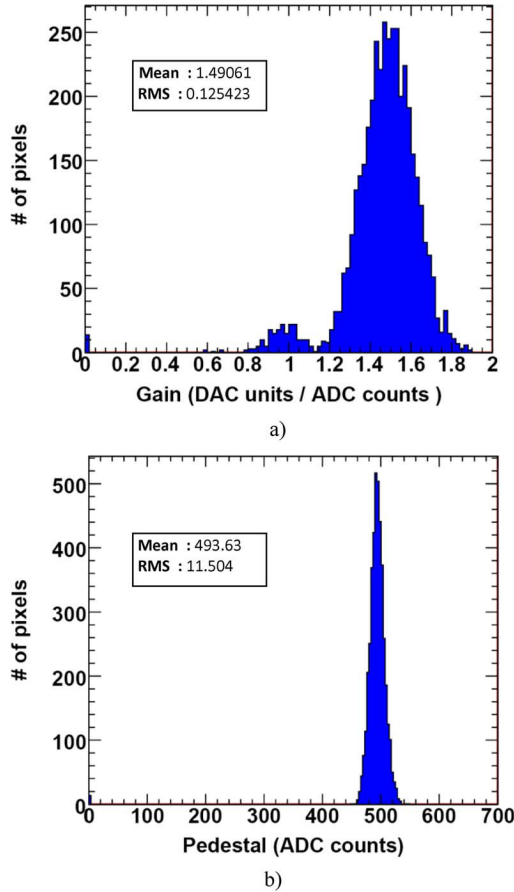


Fig. 14. (a) Gain (slope) and (b) pedestal (offset) distributions extracted from the linear region of the gain curves of the WB5_2E_2 module.

of 0.5 and 12 [16]–[18]. The dispersions are smaller within a single ROC, with RMS values of 0.097 ADC/DAC and 1600 electrons for the gain and pedestal, respectively. 3D CMS pixel detectors have a lower gain (1.49 ± 0.125 DAC/ADC) and a higher pedestal (493.6 ± 11.5 ADC).

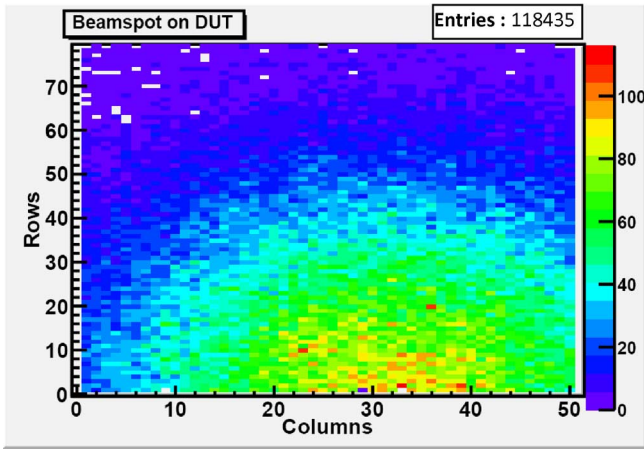


Fig. 16. Map of ADC hits on the detector WB5_2E_2.

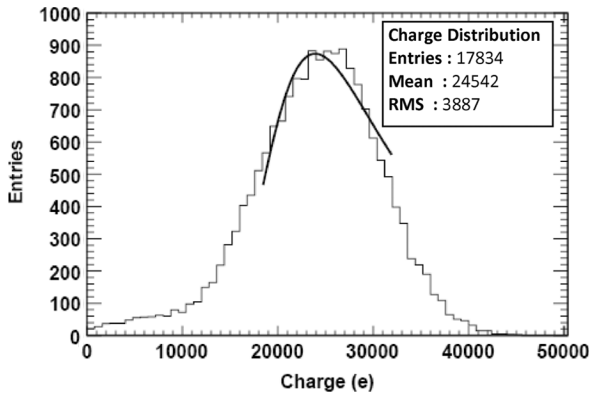


Fig. 17. Charge distribution of the detector WB5_2E_2 at reverse bias of 40 V. A small range around the peak is fitted with Landau function.

are seen clearly. The charge distribution of the same sensor at a reverse bias of 40 V is displayed in Fig. 17. The conversion of the charge from ADC counts to electrons was done as follows [19]:

$$\text{VCAL (DAC)} = \text{ADC} \times \text{gain} - \text{offset} \quad (3)$$

$$\text{Charge (e-)} = \text{VCAL} \times 65.5 - 410 \quad (4)$$

The gain calibration results shown in Fig. 14 were used to perform this conversion. The amount of charge generated through the energy deposition of incident particles is expected to follow a Landau distribution. Taking into account the Gaussian noise distribution as well, the data is normally best fitted with a convolution of the Landau and Gaussian functions. However, the measured charge distribution does not follow an excellent convoluted Landau and Gaussian trend. This indicates that further improvements on the chip calibration need to be achieved for more accurate evaluation of the charge collection. Nevertheless, the results presented in this paper can still provide reasonably close values to the exact collected charge.

The average and peak of the distribution as well as the most probable value (MPV) obtained from a Landau fit around the peak as demonstrated in Fig. 17 have been measured as a function of bias voltage and plotted in Fig. 18. The charge collection

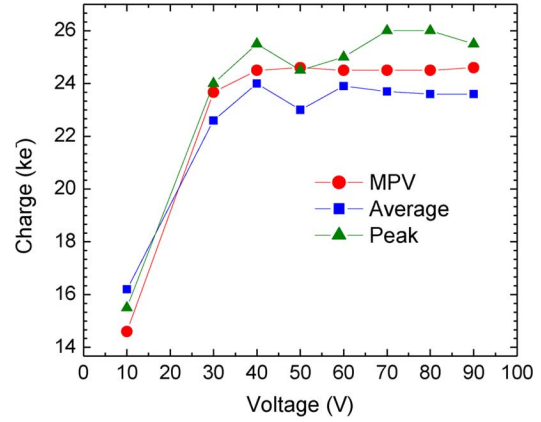


Fig. 18. Charge collection as a function of bias voltage for the detector WB5_2E_2

versus bias voltage characteristics is consistent with the depletion behavior previously quoted from the noise measurements. The efficiency increases with bias voltage up to full depletion (~ 40 V) after which it saturates. Before irradiation, the trapping of charge carriers is negligible and therefore a charge collection efficiency close to 100% is expected at complete depletion. A quite small inefficiency should arise from the charge loss associated with ionizations through the bias columns and readout columns. Simulations have shown that about 60% of the charge generated within the columns can be collected before irradiation [6]. Given that the electrodes constitute about 4% of the total detector volume for the 2E configuration, the expected overall efficiency is $\sim 98.5\%$. This efficiency is translated to a charge of ~ 23 ke- for a sensor with substrate thickness of $285 \mu\text{m}$, assuming that the minimum ionizing particle (MIP) generates a signal of about 80 electrons per distance of $1 \mu\text{m}$ along its track. This is quite close to the roughly measured charge of ~ 24 ke- at full depletion, indicating that the functioning of the detector is not unusual. More work in order to improve the chip calibration for more exact extraction of the charge is in progress. Local variation of the signal within a pixel will also be explored with further studies.

V. CONCLUSIONS AND OUTLOOK

The first 3D CMS pixel detectors fabricated at SINTEF have been characterized after bump-bonding at IZM and assembly at Purdue, and compared with the conventional planar pixel detectors currently operating in the CMS tracker. The measured leakage current and breakdown voltages show a good agreement with predictions of TCAD simulations and no degradation of I-V characteristics has been observed after bump-bonding and wire-bonding. The noise of these devices, which is a drawback in comparison with planar detectors due to larger pixel capacitance resulting from the smaller inter-electrode distance, is of particular interest. The 3D CMS pixel detectors with 4E configuration have a noise of ~ 450 electrons while the noise of those with 2E configuration was measured to be around 250–300 electrons. From the preliminary beam test studies with 120 GeV protons, a signal to noise ratio (S/N) of ~ 80 and a signal to threshold ratio (S/T) of ~ 3 have been obtained for the non-irradiated 2E detector with $285 \mu\text{m}$ substrate thickness. An S/T

ratio close to 4 at the midpoint and above 3 at the end of life of the Super-LHC is required. The current S/T ratio of 3 for 3D CMS pixel detectors, which is expected to be lower after irradiation, does not meet these criteria. In order to achieve the S/T ratio goal set by the Super-LHC requirements, the threshold will be lowered by further tuning of DAC settings.

A new batch of sensors has been bump-bonded at Selex, Italy, with indium instead of Pb-Sn. This will allow us to evaluate and compare the two different bump-bond techniques, and might help us understand if the issue of not getting any signal from the 4E sensors is related to bump-bonding. 3D detectors will have to sustain an ultimate radiation fluence of $10^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ if operated at innermost layers of the CMS tracker during the Super-LHC. Therefore, their radiation hardness performance needs to be assessed up to this fluence, which will be the next task. This high fluence is challenging not only for the sensor itself but also for the readout electronics. The dose of irradiation will be increased gradually to monitor the deterioration of the front end electronics as well as the sensor.

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