

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING
CSE 306 JULY 2022 SEMESTER
COMPUTER ARCHITECTURE SESSIONAL

Assignment on 4-bit MIPS Design, Simulation, and Implementation

In this assignment, you will design, simulate (in S/W), and implement (in H/W) a modified and reduced version of the MIPS instruction set.

1 DESIGN SPECIFICATION

- The Address bus will be of 8 bits.
- The Data bus will be of 4 bits.
- You have to implement 4-bit ALU, hence the name 4-bit MIPS.
- You have to design the following temporary registers:

\$zero, \$t0, \$t1, \$t2, \$t3, \$t4

All these registers will be of 4-bits, and the assembly code that will be provided to simulate your design will use only these mentioned registers.

- The Control unit should be microprogrammed. The control signals associated with the operations should be stored in a special memory (you can use a separate EEPROM for this purpose) units as Control Words.
- During the simulation, an Assembly Code will be given, and you have to convert it into your designed MIPS machine code. The conversion process should be automatic. For this conversion, you can write code in your preferred programming language.
- Marks will vary according to the efficiency of design.

2 INSTRUCTION SET DESCRIPTION

Instruction ID	Instruction Type	Instruction
A	Arithmetic	add
B	Arithmetic	addi
C	Arithmetic	sub
D	Arithmetic	subi
E	Logic	and
F	Logic	andi
G	Logic	or
H	Logic	ori
I	Logic	sll
J	Logic	srl
K	Logic	nor
L	Memory	lw
M	Memory	sw
N	Control	beq
O	Control	bneq
P	Control	j

3 MIPS INSTRUCTION FORMAT

Our MIPS Instructions will be 16-bits long with the following four formats.

• R-type	<table><tr><td>Opcode</td><td>Src Reg 1</td><td>Src Reg 2</td><td>Dst Reg</td></tr><tr><td>4-bits</td><td>4-bits</td><td>4-bits</td><td>4-bits</td></tr></table>	Opcode	Src Reg 1	Src Reg 2	Dst Reg	4-bits	4-bits	4-bits	4-bits
Opcode	Src Reg 1	Src Reg 2	Dst Reg						
4-bits	4-bits	4-bits	4-bits						
• S-type	<table><tr><td>Opcode</td><td>Src Reg 1</td><td>Dst Reg</td><td>Shamt</td></tr><tr><td>4-bits</td><td>4-bits</td><td>4-bits</td><td>4-bits</td></tr></table>	Opcode	Src Reg 1	Dst Reg	Shamt	4-bits	4-bits	4-bits	4-bits
Opcode	Src Reg 1	Dst Reg	Shamt						
4-bits	4-bits	4-bits	4-bits						
• I-type	<table><tr><td>Opcode</td><td>Src Reg 1</td><td>Src Reg 2/Dst Reg</td><td>Addr./Immdt.</td></tr><tr><td>4-bits</td><td>4-bits</td><td>4-bits</td><td>4-bits</td></tr></table>	Opcode	Src Reg 1	Src Reg 2/Dst Reg	Addr./Immdt.	4-bits	4-bits	4-bits	4-bits
Opcode	Src Reg 1	Src Reg 2/Dst Reg	Addr./Immdt.						
4-bits	4-bits	4-bits	4-bits						
• J-type	<table><tr><td>Opcode</td><td colspan="2">Target Jump Address</td><td>0</td></tr><tr><td>4-bits</td><td colspan="2">8-bits</td><td>4-bits</td></tr></table>	Opcode	Target Jump Address		0	4-bits	8-bits		4-bits
Opcode	Target Jump Address		0						
4-bits	8-bits		4-bits						

4 MEMORY CONSIDERATIONS

You need to consider three types of memory:

- Instruction Memory (accessed through the program counter, PC)
- Data Memory (accessed through address)
- Bonus: Stack Memory (accessed through stack pointer, sp. Sample instruction: **sw \$t0, 0(\$sp)** or **lw \$t1, 4(\$sp)**), this will be used for push and pop instructions.

5 INSTRUCTION SET ASSIGNMENT

The opcodes of the instruction will be between 0 to 15 based on the sequence of instruction id given below. Sequence ABCDEFGHIJKLMNOP means add instruction's opcode will be 0, addi instruction's opcode will be 1, sub instruction's opcode will be 2, and so on.

Group ID	Section A1	Section A2	Section B1	Section B2
1	KJEIOPFDLMCBGNHA	MGELJFKDNIOAPBHC	PGIOKMCBHDJLNFEA	CLONPHADFMKGBGJIE
2	HDAMGELBFPCJNIKO	JALMKDFGPIECNBOH	IKGDPJCLOAEFBMNH	POCABIHGNLKEJDFM
3	LABKODCHNIJEPFGM	MOJNFBHCLPKGDI EA	CEIMOLDNFAKBJPHG	PHALCNBIOFKEMGDJ
4	FONKIAJMBLEDCHGP	LPJACGBKIMFDHEON	JMFBDLIGHPOENACK	GDACJLIONFMBEKHP
5	AIPEDJMHOBGLCKFN	COGBIKAHPMJEDLFN	IJPBHDAFGMNECKOL	ACDFNHEIBLMPKGJO
6	OIKAMPEFGJCLHNDB	HOGKDJINLBFAMCPE	OFFPJLHKGBDCMAEIN	KGAMDCFBHNOJP ELI

6 REPORT CONTENT

Contents of the report are recommended as follows:

- Introduction
- Instruction Set
- Circuit Diagram printed in drawing paper
- How to write and execute a program in this machine
- Special Features Implemented if any (may carry bonus marks)
- ICs used with their count
- Discussion

7 SUBMISSION GUIDELINE

- Create a folder named "<Lab Group>_<Group ID>_Simulation" and put all the necessary simulation files in this folder.
- Create a second folder named "<Lab Group>_<Group ID>_Necessary_Content" and put all your codes to convert assembly codes into mips machine codes (or any others extra contents that will be necessary to simulate you pc).
- Finally create a third folder named "<Lab Group>_<Group ID>_Submission" and put your report along with the previously prepared two folders. Now zip this final folder and upload the zip file in moodle submission link (a single submission from each group).

Submission Deadline: February 19, 2023 (Sunday) 11:55 PM.

N.B. This doc may be updated if needed. Notifications will be given in the news forum as soon as any kind of correction is made. For any kind of confusion, feel free to mail at toufikuzzaman@teacher.cse.buet.ac.bd with the subject "July 2022 CSE 306 Assignment 3".