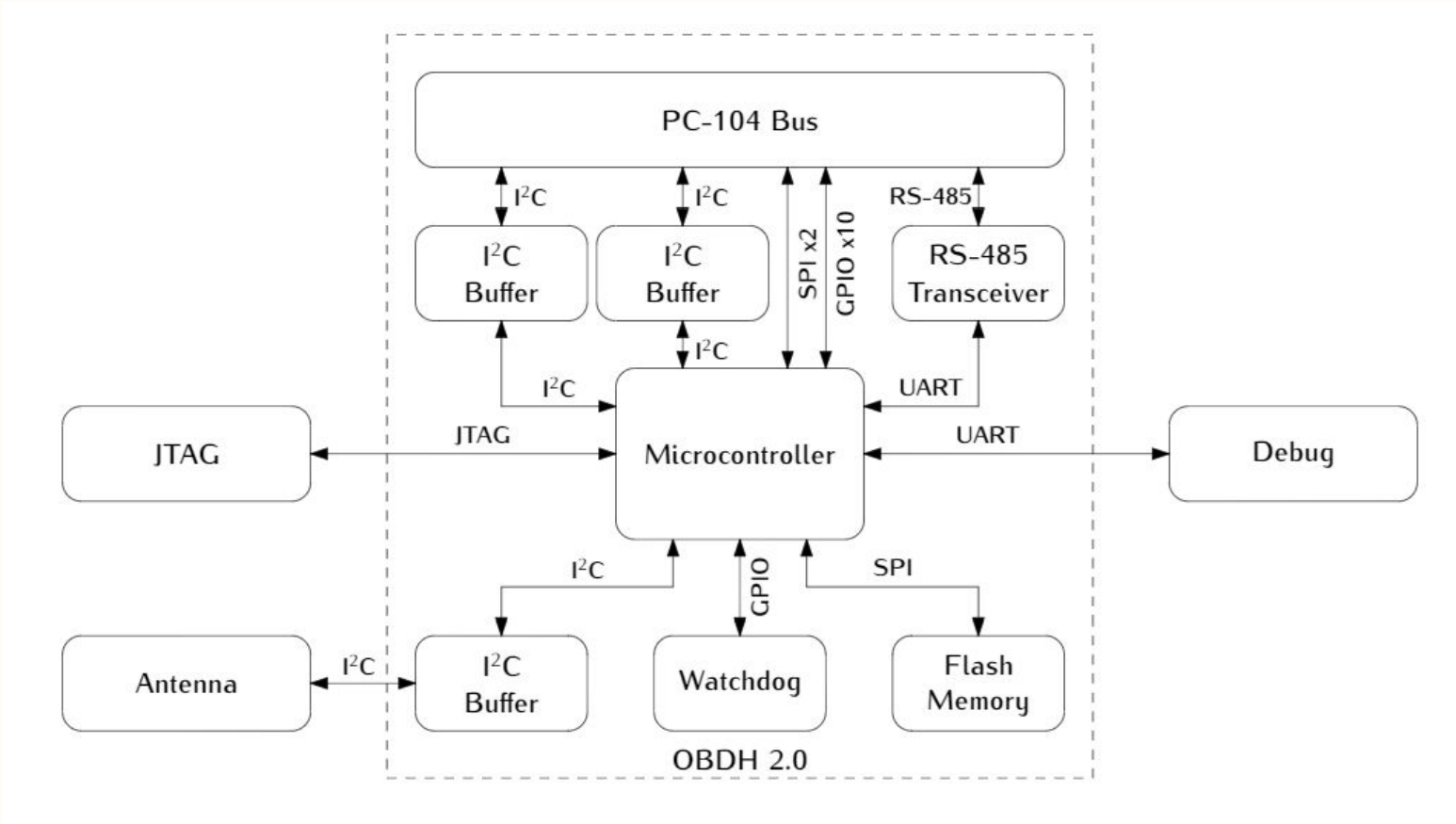
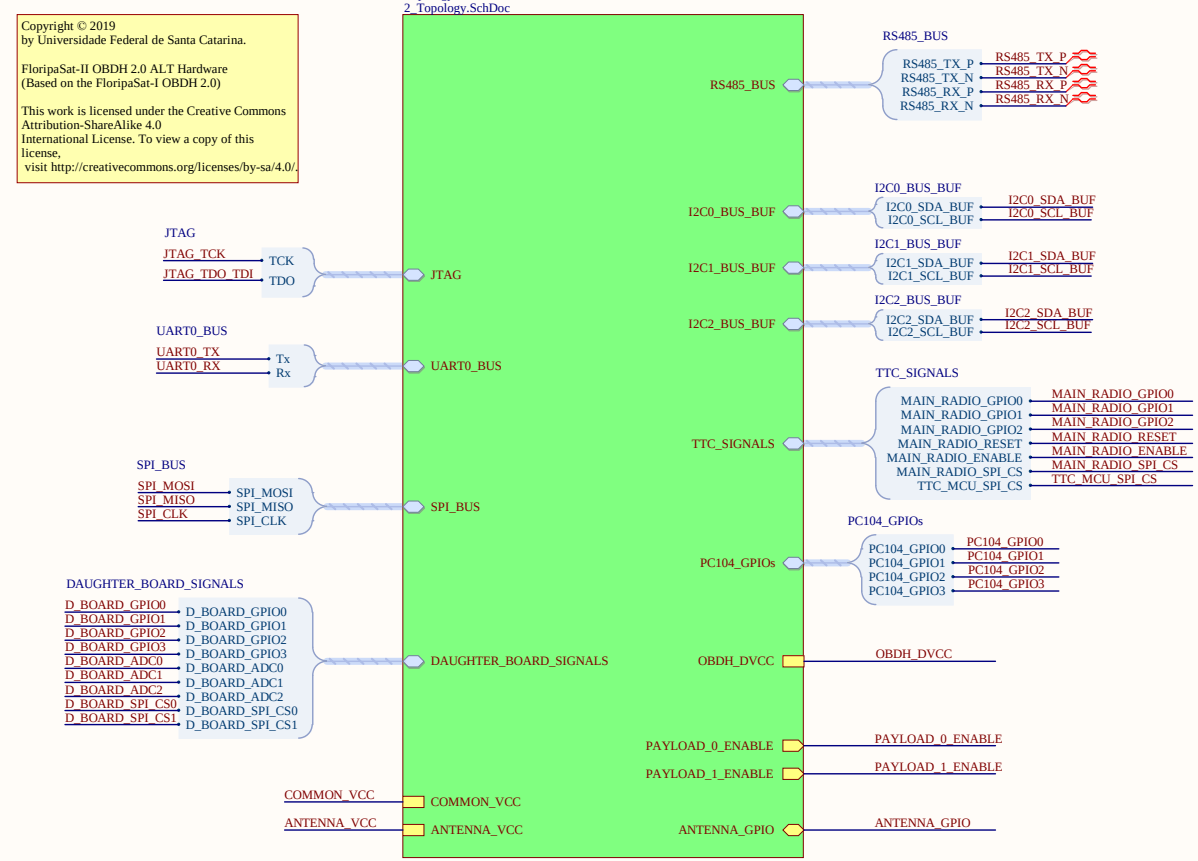
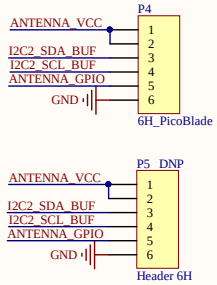


Title **OBDH Hardware Archictecture**			*UFSC - SpaceLab* *University Campus - Trindade* *Dep. of Electrical Engineering - CTC* *Florianópolis, Santa Catarina, Brazil* *CEP: 88040 - 900*
Size: A4	Project: FloripaSat	Revision:V0.1	
Date: 30/12/2019 Time: 02:01:24		Sheet0 of 7	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

Topology
2_Topology.SchDoc



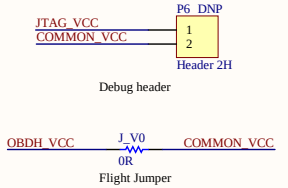
ANTENNA DEPLOYER INTERFACE



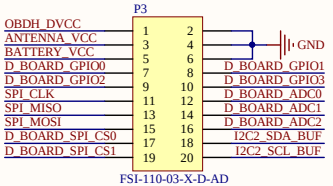
External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

POWER SUPPLY SOURCE SELECTOR
(from PC104 or JTAG)



DAUGHTER BOARD INTERFACE
(Generic Interface)

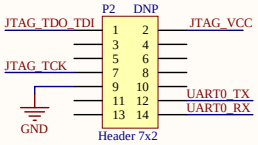


External Communication Buses Description:

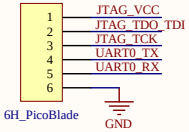
BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

PROGRAMMING HEADERS
(JTAG Spy Bi-Wire)



Debug JTAG Main MCU



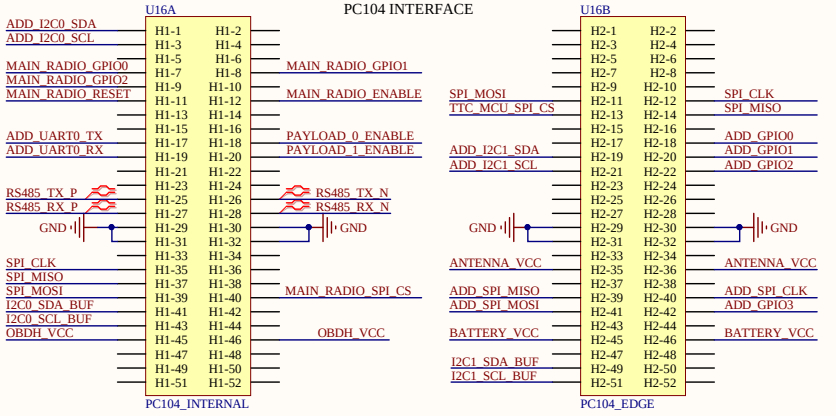
Flight Model JTAG Main MCU

External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

PC104 INTERFACE



External Communication Buses Description:

BUS1 (RS485): Payload EDC interface
Dedicated channel - UART1
PAYLOAD_0_ENABLE - Logical enable of the Payload EDC

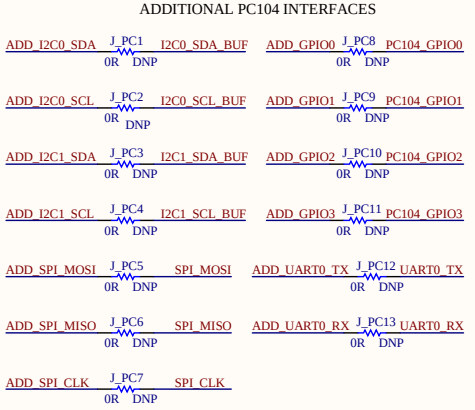
BUS2 (I2C): Payload X interface
Dedicated channel - I2C0
PAYLOAD_1_ENABLE - Logical enable of the Payload X

BUS3 (I2C): EPS interface
Dedicated channel - I2C1

BUS7 (SPI): TTC interface
Shared Channel - SPI
TTC_SPI_CS - TTC chip select

BUS8 (SPI): Main Radio interface
Shared Channel - SPI
MAIN_RADIO_SPI_CS - Main radio chip select
MAIN_RADIO_GPIOx - GPIO configuration pins
MAIN_RADIO_RESET - Main radio reset
MAIN_RADIO_ENABLE - Enable for the Main Radio regulator in EPS

ADDITIONAL PC104 INTERFACES



Additional Communication Buses Description:
(Used by demand, do not place unless necessary)

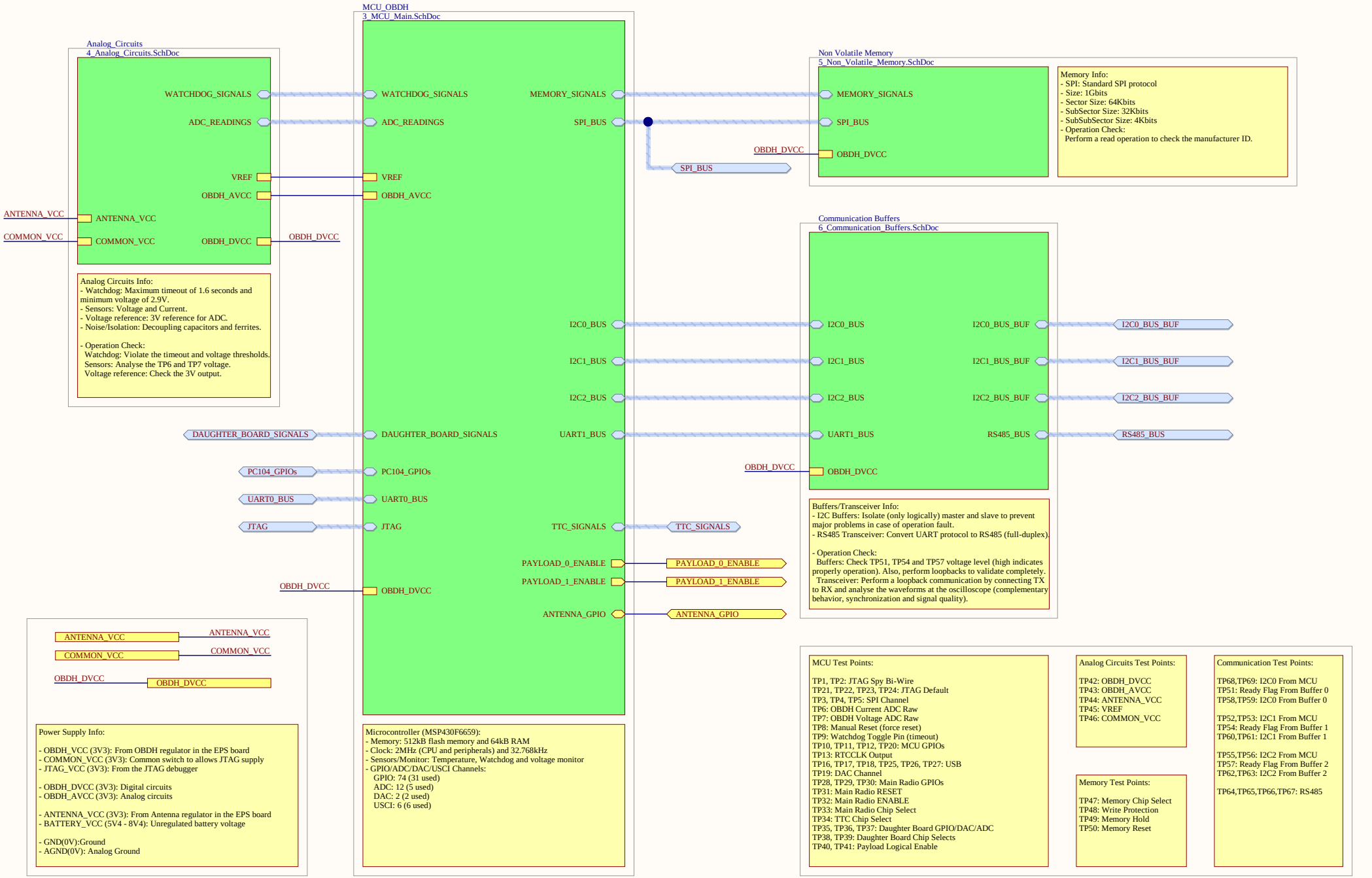
BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (UART): UART0
BUS14 (GPIO): 4 GPIOs

Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12

Allow PC104 flexibility and device sharing:
BUS13 - Require to desactivate debug routines.
BUS14 - Dedicated use of PC104.

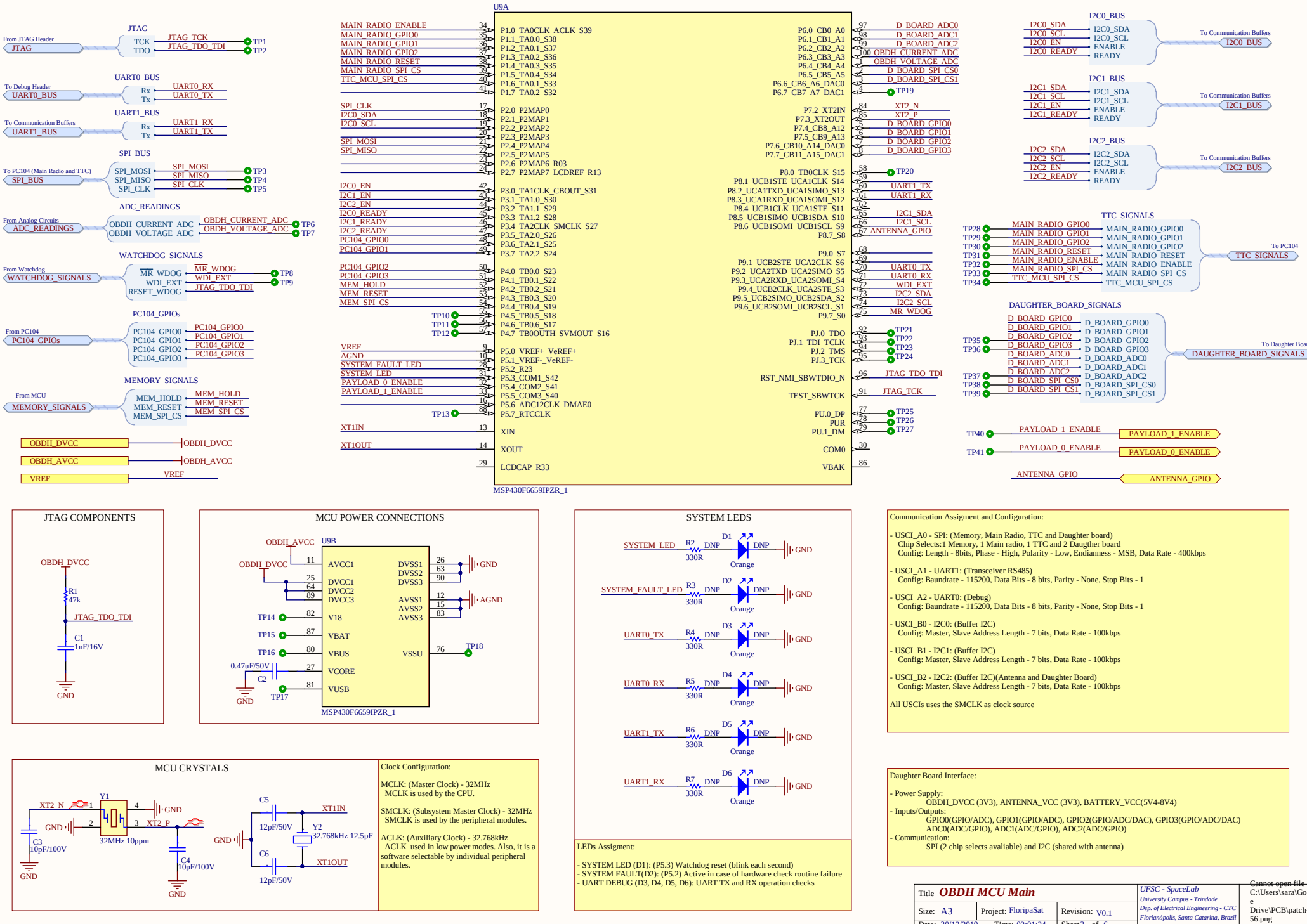
Title: **OBDH Interface**			*UFSC - SpaceLab*
Size: A3	Project: FloripaSat	Revision: V0.1	*University Campus - Trindade*
Date: 30/12/2019	Time: 02:01:24	Sheet 1 of 6	*Dep. of Electrical Engineering - CTC*
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

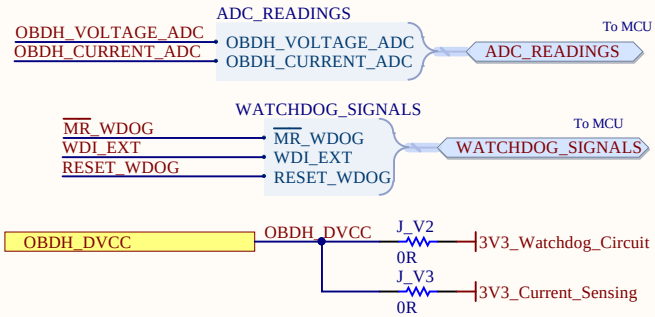
Cannot open file C:\Users\sara\Google Drive\PCB\patch-256.png



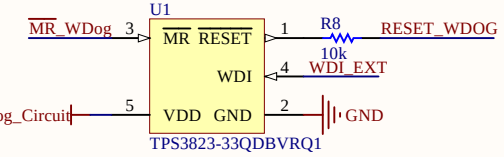
Title **OBDH Topology**			*UFSC - SpaceLab*
Size: A3	Project: FloripaSat	Revision: V0.1	*University Campus - Trindade*
Date: 30/12/2019	Time: 02:01:24	Sheet 2 of 6	*Dep. of Electrical Engineering - CTC*
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

Cannot open file C:\Users\sara\Google Drive\PCB\patch-256.png


JTAG
From JTAG Header
JTAG
TCK
TDO
JTAG_TCK
JTAG_TDO_TDI
TP1
TP2
UART0_BUS
To Debug Header
UART0_BUS
Rx
Tx
UART0_RX
UART0_TX
UART1_BUS
To Communication Buffers
UART1_BUS
Rx
Tx
UART1_RX
UART1_TX
SPI_BUS
To PC104 (Main Radio and TTC)
SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK
TP3
TP4
TP5
ADC_READINGS
From Analog Circuits
ADC_READINGS
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
TP6
TP7
WATCHDOG_SIGNALS
From Watchdog
WATCHDOG_SIGNALS
MR_WDOG
WDI_EXT
RESET_WDOG
JTAG_TDO_TDI
TP8
TP9
PC104_GPIOs
From PC104
PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
MEMORY_SIGNALS
From MCU
MEMORY_SIGNALS
MEM_HOLD
MEM_RESET
MEM_SPI_CS
OBDH_DVCC
OBDH_AVCC
VREF
U9A
MSP430F6659IPZR_1
MAIN_RADIO_ENABLE
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
SPI_CLK
I2C0_SDA
I2C0_SCL
SPI_MOSI
SPI_MISO
I2C0_EN
I2C1_EN
I2C2_EN
I2C0_READY
I2C1_READY
I2C2_READY
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
MEM_HOLD
MEM_RESET
MEM_SPI_CS
VREF
AGND
SYSTEM_FAULT_LED
SYSTEM_LED
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
XT1IN
XT1OUT
P1.0_TA0CLK_ACLK_S39
P1.1_TA0.0_S38
P1.2_TA0.1_S37
P1.3_TA0.2_S36
P1.4_TA0.3_S35
P1.5_TA0.4_S34
P1.6_TA0.1_S33
P1.7_TA0.2_S32
P2.0_P2MAP0
P2.1_P2MAP1
P2.2_P2MAP2
P2.3_P2MAP3
P2.4_P2MAP4
P2.5_P2MAP5
P2.6_P2MAP6_R03
P2.7_P2MAP7_LCDREF_R13
P3.0_TA1CLK_CBOUT_S31
P3.1_TA1.0_S30
P3.2_TA1.1_S29
P3.3_TA1.2_S28
P3.4_TA2CLK_SMCLK_S27
P3.5_TA2.0_S26
P3.6_TA2.1_S25
P3.7_TA2.2_S24
P4.0_TB0.0_S23
P4.1_TB0.1_S22
P4.2_TB0.2_S21
P4.3_TB0.3_S20
P4.4_TB0.4_S19
P4.5_TB0.5_S18
P4.6_TB0.6_S17
P4.7_TB0OUTH_SVMOUT_S16
P5.0_VREF+_VeREF+
P5.1_VREF-_VeREF-
P5.2_R23
P5.3_COM1_S42
P5.4_COM2_S41
P5.5_COM3_S40
P5.6_ADC12CLK_DMAE0
P5.7_RTCCLK
XIN
XOUT
LCDCAP_R33
P6.0_CB0_A0
P6.1_CB1_A1
P6.2_CB2_A2
P6.3_CB3_A3
P6.4_CB4_A4
P6.5_CB5_A5
P6.6_CB6_A6_DAC0
P6.7_CB7_A7_DAC1
P7.2_XT2IN
P7.3_XT2OUT
P7.4_CB8_A12
P7.5_CB9_A13
P7.6_CB10_A14_DAC0
P7.7_CB11_A15_DAC1
P8.0_TB0CLK_S15
P8.1_UCB1STE_UCA1CLK_S14
P8.2_UCA1TXD_UCA1SIMO_S13
P8.3_UCA1RXD_UCA1SOMI_S12
P8.4_UCB1CLK_UCA1STE_S11
P8.5_UCB1SIMO_UCB1SDA_S10
P8.6_UCB1SOMI_UCB1SCL_S9
P8.7_S8
P9.0_S7
P9.1_UCB2STE_UCA2CLK_S6
P9.2_UCA2TXD_UCA2SIMO_S5
P9.3_UCA2RXD_UCA2SOMI_S4
P9.4_UCB2CLK_UCA2STE_S3
P9.5_UCB2SIMO_UCB2SDA_S2
P9.6_UCB2SOMI_UCB2SCL_S1
P9.7_S0
PJ.0_TDO
PJ.1_TDI_TCLK
PJ.2_TMS
PJ.3_TCK
RST_NMI_SBWTDIO_N
TEST_SBWTCK
PU.0_DP
PUR
PU.1_DM
COM0
VBAK
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
TP19
XT2_N
XT2_P
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
TP20
UART1_TX
UART1_RX
I2C1_SDA
I2C1_SCL
ANTENNA_GPIO
UART0_TX
UART0_RX
WDI_EXT
I2C2_SDA
I2C2_SCL
MR_WDOG
TP21
TP22
TP23
TP24
JTAG_TDO_TDI
JTAG_TCK
TP25
TP26
TP27
I2C0_BUS
I2C0_SDA
I2C0_SCL
ENABLE
READY
To Communication Buffers
I2C0_BUS
I2C1_BUS
I2C1_SDA
I2C1_SCL
ENABLE
READY
To Communication Buffers
I2C1_BUS
I2C2_BUS
I2C2_SDA
I2C2_SCL
ENABLE
READY
To Communication Buffers
I2C2_BUS
TTC_SIGNALS
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
To PC104
TTC_SIGNALS
DAUGHTER_BOARD_SIGNALS
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
To Daughter Board
DAUGHTER_BOARD_SIGNALS
PAYLOAD_1_ENABLE
PAYLOAD_0_ENABLE
ANTENNA_GPIO
JTAG COMPONENTS
OBDH_DVCC
R1
47k
JTAG_TDO_TDI
C1
1nF/16V
GND
MCU POWER CONNECTIONS
OBDH_AVCC
OBDH_DVCC
U9B
MSP430F6659IPZR_1
AVCC1
DVCC1
DVCC2
DVCC3
V18
VBAT
VBUS
VCORE
VUSB
DVSS1
DVSS2
DVSS3
AVSS1
AVSS2
AVSS3
VSSU
GND
AGND
TP14
TP15
TP16
TP17
TP18
0.47uF/50V
C2
MCU CRYSTALS
XT2_N
Y1
32MHz 10ppm
XT2_P
C3
10pF/100V
C4
10pF/100V
C5
12pF/50V
C6
12pF/50V
XT1IN
Y2
32.768kHz 12.5pF
XT1OUT
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
SYSTEM LEDS
SYSTEM_LED
SYSTEM_FAULT_LED
UART0_TX
UART0_RX
UART1_TX
UART1_RX
R2
R3
R4
R5
R6
R7
330R
DNP
D1
D2
D3
D4
D5
D6
Orange
GND
LEDs Assigment:
- SYSTEM LED (D1): (P5.3) Watchdog reset (blink each second)
- SYSTEM FAULT(D2): (P5.2) Active in case of hardware check routine failure
- UART DEBUG (D3, D4, D5, D6): UART TX and RX operation checks
Communication Assigment and Configuration:
- USCI_A0 - SPI: (Memory, Main Radio, TTC and Daughter board)
Chip Selects:1 Memory, 1 main radio, 1 TTC and 2 Daugther board
Config: Length - 8bits, Phase - High, Polarity - Low, Endianness - MSB, Data Rate - 400kbps
- USCI_A1 - UART1: (Transceiver RS485)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_A2 - UART0: (Debug)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_B0 - I2C0: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B1 - I2C1: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B2 - I2C2: (Buffer I2C)(Antenna and Daughter Board)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
All USCIs uses the SMCLK as clock source
Daughter Board Interface:
- Power Supply:
OBDH_DVCC (3V3), ANTENNA_VCC (3V3), BATTERY_VCC(5V4-8V4)
- Inputs/Outputs:
GPIO0(GPIO/ADC), GPIO1(GPIO/ADC), GPIO2(GPIO/ADC/DAC), GPIO3(GPIO/ADC/DAC)
ADC0(ADC/GPIO), ADC1(ADC/GPIO), ADC2(ADC/GPIO)
- Communication:
SPI (2 chip selects avaliable) and I2C (shared with antenna)
Title
OBDH MCU Main
Size: A3
Project: FloripaSat
Revision: V0.1
Date: 30/12/2019
Time: 02:01:24
Sheet 3 of 6
Drawn by: André M. P. Mattos
Model: Eng_2_ALT
UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900
Cannot open file C:\Users\sara\Google Drive\PCB\patch-256.png

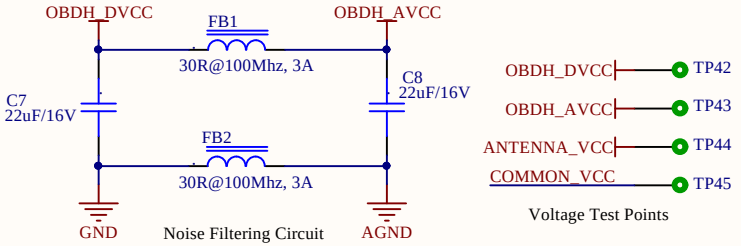


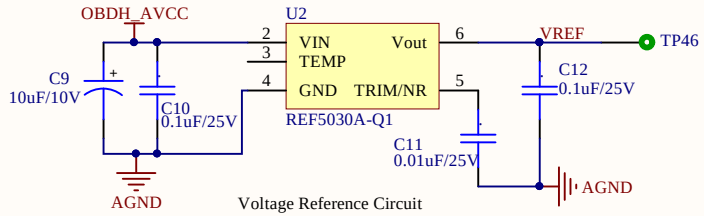
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER



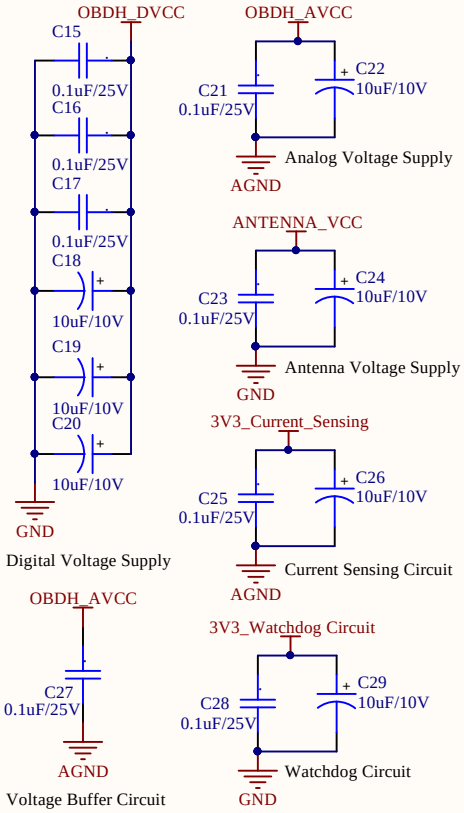
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

VOLTAGE REFERENCES



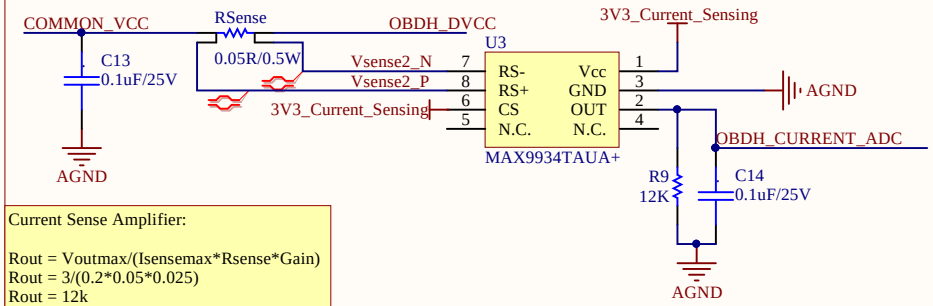


DECOUPLING CAPACITORS



INTERNAL MEASUREMENT CIRCUITS

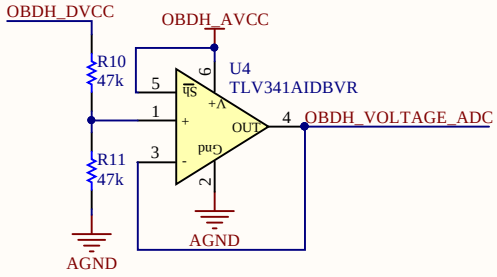
Current Sensing Circuit



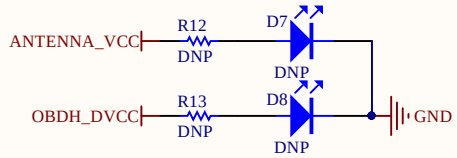
Current Sense Amplifier:

Rout = Voutmax/(Isensemax*Rsense*Gain)
Rout = 3/(0.2*0.05*0.025)
Rout = 12k

Voltage Buffer Circuit



LEDS SYSTEM



Title: **Analog Circuits**			
Size: A4	Project: FloripaSat	Revision: V0.1	
Date: 30/12/2019	Time: 02:01:25	Sheet 4 of 6	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

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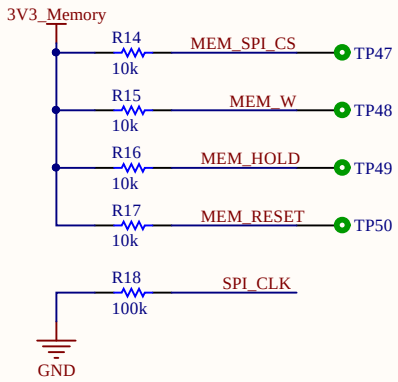
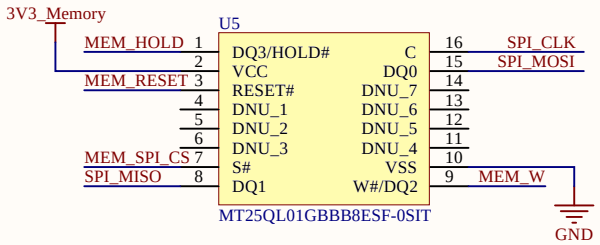
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

PULL-UP AND PULL-DOWN RESISTORS



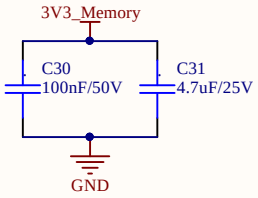
NON-VOLATILE MEMORY

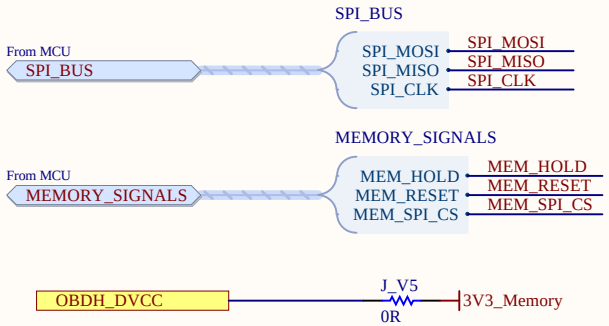


Memory Operation:

To be defined

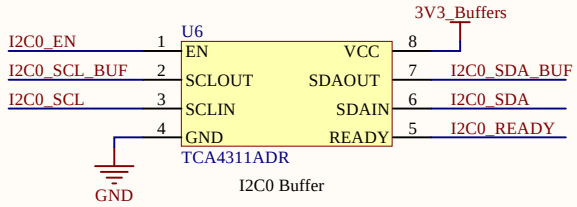
DECOUPLING CAPACITORS





Title **Non Volatile Memory**			*UFSC - SpaceLab*
Size: A4	Project: FloripaSat	Revision:V0.1	*University Campus - Trindade*
Date: 30/12/2019	Time: 02:01:25	Sheet5 of 6	*Dep. of Electrical Engineering - CTC*
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

I2C BUFFERS



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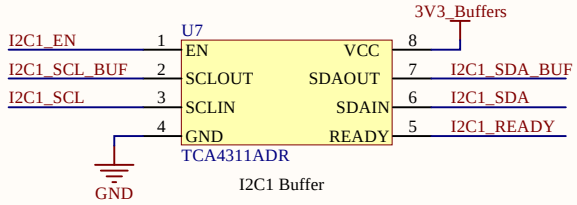
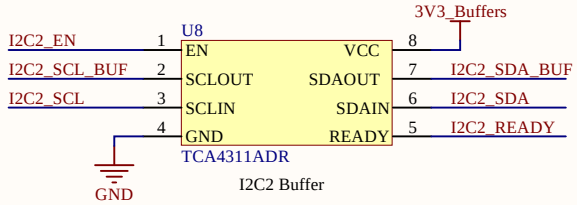
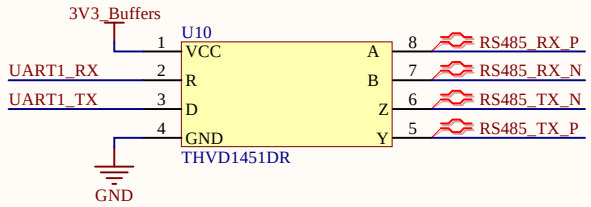


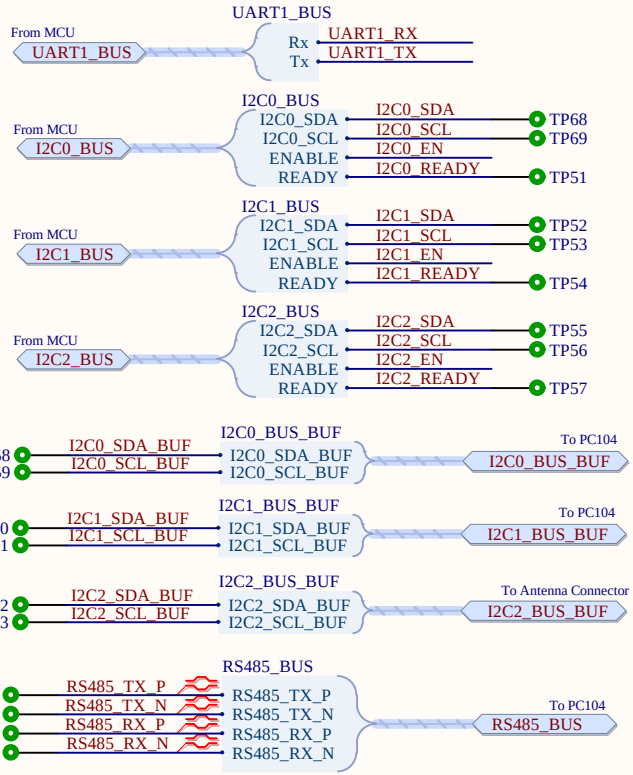
I2C1 Buffer



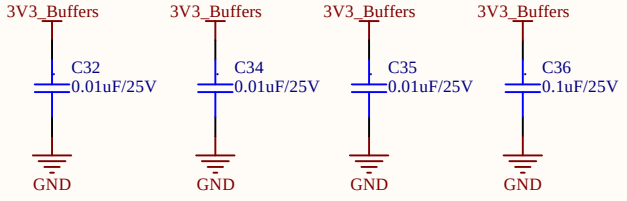
I2C2 Buffer

RS485 TRANSCEIVER (Full-Duplex)



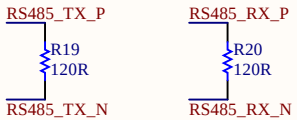


DECOUPLING CAPACITORS

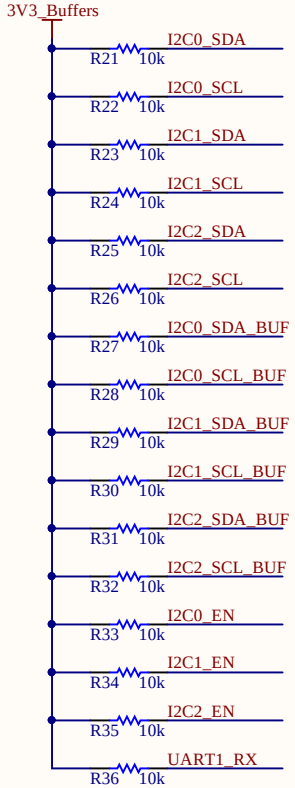


I2C0 Buffer | I2C1 Buffer | I2C2 Buffer | RS485 Transceiver

TERMINATION RESISTORS



PULL-UP RESISTORS



Title: **Communication Buffers**		
Size: A4	Project: FloripaSat	Revision: V0.1
Date: 30/12/2019 Time: 02:01:25		Sheet 6 of 6
Drawn By: André M. P. Mattos		Model: Eng_2_ALT

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