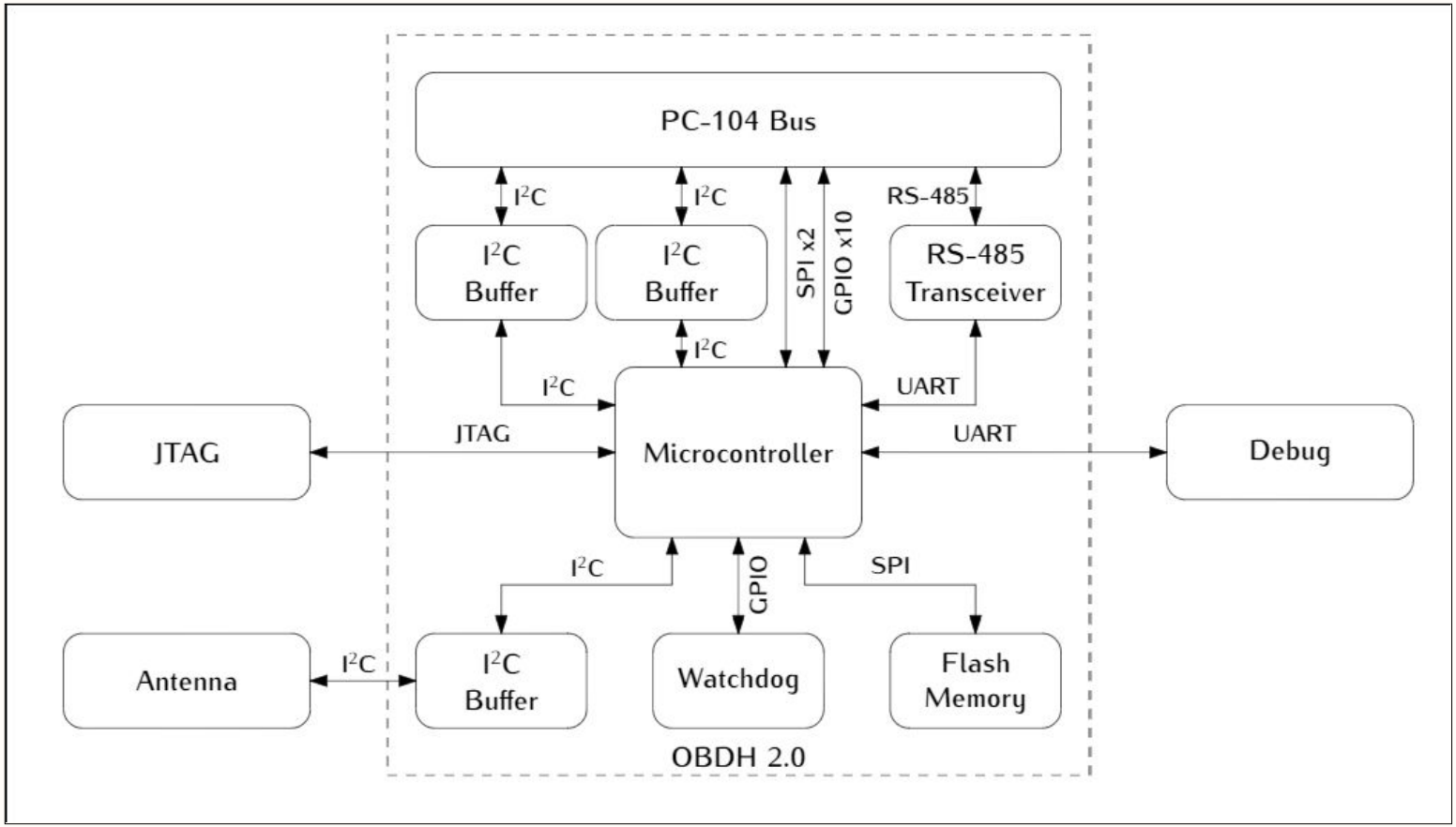

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FloripaSat-II OBDH 2.0 ALT Hardware
Based on the FloripaSat-I OBDH 2.0

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FloripaSat-II OBDH 2.0 ALT Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Cezar A. Rigo, Kleber Gouveia and Amanda B. Medeiros
- Based on FloripaSat-I OBDH designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Title ***OBDH Hardware Archictecture***		*UFSC - SpaceLab*
Size: A4	Project: FloripaSat	Revision:V0.2
Date: 11/01/2020 Time: 00:18:11		Sheet0 of 7
Drawn By: André M. P. Mattos		Model: Eng_2_ALT

University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

Topology
2_Topology.SchDoc

RS485_BUS
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N

I2C0_BUS_BUF
I2C0_SDA_BUF
I2C0_SCL_BUF

I2C1_BUS_BUF
I2C1_SDA_BUF
I2C1_SCL_BUF

I2C2_BUS_BUF
I2C2_SDA_BUF
I2C2_SCL_BUF

JTAG
JTAG_TCK
JTAG_TDO_TDI
TCK
TDO

UART0_BUS
UART0_TX
UART0_RX
Tx
Rx

TTC_SIGNALS
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS

SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK

PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3

DAUGHTER_BOARD_SIGNALS
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1

OBDH_DVCC
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
COMMON_VCC
ANTENNA_VCC
ANTENNA_GPIO

ESD PROTECTION
(Connected to the structure)
ESD
R_ESD
1M
GND

ANTENNA DEPLOYER INTERFACE
P4
ANTENNA_VCC
I2C2_SDA_BUF
I2C2_SCL_BUF
ANTENNA_GPIO
GND
6H_PicoBlade
P5_DNP
Header 6H

External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

POWER SUPPLY SOURCE SELECTOR
(from PC104 or JTAG)
P6_DNP
JTAG_VCC
COMMON_VCC
Header 2H
Debug header
OBDH_VCC
J_V0
0R
COMMON_VCC
Flight Jumper

PROGRAMMING HEADERS
(JTAG Spy Bi-Wire)
P2
DNP
JTAG_TDO_TDI
JTAG_TCK
JTAG_VCC
UART0_TX
UART0_RX
GND
Header 7x2
Debug JTAG Main MCU
P1
6H_PicoBlade
Flight Model JTAG Main MCU

DAUGHTER BOARD INTERFACE
(Generic Interface)
P3
OBDH_DVCC
ANTENNA_VCC
BATTERY_VCC
D_BOARD_GPIO0
D_BOARD_GPIO2
SPI_CLK
SPI_MISO
SPI_MOSI
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
D_BOARD_GPIO1
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
I2C2_SDA_BUF
I2C2_SCL_BUF
FSI-110-03-X-D-AD

External Communication Buses Description:

BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

PC104 INTERFACE
U16A
ADD_I2C0_SDA
ADD_I2C0_SCL
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
ADD_UART0_TX
ADD_UART0_RX
RS485_RX_P
RS485_TX_N
GND
SPI_CLK
SPI_MISO
SPI_MOSI
I2C0_SDA_BUF
I2C0_SCL_BUF
OBDH_VCC
MAIN_RADIO_GPIO1
MAIN_RADIO_ENABLE
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
RS485_RX_N
RS485_TX_P
GND
MAIN_RADIO_SPI_CS
OBDH_VCC
PC104_INTERNAL

U16B
SPI_MOSI
TTC_MCU_SPI_CS
ADD_I2C1_SDA
ADD_I2C1_SCL
GND
ANTENNA_VCC
ADD_SPI_MISO
ADD_SPI_MOSI
BATTERY_VCC
I2C1_SDA_BUF
I2C1_SCL_BUF
SPI_CLK
SPI_MISO
ADD_GPIO0
ADD_GPIO1
ADD_GPIO2
GND
ANTENNA_VCC
ADD_SPI_CLK
ADD_GPIO3
BATTERY_VCC
PC104_EDGE

External Communication Buses Description:

BUS1 (RS485): Payload EDC interface
Dedicated channel - UART1
PAYLOAD_0_ENABLE - Logical enable of the Payload EDC

BUS2 (I2C): Payload X interface
Dedicated channel - I2C0
PAYLOAD_1_ENABLE - Logical enable of the Payload X

BUS3 (I2C): EPS interface
Dedicated channel - I2C1

BUS7 (SPI)(H2): TTC interface
Shared Channel - SPI
TTC_SPI_CS - TTC chip select

BUS8 (SPI)(H1): Main Radio interface
Shared Channel - SPI
MAIN_RADIO_SPI_CS - Main radio chip select
MAIN_RADIO_GPIOx - GPIO configuration pins
MAIN_RADIO_RESET - Main radio reset
MAIN_RADIO_ENABLE - Enable for the Main Radio regulator in EPS

ADDITIONAL PC104 INTERFACES
ADD_I2C0_SDA J_PC1 I2C0_SDA_BUF 0R DNP
ADD_I2C0_SCL J_PC2 I2C0_SCL_BUF 0R DNP
ADD_I2C1_SDA J_PC3 I2C1_SDA_BUF 0R DNP
ADD_I2C1_SCL J_PC4 I2C1_SCL_BUF 0R DNP
ADD_SPI_MOSI J_PC5 SPI_MOSI 0R DNP
ADD_SPI_MISO J_PC6 SPI_MISO 0R DNP
ADD_SPI_CLK J_PC7 SPI_CLK 0R DNP
ADD_GPIO0 J_PC8 PC104_GPIO0 0R DNP
ADD_GPIO1 J_PC9 PC104_GPIO1 0R DNP
ADD_GPIO2 J_PC10 PC104_GPIO2 0R DNP
ADD_GPIO3 J_PC11 PC104_GPIO3 0R DNP
ADD_UART0_TX J_PC12 UART0_TX 0R DNP
ADD_UART0_RX J_PC13 UART0_RX 0R DNP

Additional Communication Buses Description:
(Used by demand, do not place unless necessary)

BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (UART): UART0
BUS14 (GPIO): 4 GPIOs

Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12

Allow PC104 flexibility and device sharing:
BUS13 - Require to desactivate debug routines.
BUS14 - Dedicated use of PC104.

Title	**OBDH Interface**		
Size: A3	Project: FloripaSat	Revision: V0.2	
Date: 11/01/2020	Time: 00:18:11	Sheet 1 of 6	
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	

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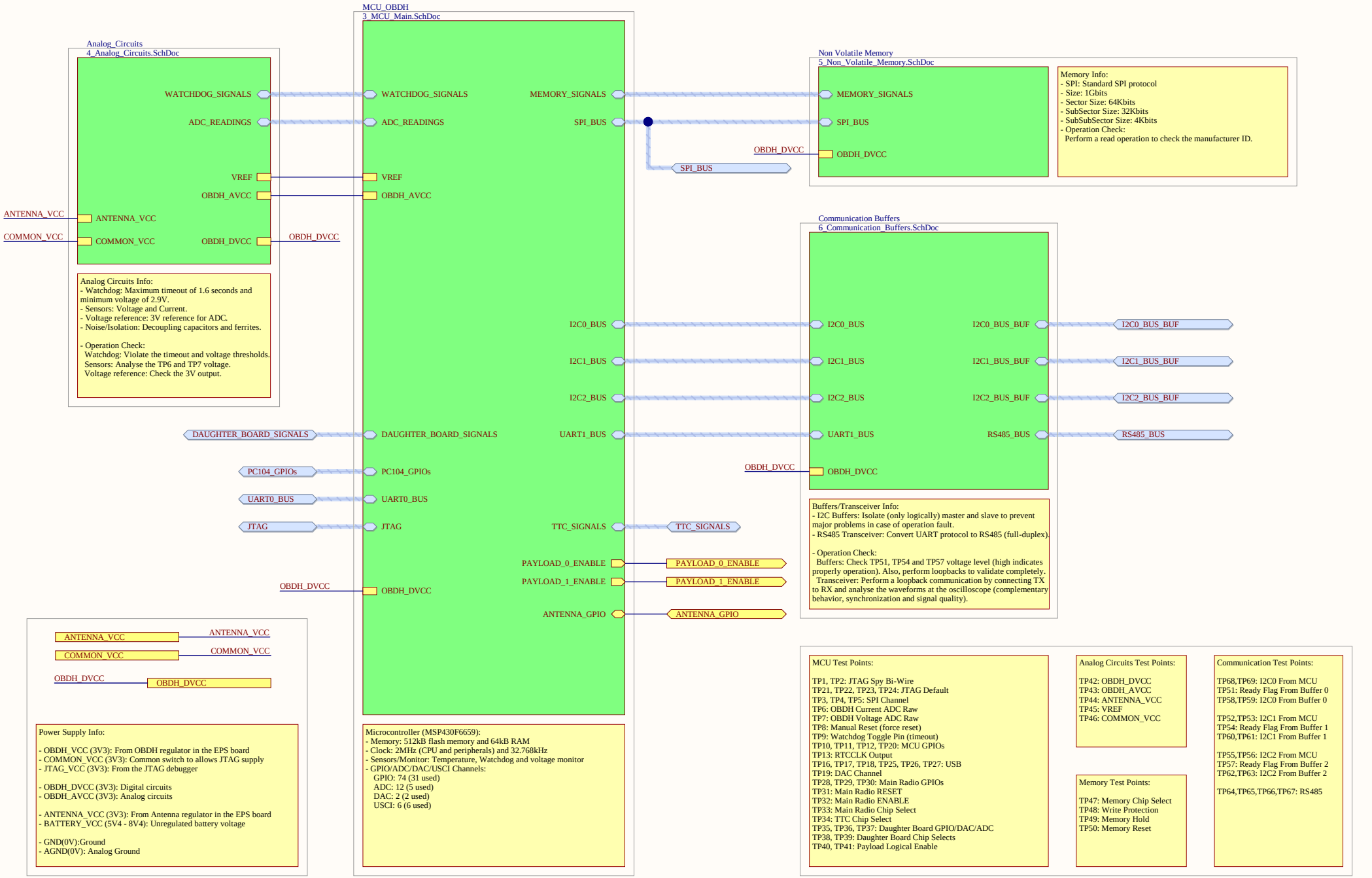

Title **OBDH Topology**		
Size: A3	Project: FloripaSat	Revision: V0.2
Date: 11/01/2020	Time: 00:18:11	Sheet 2 of 6
Drawn by: André M. P. Mattos		Model: Eng_2_ALT

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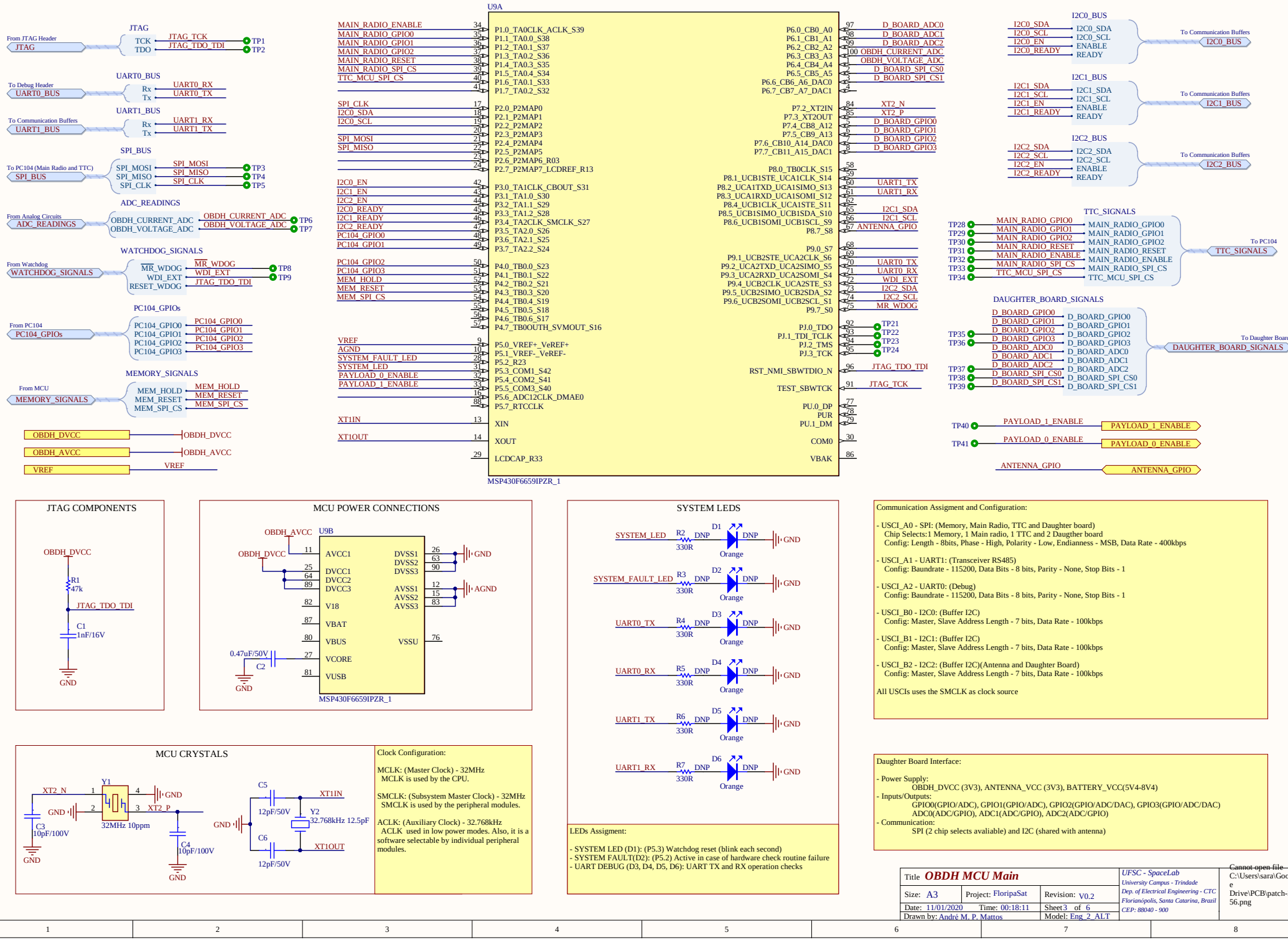
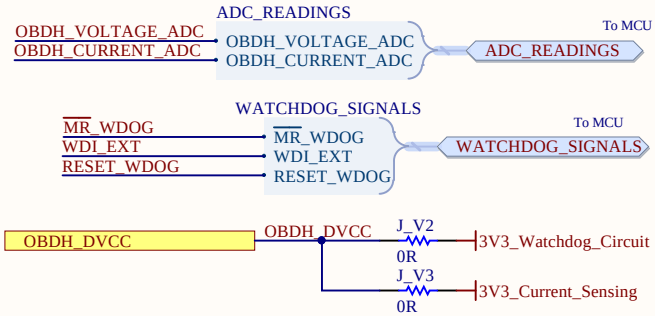
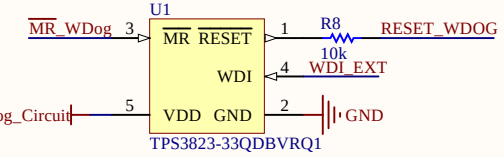

JTAG
From JTAG Header
JTAG
TCK
TDO
JTAG_TCK
JTAG_TDO_TDI
TP1
TP2
UART0_BUS
To Debug Header
UART0_BUS
Rx
Tx
UART0_RX
UART0_TX
UART1_BUS
To Communication Buffers
UART1_BUS
Rx
Tx
UART1_RX
UART1_TX
SPI_BUS
To PC104 (Main Radio and TTC)
SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_CLK
TP3
TP4
TP5
ADC_READINGS
From Analog Circuits
ADC_READINGS
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
TP6
TP7
WATCHDOG_SIGNALS
From Watchdog
WATCHDOG_SIGNALS
MR_WDOG
WDI_EXT
RESET_WDOG
MR_WDOG
WDI_EXT
JTAG_TDO_TDI
TP8
TP9
PC104_GPIOs
From PC104
PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
MEMORY_SIGNALS
From MCU
MEMORY_SIGNALS
MEM_HOLD
MEM_RESET
MEM_SPI_CS
MEM_HOLD
MEM_RESET
MEM_SPI_CS
OBDH_DVCC
OBDH_DVCC
OBDH_AVCC
OBDH_AVCC
VREF
VREF
U9A
MAIN_RADIO_ENABLE
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
SPI_CLK
I2C0_SDA
I2C0_SCL
SPI_MOSI
SPI_MISO
I2C0_EN
I2C1_EN
I2C2_EN
I2C0_READY
I2C1_READY
I2C2_READY
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
MEM_HOLD
MEM_RESET
MEM_SPI_CS
VREF
AGND
SYSTEM_FAULT_LED
SYSTEM_LED
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
XT1IN
XT1OUT
P1.0_TA0CLK_ACLK_S39
P1.1_TA0.0_S38
P1.2_TA0.1_S37
P1.3_TA0.2_S36
P1.4_TA0.3_S35
P1.5_TA0.4_S34
P1.6_TA0.1_S33
P1.7_TA0.2_S32
P2.0_P2MAP0
P2.1_P2MAP1
P2.2_P2MAP2
P2.3_P2MAP3
P2.4_P2MAP4
P2.5_P2MAP5
P2.6_P2MAP6_R03
P2.7_P2MAP7_LCDREF_R13
P3.0_TA1CLK_CBOUT_S31
P3.1_TA1.0_S30
P3.2_TA1.1_S29
P3.3_TA1.2_S28
P3.4_TA2CLK_SMCLK_S27
P3.5_TA2.0_S26
P3.6_TA2.1_S25
P3.7_TA2.2_S24
P4.0_TB0.0_S23
P4.1_TB0.1_S22
P4.2_TB0.2_S21
P4.3_TB0.3_S20
P4.4_TB0.4_S19
P4.5_TB0.5_S18
P4.6_TB0.6_S17
P4.7_TB0OUTH_SVMOUT_S16
P5.0_VREF+_VeREF+
P5.1_VREF-_VeREF-
P5.2_R23
P5.3_COM1_S42
P5.4_COM2_S41
P5.5_COM3_S40
P5.6_ADC12CLK_DMAE0
P5.7_RTCCLK
XIN
XOUT
LCDCAP_R33
P6.0_CB0_A0
P6.1_CB1_A1
P6.2_CB2_A2
P6.3_CB3_A3
P6.4_CB4_A4
P6.5_CB5_A5
P6.6_CB6_A6_DAC0
P6.7_CB7_A7_DAC1
P7.2_XT2IN
P7.3_XT2OUT
P7.4_CB8_A12
P7.5_CB9_A13
P7.6_CB10_A14_DAC0
P7.7_CB11_A15_DAC1
P8.0_TB0CLK_S15
P8.1_UCB1STE_UCA1CLK_S14
P8.2_UCA1TXD_UCA1SIMO_S13
P8.3_UCA1RXD_UCA1SOMI_S12
P8.4_UCB1CLK_UCA1STE_S11
P8.5_UCB1SIMO_UCB1SDA_S10
P8.6_UCB1SOMI_UCB1SCL_S9
P8.7_S8
P9.0_S7
P9.1_UCB2STE_UCA2CLK_S6
P9.2_UCA2TXD_UCA2SIMO_S5
P9.3_UCA2RXD_UCA2SOMI_S4
P9.4_UCB2CLK_UCA2STE_S3
P9.5_UCB2SIMO_UCB2SDA_S2
P9.6_UCB2SOMI_UCB2SCL_S1
P9.7_S0
PJ.0_TDO
PJ.1_TDI_TCLK
PJ.2_TMS
PJ.3_TCK
RST_NMI_SBWTDIO_N
TEST_SBWTCK
PU.0_DP
PUR
PU.1_DM
COM0
VBAK
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
XT2_N
XT2_P
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
UART1_TX
UART1_RX
I2C1_SDA
I2C1_SCL
ANTENNA_GPIO
UART0_TX
UART0_RX
WDI_EXT
I2C2_SDA
I2C2_SCL
MR_WDOG
TP21
TP22
TP23
TP24
JTAG_TDO_TDI
JTAG_TCK
MSP430F6659IPZR_1
I2C0_BUS
I2C0_SDA
I2C0_SCL
I2C0_EN
I2C0_READY
I2C0_SDA
I2C0_SCL
ENABLE
READY
To Communication Buffers
I2C0_BUS
I2C1_BUS
I2C1_SDA
I2C1_SCL
I2C1_EN
I2C1_READY
I2C1_SDA
I2C1_SCL
ENABLE
READY
To Communication Buffers
I2C1_BUS
I2C2_BUS
I2C2_SDA
I2C2_SCL
I2C2_EN
I2C2_READY
I2C2_SDA
I2C2_SCL
ENABLE
READY
To Communication Buffers
I2C2_BUS
TTC_SIGNALS
TP28
TP29
TP30
TP31
TP32
TP33
TP34
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
To PC104
TTC_SIGNALS
DAUGHTER_BOARD_SIGNALS
TP35
TP36
TP37
TP38
TP39
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
To Daughter Board
DAUGHTER_BOARD_SIGNALS
TP40
TP41
PAYLOAD_1_ENABLE
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
PAYLOAD_0_ENABLE
ANTENNA_GPIO
ANTENNA_GPIO
JTAG COMPONENTS
OBDH_DVCC
R1
47k
JTAG_TDO_TDI
C1
1nF/16V
GND
MCU POWER CONNECTIONS
OBDH_AVCC
U9B
OBDH_DVCC
AVCC1
DVCC1
DVCC2
DVCC3
V18
VBAT
VBUS
VCORE
VUSB
DVSS1
DVSS2
DVSS3
AVSS1
AVSS2
AVSS3
VSSU
GND
AGND
0.47uF/50V
C2
GND
MSP430F6659IPZR_1
SYSTEM LEDS
SYSTEM_LED
SYSTEM_FAULT_LED
UART0_TX
UART0_RX
UART1_TX
UART1_RX
R2
R3
R4
R5
R6
R7
330R
DNP
D1
D2
D3
D4
D5
D6
Orange
GND
LEDs Assigment:
- SYSTEM LED (D1): (P5.3) Watchdog reset (blink each second)
- SYSTEM FAULT(D2): (P5.2) Active in case of hardware check routine failure
- UART DEBUG (D3, D4, D5, D6): UART TX and RX operation checks
Communication Assigment and Configuration:
- USCI_A0 - SPI: (Memory, Main Radio, TTC and Daughter board)
Chip Selects:1 Memory, 1 Main radio, 1 TTC and 2 Daugther board
Config: Length - 8bits, Phase - High, Polarity - Low, Endianness - MSB, Data Rate - 400kbps
- USCI_A1 - UART1: (Transceiver RS485)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_A2 - UART0: (Debug)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_B0 - I2C0: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B1 - I2C1: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B2 - I2C2: (Buffer I2C)(Antenna and Daughter Board)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
All USCIs uses the SMCLK as clock source
MCU CRYSTALS
XT2_N
Y1
32MHz 10ppm
XT2_P
C3
10pF/100V
C4
10pF/100V
GND
C5
12pF/50V
XT1IN
Y2
32.768kHz 12.5pF
C6
12pF/50V
XT1OUT
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
Daughter Board Interface:
- Power Supply:
OBDH_DVCC (3V3), ANTENNA_VCC (3V3), BATTERY_VCC(5V4-8V4)
- Inputs/Outputs:
GPIO0(GPIO/ADC), GPIO1(GPIO/ADC), GPIO2(GPIO/ADC/DAC), GPIO3(GPIO/ADC/DAC)
ADC0(ADC/GPIO), ADC1(ADC/GPIO), ADC2(ADC/GPIO)
- Communication:
SPI (2 chip selects avaliable) and I2C (shared with antenna)
Title
OBDH MCU Main
Size: A3
Project: FloripaSat
Revision: V0.2
Date: 11/01/2020
Time: 00:18:11
Sheet 3 of 6
Drawn by: André M. P. Mattos
Model: Eng_2_ALT
UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900
Cannot open file C:\Users\sara\Google Drive\PCB\patch-256.png

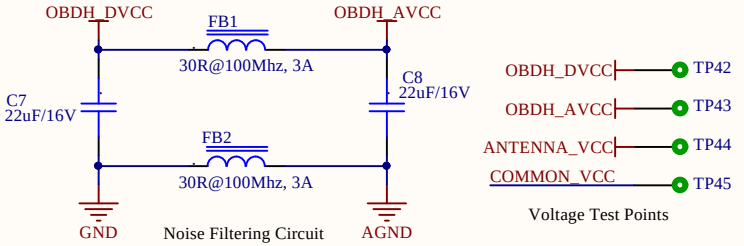


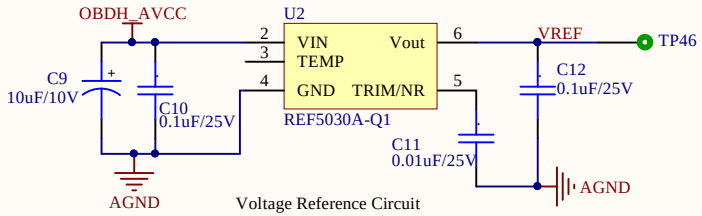
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER



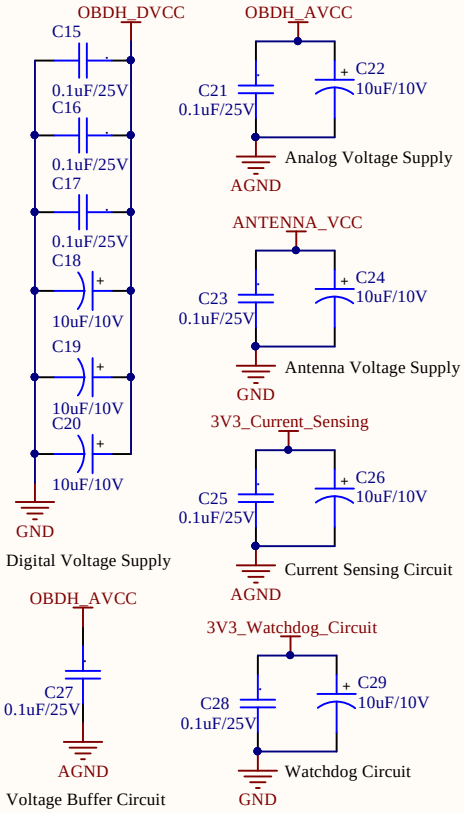
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

VOLTAGE REFERENCES



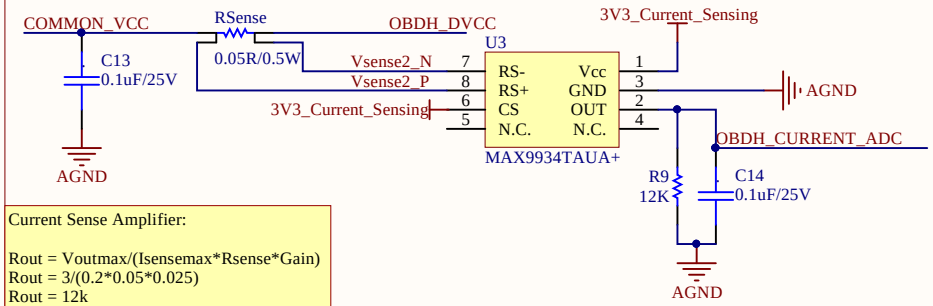


DECOUPLING CAPACITORS



INTERNAL MEASUREMENT CIRCUITS

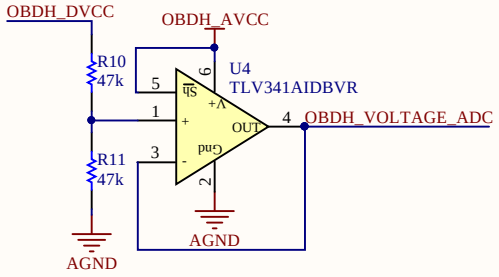
Current Sensing Circuit



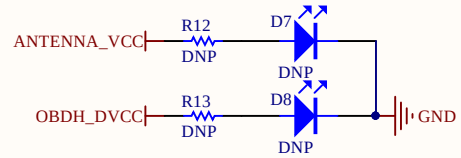
Current Sense Amplifier:

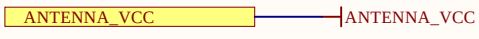
Rout = Voutmax/(Isensemax*Rsense*Gain)
Rout = 3/(0.2*0.05*0.025)
Rout = 12k

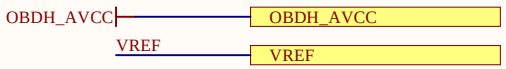
Voltage Buffer Circuit



LEDS SYSTEM







Title: **Analog Circuits**			
Size: A4	Project: FloripaSat	Revision: V0.2	
Date: 11/01/2020	Time: 00:18:11	Sheet 4 of 6	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

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Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
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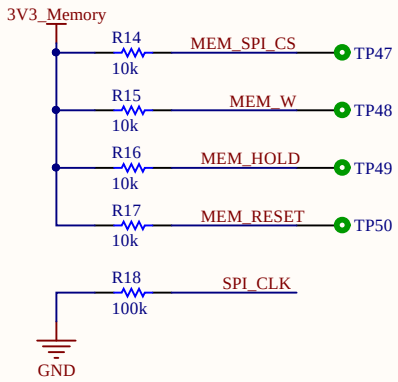
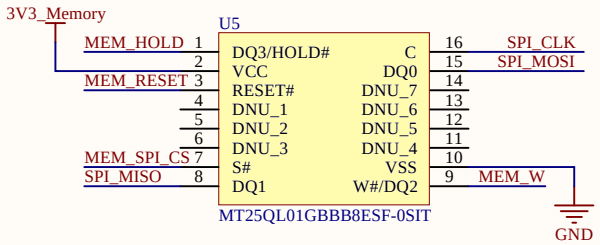
PULL-UP AND PULL-DOWN RESISTORS



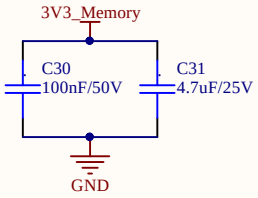
NON-VOLATILE MEMORY

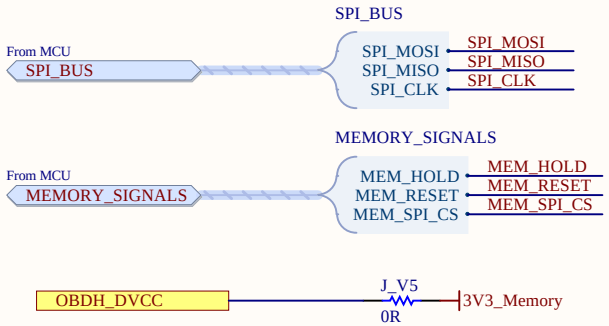


Memory Operation:

To be defined

DECOUPLING CAPACITORS





Title	***Non Volatile Memory***		
Size: A4	Project: FloripaSat	Revision: V0.2	
Date: 11/01/2020	Time: 00:18:12	Sheet 5 of 6	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

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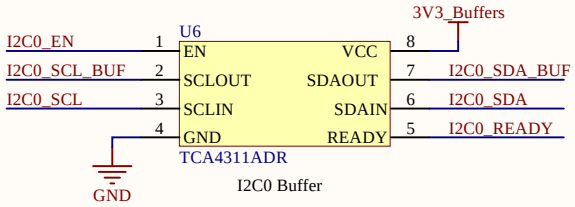
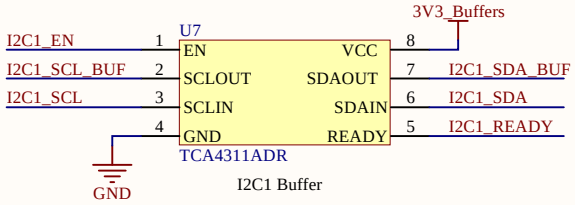
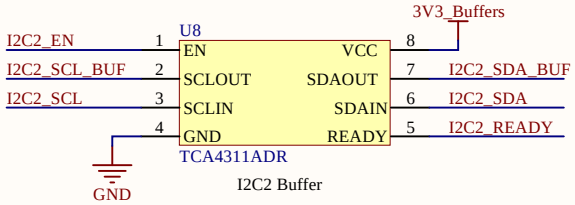
I2C BUFFERS



I2C0 Buffer

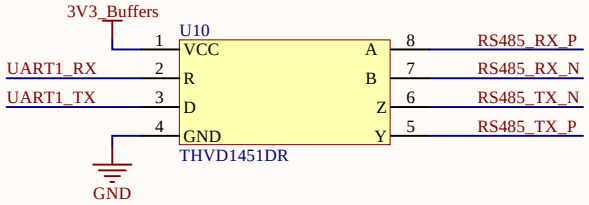


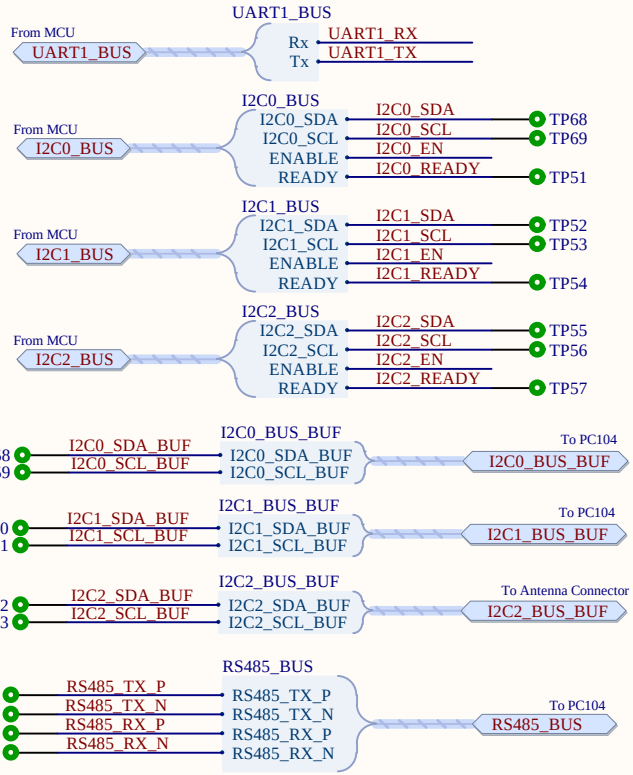
I2C1 Buffer



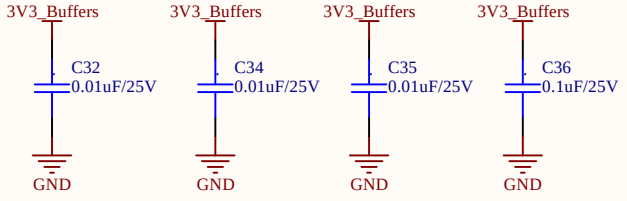
I2C2 Buffer

RS485 TRANSCEIVER (Full-Duplex)



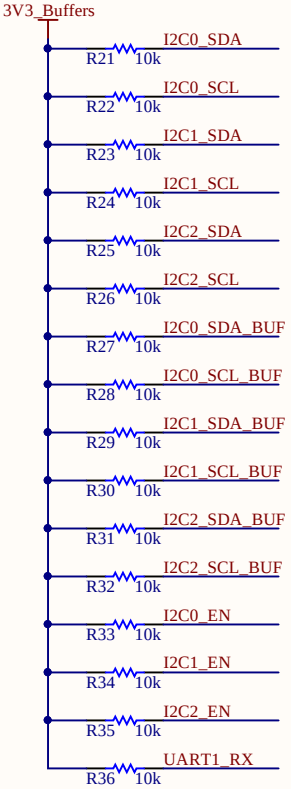


DECOUPLING CAPACITORS



TERMINATION RESISTORS

PULL-UP RESISTORS



Title	**Communication Buffers**		
Size: A4	Project: FloripaSat	Revision: V0.2	
Date: 11/01/2020	Time: 00:18:12	Sheet 6 of 6	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

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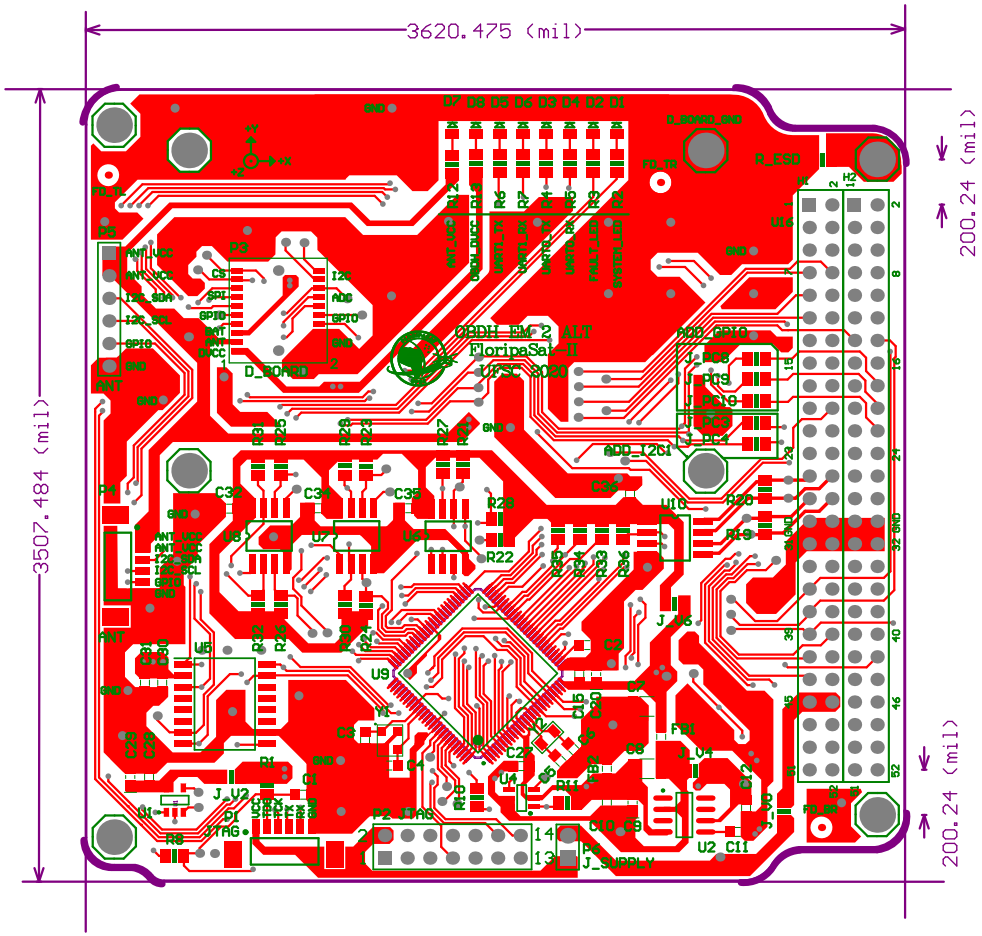
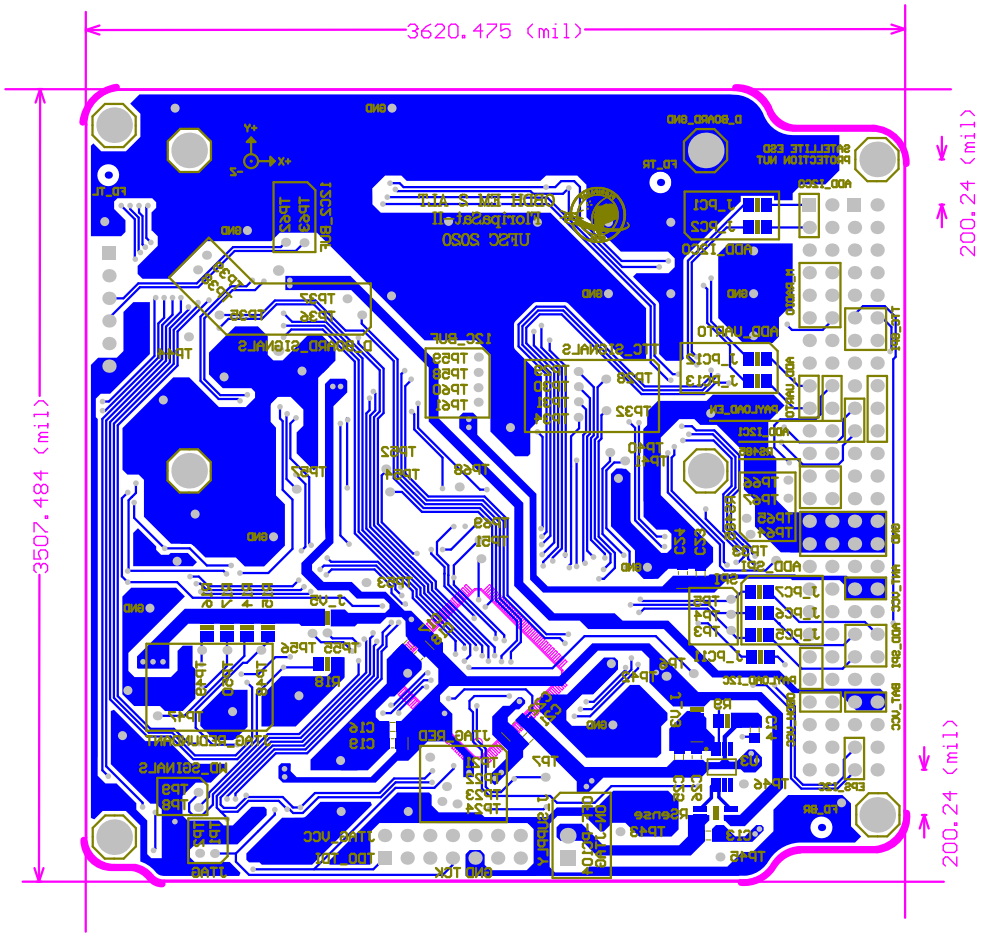


General SPEC:

Cupper base 1OZ:
PCB Material: FR4
PCB Tickness: 1.6mm
PCB Surface: ENIG
Vias: Force Complete Tenting

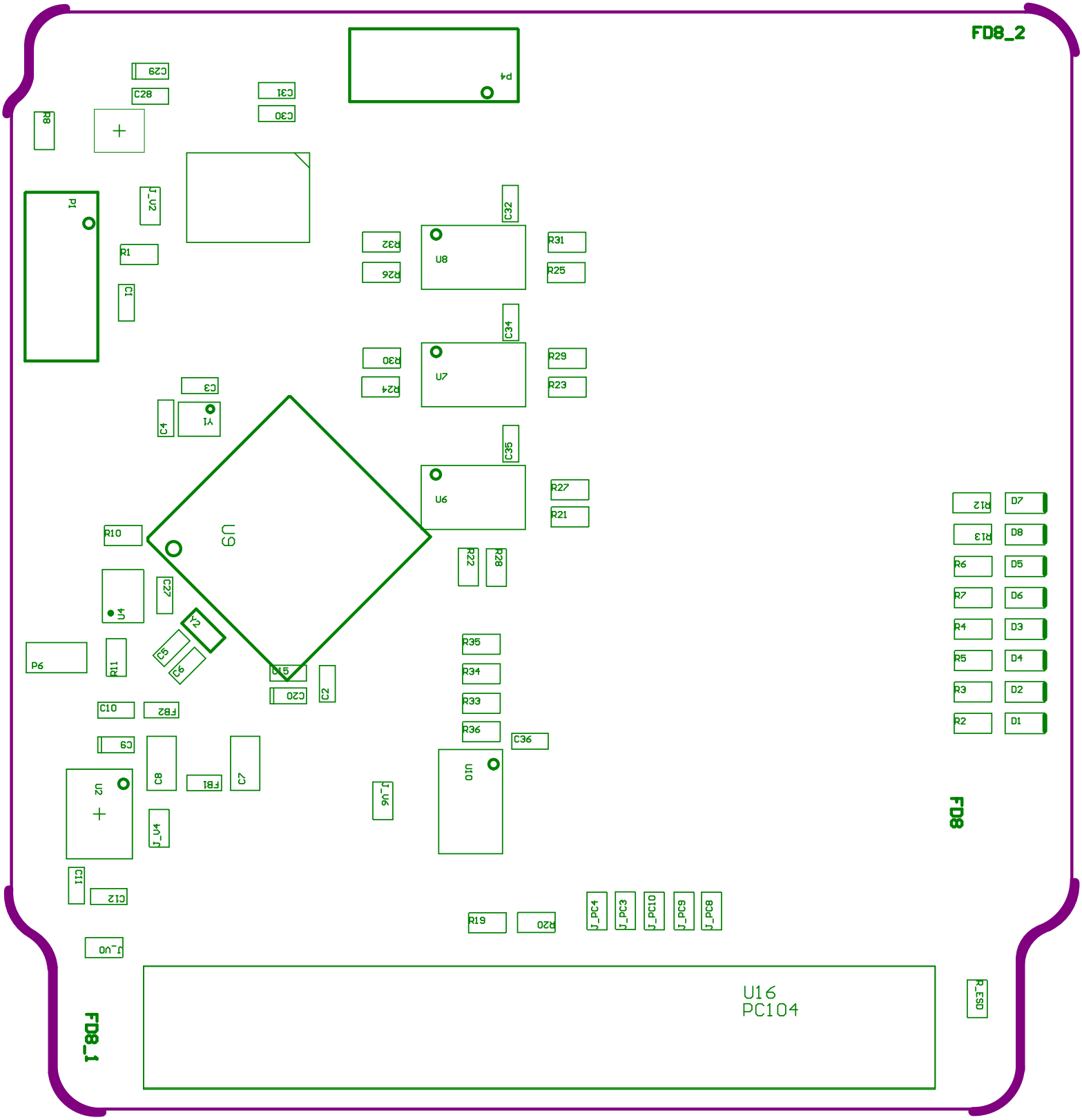
TITULO: OBDH 2018 UFSC		**REV.** 01	**VER.** Eng_2_ALT
MATERIAL: FR4	**Silkscreen color: green**		
Board Tickness: 1.6mm	**Layers: 02**	**Drawing**	**DATE**
PCB Surface: ENIG		Andre M. P. Mattos	01/12/2019



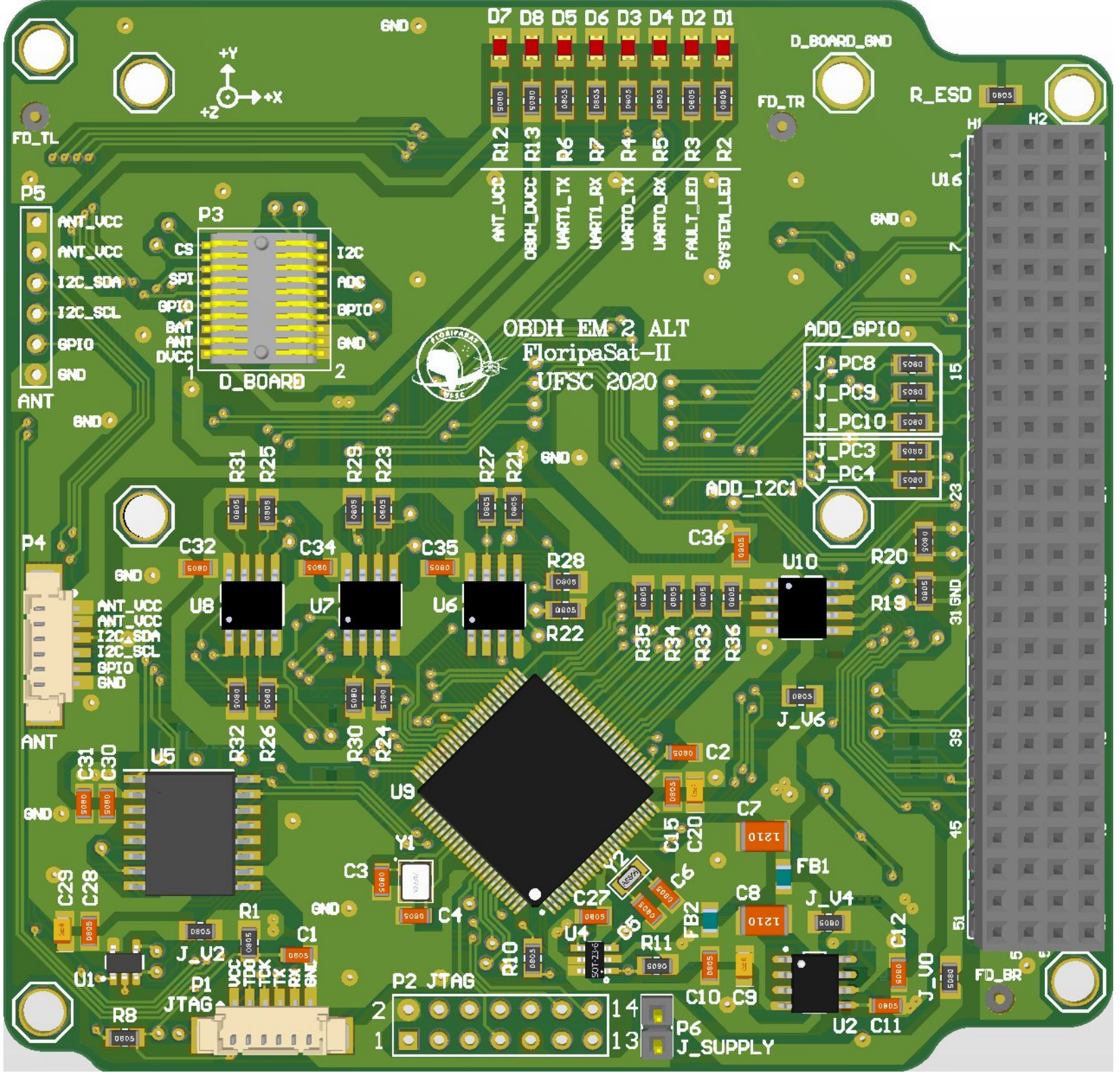
General SPEC:

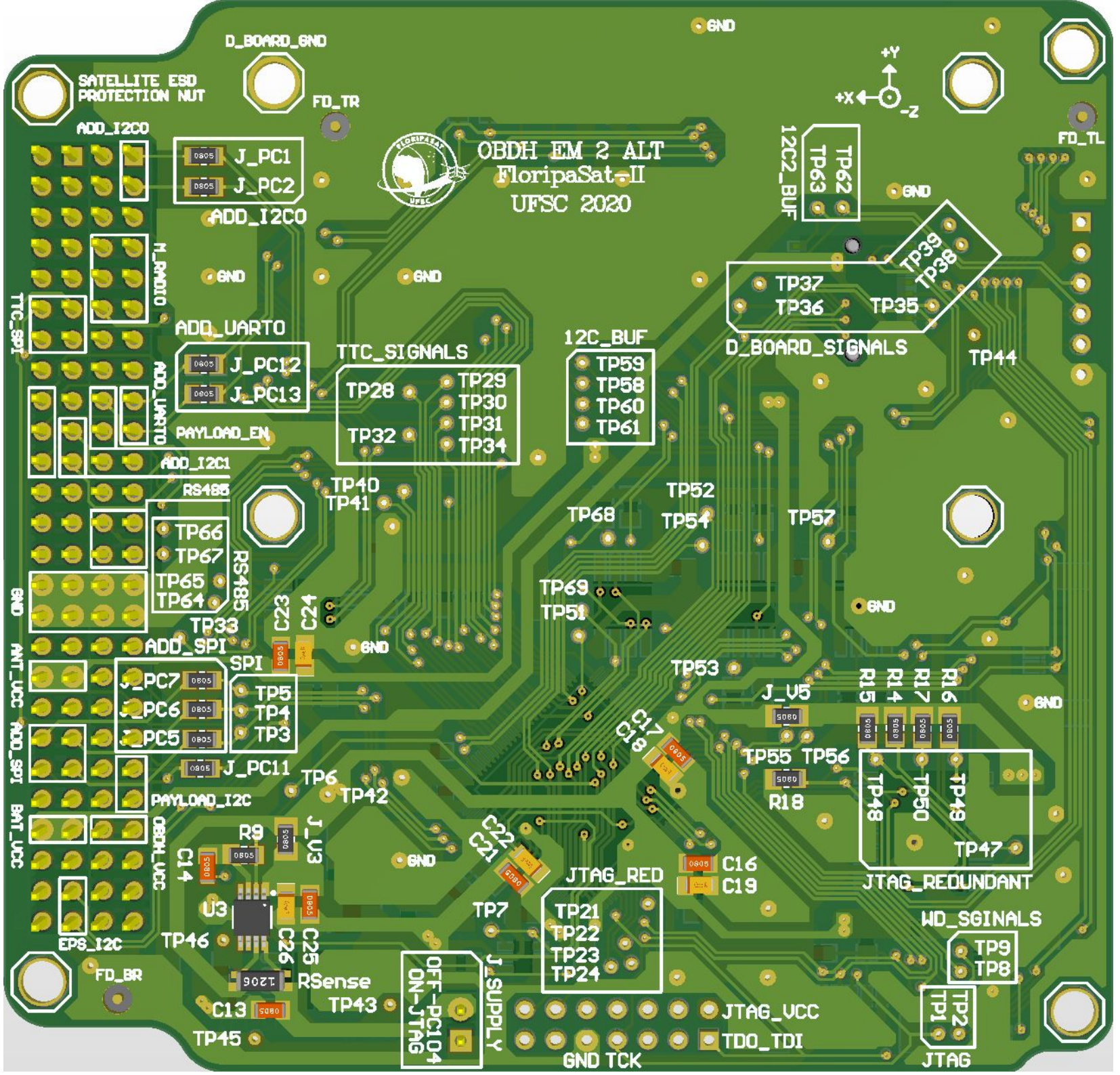
Cupper base 1OZ:
PCB Material: FR4
PCB Tickness: 1.6mm
PCB Surface: ENIG
Vias: Force Complete Tenting

TITULO: OBDH 2018 UFSC		**REV.** 01	**VER.** Eng_2_ALT
MATERIAL: FR4	**Silkscreen color: green**		
Board Tickness: 1.6mm	**Layers: 02**	**Drawing**	**DATE**
PCB Surface: ENIG		Andre M. P. Mattos	01/12/2019


FD8_2
P4
C29
C28
C31
C30
R8
P1
J_U2
R1
C1
C32
R32
R26
U8
R31
R25
C34
R30
R24
U7
R29
R23
C35
U6
R27
R21
C3
C4
Y1
U9
R10
R22
R28
U4
C22
Y2
C5
C6
P6
R11
R35
R34
R33
R36
C36
C15
C20
C2
C10
FB2
C9
C8
FB1
C7
U2
U10
J_U6
J_U4
C11
C12
J_U0
R19
R20
J_PC4
J_PC3
J_PC10
J_PC9
J_PC8
D7
D8
D5
D6
D3
D4
D2
D1
R12
R13
R6
R7
R4
R5
R3
R2
FD8
U16
PC104
R_ESD
FD8_1

FDB
FDB_2
FDB_1
J_PC1
J_PC2
J_PC12
J_PC13
J_PC7
J_PC6
J_PC5
J_PC11
C33
C34
C35
C32
U3
C14
L_VU3
R8
C13
R18
L_VU2
R15
R14
R16
C18
C17
C19
C16
C27
C22
U5


OBDH EM 2 ALT
FloripaSat-II
UFSC 2020
D_BOARD
ANT
P1 JTAG
P2 JTAG
P3
P4
P5
P6 J_SUPPLY
ADD_GPIO
ADD_I2C1
D_BOARD_GND
FD_TL
FD_TR
FD_BR
R_ESD
GND
ANT_VCC
I2C_SDA
I2C_SCL
GPIO
CS
SPI
I2C
ADC
BAT
ANT
DVCC
U1
U2
U4
U5
U6
U7
U8
U9
U10
U16
Y1
Y2
J_V0
J_V2
J_V4
J_V6
J_PC8
J_PC9
J_PC10
J_PC3
J_PC4
D7
D8
D5
D6
D3
D4
D2
D1
OBDH_DVCC
UART1_TX
UART1_RX
UART0_TX
UART0_RX
FAULT_LED
SYSTEN_LED


SATELLITE ESD PROTECTION NUT
D_BOARD_GND
FD_TR
GND
+Y
+X
-Z
FD_TL
OBDH EM 2 ALT
FloripaSat-II
UFSC 2020
ADD_I2C0
J_PC1
J_PC2
ADD_I2C0
I2C2_BUF
TP62
TP63
GND
GND
GND
TP39
TP38
TP37
TP36
TP35
D_BOARD_SIGNALS
TP44
TTC_SPI
N_RADIO
ADD_UART0
J_PC12
J_PC13
TTC_SIGNALS
TP28
TP29
TP30
TP31
TP32
TP34
I2C_BUF
TP59
TP58
TP60
TP61
PAYLOAD_EN
ADD_I2C1
RS485
TP40
TP41
TP68
TP52
TP54
TP57
TP66
TP67
TP65
TP64
RS485
TP33
C23
C24
TP69
TP51
GND
GND
ADD_SPI
SPI
TP53
GND
ANT_VCC
ADD_SPI
BAT_VCC
J_PC7
J_PC6
J_PC5
TP5
TP4
TP3
J_V5
R15
R14
R17
R16
C17
C18
TP55
TP56
R18
J_PC11
TP6
TP42
PAYLOAD_I2C
OBDH_VCC
R9
J_U3
C14
C22
C21
GND
JTAG_RED
C16
C19
TP48
TP50
TP49
TP47
JTAG_REDUNDANT
TP7
TP21
TP22
TP23
TP24
WD_SGINALS
TP9
TP8
U3
TP46
C26
C25
EPS_I2C
FD_BR
RSense
C13
TP43
OFF-PC104
ON-JTAG
J_SUPPLY
JTAG_VCC
TDO_TDI
GND TCK
TP2
TP1
JTAG
TP45

Bill of Materials

OBDH Interface

Source Data From: OBDH_Eng_Model_2_ALT.PrjPcb
Project: OBDH_Eng_Model_2_ALT.PrjPcb
Variant: None

Creation Date: 11/01/2020 00:18:20
Print Date: 11-Jan-20 12:18:29 AM

Footprint	Comment	LibRef	Designator	Description	Quantity
CC0805	1nF/16V	Cap_Cer_X7R_1nF_16V_0603	C1	CAP CER 1nF 16V 0603 5%	1
CC0805	0.47uF/50V	Cap_Cer_X7R_0.47uF_50V_0805	C2	CAP CER 0.47UF 50V 10% X7R 0805	1
CC0805	10pF/100V	Cap_Cer_X7R_10pF_100V_0805	C3, C4	CAP CER 10pF 100V 0805	2
CC0805	12pF/50V	Cap_Cer_X7R_12pF_50V_0805	C5, C6	CAP CER 12pF 50V 0805	2
CC1210	22uF/16V	Cap_Cer_X7R_0.01uF_16V_1210	C7, C8	CAP CER 22uF 16V 10% X7R 1210	2
CC0805_Tantalum	10uF/10V	Cap_Tant_SMD_10uF_6V3_0805, Cap_Tant_SMD_10uF_10V_0805	C9, C18, C19, C20, C22, C24, C26, C29	CAP Tantalum 10uF 6.3V 10% 0805, CAP Tantalum 10uF 10V 20% 0805	8
CC0805	0.1uF/25V	Cap_Cer_X7R_0.1uF_25V_0805	C10, C12, C13, C14, C15, C16, C17, C21, C23, C25, C27, C28, C36	CAP CER 0.1UF 25V 10% X7R 0805	13
CC0805	0.01uF/25V	Cap_Cer_X7R_0.01uF_50V_0805	C11, C32, C34, C35	CAP CER 0.01uF 25V 10% X7R 0805	4
CC0805	100nF/50V	Cap_Cer_X7R_100nF_50V_0603	C30	CAP CER 100nF 50V 0603 10%	1
CC0805	4.7uF/25V	Cap_Cer_X7R_4.7uF_25V_0805	C31	CAP CER 4.7UF 25V 10% X7R 0805	1
0805-LED	Orange	LED/R_0603	D1, D2, D3, D4, D5, D6	SMD Orange LED	6
0805-LED	DNP	LED/G_0805	D7, D8	SMD Green LED	2
IND0805	30R@100Mhz, 3A	FB_30R_3A_100MHz_0805	FB1, FB2	Ferrite Bead 30 OHM 3A 100MHz	2
0805	0R	R0R_JUMPER_1/16W_0805	J_PC1, J_PC2, J_PC3, J_PC4, J_PC5, J_PC6, J_PC7, J_PC8, J_PC9, J_PC10, J_PC11, J_PC12, J_PC13, J_V0, J_V2, J_V3, J_V4, J_V5, J_V6	RES 0R OHM 1/16W JUMPER 0805	19
HDR6 PicoBlade	6H_PicoBlade	Header 6H_PicoBlade	P1, P4	Header, 6-Pin, Right Angle	2
HDR2X7	Header 7x2	Header 7X2	P2	Header, 7-Pin, Dual row	1
FSI-110-03-X-D-AD	FSI-110-03-X-D-AD	FSI-110-03-X-D-AD	P3		1
HDR1X6H	Header 6H	Header 6H	P5	Header, 6-Pin, Right Angle	1
HDR 1X2	Header 2H	Header 2	P6	Header, 2-Pin	1
0805	47k	R27_5%_1/10W_0805	R1, R10, R11	RES 47k OHM 1/10W 1% 0805	3
0805	330R	R330R_1%_1/4W_0805	R2, R3, R4, R5, R6, R7	RES 330R OHM 1/4W 1% 0805	6
0805	10k	R10k_1%_1/8W_0805	R8, R14, R15, R16, R17, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36	RES 10K OHM 1/8W 1% 0805	21
0805	12K	R1.65K_1%_1/10W_0805	R9	RES 1.65K OHM 1/10W 0.1% 0805	1
0805	DNP	R1.0k_1%_1/8W_0805	R12, R13	RES 1.0K OHM 1/8W 1% 0805	2
0805	100k	R100k_1%_1/8W_0805	R18	RES 100K OHM 1/8W 1% 0805	1
0805	120R	R120R_1%_1/4W_0805	R19, R20	RES 120R OHM 1/8W 1% 0805	2
0805	1M	R1000k_1%_1/8W_0805	R_ESD	RES 1000K OHM 1/8W 1% 0805	1
1206 - ohmite	0.05R/0.5W	R0.05R_0.5%_0.5W_1206	RSense	Current Sense Resistors - SMD 0.05ohm .5% 4 Terminal	1
DBV0005A_N	TPS3823-33QDBVRQ1	CMP-0338-00011-2	U1	Processor Supervisory Circuit, 1 Supply Monitored, -40 to 85 degC, 5-Pin SOT-23 (DBV), Green (RoHS & no Sb/Br)	1
SOIC-8	REF5030A-Q1	REF5030A-Q1	U2	REF5030A-Q1	1
MSOP-8	MAX9934TAUA+	MAX9934TAUA+	U3	MAX9934TAUA+	1
SOT-23 6L	TLV341AIDBVR	TLV341AIDBVR	U4	TLV341AIDBVR	1
SOIC127P1032X265-16N	MT25QL01GBB8ESF-0SIT	MT25QL01GBB8ESF-0SIT	U5	IC FLASH 1GBIT 108MHZ 16SOIC	1
SOIC8	TCA4311ADR	TCA4311ADR	U6, U7, U8	IC SIGNAL BUFFER I2C 8SOIC	3
PZ0100A_N	MSP430F6659IPZR_1	MSP430F6659IPZR_1	U9	Imported	1
SOIC8	THVD1451DR	THVD1451DR	U10	IC INTERFACE RS422_RS485 8SOIC	1
PC104	PC104_INTERNAL	PC104	U16	PC104	1
XTAL_ABM8X	32MHz 10ppm	XTAL_32MHz_SMD_4-SMD	Y1	32MHz ±10ppm Crystal 10pF 60 Ohm -40°C ~ 125°C	1
ABS06 0805	32.768kHz 12.5pF	Xtal_32.768kHz_12pF_2_SMD	Y2	32.768kHz ±20ppm Crystal 12.5pF 70 kOhm -40°C ~ 125°C	1
					121

Approved	Notes	