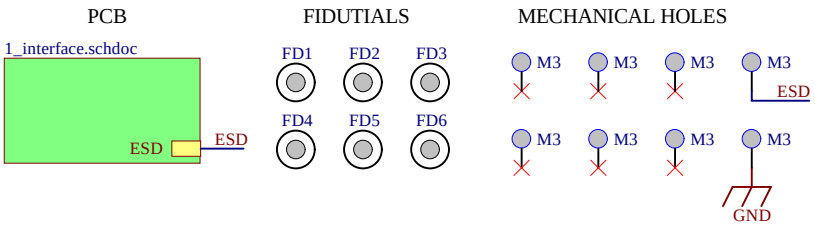
Rev	Description	Date	Author
0.5	- Update templates. - Add missing schematic to layout elements. - Update PC-104 interface. - Review circuits and architecture.	26-Aug-2020	Andre M. P. Mattos

Revision History

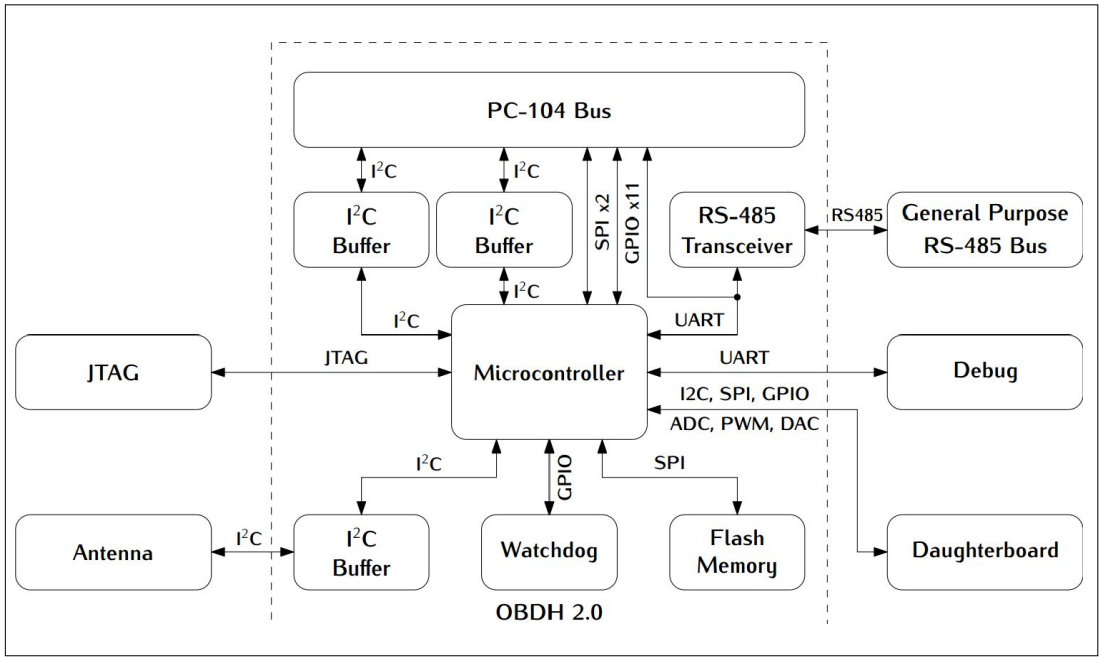


PCB Elements

OBDH2 Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Cezar A. Rigo, Kleber Gouveia and Yan C. Azeredo
- Based on FloripaSat-I OBDH designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Project Contributions



Block Diagram

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OBDH2 Hardware
Based on the FloripaSat-I OBDH 2.0

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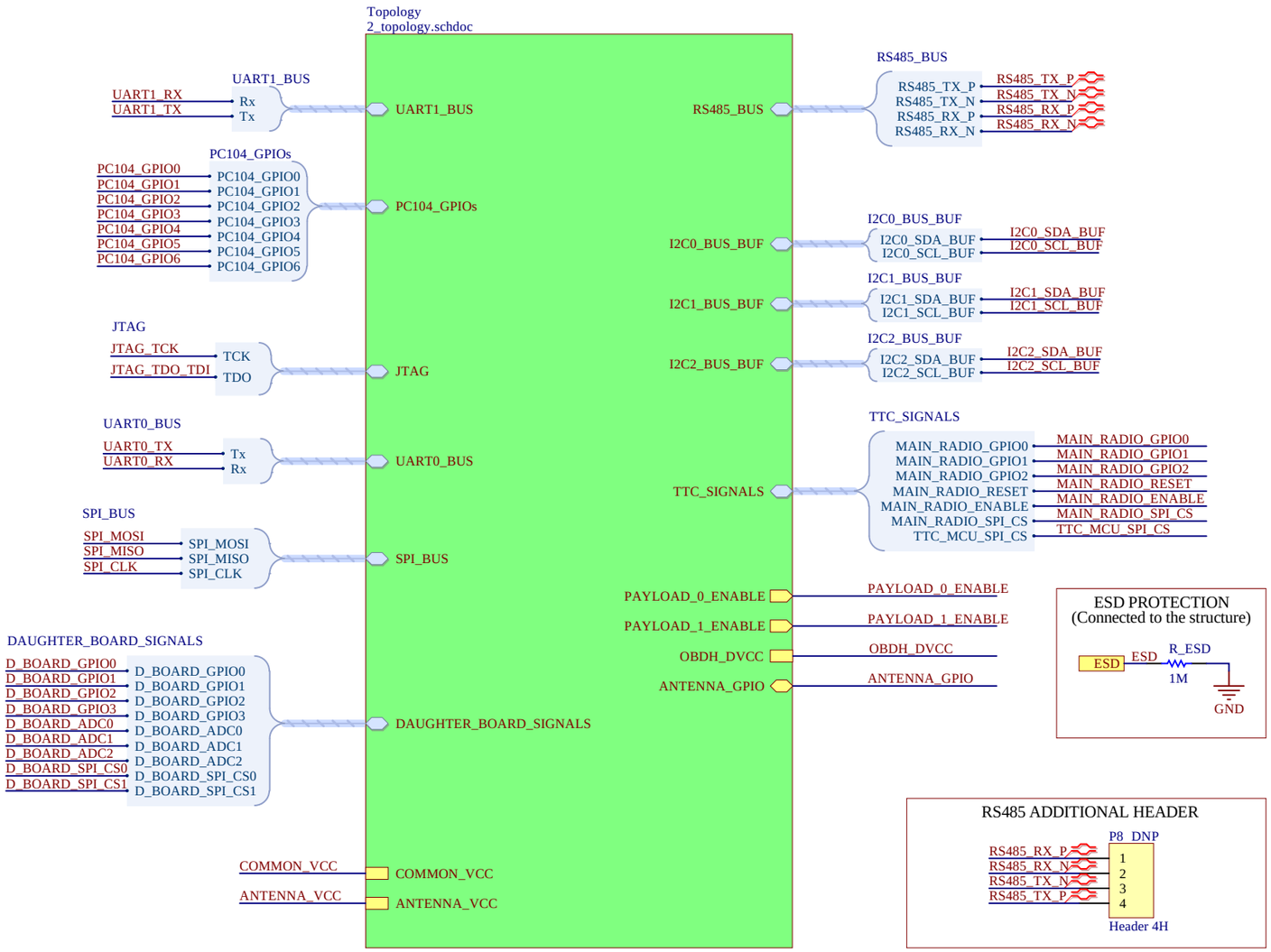
Project Information

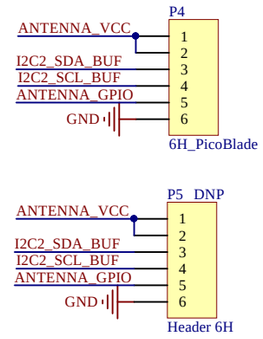
SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *OBDH Hardware Archictecture*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *0* of *6*	Size: A4



ESD PROTECTION (Connected to the structure)

RS485 ADDITIONAL HEADER

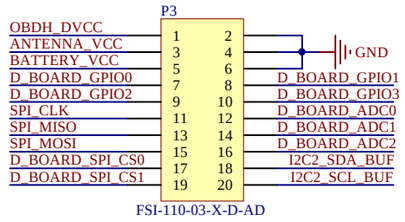
ANTENNA DEPLOYER INTERFACE



External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

DAUGHTER BOARD INTERFACE (Generic Interface)

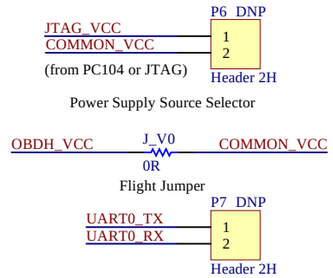


External Communication Buses Description:

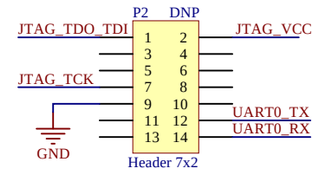
BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

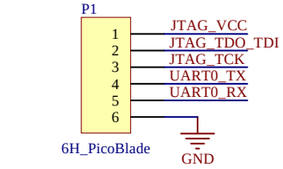
DEBUG HEADERS



PROGRAMMING HEADERS (JTAG Spy Bi-Wire)



Debug JTAG Main MCU



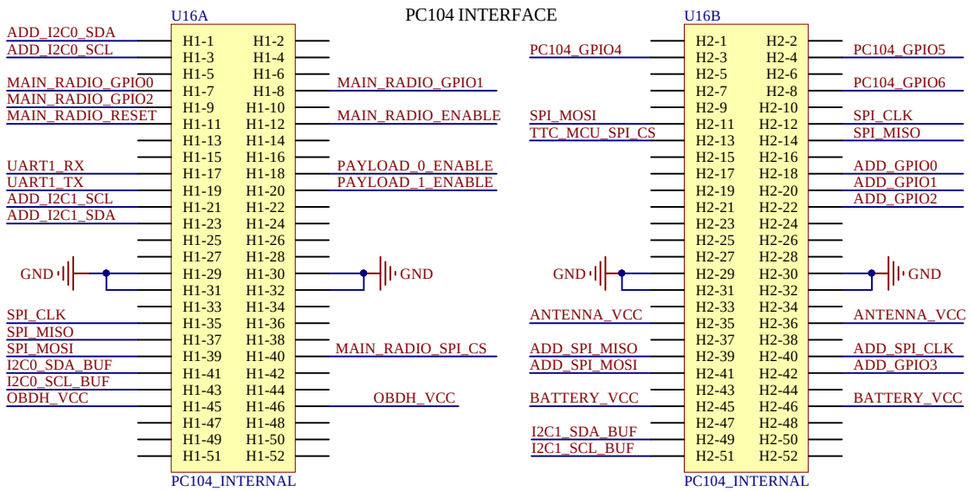
Flight Model JTAG Main MCU

External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

PC104 INTERFACE



External Communication Buses Description:

BUS1 (RS485): Payload EDC interface
Dedicated channel - UART1 (at additional header)
PAYLOAD_0_ENABLE - Logical enable of the Payload EDC

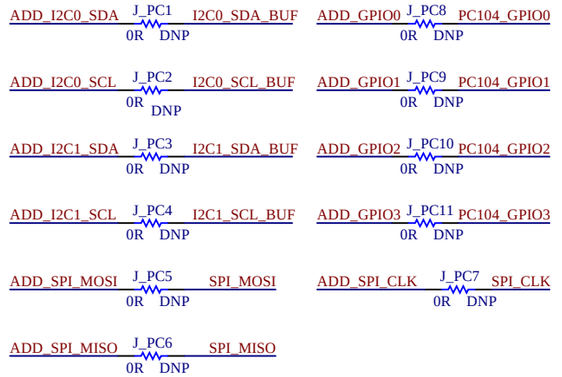
BUS2 (I2C): Payload X interface
Dedicated channel - I2C0
PAYLOAD_1_ENABLE - Logical enable of the Payload X

BUS3 (I2C): EPS interface
Dedicated channel - I2C1

BUS7 (SPI)(H2): TTC interface
Shared Channel - SPI
TTC_SPI_CS - TTC chip select

BUS8 (SPI)(H1): Main Radio interface
Shared Channel - SPI
MAIN_RADIO_SPI_CS - Main radio chip select
MAIN_RADIO_GPIOx - GPIO configuration pins
MAIN_RADIO_RESET - Main radio reset
MAIN_RADIO_ENABLE - Enable for the Main Radio regulator in EPS

ADDITIONAL PC104 INTERFACES



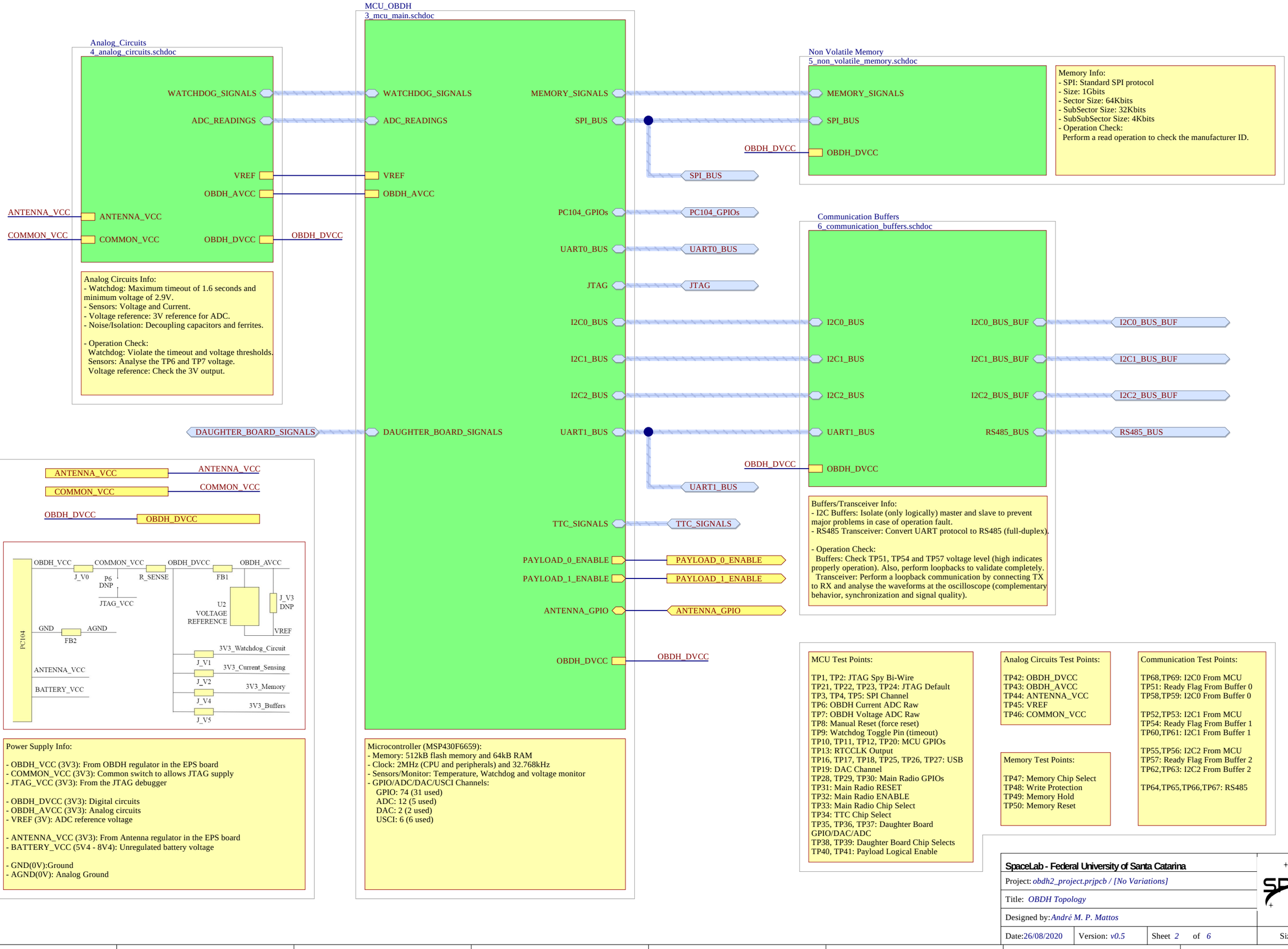
Additional Communication Buses Description:
(Used by demand, do not place unless necessary)

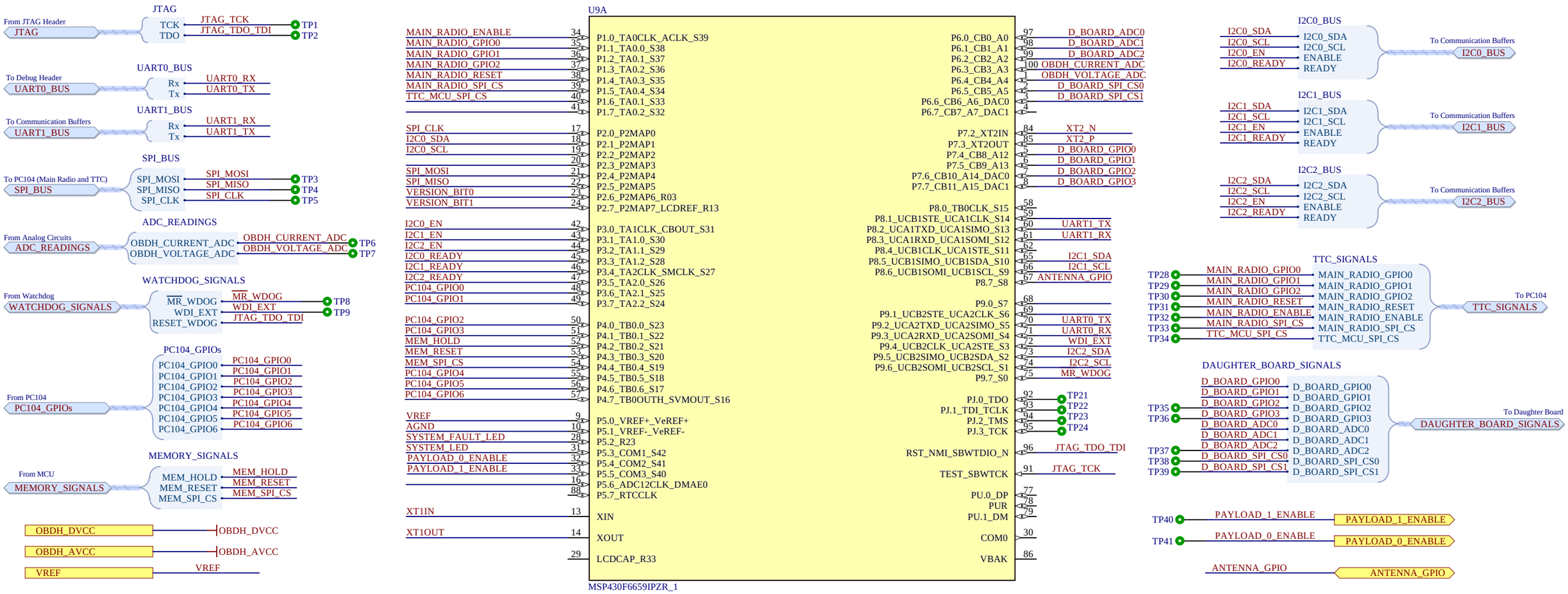
BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (GPIO): 4 GPIOs

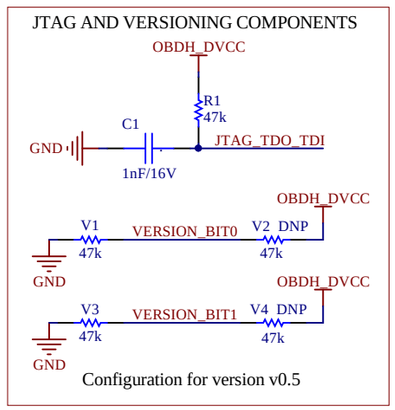
Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12

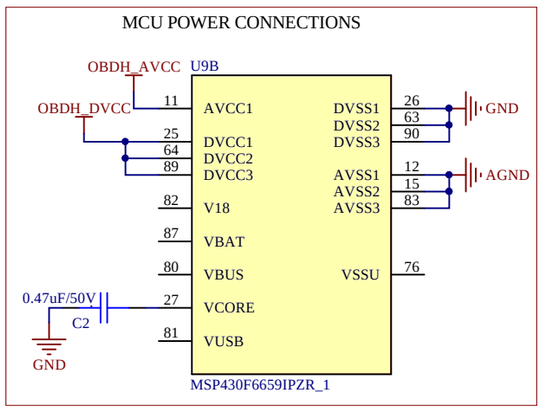
Allow PC104 flexibility and device sharing:
BUS13 - Dedicated use of PC104.

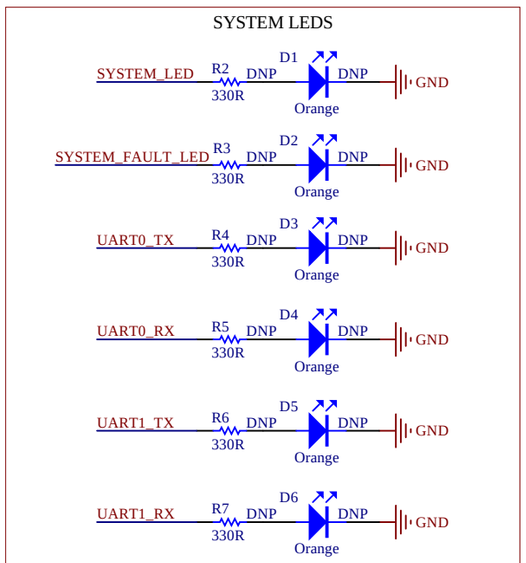
SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *OBDH Interface*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *1* of *6*	Size: A3

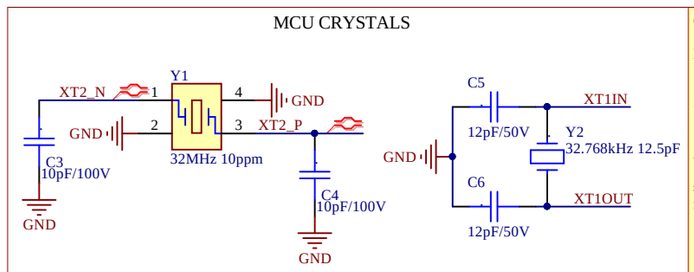

MCU_OBDH
3_mcu_main.schdoc
Analog_Circuits
4_analog_circuits.schdoc
WATCHDOG_SIGNALS
ADC_READINGS
VREF
OBDH_AVCC
ANTENNA_VCC
COMMON_VCC
OBDH_DVCC
Analog Circuits Info:
- Watchdog: Maximum timeout of 1.6 seconds and minimum voltage of 2.9V.
- Sensors: Voltage and Current.
- Voltage reference: 3V reference for ADC.
- Noise/Isolation: Decoupling capacitors and ferrites.
- Operation Check:
Watchdog: Violate the timeout and voltage thresholds.
Sensors: Analyse the TP6 and TP7 voltage.
Voltage reference: Check the 3V output.
Non Volatile Memory
5_non_volatile_memory.schdoc
MEMORY_SIGNALS
SPI_BUS
Memory Info:
- SPI: Standard SPI protocol
- Size: 1Gbits
- Sector Size: 64Kbits
- SubSector Size: 32Kbits
- SubSubSector Size: 4Kbits
- Operation Check:
Perform a read operation to check the manufacturer ID.
Communication Buffers
6_communication_buffers.schdoc
PC104_GPIOs
UART0_BUS
JTAG
I2C0_BUS
I2C1_BUS
I2C2_BUS
UART1_BUS
I2C0_BUS_BUF
I2C1_BUS_BUF
I2C2_BUS_BUF
RS485_BUS
Buffers/Transceiver Info:
- I2C Buffers: Isolate (only logically) master and slave to prevent major problems in case of operation fault.
- RS485 Transceiver: Convert UART protocol to RS485 (full-duplex).
- Operation Check:
Buffers: Check TP51, TP54 and TP57 voltage level (high indicates properly operation). Also, perform loopbacks to validate completely.
Transceiver: Perform a loopback communication by connecting TX to RX and analyse the waveforms at the oscilloscope (complementary behavior, synchronization and signal quality).
DAUGHTER_BOARD_SIGNALS
TTC_SIGNALS
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
ANTENNA_GPIO
Microcontroller (MSP430F6659):
- Memory: 512kB flash memory and 64kB RAM
- Clock: 2MHz (CPU and peripherals) and 32.768kHz
- Sensors/Monitor: Temperature, Watchdog and voltage monitor
- GPIO/ADC/DAC/USCI Channels:
GPIO: 74 (31 used)
ADC: 12 (5 used)
DAC: 2 (2 used)
USCI: 6 (6 used)
OBDH_VCC
COMMON_VCC
JTAG_VCC
OBDH_AVCC
J_V0
P6
DNP
R_SENSE
FB1
U2
VOLTAGE
REFERENCE
J_V3
DNP
VREF
PC104
GND
AGND
FB2
3V3_Watchdog_Circuit
J_V1
3V3_Current_Sensing
J_V2
3V3_Memory
J_V4
3V3_Buffers
J_V5
BATTERY_VCC
Power Supply Info:
- OBDH_VCC (3V3): From OBDH regulator in the EPS board
- COMMON_VCC (3V3): Common switch to allows JTAG supply
- JTAG_VCC (3V3): From the JTAG debugger
- OBDH_DVCC (3V3): Digital circuits
- OBDH_AVCC (3V3): Analog circuits
- VREF (3V): ADC reference voltage
- ANTENNA_VCC (3V3): From Antenna regulator in the EPS board
- BATTERY_VCC (5V4 - 8V4): Unregulated battery voltage
- GND(0V):Ground
- AGND(0V): Analog Ground
MCU Test Points:
TP1, TP2: JTAG Spy Bi-Wire
TP21, TP22, TP23, TP24: JTAG Default
TP3, TP4, TP5: SPI Channel
TP6: OBDH Current ADC Raw
TP7: OBDH Voltage ADC Raw
TP8: Manual Reset (force reset)
TP9: Watchdog Toggle Pin (timeout)
TP10, TP11, TP12, TP20: MCU GPIOs
TP13: RTCCLK Output
TP16, TP17, TP18, TP25, TP26, TP27: USB
TP19: DAC Channel
TP28, TP29, TP30: Main Radio GPIOs
TP31: Main Radio RESET
TP32: Main Radio ENABLE
TP33: Main Radio Chip Select
TP34: TTC Chip Select
TP35, TP36, TP37: Daughter Board GPIO/DAC/ADC
TP38, TP39: Daughter Board Chip Selects
TP40, TP41: Payload Logical Enable
Analog Circuits Test Points:
TP42: OBDH_DVCC
TP43: OBDH_AVCC
TP44: ANTENNA_VCC
TP45: VREF
TP46: COMMON_VCC
Memory Test Points:
TP47: Memory Chip Select
TP48: Write Protection
TP49: Memory Hold
TP50: Memory Reset
Communication Test Points:
TP68,TP69: I2C0 From MCU
TP51: Ready Flag From Buffer 0
TP58,TP59: I2C0 From Buffer 0
TP52,TP53: I2C1 From MCU
TP54: Ready Flag From Buffer 1
TP60,TP61: I2C1 From Buffer 1
TP55,TP56: I2C2 From MCU
TP57: Ready Flag From Buffer 2
TP62,TP63: I2C2 From Buffer 2
TP64,TP65,TP66,TP67: RS485
SpaceLab - Federal University of Santa Catarina
Project: obdh2_project.prjpcb / [No Variations]
Title: OBDH Topology
Designed by: André M. P. Mattos
Date: 26/08/2020
Version: v0.5
Sheet 2 of 6
Size: A3











Clock Configuration:

MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.

SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.

ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.

LEDs Assigment:

- SYSTEM LED (D1): (P5.3) Watchdog reset (blink each second)
- SYSTEM FAULT(D2): (P5.2) Active in case of hardware check routine failure
- UART DEBUG (D3, D4, D5, D6): UART TX and RX operation checks

Communication Assigment and Configuration:

- USCI_A0 - SPI: (Memory, Main Radio, TTC and Daughter board)
  Chip Selects:1 Memory, 1 Main radio, 1 TTC and 2 Daugther board
  Config: Length - 8bits, Phase - High, Polarity - Low, Endianness - MSB, Data Rate - 400kbps

- USCI_A1 - UART1: (Transceiver RS485)
  Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1

- USCI_A2 - UART0: (Debug)
  Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1

- USCI_B0 - I2C0: (Buffer I2C)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps

- USCI_B1 - I2C1: (Buffer I2C)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps

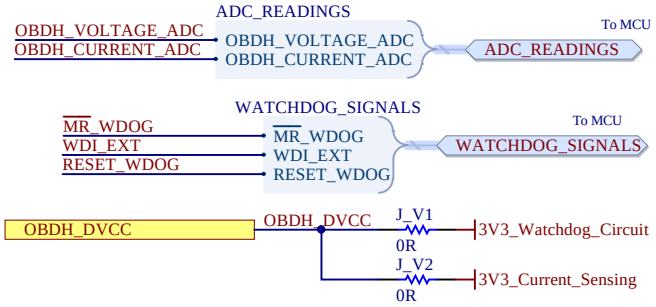
- USCI_B2 - I2C2: (Buffer I2C)(Antenna and Daughter Board)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps

All USCIs uses the SMCLK as clock source

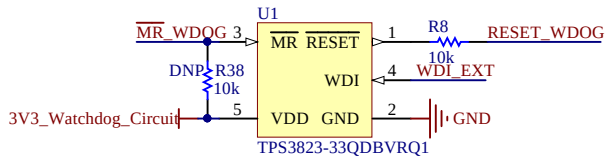
Daughter Board Interface:

- Power Supply:
  OBDH_DVCC (3V3), ANTENNA_VCC (3V3), BATTERY_VCC(5V4-8V4)
- Inputs/Outputs:
  GPIO0(GPIO/ADC), GPIO1(GPIO/ADC), GPIO2(GPIO/ADC/DAC), GPIO3(GPIO/ADC/DAC)
  ADC0(ADC/GPIO), ADC1(ADC/GPIO), ADC2(ADC/GPIO)
- Communication:
  SPI (2 chip selects avaliable) and I2C (shared with antenna)

SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *OBDH MCU Main*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *3* of *6*	Size: A3

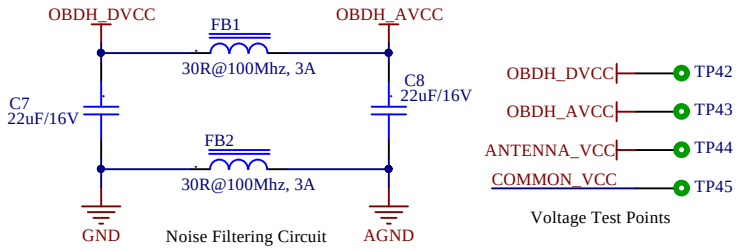


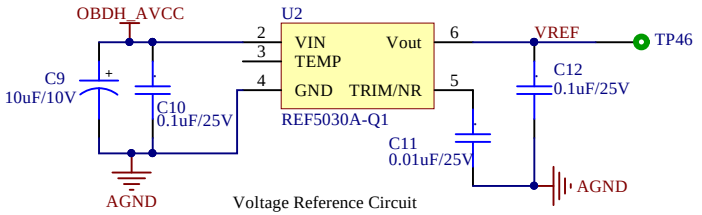
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER



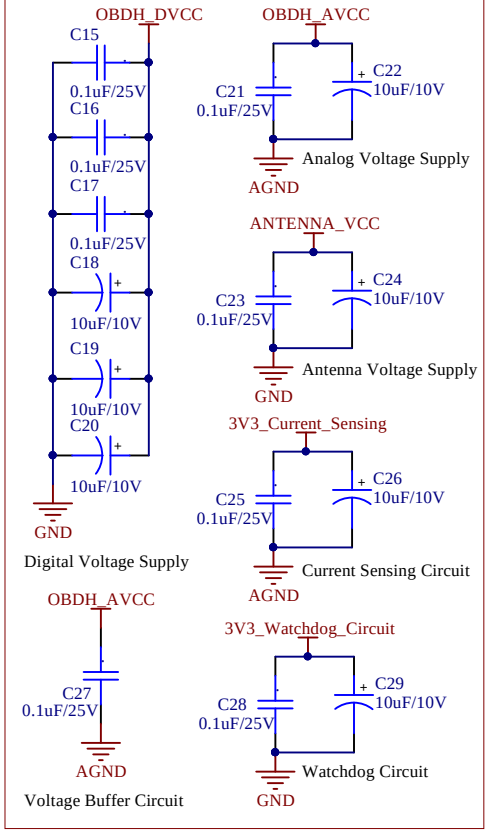
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

VOLTAGE REFERENCES



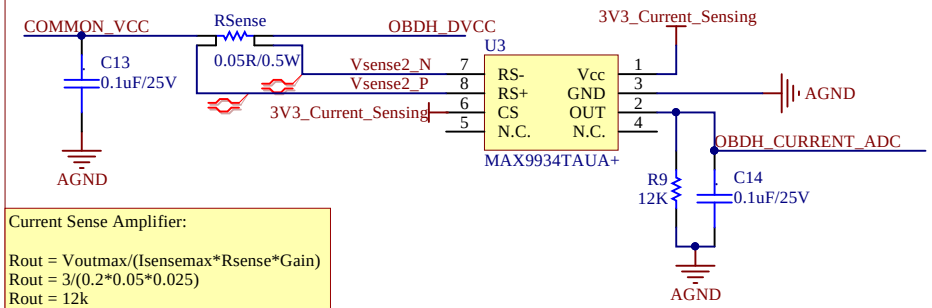


DECOUPLING CAPACITORS



INTERNAL MEASUREMENT CIRCUITS

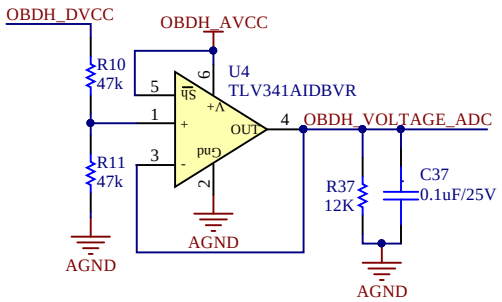
Current Sensing Circuit



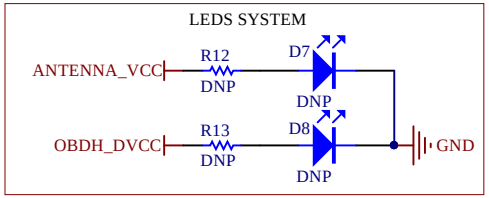
Current Sense Amplifier:

Rout = Voutmax/(Isensemax*Rsense*Gain)
Rout = 3/(0.2*0.05*0.025)
Rout = 12k

Voltage Buffer Circuit

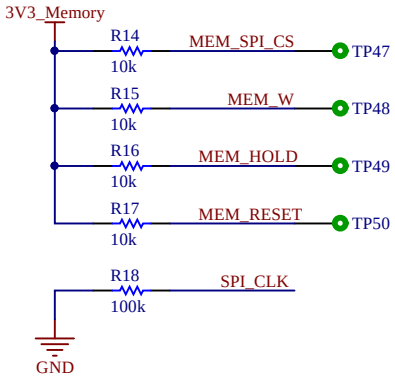


LEDS SYSTEM

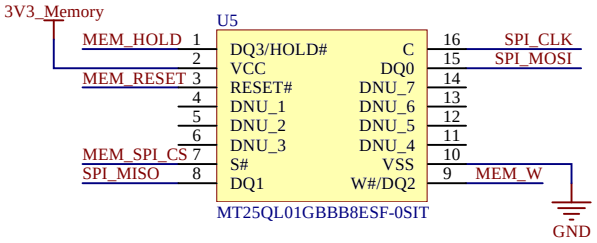


SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *Analog Circuits*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *4* of *6*	Size: A4

PULL-UP AND PULL-DOWN RESISTORS



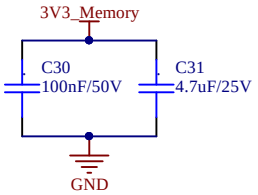
NON-VOLATILE MEMORY

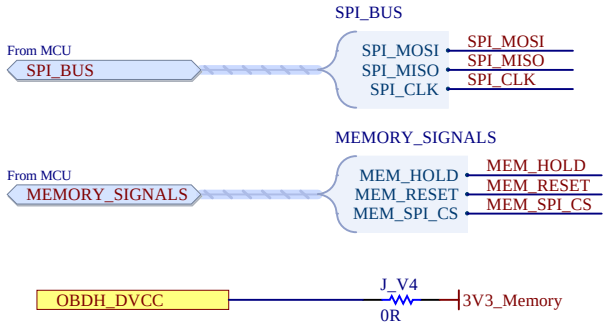


Memory Operation:

To be defined

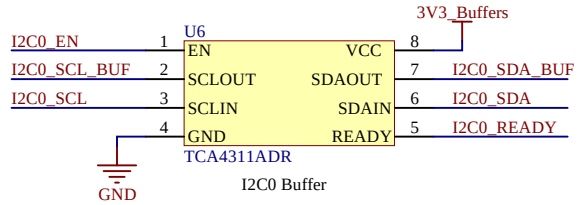
DECOUPLING CAPACITORS

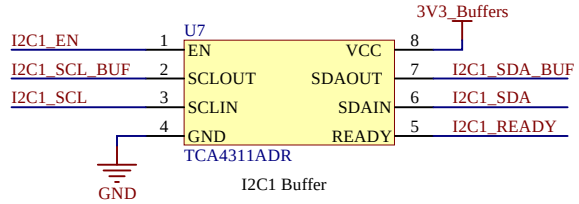


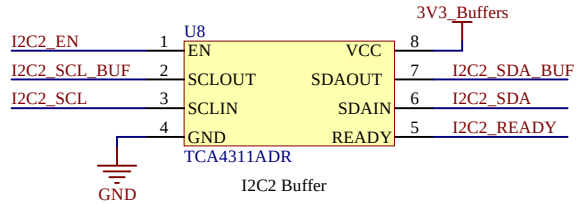


SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *Non Volatile Memory*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *5* of *6*	Size: A4

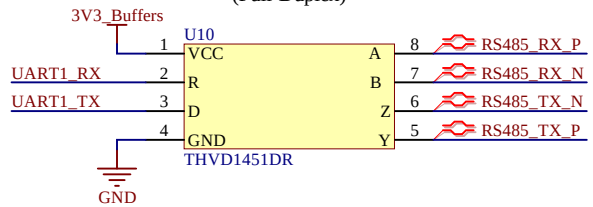
I2C BUFFERS

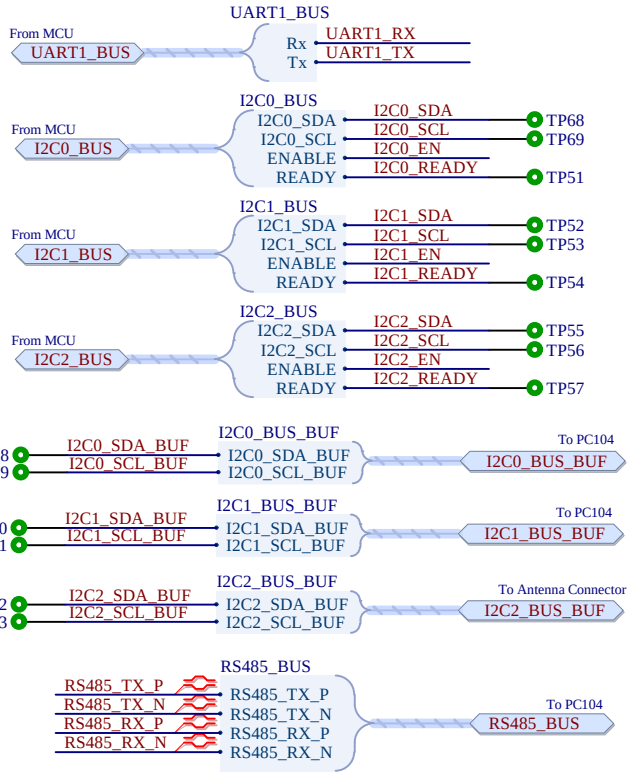




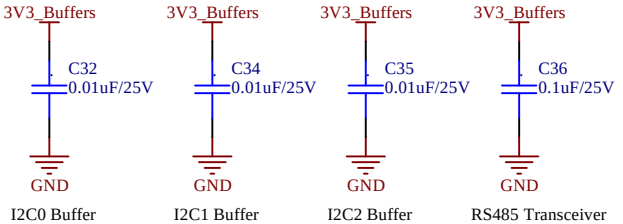


RS485 TRANSCEIVER (Full-Duplex)

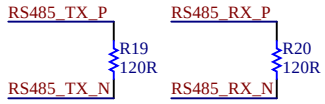




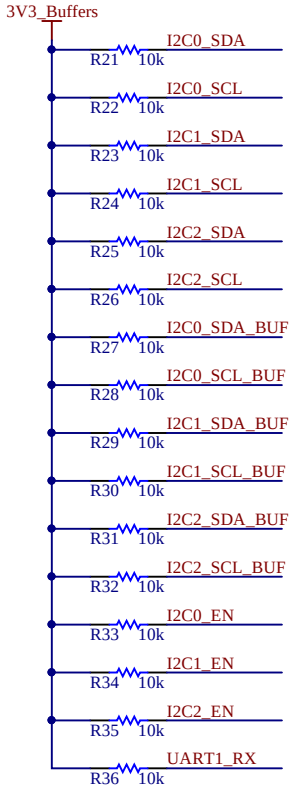
DECOUPLING CAPACITORS



TERMINATION RESISTORS



PULL-UP RESISTORS



SpaceLab - Federal University of Santa Catarina			
Project: *obdh2_project.prjpcb / [No Variations]*			
Title: *Communication Buffers*			
Designed by: *André M. P. Mattos*			
Date: 26/08/2020	Version: *v0.5*	Sheet *6* of *6*	Size: A4