

Title OBDH Hardware Architecture			UFSC - SpaceLab	
Size: A4			University Campus - Trindade	
Project: FloripaSat			Dep. of Electrical Engineering - CTC	
Revision: V0.1			Florianópolis, Santa Catarina, Brazil	
Date: 31/12/2019	Time: 13:00:24	Sheet 0 of 7	CEP: 88040 - 900	
Drawn By: André M. P. Mattos			Model: Eng 2 ALT	



A

B

C

D

A

B

C

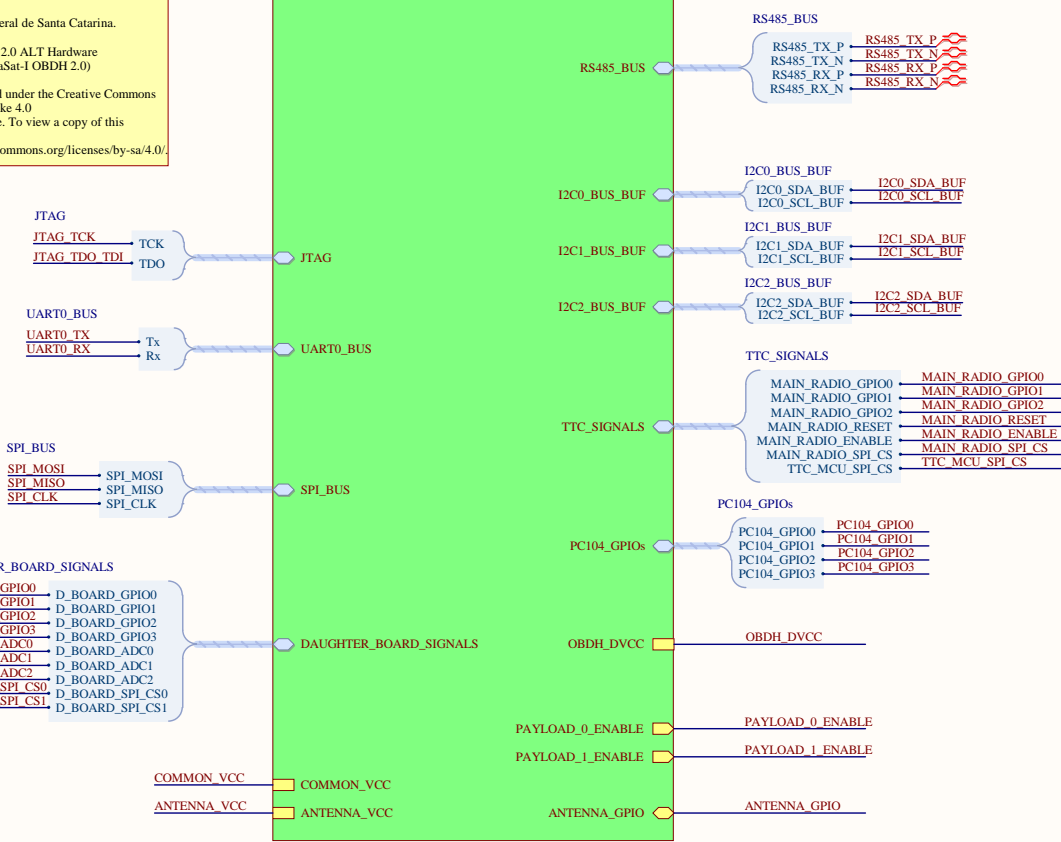
D

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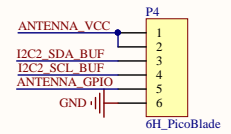
FloripaSat-II OBDH 2.0 ALT Hardware
(Based on the FloripaSat-I OBDH 2.0)

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Topology 2_Topology.SchDoc



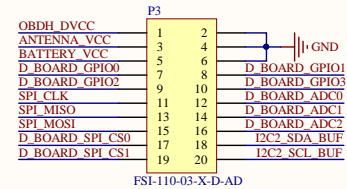
ANTENNA DEPLOYER INTERFACE



External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

DAUGHTER BOARD INTERFACE (Generic Interface)

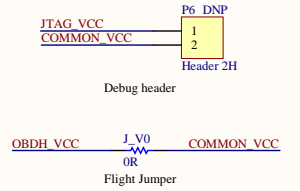


External Communication Buses Description:

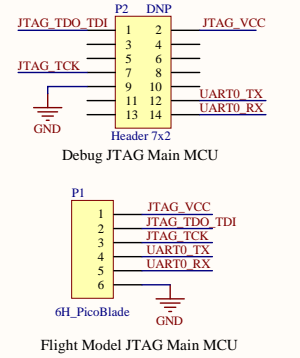
BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

POWER SUPPLY SOURCE SELECTOR (from PC104 or JTAG)



PROGRAMMING HEADERS (JTAG Spy Bi-Wire)

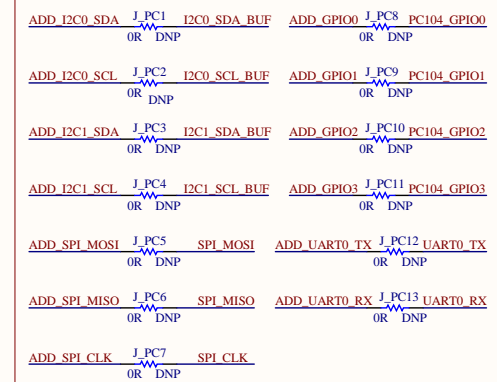


External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

ADDITIONAL PC104 INTERFACES



Additional Communication Buses Description: (Used by demand, do not place unless necessary)

BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (UART): UART0
BUS14 (GPIO): 4 GPIOs

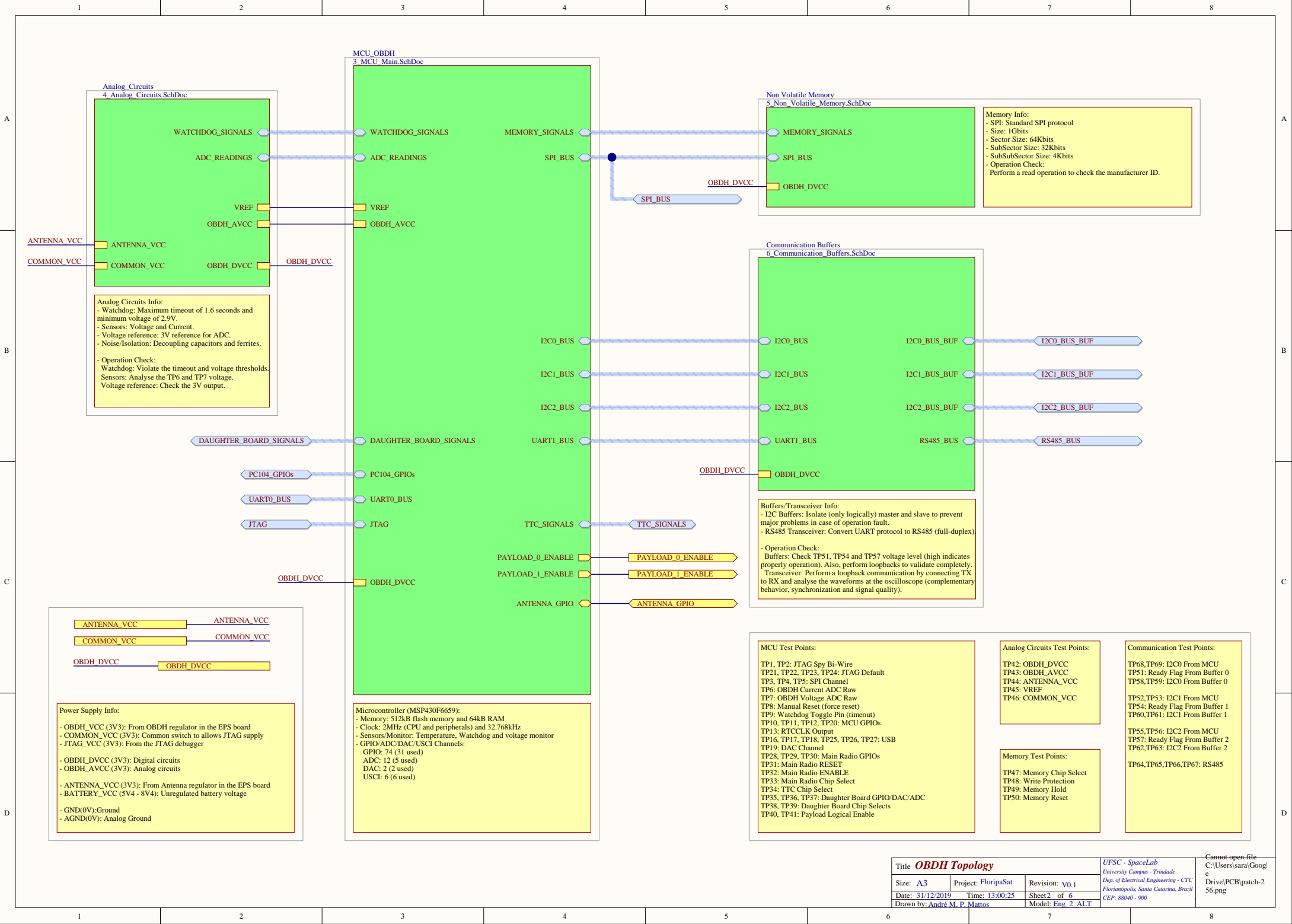
Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12
Allow PC104 flexibility and device sharing:
BUS13 - Require to deactivate debug routines.
BUS14 - Dedicated use of PC104.

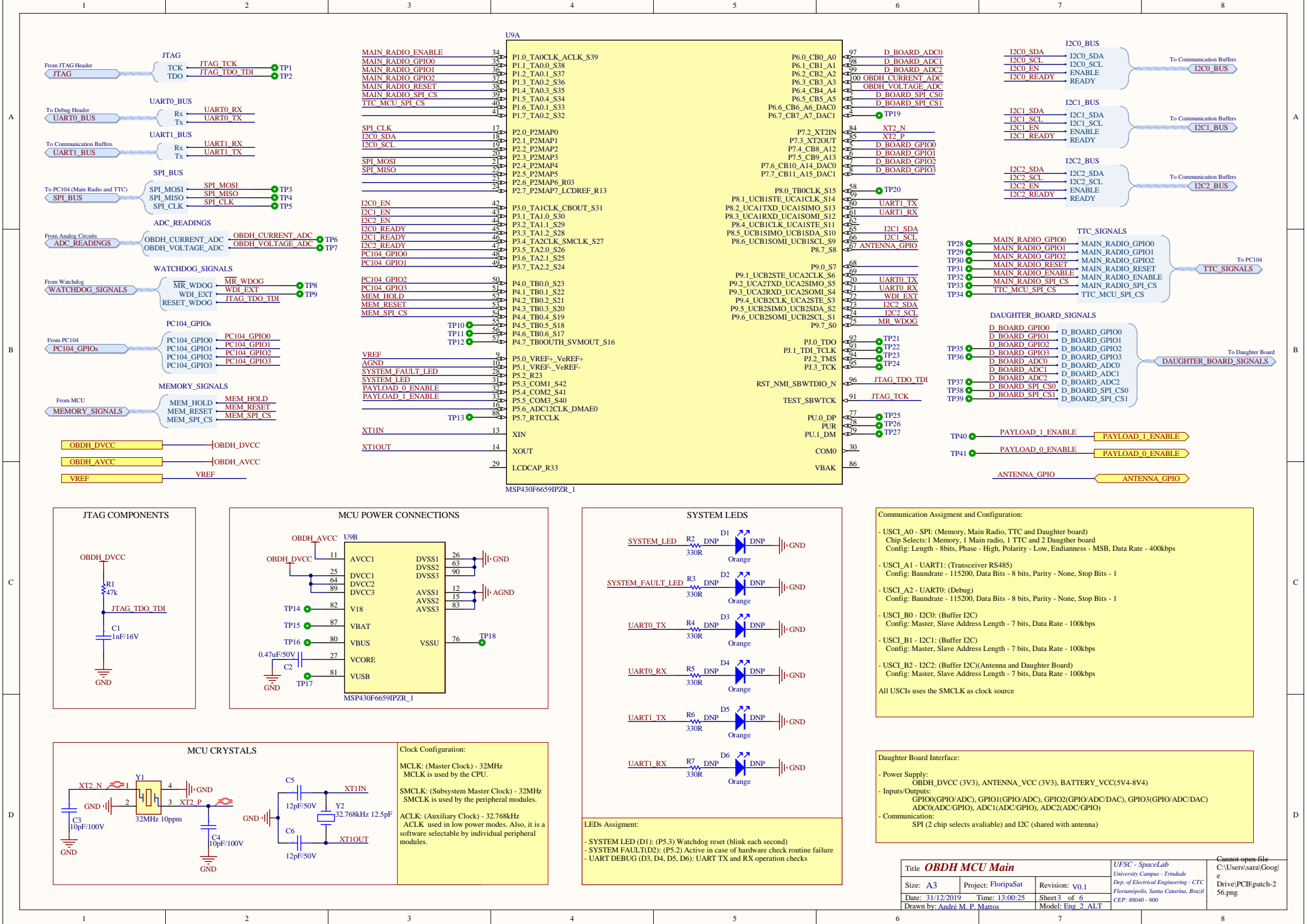
Title OBDH Interface

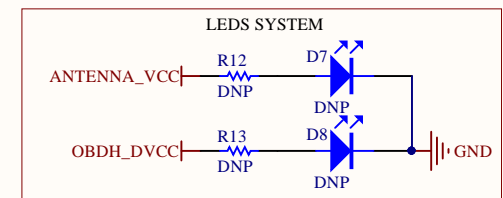
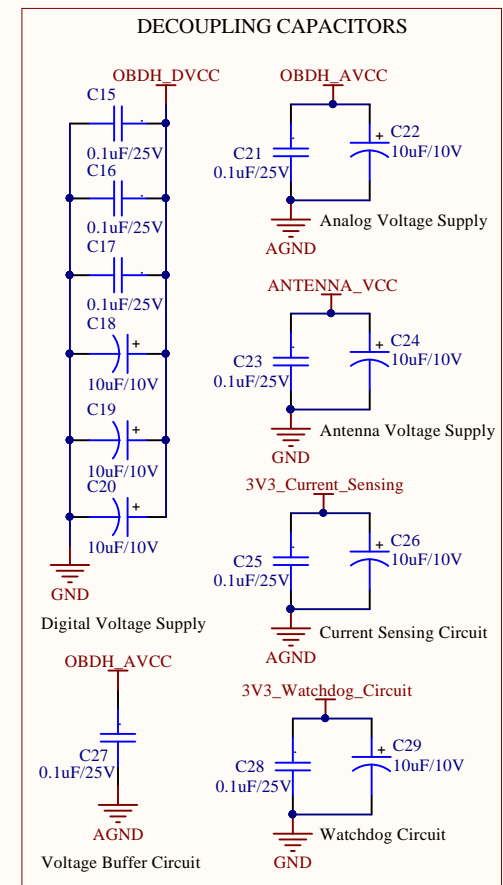
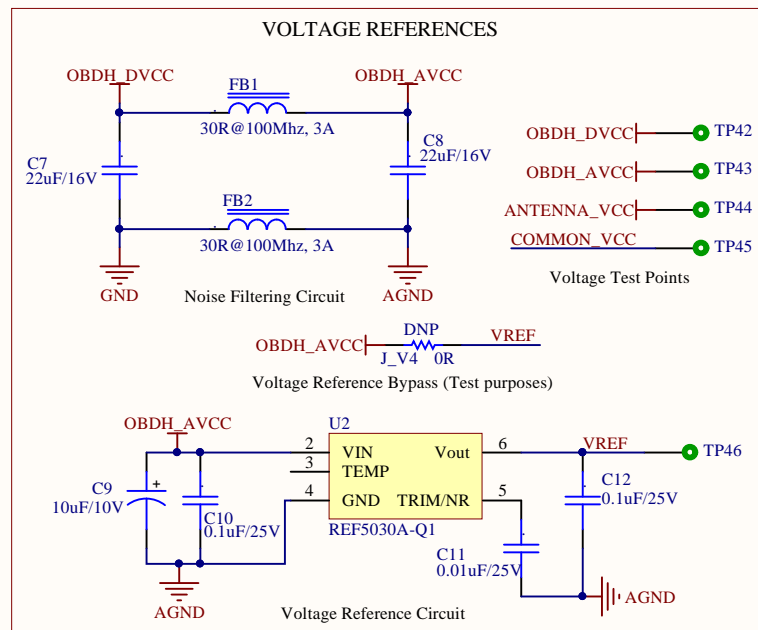
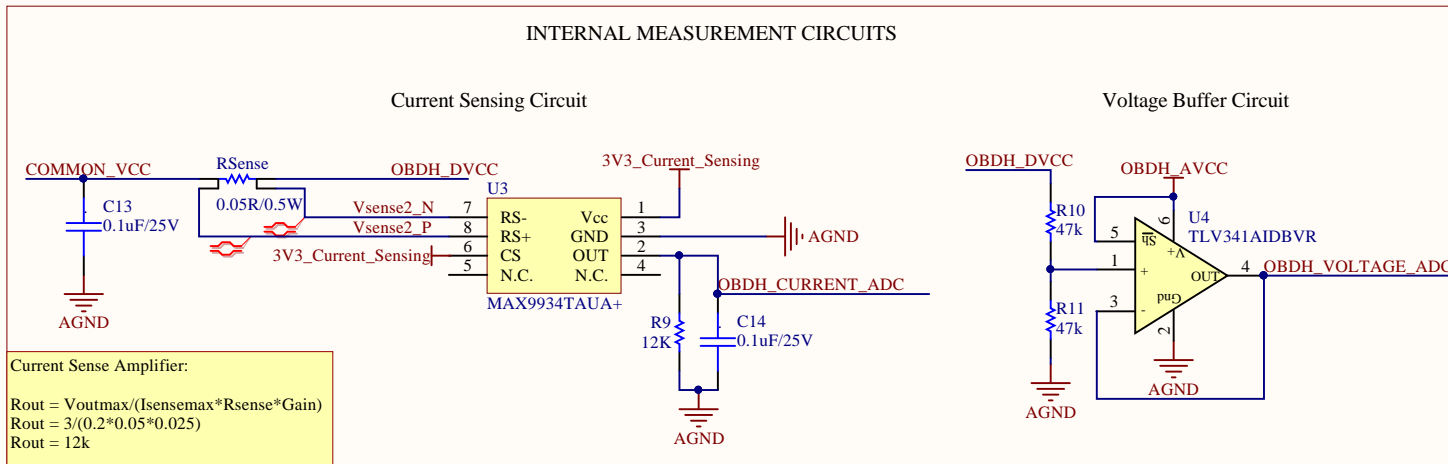
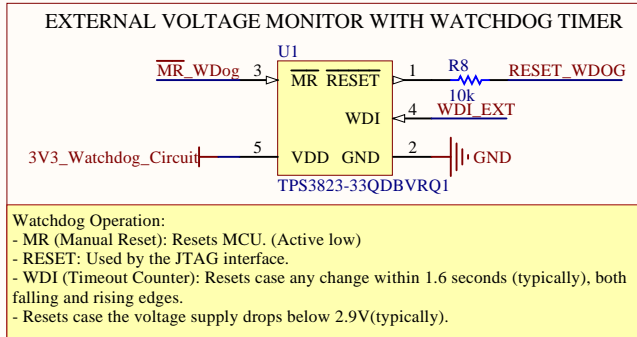
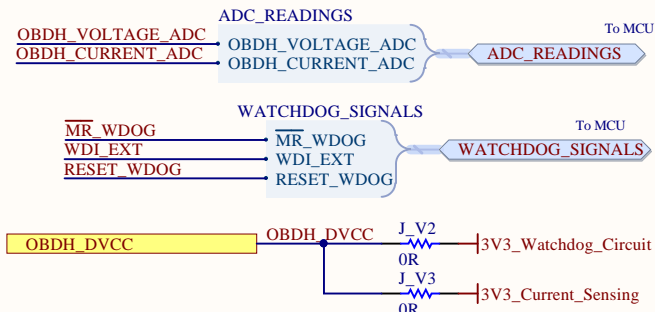
Size: A3
Project: FloripaSat
Date: 31/12/2019
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Sheet 1 of 6
Model: Eng 2_ALT

Cannot-open-file
C:\Users\sara\Google Drive\PCB\patch-2 56.png



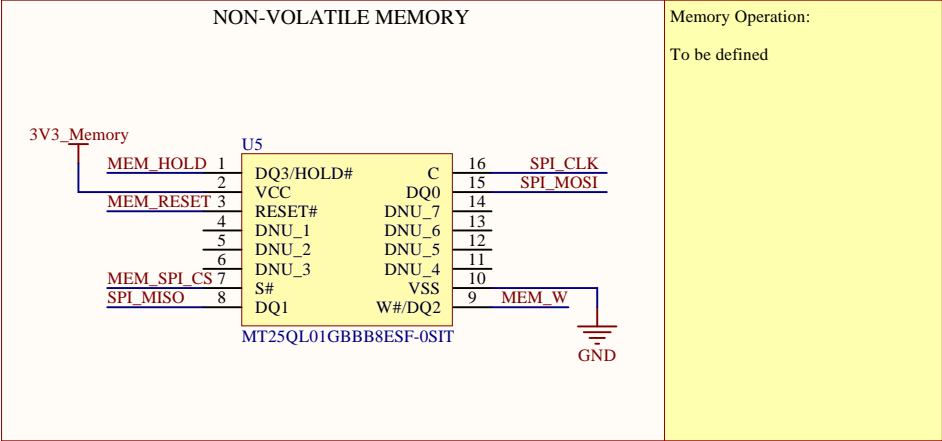
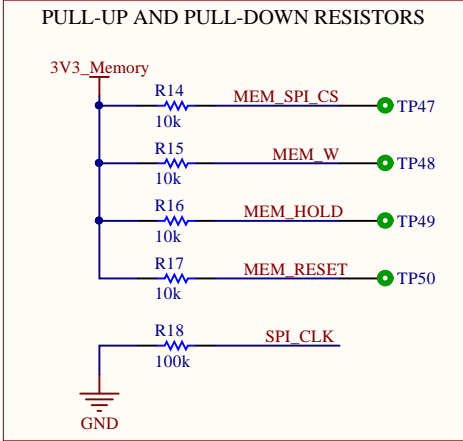




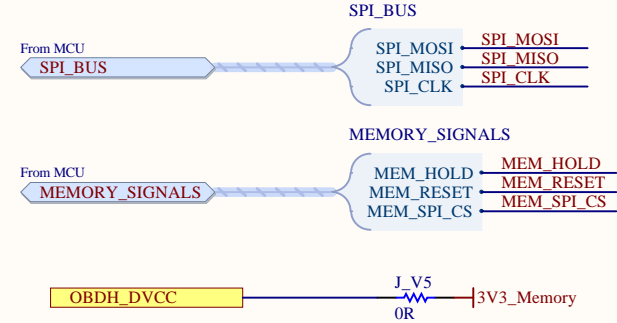
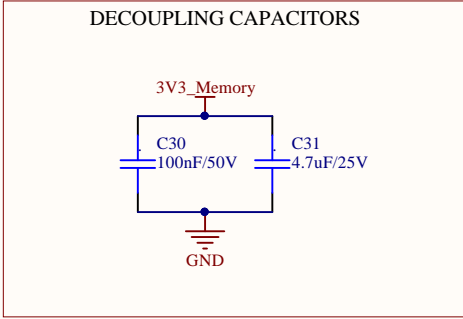
Title Analog Circuits		
Size: A4	Project: FloripaSat	Revision: V0.1
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Drawn By: André M. P. Mattos		Model: Eng 2 ALT

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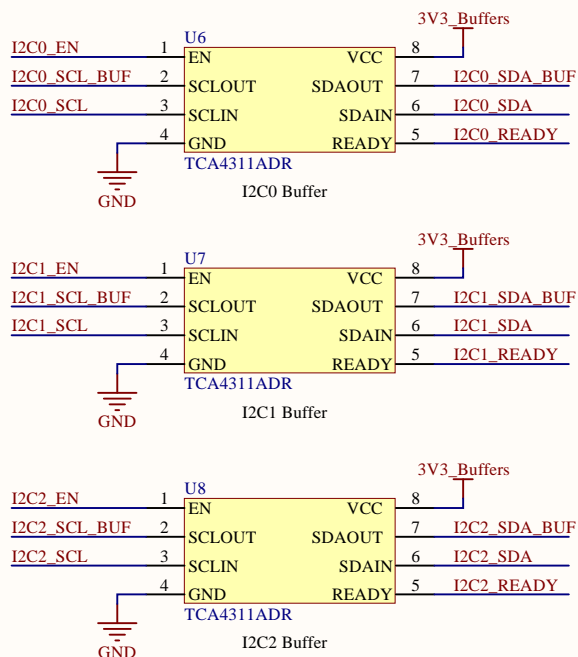
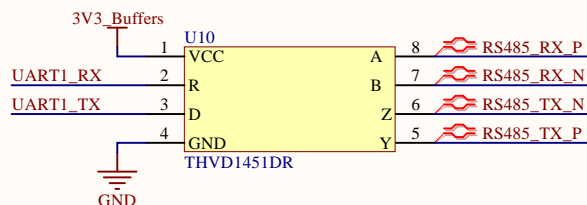




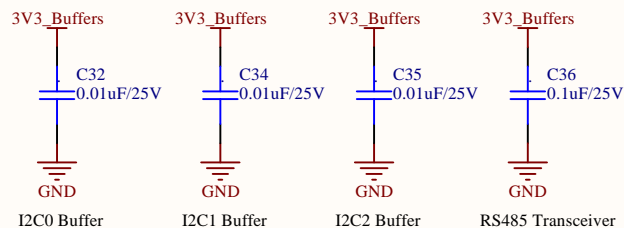
Memory Operation:
To be defined



I2C BUFFERS

RS485 TRANSCEIVER
(Full-Duplex)

DECOUPLING CAPACITORS



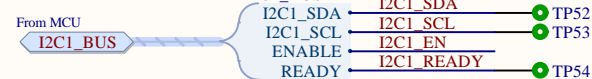
UART1_BUS



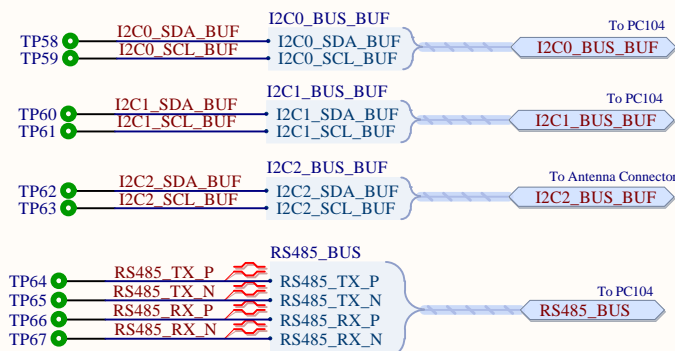
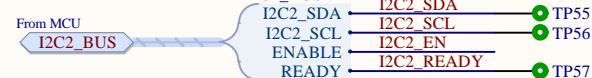
I2C0_BUS



I2C1_BUS



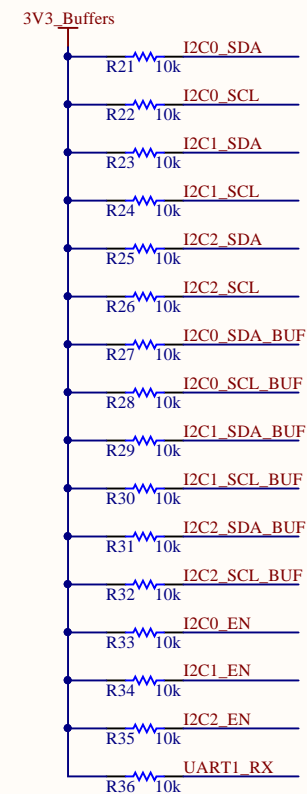
I2C2_BUS



TERMINATION RESISTORS



PULL-UP RESISTORS

Title **Communication Buffers**

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