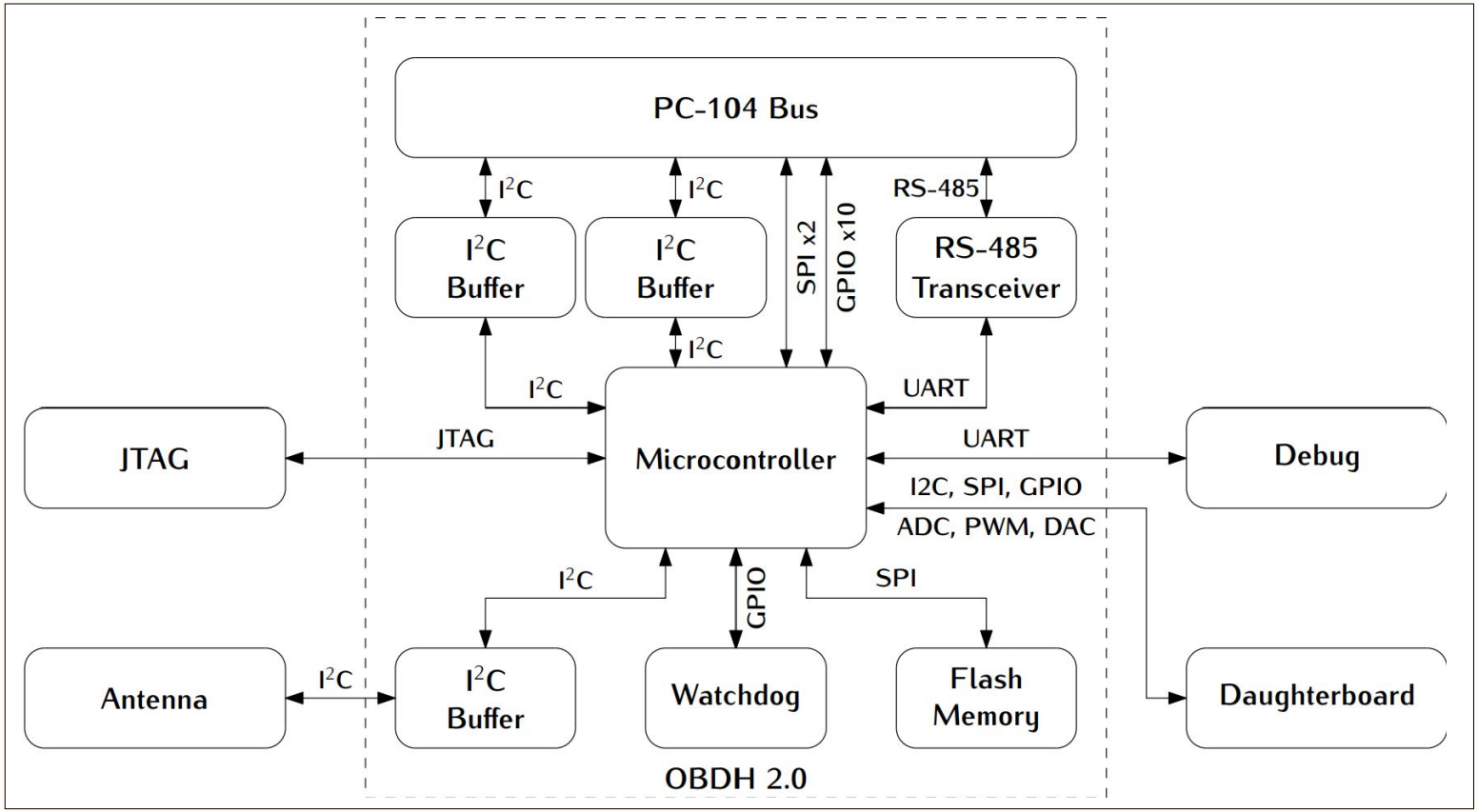

FloripaSat-II OBDH 2.0 ALT Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Cezar A. Rigo, Kleber Gouveia and Amanda B. Medeiros
- Based on FloripaSat-I OBDH designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Title **OBDH Hardware Archictecture**		
Size: A4	Project: FloripaSat	Revision:V0.2
Date: 31/01/2020 Time: 12:16:53		Sheet0 of 6
Drawn By: André M. P. Mattos		Model: Eng_2_ALT

UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

Topology
2_Topology.SchDoc

RS485_BUS
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N

I2C0_BUS_BUF
I2C0_SDA_BUF
I2C0_SCL_BUF

I2C1_BUS_BUF
I2C1_SDA_BUF
I2C1_SCL_BUF

I2C2_BUS_BUF
I2C2_SDA_BUF
I2C2_SCL_BUF

JTAG
JTAG_TCK
JTAG_TDO_TDI
TCK
TDO

UART0_BUS
UART0_TX
UART0_RX
Tx
Rx

TTC_SIGNALS
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS

SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK

PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3

DAUGHTER_BOARD_SIGNALS
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1

OBDH_DVCC
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
COMMON_VCC
ANTENNA_VCC
ANTENNA_GPIO

ESD PROTECTION
(Connected to the structure)
ESD
R_ESD
1M
GND

ANTENNA DEPLOYER INTERFACE
P4
ANTENNA_VCC
I2C2_SDA_BUF
I2C2_SCL_BUF
ANTENNA_GPIO
GND
6H_PicoBlade
P5_DNP
Header 6H

External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

POWER SUPPLY SOURCE SELECTOR
(from PC104 or JTAG)
P6_DNP
JTAG_VCC
COMMON_VCC
Header 2H
Debug header
OBDH_VCC
J_V0
0R
COMMON_VCC
Flight Jumper

PROGRAMMING HEADERS
(JTAG Spy Bi-Wire)
P2
DNP
JTAG_TDO_TDI
JTAG_TCK
JTAG_VCC
UART0_TX
UART0_RX
GND
Header 7x2
Debug JTAG Main MCU
P1
6H_PicoBlade
Flight Model JTAG Main MCU

DAUGHTER BOARD INTERFACE
(Generic Interface)
P3
OBDH_DVCC
ANTENNA_VCC
BATTERY_VCC
D_BOARD_GPIO0
D_BOARD_GPIO2
SPI_CLK
SPI_MISO
SPI_MOSI
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
GND
D_BOARD_GPIO1
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
I2C2_SDA_BUF
I2C2_SCL_BUF
FSI-110-03-X-D-AD

External Communication Buses Description:

BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

PC104 INTERFACE
U16A
PC104_INTERNAL
U16B
PC104_EDGE

External Communication Buses Description:

BUS1 (RS485): Payload EDC interface
Dedicated channel - UART1
PAYLOAD_0_ENABLE - Logical enable of the Payload EDC

BUS2 (I2C): Payload X interface
Dedicated channel - I2C0
PAYLOAD_1_ENABLE - Logical enable of the Payload X

BUS3 (I2C): EPS interface
Dedicated channel - I2C1

BUS7 (SPI)(H2): TTC interface
Shared Channel - SPI
TTC_SPI_CS - TTC chip select

BUS8 (SPI)(H1): Main Radio interface
Shared Channel - SPI
MAIN_RADIO_SPI_CS - Main radio chip select
MAIN_RADIO_GPIOx - GPIO configuration pins
MAIN_RADIO_RESET - Main radio reset
MAIN_RADIO_ENABLE - Enable for the Main Radio regulator in EPS

ADDITIONAL PC104 INTERFACES
J_PC1 I2C0_SDA_BUF
J_PC2 I2C0_SCL_BUF
J_PC3 I2C1_SDA_BUF
J_PC4 I2C1_SCL_BUF
J_PC5 SPI_MOSI
J_PC6 SPI_MISO
J_PC7 SPI_CLK
J_PC8 PC104_GPIO0
J_PC9 PC104_GPIO1
J_PC10 PC104_GPIO2
J_PC11 PC104_GPIO3
J_PC12 UART0_TX
J_PC13 UART0_RX
0R DNP

Additional Communication Buses Description:
(Used by demand, do not place unless necessary)

BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (UART): UART0
BUS14 (GPIO): 4 GPIOs

Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12

Allow PC104 flexibility and device sharing:
BUS13 - Require to desactivate debug routines.
BUS14 - Dedicated use of PC104.

Title: **OBDH Interface**			UFSC - SpaceLab University Campus - Trindade Dep. of Electrical Engineering - CTC Florianópolis, Santa Catarina, Brazil CEP: 88040 - 900
Size: A3	Project: FloripaSat	Revision: V0.2	
Date: 31/01/2020	Time: 12:16:53	Sheet 1 of 6	
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	

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Analog_Circuits
4_Analog_Circuits.SchDoc

WATCHDOG_SIGNALS
ADC_READINGS
VREF
OBDH_AVCC
ANTENNA_VCC
COMMON_VCC
OBDH_DVCC

Analog Circuits Info:
- Watchdog: Maximum timeout of 1.6 seconds and minimum voltage of 2.9V.
- Sensors: Voltage and Current.
- Voltage reference: 3V reference for ADC.
- Noise/Isolation: Decoupling capacitors and ferrites.

- Operation Check:
Watchdog: Violate the timeout and voltage thresholds.
Sensors: Analyse the TP6 and TP7 voltage.
Voltage reference: Check the 3V output.

MCU_OBDH
3_MCU_Main.SchDoc

WATCHDOG_SIGNALS
ADC_READINGS
VREF
OBDH_AVCC
DAUGHTER_BOARD_SIGNALS
MEMORY_SIGNALS
SPI_BUS
PC104_GPIOs
UART0_BUS
JTAG
I2C0_BUS
I2C1_BUS
I2C2_BUS
UART1_BUS
TTC_SIGNALS
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
ANTENNA_GPIO
OBDH_DVCC

Microcontroller (MSP430F6659):
- Memory: 512kB flash memory and 64kB RAM
- Clock: 2MHz (CPU and peripherals) and 32.768kHz
- Sensors/Monitor: Temperature, Watchdog and voltage monitor
- GPIO/ADC/DAC/USCI Channels:
GPIO: 74 (31 used)
ADC: 12 (5 used)
DAC: 2 (2 used)
USCI: 6 (6 used)

Non Volatile Memory
5_Non_Volatile_Memory.SchDoc

MEMORY_SIGNALS
SPI_BUS
OBDH_DVCC

Memory Info:
- SPI: Standard SPI protocol
- Size: 1Gbits
- Sector Size: 64Kbits
- SubSector Size: 32Kbits
- SubSubSector Size: 4Kbits
- Operation Check:
Perform a read operation to check the manufacturer ID.

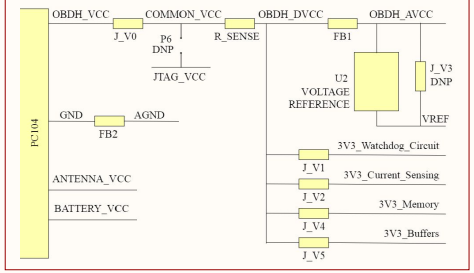
Communication Buffers
6_Communication_Buffers.SchDoc

I2C0_BUS
I2C1_BUS
I2C2_BUS
UART1_BUS
OBDH_DVCC
I2C0_BUS_BUF
I2C1_BUS_BUF
I2C2_BUS_BUF
RS485_BUS

Buffers/Transceiver Info:
- I2C Buffers: Isolate (only logically) master and slave to prevent major problems in case of operation fault.
- RS485 Transceiver: Convert UART protocol to RS485 (full-duplex).

- Operation Check:
Buffers: Check TP51, TP54 and TP57 voltage level (high indicates properly operation). Also, perform loopbacks to validate completely.
Transceiver: Perform a loopback communication by connecting TX to RX and analyse the waveforms at the oscilloscope (complementary behavior, synchronization and signal quality).

ANTENNA_VCC
COMMON_VCC
OBDH_DVCC



Power Supply Info:

- OBDH_VCC (3V3): From OBDH regulator in the EPS board
- COMMON_VCC (3V3): Common switch to allows JTAG supply
- JTAG_VCC (3V3): From the JTAG debugger

- OBDH_DVCC (3V3): Digital circuits
- OBDH_AVCC (3V3): Analog circuits
- VREF (3V): ADC reference voltage

- ANTENNA_VCC (3V3): From Antenna regulator in the EPS board
- BATTERY_VCC (5V4 - 8V4): Unregulated battery voltage

- GND(0V):Ground
- AGND(0V): Analog Ground

MCU Test Points:

TP1, TP2: JTAG Spy Bi-Wire
TP21, TP22, TP23, TP24: JTAG Default
TP3, TP4, TP5: SPI Channel
TP6: OBDH Current ADC Raw
TP7: OBDH Voltage ADC Raw
TP8: Manual Reset (force reset)
TP9: Watchdog Toggle Pin (timeout)
TP10, TP11, TP12, TP20: MCU GPIOs
TP13: RTCCLK Output
TP16, TP17, TP18, TP25, TP26, TP27: USB
TP19: DAC Channel
TP28, TP29, TP30: Main Radio GPIOs
TP31: Main Radio RESET
TP32: Main Radio ENABLE
TP33: Main Radio Chip Select
TP34: TTC Chip Select
TP35, TP36, TP37: Daughter Board GPIO/DAC/ADC
TP38, TP39: Daughter Board Chip Selects
TP40, TP41: Payload Logical Enable

Analog Circuits Test Points:

TP42: OBDH_DVCC
TP43: OBDH_AVCC
TP44: ANTENNA_VCC
TP45: VREF
TP46: COMMON_VCC

Memory Test Points:

TP47: Memory Chip Select
TP48: Write Protection
TP49: Memory Hold
TP50: Memory Reset

Communication Test Points:

TP68,TP69: I2C0 From MCU
TP51: Ready Flag From Buffer 0
TP58,TP59: I2C0 From Buffer 0

TP52,TP53: I2C1 From MCU
TP54: Ready Flag From Buffer 1
TP60,TP61: I2C1 From Buffer 1

TP55,TP56: I2C2 From MCU
TP57: Ready Flag From Buffer 2
TP62,TP63: I2C2 From Buffer 2

TP64,TP65,TP66,TP67: RS485

Title **OBDH Topology**			*UFSC - SpaceLab*
Size: A3	Project: FloripaSat	Revision: V0.2	*University Campus - Trindade*
Date: 31/01/2020	Time: 12:16:53	Sheet 2 of 6	*Dep. of Electrical Engineering - CTC*
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

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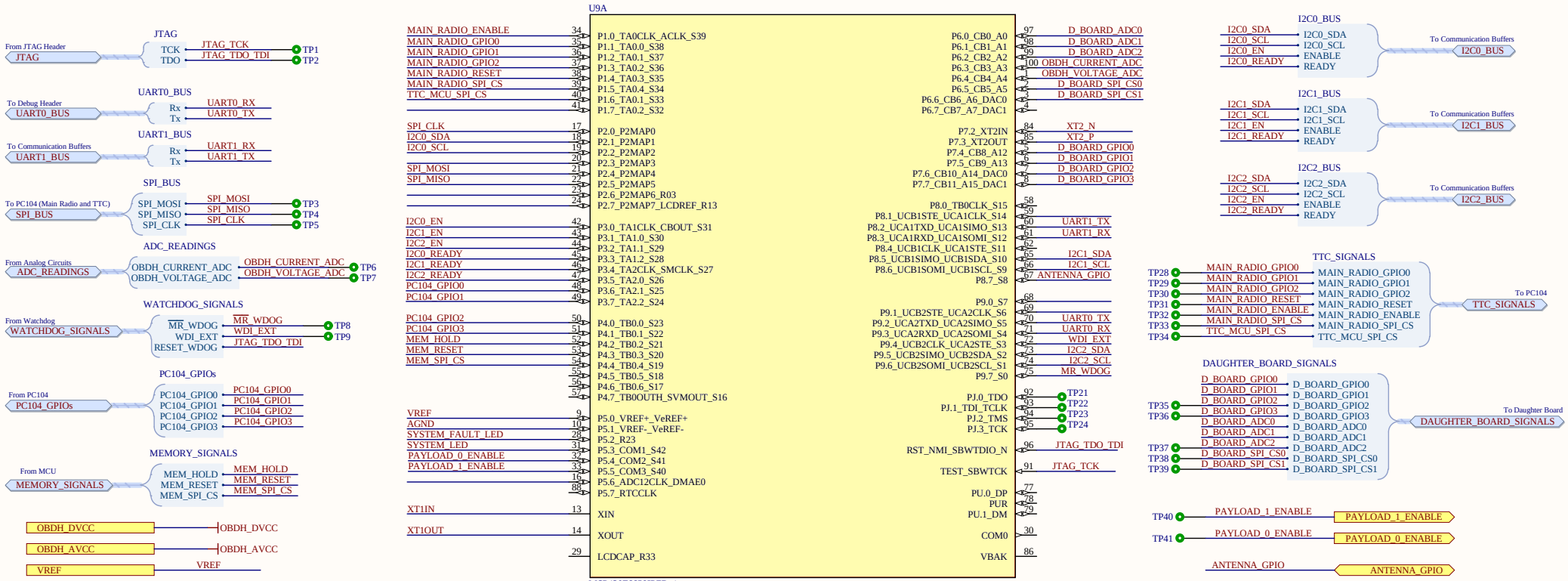
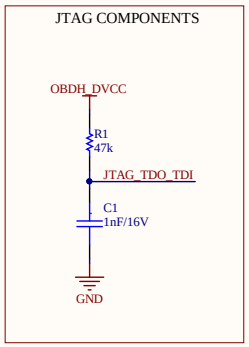
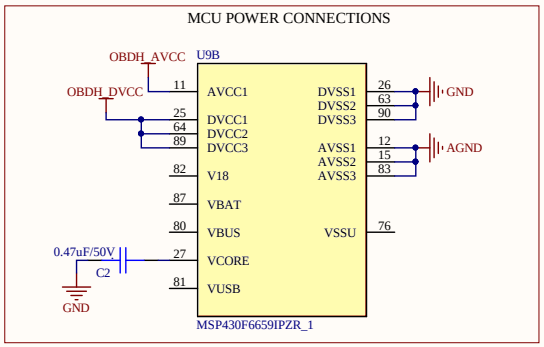
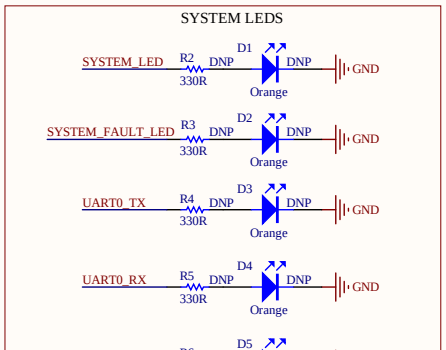




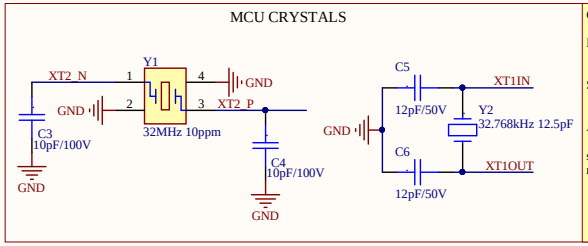




Communication Assigment and Configuration:

- USCI_A0 - SPI: (Memory, Main Radio, TTC and Daughter board)
  Chip Selects:1 Memory, 1 Main radio, 1 TTC and 2 Daugther board
  Config: Length - 8bits, Phase - High, Polarity - Low, Endianness - MSB, Data Rate - 400kbps
- USCI_A1 - UART1: (Transceiver RS485)
  Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_A2 - UART0: (Debug)
  Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_B0 - I2C0: (Buffer I2C)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B1 - I2C1: (Buffer I2C)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B2 - I2C2: (Buffer I2C)(Antenna and Daughter Board)
  Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps

All USCIs uses the SMCLK as clock source



Clock Configuration:

MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.

SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.

ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.

LEDs Assigment:

- SYSTEM LED (D1): (P5.3) Watchdog reset (blink each second)
- SYSTEM FAULT(D2): (P5.2) Active in case of hardware check routine failure
- UART DEBUG (D3, D4, D5, D6): UART TX and RX operation checks

Daughter Board Interface:

- Power Supply:
  OBDH_DVCC (3V3), ANTENNA_VCC (3V3), BATTERY_VCC(5V4-8V4)
- Inputs/Outputs:
  GPIO0(GPIO/ADC), GPIO1(GPIO/ADC), GPIO2(GPIO/ADC/DAC), GPIO3(GPIO/ADC/DAC)
  ADC0(ADC/GPIO), ADC1(ADC/GPIO), ADC2(ADC/GPIO)
- Communication:
  SPI (2 chip selects avaliable) and I2C (shared with antenna)

Title: **OBDH MCU Main**			*UFSC - SpaceLab*
Size: A3	Project: FloripaSat	Revision: V0.2	*University Campus - Trindade*
Date: 31/01/2020	Time: 12:16:54	Sheet 3 of 6	*Dep. of Electrical Engineering - CTC*
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

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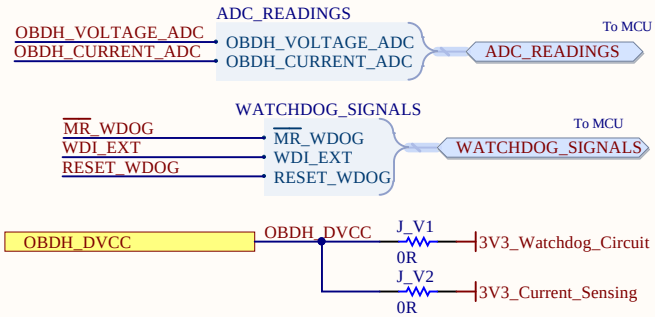
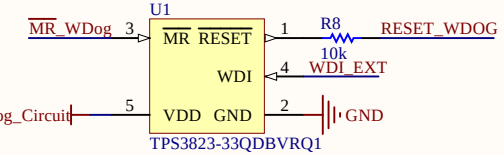
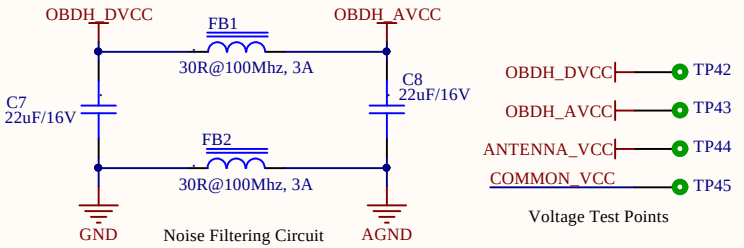


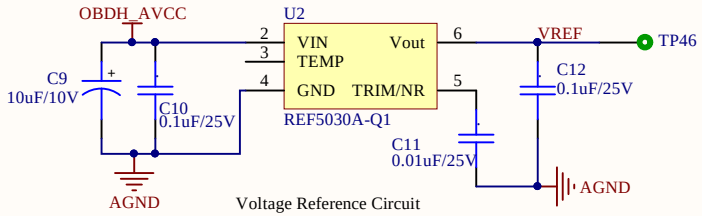
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER



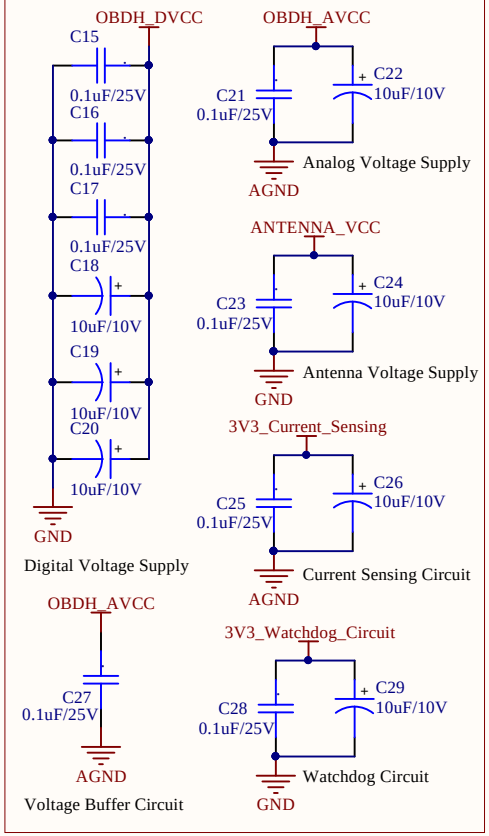
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

VOLTAGE REFERENCES



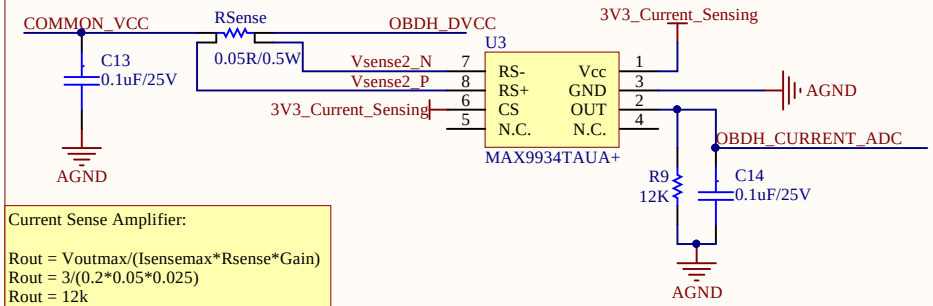


DECOUPLING CAPACITORS



INTERNAL MEASUREMENT CIRCUITS

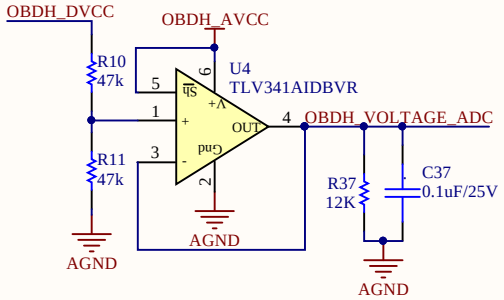
Current Sensing Circuit



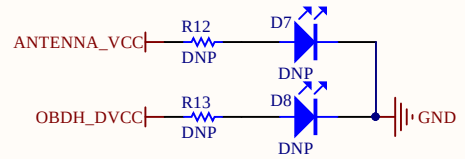
Current Sense Amplifier:

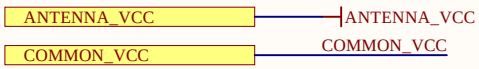
Rout = Voutmax/(Isensemax*Rsense*Gain)
Rout = 3/(0.2*0.05*0.025)
Rout = 12k

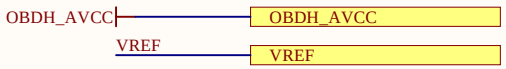
Voltage Buffer Circuit



LEDS SYSTEM







Title **Analog Circuits**			
Size: A4	Project: FloripaSat	Revision: V0.2	
Date: 31/01/2020	Time: 12:16:54	Sheet 4 of 6	
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	

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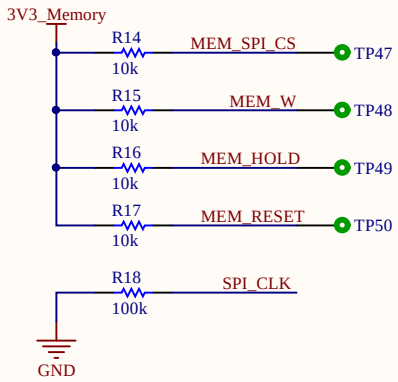
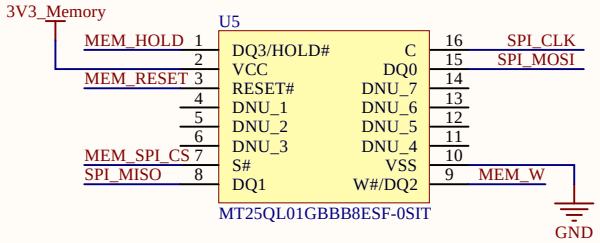
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

PULL-UP AND PULL-DOWN RESISTORS



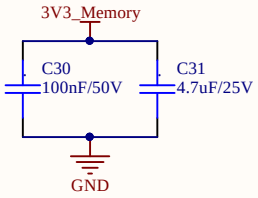
NON-VOLATILE MEMORY

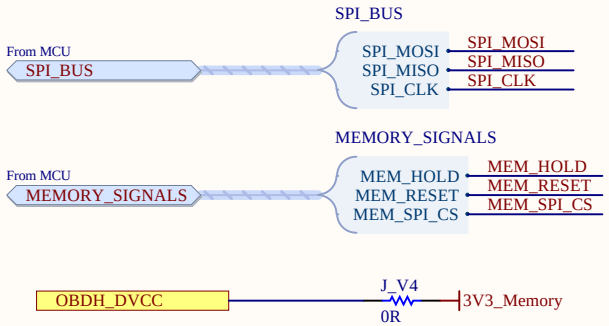


Memory Operation:

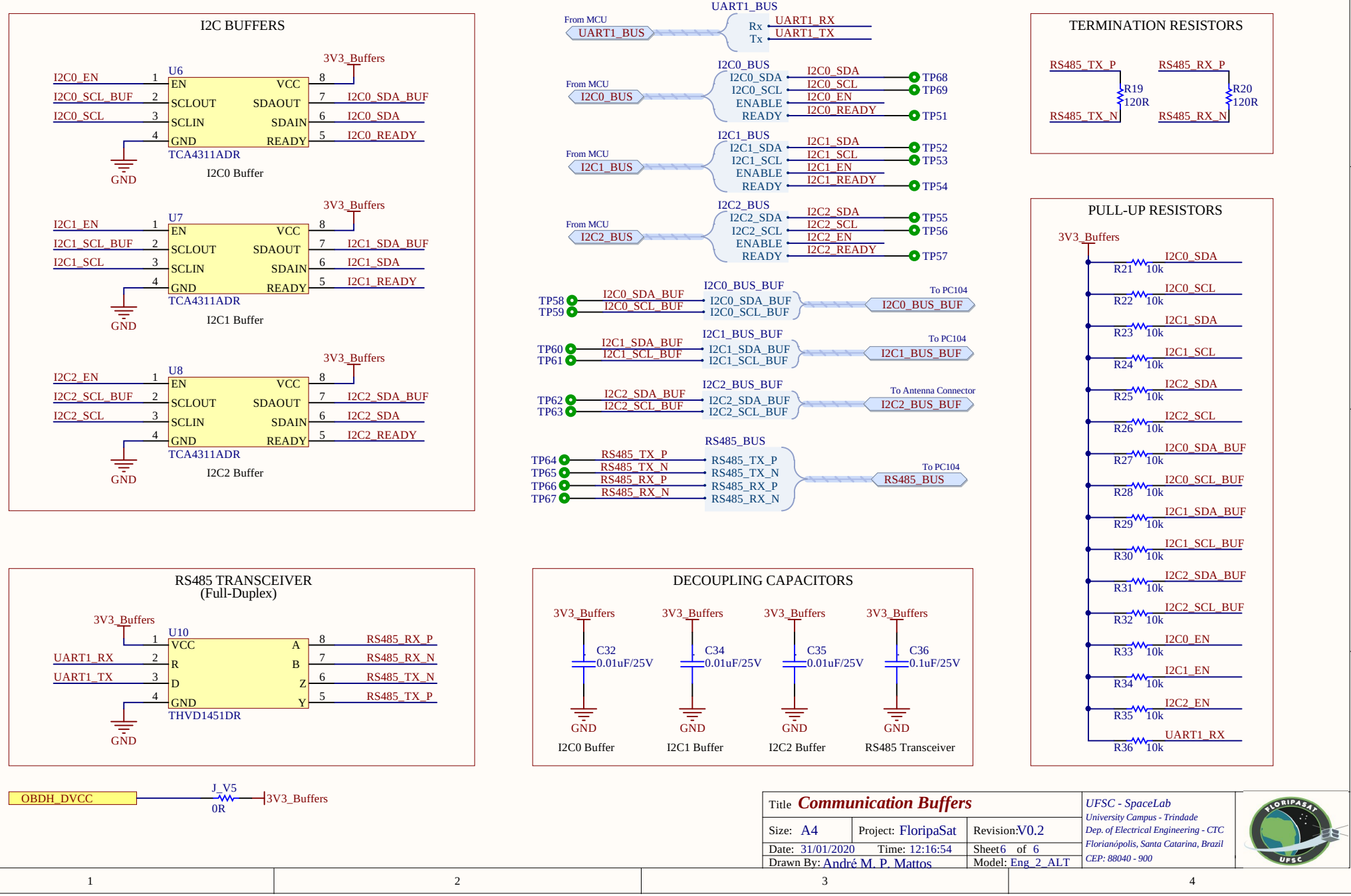
To be defined

DECOUPLING CAPACITORS





Title **Non Volatile Memory**			*UFSC - SpaceLab*
Size: A4	Project: FloripaSat	Revision:V0.2	*University Campus - Trindade*
Date: 31/01/2020	Time: 12:16:54	Sheet5 of 6	*Dep. of Electrical Engineering - CTC*
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900


I2C BUFFERS
3V3_Buffers
U6
I2C0_EN
I2C0_SCL_BUF
I2C0_SCL
EN
SCLOUT
SCLIN
GND
VCC
SDAOUT
SDAIN
READY
I2C0_SDA_BUF
I2C0_SDA
I2C0_READY
TCA4311ADR
GND
I2C0 Buffer
U7
I2C1_EN
I2C1_SCL_BUF
I2C1_SCL
I2C1_SDA_BUF
I2C1_SDA
I2C1_READY
I2C1 Buffer
U8
I2C2_EN
I2C2_SCL_BUF
I2C2_SCL
I2C2_SDA_BUF
I2C2_SDA
I2C2_READY
I2C2 Buffer
UART1_BUS
From MCU
UART1_BUS
Rx
Tx
UART1_RX
UART1_TX
I2C0_BUS
I2C0_SDA
I2C0_SCL
ENABLE
READY
I2C0_EN
TP68
TP69
TP51
I2C1_BUS
I2C1_SDA
I2C1_SCL
I2C1_EN
I2C1_READY
TP52
TP53
TP54
I2C2_BUS
I2C2_SDA
I2C2_SCL
I2C2_EN
I2C2_READY
TP55
TP56
TP57
I2C0_BUS_BUF
TP58
TP59
To PC104
I2C1_BUS_BUF
TP60
TP61
I2C2_BUS_BUF
TP62
TP63
To Antenna Connector
RS485_BUS
TP64
TP65
TP66
TP67
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N
TERMINATION RESISTORS
R19
120R
R20
PULL-UP RESISTORS
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
10k
RS485 TRANSCEIVER
(Full-Duplex)
U10
VCC
R
D
GND
A
B
Z
Y
THVD1451DR
DECOUPLING CAPACITORS
C32
0.01uF/25V
C34
0.01uF/25V
C35
0.01uF/25V
C36
0.1uF/25V
I2C0 Buffer
I2C1 Buffer
I2C2 Buffer
RS485 Transceiver
OBDH_DVCC
J_V5
0R
Title Communication Buffers
Size: A4
Project: FloripaSat
Revision:V0.2
Date: 31/01/2020
Time: 12:16:54
Sheet6 of 6
Drawn By: André M. P. Mattos
Model: Eng_2_ALT
UFSC - SpaceLab
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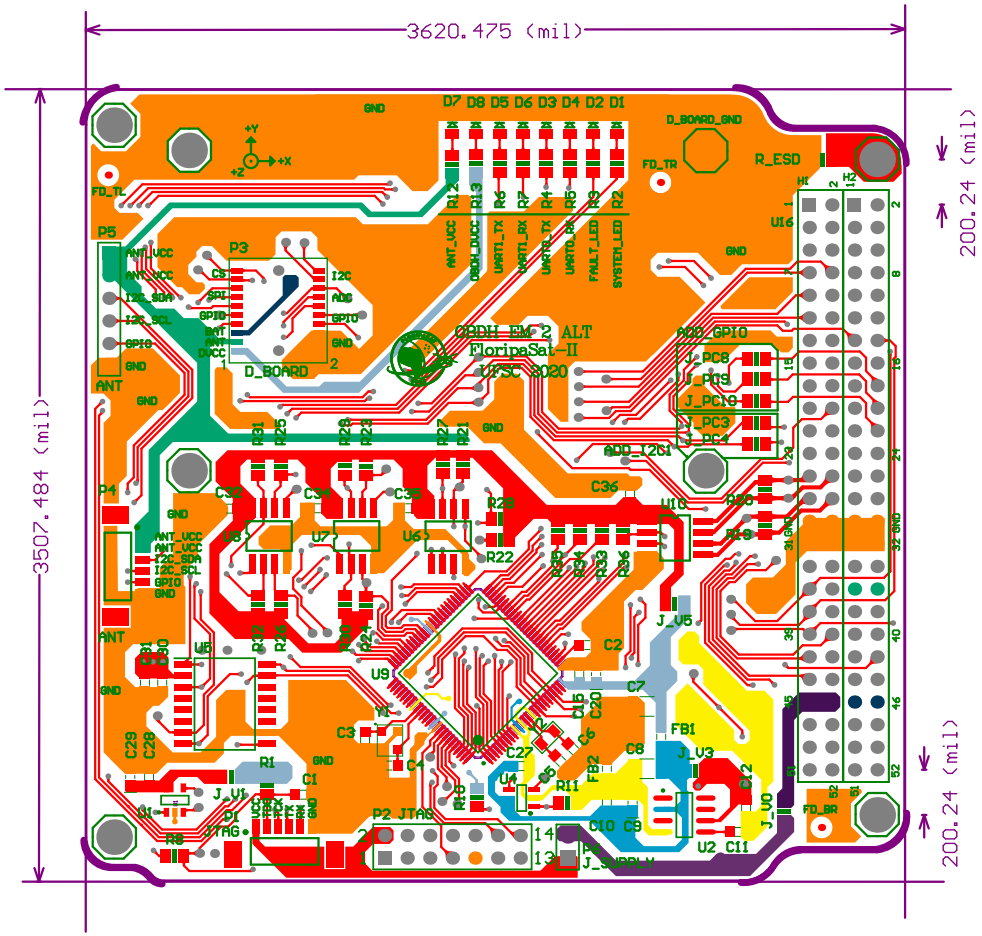
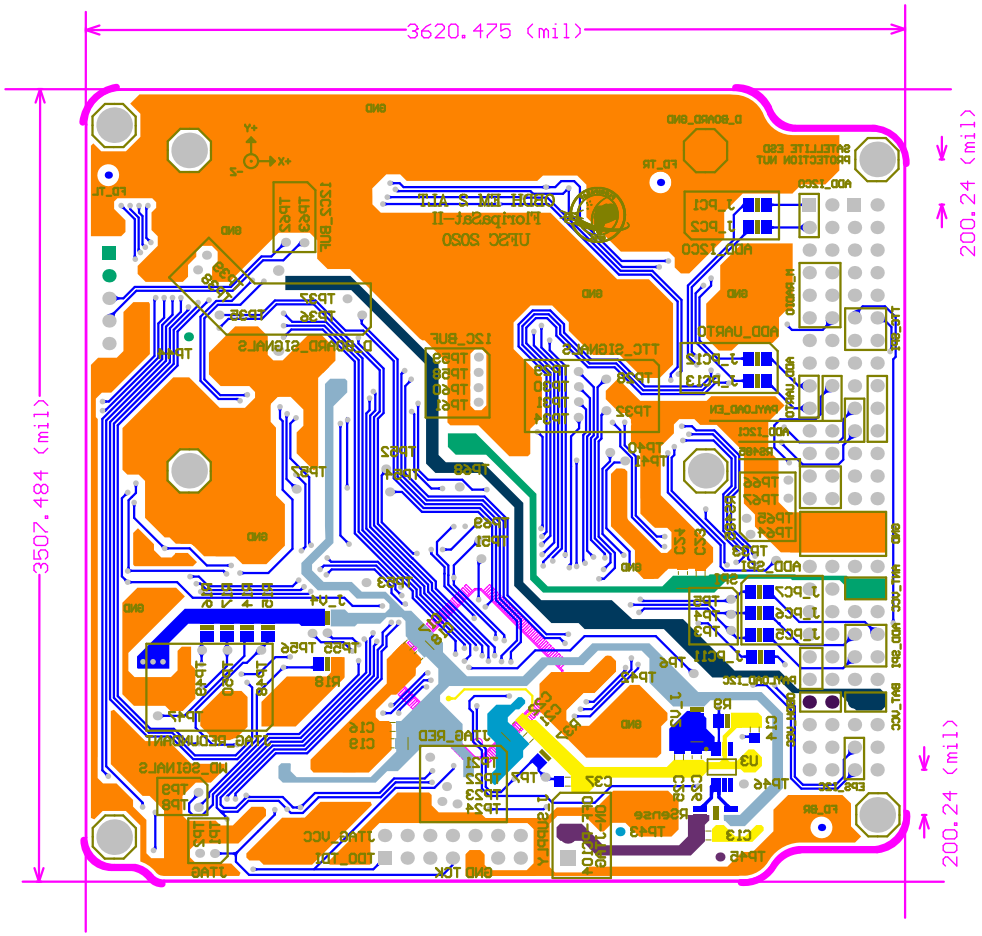


General SPEC:

Cupper base 1OZ:
PCB Material: FR4
PCB Tickness: 1.6mm
PCB Surface: ENIG
Vias: Force Complete Tenting

TITULO: OBDH 2018 UFSC		**REV.** 01	**VER.** Eng_2_ALT
MATERIAL: FR4	**Silkscreen color: green**		
Board Tickness: 1.6mm	**Layers: 02**	**Drawing**	**DATE**
PCB Surface: ENIG		Andre M. P. Mattos	01/12/2019



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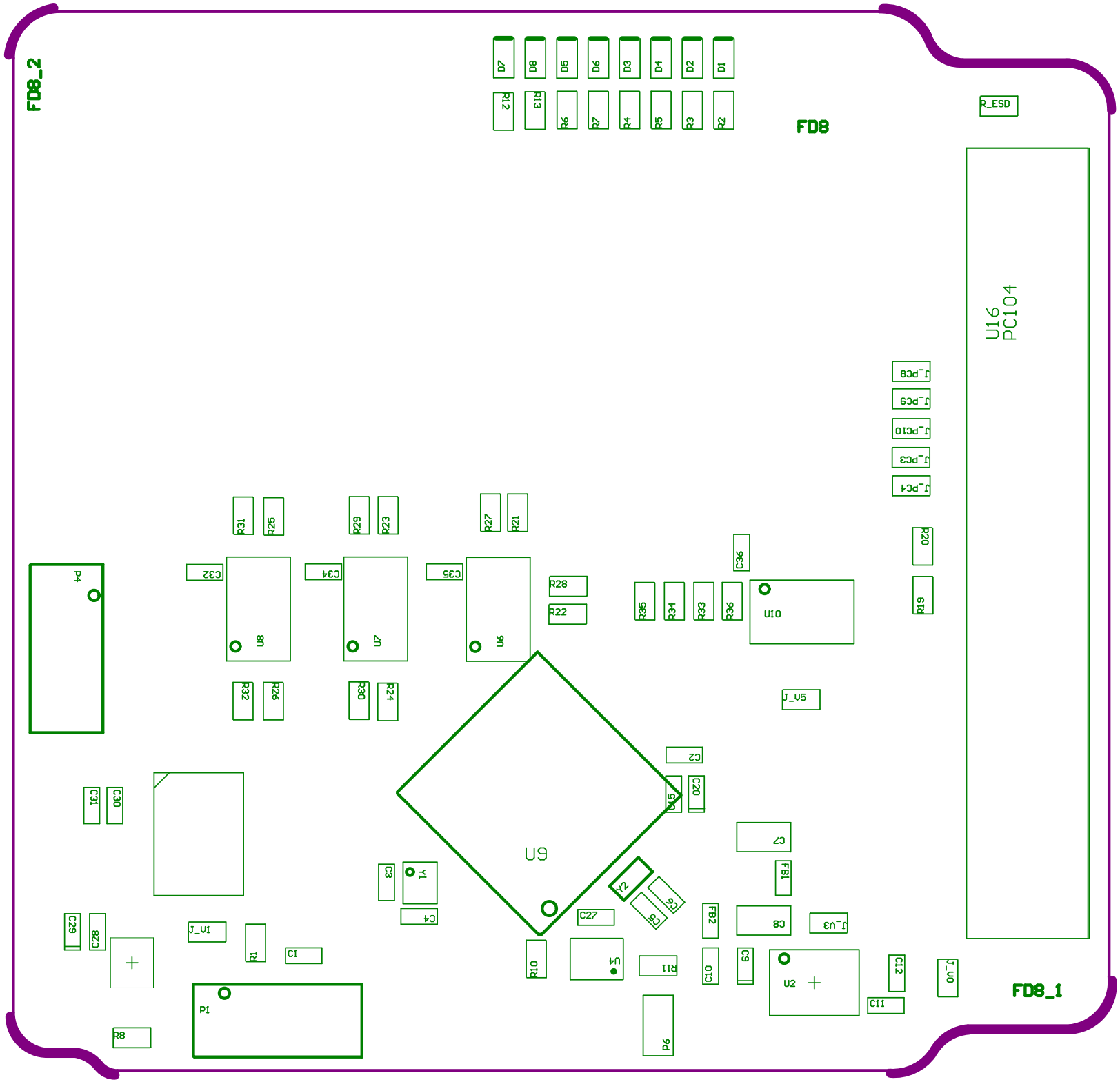
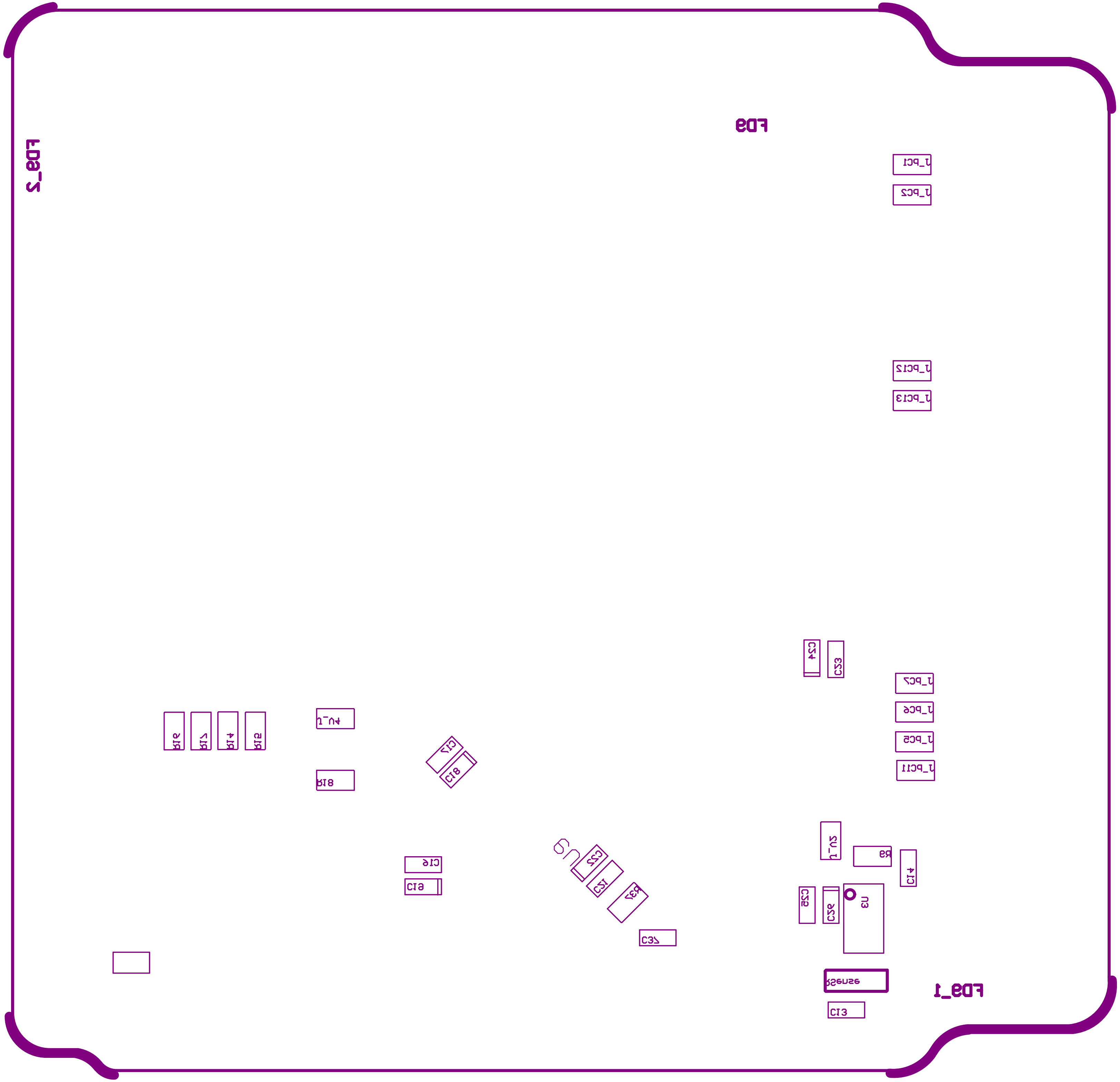
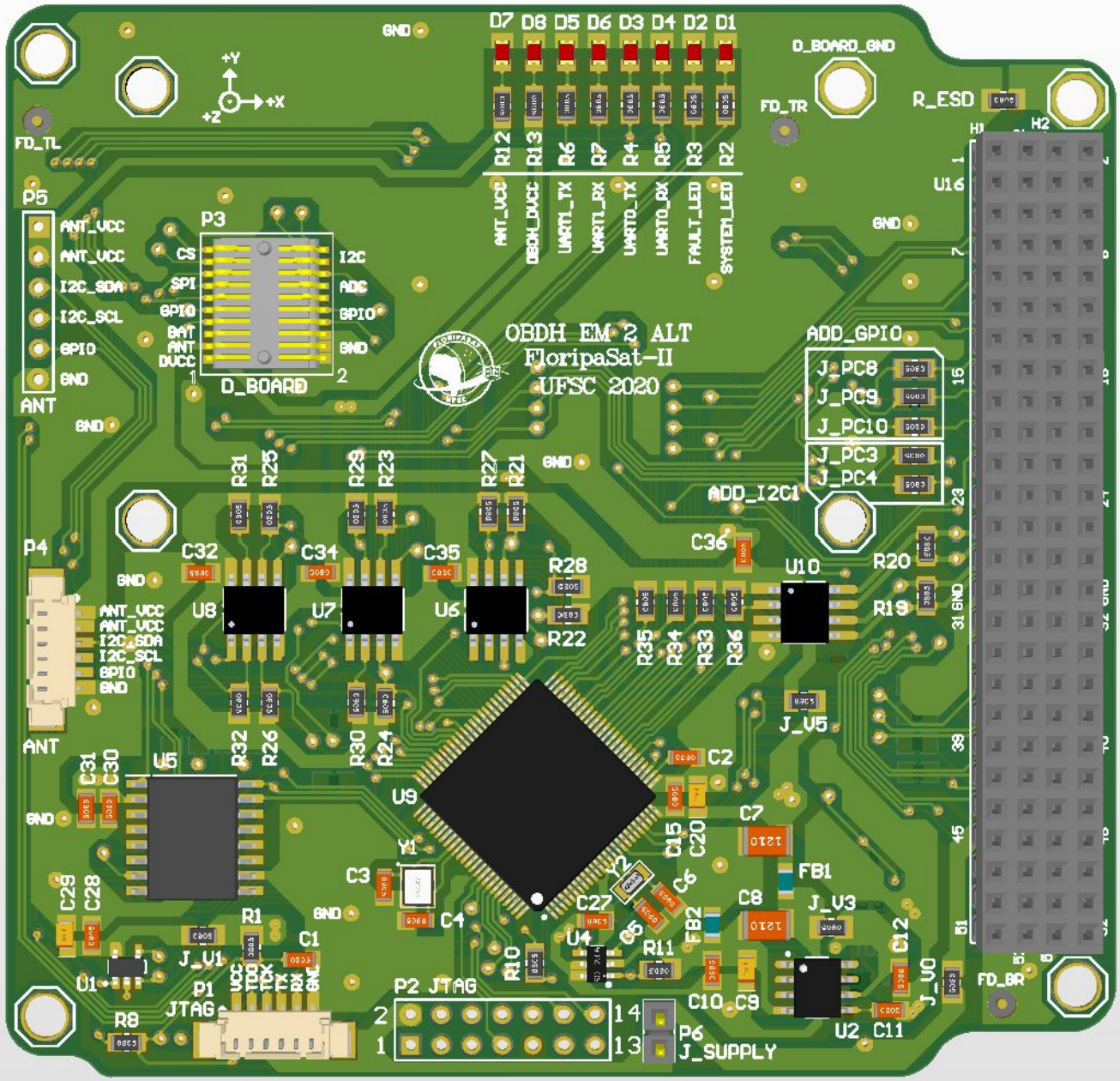
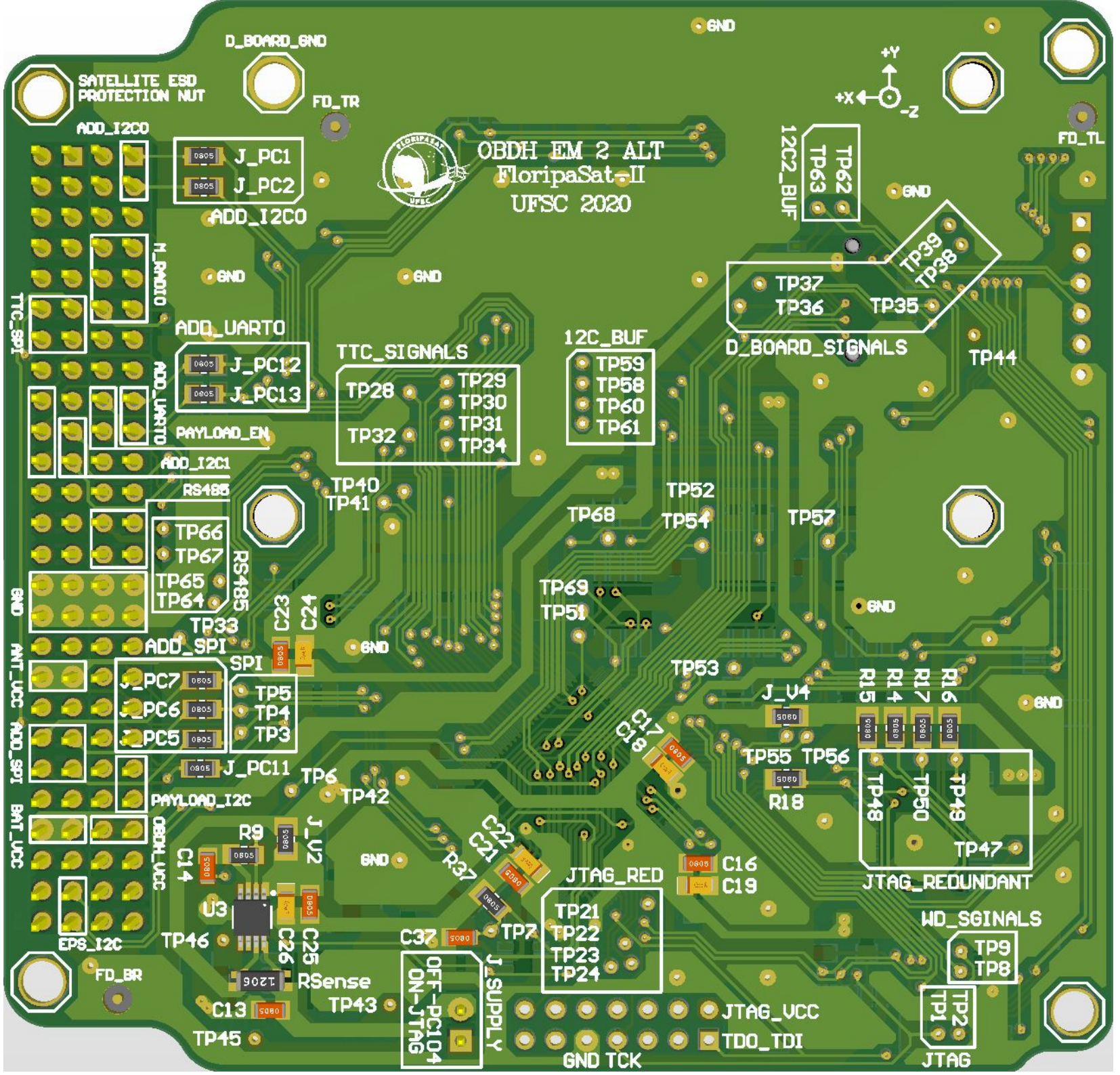

FD8_2
FD8
FD8_1
D7
D8
D5
D6
D3
D4
D2
D1
R12
R13
R6
R7
R4
R5
R3
R2
R_ESD
U16
PC104
J_PC8
J_PC9
J_PC10
J_PC3
J_PC4
R20
R19
C36
U10
R35
R34
R33
R36
J_U5
R28
R22
C35
U6
R27
R21
C34
U7
R29
R23
C32
U8
R31
R25
P4
R32
R26
R30
R24
C2
D5
C20
U5
C7
FB1
C3
V1
C4
Y2
C5
C6
C27
FB2
C8
J_U3
R10
U4
R11
C10
C9
U2
C12
C11
J_U6
P6
P1
C31
C30
C29
C28
J_V1
R1
C1
R8


FD9
FD9_1
FD9_2
J_PC1
J_PC2
J_PC12
J_PC13
J_PC7
J_PC6
J_PC5
J_PC11
C24
C23
R16
R17
R14
R15
U_V4
R18
C17
C18
C16
C19
U9
C22
C21
R37
C37
U_Z1
R9
C14
C25
C26
U3
RSense
C13


OBDH EM 2 ALT
FloripaSat-II
UFSC 2020
D_BOARD
ANT
JTAG
P6
J_SUPPLY
D_BOARD_GND
R_ESD
FD_TL
FD_TR
FD_BR
ADD_GPIO
ADD_I2C1
GND
ANT_VCC
I2C_SDA
I2C_SCL
GPIO
UART1_TX
UART1_RX
UART0_TX
UART0_RX
FAULT_LED
SYSTEN_LED
OBDH_DUCC
J_V0
J_V1
J_V3
J_V5
J_PC8
J_PC9
J_PC10
J_PC3
J_PC4


SATELLITE ESD PROTECTION NUT
D_BOARD_GND
FD_TR
GND
+Y
+X
-Z
FD_TL
OBDH EM 2 ALT
FloripaSat-II
UFSC 2020
ADD_I2C0
J_PC1
J_PC2
ADD_I2C0
I2C2_BUF
TP62
TP63
GND
GND
GND
TP39
TP38
TP37
TP36
TP35
D_BOARD_SIGNALS
TP44
N_RADIO
TTC_SPI
ADD_UART0
J_PC12
J_PC13
TTC_SIGNALS
TP28
TP29
TP30
TP31
TP32
TP34
I2C_BUF
TP59
TP58
TP60
TP61
PAYLOAD_EN
ADD_I2C1
RS485
TP40
TP41
TP68
TP52
TP54
TP57
TP66
TP67
TP65
TP64
RS485
TP33
C23
C24
TP69
TP51
GND
GND
ADD_SPI
SPI
TP53
GND
ANT_VCC
ADD_SPI
BAT_VCC
J_PC7
J_PC6
J_PC5
TP5
TP4
TP3
J_V4
R15
R14
R17
R16
C17
C18
TP55
TP56
R18
TP48
TP50
TP48
TP47
JTAG_REDUNDANT
J_PC11
TP6
TP42
PAYLOAD_I2C
OBDH_VCC
R9
J_U2
C14
GND
C22
C21
R37
JTAG_RED
C16
C19
U3
TP46
C26
C25
TP7
C37
TP21
TP22
TP23
TP24
WD_SGINALS
TP9
TP8
EPS_I2C
FD_BR
RSense
C13
TP43
OFF-PC104
ON-JTAG
J_SUPPLY
JTAG_VCC
TDO_TDI
GND TCK
TP2
TP1
JTAG
TP45

Bill of Materials

OBDH Interface

Source Data From: OBDH_Eng_Model_2_ALT.PrjPcb
Project: OBDH_Eng_Model_2_ALT.PrjPcb
Variant: None

Creation Date: 31/01/2020 12:17:14
Print Date: 31-Jan-20 12:17:26 PM

Footprint	Comment	LibRef	Designator	Description	Quantity
CC0805	1nF/16V	Cap_Cer_X7R_1nF_16V_0603	C1	CAP CER 1nF 16V 0603 5%	1
CC0805	0.47uF/50V	Cap_Cer_X7R_0.47uF_50V_0805	C2	CAP CER 0.47UF 50V 10% X7R 0805	1
CC0805	10pF/100V	Cap_Cer_X7R_10pF_100V_0805	C3, C4	CAP CER 10pF 100V 0805	2
CC0805	12pF/50V	Cap_Cer_X7R_12pF_50V_0805	C5, C6	CAP CER 12pF 50V 0805	2
CC1210	22uF/16V	Cap_Cer_X7R_0.01uF_16V_1210	C7, C8	CAP CER 22uF 16V 10% X7R 1210	2
CC0805_Tantalum	10uF/10V	Cap_Tant_SMD_10uF_6V3_0805, Cap_Tant_SMD_10uF_10V_0805	C9, C18, C19, C20, C22, C24, C26, C29	CAP Tantalum 10uF 6.3V 10% 0805, CAP Tantalum 10uF 10V 20% 0805	8
CC0805	0.1uF/25V	Cap_Cer_X7R_0.1uF_25V_0805	C10, C12, C13, C14, C15, C16, C17, C21, C23, C25, C27, C28, C36, C37	CAP CER 0.1UF 25V 10% X7R 0805	14
CC0805	0.01uF/25V	Cap_Cer_X7R_0.01uF_50V_0805	C11, C32, C34, C35	CAP CER 0.01uF 25V 10% X7R 0805	4
CC0805	100nF/50V	Cap_Cer_X7R_100nF_50V_0603	C30	CAP CER 100nF 50V 0603 10%	1
CC0805	4.7uF/25V	Cap_Cer_X7R_4.7uF_25V_0805	C31	CAP CER 4.7UF 25V 10% X7R 0805	1
0805-LED	Orange	LED/R_0603	D1, D2, D3, D4, D5, D6	SMD Orange LED	6
0805-LED	DNP	LED/G_0805	D7, D8	SMD Green LED	2
IND0805	30R@100Mhz, 3A	FB_30R_3A_100MHz_0805	FB1, FB2	Ferrite Bead 30 OHM 3A 100MHz	2
0805	0R	R0R_JUMPER_1/16W_0805	J_PC1, J_PC2, J_PC3, J_PC4, J_PC5, J_PC6, J_PC7, J_PC8, J_PC9, J_PC10, J_PC11, J_PC12, J_PC13, J_V0, J_V1, J_V2, J_V3, J_V4, J_V5	RES 0R OHM 1/16W JUMPER 0805	19
HDR6 PicoBlade	6H_PicoBlade	Header 6H_PicoBlade	P1, P4	Header, 6-Pin, Right Angle	2
HDR2X7	Header 7x2	Header 7X2	P2	Header, 7-Pin, Dual row	1
FSI-110-03-X-D-AD	FSI-110-03-X-D-AD	FSI-110-03-X-D-AD	P3		1
HDR1X6H	Header 6H	Header 6H	P5	Header, 6-Pin, Right Angle	1
HDR 1X2	Header 2H	Header 2	P6	Header, 2-Pin	1
0805	47k	R27_5%_1/10W_0805	R1, R10, R11	RES 47k OHM 1/10W 1% 0805	3
0805	330R	R330R_1%_1/4W_0805	R2, R3, R4, R5, R6, R7	RES 330R OHM 1/4W 1% 0805	6
0805	10k	R10k_1%_1/8W_0805	R8, R14, R15, R16, R17, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34, R35, R36	RES 10K OHM 1/8W 1% 0805	21
0805	12K	R1.65K_1%_1/10W_0805	R9, R37	RES 1.65K OHM 1/10W 0.1% 0805	2
0805	DNP	R1.0k_1%_1/8W_0805	R12, R13	RES 1.0K OHM 1/8W 1% 0805	2
0805	100k	R100k_1%_1/8W_0805	R18	RES 100K OHM 1/8W 1% 0805	1
0805	120R	R120R_1%_1/4W_0805	R19, R20	RES 120R OHM 1/8W 1% 0805	2
0805	1M	R1000k_1%_1/8W_0805	R_ESD	RES 1000K OHM 1/8W 1% 0805	1
1206 - ohmite	0.05R/0.5W	R0.05R_0.5%_0.5W_1206	RSense	Current Sense Resistors - SMD 0.05ohm .5% 4 Terminal	1
DBV0005A_N	TPS3823-33QDBVRQ1	CMP-0338-00011-2	U1	Processor Supervisory Circuit, 1 Supply Monitored, -40 to 85 degC, 5-Pin SOT-23 (DBV), Green (RoHS & no Sb/Br)	1
SOIC-8	REF5030A-Q1	REF5030A-Q1	U2	REF5030A-Q1	1
MSOP-8	MAX9934TAUA+	MAX9934TAUA+	U3	MAX9934TAUA+	1
SOT-23 6L	TLV341AIDBVR	TLV341AIDBVR	U4	TLV341AIDBVR	1
SOIC127P1032X265-16N	MT25QL01GBB8ESF-0SIT	MT25QL01GBB8ESF-0SIT	U5	IC FLASH 1GBIT 108MHZ 16SOIC	1
SOIC8	TCA4311ADR	TCA4311ADR	U6, U7, U8	IC SIGNAL BUFFER I2C 8SOIC	3
PZ0100A_N	MSP430F6659IPZR_1	MSP430F6659IPZR_1	U9	Imported	1
SOIC8	THVD1451DR	THVD1451DR	U10	IC INTERFACE RS422_RS485 8SOIC	1
PC104	PC104_INTERNAL	PC104	U16	PC104	1
XTAL_ABM8X	32MHz 10ppm	XTAL_32MHz_SMD_4-SMD	Y1	32MHz ±10ppm Crystal 10pF 60 Ohm -40°C ~ 125°C	1
ABS06 0805	32.768kHz 12.5pF	Xtal_32.768kHz_12pF_2_SMD	Y2	32.768kHz ±20ppm Crystal 12.5pF 70 kOhm -40°C ~ 125°C	1
					123

Approved	Notes	