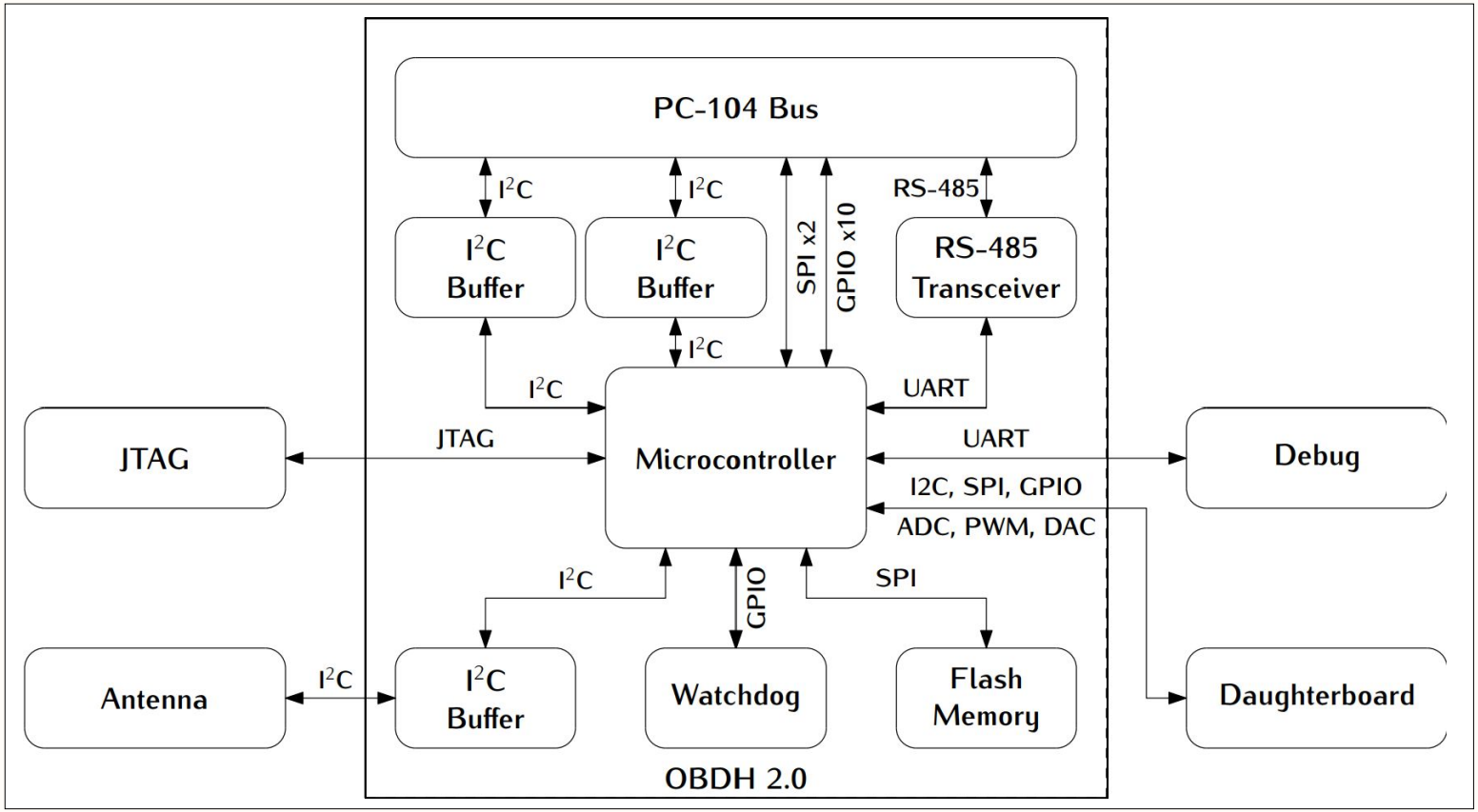

FloripaSat-II OBDH 2.0 ALT Hardware:

- Drawn by: André M. P. Mattos
- Reviewers: Cezar A. Rigo, Kleber Gouveia and Yan C. Azeredo
- Based on FloripaSat-I OBDH designed by: Sara V. Martinez
- Support: Gabriel M. Marcelino

Title **OBDH Hardware Archictecture**		
Size: A4	Project: FloripaSat	Revision:V0.3
Date: 20/08/2020 Time: 17:59:39		Sheet0 of 6
Drawn By: André M. P. Mattos		Model: Eng_2_ALT

UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900

Topology
2_Topology.SchDoc

UART1_BUS
UART1_RX
UART1_TX
Rx
Tx
UART1_BUS

PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
PC104_GPIO4
PC104_GPIO5
PC104_GPIO6
PC104_GPIOs

JTAG
JTAG_TCK
JTAG_TDO_TDI
TCK
TDO
JTAG

UART0_BUS
UART0_TX
UART0_RX
Tx
Rx
UART0_BUS

SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_BUS

DAUGHTER_BOARD_SIGNALS
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
DAUGHTER_BOARD_SIGNALS

COMMON_VCC
COMMON_VCC

ANTENNA_VCC
ANTENNA_VCC

RS485_BUS
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N
RS485_BUS

I2C0_BUS_BUF
I2C0_SDA_BUF
I2C0_SCL_BUF
I2C0_BUS_BUF

I2C1_BUS_BUF
I2C1_SDA_BUF
I2C1_SCL_BUF
I2C1_BUS_BUF

I2C2_BUS_BUF
I2C2_SDA_BUF
I2C2_SCL_BUF
I2C2_BUS_BUF

TTC_SIGNALS
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
TTC_SIGNALS

PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
OBDH_DVCC
ANTENNA_GPIO

ESD PROTECTION
(Connected to the structure)
ESD
R_ESD
1M
GND

RS485 ADDITIONAL HEADER
P8 DNP
RS485_RX_P
RS485_RX_N
RS485_TX_N
RS485_TX_P
Header 4H

ANTENNA DEPLOYER INTERFACE
P4
ANTENNA_VCC
I2C2_SDA_BUF
I2C2_SCL_BUF
ANTENNA_GPIO
GND
6H_PicoBlade
P5 DNP
Header 6H

External Communication Buses Description:

BUS4 (I2C): Antenna interface
Shared channel - I2C2

DAUGHTER BOARD INTERFACE
(Generic Interface)
P3
OBDH_DVCC
ANTENNA_VCC
BATTERY_VCC
D_BOARD_GPIO0
D_BOARD_GPIO2
SPI_CLK
SPI_MISO
SPI_MOSI
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
GND
D_BOARD_GPIO1
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
I2C2_SDA_BUF
I2C2_SCL_BUF
FSI-110-03-X-D-AD

External Communication Buses Description:

BUS5 (I2C): Daughter Board interface
Shared channel - I2C2

BUS6 (SPI): Daughter Board interface
Shared Channel - SPI
D_BOARD_SPI_CS0 - Daughter Board chip select 0
D_BOARD_SPI_CS1 - Daughter Board chip select 1

DEBUG HEADERS
P6 DNP
JTAG_VCC
COMMON_VCC
(from PC104 or JTAG)
Header 2H
Power Supply Source Selector
OBDH_VCC
J_V0
0R
COMMON_VCC
Flight Jumper
P7 DNP
UART0_TX
UART0_RX
Header 2H
UART Debug Header

PROGRAMMING HEADERS
(JTAG Spy Bi-Wire)
P2 DNP
JTAG_TDO_TDI
JTAG_TCK
GND
JTAG_VCC
UART0_TX
UART0_RX
Header 7x2
Debug JTAG Main MCU
P1
JTAG_VCC
JTAG_TDO_TDI
JTAG_TCK
UART0_TX
UART0_RX
6H_PicoBlade
GND
Flight Model JTAG Main MCU

External Communication Buses Description:

BUS0 (UART): Debug interface
Dedicated channel - UART0

BUS9 (JTAG): Debug interface
Dedicated channel - JTAG (Spi Bi-Wire)

PC104 INTERFACE
U16A
ADD_I2C0_SDA
ADD_I2C0_SCL
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
UART1_RX
UART1_TX
ADD_I2C1_SCL
ADD_I2C1_SDA
GND
SPI_CLK
SPI_MISO
SPI_MOSI
I2C0_SDA_BUF
I2C0_SCL_BUF
OBDH_VCC
MAIN_RADIO_GPIO1
MAIN_RADIO_ENABLE
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
MAIN_RADIO_SPI_CS
OBDH_VCC
PC104_INTERNAL
U16B
PC104_GPIO4
SPI_MOSI
TTC_MCU_SPI_CS
GND
ANTENNA_VCC
ADD_SPI_MISO
ADD_SPI_MOSI
BATTERY_VCC
I2C1_SDA_BUF
I2C1_SCL_BUF
PC104_GPIO5
PC104_GPIO6
SPI_CLK
SPI_MISO
ADD_GPIO0
ADD_GPIO1
ADD_GPIO2
GND
ANTENNA_VCC
ADD_SPI_CLK
ADD_GPIO3
BATTERY_VCC
PC104_INTERNAL

External Communication Buses Description:

BUS1 (RS485): Payload EDC interface
Dedicated channel - UART1 (at additional header)
PAYLOAD_0_ENABLE - Logical enable of the Payload EDC

BUS2 (I2C): Payload X interface
Dedicated channel - I2C0
PAYLOAD_1_ENABLE - Logical enable of the Payload X

BUS3 (I2C): EPS interface
Dedicated channel - I2C1

BUS7 (SPI)(H2): TTC interface
Shared Channel - SPI
TTC_SPI_CS - TTC chip select

BUS8 (SPI)(H1): Main Radio interface
Shared Channel - SPI
MAIN_RADIO_SPI_CS - Main radio chip select
MAIN_RADIO_GPIOx - GPIO configuration pins
MAIN_RADIO_RESET - Main radio reset
MAIN_RADIO_ENABLE - Enable for the Main Radio regulator in EPS

ADDITIONAL PC104 INTERFACES
ADD_I2C0_SDA J_PC1 I2C0_SDA_BUF 0R DNP
ADD_I2C0_SCL J_PC2 I2C0_SCL_BUF 0R DNP
ADD_I2C1_SDA J_PC3 I2C1_SDA_BUF 0R DNP
ADD_I2C1_SCL J_PC4 I2C1_SCL_BUF 0R DNP
ADD_SPI_MOSI J_PC5 SPI_MOSI 0R DNP
ADD_SPI_MISO J_PC6 SPI_MISO 0R DNP
ADD_SPI_CLK J_PC7 SPI_CLK 0R DNP
ADD_GPIO0 J_PC8 PC104_GPIO0 0R DNP
ADD_GPIO1 J_PC9 PC104_GPIO1 0R DNP
ADD_GPIO2 J_PC10 PC104_GPIO2 0R DNP
ADD_GPIO3 J_PC11 PC104_GPIO3 0R DNP

Additional Communication Buses Description:
(Used by demand, do not place unless necessary)

BUS10 (I2C): I2C0
BUS11 (I2C): I2C1
BUS12 (SPI): SPI
BUS13 (GPIO): 4 GPIOs

Guidelines:
Only allow PC104 flexibility:
(Do not use these channels to share devices)
BUS10
BUS11
BUS12

Allow PC104 flexibility and device sharing:
BUS13 - Dedicated use of PC104.

Title: OBDH Interface			UFSC - SpaceLab University Campus - Trindade Dep. of Electrical Engineering - CTC Florianópolis, Santa Catarina, Brazil CEP: 88040 - 900
Size: A3	Project: FloripaSat	Revision: V0.3	
Date: 20/08/2020	Time: 17:59:39	Sheet 1 of 6	
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	

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Analog_Circuits
4_Analog_Circuits.SchDoc

WATCHDOG_SIGNALS
ADC_READINGS
VREF
OBDH_AVCC
ANTENNA_VCC
COMMON_VCC
OBDH_DVCC

Analog Circuits Info:
- Watchdog: Maximum timeout of 1.6 seconds and minimum voltage of 2.9V.
- Sensors: Voltage and Current.
- Voltage reference: 3V reference for ADC.
- Noise/Isolation: Decoupling capacitors and ferrites.

- Operation Check:
Watchdog: Violate the timeout and voltage thresholds.
Sensors: Analyse the TP6 and TP7 voltage.
Voltage reference: Check the 3V output.

MCU_OBDH
3_MCU_Main.SchDoc

WATCHDOG_SIGNALS
ADC_READINGS
VREF
OBDH_AVCC
ANTENNA_VCC
COMMON_VCC
OBDH_DVCC
DAUGHTER_BOARD_SIGNALS
MEMORY_SIGNALS
SPI_BUS
PC104_GPIOs
UART0_BUS
JTAG
I2C0_BUS
I2C1_BUS
I2C2_BUS
UART1_BUS
TTC_SIGNALS
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
ANTENNA_GPIO
OBDH_DVCC

Microcontroller (MSP430F6659):
- Memory: 512kB flash memory and 64kB RAM
- Clock: 2MHz (CPU and peripherals) and 32.768kHz
- Sensors/Monitor: Temperature, Watchdog and voltage monitor
- GPIO/ADC/DAC/USCI Channels:
GPIO: 74 (31 used)
ADC: 12 (5 used)
DAC: 2 (2 used)
USCI: 6 (6 used)

Non Volatile Memory
5_Non_Volatile_Memory.SchDoc

MEMORY_SIGNALS
SPI_BUS
OBDH_DVCC

Memory Info:
- SPI: Standard SPI protocol
- Size: 1Gbits
- Sector Size: 64Kbits
- SubSector Size: 32Kbits
- SubSubSector Size: 4Kbits
- Operation Check:
Perform a read operation to check the manufacturer ID.

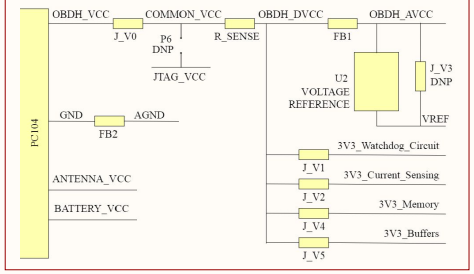
Communication Buffers
6_Communication_Buffers.SchDoc

I2C0_BUS
I2C1_BUS
I2C2_BUS
UART1_BUS
OBDH_DVCC
I2C0_BUS_BUF
I2C1_BUS_BUF
I2C2_BUS_BUF
RS485_BUS

Buffers/Transceiver Info:
- I2C Buffers: Isolate (only logically) master and slave to prevent major problems in case of operation fault.
- RS485 Transceiver: Convert UART protocol to RS485 (full-duplex).

- Operation Check:
Buffers: Check TP51, TP54 and TP57 voltage level (high indicates properly operation). Also, perform loopbacks to validate completely.
Transceiver: Perform a loopback communication by connecting TX to RX and analyse the waveforms at the oscilloscope (complementary behavior, synchronization and signal quality).

ANTENNA_VCC
COMMON_VCC
OBDH_DVCC



Power Supply Info:

- OBDH_VCC (3V3): From OBDH regulator in the EPS board
- COMMON_VCC (3V3): Common switch to allows JTAG supply
- JTAG_VCC (3V3): From the JTAG debugger

- OBDH_DVCC (3V3): Digital circuits
- OBDH_AVCC (3V3): Analog circuits
- VREF (3V): ADC reference voltage

- ANTENNA_VCC (3V3): From Antenna regulator in the EPS board
- BATTERY_VCC (5V4 - 8V4): Unregulated battery voltage

- GND(0V):Ground
- AGND(0V): Analog Ground

MCU Test Points:

TP1, TP2: JTAG Spy Bi-Wire
TP21, TP22, TP23, TP24: JTAG Default
TP3, TP4, TP5: SPI Channel
TP6: OBDH Current ADC Raw
TP7: OBDH Voltage ADC Raw
TP8: Manual Reset (force reset)
TP9: Watchdog Toggle Pin (timeout)
TP10, TP11, TP12, TP20: MCU GPIOs
TP13: RTCCLK Output
TP16, TP17, TP18, TP25, TP26, TP27: USB
TP19: DAC Channel
TP28, TP29, TP30: Main Radio GPIOs
TP31: Main Radio RESET
TP32: Main Radio ENABLE
TP33: Main Radio Chip Select
TP34: TTC Chip Select
TP35, TP36, TP37: Daughter Board GPIO/DAC/ADC
TP38, TP39: Daughter Board Chip Selects
TP40, TP41: Payload Logical Enable

Analog Circuits Test Points:

TP42: OBDH_DVCC
TP43: OBDH_AVCC
TP44: ANTENNA_VCC
TP45: VREF
TP46: COMMON_VCC

Memory Test Points:

TP47: Memory Chip Select
TP48: Write Protection
TP49: Memory Hold
TP50: Memory Reset

Communication Test Points:

TP68,TP69: I2C0 From MCU
TP51: Ready Flag From Buffer 0
TP58,TP59: I2C0 From Buffer 0

TP52,TP53: I2C1 From MCU
TP54: Ready Flag From Buffer 1
TP60,TP61: I2C1 From Buffer 1

TP55,TP56: I2C2 From MCU
TP57: Ready Flag From Buffer 2
TP62,TP63: I2C2 From Buffer 2

TP64,TP65,TP66,TP67: RS485

Title: **OBDH Topology**			*UFSC - SpaceLab* *University Campus - Trindade* *Dep. of Electrical Engineering - CTC* *Florianópolis, Santa Catarina, Brazil* *CEP: 88040 - 900*
Size: A3	Project: FloripaSat	Revision: V0.3	
Date: 20/08/2020	Time: 17:59:39	Sheet 2 of 6	
Drawn by: André M. P. Mattos		Model: Eng_2_ALT	

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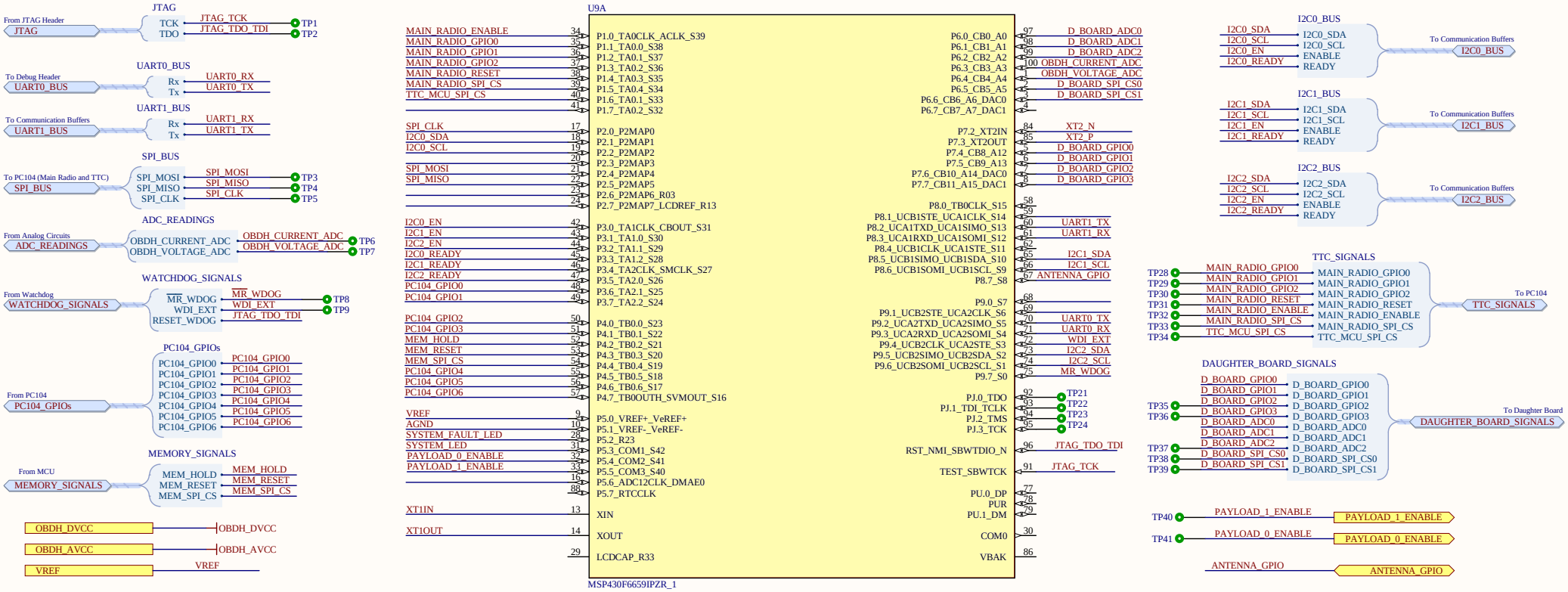
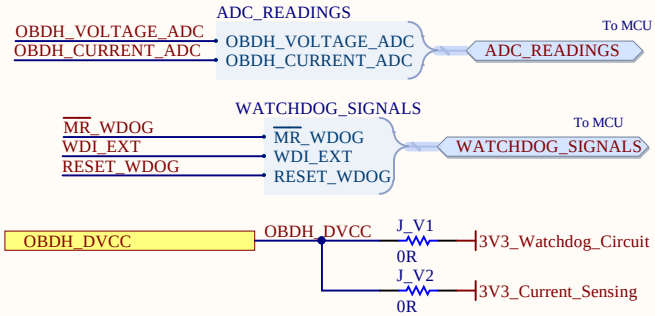
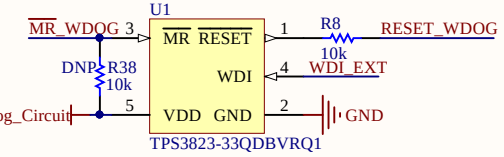

JTAG
From JTAG Header
JTAG
TCK
TDO
JTAG_TCK
JTAG_TDO_TDI
TP1
TP2
UART0_BUS
To Debug Header
UART0_BUS
Rx
Tx
UART0_RX
UART0_TX
UART1_BUS
To Communication Buffers
UART1_BUS
Rx
Tx
UART1_RX
UART1_TX
SPI_BUS
To PC104 (Main Radio and TTC)
SPI_BUS
SPI_MOSI
SPI_MISO
SPI_CLK
TP3
TP4
TP5
ADC_READINGS
From Analog Circuits
ADC_READINGS
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
TP6
TP7
WATCHDOG_SIGNALS
From Watchdog
WATCHDOG_SIGNALS
MR_WDOG
WDI_EXT
RESET_WDOG
JTAG_TDO_TDI
TP8
TP9
PC104_GPIOs
From PC104
PC104_GPIOs
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
PC104_GPIO4
PC104_GPIO5
PC104_GPIO6
MEMORY_SIGNALS
From MCU
MEMORY_SIGNALS
MEM_HOLD
MEM_RESET
MEM_SPI_CS
OBDH_DVCC
OBDH_AVCC
VREF
U9A
MAIN_RADIO_ENABLE
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
SPI_CLK
I2C0_SDA
I2C0_SCL
SPI_MOSI
SPI_MISO
I2C0_EN
I2C1_EN
I2C2_EN
I2C0_READY
I2C1_READY
I2C2_READY
PC104_GPIO0
PC104_GPIO1
PC104_GPIO2
PC104_GPIO3
PC104_GPIO4
PC104_GPIO5
PC104_GPIO6
VREF
AGND
SYSTEM_FAULT_LED
SYSTEM_LED
PAYLOAD_0_ENABLE
PAYLOAD_1_ENABLE
XT1IN
XT1OUT
P1.0_TA0CLK_ACLK_S39
P1.1_TA0.0_S38
P1.2_TA0.1_S37
P1.3_TA0.2_S36
P1.4_TA0.3_S35
P1.5_TA0.4_S34
P1.6_TA0.1_S33
P1.7_TA0.2_S32
P2.0_P2MAP0
P2.1_P2MAP1
P2.2_P2MAP2
P2.3_P2MAP3
P2.4_P2MAP4
P2.5_P2MAP5
P2.6_P2MAP6_R03
P2.7_P2MAP7_LCDREF_R13
P3.0_TA1CLK_CBOUT_S31
P3.1_TA1.0_S30
P3.2_TA1.1_S29
P3.3_TA1.2_S28
P3.4_TA2CLK_SMCLK_S27
P3.5_TA2.0_S26
P3.6_TA2.1_S25
P3.7_TA2.2_S24
P4.0_TB0.0_S23
P4.1_TB0.1_S22
P4.2_TB0.2_S21
P4.3_TB0.3_S20
P4.4_TB0.4_S19
P4.5_TB0.5_S18
P4.6_TB0.6_S17
P4.7_TB0OUTH_SVMOUT_S16
P5.0_VREF+_VeREF+
P5.1_VREF-_VeREF-
P5.2_R23
P5.3_COM1_S42
P5.4_COM2_S41
P5.5_COM3_S40
P5.6_ADC12CLK_DMAE0
P5.7_RTCCLK
XIN
XOUT
LCDCAP_R33
P6.0_CB0_A0
P6.1_CB1_A1
P6.2_CB2_A2
P6.3_CB3_A3
P6.4_CB4_A4
P6.5_CB5_A5
P6.6_CB6_A6_DAC0
P6.7_CB7_A7_DAC1
P7.2_XT2IN
P7.3_XT2OUT
P7.4_CB8_A12
P7.5_CB9_A13
P7.6_CB10_A14_DAC0
P7.7_CB11_A15_DAC1
P8.0_TB0CLK_S15
P8.1_UCB1STE_UCA1CLK_S14
P8.2_UCA1TXD_UCA1SIMO_S13
P8.3_UCA1RXD_UCA1SOMI_S12
P8.4_UCB1CLK_UCA1STE_S11
P8.5_UCB1SIMO_UCB1SDA_S10
P8.6_UCB1SOMI_UCB1SCL_S9
P8.7_S8
P9.0_S7
P9.1_UCB2STE_UCA2CLK_S6
P9.2_UCA2TXD_UCA2SIMO_S5
P9.3_UCA2RXD_UCA2SOMI_S4
P9.4_UCB2CLK_UCA2STE_S3
P9.5_UCB2SIMO_UCB2SDA_S2
P9.6_UCB2SOMI_UCB2SCL_S1
P9.7_S0
PJ.0_TDO
PJ.1_TDI_TCLK
PJ.2_TMS
PJ.3_TCK
RST_NMI_SBWTDIO_N
TEST_SBWTCK
PU.0_DP
PUR
PU.1_DM
COM0
VBAK
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
OBDH_CURRENT_ADC
OBDH_VOLTAGE_ADC
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
XT2_N
XT2_P
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
UART1_TX
UART1_RX
I2C1_SDA
I2C1_SCL
ANTENNA_GPIO
UART0_TX
UART0_RX
WDI_EXT
I2C2_SDA
I2C2_SCL
MR_WDOG
TP21
TP22
TP23
TP24
JTAG_TDO_TDI
JTAG_TCK
MSP430F6659IPZR_1
I2C0_BUS
I2C0_SDA
I2C0_SCL
I2C0_EN
I2C0_READY
ENABLE
READY
To Communication Buffers
I2C0_BUS
I2C1_BUS
I2C1_SDA
I2C1_SCL
I2C1_EN
I2C1_READY
ENABLE
READY
To Communication Buffers
I2C1_BUS
I2C2_BUS
I2C2_SDA
I2C2_SCL
I2C2_EN
I2C2_READY
ENABLE
READY
To Communication Buffers
I2C2_BUS
TTC_SIGNALS
TP28
TP29
TP30
TP31
TP32
TP33
TP34
MAIN_RADIO_GPIO0
MAIN_RADIO_GPIO1
MAIN_RADIO_GPIO2
MAIN_RADIO_RESET
MAIN_RADIO_ENABLE
MAIN_RADIO_SPI_CS
TTC_MCU_SPI_CS
To PC104
TTC_SIGNALS
DAUGHTER_BOARD_SIGNALS
TP35
TP36
TP37
TP38
TP39
D_BOARD_GPIO0
D_BOARD_GPIO1
D_BOARD_GPIO2
D_BOARD_GPIO3
D_BOARD_ADC0
D_BOARD_ADC1
D_BOARD_ADC2
D_BOARD_SPI_CS0
D_BOARD_SPI_CS1
To Daughter Board
DAUGHTER_BOARD_SIGNALS
TP40
TP41
PAYLOAD_1_ENABLE
PAYLOAD_0_ENABLE
ANTENNA_GPIO
JTAG COMPONENTS
OBDH_DVCC
R1
47k
JTAG_TDO_TDI
C1
1nF/16V
GND
MCU POWER CONNECTIONS
OBDH_AVCC
OBDH_DVCC
U9B
AVCC1
DVCC1
DVCC2
DVCC3
V18
VBAT
VBUS
VCORE
VUSB
DVSS1
DVSS2
DVSS3
AVSS1
AVSS2
AVSS3
VSSU
GND
AGND
0.47uF/50V
C2
MSP430F6659IPZR_1
SYSTEM LEDS
SYSTEM_LED
SYSTEM_FAULT_LED
UART0_TX
UART0_RX
UART1_TX
UART1_RX
R2
R3
R4
R5
R6
R7
330R
DNP
D1
D2
D3
D4
D5
D6
Orange
GND
LEDs Assigment:
- SYSTEM LED (D1): (P5.3) Watchdog reset (blink each second)
- SYSTEM FAULT(D2): (P5.2) Active in case of hardware check routine failure
- UART DEBUG (D3, D4, D5, D6): UART TX and RX operation checks
Communication Assigment and Configuration:
- USCI_A0 - SPI: (Memory, Main Radio, TTC and Daughter board)
Chip Selects:1 Memory, 1 Main radio, 1 TTC and 2 Daugther board
Config: Length - 8bits, Phase - High, Polarity - Low, Endianness - MSB, Data Rate - 400kbps
- USCI_A1 - UART1: (Transceiver RS485)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_A2 - UART0: (Debug)
Config: Baundrate - 115200, Data Bits - 8 bits, Parity - None, Stop Bits - 1
- USCI_B0 - I2C0: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B1 - I2C1: (Buffer I2C)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
- USCI_B2 - I2C2: (Buffer I2C)(Antenna and Daughter Board)
Config: Master, Slave Address Length - 7 bits, Data Rate - 100kbps
All USCIs uses the SMCLK as clock source
MCU CRYSTALS
XT2_N
XT2_P
Y1
32MHz 10ppm
C3
10pF/100V
C4
10pF/100V
C5
12pF/50V
C6
12pF/50V
XT1IN
XT1OUT
Y2
32.768kHz 12.5pF
Clock Configuration:
MCLK: (Master Clock) - 32MHz
MCLK is used by the CPU.
SMCLK: (Subsystem Master Clock) - 32MHz
SMCLK is used by the peripheral modules.
ACLK: (Auxiliary Clock) - 32.768kHz
ACLK used in low power modes. Also, it is a software selectable by individual peripheral modules.
Daughter Board Interface:
- Power Supply:
OBDH_DVCC (3V3), ANTENNA_VCC (3V3), BATTERY_VCC(5V4-8V4)
- Inputs/Outputs:
GPIO0(GPIO/ADC), GPIO1(GPIO/ADC), GPIO2(GPIO/ADC/DAC), GPIO3(GPIO/ADC/DAC)
ADC0(ADC/GPIO), ADC1(ADC/GPIO), ADC2(ADC/GPIO)
- Communication:
SPI (2 chip selects avaliable) and I2C (shared with antenna)
Title
OBDH MCU Main
Size: A3
Project: FloripaSat
Revision: V0.3
Date: 20/08/2020
Time: 17:59:39
Sheet 3 of 6
Drawn by: André M. P. Mattos
Model: Eng_2_ALT
UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900
Cannot open file C:\Users\sara\Google Drive\PCB\patch-256.png

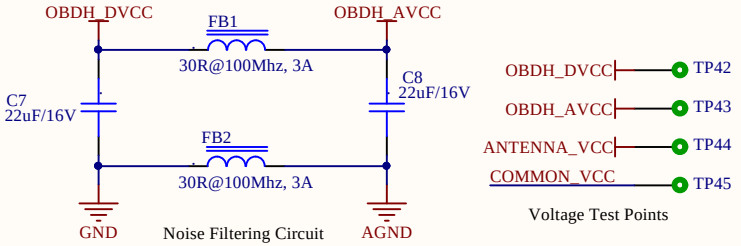


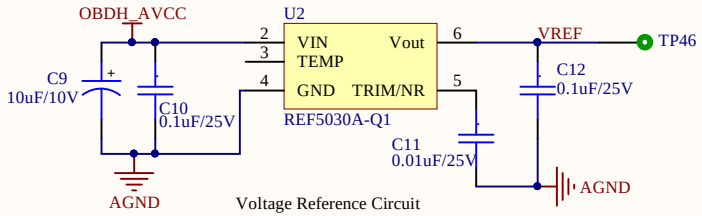
EXTERNAL VOLTAGE MONITOR WITH WATCHDOG TIMER



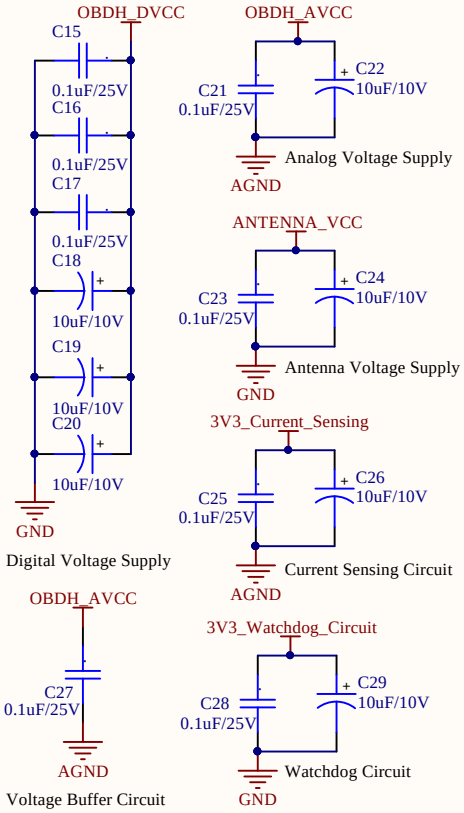
Watchdog Operation:
- MR (Manual Reset): Resets MCU. (Active low)
- RESET: Used by the JTAG interface.
- WDI (Timeout Counter): Resets case any change within 1.6 seconds (typically), both falling and rising edges.
- Resets case the voltage supply drops below 2.9V(typically).

VOLTAGE REFERENCES



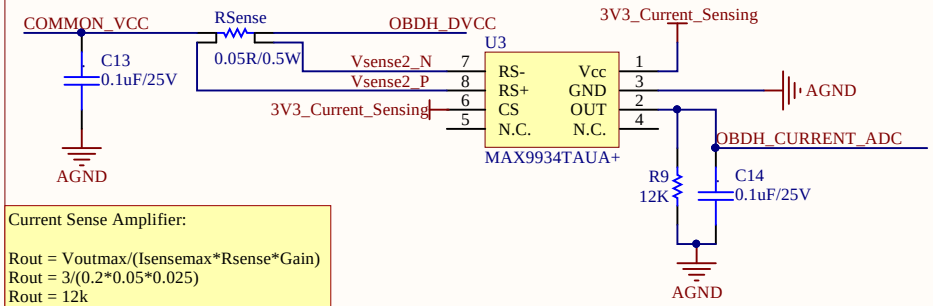


DECOUPLING CAPACITORS



INTERNAL MEASUREMENT CIRCUITS

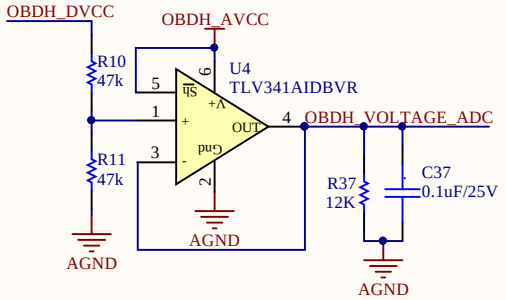
Current Sensing Circuit



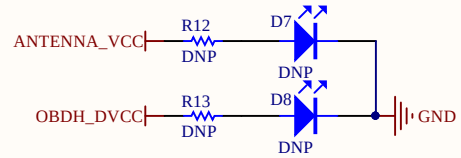
Current Sense Amplifier:

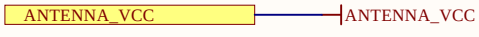
Rout = Voutmax/(Isensemax*Rsense*Gain)
Rout = 3/(0.2*0.05*0.025)
Rout = 12k

Voltage Buffer Circuit



LEDS SYSTEM





Title **Analog Circuits**		
Size: A4	Project: FloripaSat	Revision: V0.3
Date: 20/08/2020 Time: 17:59:40		Sheet 4 of 6
Drawn By: André M. P. Mattos		Model: Eng_2_ALT

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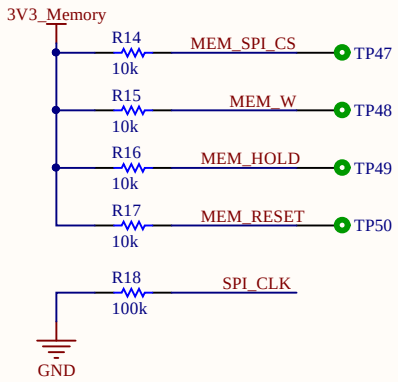
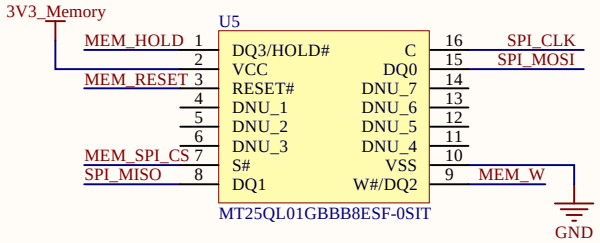
CEP: 88040 - 900

PULL-UP AND PULL-DOWN RESISTORS



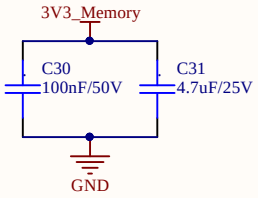
NON-VOLATILE MEMORY

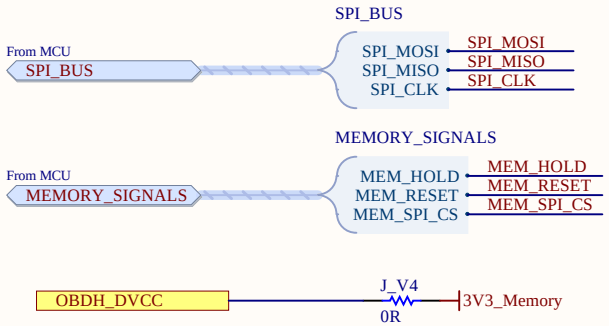


Memory Operation:

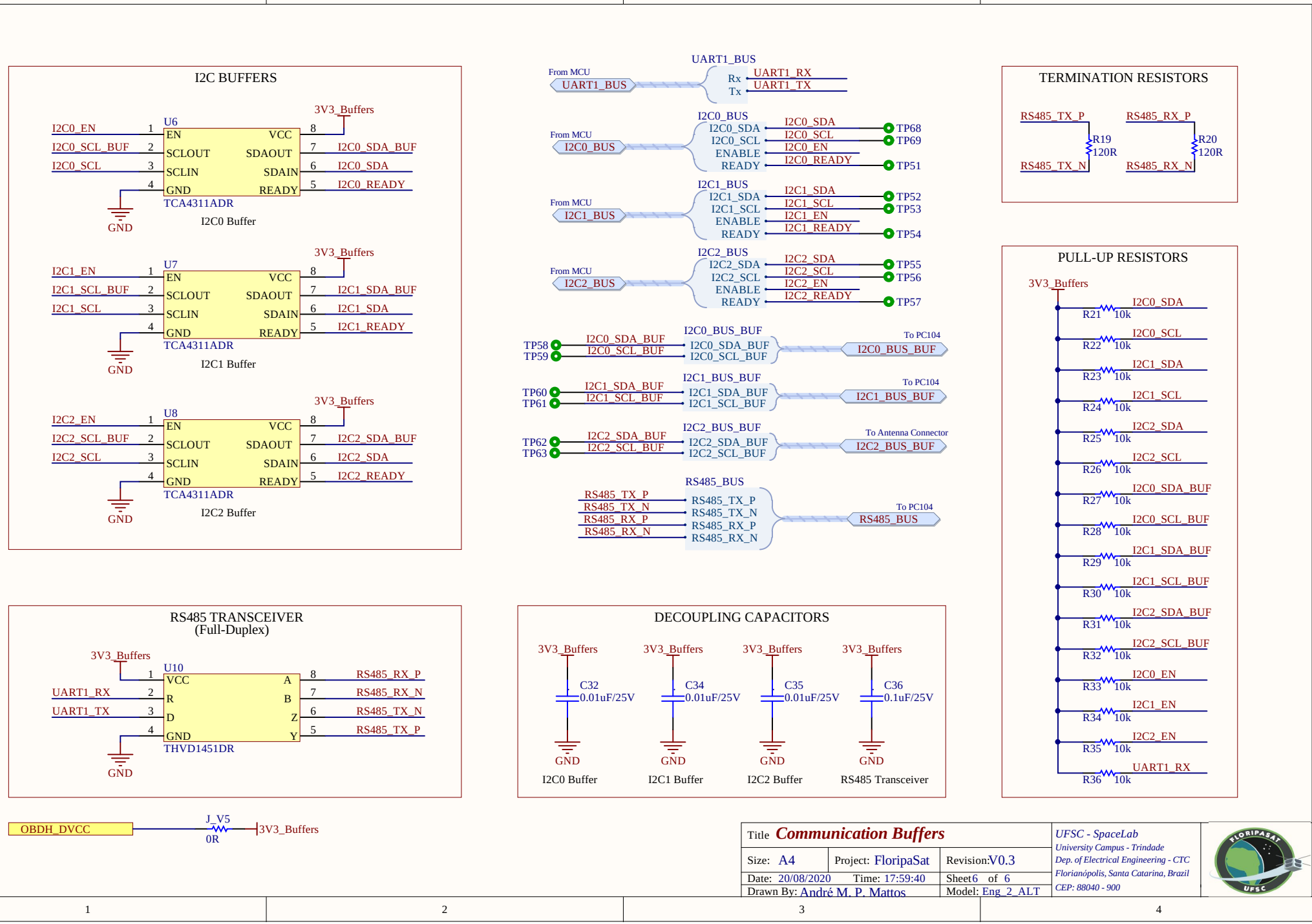
To be defined

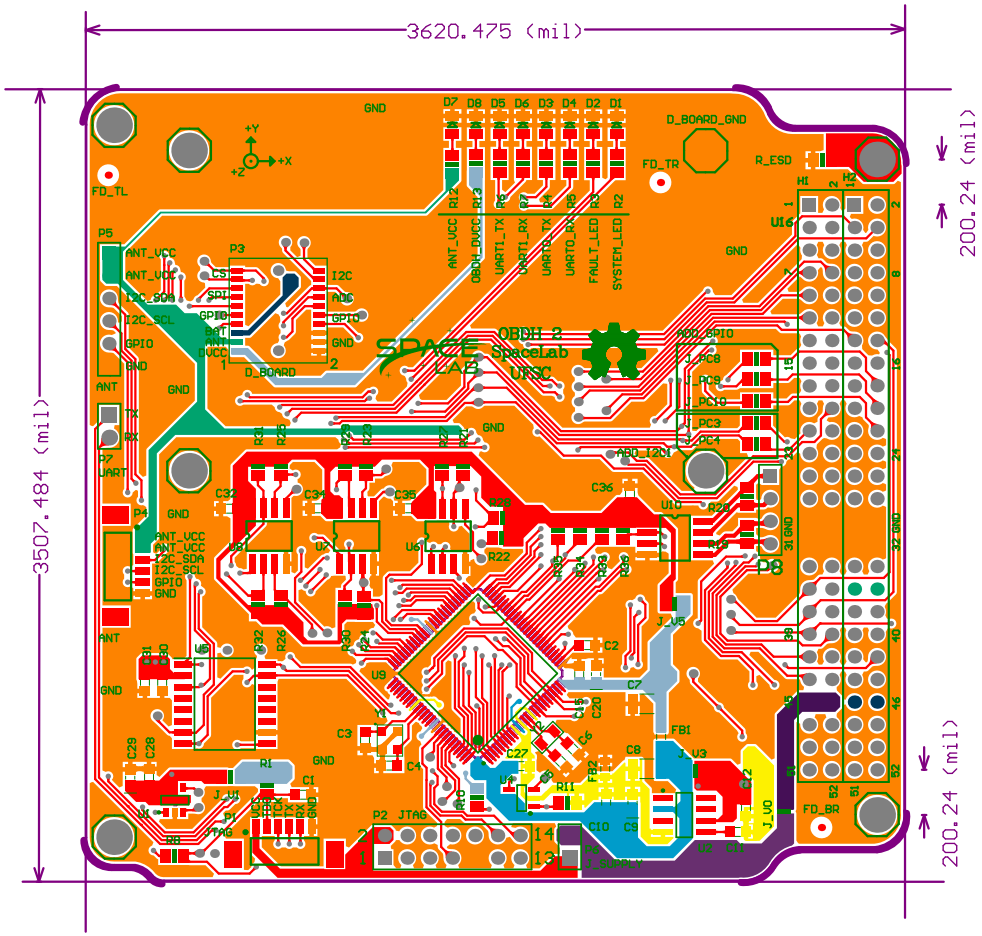
DECOUPLING CAPACITORS





Title **Non Volatile Memory**			*UFSC - SpaceLab*
Size: A4	Project: FloripaSat	Revision:V0.3	*University Campus - Trindade*
Date: 20/08/2020	Time: 17:59:40	Sheet5 of 6	*Dep. of Electrical Engineering - CTC*
Drawn By: André M. P. Mattos		Model: Eng_2_ALT	*Florianópolis, Santa Catarina, Brazil*
			CEP: 88040 - 900

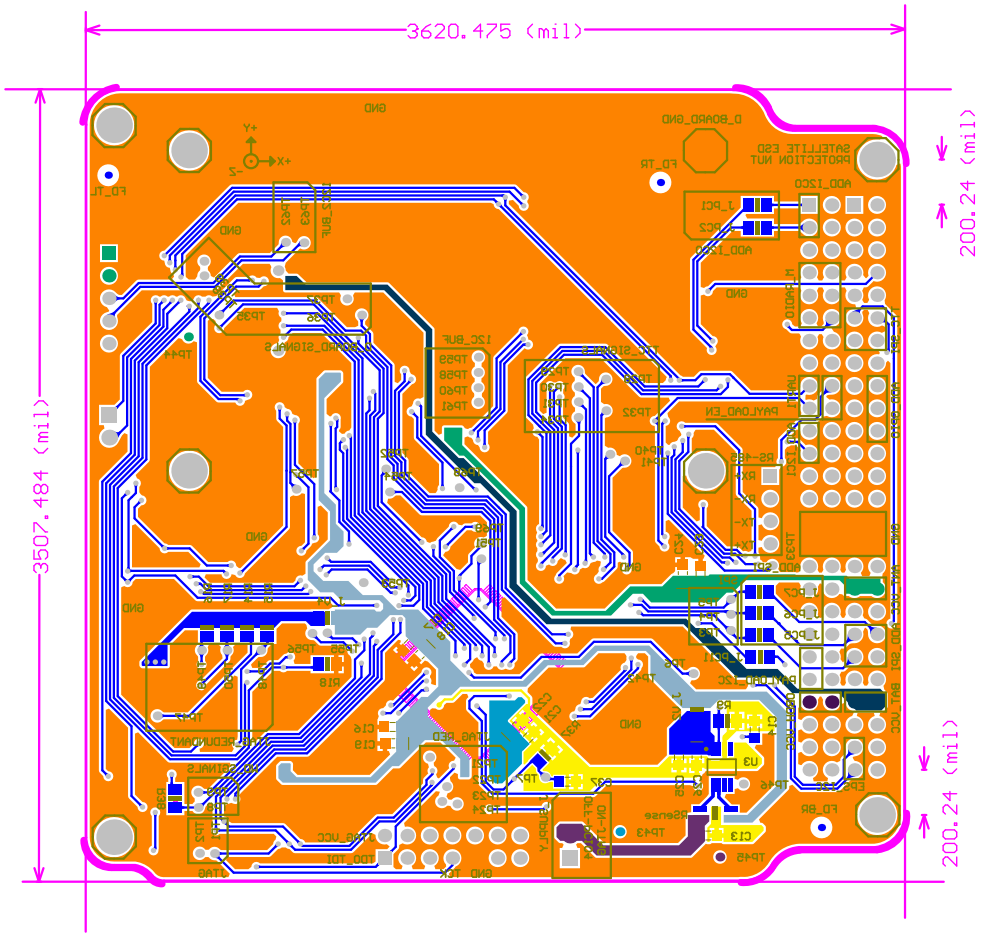

I2C BUFFERS
3V3_Buffers
U6
I2C0_EN
I2C0_SCL_BUF
I2C0_SCL
EN
SCLOUT
SCLIN
GND
VCC
SDAOUT
SDAIN
READY
I2C0_SDA_BUF
I2C0_SDA
I2C0_READY
TCA4311ADR
GND
I2C0 Buffer
U7
I2C1_EN
I2C1_SCL_BUF
I2C1_SCL
I2C1_SDA_BUF
I2C1_SDA
I2C1_READY
I2C1 Buffer
U8
I2C2_EN
I2C2_SCL_BUF
I2C2_SCL
I2C2_SDA_BUF
I2C2_SDA
I2C2_READY
I2C2 Buffer
UART1_BUS
From MCU
UART1_BUS
Rx
Tx
UART1_RX
UART1_TX
I2C0_BUS
I2C0_SDA
I2C0_SCL
ENABLE
READY
TP68
TP69
TP51
I2C1_BUS
I2C1_SDA
I2C1_SCL
I2C1_EN
I2C1_READY
TP52
TP53
TP54
I2C2_BUS
I2C2_SDA
I2C2_SCL
I2C2_EN
I2C2_READY
TP55
TP56
TP57
I2C0_BUS_BUF
TP58
TP59
To PC104
I2C1_BUS_BUF
TP60
TP61
I2C2_BUS_BUF
TP62
TP63
To Antenna Connector
RS485_BUS
RS485_TX_P
RS485_TX_N
RS485_RX_P
RS485_RX_N
TERMINATION RESISTORS
R19
120R
R20
120R
PULL-UP RESISTORS
R21 10k
R22 10k
R23 10k
R24 10k
R25 10k
R26 10k
R27 10k
R28 10k
R29 10k
R30 10k
R31 10k
R32 10k
R33 10k
R34 10k
R35 10k
R36 10k
RS485 TRANSCEIVER
(Full-Duplex)
U10
VCC
R
D
GND
A
B
Z
Y
THVD1451DR
DECOUPLING CAPACITORS
C32
0.01uF/25V
C34
0.01uF/25V
C35
0.01uF/25V
C36
0.1uF/25V
I2C0 Buffer
I2C1 Buffer
I2C2 Buffer
RS485 Transceiver
OBDH_DVCC
J_V5
0R
Title Communication Buffers
Size: A4
Project: FloripaSat
Revision:V0.3
Date: 20/08/2020
Time: 17:59:40
Sheet6 of 6
Drawn By: André M. P. Mattos
Model: Eng_2_ALT
UFSC - SpaceLab
University Campus - Trindade
Dep. of Electrical Engineering - CTC
Florianópolis, Santa Catarina, Brazil
CEP: 88040 - 900



General SPEC:

Cupper base 1OZ:
PCB Material: FR4
PCB Tickness: 1.6mm
PCB Surface: ENIG
Vias: Force Complete Tenting

TITULO: OBDH 2018 UFSC		**REV.** 02	**VER.** Eng_2_ALT
MATERIAL: FR4	**Silkscreen color: green**		
Board Tickness: 1.6mm	**Layers: 02**	**Drawing**	**DATE**
PCB Surface: ENIG		Andre M. P. Mattos	30/04/2020



General SPEC:

Cupper base 1OZ:
PCB Material: FR4
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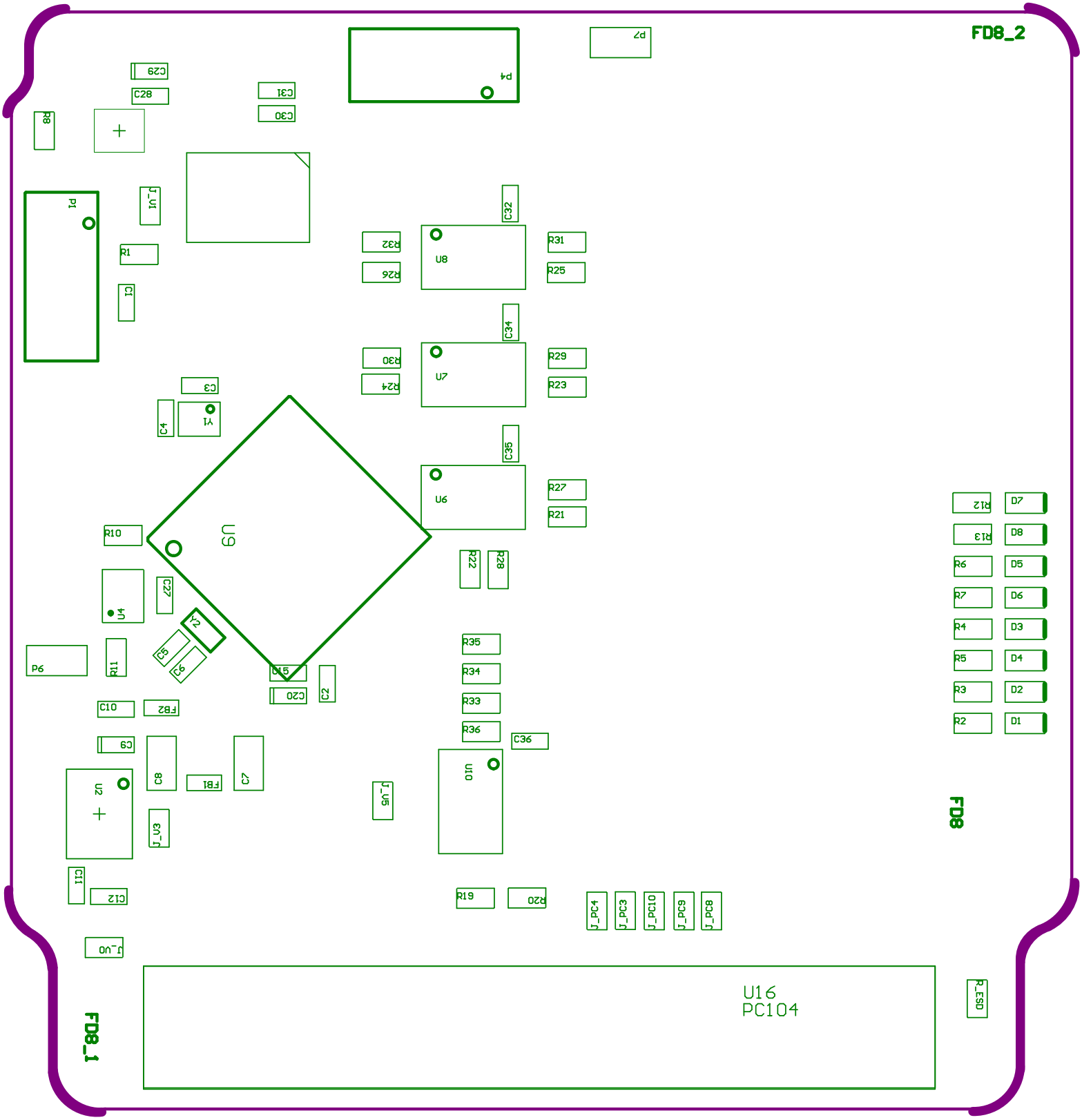
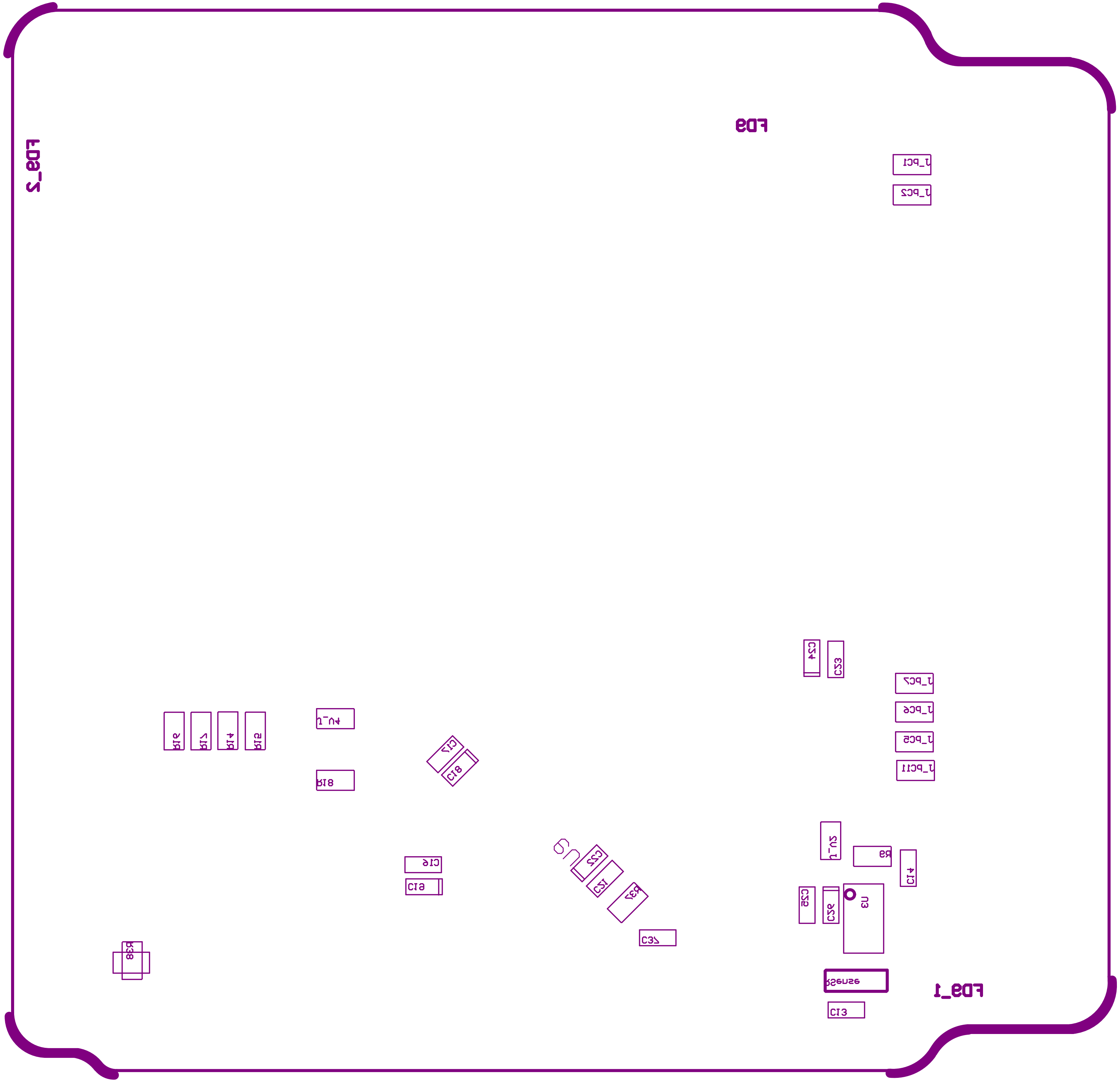
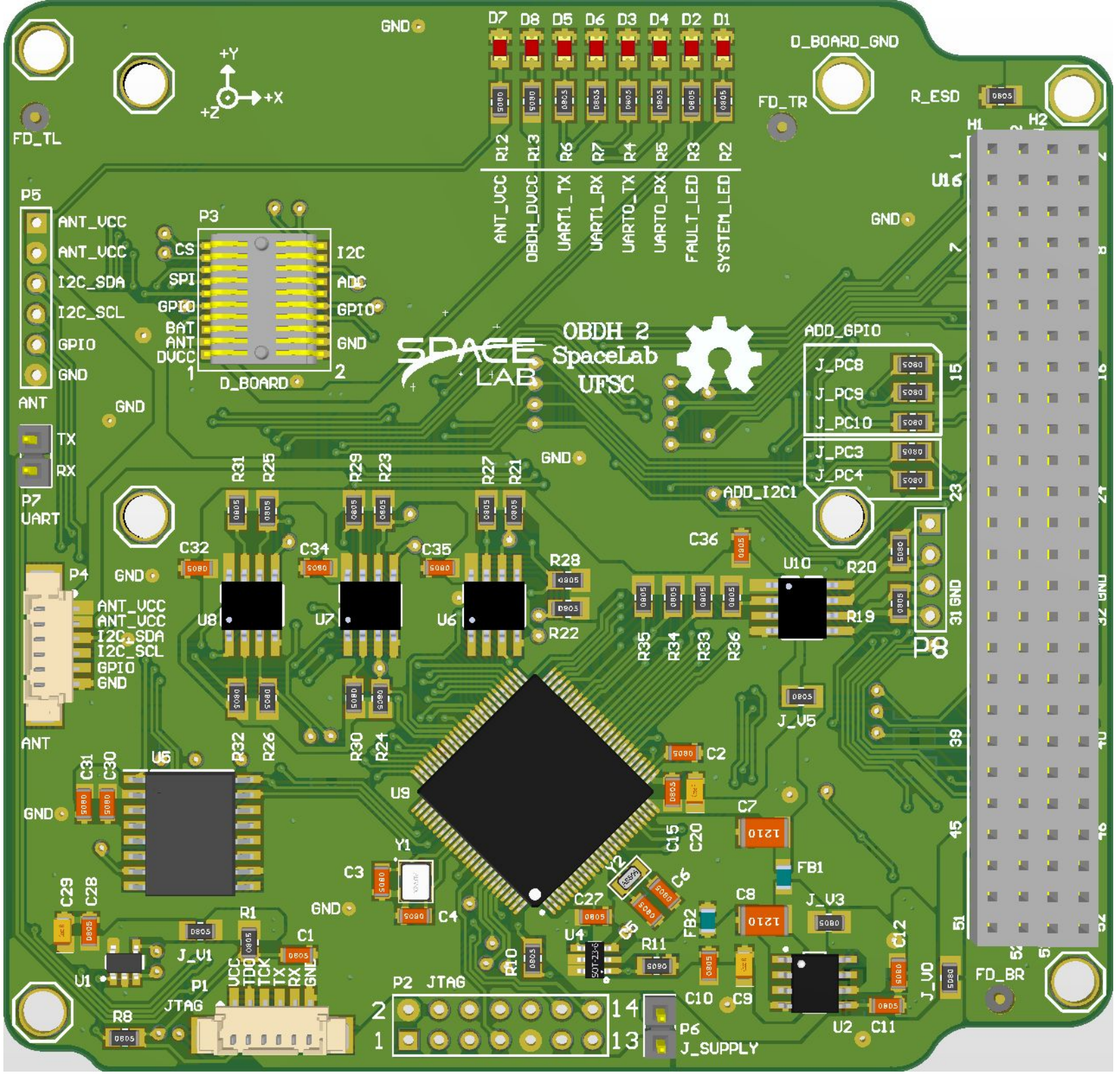
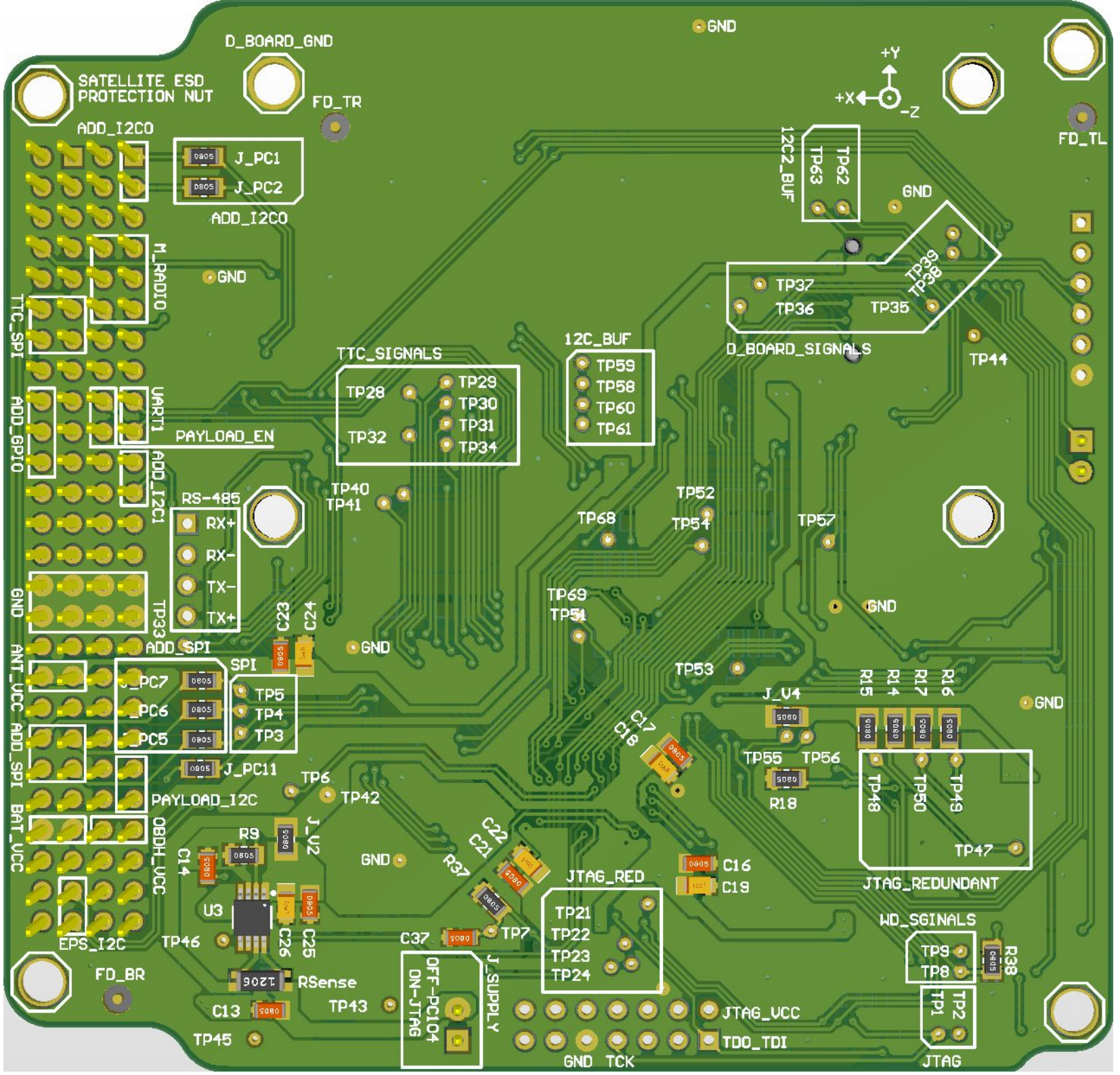
PCB Surface: ENIG
Vias: Force Complete Tenting

TITULO: OBDH 2018 UFSC		**REV.** 02	**VER.** Eng_2_ALT
MATERIAL: FR4	**Silkscreen color: green**		
Board Tickness: 1.6mm	**Layers: 02**	**Drawing**	**DATE**
PCB Surface: ENIG		Andre M. P. Mattos	30/04/2020


FD8_2
P7
P4
C29
C28
C31
C30
R8
J_U1
P1
R1
C1
C32
R32
R26
U8
R31
R25
C34
R30
R24
U7
R29
R23
C3
C4
Y1
C35
U6
R27
R21
U9
R10
R22
R28
U4
C27
Y2
C5
C6
P6
R11
C15
C20
C2
R35
R34
R33
R36
C36
C10
FB2
C9
C8
FB1
C7
U2
U10
J_U5
J_V3
C11
C12
R19
R20
J_PC4
J_PC3
J_PC10
J_PC9
J_PC8
J_U0
FD8_1
U16
PC104
R_ESD
R12
D7
R13
D8
R6
D5
R7
D6
R4
D3
R5
D4
R3
D2
R2
D1
FD8


FD9
FD9_1
FD9_2
C13
C14
C16
C17
C18
C19
C23
C24
C25
C26
C31
C32
C37
R9
R14
R15
R16
R17
R18
R33
R38
U3
RSense


OBDH 2
SpaceLab
UFSC
SPACE LAB
D_BOARD_GND
FD_TR
FD_TL
FD_BR
R_ESD
GND
+Y
+X
+Z
D7 D8 D5 D6 D3 D4 D2 D1
R12 R13 R6 R7 R4 R5 R3 R2
ANT_VCC
OBDH_DVCC
UART1_TX
UART1_RX
UART0_TX
UART0_RX
FAULT_LED
SYSTEM_LED
P5
ANT_VCC
ANT_VCC
I2C_SDA
I2C_SCL
GPIO
GND
ANT
P3
CS
SPI
GPIO
BAT
ANT
DVCC
I2C
ADC
GPIO
GND
D_BOARD
P7
UART
TX
RX
P4
ANT_VCC
ANT_VCC
I2C_SDA
I2C_SCL
GPIO
GND
ANT
ADD_GPIO
J_PC8
J_PC9
J_PC10
J_PC3
J_PC4
ADD_I2C1
P8
GND
U8
U7
U6
U10
U9
U5
U4
U2
U1
P1
JTAG
P2 JTAG
P6
J_SUPPLY
J_V0
J_V1
J_V3
J_V5
H1
H2
U16
Y1
Y2
FB1
FB2


D_BOARD_GND
SATELLITE ESD PROTECTION NUT
FD_TR
GND
+Y
+X
-Z
FD_TL
ADD_I2C0
J_PC1
J_PC2
ADD_I2C0
12C2_BUF
TP63
TP62
GND
TP39
TP38
TP37
TP36
TP35
D_BOARD_SIGNALS
TP44
M_RADIO
GND
TTC_SPI
ADD_GPIO
UART1
PAYLOAD_EN
ADD_I2C1
TTC_SIGNALS
TP28
TP29
TP30
TP31
TP32
TP34
12C_BUF
TP59
TP58
TP60
TP61
TP40
TP41
RS-485
RX+
RX-
TX-
TX+
TP68
TP52
TP54
TP57
GND
ANT_VCC
ADD_SPI
BAT_VCC
TP33
ADD_SPI
C23
C24
GND
TP69
TP51
TP53
SPI
TP5
TP4
TP3
J_PC7
J_PC6
J_PC5
J_PC11
TP6
TP42
PAYLOAD_I2C
OBDH_VCC
C14
R9
J_V2
GND
C22
C21
R37
JTAG_RED
C16
C19
U3
C26
C25
TP46
C37
TP7
EPS_I2C
FD_BR
RSense
C13
TP43
TP45
OFF-PC104
ON-JTAG
J_SUPPLY
TP21
TP22
TP23
TP24
JTAG_VCC
TDO_TDI
GND
TCK
J_V4
R15
R14
R17
R16
GND
C17
C18
TP55
TP56
R18
TP48
TP50
TP49
TP47
JTAG_REDUNDANT
WD_SGINALS
TP9
TP8
R38
TP1
TP2
JTAG