Course Project

Submitted to- DR. Mahindra sakare

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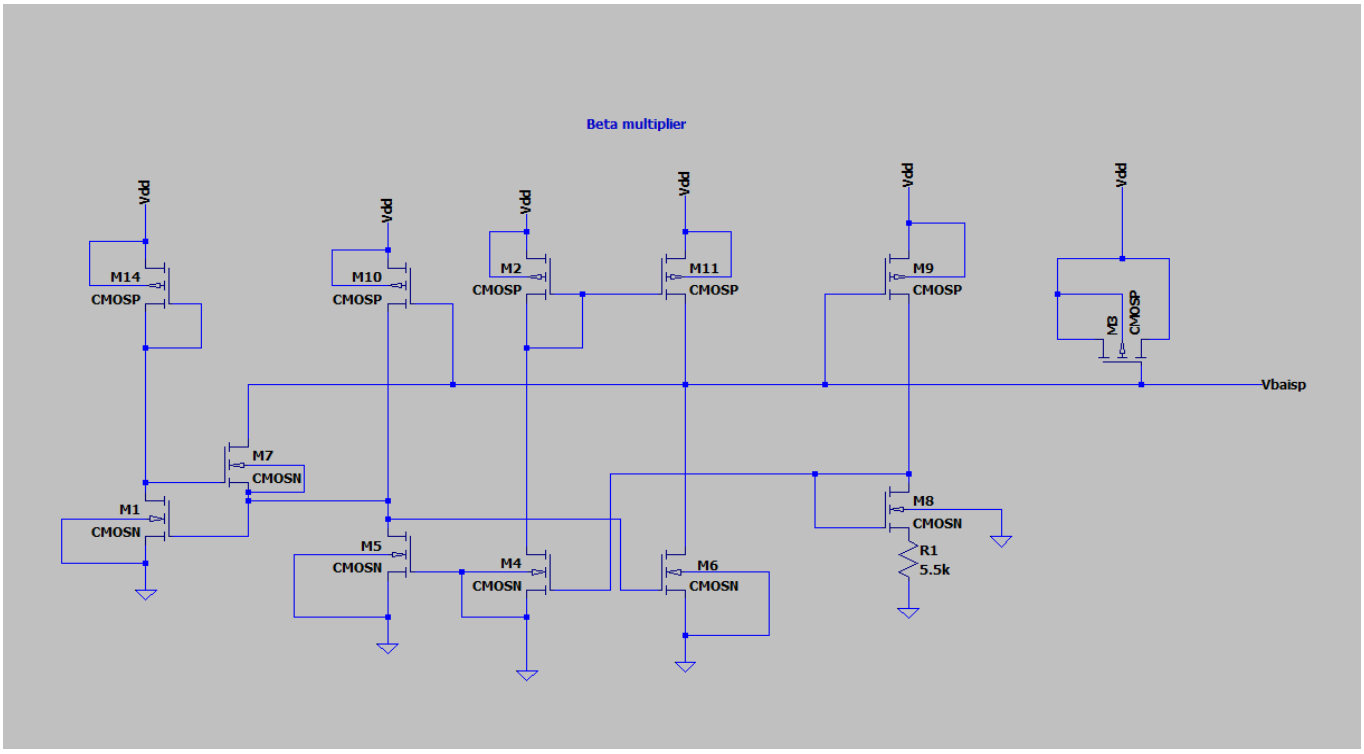
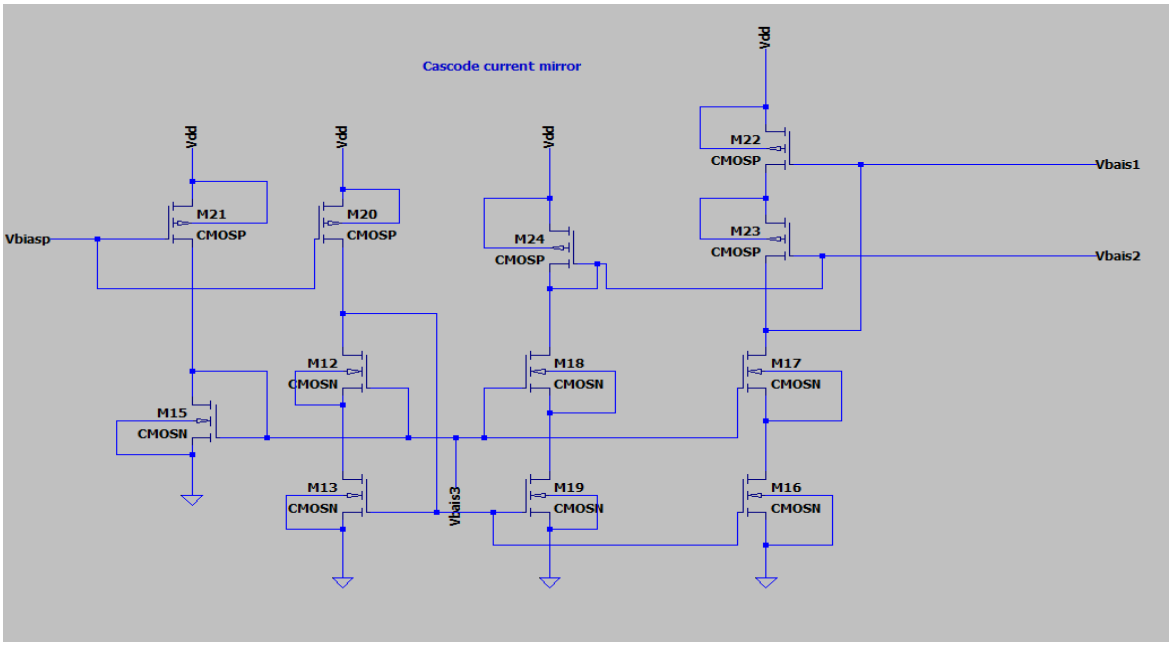
- **Objectives:** Design of cascode amplifier and cascode current mirror in schematic and layout using LT Spice and Magic tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node

180nm Technology

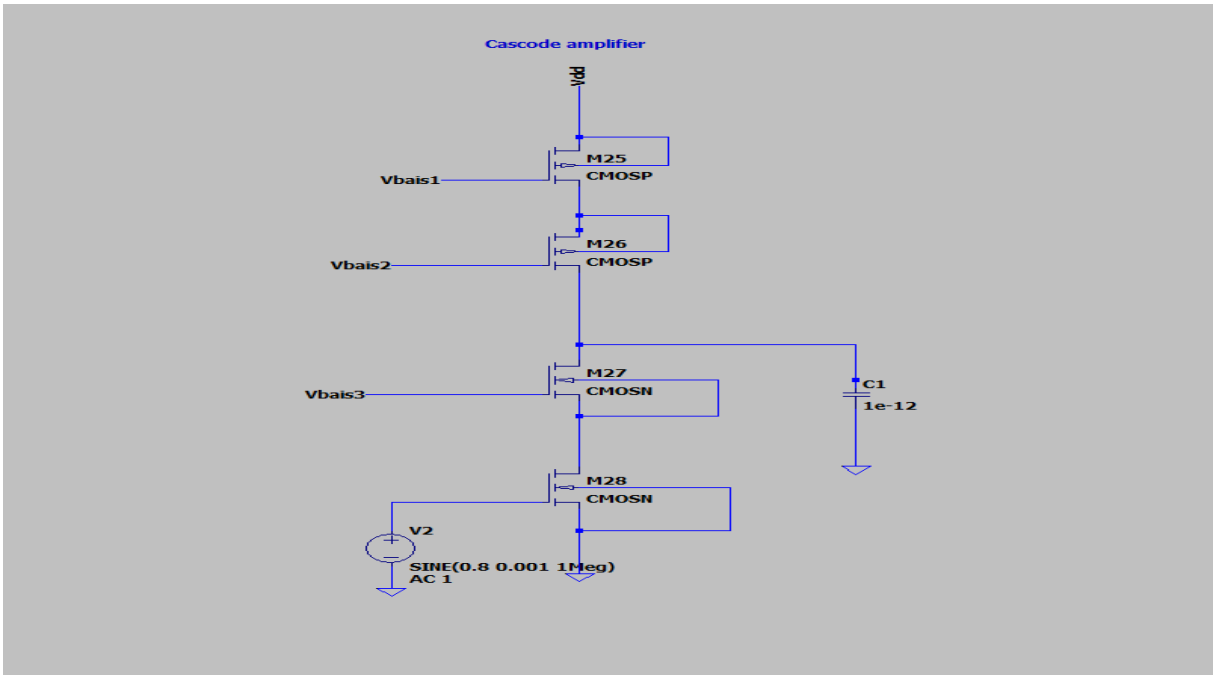
➢ Circuit Diagram:



Beta multiplier LtSpice



Cascode current mirror LtSpice



Cascode Amplifier Ltspice

Calculations:

- UnCox for NMOS = 350.8 uA/V2
- UnC_{ox} for PMOS = 71.2 uA /V^2
- Vdd=1.8V
- A_V=20V/V
- Power dissipation (PD) < 5 mW
- Load Capacitance=1pf
- Unity gain bandwidth>500khz

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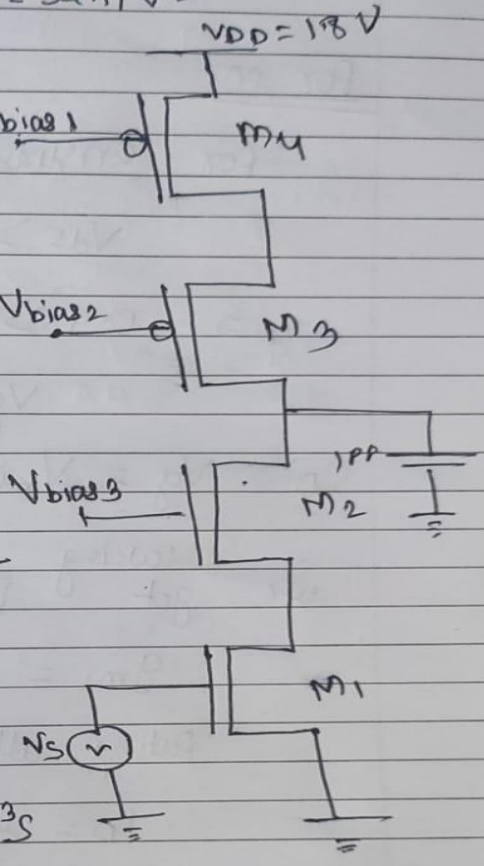
calculation for 180nm

$\mu_n C_{ox}$ for NMOS = $350.8\ \mu A/V^2$
$\mu_n C_{ox}$ for PMOS = $71.2\ \mu A/V^2$



Firstly we assume that Vbias1
Vds for Nmos and PMOS is 400mV

Input Freq = 1MHz

$$F = \frac{1}{2\pi C_L R_{out}}$$

$$R_{out} = \frac{1}{2\pi C_L F} = 159.1\ K\Omega$$

gain Av = $g_m \times R_{out}$

Av = 20 V/V

$$g_m = \frac{20}{R_{out}} = 0.125 \times 10^{-3}\ S$$

$g_m = 0.125 \times 10^{-3}\ S$

The effective gain of cascode amplifier is approximately g_{m1}

$$g_{m_1} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$

for M_1

for ensuring saturation region

$$V_{ds} > V_{gs} - V_{th}$$

$$\Rightarrow 0.4 > V_g - 0.5V$$

$$V_g < 0.9V$$

So $V_g = V_{bias4}$ from fig.

taking a value which satisfies inequality we get $\boxed{V_{bias4} = 0.6V}$

$$g_{m_1} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})$$

puting all value we get $\frac{W}{L} \approx 5/2$

$$I_D = \frac{\mu_n C_{ox} W}{2L} (V_{ov})^2 = 8.58\mu A$$

for M_2

$$V_{ds} > V_{gs} - V_{th}$$

$$0.45 > V_g - 0.4 - 0.5 \quad , \quad \boxed{V_g < 1.3V}$$

$$V_g = V_{bias3}$$

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we get $V_g = V_{bias3} = 1.1V$

equating $I_d = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$

we get $\frac{W}{L} \approx 5/2$

For M4

$V_s = 1.8V$, $V_d = 1.4V$

$V_{sd} > V_{sg} - |V_{th}|$ for pmos

$0.4 > 1.8 - V_g - 0.5$

$V_g > 0.9V$

taking $V_g = V_{bias1} = 1.15V$

we get $\frac{W}{L} \approx \frac{24}{2}$

by equating $I_D = 8.584A$

V_{bias}

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for M3

$V_S = 1.4$, $V_d = 1.0V$

$0.4 > 1.4 - V_g - 0.5$

$V_g > 0.5\,V$

taking $V_g = V_{bias2} = 0.76\,V$

$\frac{W}{L} \approx \frac{24}{2}$

$V_{dd} = 1.8V$

$I_D = 8.5\mu A$

$V_{dd} \cdot I_d < 5mW$

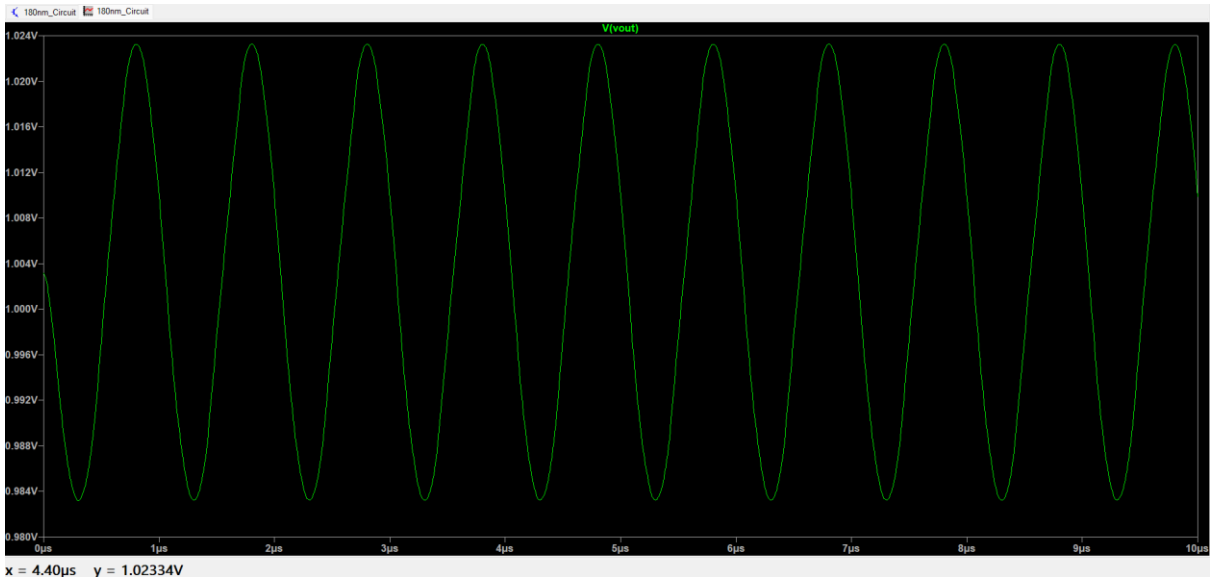


Fig: Voltage Swing

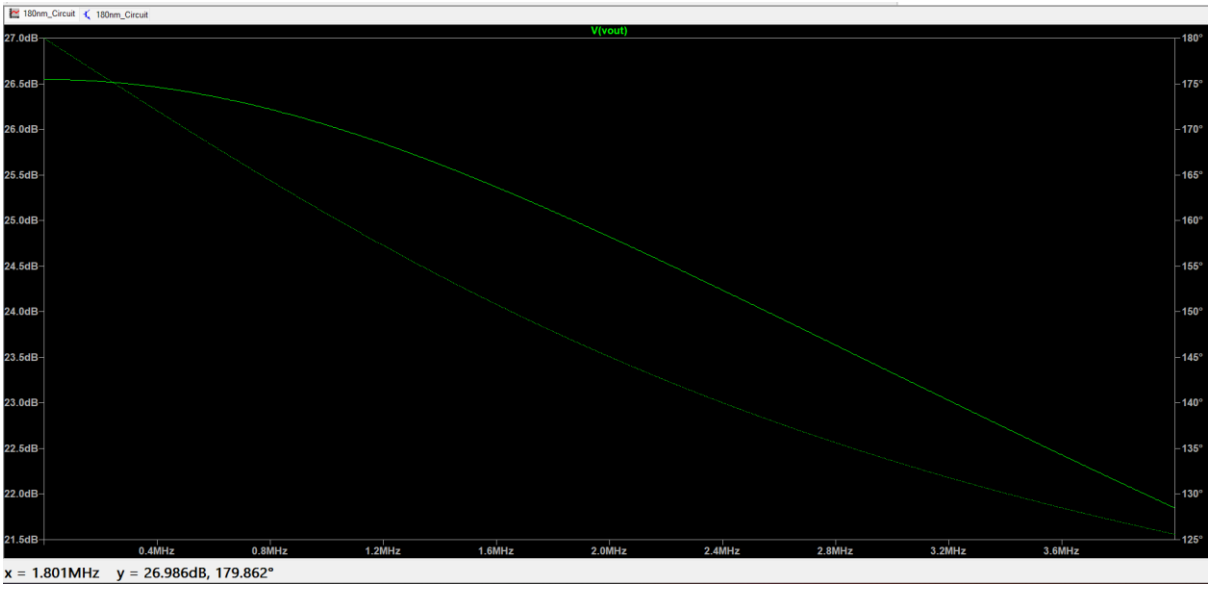
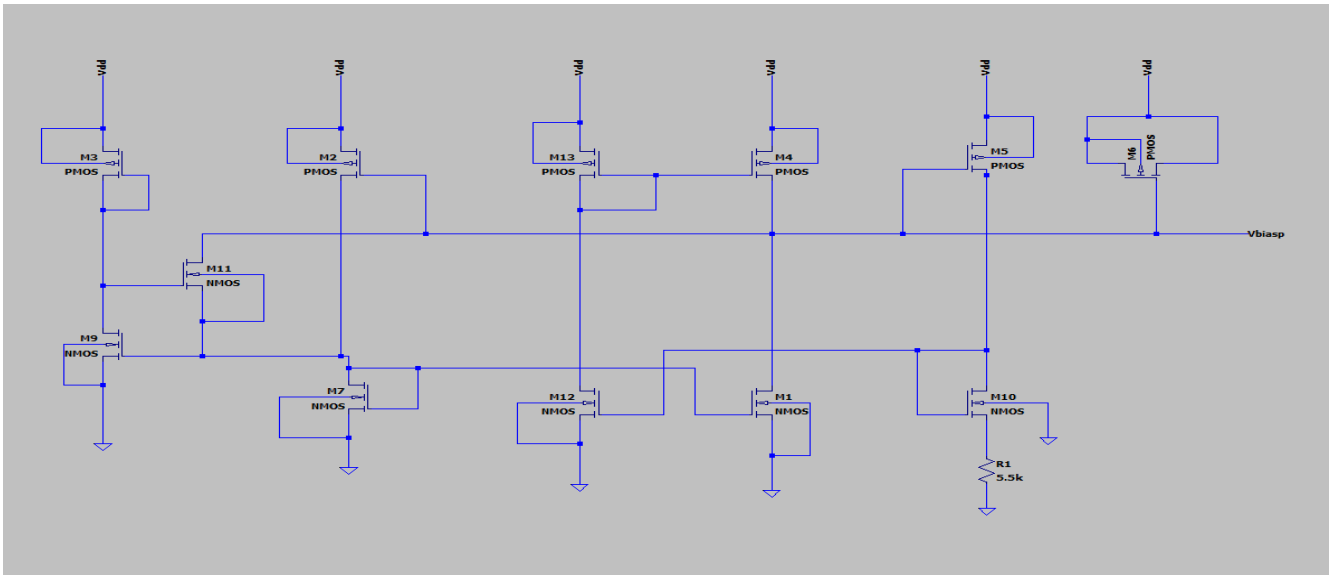


Fig: Frequency Response for 180nm

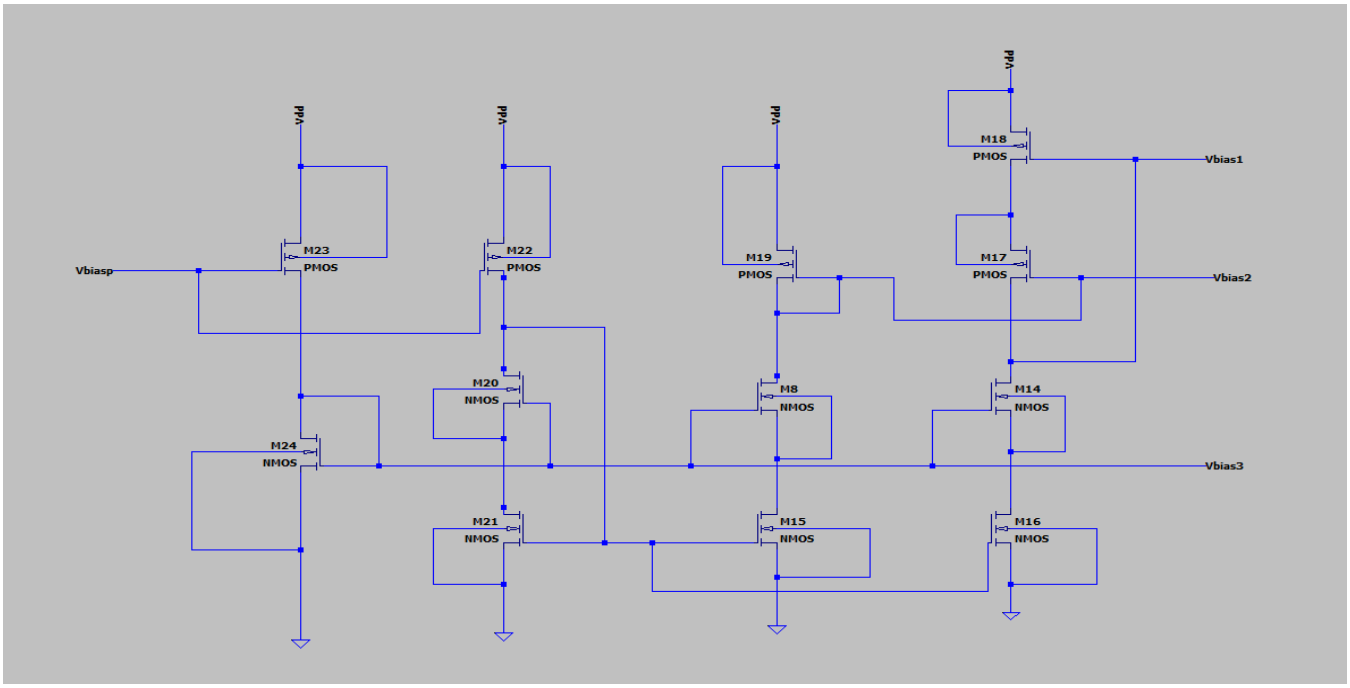
The practical and calculated values of Vbias differ because we used inequalities, and there are certain non-idealities in the circuit that have not been taken into account.

22nm Technology

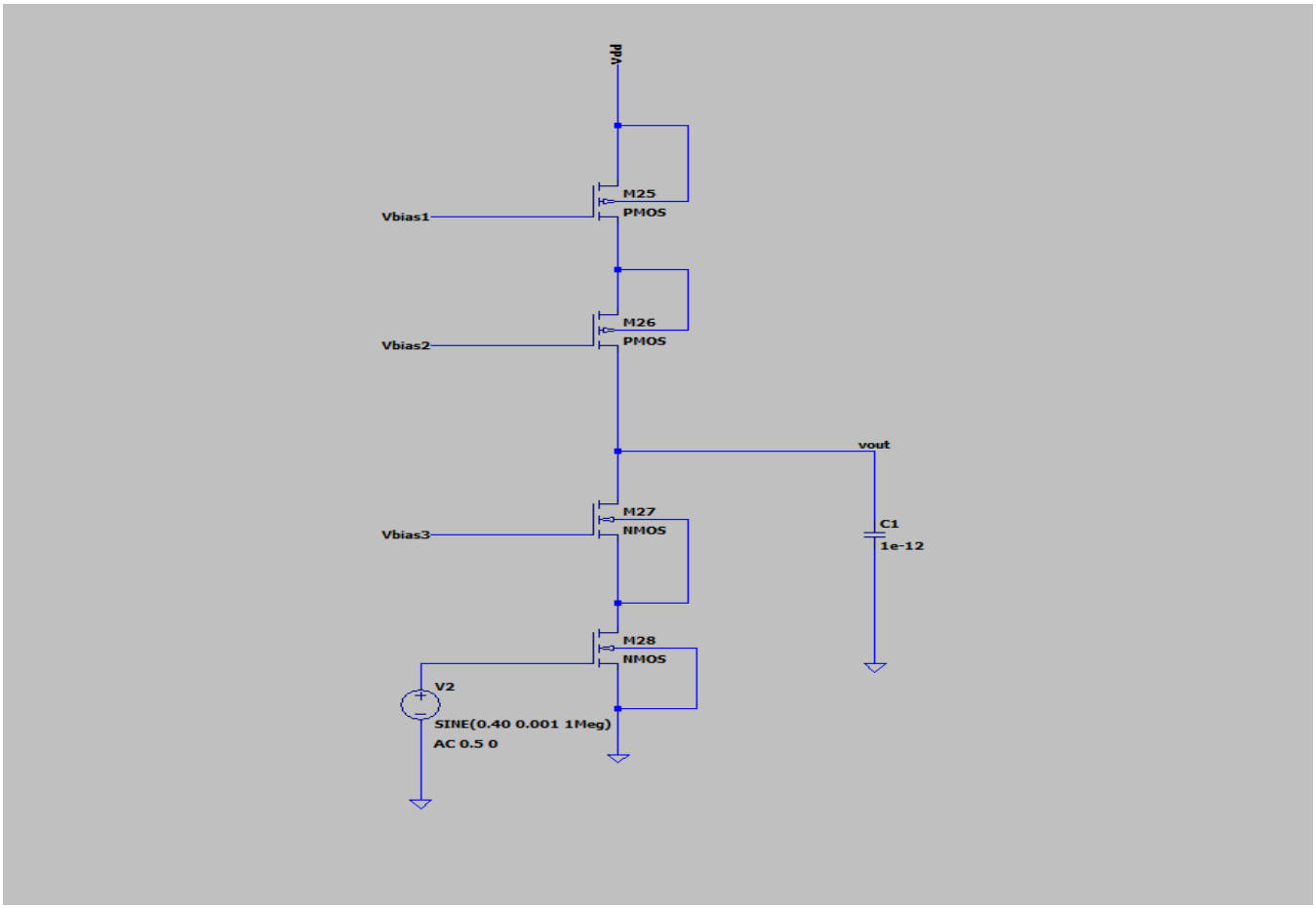
Circuit:



Beta multiplier LtSpice 22nm technology



Current Mirror LtSpice 22nm technology



Cascode LtSpice 22nm technology

Calculations:

→ Provided Data:

- ♦ UnCox for NMOS = 100 uA/V²
- ♦ UnCox for PMOS = 50 uA/V²
- ♦ VDD = 0.8 V
- ♦ AV = 20 V/V
- ♦ Power dissipation (PD) < 5 mW
- ♦ Load Capacitance (CL) = 1 pF
- ♦ Unity Gain Bandwidth(UGB) > 500 KHz.

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For 22nm

given

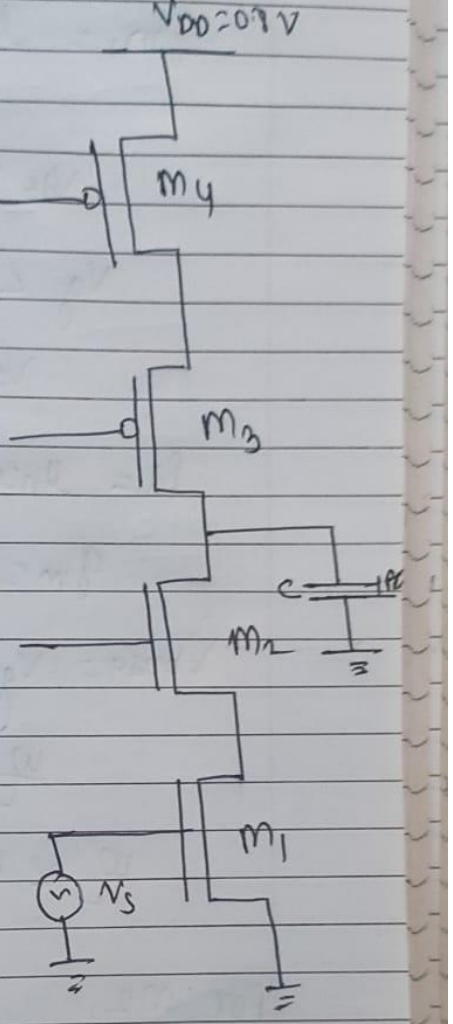
$V_{DD} = 0.9\,V$

$\mu_n C_{ox}$ for NMOS $= 100\,\mu A/V^2$

$\mu_p C_{ox}$ for PMOS $= 50\,\mu A/V^2$

$0.3 < V_{th} < 0.4$

Amplifier $f = 1\,MHz$



Calculation

$$P = \frac{1}{2\pi R_{out} C_L}$$

$$R_{out} = \frac{1}{2\pi f C_L} = 159 \times 10^3 \Omega$$

$R_{out} = 159.15\,K\Omega$

$A_V = g_{meff} \times R_{out}$

$g_{meff} = A_V / R_{out}$

For cascode amplifier $g_{meff} \approx g_{m1}$

$$g_{meff} = \frac{A_V}{R_{out}} = \frac{20}{159.15 \times 10^3} = 0.125 \times 10^{-3}\,S$$

$g_m \approx 0.125\,mS$

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For M1

$g_{m1} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) = 0.125 \times 10^{-3}$

$V_{ds} > V_{gs} - V_{th}$ for saturation

$V_g < 0.2 - 0 + 0.4$ ($V_{ds} = 0.2V$)

$V_g < 0.6V$

$I_d = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2$

$g_m = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) = 0.125 m$

$V_{bias4} = V_g = 0.6V$

$\frac{W}{L} \approx 6.25 = 25/4$

$\frac{W}{L} \approx \frac{25}{4}$ $I_d = 12.5 \mu A$

For M2

$V_{ds} > V_{gs} - V_{th}$

$\Rightarrow 0.2 > V_g - 0.2 - 0.4$

$V_g \leq 0.8$

taking $V_{bias3} = 0.8$

I_{d2}

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$$I_d = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{ov})^2$$

$$\boxed{\frac{W}{L} \simeq \frac{25}{4}}$$

For M4

$V_s = 0.8\,V \quad V_d = 0.6\,V$

$V_{sd} > V_{sg} - |V_{th}|$

$0.2 > 0.8 - V_g - 0.4$

$V_g \geq 0.2\,V$

taking $V_g = 0.2\,V$ we get $\boxed{\frac{W}{L} \simeq \frac{12}{1}}$

For M3

$V_g = 0.6\,V \quad V_d = 0.4\,V$

$V_{sd} > V_{sg} - |V_{th}|$

$0.2 > 0.6 - V_g - 0.4$

$V_g \geq 0$

take $V_g = 0.1 \quad \frac{W}{L} \simeq 7$

$V_{dd} = 0.8\,V$

$f_d = 125\,MHz \quad V_{dd} \cdot f_d < 5mW$

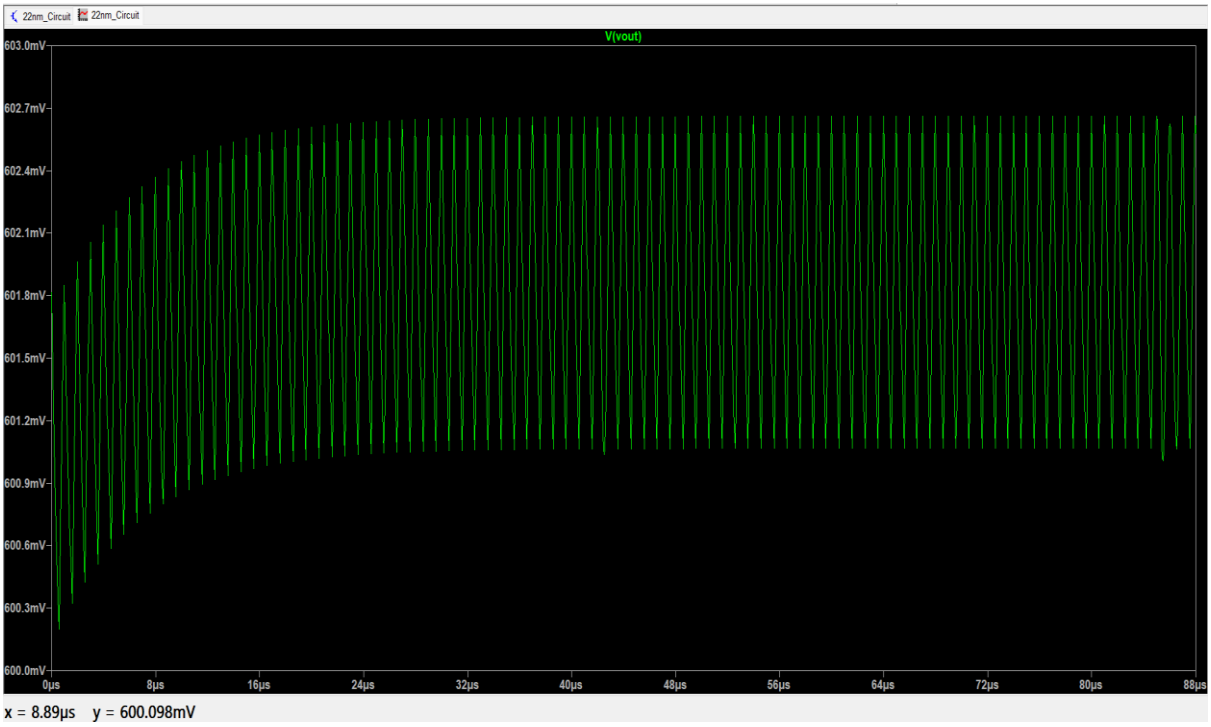


Fig: DC Swing

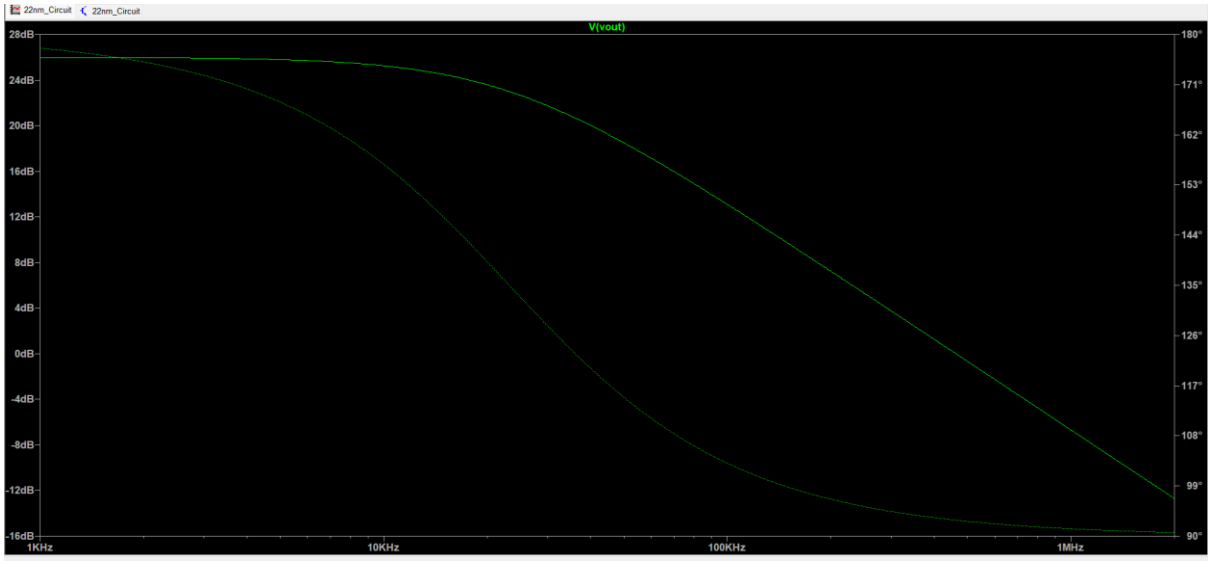
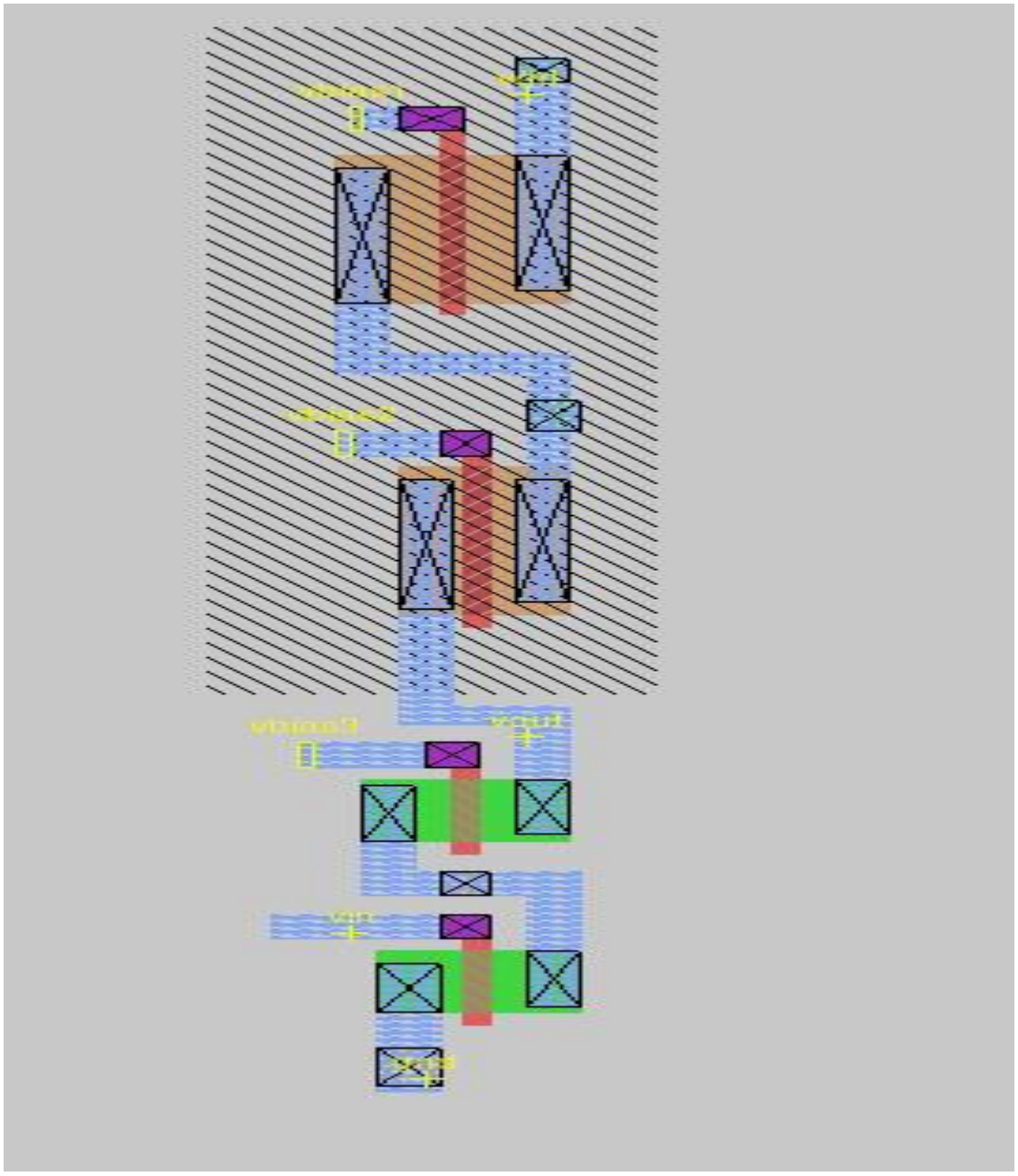


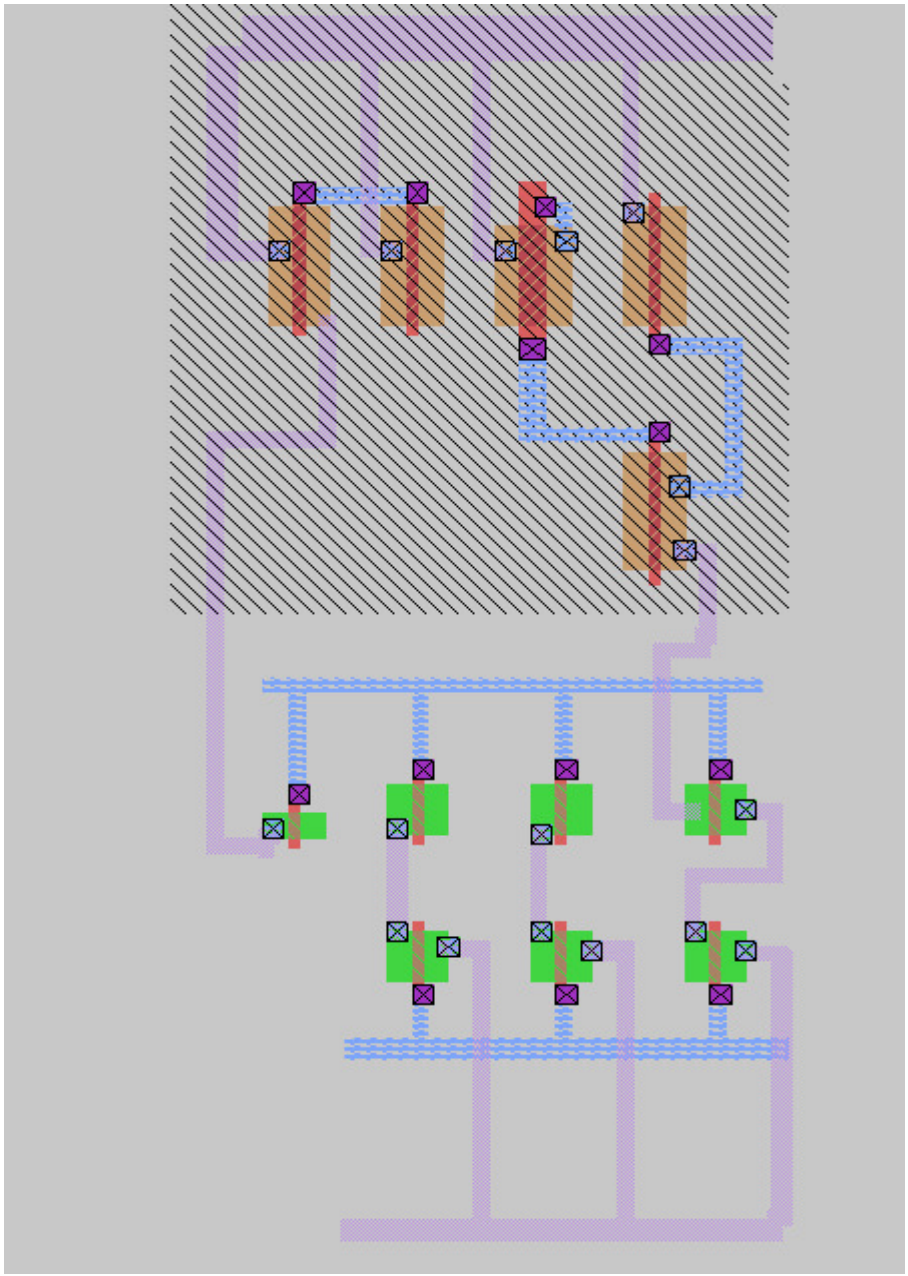
Fig: Frequency Response 22nm technology

The practical and calculated values of Vbias differ because we used inequalities, and there are certain non-idealities in the circuit that have not been taken into account.

➢ Layout in Magic for 180nm:

→ The magic layout was created based on the specified parameters, with each block in the layout representing a dimension of 90 nanometers.
→ Metal 1 was utilized for establishing connections and for providing Vdd and ground connections.
→ Polysilicon was used for forming the gate structure.
→ PD contact, ND contact, and polycontact were also incorporated in the design.
→ The Design Rule Check resulted in a zero violation.





In conclusion, we can affirm that the project successfully achieved the target gain for both 180nm and 22nm technology files while adhering to the specified constraints. This was accomplished in the context of a cascaded amplifier biased through a current mirror and simulated using LT Spice. The layout for the cascode amplifier was created in Magic in accordance with design rules and subsequently transferred to LT Spice for further analysis